INSTRUCTION MANUAL

MODEL 193
20 MHz
SWEEP/MODULATION GENERATOR

WAVETEK

WAVETEK SAN DIEGO, INC.

9045 Balboa Ave., San Diego, CA 92123
P. O. Box 85265, San Diego, CA 92138
Tel 619/279-2200 TWX 910/335-2007

Manual Revision 5/87

WARRANTY

Wavetek warrants that all products manufactured by Wavetek conform to published Wavetek specifications and are free from defects in materials and workmanship for a period of one (1) year from the date of delivery when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Wavetek arising from a Warranty claim shall be limited to repairing, or at its option, replacing without charge, any product which in Wavetek's sole opinion proves to be defective within the scope of the Warranty. In the event Wavetek is not able to modify, repair or replace non-conforming defective parts or components to a condition as warrantied within a reasonable time after receipt thereof, Buyers shall be credited for their value at the original purchase price.

Wavetek must be notified in writing of the defect or nonconformity within the Warranty period and the affected product returned to Wavetek's factory or to an authorized service center within (30) days after discovery of such defect or nonconformity.

For product warranties requiring return to Wavetek, products must be returned to a service facility designated by Wavetek. Buyer shall prepay shipping charges, taxes, duties and insurance for products returned to Wavetek for warranty service. Except for products returned to Buyer from another country, Wavetek shall pay for return of products to Buyer.

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Exclusion of Other Warranties

The Warranty described above is Buyer's sole and exclusive remedy and no other warranty, whether written or oral, is expressed or implied. Wavetek specifically disclaims the implied warranties of merchantability and fitness for a particular purpose. No statement, representation, agreement, or understanding, oral or written, made by an agent, distributor, representative, or employee of Wavetek, which is not contained in the foregoing Warranty will be binding upon Wavetek, unless made in writing and executed by an authorized Wavetek employee. Under no circumstances shall Wavetek be liable for any direct, indirect, special, incidental, or consequential damages, expenses, losses or delays (including loss of profits) based on contract, tort, or any other legal theory.

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SAFETY

This instrument is wired for earth grounding via the facility power wiring. Do not bypass earth grounding with two wire extension cords, plug adapters, etc.

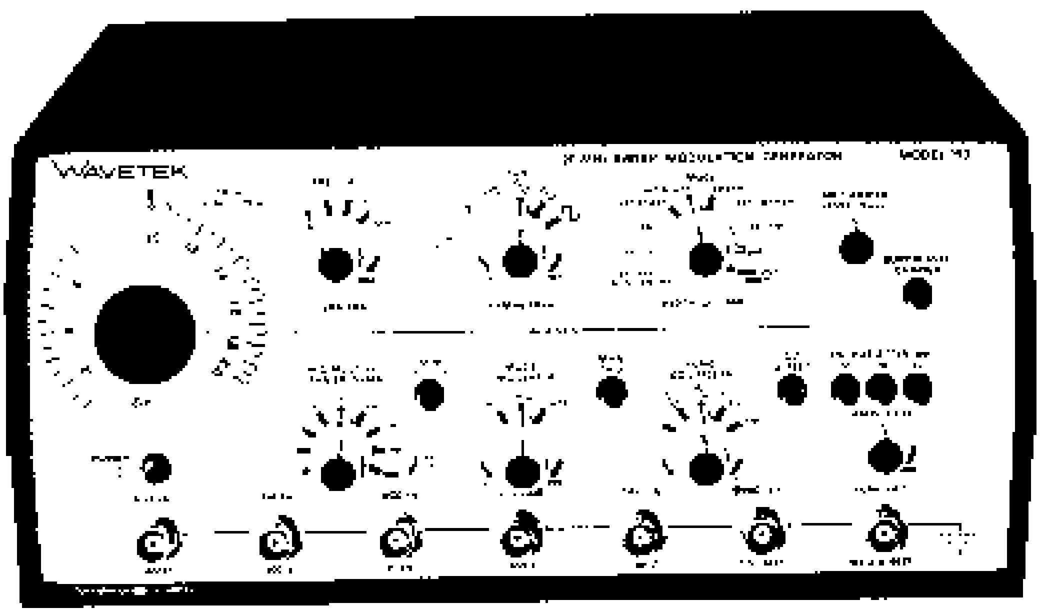
BEFORE PLUGGING IN the instrument, comply with installation instructions.

MAINTENANCE may require power on with the instrument covers removed. This should be done only by qualified personnel aware of the electrical hazards.

The instrument power receptacle is connected to the instrument safety earth terminal with a green/yellow wire. Do not alter this connection. (Reference ⏚ or ⚠ stamped inside the rear panel near the safety earth terminal.)

WARNING notes call attention to possible injury or death hazards in subsequent operations.

CAUTION notes call attention to possible equipment damage in subsequent operations.



Model 183, 20 MHz Sweep/Modulation Generator

SECTION 1
GENERAL DESCRIPTION

1.1 THE MODEL 193

The Wavetek Model 193, a 20 MHz Sweep/Modulation Generator, is a precision source of sine ∿, triangle ∿, square ⊓⊔, AM sine ∞ and dc. All waveforms are front panel variable from 0.002 Hz to 20 MHz and can be internally and externally modulated. Outputs can be continuous, triggered or gated by an external trigger signal or a front panel manual trigger switch. The main generator can be swept, frequency modulated, 0 to 100% amplitude modulated and suppressed carrier modulated using the auxiliary generator or an external source. The auxiliary generator, in addition to being an internal modulation generator, can be used as an independent function generator. Both generators have symmetry control of waveforms and can be frequency modulated by an external signal. Each modulation parameter has a static setup feature to allow its exact selection. Amplitude of the waveforms is variable from 30 Vp-p (15 Vp-p into 50Ω) down to 1.5 mVp-p. DC reference of the waveform can be offset positively or negatively. Maximum 150 mA peak current can be continuously varied over an 80 dB range. A sync output provides a TTL level into 50Ω.

1.2 SPECIFICATIONS

1.2.1 Main Generator

Waveforms
Selectable sine ∿, triangle ∿, square ⊓⊔, AM sine ∞ and dc.

Symmetry
Symmetry of all waveform outputs is continuously adjustable from 1:19 to 19:1*. Varying symmetry provides variable duty-cycle pulses, sawtooth ramps and distorted sine waves.

Operational Modes
Continuous: Generator runs continuously at selected frequency.

Triggered: Generator is quiescent until triggered by external signal or manual trigger, then generates one complete waveform cycle at selected frequency.

Gated: As triggered mode, except output continues for duration of gate signal. Last waveform started is completed.

Frequency Range
0.002 Hz to 20 MHz in nine overlapping decade ranges with 1% of full scale vernier.

Function Output
Waveforms variable to 30 Vp-p (15 Vp-p into 50Ω). Waveforms may be attenuated continuously to 80 dB. 50Ω source impedance.

DC Output and DC Offset
Adjustable between ±15 Vdc (±7.5 Vdc into 50Ω) with signal peak plus dc offset limited to ±15 Vdc (±7.5 Vdc into 50Ω). DC offset and waveform attenuated proportionately 10 dB/step to 70 dB.

Sync Output
TTL level pulse into 50Ω. Duty cycle varies with SYM control. 50Ω source impedance.

GCV Output
0 to +5V open circuit voltage level proportional to main generator frequency. 600Ω source impedance.

AM—Amplitude Modulation
Either an internal signal (AUX GEN), or external signal (AM IN), or internal plus external signals (AUX GEN MODE—AM, main generator FUNC—AM) amplitude modulates the main generator's sine wave in either the 0 to 100% AM or suppressed carrier mode.

AM Input: 5 Vp-p gives 100% modulation 10 Vp-p gives suppressed carrier operation. 600Ω input impedance.

Carrier Level (0 to 100% AM): Adjustable 10 to 50% of full amplitude at function output.

Carrier Null (Suppressed Carrier AM): Adjustable ±2% of full amplitude at function output.

VCG—Voltage Controlled Generator
Up to 1000: 1 frequency change with external 0 to +5V signal. Upper frequency limited to maximum of range.

Slew Rate: 2% of range per μs.

Linearity: ±0.5% thru X100K range; ±5% on X1M and X10M.

Impedance: 10 kΩ.

Trigger Input
Input Range: 1 Vp-p to ±10 V.

Trigger Level Adj.: −5V to +5V.

Impedance: 1.5kΩ shunted by 15 pF.

Pulse Width: 25 ns minimum.

Repetition Rate:

Input	Max Rep Rate
±1V	1 MHz
±2.5V	10 MHz

Frequency Precision

Dial Accuracy
±3% of full scale from X .1 Hz to X 1 MHz range.
±5% of full scale on X 10M range

1.2.2 Amplitude Precision

Sine Frequency Response
< ±0.2 dB all ranges thru X 100K
< ±0.5 dB on X 1M range.
< ±1.5 dB on X 10M range.

Step Attenuator Accuracy
±0.3 dB with 10, 20 and 40 dB
±0.6 dB with 30, 50 and 60 dB
±0.9 dB with 70 dB setting

1.2.3 Waveform Characteristics

Sine Distortion
< 0.5% on X 100, X 1K and X 10K. < 1.0% on X 0.1 to X 100.

All harmonics 30 dB below fundamental on X 100K, X 1M range, and 25 dB below fundamental on X 10M range.

Square Wave
Rise/Fall Time: < 15 ns (10% to 90%)
Total Aberrations: 5% of full amplitude for each waveform peak.

Time Symmetry
Square wave variation from 0.1 to 2 on dial less than: ±1% to 200 kHz. ±10% to 20 MHz.

Triangle Linearity
>99% for 0.002 Hz to 200 kHz.

1.2.4 Auxiliary Generator

Waveforms
Selectable ∿, ∧, ⊓, ⟋| and ⊓_. Symmetry of ⟋ and ⊓_ adjustable 1:19 thru 19:1.*

Frequency Range
0.1Hz to 100 kHz in 4 ranges.*

Auxiliary Output
Waveforms selectable and variable to 10 Vp-p (5V p-p into 600Ω).

Auxiliary Sync Output
Rear panel BNC. TTL level pulse coincident with AUX GEN output. Duty cycle varies with symmetry control.

AUX VCG Input
Rear Panel BNC. Up to 33:1 frequency change with external ±5V signal. Upper frequency limited to maximum of selected range. 11 kΩ input impedance.

1.2.5 Modes of Operation

Internal auxiliary generator used as the modulation source.

FM
Two setup and one operate mode
Set-Freq/Aux-Gen-Off: Disables auxiliary generator for main generator adjustment

Set ΔF: Allows vernier setup of peak deviation. Vernier range is up to ±10% of main generator range

FM: Operate mode

Sweep
Two setup and one operate mode.

Set Start: Allows setup of main generator start frequency.

Set Width: Allows vernier setup of main generator stop frequency.

Sweep: Operate mode

AM
Two setup and one operate mode for double sideband or suppressed carrier operation.

Set Carrier: Allows setup of carrier amplitude.

Set ΔM: Allows the setup of the modulation level.

AM: Operate mode. 0 to 100 % AM or suppressed carrier modulation of main generator by auxiliary generator plus external signal if present at AM IN.

Aux Out Only: Disconnects the modulator for independent operation of auxiliary generator.

1.2.6 General

Stability
Amplitude, frequency and dc offset at FUNC output after 2 hour warmup: ±0.05% for 10 minutes. ±0.25% for 24 hours.

Environmental
Specifications apply at 25°C ±5°C. Operates 0°C to +50°C.

Dimensions
28.6 cm (11¼ in.) wide; 13.3 cm (5¼ in.) high; 28.6 cm (11¼ in.) deep.

Weight

4.6 kg (10 lb) net, 6.4 kg (14 lb) shipping

Power

100/120/220/240V (+5%, −10%), 48 to 66 Hz, ≤70 VA

VA.

NOTE: All specifications apply from 0.1 to 2.0 on frequency dial when FUNC OUT amplitude is max and 50 Ω terminated, and with SYM control OFF.

SYMMETRY and VERNIER controls affect frequency calibration. Maximum possible asymmetry is a function of frequency setting.

**NOTE: When SYMMETRY control is used, indicated frequency is divided by approximately 10.*

SECTION 2
INITIAL PREPARATION

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

WARNING

To preclude injury or death due to shock, the third wire earth ground must be continuous to the facility power outlet. Before connecting to the facility power outlet, examine extension cords, autotransformers, etc., between the instrument and the facility power outlet for a continuous earth ground path. The earth ground path can be identified at the plug on the instrument power cord; of the three terminals, the earth ground terminal is the nonmatching shape, usually cylindrical.

CAUTION

To prevent damage to the instrument, check for proper match of line and instrument voltage and proper fuse type and rating.

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 120 Vac line supply and with a ¾ amp fuse.

Conversion to other input voltages requires a change in rear panel fuse holder voltage card position and fuse (figure 2-1) according to the following procedure.

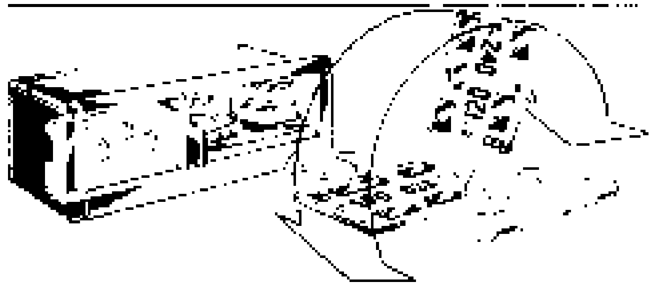


Figure 2-1. Voltage Selector and Fuse

1. Disconnect the power cord at the instrument, open fuse holder cover door and rotate fuse-pull to left to remove the fuse.
2. Remove the small printed circuit board and select operating voltage by orienting the printed circuit board to position the desired voltage to the top left side. Push the board firmly into its module slot.
3. Rotate the fuse-pull back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.
4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

Card Position	Input Vac	Fuse
100	90 to 105	¾ amp
120	108 to 126	¾ amp
220	198 to 231	⅜ amp
240	216 to 252	⅜ amp

2.2.2 Signal Connections

Use RG58U 50Ω coaxial cables equipped with BNC connectors to distribute signals when connecting this instrument to associated equipment.

2.3 ELECTRICAL ACCEPTANCE CHECKOUT

This checkout procedure verifies the generator operation. If a malfunction is found, refer to the Warranty in the front of this manual. A dual trace, 150 MHz bandwidth oscilloscope with X10 time base magnification, a 50Ω load, a coaxial tee and three 50Ω cables are required to perform this checkout.

Set up as in figure 2-2 and preset the generator front panel controls as follows, then perform the steps in table 2-1.

Control	Position
FREQ/START FREQ	1.0
FREQ MULT	1K
VERNIER/SYM	FREQ CAL (cw)
SYM	Off (extended)
MODE	CONT
TRIG LEVEL	10 o'clock
FUNCTION	∿
DC OFFSET (On/Off)	OFF (Extended)
DC OFFSET (Variable Control)	ccw
OUTPUT ATTEN 40, 20, 10	All extended
AMPLITUDE	MAX (cw)
SUPPRESSED CARRIER	AM (extended)
AM CARRIER LEVEL/NULL	ccw
AUX GEN MODE	AUX OUT ONLY
WIDTH/ΔF/ΔM	cw
AUX GEN FUNC	∿
AUX GEN SYMMETRY	cw
AUX GEN FREQ	100-3K
AUX GEN VERNIER	MAX (cw)
POWER	ON

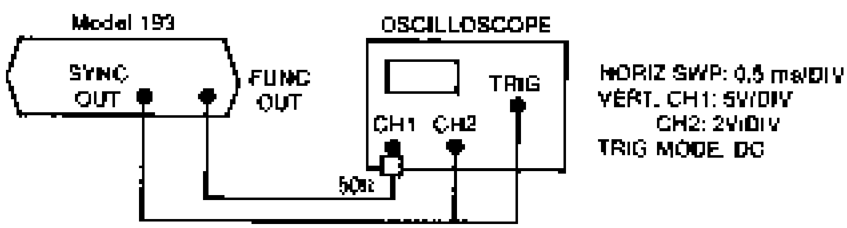


Figure 2-2. Main Generator Check Setup

Table 2-1. Checkout Procedure

Step	Control	Position/Operation	Observation
1	Oscilloscope	Trig level and slope both positive.	CH2: Square wave that begins on positive going edge. CH1: 15 Vp-p sine wave.
2	Dial and VERNIER/SYM	Rotate dial full cw, vernier full ccw. Then the opposite. Return dial to 1.0, vernier to CAL.	CH2: Square wave remains in sync for all dial positions. Range is greater than 2 Hz to 2000 Hz (1000:1).
3	FREQ MULT	Rotate to all positions. Return to 1K position.	Frequency is 1 × each range position.
4	AMPLITUDE	Set to 6 Vp-p on scope	CH1: Amplitude decreases to approximately 6 Vp-p.
5	DC OFFSET	Depress DC OFFSET switch, then rotate DC OFFSET Control cw. (Extended DC OFFSET upon completion.)	Full ccw gives negative offset. Clipping occurs when the offset plus waveform peak amplitude exceeds approximately ± 7.5V into 50Ω. Initially the negative peak is clipped, but as the dc offset is rotated cw the clipping of the negative peak disappears and eventually the positive peak begins to clip.

Table 2-1. Checkout Procedure (cont)

Step	Control	Position/Operation	Observation
6	AMPLITUDE	Rotate cw	Waveform returns to 15 Vp-p.
7	OUTPUT ATTN 10, 20, 40	Depress buttons in various combinations. Then release all buttons	Output level varies from 15 Vp-p (0 dB) to 4.7 mV (70 dB)
8	FUNC (Main Generator)	Select DC, ∿, △, ⊓. Reset to ∿.	Observe 0 Vdc level; ∿, △ and ⊓ are 15 Vp-p. Note phase relationships; ⊓ in phase with ∿ and △.
9	SYM, VERNIER/SYM.	Depress SYM switch and rotate VERNIER/SYM control ccw. Extend SYM, return VERNIER/SYM to CAL.	Frequency decreases to approximately 100 Hz. ccw of the 12 o'clock position gives 1:19; cw gives 19:1 (skewed sine wave and variable duty cycle pulses can be observed for ∿ and ⊓.)
10	MODE and FUNC (Main Generator)	Select GATE. Select ∿, △, ⊓. Return to ∿.	A dc level near zero volts (except ⊓ function; quiescent level is at negative peak value).
11	MANUAL TRIGGER	Press, hold and release.	A burst of ∿ for the period the MAN TRIG is depressed.
Set up trigger source (200 Hz triangle 10Vp-p), scope and Model 193 as shown in figure 2-3.			
12	TRIG LEVEL	Rotate throughout its range. Return to 10 o'clock.	CH 1: The number of waveform cycles in each gated "burst" varies with the trigger level. Notice relationships between Channels 1 and 2 waveforms as the TRIGGER LEVEL is rotated.
13	MODE	Select TRIG	CH1: A single triggered ∿ recurring at the 200 Hz trigger rate.
Return all controls to the initial setup. Set up scope and Model 193 as shown in figure 2-4.			
14	AUX GEN FUNC	Rotate to ∿, △, ⊓.	∿, △, ⊓ are approximately 10 Vp-p, 3 kHz.
15	Width/ΔF/ΔM	Rotate ccw. Return to cw position.	CH1:AUX OUT level varies from approximately 10 Vp-p to 0 Vp-p.
16	AUX GEN FUNC and SYMMETRY	Rotate to ⩘, ⊓. Vary symmetry control. Return to ∿.	⩘ and ⊓ are approximately 10 Vp-p, 300 Hz. Symmetry varies from 19:1 to 1:19.
17	AUX GEN FREQ and VERNIER	Rotate VERNIER in all FREQ range positions. Return FREQ range to 100-3K and VERNIER to cw.	Frequency varies in each range to the range limits as marked.

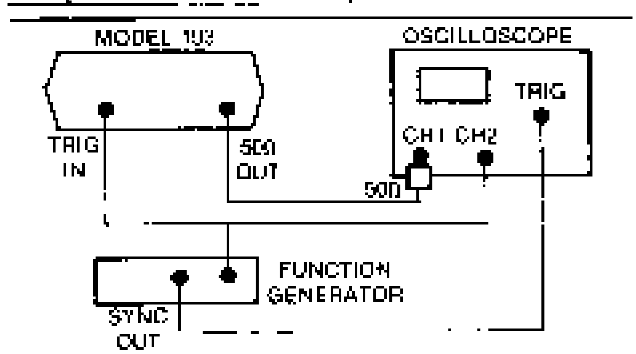


Figure 2-3. Checkout Setup

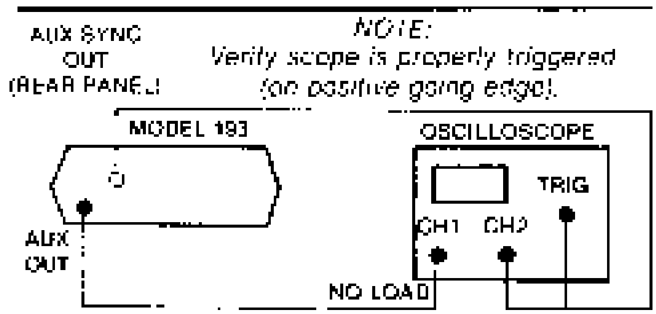


Figure 2-4. Auxiliary Generator Check

Table 2-1. Checkout Procedure (cont)

Step	Control	Position/Operation	Observation
Set up the Model 193 and scope as shown in figure 2-5.			
18	AUX GEN MODE	Set to SET FREQ/AUX GEN OFF	FM center frequency of 1kHz on CH1
19	AUX GEN FREQ Range, VERNIER	FREQ range to .1-3 and VERNIER to 12 o'clock.	(This sets the rate of modulation.)
20	AUX GEN MODE and WIDTH/ΔF/ΔM	Select SET ΔF and vary WIDTH/ΔF/ΔM for 1.1 kHz on scope	Approximately 1.1 kHz on CH1. This will be maximum peak frequency of modulated signal
21	AUX GEN MODE	Select FM.	Both channels: CH1 frequency varies with instantaneous amplitude of AUX OUT waveform on CH2
22	AUX GEN FUNC and SYMMETRY	Select ⟋ and full ccw rotation	(Ramp's instantaneous amplitude controls sweep: A slow sweep up and fast return to start frequency.)
23	AUX GEN MODE	Select SET START	(Ramp is held at its start voltage.)
24	FREQ/START FREQ Dial and VERNIER/SYM	Set dial to .02 and VERNIER full ccw.	CH1: Approximately 2 Hz. (start frequency).
25	AUX GEN MODE and WIDTH/ΔF/ΔM	Select SET WIDTH and rotate WIDTH/ΔF/ΔM cw	CH1: Approximately 2 kHz. (Max sweep frequency for range)
26	AUX MODE	Select SWEEP	Sweep of main generator from 2 Hz to 2 kHz (If AUX GEN symmetry is rotated cw, the main generator sweeps from 2 kHz to 2 Hz

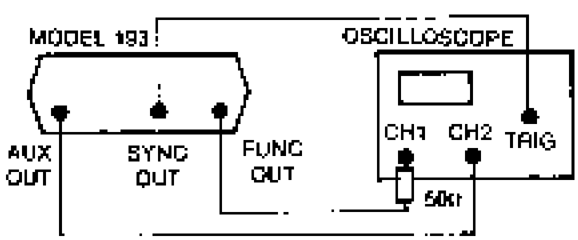


Figure 2-5. FM and Sweep Check Setup

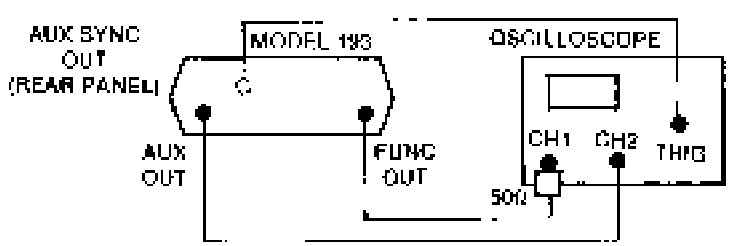
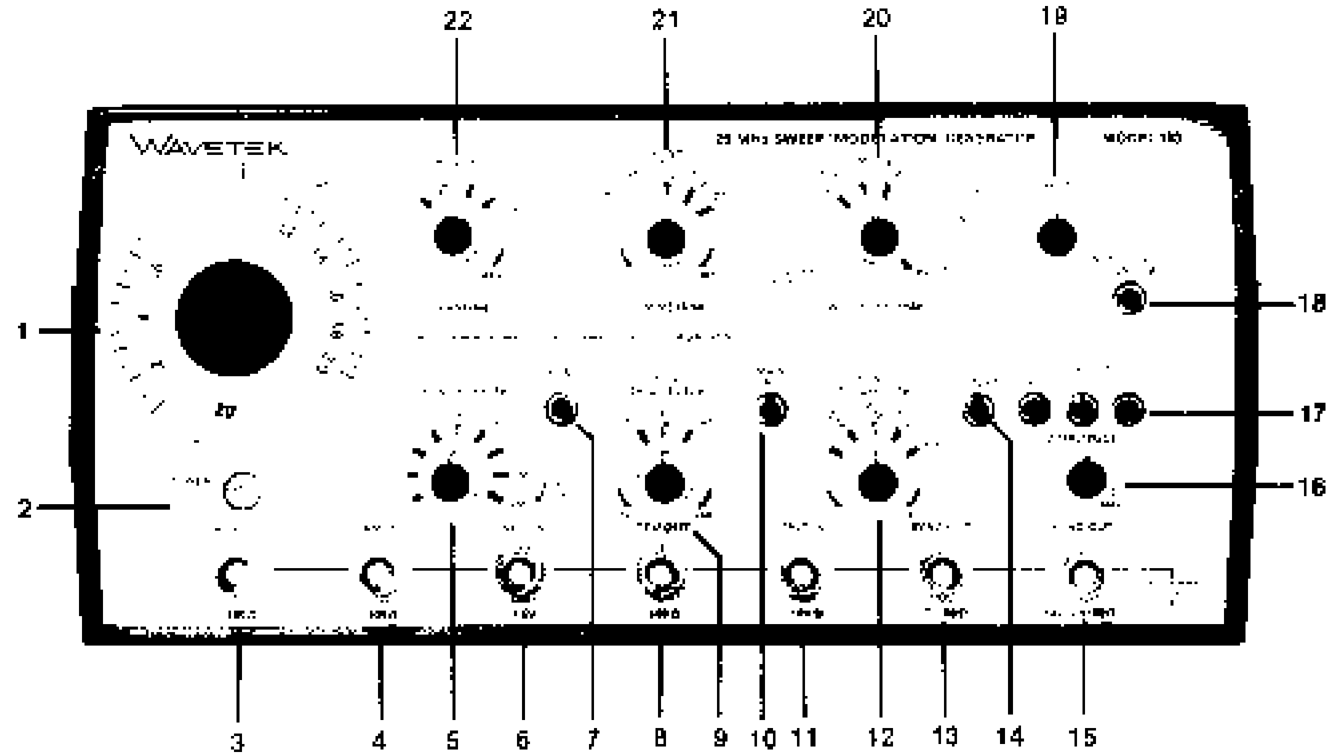
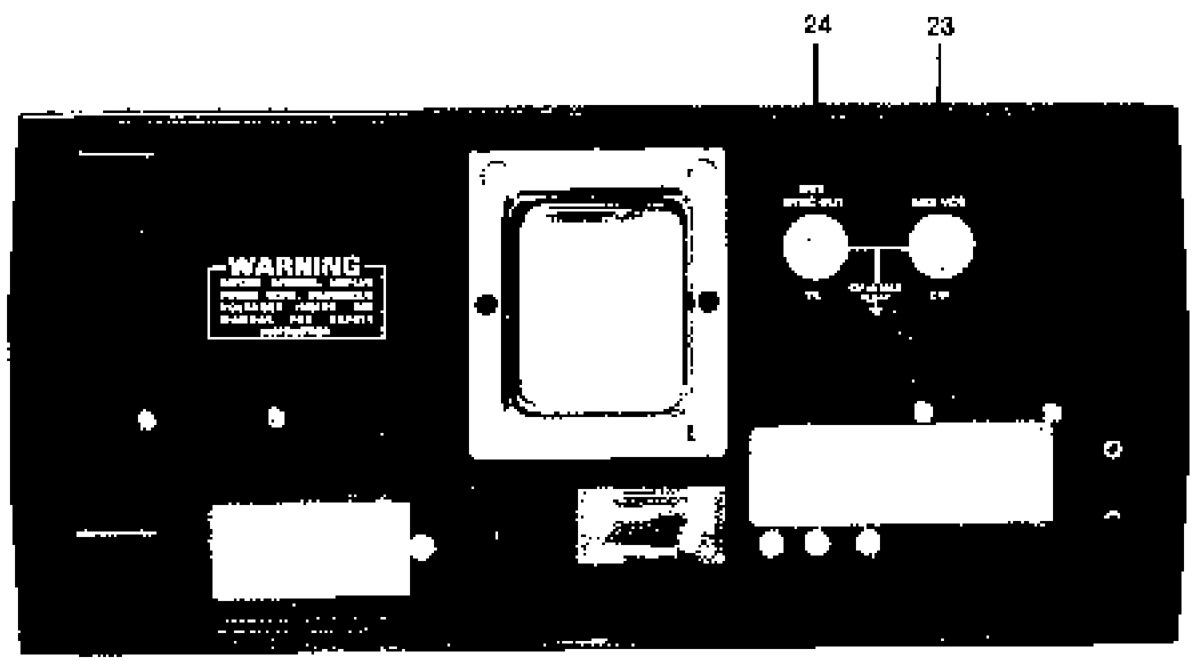


Figure 2-6. AM Check Setup

Table 2-1. Checkout Procedure (cont)

Step	Control	Position/Operation	Observation
	Set up the Model 193 and scope as shown in figure 2-6.		
27	AUX GEN MODE FREQ MULT (Main Gen) FREQ/START FREQ Dial FUNC (Main Gen)	Select SET CARRIER 10K 1.0 AM	CH1: When AM is selected, the unmodulated carrier level at the FUNC OUT decreases to one-half the normal amplitude to prevent clipping of AM peaks. 7.5 Vp-p unmodulated carrier shown on CH1. (Note: AM CARRIER LEVEL/NULL varies carrier level.
28	AUX GEN MODE AUX GEN FUNC AUX GEN FREQ AUX GEN FREQ VERNIER	Δ M ∿ 100I3K 9 o'clock	
29	WIDTH/ΔF/AM	Adjust for 4 Vp-p sine wave.	CH1: 4 Vp-p sine wave.
30	AUX GEN MODE	AM	CH1: Modulation envelope varies with instantaneous amplitude of CH2 waveform. Approximately 30% modulation
31	SUPPRESSED CARRIER	Depress	Suppressed carrier signal on CH1. (Adjusting AM CARRIER LEVEL/NULL controls the balance of the modulation envelope peaks.)





REAR PANEL

Figure 3-1. Controls and Connectors.

SECTION 3
OPERATION

3.1 CONTROLS AND CONNECTORS

The generator front panel controls and connectors are shown in figure 3-1 and keyed to the following descriptions.

1 **FREQ/START FREQ Dial** — Settings under the dial index mark summed with **6** and multiplied by **5** determine the main generator signal frequency at FUNC OUT **15**.

2 **POWER Pushbutton** — Depressed is power on, extended is power off.

3 **AUX OUT Connector** — This BNC is the auxiliary generator waveform output. The FUNC control **21** of the AUX GEN selects the waveform and the WIDTH/ΔF/ΔM control **20** varies the waveform level from 0 to 10 Vp-p (5 Vp-p into 600Ω). Source impedance is 600Ω.

4 **AM IN Connector** — This BNC receives the external amplitude modulation or suppressed carrier signal. When FUNC switch **12** selects AM, a 5 Vp-p signal gives 100% modulation for normal AM (SUPPRESSED CARRIER **18** extended) or a 10 Vp-p signal gives suppressed carrier operation (SUPPRESSED CARRIER **18** pressed). Source impedance is 600Ω.

5 **FREQ MULT Control** — Outer coax control selects one of nine frequency multipliers for dial **1** setting.

VERNIER/SYM Control — When SYM **7** is off (extended) this inner coax control is a fine adjustment of the dial **1** setting. When SYM **7** switch is on (depressed) this control varies the symmetry of the main generator waveforms (normally 50% duty cycle). Symmetry range is 19:1 to 1:19 (half cycle to half cycle ratio). When SYM is used, the main generator frequency is divided by 10. Extending SYM switch ensures 1:1 (50%) symmetry.

6 **VCG IN Connector** — This BNC accepts ac or dc voltages to proportionately control main generator frequency within the range determined by the FREQ MULT **5**. Positive voltages increase the frequency set by the dial **1**. negative voltages decrease the frequency. The VCG IN will not drive the generator frequency beyond the normal limits of a range. (Upper limit: 2 × FREQ MULT setting. Lower limit: 1/1000 upper limit) Input impedance is 5 kΩ.

7 **SYM Pushbutton** — This switch, when depressed, allows main generator waveform symmetry to be varied 19:1 to 1:19 range by the VERNIER/SYM control **5** (as a result, the main generator frequency is divided by 10). When extended, the switch allows the main generator to produce normal (50% duty cycle) waveforms.

8 **GCV OUT Connector** — This BNC provides dc excursions of 0 to +5V (open circuit) that represents the main generator output frequency in the range selected by FREQ MULT **5**. Source impedance is 600Ω.

9 **MODE Control** — This outer coax control selects one of the three main generator operating modes:

CONT — Continuous output at FUNC OUT **15** and SYNC OUT **13** connectors.

TRIG — A dc level output until the generator is triggered by the MAN TRIG **10** or with a signal at the TRIG IN connector **11**. When triggered, the generator output is one cycle of waveform followed by a dc level.

GATE — As for TRIG except the output is continuous for the duration of the manual or external trigger signal. The last waveform cycle started is always completed.

TRIG LEVEL Control — This inner coax control is a continuously variable adjustment of the trigger circuitry firing point. When full ccw, a positive going signal at approximately +5V is required for triggering (see figure 3-2). In the full cw position, a positive going signal at approximately −5V or more positive voltage is required for triggering. In the gated modes, the generator will run continuously when the control is cw of 12 o'clock.

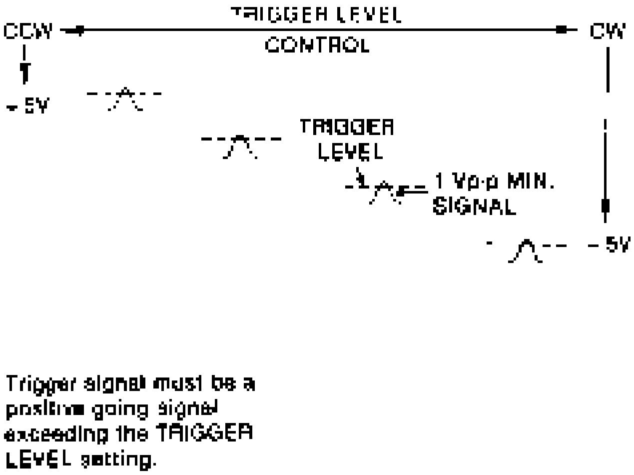


Figure 3-2. Minimum Trigger Signal

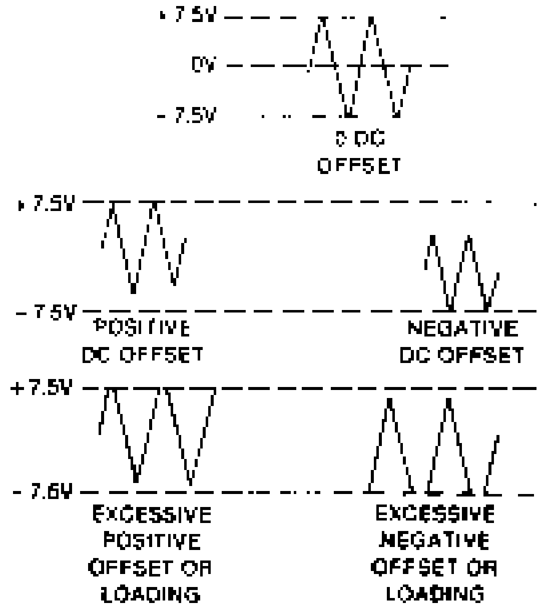


Figure 3-3. DC OFFSET Control

10 MAN TRIG Pushbutton — Triggers or gates the output signals when main generator mode is TRIG or GATE **9**. In trigger mode, one waveform cycle is output when the button is pushed. In gated mode, waveform cycles are continuously output as long as the button is held in.

11 TRIG IN Connector — This BNC receives the external trigger and gate signals. These signals are applied to the trigger and gate circuit when the MODE switch **9** is in the TRIG or GATE positions. Refer to Section 1 Trigger (and Gate).The TRIG LEVEL control **8** varies the firing point of the TRIG IN signal.

12 FUNCTION Selector — Outer coaxial knob selects one of the three main generator waveforms (sine, triangle, square), dc, and AM.

DC OFFSET Control — Inner coaxial control offsets the main generator output waveform vertically from its normal position and, when FUNCTION (outer coaxial switch) **12** is in the DC position, controls polarity and voltage of dc output. DC output range is 0 ± 10 Vdc (± 5 Vdc into 50Ω). DC OFFSET switch **14** must be depressed to enable this DC OFFSET control. Extending the DC OFFSET switch ensures zero volt offset. DC offset and waveform are attenuated by the OUTPUT ATTEN control **17**, but dc offset is not attenuated by the AMPLITUDE control **16**. Waveform peak voltage plus dc offset is limited to ± 15 Vdc (± 7.5 Vdc into 50Ω). See Figure 3-3.

13 SYNC OUT Connector — The sync signal from this BNC is a TTL level into 50Ω, synchronous with FUNC OUT **15** signal. In CW, duty cycle varies with waveform symmetry. Source impedance is 50Ω.

14 DC OFFSET Pushbutton — Depressed button activates dc offset **12**. Extended button ensures zero dc offset.

15 FUNC OUT Connector — This BNC is the waveform, or dc output of the main generator (alone or modulated). Maximum output is 30 Vp-p (15 Vp-p into 50Ω). Source impedance is 50Ω.

16 AMPLITUDE Control — Continuously varies waveform amplitude within each OUTPUT ATTEN **17** range. Full ccw rotation reduces waveform amplitudes by greater than 10 dB. DC and dc offset voltages are not affected by this control.

17 OUTPUT ATTEN Pushbuttons — Select the attenuation range of the FUNC OUT **15** signal. The AMPLITUDE control **16** allows continuous waveform (but not dc) level variations within each attenuator range. Each of the three buttons may be used individually for 40, 20 or 10 dB steps of attenuation, or pressed in combinations for up to 70 dB of attenuation. The attenuator attenuates both the waveform and dc offset.

18 SUPPRESSED CARRIER Pushbutton — When pressed, selects suppressed carrier operation and if extended, selects AM operation.

19 **AM CARRIER LEVEL/NULL Control** — In the AM function (FUNC **12**) with the MODE switch **20** set to SET CARRIER, this control sets the peak-to-peak level of the carrier (main generator sine wave) at FUNC OUT **15**.

If SUPPRESSED CARRIER **18** is pressed, the AM CARRIER LEVEL/NULL control balances the peaks of the suppressed carrier signal at FUNC OUT **15**.

20 **MODE Switch** — Outer coax control selects one of three basic operating modes of the auxiliary generator: frequency modulation, frequency sweep, or amplitude modulation. Additional settings allow static setup of these modes. The following sections describe each switch setting.

SET FREQ/AUX GEN OFF — Auxiliary generator is turned off for main generator only operation, or to allow center frequency (f_0) adjustment for FM operation. The dial 1 and **FREQ MULT 5** sets the center frequency (f_0) for frequency modulation.

SET ΔF — In preparation for FM operation, **FUNC OUT 15** frequency is held at the maximum frequency deviation ($f_0 + \Delta f$). The WIDTH/ΔF/ΔM control **20** sets the maximum frequency. (Refer to previous paragraph for f_0 selection.)

FM — Allows the auxiliary generator to frequency modulate the main generator creating an FM signal at FUNC OUT **15**.

SET START — In preparation for sweep operation, FUNC OUT **15** is held at initial sweep frequency. Dial **1** and FREQ MULT **5** sets the initial frequency. FUNC **21** sets the waveform that controls the main generator frequency.

SET WIDTH — In preparation for sweep operation, FUNC OUT **15** frequency is held at the final sweep frequency. The WIDTH/ΔF/ΔM control **20** sets the final sweep frequency.

SWEEP — Allows the auxiliary generator to sweep the main generator creating a frequency swept signal at FUNC OUT **15**.

SET CARRIER — In preparation for AM operation, allows setting of unmodulated output carrier level (main generator output) at FUNC OUT **15** by the AM CARRIER LEVEL/NULL control **19** and AMPLITUDE control **16**.

SET ΔM — In preparation for AM operation, holds FUNC OUT **15** at the valley of the modulation signal from the auxiliary generator to allow level adjustment by the WIDTH/ΔF/ΔM control **20**.

AM — Allows the auxiliary generator to AM or suppress carrier modulate the main generator for AM or suppressed carrier signal at FUNC OUT **15**.

AUX OUT ONLY — Disconnects the auxiliary generator from the main generator. Allows the auxiliary generator to be used as an independent function generator whose output is AUX OUT **3**.

WIDTH/ΔF/ΔM — Inner coax control serves several functions dependent upon the outer coax MODE switch setting. With MODE in ΔF position, WIDTH/ΔF/ΔM sets the maximum positive frequency deviation. With MODE SET WIDTH, WIDTH/ΔF/ΔM sets the final sweep frequency. With MODE in SET ΔM, WIDTH/ΔF/ΔM sets the valley of the FUNC OUT **15** modulation signal. Finally, with MODE in AUX OUT ONLY, WIDTH/ΔF/ΔM controls the signal amplitude at AUX OUT **3**.

21 **FUNC Control** — This outer coax control selects one of five auxiliary generator waveforms: sine, triangle, square, sawtooth and pulse. Symmetry of the sawtooth and pulse is adjustable between 1:19 and 19:1 by the inner coax SYMMETRY control. When sawtooth and pulse are selected, the auxiliary generator frequency is divided by 10.

SYMMETRY — When outer coax FUNC control is set to sawtooth or pulse, this inner coax control varies the symmetry of sawtooth and pulse over a 1:19 to 19:1 range.

22 **FREQ Control** — Outer coax control selects one of four auxiliary generator frequency ranges, e.g., 3-100 Hz.

VERNIER — Inner coax control provides continuous frequency control of the auxiliary generator frequency range selected by outer coax FREQ control.

23 **AUX VCG Connector** — This BNC allows up to a 33:1 auxiliary generator frequency change with a +5V signal. Upper frequency is limited to the maximum of the selected range. Input impedance is 11 kΩ.

24 **AUX SYNC OUT Connector** — This BNC provides a TTL level pulse which leads the AUX OUT **3** sine wave by 90°, lags the triangle wave by 90° and is 180° out of phase with the square wave. AUX SYNC OUT duty cycle varies with SYMMETRY control **21**.

3.2 OPERATION

Perform the initial checkout in Section 2 for the feel of the instrument. Any questions concerning individual controls and connectors may be answered in paragraph 3.1

3.2.1 Signal Termination

Proper signal termination, or loading, of the generator connectors is necessary for its specified operation. For example, figure 3-4 shows proper termination of the FUNC OUT connector. Placing the 50Ω terminator, or 50Ω resistance, in parallel with a higher impedance, matches the receiving instrument input impedance to the coax characteristic and generator output impedance, thereby minimizing signal reflection or power loss on the line due to impedance mismatch.

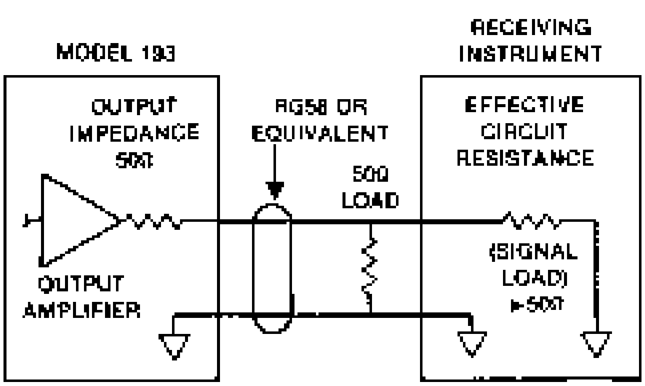


Figure 3-4. Signal Termination

The input and output impedances of the generator connectors are:

Connectors	Impedance
FUNC OUT	50Ω
SYNC OUT	50Ω
GCV OUT	600Ω
AUX OUT	600Ω
AUX SYNC OUT	TTL
TRIG IN	1.5kΩ
VCG IN	10kΩ
AM IN	600Ω
AUX VCG IN	10kΩ

3.2.2 Manual Main Generator Basic Operation

The following steps demonstrate setting up the main generator for continuous operation. (Bold numbers are keys to figure 3-1. Refer to paragraph 3.1 for further explanations of controls and connectors.) Outputs are shown in figure 3-5.

Step	Control/Connector	Setting
1	AUX GEN MODE **20**	Select AUX GEN OFF.
2	FUNC OUT **15**	Connect to under test (refer to paragraph 3.2.1).
3	MODE **9**	Select CONT
4	SYM **7**	Extended.
5	FREQ MULT **5**	Set to desired range of frequency
6	FREQ/START FREQ Dial **1**	Set to desired frequency within the range.
7	FUNCTION **12**	Select desired waveform.
8	DC OFFSET **14**, Inner Control **12**	Set as desired. Limit offset to prevent clipping (See figure 3-3).
9	OUTPUT ATTEN **17**	Select for desired attenuator range.

As an actual exercise in operation, perform steps 1 through 13 in table 2-1.

3.2.3 Voltage Controlled Main Generator Operation

Operation of the main generator as a voltage controlled function generator (VCG) is as for a manually controlled function generator, only the frequency within particular ranges is additionally controlled by an external voltage (± 5V excursions) injected at the VCG IN connector. Perform the steps given in paragraph 3.2.2, only set FREQ/START FREQ to determine a reference from which the frequency is to be voltage controlled.

1. For frequency control with positive dc inputs at VCG IN, set the dial for a lower frequency limit.
2. For frequency control with negative dc inputs at VCG IN, set the dial for an upper frequency limit.
3. For modulation with an ac input at VCG IN, set the dial at the desired center frequency. When applying VCG voltage, do not exceed the maximum dial range of the selected frequency range.

Figure 3-6 is a nomograph with examples of dial and voltage effects. Example 1 shows that with 0V VCG input, frequency is determined by the dial setting 1.0 in this example. Example 2 shows that with a positive

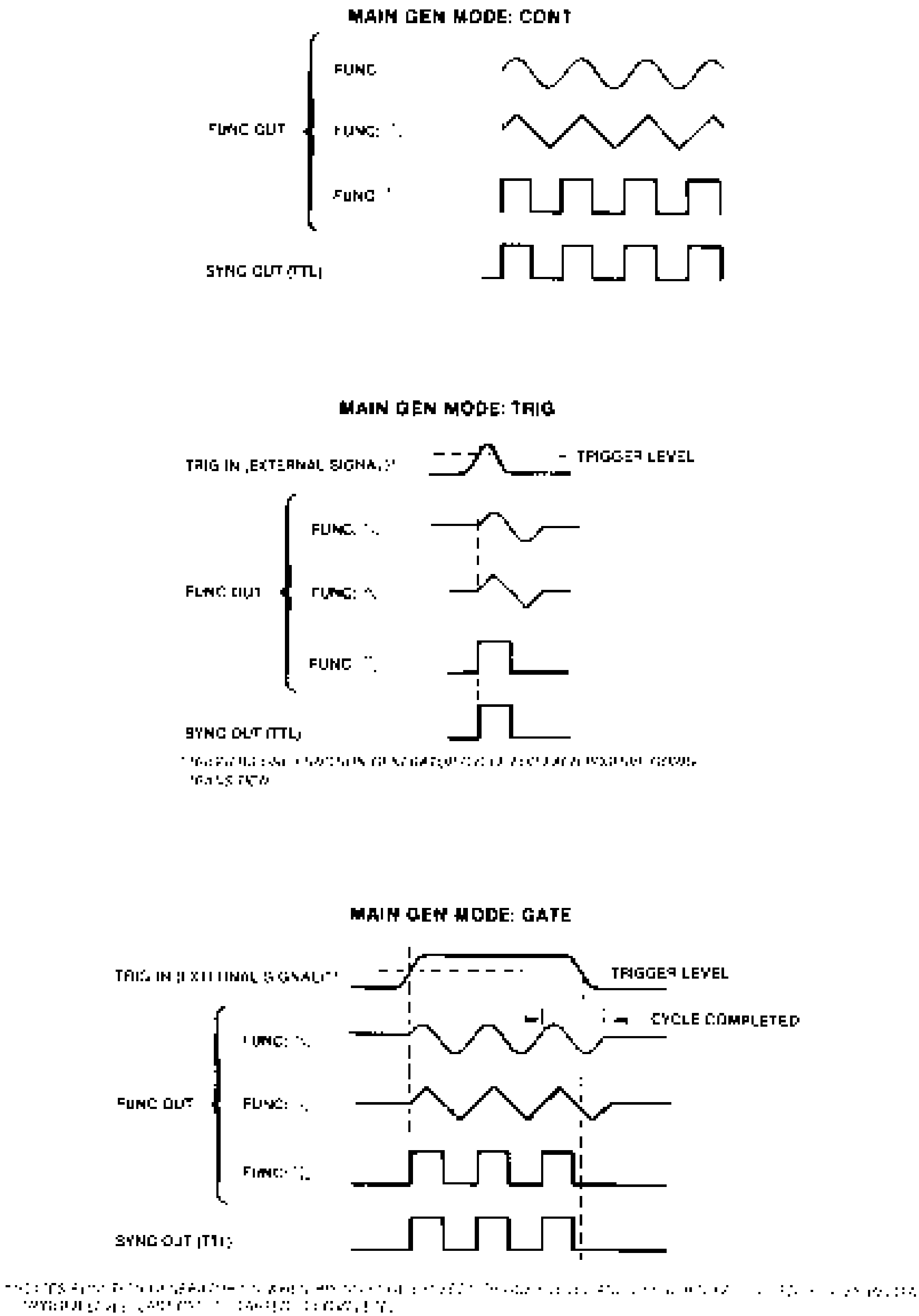
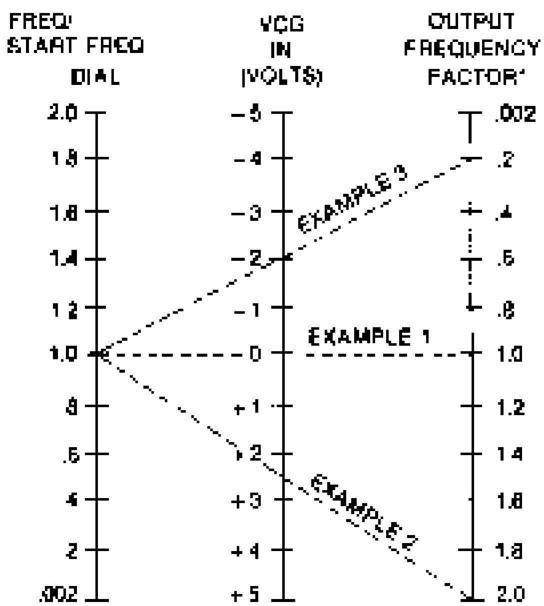


Figure 3-5. Main Generator Basic Operation

VCG input, output frequency is increased. Example 3 shows that with a negative VCG input, output frequency is decreased. (Note that the Output Frequency Factor column value must be multiplied by a frequency range multiplier to give the actual output frequency.)

NOTE

Nonlinear operation may result when the VCG input voltage is excessive, that is when the attempted generator frequency exceeds the range limits. The upper limit is 2 times the multiplier setting, and the lower limit is 1/1000th of the upper limit.



*Must be multiplied by FREQ MULT switch setting

Figure 3-6. VCG Voltage-to-Frequency Nomograph

The up to 1000:1 VCG sweep of the generator frequencies available in each range results from a 5V excursion at the VCG IN connector. With the frequency dial set to 2.0 and the main generator VERNIER fully ccw, excursion between +5V and 0V at VCG IN provide the up to 1000:1 sweep within the set frequency range.

3.2.4 Manual Auxiliary Generator Operation

The auxiliary generator, when used as a separate function generator, provides frequency and function selection in a continuous mode. (Bold numbers are keyed to figure 3-1. Refer to paragraph 3.1 for further explanations of controls and connectors.) The following steps demonstrate setting up of the auxiliary generator for continuous operation.

Step	Control/Connector	Setting
1	AUX GEN MODE **20**	Set to AUX OUT only.
2	AUX OUT **3**	Connect to circuit under test, source impedance is 600Ω.
3	FREQ **22**	Select desired frequency range.
4	VERNIER **22**	Set to desired frequency within the range.
5	FUNC **21**	Select desired waveform.
6	WIDTH/ΔF/ΔM **20**	Select desired amplitude at AUX OUT.

NOTE

AUX SYNC OUT Connector — This rear panel BNC provides a TTL level pulse which lags the AUX OUT 3 triangle signal by 90°.

As an actual exercise in operation, perform steps 14 through 17 of table 2-1.

3.2.5 Voltage Controlled Auxiliary Generator Operation

Operation of the auxiliary generator in Voltage Controlled Generator (VCG) mode is very similar to VCG operation of the main generator (paragraph 3.2.3) except there is a maximum of 33:1 frequency change with a 0 to ±5V change at the AUX VCG input BNC (a 1000:1 change is maximum for the main generator).

3.2.6 FM Operation

In FM operation, the instantaneous frequency of the output signal varies with the instantaneous amplitude of the modulating signal (Figure 3-7). Both main and auxiliary generators may be frequency modulated by external signals at their VCG inputs (ref: paragraphs 3.2.3 and 3.2.5). Internal operation is the main generator modulated by the auxiliary generator. Internal FM operation is the same as a manually controlled main generator operation (ref. paragraph 3.2.2) except that, in addition, the main generator is frequency modulated by the auxiliary generator. The following steps demonstrate setting up the unique controls for FM modulation. (Bold numbers are keyed to figure 3-1. Refer to paragraph 3.1 for further explanations of controls and connectors.)

Step	Control/Connector	Setting
1	AUX GEN Mode **20**	Select SET FREQ/AUX GEN OFF.

2	FREQ/START FREQ Dial **1** FREQ MULT **5** and VERNIER/SYM **5**	Set for FM center frequency.
3	AUX GEN MODE **20** WIDTH/ΔF/ΔM **20**	Select SET ΔF. Set for peak frequency deviation.
4	AUX GEN MODE **20**	Select FM
5	FUNC **21**	Select modulation function.
6	AUX GEN FREQ, AUX GEN VERNIER **22**	Set modulation rate

As an actual exercise in operation, perform steps 18 through 21 of table 2-1

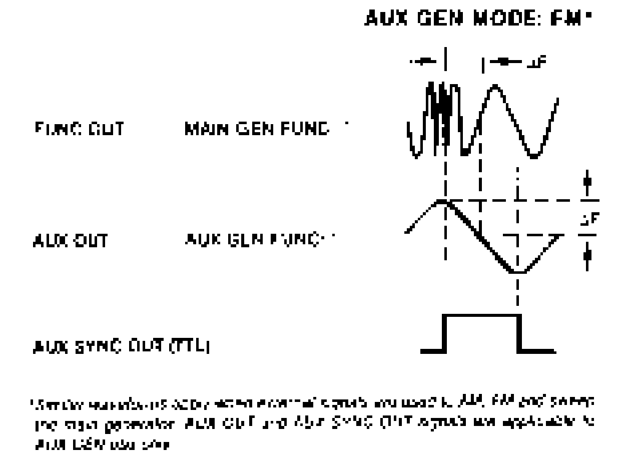


Figure 3-7. FM Operation

3.2.7 Sweep Operation

Both the main generator and auxiliary generator may be swept with a ramp voltage applied to their respective VCG inputs (ref paragraphs 3.2.3 and 3.2.5). Internal sweep is the main generator being swept by the auxiliary generator. Internal sweep operation is the same as manually controlled main generator operation (ref paragraph 3.2.2), except that, in addition, the auxiliary generator sweeps the main generator frequency between two preset frequency limits (Figure 3-8). The following steps demonstrate setting up the controls for frequency sweep of the main generator. (Bold numbers are keyed to figure 3-1. Refer to paragraph 3.1 for further explanations of controls and connectors.)

Step	Control/Connector	Setting
1	AUX GEN MODE **20**	Select SET START
2	START FREQ Dial **1**, FREQ MULT **5** and VERNIER/SYM **5**	Select start frequency
3	AUX GEN MODE **20**	Select SET WIDTH.
	WIDTH/ΔF/ΔM **20**	Set maximum sweep (stop) frequency.
4	AUX GEN MODE **20**	Select SWEEP
5	FUNC **21**	Select modulation function.
6	AUX GEN FREQ, AUX GEN/ VERNIER **22**	Set sweep rate.

As an actual exercise in operation, perform steps 22 through 26 of table 2-1

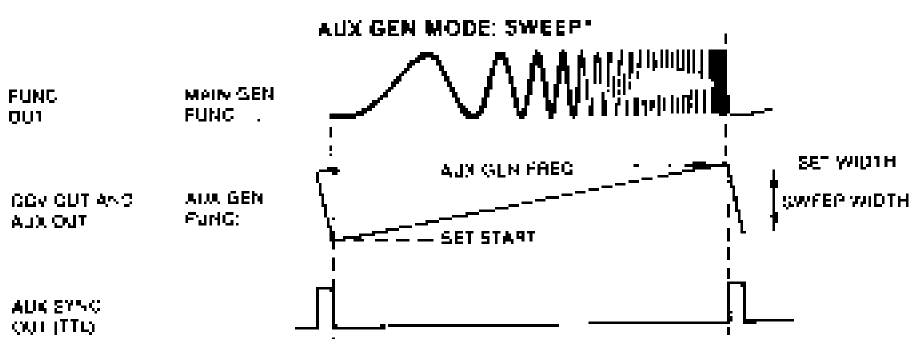


Figure 3-8. Sweep Operation

3.2.8 AM Operation

In amplitude modulation, the instantaneous amplitude of the output signal varies with the instantaneous amplitude of the modulation signal figure 3-9. The main generator may be amplitude modulated by an external signal (with MODE set to AUX GEN OFF) applied to the AM IN BNC connector as well as internally modulated by the auxiliary generator. For internal AM operation, set up the generator as for continuous operation (refer to paragraph 3.2.2). The following steps demonstrate setting up the additional controls for AM Modulation. (Bold numbers are keyed to figure 3-1. Refer to paragraph 3.1 for explanations of controls and connectors.)

Step	Control/Connector	Setting
1	Main Generator FUNC **12**	Select AM. FUNC OUT decreases by 50% to prevent waveform clipping when amplitude modulating
2	AUX GEN MODE **20**	Select SET CARRIER
3	AM CARRIER LEVEL/NULL **19**	Set unmodulated output carrier level
4	AUX GEN MODE **20**	Select AM.
5	AUX GEN MODE WIDTH/ΔF/ΔM **20**	Select the valley of the modulation signal.
6	**AUX GEN** MODE **20**	Select AM.
7	AUX GEN FREQ/VERNIER **22**	Sets amplitude modulation rate
8	AUX GEN FUNC **21**	Selects modulation function

As an actual exercise in operation, perform steps 27 through 30 of table 2-1.

3.2.9 Suppressed Carrier Operation

Operation as a suppressed carrier modulated generator is the same as for AM operation (ref paragraph 3.2.8), except the main generator carrier is suppressed (figure 3-9). The following steps demonstrate setting up the controls for suppressed carrier modulation. (Bold numbers are keyed to figure 3-1. Refer to paragraph 3.1 for explanations of controls and connectors.)

Step	Control/Connector	Setting
1	SUPPRESSED CARRIER **18**	Depressed Selects suppressed carrier operation.
2	AM CARRIER LEVEL/NULL **19**	Adjusts for equal balance of modulation envelope peaks. Balanced peaks ensures greatest carrier suppression

As an actual exercise in operation, perform steps 27 through 31 of table 2-1

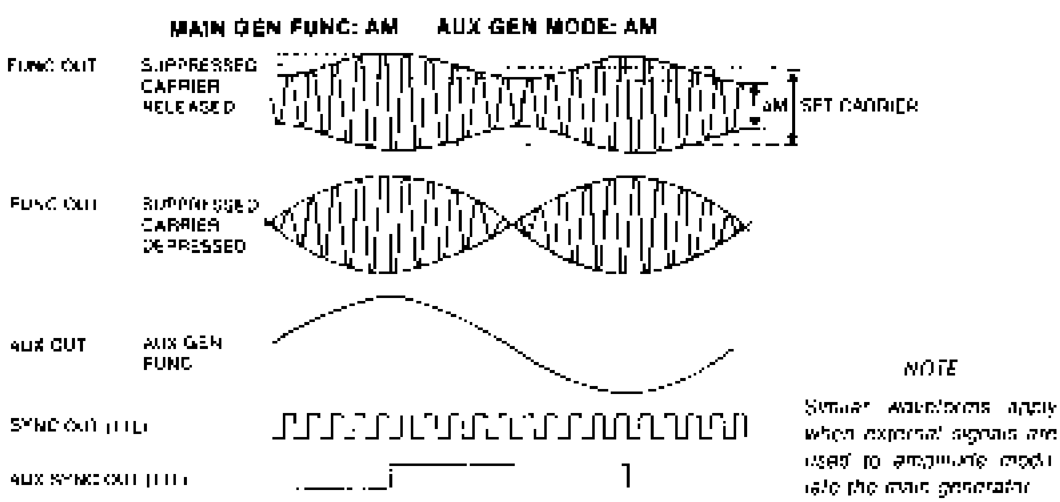


Figure 3-9. AM Operation

SECTION 4
CIRCUIT DESCRIPTION

4.1 INTRODUCTION

The Model 193 consists of two completely seperate, independent function generators: the main generator and sweep/modulation generator. This section describes the functional relationship between the two generators, and the function and relationship of the major circuit element of each generator.

While each generator can operate independently, they can be interconnected for frequency sweep, frequency modulation (FM), doubleside band amplitude modulation, and suppressed carrier amplitude modulation (refer to figure 4-1). For sweep and FM, the sweep/modulation generator varies the frequency of the main generator. In AM, both suppressed carrier and double side band, the main generator supplies a carrier signal that mixes, on the sweep/modulation generator board, with the modulating signal created by the sweep/modulation generator, to produce the amplitude modulated signal which feeds back to the main generator output amplifier.

Figure 4-2 illustrates the Main Generator circuit elements and their functional relationships, which paragraphs 4-2 and 4-4 describe. Figure 4-3 shows the Sweep/Modulation Generator circuit elements and their functional relationships, which paragraph 4-3 and 4-5 describe.

4.2 MAIN GENERATOR BLOCK DIAGRAM ANALYSIS

As shown in figure 4-2, the VCG (Voltage Controlled Generator) sums the voltage inputs from the FREQ/START FREQ Dial, VCG IN, sweep/FM Input and frequency vernier to provide a voltage control signal for the positive and negative current sources and the GCV amplifier. The positive and negative current sources generate precision currents, linearly related to the output of the VCG summing amplifier, which pass through the current switch to the timing capacitors. Additional linear currents are generated for loop dc delay compensation and the trigger baseline com-

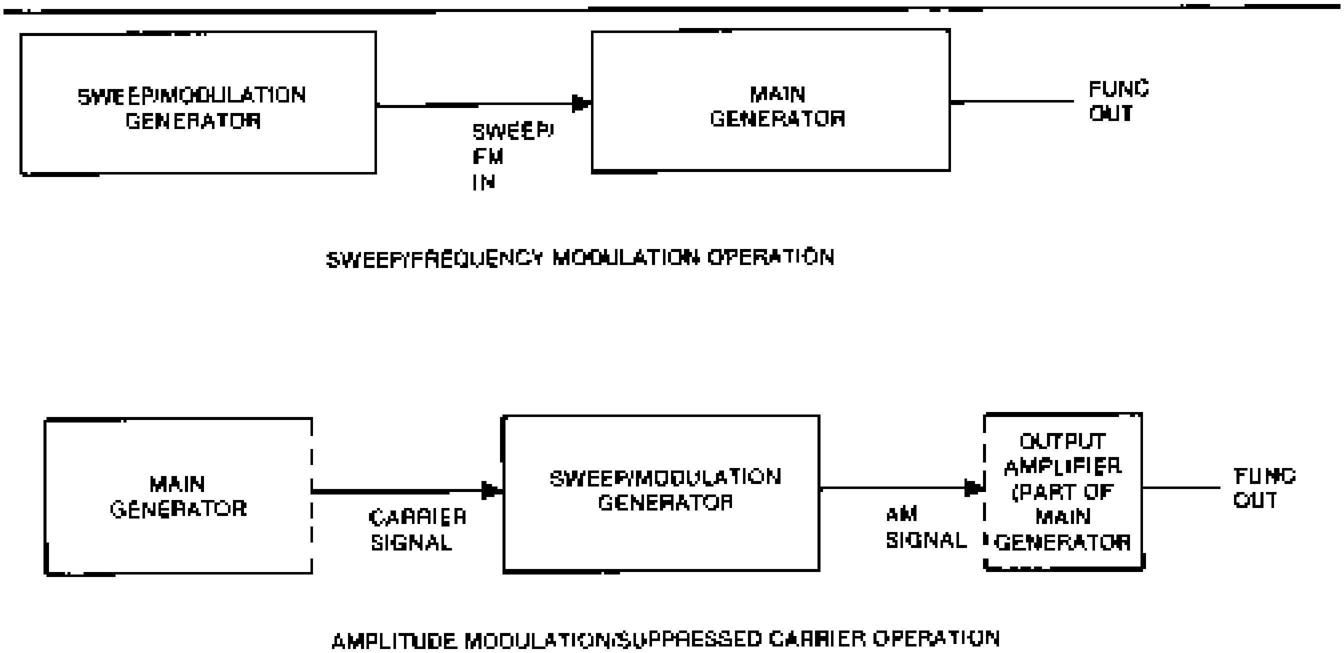


Figure 4-1. Model 193 Overall Block Diagram

pensation. The GCV amplifier provides a dc voltage proportional to the main generator frequency.

The current switch, controlled by the hysteresis output, causes either the positive current source or the negative current source to charge the timing capacitor selected by the frequency multiplier. When the positive current source is switched in, the charge on the timing capacitor will rise linearly producing the positive-going triangle slope. Likewise the negative current source produces the negative going triangle slope.

The triangle buffer amplifier is a unity gain amplifier whose output is fed to the hysteresis switch, sine converter and function switch. The hysteresis switch operates as a "window" comparator with limit points set to the triangle peaks. When the positive going ramp reaches +1.0V, the hysteresis switch toggles to a low state causing the current switch to connect the negative current source. This causes the timing capacitor voltage to linearly ramp to −1.0V. As the timing capacitor voltage reaches −1.0V, the hysteresis switch toggles to a high state, switching in the positive current source. The generator loop continues to oscillate producing simultaneous triangle and square waves, at a frequency determined by the frequency multiplier and the magnitude of the timing current controlled by the sum of the dial setting, the VCG input, and the vernier.

Depressing the SYM button produces an unsymmetrical waveform and a division of the frequency by a factor of 10. The VERNIER/SYM control creates an imbalance in the current sources and therefore an imbalance in the waveform symmetry up to a ratio of 19:1. The result is variable duty cycle pulse, variable askewed sine wave and variable "sawtooth" triangle waves.

On the X1M and X10M ranges the dc loop delay compensation circuit compensates for delays in the generator loop. This circuit causes the hysteresis switch trip points to switch earlier in the cycle, and prevents the timing capacitors from charging beyond ±1.0V. The switch points are adjusted in proportion to the charging current, thus ensuring a constant amplitude as frequency is varied.

The capacitance multiplier is an active circuit which simulates capacitors up to 10,000 times larger than the timing capacitor, thus allowing very long charging times using physically small capacitors. This circuit is used in the four lowest frequency ranges.

The sine converter accepts a ±1.0 volt triangle signal from the triangle buffer and converts it to a sine wave current. The output is fed via the function switch to the preamplifier.

The trigger circuit allows precise single or multiple (gated) cycles at the output in response to external trigger signals or manual trigger operation. The trigger circuit operates by holding the timing capacitor at 0 volts, via the loop stop signal, on the positive going triangle ramp, until a trigger signal occurs. In the TRIG mode a single cycle is produced for each trigger signal above the variable trigger level threshold. In the GATED mode continuous cycles are generated for the time period at which the external signal is above the trigger level threshold plus the time for completion of the last partial cycle. The $\overline{RUN}$ signal causes the SYNC output to stay in the low state when the generator is quiescent. The TRG RST signal resets the trigger circuit and generator to the quiescent state on every generator cycle to arm it for the next trigger input. The trigger baseline compensation, LOOP STOP, circuit holds the generator output at zero volts, LOOP STOP, (within specified limits) during the quiescent intervals at any position (value) of the frequency dial, FREQ MULT, VCG IN, or VERNIER.

The sync circuit accepts the square wave signal from the hysteresis switch or zero crossing detector and converts it to a true 50Ω TTL level output. In square wave function (SYNC SELECT enabled) the sync is in phase with the output, but in triangle or sine functions (SYNC SELECT disabled), the zero crossing detector causes the sync output to be in phase withthe zero crossing of the output waveform.

When square is selected by the function switch, the square shaper accepts the signal from the hysteresis switch and converts it to a clean, fast square wave current which drives the preamplifier. In sine, triangle or DC functions, the square shaper input and output are disabled so as not to interfere with the selected waveform.

The preamplifier is fed from both the function switch and the square shaper. In all functions except AM, the preamplifier voltage output drives the output amplifier via the amplitude control. But when the AM function is selected, the voltage output (carrier signal) drives the amplitude modulator on the Sweep/Mod board.

The output amplifier receives input signals from a section of the function switch via the amplitude control and drives the output attenuator. DC offset is achieved by offsetting the output amplifier.

The output attenuator, fed directly from the output amplifier, provides up to 70 dB of attenuation to the selected waveform or DC offset. This signal is connected directly to the FUNC OUT BNC.

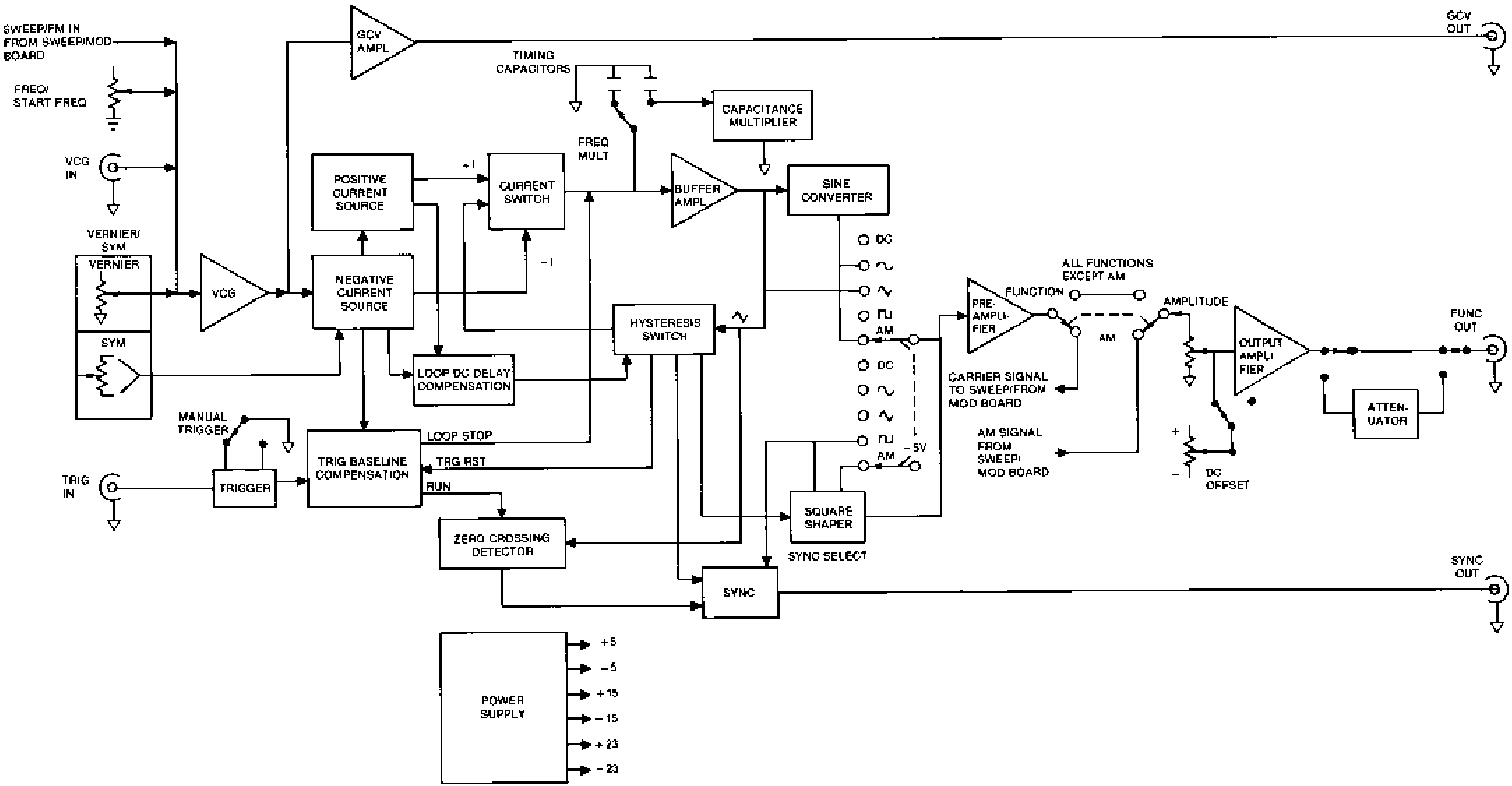


Figure 4-2. Main Generator Block Diagram

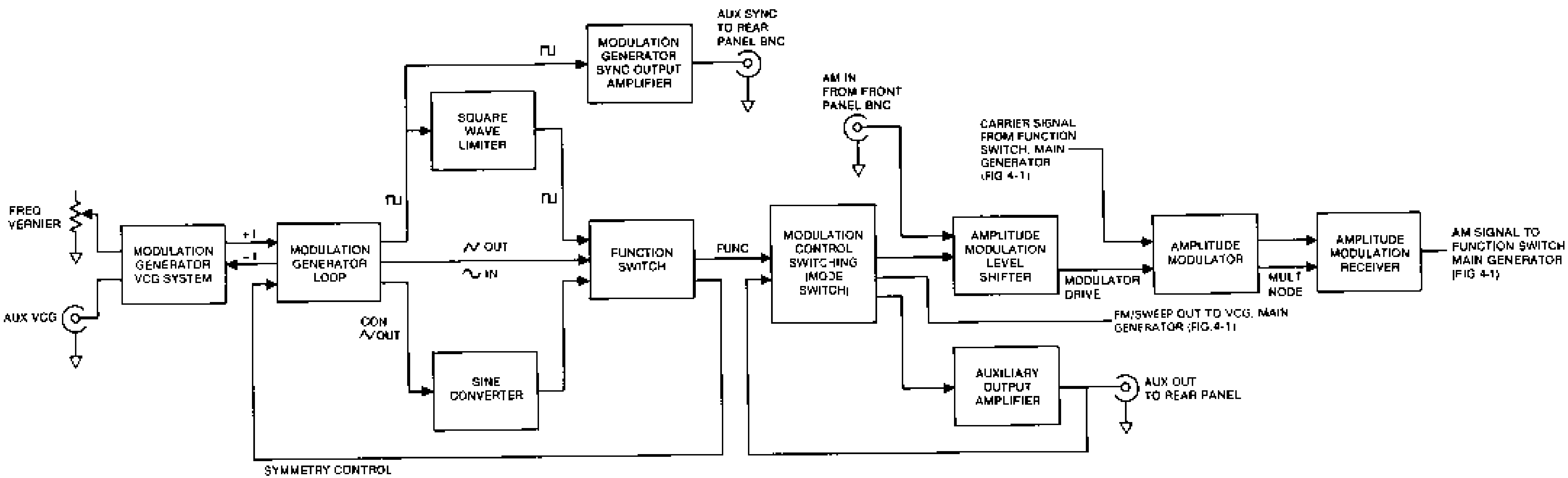


Figure 4-3. Sweep/Modulation Generator Block Diagram

4.3 SWEEP/MOD GENERATOR BLOCK DIAGRAM ANALYSIS

As shown in figure 4-3 the modulation generator VCG (voltage controlled generator) system sums voltage inputs from the FREQ VERNIER and AUX VCG input to provide a voltage control signal for the positive and negative current sources. The positive and negative current sources generate precision currents, linearly related to the VCG system output, which controls the modulation generator loop.

The modulation generator loop produces triangles and square waves whose frequency is related to the magnitude of the current from the modulation generator VCG system and the FREQ (Hz) range selected.

The sine converter accepts the 5 Vp-p triangle from the modulation generator loop and converts it to a 5 Vp-p sine wave. The sine converter output is routed to the function switch. The square wave limiter receives a square wave input directly from the modulation generator loop and shapes the square wave to drive the function switch.

The function switch selects the sweep/modulation generator's output waveform, either a sine, triangle or square wave. Also, the function switch enables the SYMMETRY control when pulse or sawtooth function is selected.

The modulation control switching (sweep/generator's MODE switch) selects how the sweep/modulation generator will modulate the main generator. When internal sweep or FM is selected, the switching circuit routes the modulating waveform to the VCG of the generator board. Or, if AM is selected, the circuit routes the modulating waveform to the amplitude modulation level shifter.

The auxiliary output amplifier performs two functions. First, it provides a method of controlling the level (WIDTH/ΔF/ΔM) of the modulating signal which is routed back through the modulation control switching to the amplitude modulation level shifter. Second, it supplies an output signal of the same frequency and function as the modulating signal to the AUX OUT. The Output level is proportional to the modulating signal.

The amplitude modulation level shifter sums inputs from the modulation control switching (internal AM) and AM IN (front panel). It shifts the dc level of the waveform and drives the amplitude modulator. The level shifter output level depends upon the suppressed carrier switch position, double side band up to 2.5 Vp-p (max.) offset between −2.2 and −3.7V; suppressed carrier up to 5Vp-p (max.) offset between −2.2 and −2.5V.

The amplitude modulator then mixes the waveform from the level shifter (Modulator Drive) and a sine wave (Carrier Signal from the main generator). The differential output from the modulator drives the amplitude modulation receiver, which converts the differential input to a single ended output. This signal is routed back to the output amplifier at the main generator.

The modulation generator sync output amplifier converts the square wave from the modulation generator loop to a TTL square wave (0 to +5V open circuit) that drives the AUX SYNC BNC.

4.4 DETAILED MAIN GENERATOR BOARD CIRCUIT DESCRIPTION

4.4.1 VCG and Current Sources

Refer to the Generator Board Schematic sheet 4. The VCG IN (J7) Sweep/FM input (from Sweep/Mod board) and FREQ VERNIER (R88) are summed with the FREQ/START FREQ dial potentiometer (R56) at the summing node, U14 pin 6 of the VCG amplifier. Full scale on the dial causes a −5 volt control signal at the dial buffer output U14 pin 7. Rotating the dial to minimum, plus turning the FREQ VERNIER ccw produces −5 mV at U14 pin 7. The output of the buffer drives both the GCV buffer and current sources. The GCV output at U14 pin 1 is +5.0 volts at full scale.

The voltage output from U14 pin 7 is present at U13 pin 1. The output of U13 at pin 12 is fed through level shifting transistor Q14 to U8 pin 6. The collector current at pin 7 flows from ground through R81 and R90. As the voltage at U14 pin 7 varies, amplifier U13 and transistor Q14 adjust the base drive of U8 pin 6, and hence the collector current, until the voltage at U13 pin 2 equals the voltage at U13 pin 1. Because U8 is an array of matched transistors with the bases connected together and all emitter resistors are equal with VERNIER selected, all collector currents are also equal.

The positive current source is controlled by a current control signal at U8 pin 1, which is held at 0 volts by the servo action of U13 pins 6, 7 and 10, level shifting transistor Q15 and U7 pins 6 and 7. The current "I" in R84 must flow through R93, and because these resistors are both 1kΩ, an equal but opposite base control voltage is present on U7 pin 6 compared to U8 pin 6. Because the transistors in U7 are matched and their bases are at the same point, a positive current "I" flows in R97 and hence the positive current source. A small amount of adjustable balance is provided by R95 and R94 to enable the positive and negative currents to be set for correct symmetry.

On the 1M and 10M ranges, the timing current is increased by approximately 25%, allowing the use of larger timing capacitors and hence, minimizing the effect of any stray capacitance. On the higher ranges, the parallel resistance across R83 (at ISCAL) is greater than the resistance on the lower ranges. This would decrease the current through U8 pin 8 were it not for the servo loop action of U13 pin 12, Q14 and U8 pins 6, 7 and 8. For any VCG setting at U14 pin 7 and U13 pin 1, no matter which range is selected, this servo loop maintains the voltage at U13 pin 2 equal to pin 1. Because the voltage at U13 pin 2 remains constant from range to range, the voltage across, and therefore the current through R80 and R81 also remains constant. This current also flows through U8 pins 7 and 8. To enable this current to remain constant, the servo loop drives the base voltage at U8 pin 6 in a positive direction. Because all of the bases in U8 are at the same point, the current relative to the lower ranges increases in R84 through R87 and also in the collectors of U8 pins 1, 14, 2, and 9.

Variable symmetry is controlled by R88 which doubles as the frequency vernier. With VERNIER selected, R88 functions as a frequency vernier with one end of the control connected to ground and the other connected to the −15 volt supply. The wiper supplies current to the summing node U14 pin 6. Additionally, one end of 1kΩ resistors R84 through R87 are all connected to the −15 volt supply. For any given dial setting, the current through each of the four resistors is "I". With SYM selected, R88 functions as a variable symmetry vernier with the wiper connected to the −15 volt supply. One end of this vernier supplies current to R84 and R85, while the other end supplies current to R86 and R87. With the vernier centered, each leg is approximately 5000Ω and reduces the current through each of these 4 resistors to 1/10 I, dividing the generator frequency by 10. As the symmetry control is varied, emitter resistance in the positive and negative current sources change unequally, hence the current sources are unbalanced and the timing for the positive waveform is varied in respect to the negative waveform, resulting in variable symmetry.

Loop delay dc compensation currents (+ICMP and −ICMP), are supplied by Q16 and U8 pin 9 and track the timing currents.

A current (ITRGBL), is supplied by U8 pin 14 to the trig baseline circuit to compensate for variations in dial settings when the generator is in a quiescent trigger or gated mode.

4.4.2 Current Switch

Refer to sheet 3. The current switch is driven by the square wave signal (ISWCTRL) from the hysteresis switch. Level shifting transistor Q15 provides a control signal for the diode bridge CR8, CR9, CR30 and CR31. When the control signal is +1.8 volts, CR30 is reversed biased, allowing CR8 to conduct current from the positive current source to the timing capacitor selected by SW9-D. This produces a positive going ramp. CR31 is also turned on, which reverse biases CR9 and prevents current sinking from the timing capacitor to the negative current source. When the control signal is −1.8 volts, both CR30 and CR9 are forward biased, while CR31 and CR8 are reversed biased. At this time, current from the negative current source sinks from the timing capacitor, producing a negative going ramp.

4.4.3 Triangle Buffer Amplifier

Refer again to sheet 3 of the schematic. The signal on the selected timing capacitor is present at both the gate of Q11, and at U9 pin 2. These devices provide a very high input impedance for the signal to avoid leakage which would otherwise cause poor triangle linearity. The output current of Q11 controls the base drive to emitter follower Q13 and hence the output voltage on the emitter. This voltage is sensed at U9 pin 3, causing U9 to adjust the base voltage of Q12 until the differential input of U9 is zero. The low impedance source output voltage at the emitter follower Q13 now follows the high impedance input signal at the gate of Q11 with a circuit gain of unity.

4.4.4 Hysteresis Switch

Refer to sheet 2. U10 pin 5 is the input to the positive peak comparator, while pin 10 is the input to the negative peak comparator. A level shifted triangle signal of −0.9 volts to −2.8 volts is present at pins 5 and 10 of U10. Assume a positive going ramp. R18 and R19 set the reference voltage on U10 pin 4 at −0.9 volts. When the voltage on pin 5 exceeds the reference voltage on pin 4, the positive comparator changes state and the voltage on pin 3 pulses from an ECL low (−1.8V) to an ECL high (−0.8V). This signal is connected to clear direct (pin 4) of D flip flop U5. The output of U5 pin 2 goes low, while U5 pin 3 goes high. These outputs toggle the differential pair Q7 and Q8 so that Q7 is on and Q8 is off. This causes the current switch control signal (ISWCTRL) to go low, which connects the negative current source to the timing capacitor, and causes the triangle to begin to ramp negative. The negative peak comparator functions in an identical manner to the positive comparator except that the reference voltage at U10 pin 9 is −2.8 volts. At the negative triangle peak, U10 pin 6 pulses high causing a set direct at U5 pin 5, toggling the current switch signal (ISWCTRL) high and producing a positive going ramp. In addition to being used to store the first peak comparison pulse from U10 pins 3 and 6, U5 also ignores "chatter" from both positive and negative comparators.

4.4.5 Loop DC Delay Compensation

The circuit is also located on sheet 2 of the schematic diagram. The purpose of this circuit is to adjust the reference voltages on the comparators in the two highest frequency ranges so that the triangle peaks do not increase in amplitude due to loop delay. Q2 functions as a variable positive current source controlled by the range switch and the main current source. As the generator frequency is increased, the base voltage of Q2 progressively moves negative causing positive current through R15 and increasing the reference voltage on U10 pin 9 in a positive direction. This causes the negative peak to switch earlier in time, compensating for the loop delay and maintaining constant triangle amplitude and correct frequency tracking.

The positive peak comparator reference is changed in an identical way, except that the voltage on U10 pin 4 becomes more negative with increased frequency. Q4 is a variable negative current source. Q1 and Q3 function as temperature compensating diodes.

4.4.6 Capacitance Multiplier

Refer to schematic diagram sheet 5. The capacitance multiplier is a precision current splitter which shunts up to 99.990% of the VCG current away from the integrating capacitor (C57) to produce the 100 through 0.1 frequency ranges. Timing current is divided between C57 and R114, then again between R113 and the selected timing resistor (R110 through R112 or R106).

The signal at U11 pins 2, 6, and 7 is a ±1.0 volt triangle. U11 (pins 6, 7, and 10) is a non-inverting amplifier with a gain of 8. The waveform at U11 pin 1 is a ±1.0 volt triangle with 0.5 volt spikes at each peak. At any given moment, the junction of R103 and C55 (differentiator circuit input) has 8 times the voltage as the junction of R104 and C55. This voltage difference causes a constant current to charge C55 through R104 and the selected timing resistor. Thus a frequency dependent charging current flows into the summing node of U11 pin 1, producing an inverted square wave component at the differentiator output U11 pin 12 sinking or sourcing current from the main current sources and limiting the amount of current available to charge C57. The ±1.0 triangle at U11 pin 2 provides the triangle portion of the waveform at U11 pin 12. Since the triangle slopes on U11 pins 1 and 12 are identical, only the square wave component of the waveform at U11 pin 12 is across the timing resistor. The amount of current supplied to charge C55 is therefore this voltage divided by the range resistor value. As the range resistor is increased, the feedback for U11 between pins 1 and 12 is also increased, causing less current to charge C55 and increasing the amount of current being shunted to U11 pin 12 by a factor of 10 for each lower frequency range.

4.4.7 Sine Converter

Refer to sheet 6 of the schematic. The sine converter converts the buffered ±1.0 volt peak triangle to a sinusoidal current of 2mA peak. The input triangle voltage (TRIBUFC) passes through a voltage divider network to the input of the diode at pins 1, 4 and 6. As this signal progressively increases, the diode between pins 1 and 9 is progressively reversed biased, sinking less current and causing the diode between pins 2 and 5 to pass increasingly more current in a sinusoidal manner to IFUNC. This produces the positive half of the sine wave at the output of the preamplifier. At the same time, the diode between pins 2 and 8 is progressively reversed biased. This slows and eventually prevents current from flowing from the negative portion of the sine converter.

When the input waveform moves negatively, the diode between pins 2 and 5 is reversed biased and the diode between pins 2 and 8 progressively conducts, producing the negative half of the sine wave.

R159 sets the input amplitude for correct biasing of the sine conversion diodes, while R165 adjusts the input signal offset. Thermister R161 adjusts the input voltage to compensate for the diode voltage change with temperature. The network consisting of R166, R167 and C102 provides a signal (SINCMP) to the non-inverting input of the preamplifier to compensate for the effects of diode capacitance which would otherwise distort the sinewave peaks at high frequencies.

4.4.8 Trigger Circuit

Refer to sheet 5. The trigger input at J8 is added to the voltage from the trigger level control R119 and compared at U12 pin 5 with a reference at U12 pin 4. When the signal at U12 pin 5 exceeds pin 4 by a few millivolts, U12 pin 3 goes high. R120 and C60 ensure a noise free pulse at U12 pin 3 which is one of two wire ORed inputs to U4 pin 7. The second input originates from the MAN TRIG switch circuit. When this switch is depressed, R115 pulls U12 pin 10 low. Pin 10 is compared to the Vbb reference voltage at pin 9, latching pin 6 high and preventing false triggering due to switch contact bounce. Pin 13 connected to pin 6, is referenced to pin 12, causing pin 15 to also go high. When either U12 pin 2 or pin 15 go high, U4 pin 3 goes low because these outputs are wire ORed to U4 pin 7. U4 pin 2 is connected to pins 4 and 10. Because pin 10 was previously high, U4 pin 14 was low causing a low at U4 pin 5. The trigger pulse low at U4 pin 4 causes a 10 ns ECL high pulse at U4 pin 2. At the same time, U4 pin 14 goes high and after the time delay set by R126 and C62, U4 pin 5 also goes high. This causes U4 pin 2 to return low.

In the gate mode CR14 holds U4 pin 11 high, forcing pin 14 low. The length of the control pulse at U4 pin 2 is now equal to the period during which U4 pin 7 is held high. In the continuous mode, U4 pin 2 is held high by CR16 regardless of any input trigger signals.

4.4.9 Trigger Baseline

Refer to sheet 5. In the trigger mode, with no trigger inputs, U5 pin 12 is held low. On the next positive going triangle, the trigger reset (TRIG RST) signal at U5 pin 11 causes U5 pin 14 to go high. This turns Q18 off and Q17 on, which turns off Q19. The Q19 emitter voltage is pulled down by the negative current sources Q20 and Q21, causing CR19 to conduct. Because the anode is at ground and CR18 is matched to CR19, the voltage at the anode of CR18 is also zero. This causes the triangle on the positive going ramp to stop at exactly zero volts. When a trigger signal occurs, U5 pin 12 goes high for about 10ns, causing pin 15 to also go high. This turns on Q18 and turns off Q17, which turns on Q19, causing the emitter to rise to about 1.7 volts. This reverse biases CR18 and CR19 causing the generator to run for exactly one cycle. In the gate mode, U5 pin 12 is held high for the duration of the input signal causing the generator to run for this interval plus the time required to complete a partial cycle.

In the trigger or gated mode, quiescent state, positive charging current I flows in CR18. As the VCG current is varied, I also varies, causing the voltage across CR18 to vary. To prevent this from causing a baseline shift, current (I) must also flow in the reference diode CR19. A negative current source (ITRGBL) is connected to the bases of Q20 and Q21. Negative current (− I) flows through the collector of Q20 and R133. Because of the configuration of Q20 and Q21, and because R133 and R134 are both 1kΩ, an equal amount of current − I also flows through the collector of Q21 and R134, causing − 2I to flow at the junction of R133 and R134. Half of this current (− I) flows through CR19, while the remaining current flows through CR18. Therefore, the anode of CR19 is held at zero volts regardless of the VCG summing node current.

The RUN signal is used to hold the sync output low during quiescent periods.

4.4.10 Sync

Refer to schematic sheet 2. The SYNC OUT amplifier is driven from the signal at U6 pin 10 in the triangle and sine functions, and from U6 pin 7 when the function switch is in the square function. These two inputs are wire ORed at U6 pin 13.

In the triangle and sine functions, SYNC SEL allows R23 to pull CR4 high causing a low at U6 pin 2. This enables the signal from the zero crossing detector output (U10 pin 15), and disables the hysteresis switch input at U6 pin 7. When the positive going ramp crosses 0 volts at the zero crossing detector input U10 pin 13, U10 pin 15 and U6 pin 10 go high. This causes a low at U6 pins 14 and 13. U6 pin 9 goes low and pin 15 goes high turning on Q5 and turning off Q6. This results in a high at SYNC OUT. As the triangle at U10 pin 13 crosses 0 volts in a negative direction, pin 15 goes low, causing Q6 to be turned on, producing a low at SYNC OUT. Therefore the SYNC OUT always toggles when the triangle crosses 0 volts.

When the square wave function is selected, CR4 pulls U6 pins 4 and 6 low. U6 pins 2 and 11 now go high, disabling the zero crossing detector input from pin 10, and enabling the square wave input from U6 pin 7. U5 pin 3 now drives the SYNC OUT connector in a similar manner as U10 pin 15. The SYNC OUT is in phase with the square wave output.

R26, a 49.9Ω resistor sets the 50Ω output impedance.

4.4.11 Square Shaper

The square shaper schematic is located on sheet 6. In square function, CR20 pulls U4 pin 13 low, enabling the hysteresis switch input (HYS) at U4 pin 12. A low at U4 pin 12 causes a low at U4 pin 15 and a high at pin 9. Q22 turns on while Q23 is turned off, producing a + 1.2 volt high at the bases of the current switch control transistors Q24 and Q25. Transistor Q25 is on, reverse biasing CR23. Transistor Q24 is off allowing positive current to flow through R147, CR22, R154 and into the preamplifier node via R152.

When $\overline{\text{HYS}}$ toggles high, Q23 turns on forcing the bases of Q24 and Q25 to − 1.2 volts. Q24 turns on and Q25 turns off, allowing negative current to flow through R157, CR23, R154 and the the amplifier node via R152.

R152 and R154 form a current divider to obtain a 2mA full scale current into the preamplifier. Overshoot caused by diode capacitance is reduced by R153 and C73. The output of the square shaper is disabled in all other functions by turning on Q26 and CR24 which reverse bias CR22 and CR23 and prevents current from flowing through R152.

4.4.12 Preamplifier

Refer to sheet 7 of the schematic circuitry. For all functions, full scale output voltage is produced when 2mA is injected into the input summing node U1 pin 8. Transistor array U1 forms a cascaded differential stage. Transistor Q27 is a fixed current source. Q28 and Q29 form a high gain voltage follower. DC negative feedback is applied through R195 to U1 pin 8. The closed loop voltage gain of the amplifier is determined by the ratio of R195 to the input resistors, R152 for square wave and R176 for triangle. The sine converter output supplies the correct current directly from U3 pin 2 to U1 pin 8. The servo action of the preamplifier holds this point at 0 volts, therefore no voltage can be measured. U1 pin 4 is the non-inverting input and is used both to adjust the offset to 0 volts at TP2 using R185 and to inject the sine converter compensation signal (SINCMP) described under paragraph 4.3.7, Sine Converter. High frequency compensation is provided by R182, C81, C86 and C153. Zener diode CR29 provides increased collector voltages for U1 pins 11 and 12 and also allows these two points to be relatively close in voltage.

4.4.13 Output Amplifier

The output amplifier consists of an ac coupled amplifier for signals above about 16 kHz, and a dc coupled amplifier for signals below about 16 kHz, and to maintain zero dc output offset within specified limits. Refer to the simplified output amplifier schematic, figure 4-4.

Assume zero input voltage at the junction of R203 and R218. The output at R222 and R224 is maintained at 0 volts by dc amplifier U2. U2 pin 3 is connected to a 0 volt reference. If the output drifts away from 0 volts, this will be sensed at U2 pin 2 through R256, R257 and R254. Amplifier U2 will sense a difference between its inputs and produce an output voltage which adjusts the bias in the ac coupled amplifier to return the output to 0 volts. Because R218 and R223 form half of a balanced bridge, and R253, R256 and R257 form the second half, the amplifier node at the junction of R218 and R223 will be held at 0 volts as U2 has returned the junction of R253 and R256 to 0 volts.

A dc input of +1 volt at R218 and R253 is sensed as a positive increase at U2 pin 2, causing U2 pin 6 to go negative. The ac amplifier output goes negative in response to the dc control input. This continues until the output becomes sufficiently negative to sink all the input current, and return U2 pin 2 to 0 volts. The bridge circuit causes the ac amplifier node to be 0 volts. If the input is +1 volt and the node at the junction of R218 and R223 is 0 volts then the input current is 8.26 mA which flows through R223 to produce an output voltage of −16.52V. Therefore the amplifier voltage gain is 16.52 (R223/R218).

Above about 16 kHz, the ac amplifier controls the summing node directly, sinking or sourcing current through R223 by adjusting the output voltage to hold the node at 0 volts. The ac amplifier gain is also R223/R218 = 16.25. This is divided by 2 at the output terminal, due to the 50Ω source impedance resistors R222 and R224, providing the output is also terminated into 50Ω.

Refer to sheet 7. The top half of the circuit amplifies

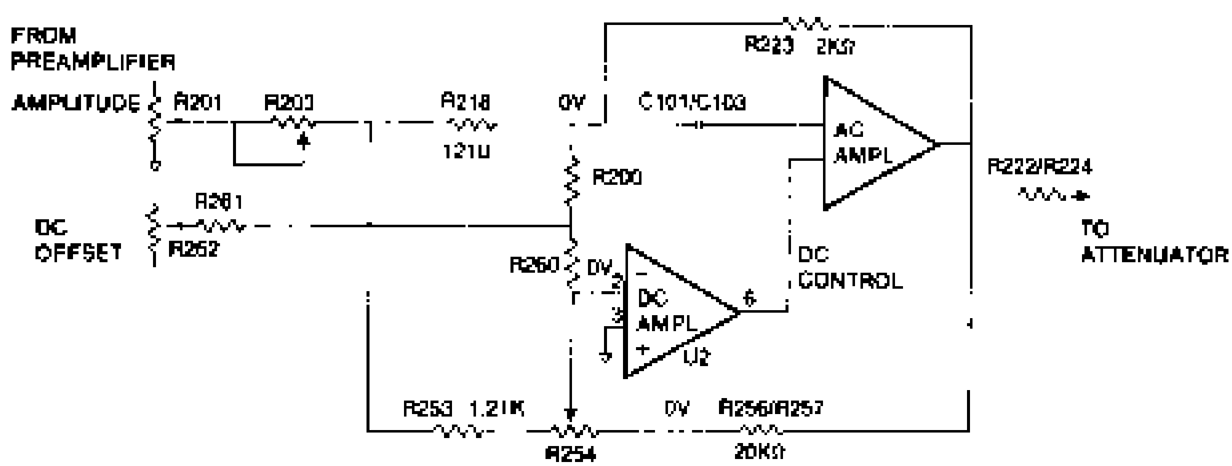


Figure 4-4. Simplified Output Amplifier

the positive portion of the signal, and the bottom half amplifies the negative part. Q30 and Q31 form an ac gain stage. An emitter follower stage is formed by Q32 and Q33, to provide a low impedance drive to the second voltage gain stage Q36 and Q39. This stage drives the parallel output emitter followers Q37 and Q38 on the positive side, and Q40 and Q41 on the negative. Diodes CR23 and CR26 set thermally stable bias for the output transistors. Networks R211, R212, C94 and C93 bypass emitter resistor R208, while R245, R246, C107 and C106 bypass R244. As frequency is increased, these components decrease the local negative feedback in the driver stage, increasing the high frequency gain. Voltage regulators VR5 and VR6 have external current limiting circuitry set to limit at about 220 mA to prevent damage in the event of a shorted transistor. When the offset button is depressed, offset current is injected directly into both nodes in proportion to the feedback resistor values. The amplifier responds exactly as described above for a dc input.

4.4.14 Output Attenuator

Also refer to sheet 7. Each attenuator button selects an independent voltage divider, which has 50Ω input and output impedances to correctly load the amplifier and to provide a constant 50Ω impedance at the FUNC OUT terminal.

The 10dB attenuator has a 3.16/1 voltage division ratio. The 20dB attenuator has a 10/1 voltage division ratio, and the 40dB stage has a 100/1 ratio. These ratios multiply in voltage. For example if the 20dB and 40dB buttons are depressed, the voltage division ratio is 1000/1. The attenuators add algebraically in dB, therefore any attenuation from 10 to 70dB may be selected in 10dB steps.

4.5 SWEEP MODULATION BOARD DETAILED CIRCUIT DESCRIPTION

4.5.1 Modulation Generator VCG System

Refer to Sweep/Mod board schematic sheet 1. The modulation generator VCG system consists of an input buffer, the positive current source, and negative current source.

4.5.1.1 Input Buffer

The input buffer U1 pin 7 sums inputs from the AUX VCG (J16) and FREQ VERNIER. The buffer drives both positive current source inverter U1 pin 2 and the negative current source U1 pin 9. With FREQ VERNIER full cw and no AUX VCG input, the buffer supplies −0.546V, and −0.014V with FREQ VERNIER full ccw.

4.5.1.2 Positive Current Source

U1 pin 1 is an amplifier with a gain of −1 that drives the positive current source U1 pin 13.

The positive current source produces a current that charges the modulation generator loop timing capacitor. The positive current source receives its input at U1 pin 13. The output U1 pin 14 is dc coupled by a zener diode CR1 and resistor R13, which shifts the dc bias, to the two bases U2 pins 11 and 14. The base bias U1 pins 11 and 14 controls the emitter currents U1 pins 10 and 13. Emitter resistors R14 and R16 are matched and supplied by the same +15V supply, thus providing equal emitter currents and, consequently, equal collector currents. The collector current U2 pin 12 flows through resistor R17 and the function switch, to the negative current source. The collector U2 pin 12 connects to U1 pin 12, this provides the feedback to stabilize the positive current source. The collector current at U2 pin 15, which equals the collector current U2 pin 12, flows to the current switch in the modulation generator loop (see paragraph 4.5.2.1). The RC network R12 and C1, across U1 pins 12 and 13, provide loop stabilization.

4.5.1.3 Negative Current Source

The negative source is similar to the positive source, except it supplies the current that discharges the modulation generator loop's timing capacitor. The negative current source receives its input at U1 pin 9 from the input buffer U1 pin 7. The amplifier output U1 pin 8 drives the two transistor bases U2 pins 5 and 8 via the dc bias shifter CR2 and R23. As with the positive current source, the emitter resistors R24 and R26 are matched and biased to the −15V supply, therefore, the collector currents U2 pins 6 and 9 are equal. U2 pin 9 drives the current switch in the modulation generator loop (refer to paragraph 4.5.2). The RC network, C2 and R22, across U1 pins 9 and 10 provide loop stabilization.

4.5.1.4 Symmetry Control

When the function switch is set to a symmetrical waveform: sine, triangle or square, the symmetry control R19 is shorted out. This allows the current to flow directly from the positive to the negative current source.

But if the ramp or pulse is selected, SW2-B connects the wiper of the SYMMETRY potentiometer to circuit ground, and SW2-C opens the short across R19. This increases the total resistance in the string R17, R19, R21 by ten times, thus reducing the current and frequency to 1/10th. As the SYMMETRY potentiometer is rotated from one end to the other, one current increases as the other decreases, thus changing the slope of each half cycle over a 19:1 range without changing the frequency.

4.5.2 Modulation Generator Loop

Refer to Sweep/Mod board schematic sheet 1. The modulation generator loop consist of the current switch, timing capacitors and triangle buffer, and hysteresis switch.

4.5.2.1 Current Switch

The current switch selects which current source will charge or discharge the timing capacitor. The hysteresis switch U13 pin 6 controls the current switch.

When the hysteresis output is high (+3V), diode U3 pins 4 and 9 conducts current, Q2 is reverse biased, and the positive current source charges the timing capacitor. In addition, transistor Q1 is forward biased, thus reverse biasing diode U3 pins 3 and 4, this sinks the negative current source to the +15V supply.

When the hysteresis output is low (−3V), diode U3 pins 3 and 4 is forward biased, this reverse biases transistor Q1, the current now flows from the timing capacitor through the diode U3 pin 3 and 4 to the negative current source. Meanwhile, transistor Q2 conducts current, which reverse biases diode U3 pins 4 and 9, thus the −15V supply sinks the current from the positive current source.

4.5.2.2 Timing Capacitor and Triangle Buffer

The timing capacitor C5 and C6 together with the currents from the current sources determine the frequency of the modulation generator loop. On two ranges 3 − 100 and 3K − 100K, the current sources directly charge and discharge the timing capacitors. But, on the .1 − 3 and 100 − 3K ranges, resistors R46 and R47 acts as a capacitance multiplier. R46 connects between the current switch and the timing capacitor, while R47 provides a shunt to 97% of the current, thus reducing the current at the timing capacitor to 3% of the current from the current sources.

The triangle buffer U12 pin 6, a unity gain non inverting amplifier, follows the voltage across the timing capacitor.

4.5.2.3 Hysteresis Switch

Refer to sweep/mod board schematic sheet 1 and figure 4-5.

The hysteresis switch U3 and U13 operates as a comparator. When the triangle input reaches the positive limit (+2.5V) the switch output toggles to −3V. And, when the triangle reaches the negative limit (−2.5V) the switch output toggles to +3V. The hysteresis switch output drives the current switch, square wave limiter, and modulation generator sync output amplifier. Figure 4-5 shows a simplified schematic and timing diagram.

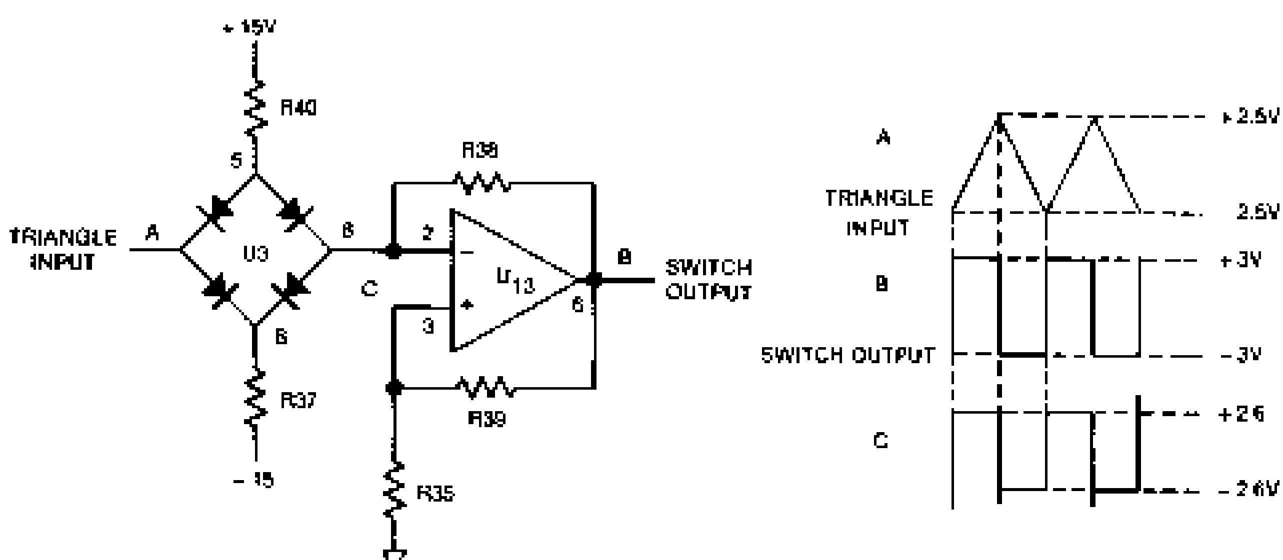


Figure 4-5. Hysteresis Switch

During the triangle's positive-going ramp, the hysteresis switch output is +3V. Current flows from the +15V supply through R40 and U3 pins 5 and 2 to the triangle buffer output U12 pin 6. At the same time, current flows from the hysteresis switch output U13 pin 6 through R38, U3 pins 6 and 8, and R37 to the −15V supply. Diodes U3 pins 5, 6 and 2, 8 are reverse biased. Resistor R38 provides negative feedback, while resistors R39 and R35 provide positive feedback.

As the triangle reaches the positive limit +2.5V, the diodes U3 pins 2, 8 and 5, 6 begin conduction. This also decreases the current through diodes U3 pins 2, 5 and 6, 8. This causes a positive increase in the voltage level at U13 pin 2. As U13 pin 2 becomes slightly more positive, with respect to pin 3, U13 pin 6 will instantaneously toggle to −3V.

During the triangles negative-going ramp, the current through diodes U3 pins 2, 8 and 5, 6 increases, while the current through diodes U3 pins 2, 5 and 6, 8 decreases and, eventually, cutoff.

As the triangle reaches the negative limit, −2.5V, the diodes U3 pins 6, 8 and 2, 5 begin conduction. This decreases the current through U3 pins 5, 6 and 2, 8, thus forcing U3 pin 2 slightly more negative, with respect to pin 3, which causes the output pin 6 to toggle to +3V.

4.5.3 Square Wave Limiter

Refer to Sweep/Mod board schematic sheet 1. The square wave limiter, which receives its input from the hysteresis switch, limits the square wave peaks to ±2.8V and routes the square wave to the function switch.

When the hysteresis switch output U13 pin 6 goes high (+3V), diodes CR4 and CR7 are foward biased, and diodes CR5 and CR6 are reverse biased. This allows current flow from the +15V supply, through R29, CR4 and R27.

The diodes CR5 and CR6 are forward biased when the hysteresis switch output is low (−3V), also diodes CR4 and CR7 are reverse biased. Now current flows from circuit ground through R27, CR6, and R28 to −15V supply.

4.5.4 Sine Converter

Refer to Sweep/Mod board schematic sheet 2. The sine converter circuit converts a buffered ±2.5V triangle to a ±2.5V sine waveform. The sine converter uses the nonlinear characteristics of the diode to convert a linear triangle slope to a sinusoidal curve. The sine converter consists of a diode network, buffer amplifier, and temperature compensated ±10V supplies. The triangle from the modulation generator loop is reduced in amplitude by resistors R41 and R42 and feeds the diode network U4 pins 3, 9 and 1.

The following section illustrates the operation of the diode network when shaping a sine wave.

At the negative peak of the input triangle the diodes U4 pins 3, 4 and 5, 6 are forward biased, which reverse biases U4 pins 2, 5. Also, diodes U4 pins 1, 9 and 6, 8 are cut off, which forward biases U4 pins 2, 8. When the input triangle slope increases from negative to positive peak, diodes U4 pins 1, 9 and 6, 8 begin to conduct, which decreases the current through U4 pins 2, 8. At the same time, diodes U4 pins 3, 4 and 5, 6 decrease conduction, which causes diode U4 pins 2, 5 to begin conduction. When the triangle reaches the positive peak, diode U4 pins 2, 5 is forward biased and U4 pins 2, 8 is cutoff. The current from the diode network U4 pin 2 drives the sine buffer U6.

Shaping the negative-going slope of the sine wave is similar to the positive-going slope. Except, when the input triangle ramps positive to negative, diodes U4 pins 1, 9 and 6, 8 decrease conduction and diodes U4 pins 3, 4 and 5, 6 increase conduction. This, eventually, forward biases diode U4 pin 2, 8 and reverse biases diode U4 pins 2, 5.

The sine buffer U6 pin 6 sums the currents supplied by the diode network to produce a 5Vp-p sine wave that drives the function switch.

The bias for the diode network is supplied by temperature compensated ±10V supplies. The +10V supply is amplifier U5 pin 1, with a gain of −2/3, which is referenced to the −15V supply. The −10V supply is amplifier U5 pin 7, with a gain of −1, which is referenced to the +10V supply. A temperature sensing device, RT1, adjusts the gain of the +10V supply, which gives the ±10V supplies a negative temperature coefficient.

4.5.5 Function Switch

Refer to Sweep/Mod board schematic sheet 1. The function switch selects the function (waveform) of the sweep/mod generator. Wafer SW2-A routes the selected function, (sine, triangle or square) to SW3-D of the Modulation Control switching. Wafers SW2-B and C control the current source when a pulse or sawtooth function is selected.

4.5.6 Modulation Control Switching

Refer to sweep/mod board schematic sheet 3. The modulation control switching, which selects the sweep/modulation generator operating mode, consists of the MODE and SUPPRESSED CARRIER switches.

The MODE switch is a four wafer switch. Wafer SW3-A, in AM and SET ΔM routes either a modulating signal (AM) or a dc level (SET ΔM) from the auxiliary output amplifier to the AM level shifter. Wafer SW3-B, when MODE is set to SWEEP, SET WIDTH, SET START, FM, SET ΔF, and SET FREQ, connects either a modulating signal (SWEEP and FM) or a dc level (SET WIDTH, SET START, SET ΔF, and SET FREQ) from the auxiliary output amplifier to the SWEEP/FM IN at the main generator VCG. Wafer SW3-C controls bias amplifiers U10 pins 1 and 7, part of the auxiliary output amplifier. Table 4-1 shows the bias amplifiers output levels relative to MODE switch settings. Wafer SW3-D controls the input conditions, via the WIDTH/ΔF/ΔM control, for the auxiliary output amplifier: for AUX OUT ONLY and AM SW3-D routes the waveform (FUNC) to one end (E5) of the WIDTH/ΔF/ΔM control; for SET ΔM, SET WIDTH, and SET ΔF SW3-D grounds one end (E5) of the WIDTH/ΔF/ΔM control; and for SET CARRIER, SET START, and SET ΔF SW3-D shorts out the WIDTH/ΔF/ΔM control.

The SUPPRESSED CARRIER controls the bias and gain of the amplitude modulation level shifter. When SUPPRESSED CARRIER is pressed, one section of SW4 shorts out R118, this increases the gain of the amplitude modulation level shifter, and removes R126, which was in parallel with R86. Also, the other section now supplies a +15V bias when SET ΔM is selected.

4.5.7 Amplitude Modulation Level Shifter

The amplitude modulation level shifter sums inputs from the modulation control switching (dc reference levels or ac waveforms), suppressed carrier switch SW4 (dc reference level), and the AM IN BNC J14 (an external signal). This circuit shifts the dc level, depending upon the position of the SUPPRESSED CARRIER switch, that drives the Amplitude Modulator.

4.5.8 Auxiliary Output Amplifier

Refer to sweep/mod board schematic sheet 3. The auxiliary output amplifier consists of a single amplifier U9. The amplifier input signal originates at the sine converter, square wave limiter, or modulation generator loop (triangle) and is selected by the function switch to be routed through the Mode switch of the modulation control switching to the WIDTH/ΔF/ΔM control. The WIDTH/ΔF/ΔM control varies the level of the auxiliary output signal. The output from U10 pin 7 provides dc offset to the inverting input of the auxiliary

Table 4-1. Bias Amplifier Levels Vs. Modes

Mode Switch	Suppressed Carrier Switch	Bias Amplifier Level U10 Pin 1	Bias Amplifier Level U10 Pin 7
SET FREQ AUX GEN OFF	No affect	+5V	+10V
SET ΔF	No affect	−2.5V	−5V
FM	No affect	0V	0V
SET START	No affect	0V	0V
SET WIDTH	No affect	−4.8V	−9.6V
SWEEP	No affect	−2.5V	−5V
SET CARRIER	No affect	0V	0V
SET ΔM	Off	+2.5V	+5V
	On	−2.5V	−5V
AM	No affect	0V	0V
AUX OUT ONLY	No affect	0V	0V

output amplifier U9 pin 2, the mode switch SW3-C controls the dc offset. Refer to the table on the schematic sheet 3. The auxiliary output signal feeds both the AUX OUT BNC and MODE switch SW3-A and B for sweep, frequency or amplitude modulations.

If the MODE switch is set to SET FREQ, SET START, or SET CARRIER, both ends of the WIDTH/ΔF/ΔM are shorted together, R108 has no affect. This biases the Auxiliary output amplifiers output to a level dependent upon the Mode SW3-C selected: 0V for SET CARRIER and SET START, and +5V for SET FREQ. This allows setting of front panel controls for the generator board.

If the mode switch is set to SET ΔF, SET WIDTH, or SET ΔM, a dc level, referenced to ground is connected to the WIDTH/ΔF/ΔM control. This level represents a dc equivalent of the modulating signal and allows static set up conditions of the main generator. The maximum dc level applied to the WIDTH/ΔF/ΔM control depends on the mode selected and SUPPRESSED CARRIER switch position, refer to table 4-1.

When AUX GEN OFF is selected, the output from U10 pin 7 (LOOP STOP) shuts off the current source in the modulation generator VCG system.

4.5.9 Amplitude Modulator

Refer to sweep/mod board schematic sheet 2. The amplitude modulator U7 is a wide-band four-quadrant multiplier that is configured as an amplitude modulator. The amplitude modulator produces an output current that is the linear product of the CARRIER SIGNAL U7 pin 9 and MODULATOR DRIVE U7 pin 8.

The CARRIER SIGNAL, originating at the main generator preamplifier (FUNC/AM only), drives the non-inverting X input U7 pin 9 with a fixed ± 3.2V sine wave. Resistors R73, R74, R75, and R76 bias the inverting X input U7 pin 12 at 0Vdc, this provides the reference voltage for the CARRIER SIGNAL.

The MODULATION DRIVE signal from the amplitude modulation level shifter, controls the inverting Y input. This signal level depends upon the type of AM selected: double-sideband modulation −2.5 to −5.0V (max) and suppressed carrier modulation 0 to −5.0V (max). The MODULATION DRIVE signal is referenced to −2.5V at the non-inverting Y input U7 pin 4.

The modulator outputs U7 pins 2 and 14 each receive 4 ma current from the amplitude modulation receiver. The modulator differentially varies these currents up to ±2 ma.

4.5.10 Amplitude Modulation Receiver

Refer to sweep/mod board schematic sheet 3 and figure 4-6. The amplitude modulation receiver converts the differential current from the amplitude modulator to a single-ended output signal, which drives the output amplifier of the main generator. The receiver consists of two amplifiers (a bridge amplifier and output amplifier) and a resistor bridge.

To best understand this circuit refer to the simplified schematic figure 4-6. Basically, resistors R92, R93, R101, and R103 form a resistor bridge. When the currents I6 and I7 from the modulator outputs U7 pins 14 and 2 are equal, the bridge is balanced and the output E2 is 0V.

The amplitude modulator differentially varies the currents I6 and I7. For example, when I7 increases and I6 decreases, both an equal but opposite amount, current I2 increases, while current I3 remains unchanged. This increases the voltage E1. As a result, current I4 increases, but the modulator demands less current I6. Therefore, the current I5 flowing through R103 equals the difference between I6 and I7. Thus, E2 swings negative.

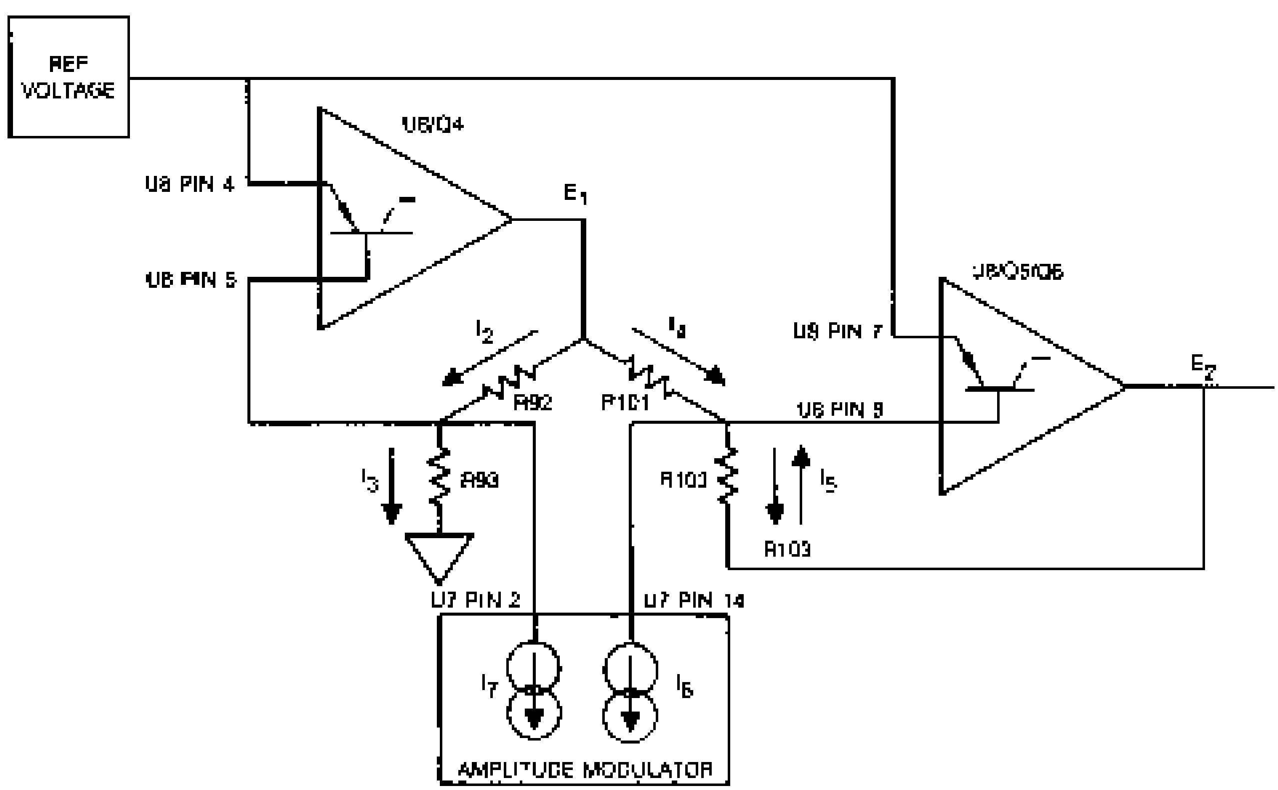


Figure 4-6. Amplitude Modulation Receiver

For the opposite polarity, the modulator demands less current I7 at U7 pin 2 and more current I6 at U7 pin 14. This decreased current I7 decreases the voltage E1 which decreases the current I4. But now, the modulator output U7 pin 14 demands more current I6 all of which cannot be supplied by current I4 and the difference in current must be supplied by I5. Output voltage E2 now swings positive.

The bridge amplifier (sections of U8 and Q4) supplies the drive voltage E1 for the resistor bridge. It supplies all the current for the R92, R93 legs of the bridge, and part of current for the R101, R103 leg of the bridge.

The output amplifier (sections of U8 and Q5/Q6) supplies the receiver output signal E2. This voltage E2 serves two functions; it supplies the AM signal which drives the main generator output amplifier, and provides a current source or sink for a portion of the resistor bridge.

Both amplifiers are tied to a common reference voltage. Resistors R95 and R100 bias transistors U8 pin 14 and U8 pin 11 (see sweep/mod schematic sheet 3) which serve as active loads for the input transistors of the amplifiers. These active loads set the emitter currents from U8 pins 4 and 7. The emitter currents collectively pass through R129 to ground. The voltage drop across R129 provides the reference voltage for the amplifiers.

4.5.11 Modulation Generator Sync Output Amplifier

Refer to sweep/mod board schematic sheet 1. The modulation generator sync output amplifier, driven by the hysteresis switch of the modulation generator loop, provides a TTL level output at AUX SYNC OUT J17. The amplifier Q3 is a transistor switch that is turned off and on by the driving square wave. This causes the collector of Q3 to switch between +5 and 0V (no load).

SECTION 5
CALIBRATION

5.1 FACTORY REPAIR

Wavetek maintains a factory department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

5.2 REQUIRED TEST EQUIPMENT

Voltmeter	Millivolt dc measurement (1% accuracy), true rms
Oscilloscope, Dual Channel	100 MHz bandwidth
Counter	20 MHz (0.01% accuracy)
50Ω	± 1.0% accuracy, 2W
Distortion Analyzer	To 200 kHz
RG58U Coax Cable	3 ft length BNC male contacts
Spectrum Analyzer	To 20 MHz

5.3 COVER REMOVAL

NOTE

Before removing the covers, disconnect the instrument from the ac power source.

Invert the instrument and remove the four screws in the bottom cover. Remove the bottom cover.

NOTE

Remove the cover only when it is necessary to make adjustments or measurements.

5.4 CALIBRATION

After referring to the following preliminary data, perform calibration, as necessary, per table 5-1/5-2. If performing partial calibration, check previous settings and adjustments for applicability. Figure 5-1 shows generator board calibration points while figure 5-2 shows sweep/mod board calibration points.

NOTE

The completion of the calibration procedure returns the instrument to correct alignment.

CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS

Instrument specifications are given in Section 1 of this manual.

1. All measurements made at the FUNCTION OUT connector must be terminated into a 50Ω (± 1.0%) load.

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

2. Start the calibration by removing covers as described in paragraph 5.3, connecting the unit to an ac source and setting these front panel switches as follows:

SYM	Off (extended)
TRIG LEVEL	12 o'clock
DC OFFSET	Off (extended)
OUTPUT ATTEN	0 dB (all extended)
AUX GEN MODE	SET FREQ/AUX GEN OFF

3. Allow the unit to warm up at least 2 hours for final calibration. Keep the instrument covers on to maintain heat. Remove covers only to make adjustments or measurements.

Table 5-1. Generator Board Calibration Procedure

Note: Where there are no entries, open column indicates previous entry is applicable.

Step	Test	Freq/Start Freq	Freq Mult	Vern/Sym	Mode	Func	Ampl	Test Point	Tester	Adjust	50Ω Load	Result	Remarks
1(1)	+15V Reference	2.0	1K	CW	CONT	Sq	CW	Board +15V	DVM	R[illegible]	No	+15 ± .75 VDC	Ref. std is [illegible]
1(2)	—	—	—			—	—	Board −15V		Verify	—	−15 ± [illegible] Vdc See remarks	−15V = +15V reading ±10 mV, [illegible] R[illegible]
2	+5V Supply	—		—	—	—		+5V	—			+5 ± .25 Vdc	
3	−5V Supply	—	—	—	—	—		−5V	—			−5 ± .25 Vdc	
4	+21V Supply	—	—			—	—	FB1	—			+21 ± 1.15 Vdc	
5	−21V Supply		—	—		—	—	FB2	—	—		−21 ± 1.15 Vdc	
6	Power Amp Zero		—	—	—	DC	CCW	FUNC OUT		R270	Yes	0 ± 20 mVdc	
7	Preamp Zero	—		—	—	—	CW	—	—	R155	—		
8	[illegible] Dial Symmetry			—	—	Sq		—	Scope	R66		Asym < 1%	Set for min asym. (Set by alternate triggering of scope + slope.)
9	VCO Null	.02	100K	—	—	—		—	—	R65	—	See remarks	Set for min freq shift when VCO is [illegible]. Repeat steps 8 and 9 as necessary.
10	100K Symmetry	—		—			—	—		R44	—	Asym < 1%	Set for min asym.
11	100K Frequency	—	—	CCW	—	—	—		Counter	R61	—	100K + 0 − 200 Hz	
12	Triangle Offset	2.0	1K	CW		Tri	—	—	DVM	R17	—	0 ± 20 mVdc	
13	Sine Distortion	—	—		—	Sine	—		Dist Analyzer	R159 R165	—	< 1.8%	
14	Triangle Trigger Baseline		—	—	TRIG	Tri	—	—	DVM	R51	—	0 ± 20 mV	
15(1)	Dial Alignment		—	—	CONT	Sq	—	SYNC OUT	Counter	R[illegible]	—	2 kHz ± 10 Hz	
15(2)	—	.02	—	—	—			—	—	Verify		200 ± 10 Hz	If satisfactory skip to step 15(5)
15(3)		See remarks	—			—	—		—	R41	—	2.08 kHz ± 10 Hz	Remove dial and set the shaft [illegible]
15(4)	—		—	—	—					See remarks	—	200 ± 10 Hz	Replace dial, tighten [illegible] set screw and verify setting
15(5)	—	2.0	—	—	—		—	—	—	R8	—	2.00 ± 40 Hz	
16(1)	20M Frequency		10M	—	—		—	—	—	C37	—	20 MHz ± 500 kHz	Change C36 value if setting is out of range for C37
16(2)	—	See remarks		—	—	—		—	—	Verify	—	Dial mark ± 600 kHz	Verify frequency at each major dial mark
17(1)	Xtal Frequency	2.0	1M	CW	CONT	Sq	—	SYNC OUT	Counter	Verify	—	2 MHz ± 40 kHz	Trim C33 in [illegible] between 2.020 and 2.040 MHz
17(2)	100K Frequency	—	100K			—	—				—	200 ± 4.0 kHz	Optimize R35 value if necessary
19	Capacity Mult Symmetry	.01	100	—	—	—		FUNC OUT	Scope	R126		< 3.0%	Set for min asym. Very important for low freq sine dist.
20(1)	Capacity Mult Frequency	2.0		—			—	SYNC OUT	Counter	R127	—	199.5 ± .5 Hz	
21	Low Frequency Aberrations		1K	—	—	—		FUNC OUT	Scope	R254	—	See remarks	Adjust the "Corner Shape" for [illegible] acceptable peaking
22(1)	Function Output Amplitude			—		Sine	—	—	DVM	R303		5.35 Vrms ± .01V	Verify sine output for ampl
23	High Frequency Aberrations	5	10M	—	—	Sq	—		Scope	R245 R211	—	< 0.6 Vp-p	Initial wave aberrations not to exceed 4% of full amplitude each peak

Table 5-2. Sweep/Mod Board Calibration Procedure

NOTE: Replace the bottom cover, turn the instrument upright and remove the top cover. The following adjustments are located on the Sweep/mode Board. Set the AUX GEN controls as follows: WIDTH/ΔF/AM . . . . cw. SYMMETRY . . . cw.

Step	Test	Freq (Hz)	Vernier	Aux Gen Func	Aux Gen Mode	AM Carrier Level/ Null	Suppressed Carrier	Main Generator FUNC	Main Generator Freq/Start Freq and Mult	Test Point	Adjust	Tester	Results	Remarks
1	Auxiliary Output Zero	100 3 KHZ	CW	Tri	SET START	CW	On (unchanged)	Sqr	2.0 x 1K	AUX OUT (no load)	R109	DVM (DC)	0 ± 5 mVdc	
2(1)	Triangle Peak Adjustment	—			AUX OUT ONLY	—	—	—		—	R[illegible]	—	[illegible] ± 5 mVdc	
2(2)	—	—			—	—	—			—	R[illegible]	DVM (see remarks)	2.83 ± 0.1 Vrms	True rms reading AC voltmeter
3(1)	Top of Range Symmetry and Frequency	2 100 HZ	—	Sqr	—		—	—	—	—	R18	Scope and Counter	ASYM < 2% of period	Short either outside leg of the SYMMETRY pot (R19) to circuit ground before performing steps 3 and 4. Using scope, match the period of the positive half cycle to the negative half cycle while monitoring the frequency on the counter. Adjusting R18 and R20 affects frequency.
3(2)		—	—	—	—	—	—	—	—	—	R20	—	—	
3(3)	—		—	—	—			—	—	—	Verify		100 ± 1 Hz	Repeat step 3(1) and (2) if necessary
4	Bottom of Range Symmetry Adjustment	3K 100 KHZ	CCW	Sqr	—	—	—	—	—	—	R12	Scope	ASYM < 1%	Set for minimum asymmetry. Remove ground short from SYMMETRY pot (R19).
5	Bottom of Range Frequency Adjustment		—	—	—			—	—	—	R2	Counter	[illegible]	
6	Capacitance Mult Balance	100 3 KHZ			—	—	—	—	—	—	R45	Scope	ASYM < 2% of period	Set for minimum asymmetry
7	Sine Distortion	—	CW	Sine	—	—	—		—	—	R[illegible] and R[illegible]	Distortion Analyzer	Adjust for minimum distortion < [illegible]% typical	
8(1)	Sine Zero and Amplitude Set	—	—	—	—			—	—	—	R[illegible]	DVM DC	0 ± [illegible] mVdc	
8(2)			—	—	—	—	...		—	—	R[illegible]	DVM (see remarks)	[illegible] ± 0.[illegible] Vrms	True rms reading AC voltmeter
9	Modulation Null	3 100 Hz	—	Sqr		12 o'clock	In (Suppressed)	AM	2.0 x 10K	FUNC OUT 50Ω	R[illegible]	Scope	Null < 50 mVp-p	Trigger scope from AUX SYNC OUT. Set scope: vert. 10 mV/div; hor. 2 ms/div
10	Carrier Zero	—	—	—	AM	See remarks	...	—	—	—	R73	—	See remarks	Set scope to display 2 cycles. Merge both traces using CARRIER NULL and R73 so the peaks of both square waves coincide.

Table 5-2. Sweep/Mod Board Calibration Procedure (Continued)

Step	Test	Freq (Hz)	Vernier	Aux Gen Func	Aux Gen Mode	AM Carrier Level/ Null	Suppressed Carrier	Main Generator Func	Main Generator Freq/Start Freq and Mult	Test Point	Adjust	Tester	Results	Remarks
11 (1)	Multiplier Zero	0-100 Hz	cw	Sine	SET AM	See remarks	On (depressed)	Sine	2.0 x 1K	[illegible] OUT (50Ω)	NA	DVM (dc)	See remarks	Note voltmeter reading for reference in step 11 (2). CARRIER LEVEL/NULL remains unchanged from step 10.
11 (2)	—	—	—	—	—	—		AM	—	—	R96	—	—	Adjust R96 for voltage referenced in step 11 (1) ± 10 mV.
12 (1)	Carrier Amplitude	—	—	—		—	—	Sine			NA	DVM (See remarks)		Using a true rms AC voltmeter, note reading for reference in step 12 (2).
12 (2)	—	—	—	—	—	—		AM	—	—	R70	—	—	Adjust R70 for voltage referenced in step 12 (1) ± 20 mV rms.
13 (1)	Sweep Width		—	—	—	—		Sine	2.0 x 100K	—	NA	Counter	—	Note the frequency for reference in step 13 (2) (± 100 Hz).
13 (2)	—			—	SET WIDTH	—	—	—	0.2 x 100K	—	R120	—	—	Set VERNIER/SYM ccw. Adjust R120 for frequency referenced in step 13 (1) (+ 100 – 0 Hz).
14 (1)	Carrier Bandwidth	—	—	—	SET AM	—	—	AM	1.0 x 1 MHz	—	NA	Scope	—	Set VERNIER/SYM fully cw. Use the scope AC coupled to set a peak to peak reference level (from 10 vertical divisions) for step 14 (2) and (3).
14 (2)		—	—	—	—		—	—	2.0 x 10 MHz	—	C15	—	[illegible]	Verify [illegible] deviation ([illegible] minor divisions) while moving FREQ START [illegible] between 1 and 2.0.
14 (3)	—	—	—		—	—	—	—	—	—		—	—	

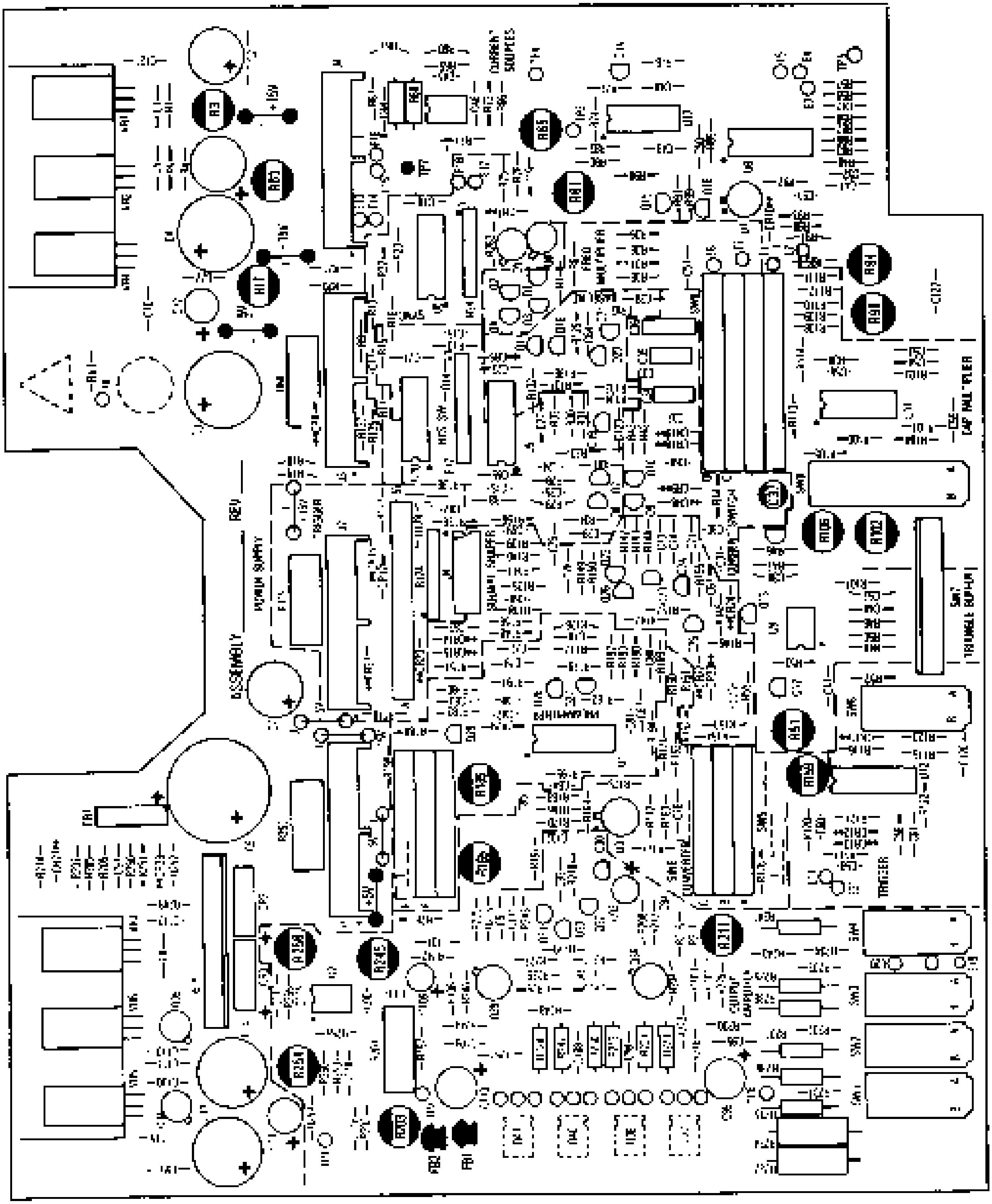


Figure 5-1. Generator Board Calibration Points

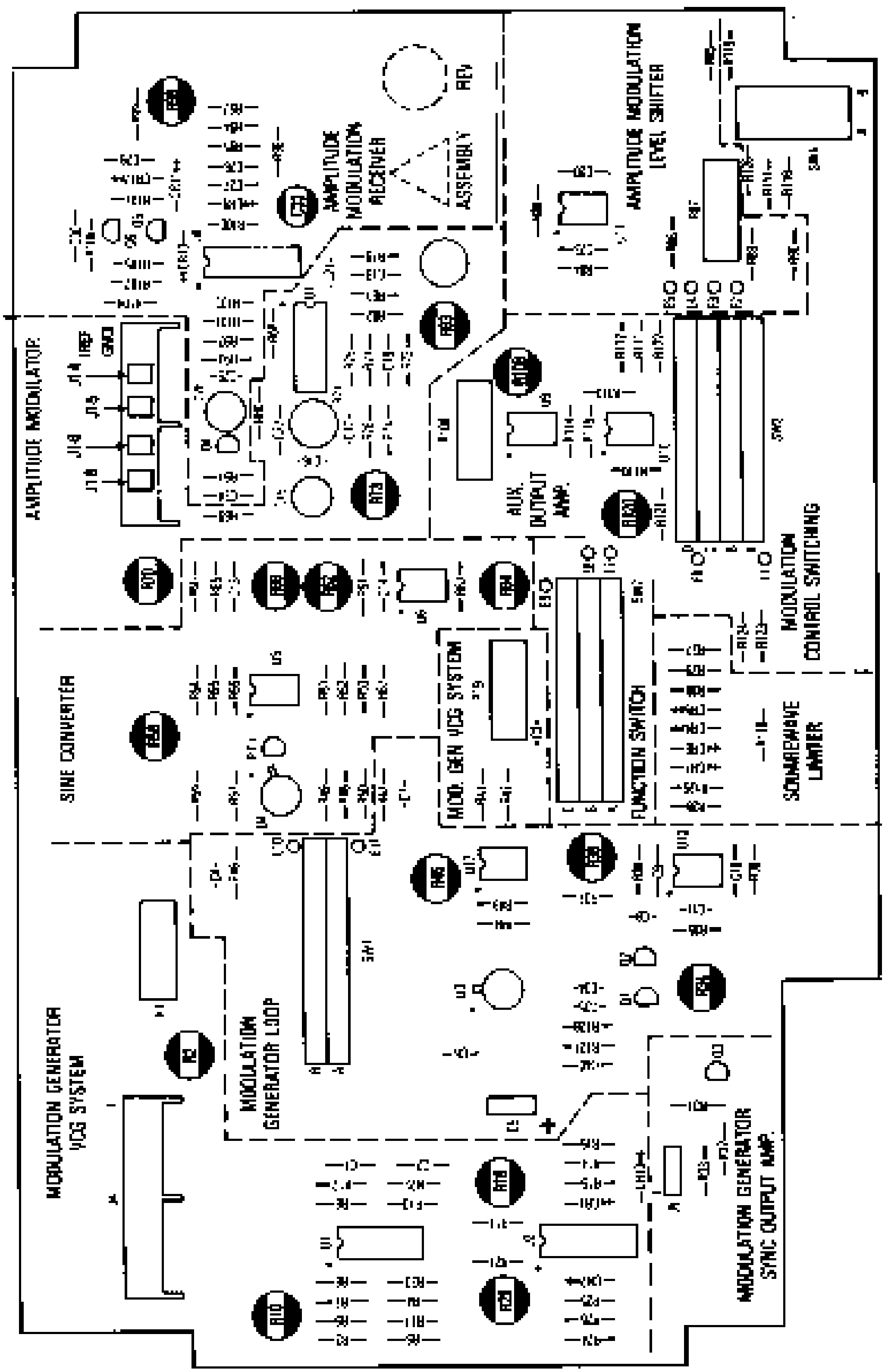


Figure 5-2. Sweep Mod Board Calibration Points

SECTION 6
TROUBLESHOOTING

6.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 BEFORE YOU START

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this guide is to give a methodology which, if applied consistently, will lead to the problem area. Therefore, it is necessary to familiarize yourself with the instrument by reviewing the functional description and the detailed circuit description in conjunction with the schematic. Successful troubleshooting depends upon understanding the circuit operation within each functional block as well as the block relationships.

For sweep/mod board problems, refer to paragraph 6.5. For all other problems, refer to paragraph 6.3.

6.3 GENERATOR BOARD TROUBLESHOOTING

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

Table 6-1 gives an index of common generator board symptoms. For each symptom a troubleshooting guide is referenced (Paragraphs 6.3.1 through 6.3.15) that, when correctly followed, will lead to a solution to the problem.

The troubleshooting guide is arranged in three (3) levels:

1. Identify improperly set controls.
2. Isolate the faulty functional blocks.
3. Identify the faulty circuit or component.

Individual component troubleshooting is given in paragraph 6.7, recommended test equipment is given in paragraph 5.2 and circuit schematics are in the back of this manual.

In all problems:

1. Double check for proper control settings.
2. Calibrate or rule out calibration as a problem.
3. Inspect components, wiring and circuit boards for heat damage.
4. Recalibrate as necessary after circuit repair.

Find the instrument symptom in table 6-1 and proceed as directed to the proper troubleshooting paragraph. See paragraph 6.5 for sweep/mod board related problems.

Table 6-1. Generator Board Related Problems

Symptom	Paragraph
Fuse blows, no dial lamp.	6.3.1
Power supply >100 mVp-p ripple or out of specification.	6.3.2
Function out (all functions) distorted or missing.	6.3.3
Square output distorted or missing.	6.3.4
Sine wave output distorted or missing.	6.3.5
Triangle output distorted or missing.	6.3.6
Sync output distorted or missing (FUNC OUT normal).	6.3.7
Excessive high frequency sine or triangle roll off, excessive square wave overshoot and rise/fall time.	6.3.8
Low frequency square wave tilt.	6.3.9
Time symmetry cannot be adjusted within specification.	6.3.10
Frequency accuracy and FREQ/START FREQ dial response problems.	6.3.11
Trigger, gate and trigger baseline problems.	6.3.12
Voltage at VCG IN connector not changing frequency properly.	6.3.13
DC offset not functioning correctly.	6.3.14
Variable symmetry problems.	6.3.15

6.3.1 Fuse Blows, No Dial Lamp

1. Fuse size incorrect for voltage setting.
2. Line voltage selector incorrectly positioned.

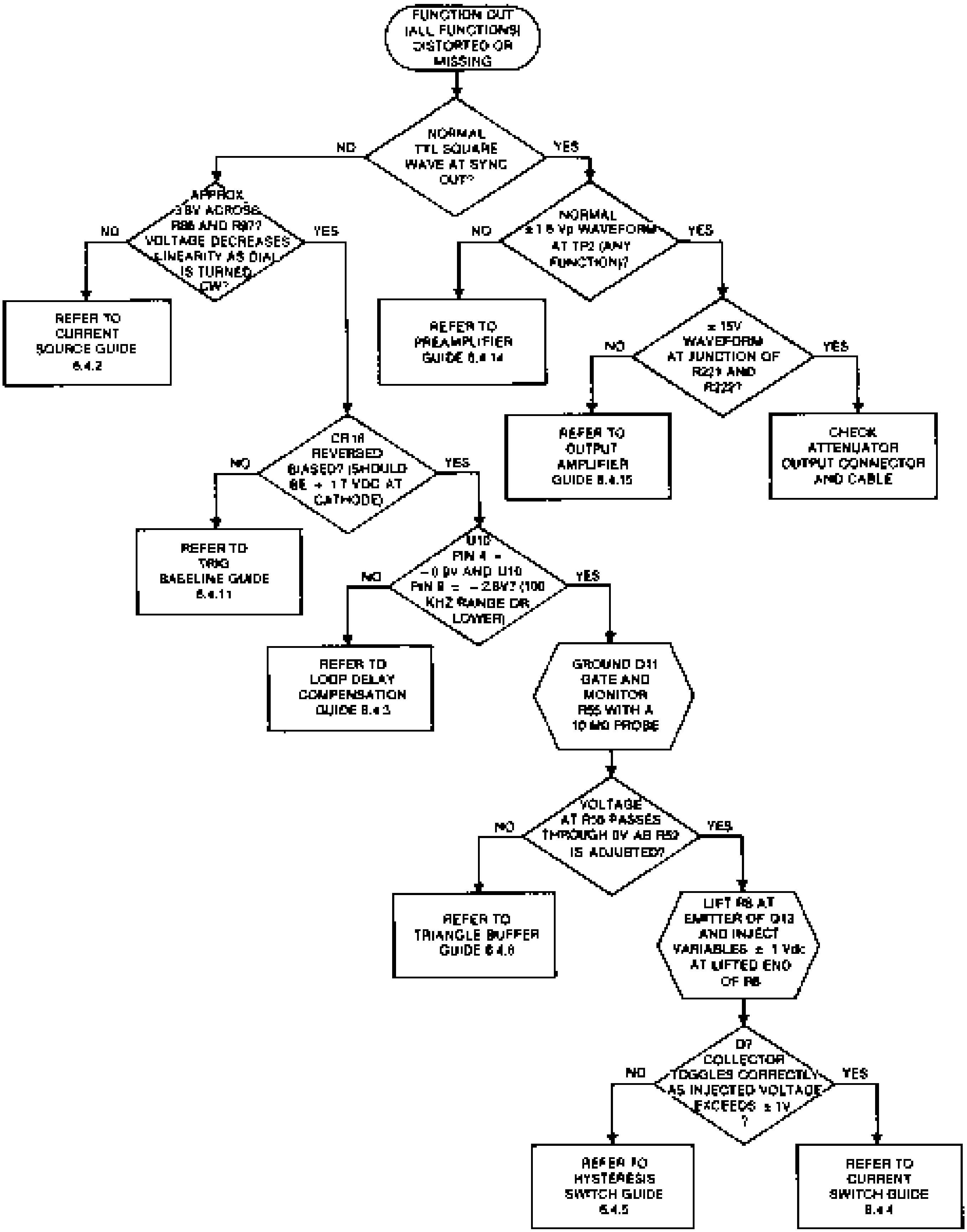


Figure 6-1. Function Output Troubleshooting

3. Disconnect P5. If ac voltages are now correct, refer to the power supply guide, paragraph 6.4.1. If not, inspect the transformer and power receptacle.

6.3.2 Power Supply > 100 mVp-p Ripple or Out of Specification

1. Check line voltage selector for correct position.
2. If the supply is 0V, check for a short between the faulty supply and ground by lifting the jumpers at rear of the board.
3. Lift P5 from the board. If the voltages at P5 are not close to the values shown on the schematic table, inspect the transformer and power receptacle. If the voltages are normal, connect P5, then lift the jumpers (rear of board) for faulty supply. If the supplies are still bad, refer to paragraph 6.4.1. If not, the problem is caused by an excessive current drain by the generator circuits.

6.3.3 All Waveforms at FUNC OUT Distorted or Missing

Improperly set controls:

1. OUTPUT ATTEN or AMPLITUDE controls incorrectly set too low for scope gain or voltmeter range.
2. FUNCTION switch incorrectly set to DC or AM.
3. MODE switch incorrectly set to TRIG or GATE.
4. SYM or DC OFFSET buttons depressed.

Functional block isolation:

1. Verify power supply voltages are within ± 5% of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. Check for a nonlinear triangle. If the triangle is nonlinear on only one range, check for a leaky capacitor on that range. If the triangle is nonlinear in more than one range, check for leaky capacitors or faulty active components in the frequency multiplier and triangle buffer circuits.
3. If the waveform is bad in one of the four lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to the capacitance multiplier guide 6.4.9.
4. If the waveform is bad only in 1M or 10M FREQ MULT positions, refer to paragraph 6.4.3. If the delay compensation circuit appears normal, refer to figure 6-1.
5. If square wave symmetry, measured at FUNC OUT, is out of specification and cannot be calibrated, refer to paragraph 6.3.10.
6. If none of the above conditions apply, refer to figure 6-1.

6.3.4 Square Wave Distorted or Missing

Improperly set controls:

1. SYM button depressed.
2. Excessive dc offset overdriving output amplifier.

Functional block isolation:

1. Verify power supply voltages are within ± 5% of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. If the waveform is bad in one or more of the four lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.
3. If symmetry is not in specification and cannot be calibrated refer to paragraph 6.3.10.
4. If none of the above conditions apply, refer to figure 6-2.

6.3.5 Sine Wave Distorted or Missing

Improperly set controls:

1. SYM button depressed.
2. Excessive dc offset overdriving output amplifier.

Functional block isolation:

1. Verify power supply voltages are within ± 5% of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. Check the triangle for nonlinearity at FUNC OUT. If it is nonlinear but only on one range, check for a leaky capacitor on that range. If the triangle is nonlinear on more than one range, check for a leaky capacitor or faulty active component in the frequency multiplier and triangle buffer circuits. (NOTE: Some nonlinearity above 200 kHz is normal and not specified.)
3. If the waveform is bad in one or more of the four lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.
4. Verify that square wave symmetry, at FUNC OUT is in specification. If not and cannot be calibrated refer to paragraph 6.3.10.
5. If none of the above conditions apply, refer to figure 6-3.

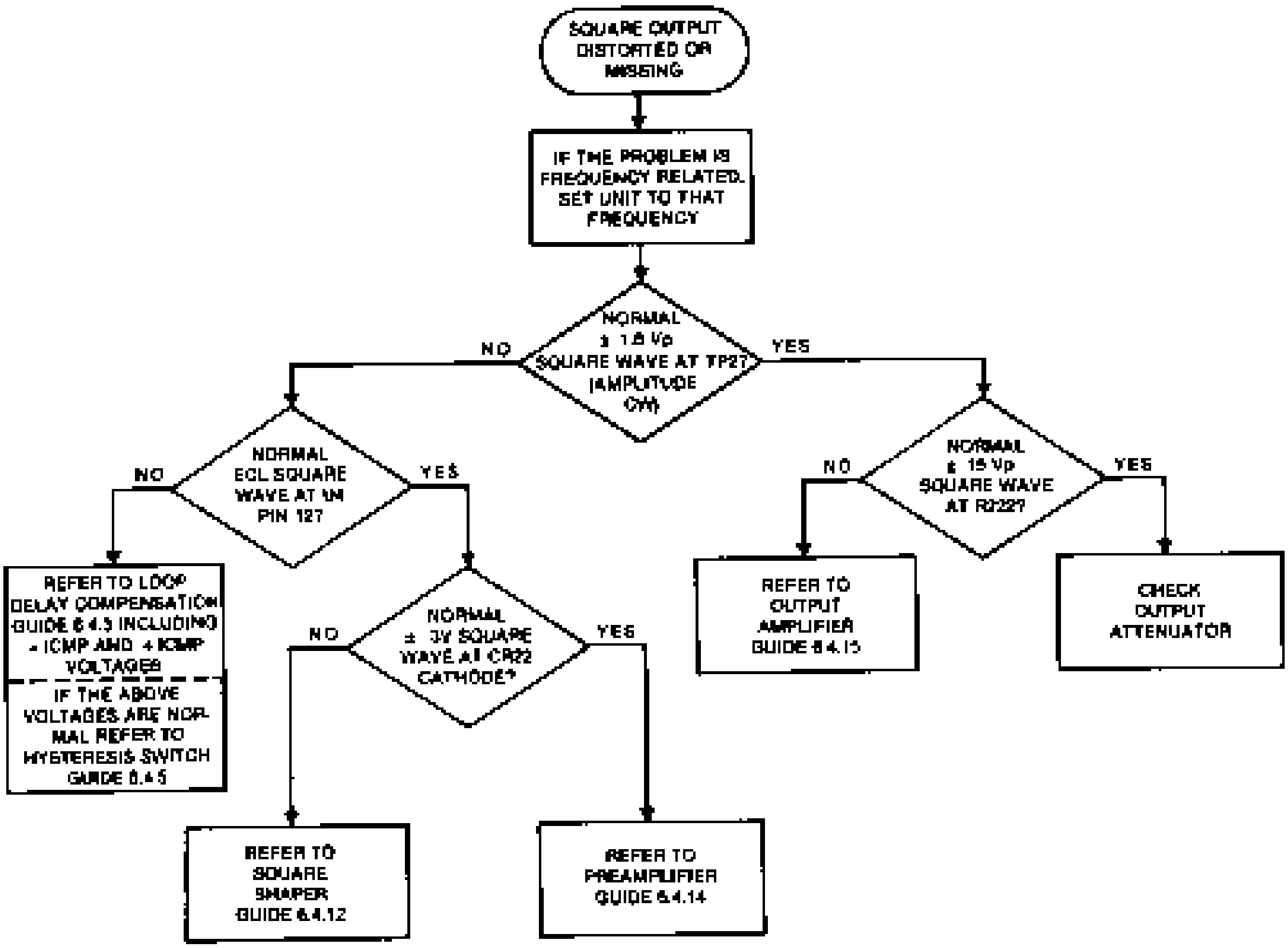


Figure 6-2. Square Output Troubleshooting

6.3.6 Triangle Distorted or Missing

Improperly set controls:

1. SYM button depressed
2. Excessive dc offset overdriving output amplifier

Functional block isolation

1. Verify power supply voltages are within ±5% of nominal with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. Check the triangle for nonlinearity at FUNC OUT. If it is nonlinear, but only on one range, check for a leaky capacitor on that range. If the triangle is nonlinear on more than one range, check for a leaky capacitor or faulty active component in the frequency multiplier and triangle buffer circuits. (NOTE: Some nonlinearity above 200 kHz is normal and not specified.)
3. If the waveform is bad in one or more of the four lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.
4. Verify square wave symmetry at FUNC OUT is in specification. If not and cannot be calibrated, refer to paragraph 6.3.10.
5. If none of the above conditions apply, refer to figure 6-4.

6.3.7 Sync Output Distorted or missing (FUNC OUT Normal)

Improperly set controls.

1. Because the FUNC OUT is normal, this cannot be caused by improperly set controls.

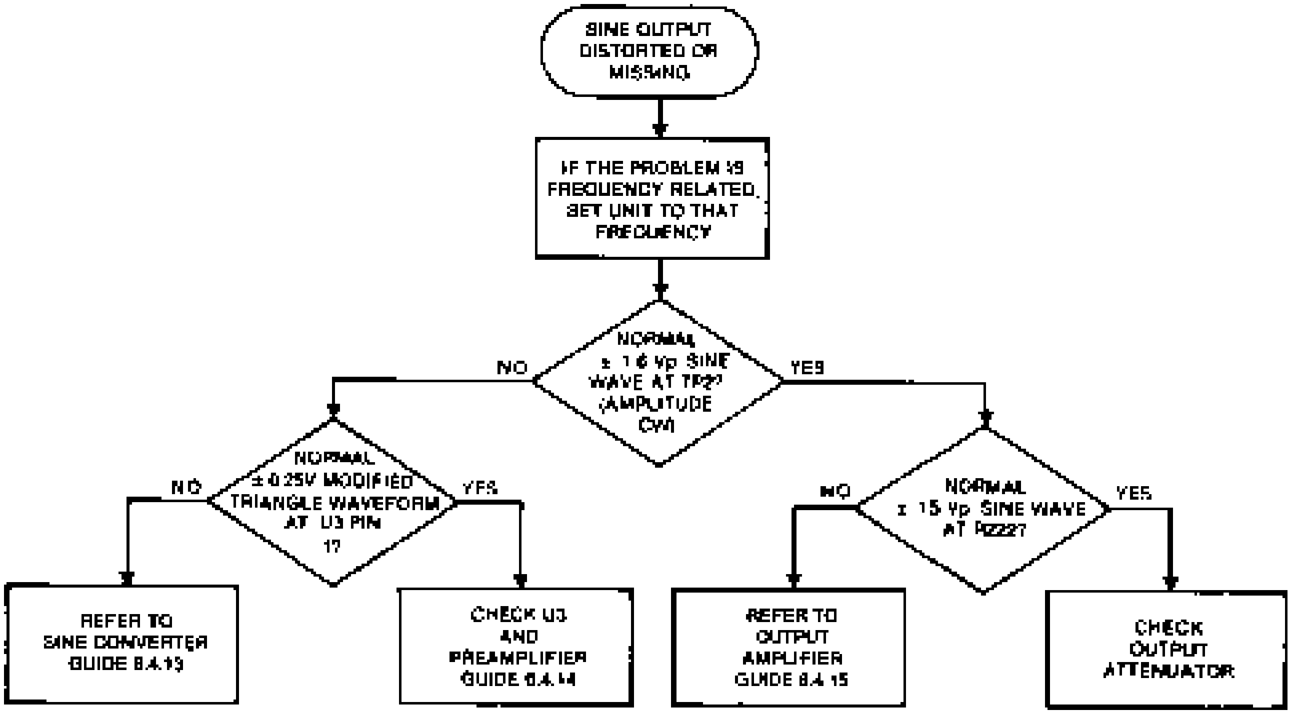


Figure 6-3. Sine Output Troubleshooting

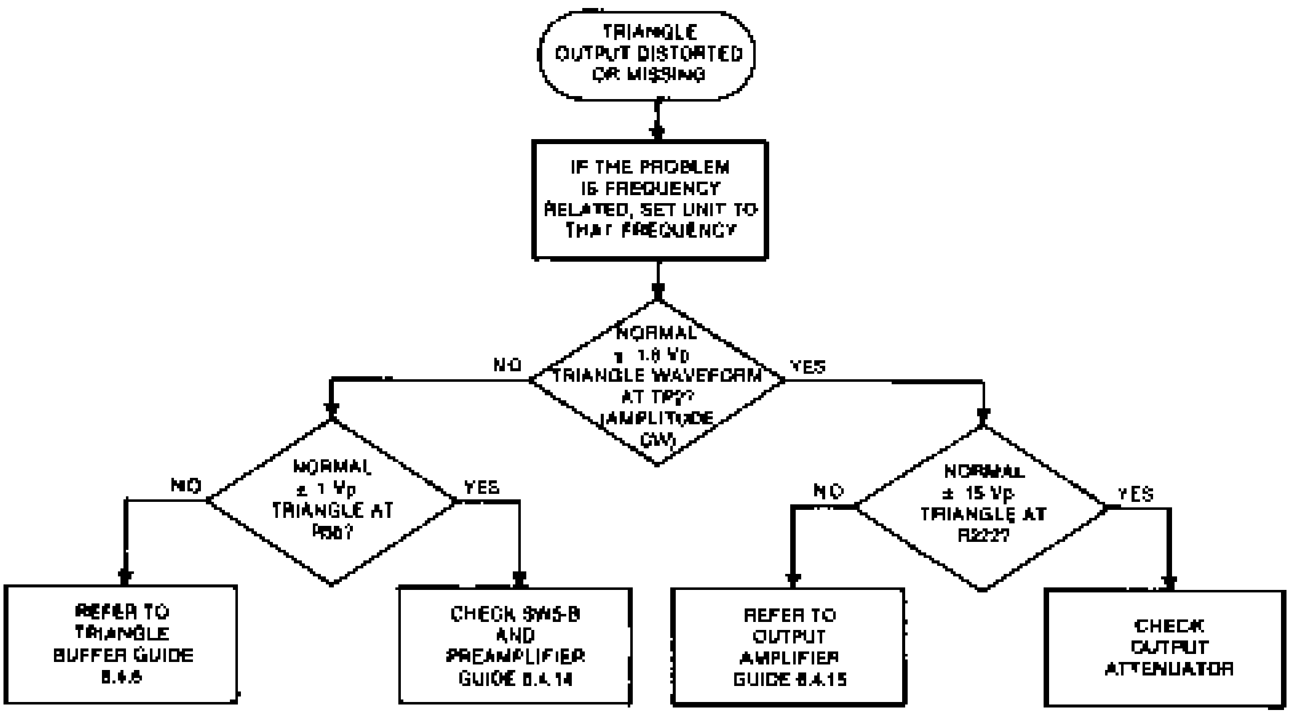


Figure 6-4. Triangle Output Troubleshooting

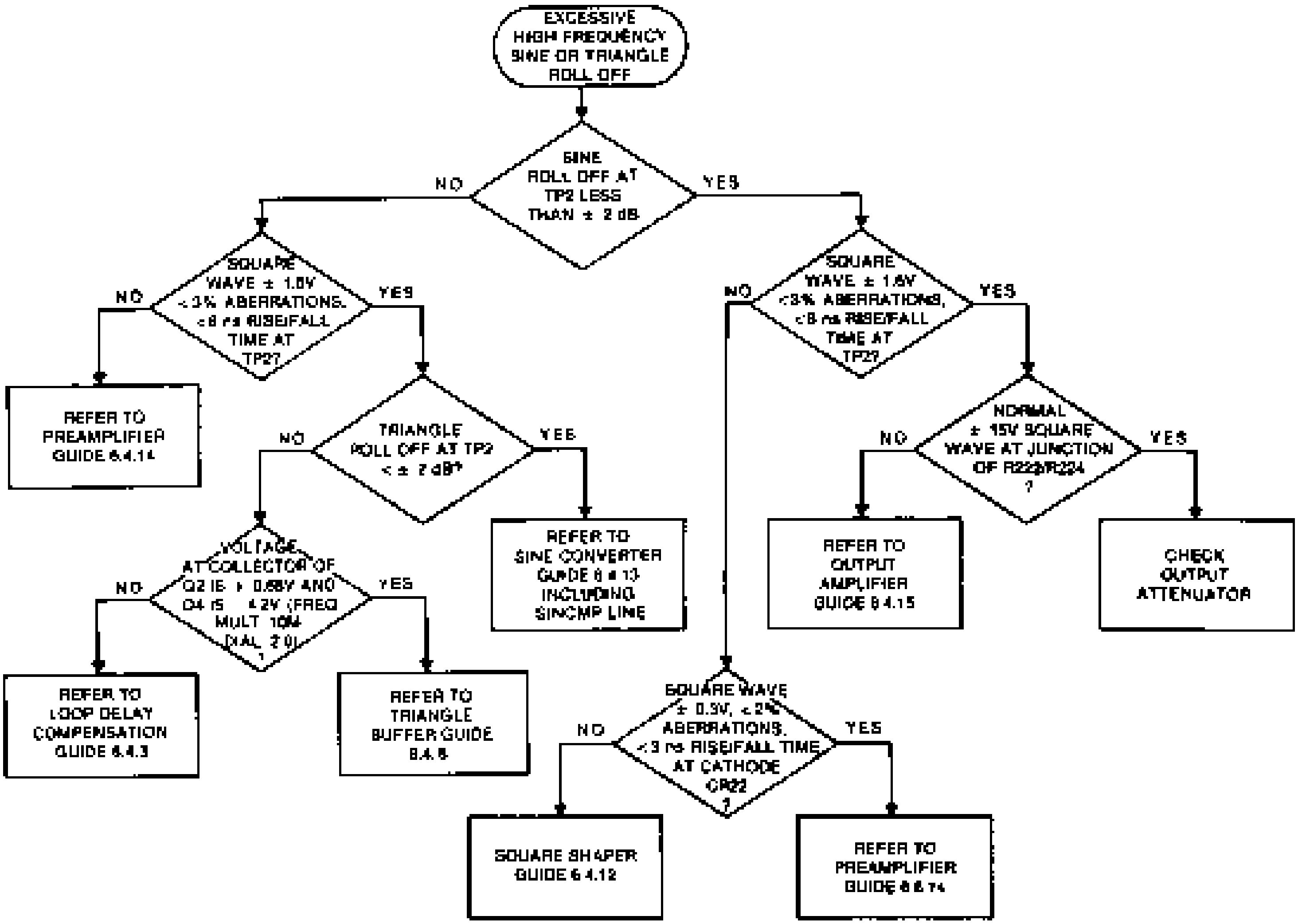


Figure 6-5. High Frequency Waveform Troubleshooting

Functional block isolation:

1. If there is no ECL square wave at U6 pin 10, refer to paragraph 6.4.7. If there is an ECL square wave, refer to paragraph 6.4.8.

6.3.8 Excessive High Frequency Sine or Triangle Roll Off

Improperly set controls:

1. Excessive dc offset overdriving output amplifier.
2. Verify 50Ω load on the cable at oscilloscope end.

Functional block isolation:

1. Verify power supply voltages are within ± 5% of nominal with less than 100 mVp-p of ac ripple. If not refer to paragraph 6.4.1.
2. If none of the above conditions apply, refer to figure 6-5. Use a X10 probe with a very short ground lead and a spectrum analyzer, RF voltmeter or a 200 MHz bandwidth scope when performing sine or triangle roll-off tests.

6.3.9 Low Frequency Square Wave Tilt

Improperly set controls:

1. Scope improperly set to ac.

Functional block isolation:

1. Verify power supply voltages are within ± 5% of nominal, and less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. If none of the above conditions apply, refer to figure 6-6.

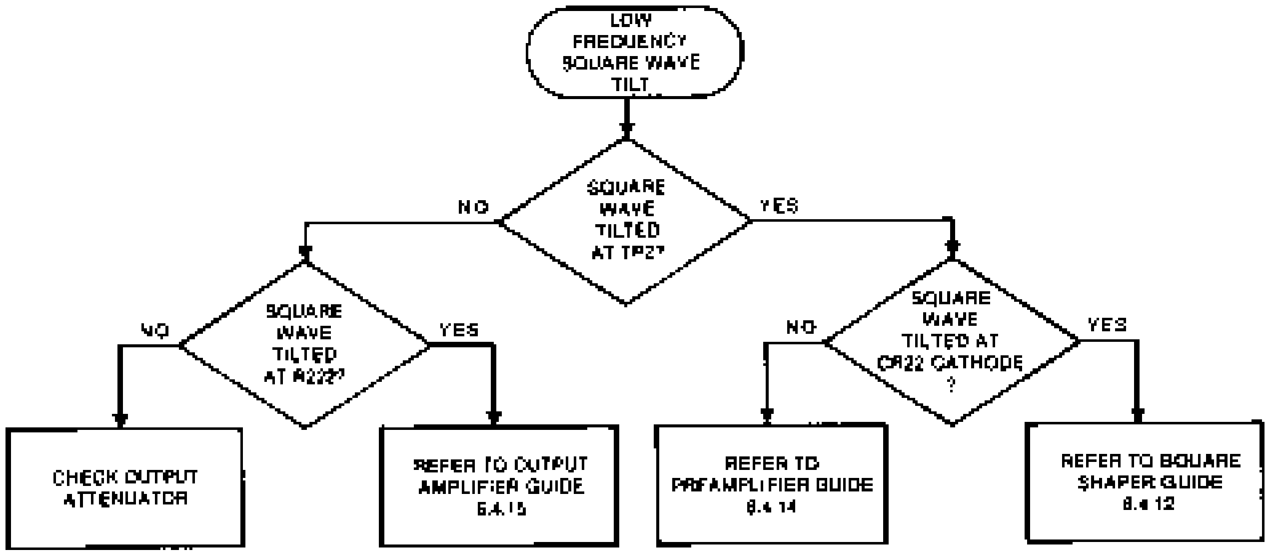


Figure 6-6. Low Frequency Square Wave Troubleshooting

6.3.10 Time Symmetry Cannot Be Adjusted To Within Specifications

Improperly set controls

1. SYM button depressed

Functional block isolation:

1. Verify power supply voltages are within ±5% of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. If symmetry is out of specification in one of the four lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.
3. If symmetry is out of specification on FREQ MULT settings 1M or 10M only, refer to paragraph 6.4.3.
4. If the voltages across R86 and R97 are not equal (typically 3.8V, Freq Dial 2.0 Freq Mult 100K or less), refer to paragraph 6.4.2.

6.3.11 Frequency Accuracy and FREQ/START FREQ Dial Response Problems

Improperly set controls

1. SYM button depressed
2. External signal connected to VCG in BNC
3. VERNIER not in FREQ CAL position.

Functional block isolation:

1. Verify power supply voltages are within ±5% of nominal with less than 100 mVp-p ac ripple. If not, refer to paragraph 6.4.1.
2. If the problem occurs in one of the four lowest frequency ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.
3. If the frequency accuracy is out of specification on FREQ MULT settings 1M and 10M, refer to paragraph 6.4.3.
4. If the frequency is out of specification, but only on one range, check the range capacitor for that range.
5. If the problem occurs on the 1K, 10K, or 100K range, check the range capacitor.
6. On the 1K range and frequency dial set at 2.0, check for 3.8V across R86 and R97. As the FREQ/START FREQ dial is rotated, this voltage should linearly track the dial settings within +3% of full scale. If not, refer to paragraph 6.4.2.
7. If none of the above conditions apply, refer to figure 6-7.

6.3.12 Trigger, Gating and Trigger Baseline Problems

Improperly set controls:

1. MODE incorrectly set to CONT.
2. FUNCTION incorrectly set to DC.
3. DC OFFSET overdriving output amplifier.

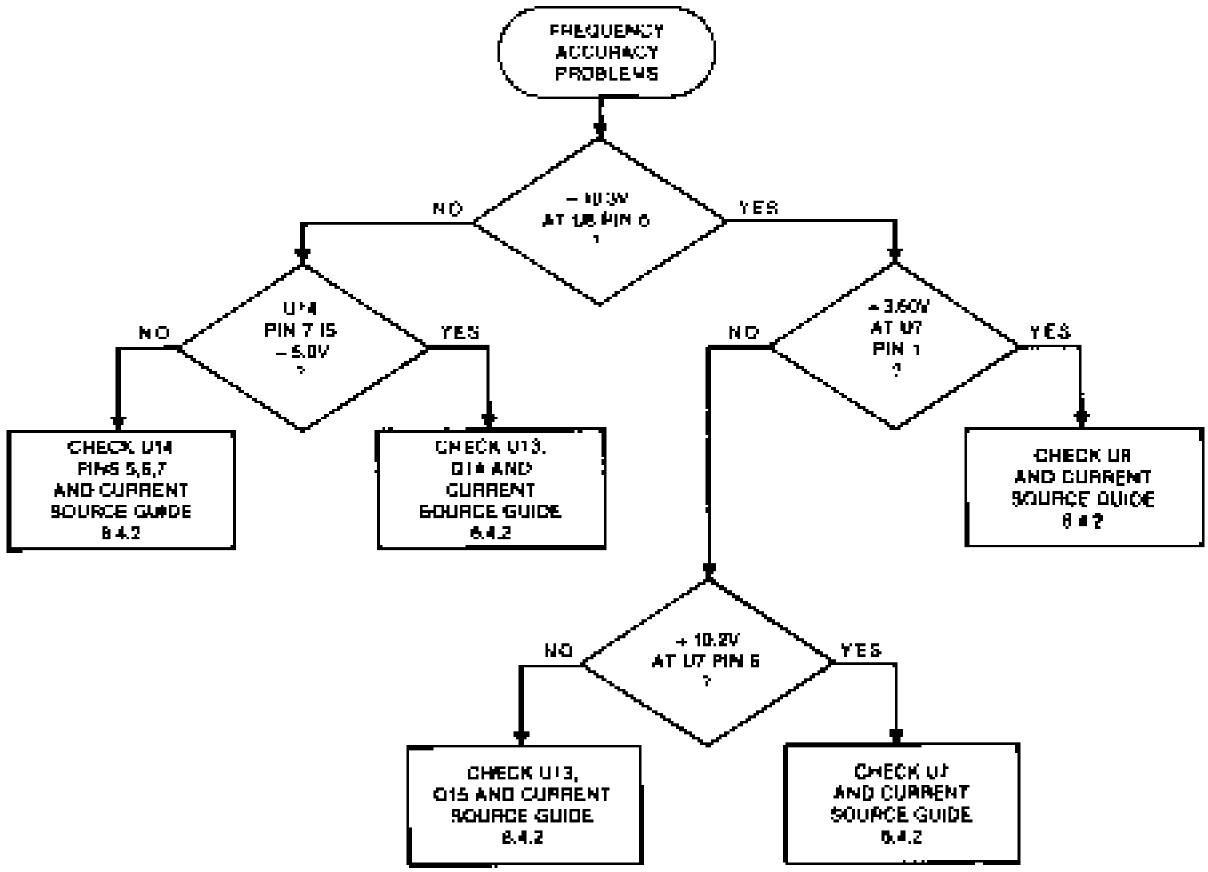


Figure 6-7. Frequency Accuracy Troubleshooting

Functional block isolation:

1. Verify power supply voltages are within ±5% of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. If the trigger baseline cannot be calibrated within specification, set MODE to GATE and monitor the emitter of Q19. With TRIG IN disconnected, rotate the TRIG LEVEL ccw. The voltage should go about − 0.7 Vdc. Rotating the TRIG LEVEL cw should change this voltage to about + 1.8 Vdc. If these voltage readings are normal, check CR10 and CR19.
3. If none of the above conditions apply, refer to figure 6-8.
4. For high frequency (1M and 10M ranges) trigger or gate problems, set the controls as follows:

FREQ/START FREQ	2.0
FREQ MULT:	10M
SYM:	OFF
MODE:	TRIG or GATE (Depends on symptom-GATE preferred)
TRIG LEVEL:	12 o'clock

Set the scope as follows:

Horizontal:	20 ns/div
Vertical:	1 V/div

Inject a 15 MHz 1 Vp-p trigger signal and refer to figure 6-9.

6.3.13 Voltage At VCG IN Connector Not Changing Frequency Properly

Improperly set controls:

1. Excessive VCG IN voltage for dial setting (maximum input voltage is + 5.0 Vdc with FREQ/START FREQ set at .02 and the Freq VERNIER turned ccw)
2. MODE (AUX GEN) incorrectly set to FM

Functional block isolation:

1. Set FREQ/START FREQ to 2.0, FREQ MULT to 1K, and VCG IN with no input. Measure voltage across R86 and R97 (− 3.8 Vdc). In addition, as the frequency dial is rotated, the voltage linearly

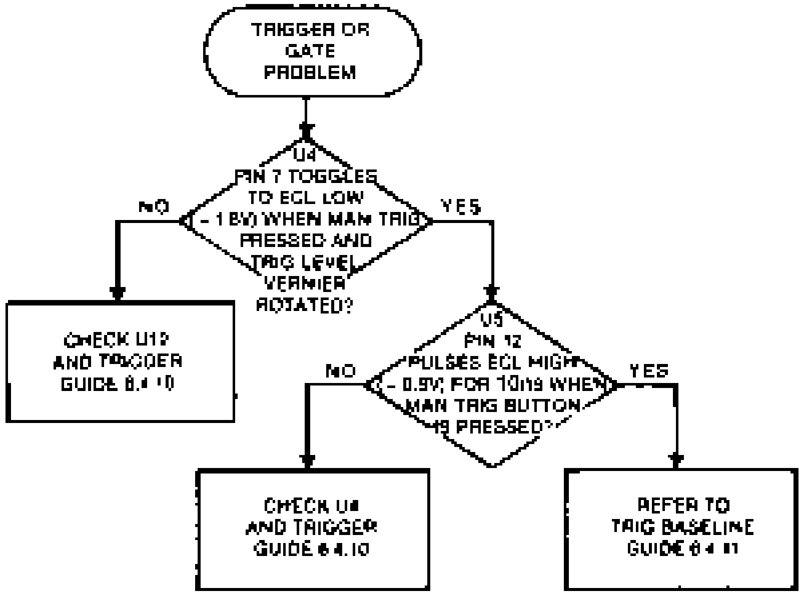


Figure 6-8. Trigger Gate Troubleshooting

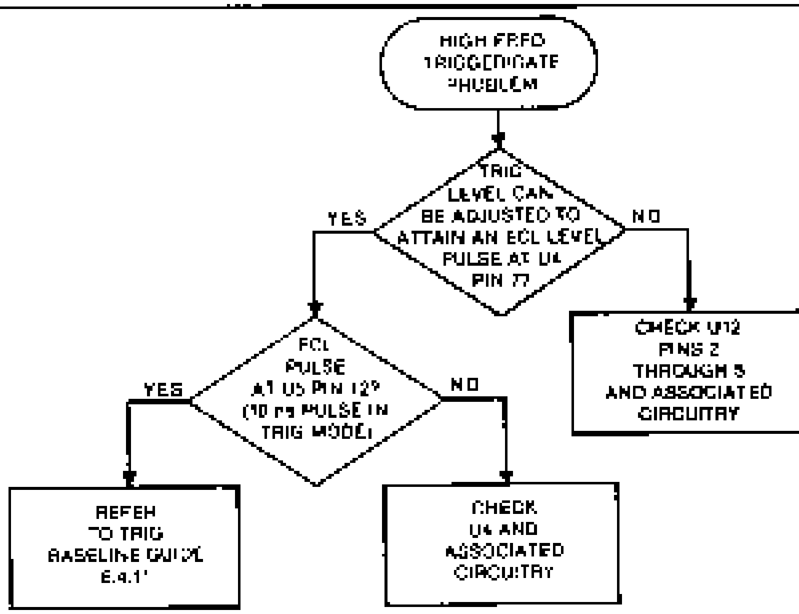


Figure 6-9. High Frequency Trigger/Gate Troubleshooting

tracks FREQ/START FREQ settings within ±3% full scale. If it functions properly, check R67, R68, R69 and associated circuitry, but if not, refer to paragraph 6.3.11.

6.3.14 DC Offset Not Functioning Correctly

Improperly set controls:

1. Signal peak plus offset exceeding + or − 7.5V (with a 50Ω load), or ± 15V open circuit.
2. Check OUTPUT ATTEN since this also attenuates output offset.

Functional block isolation.

1. Verify power supply voltages are within ±5% of nominal with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. Take the following voltage measurements with the DC OFFSET button depressed and the DC OFFSET control rotated cw:
   a) The junction of R260 and C116 should vary from +8.0V to −8.0V.
   b) U2 pin 2 should hold at 0.0V.

c) U2 pin 6 should vary from −1.0V to +1.0V. (Drifting of this voltage is typical because of constant compensation by U2 of variations in output transistor currents.)

3. If none of the above conditions apply, refer to paragraph 6.4.15.

6.3.15 Variable Symmetry Problems

Improperly set controls:

1. SYM button is incorrectly extended.
2. Note: When SYM is depressed the output frequency should be one-tenth the selected frequency.
3. DC offset is overdriving the output amplifier.

Functional block isolation:

1. Verify power supply voltages within ±5% of nominal with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. When the voltage at the right leg of R88 (VERNIER/SYM CW) is −15V and when the voltage at the left leg of R88 (VERNIER/SYM) is −15V, refer to paragraph 6.4.2. If not, check R88 and SW8.

6.4 CIRCUIT GUIDES

Circuit guides provide listings of voltage levels, waveforms, and hints that, when used with the schematics, are helpful in isolating faulty circuits. Table 6-2 is an index of circuit guides.

Table 6-2. Circuit Guide Index

Circuit Guide	Paragraph
Power Supply	6.4.1
Current Source	6.4.2
Loop Delay Compensation	6.4.3
Current Switch	6.4.4
Hysteresis Switch	6.4.5
Triangle Buffer	6.4.6
Zero Crossing Detector	6.4.7
Sync	6.4.8
Capacitance Multiplier	6.4.9
Trigger	6.4.10
Trig Baseline	6.4.11
Square Shaper	6.4.12
Sine Converter	6.4.13
Preamplifier	6.4.14
Output Amplifier	6.4.15

6.4.1 Power Supply Guide

1. To determine a faulty power supply, check for the voltages given in table 6-3.
2. If the regulator input is bad, remove P5 and check for:
   a. Shorted or open diodes (CR1, CR2, or CR3).
   b. Shorted or open capacitors at the input of the regulator.
   c. Short between the regulator metal mounting tab and chassis ground.
3. If the regulator input is good, check for:
   a. Shorted or open capacitors at the output of the regulator.
   b. Short between regulator metal mounting tab and chassis ground.
   c. Excessive loading by main board circuits. To verify, lift jumper of the appropriate supply.
   d. If all of the above conditions appear normal, replace the voltage regulator.

Table 6-3. Power Supply Checks

Supply	Voltage Tolerance	Maximum Regulator Input Ripple (p-p)	Maximum Regulator Output Ripple (p-p)
±15V Balance	30 ± 1.5 Vdc (a)	—	—
+15V	(b)	1.5 Vac	10 mV
−15V	(c)	1.5 Vac	10 mV
+5V	±750 mV	1.5 Vac	10 mV
−5V	±750 mV	1.5 Vac	10 mV
+23V	±1.15 Vdc	1.5 Vac	10 mV
−23V	±1.15 Vdc	1.5 Vac	10 mV

(a) Measured between +15V and −15V supplies.
(b) Measure and note +15V supply (V_{+15}).
(c) −15V supply = $-V_{+15} \pm .01V$.

6.4.2 Current Source Guide

Top of Dial Check: Set the controls as follows; then perform the checks in table 6-4.

Control	Setting
FREQ/START FREQ	2.0
FREQ MULT	1K
VERNIER	FREQ CAL
SYM	Off (extended)

VCG IN	Disconnected
MODE (AUX GEN)	AUX OUT ONLY

VCG Check: Set the controls as follows; then perform the checks in table 6-5.

Control	Setting
FREQ START FREQ	0.2
FREQ MULT	1K
VERNIER	Full ccw
SYM	Off (extended)
VCG IN	+ 5.0 Vdc input
MODE (AUX GEN)	AUX OUT ONLY

Table 6-4. Current Source Check (Top of Dial)

Test Point	Desired Results
U14 pin 7	−5 ± .5 Vdc
U13 pins 1, 2	−5 ± .5 Vdc
Measure across R83	+3.8 ± .38 Vdc
U8 pin 6	−10.3 ± 1.03 Vdc
Measure across R84 and R93	+3.8 ± .38 Vdc
U13 pin 6	0 ± .01 Vdc
U7 pin 6	+10.2 ± 1.02 Vdc
Measure across R86 and R97	+3.8 ± .38 Vdc

Table 6-5. Current Source (VCG IN)

Test Point	Desired Results
U7 pin 6	+14.38 ± 1.44 Vdc
U8 pin 6 (disconnect VCG IN)	−14.3 ± 1.43 Vdc

10 MHz Range Check: Set the controls as shown below, then perform the checks in table 6-6.

Control	Setting
FREQ/START STOP	2.0
FREQ MULT	10M
VERNIER	FREQ CAL
SYM	Off (extended)
VCG IN	Disconnected
MODE (AUX GEN)	AUX GEN ONLY

Table 6-6. Current Source Check (10 MHz Range)

Test Point	Desired Results
Measure across R99	+5.9 ± .59 Vdc
Measure across R83	+6.05 ± .61 Vdc
U8 pin 6	−6.2 ± .62 Vdc

Variable Symmetry Check: Set the controls as shown then measure the voltage across resistors R84, R85, R86, R87, R93, and R97. The measured voltages should read +0.38 ± .04V.

Control	Settings
FREQ/START STOP	2.0
VERNIER	12 o'clock position
VCG IN	Disconnected
FREQ MULT	1K
SYM	On (depressed)

6.4.3 Loop Delay Compensation Guide

Set the controls as shown, then perform the checks in table 6-7.

Controls	Settings
FREQ/START FREQ	2.0
VERNIER	FREQ CAL
VCG IN	Disconnected
FREQ MULT	10M
SYM	Off (extended)

Table 6-7. Loop Delay Compensation Checks

Test Point	Desired Results
Q1 and Q2 emitters	+ 9.2 ± .92 Vdc
Q1 base and collector, Q2 base	+8.5 ± .9 Vdc
Q2 collector	+0.68 ± .07 Vdc
Q3 and Q4 emitter	− 9.05 ± .91 Vdc
Q3 and Q4 bases, Q3 collector	− 8.32 ± .83 Vdc
Q4 collector	− 4.2 ± .42 Vdc
U10 pin 4	− 1.6 ± .16 Vdc (+ Peak reference)
U10 pin 9	− 2.17 ± .22 Vdc (− Peak reference)

6.4.4 Current Switch Guide

Set the controls as shown, then take waveform measurements. Refer to figure 6-10.

Controls	Settings
FREQ/START FREQ	2.0
FREQ MULT	1K
SYM	Off (extended)
MODE	CONT

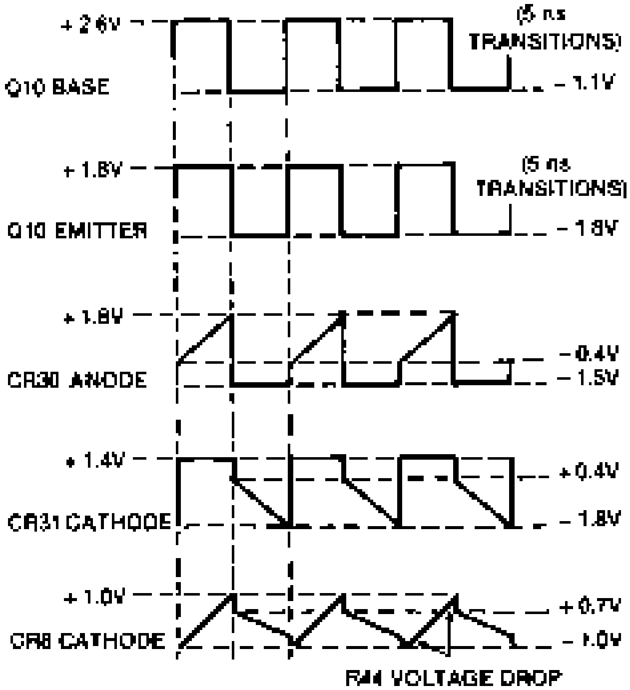


Figure 6-10. Current Switch Waveforms

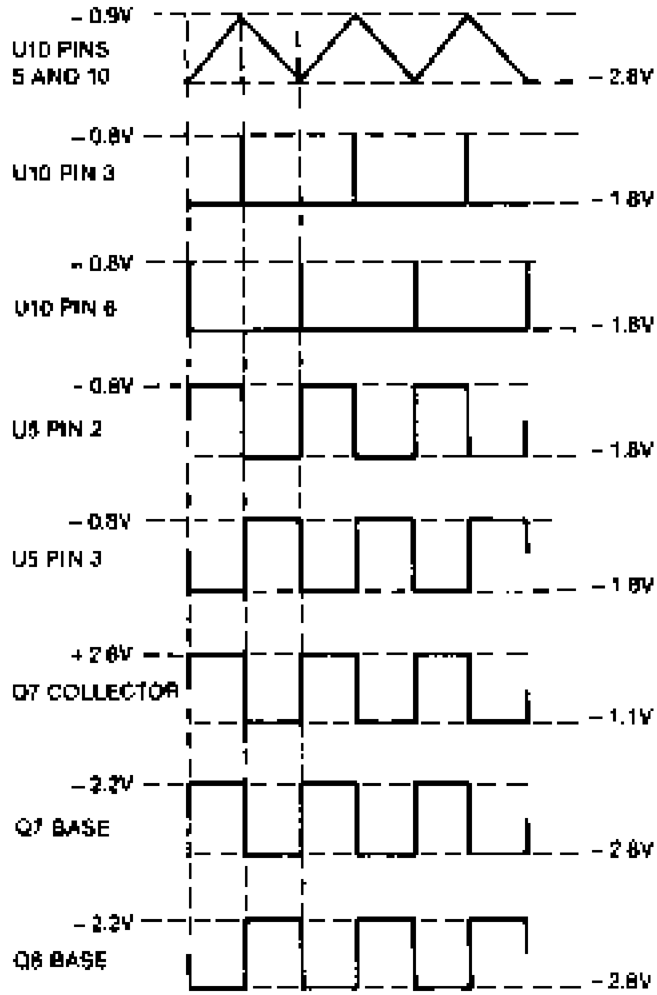


Figure 6-11. Hysteresis Switch Waveforms

6.4.5 Hysteresis Switch Guide

Set the controls as shown; then perform the checks in table 6-8, and take waveform measurements. Refer to figure 6-11.

Controls	Settings
FREQ/START FREQ	2.0
FREQ MULT	1K
SYM	Off
MODE	CONT

Table 6-8. Hysteresis Switch Guide

Test Point	Desired Results
U10 pin 4	0.9 ± .09 Vdc (+ Peak reference)
U10 pin 9	−2.8 ± .28 Vdc (− Peak reference)
Q7 and Q8 emitters	−3.0 ± .3 Vdc

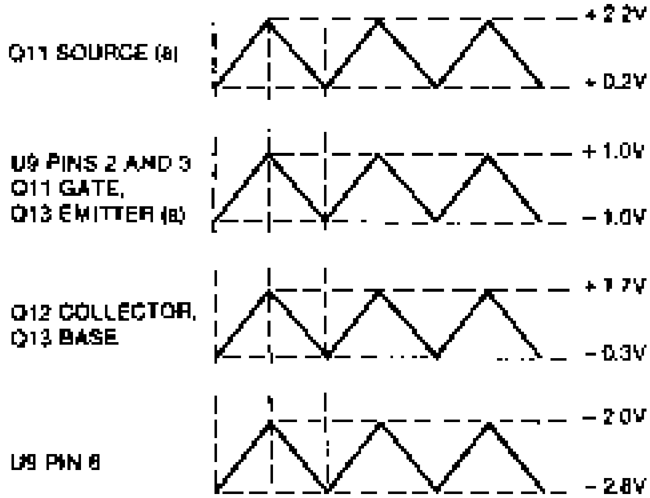
6.4.6 Triangle Buffer Guide

Set the controls as shown; then perform the checks in table 6-9 and take waveform measurements. Refer to figure 6-12. If, after setting the controls, the generator loop does not run, lift R45 at E23 and inject a ± 1.0V triangle into R45.

Controls	Settings
FREQ/START FREQ	2.0
FREQ MULT	1K
SYM	Off
MODE	CONT

Table 6-9. Triangle Buffer Checks

Test Point	Desired Results
Q11 drain	+6.5 ± .65 Vdc
Q12 emitter	0.3 ± .03 Vp-p triangle, offset −10 ± 1 Vdc
Q12 base	0.3 ± .03 Vp-p triangle, offset −9.3 ± .9 Vdc
Q13 collector	+5.0 ± .5 Vdc



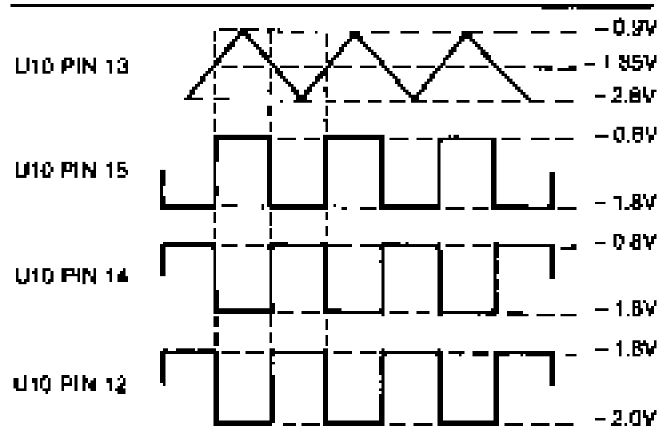
(a) Requires a X10 Probe (high impedance)

Figure 6-12. Triangle Buffer Waveforms

6.4.7 Zero Crossing Detector Guide

Set the controls as shown; then take waveform measurements. Refer to figure 6-13.

Controls	Settings
FREQ/START FREQ	2.0
FREQ MULT	1K
SYM	Off
MODE	CONT



(In TRIG mode, no input, voltage is −1.2 Vdc.)

Figure 6-13. Zero Crossing Detector Waveforms

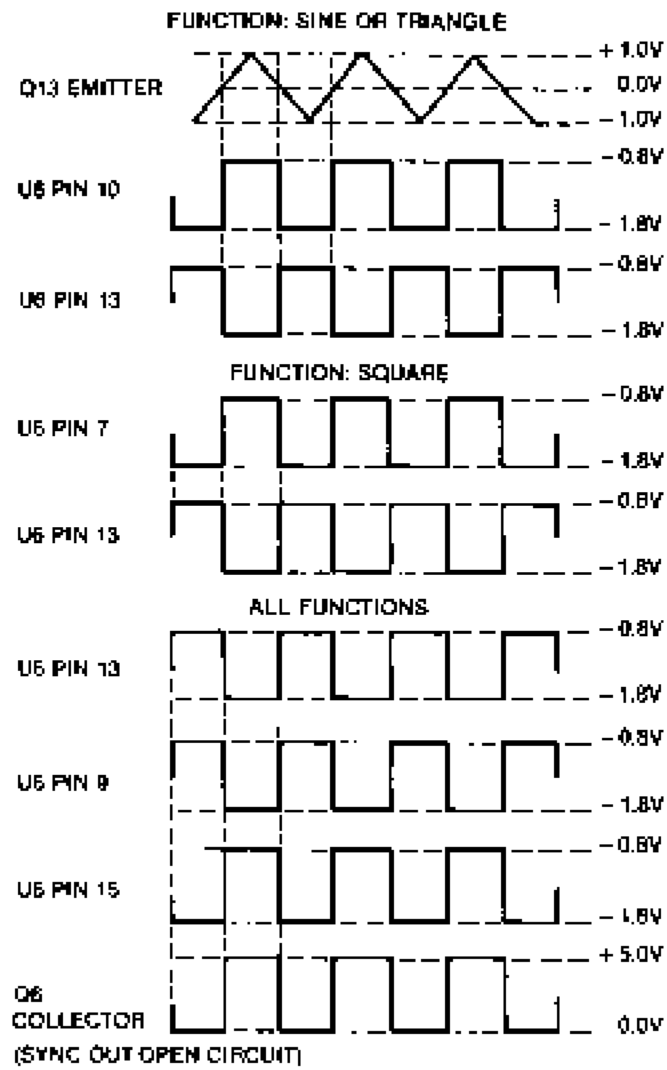


Figure 6-14. Sync Waveforms

6.4.8 Sync Guide

Set the controls as shown then perform the checks in table 6-10 and take waveform measurements see figure 6-14.

Controls	Settings
FREQ/START FREQ	2.0
FREQ MULT	1K
SYM	Off
MODE	CONT

Table 6-10. Sync Check

Test Point	Desired Results: Function: Sine or Triangle Wave	Desired Results: Function: Square Wave
CR4 cathode	+1.2 ± .12 Vdc	− 5 ± 5 Vdc
U5 pins 4 and 6	1 ± .1 Vdc	−4.3 ± .43 Vdc
U5 pins 2 and 11	1.8 ± .16 Vdc	−3.8 ± .08 Vdc
Q5/Q6 emitters	−1.6 ± .16 Vdc	−1.6 ± .16 Vdc

6.4.9 Capacitance Multiplier Guide

Set the controls as shown, then take the waveform measurements. Refer to figure 6-15.

Controls	Settings
FREQ/START FREQ	2.0
FREQ MULT	100
SYM	Off
MODE	CONT

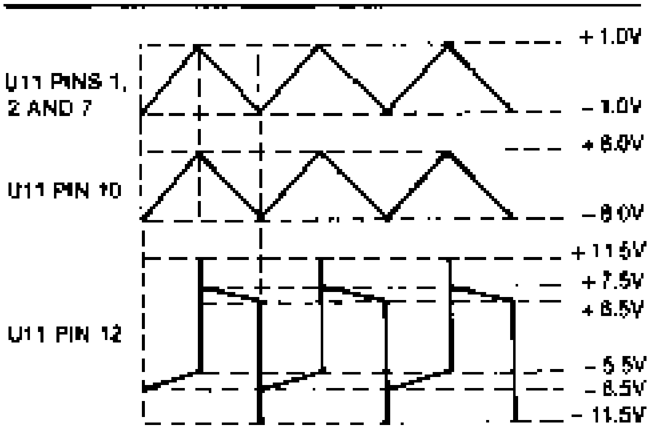


Figure 6-15. Capacitance Multiplier Waveforms

6.4.10 Trigger Guide

TRIG or CONT Check: Set the controls as shown; then take the waveform measurements. Refer to figure 6-16

Controls	Settings
FREQ/START FREQ	2.0
FREQ MULT	1K
MODE	TRIG or CONT
TRIG IN	± 1V 1 kHz Square wave

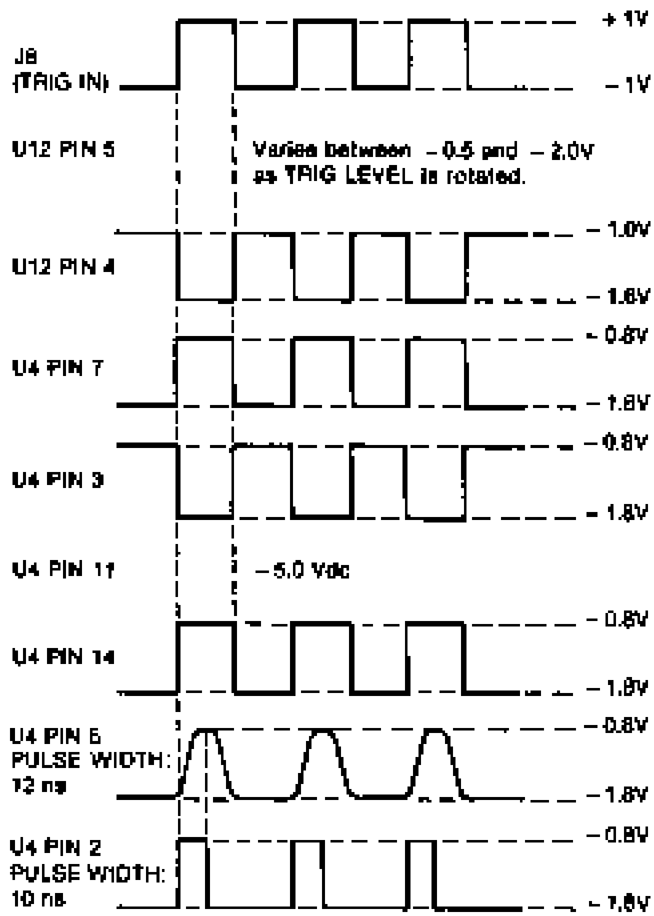


Figure 6-16. Trigger Waveforms (TRIG or CONT)

GATE Checks: Set the controls as shown; then take the waveform measurements. Refer to figure 6-17.

Controls	Settings
FREQ/START FREQ	2.0
FREQ MULT	1K
MODE	GATE
TRIG IN	± 1V 1 kHz Square wave

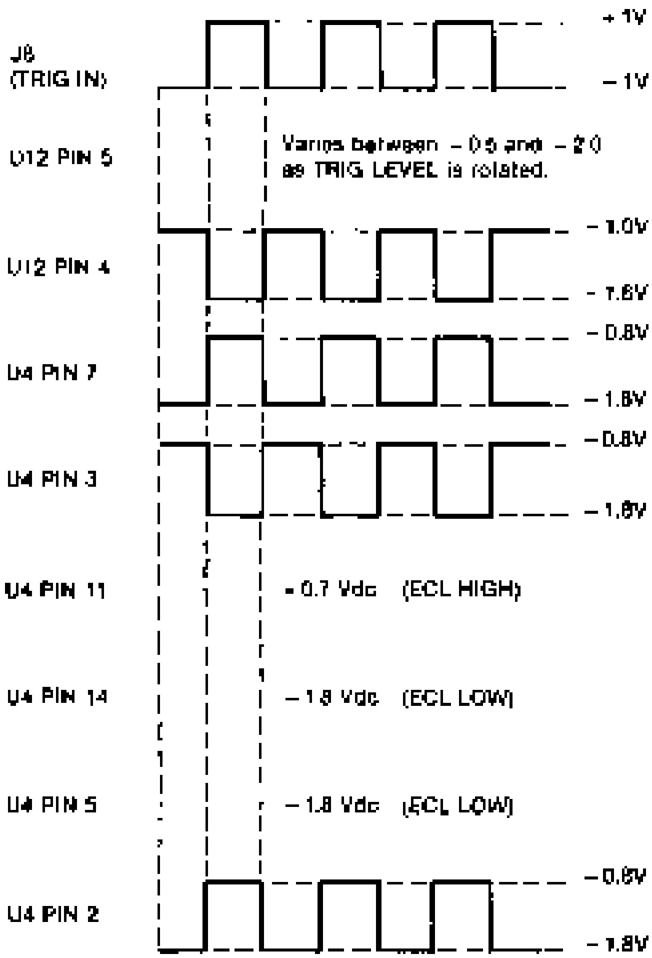


Figure 6-17. Trigger Waveforms (Gate)

6.4.11 Trigger Baseline Guide

Trigger or Gate Mode Problems: Set the controls as shown; then take the waveform measurements. Refer to figure 6-18.

Controls	Settings
FREQ/START FREQ	2.0
FREQ MULT	10K
SYM	Off
MODE	TRIG or GATE (Depends on symptom—GATE preferred
TRIG LEVEL	Approximately centered
TRIG IN	± 1V 10 kHz Square wave

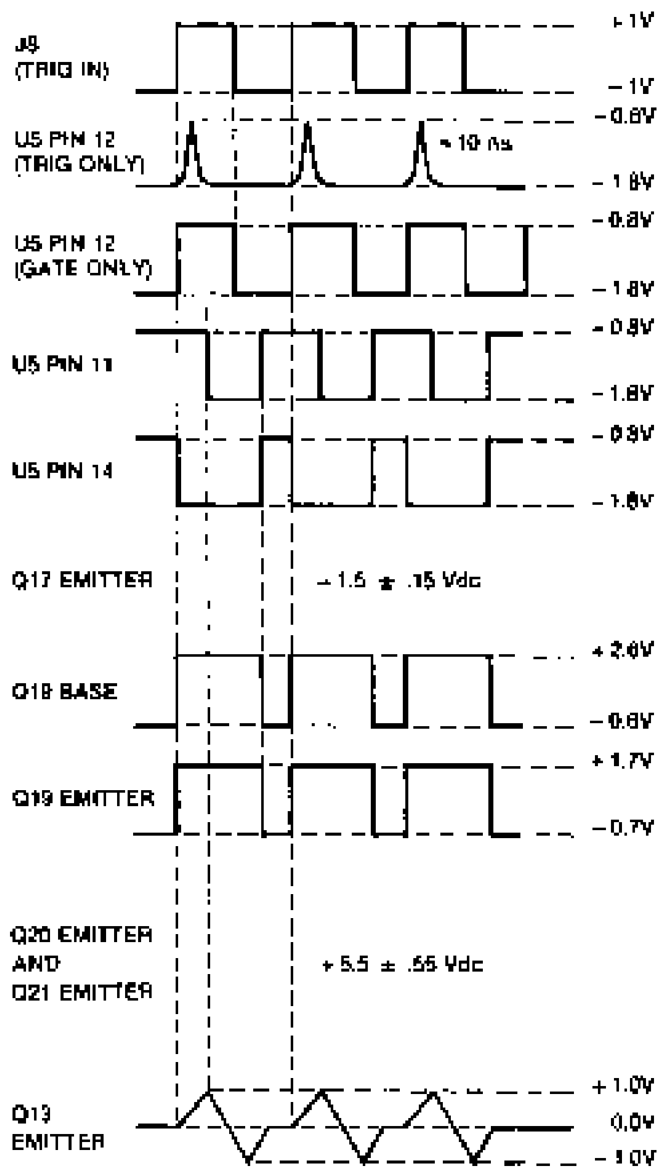


Figure 6-18. Trigger Baseline Waveforms

Continuous Mode Problems: Set the controls as shown; then take the waveform measurments. Refer to table 6-11.

Controls	Settings
FREQ/START FREQ	2.0
FREQ MULT	10K
SYM	Off
MODE	CONT

Table 6-11. Trigger Baseline Check (Continuous)

Test Point	Desired Results
U5 pin 12	− 0.8 ± .08 Vdc
U5 pin 14	− 1.8 ± .18 Vdc
Q17 emitter	− 1.5 ± .15 Vdc
Q19 base	+ 2.6 ± .26 Vdc
Q19 emitter	+ 1.7 ± .17 Vdc
Q20 emitter	+ 5.5 ± .55 Vdc
Q21 emitter	+ 5.5 ± .55 Vdc
Q13 emitter	± 1.0V triangle

6.4.12 Square Shaper Guide

Set the controls as shown; then perform the checks in table 6-12 and take waveform measurements. Refer to figure 6-19.

Controls	Settings
FREQ/START FREQ	2.0
FREQ MULT	1K
SYM	Off
MODE	CONT
FUNCTION	See Table 6-12 and Figure 6-19

Table 6-12. Square Shaper Checks

	Desired Results	
Test Point	Sine or Triangle	Square
Q22 emitter	- 3.0 ± .3 Vdc	- 3.0 ± .3 Vdc
U4 pin 13	− 0.8 ± .08 Vdc	− 4.3 ± .43 Vdc
Q26 base	− 0.8 ± .08 Vdc	− 4.2 ± .42 Vdc
Q26 emitter	− 1.6 ± .16 Vdc	− 4.0 ± .4 Vdc
CR24 anode	+ 1.6 ± .16 Vdc	− 1.5 ± .15 Vdc

6.4.13 Sine Converter Guide

Set the controls as shown; then perform the checks in table 6-13 and take waveform measurements. Refer to figure 6-20.

Controls	Settings
FREQ/START FREQ	2.0
FREQ MULT	1K
SYM	Off
MODE	CONT
FUNCTION	Sine

Table 6-13. Sine Converter Checks

Test Point	Desired Results
Junction R170 and R171	+ 14.8 ± 1.5 Vdc
Junction R173 and R174	− 14.8 ± 1.5 Vdc
U3 pin 2	0.0V (Full scale current = 2 mA

6.4.14 Preamplifier Guide

DC Problems: Set the FUNCTION control to DC, then perform the checks in table 6-14.

Table 6-14. Preamplifier Checks (DC)

Test Point	Desired Results
U1 pin 2	+ 14.86 ± 1.5 Vdc
U1 pin 3	− 0.7 ± .07 Vdc
U1 pin 13	− 1.4 ± .14 Vdc
U1 pin 9	− 0.7 ± .07 Vdc
U1 pin 4	0.0 ± 10 mV
U1 pin 8	0.0 ± 10 mV
U1 pin 12	+ 5.8 ± .58 Vdc
U1 pin 11	+ 6.6 ± .66 Vdc
Q27 base	+ 9.6 ± .96 Vdc
Q27 emitter	+ 10.3 ± 1 Vdc
Q28 collector	+ 11.3 ± 1.1 Vdc

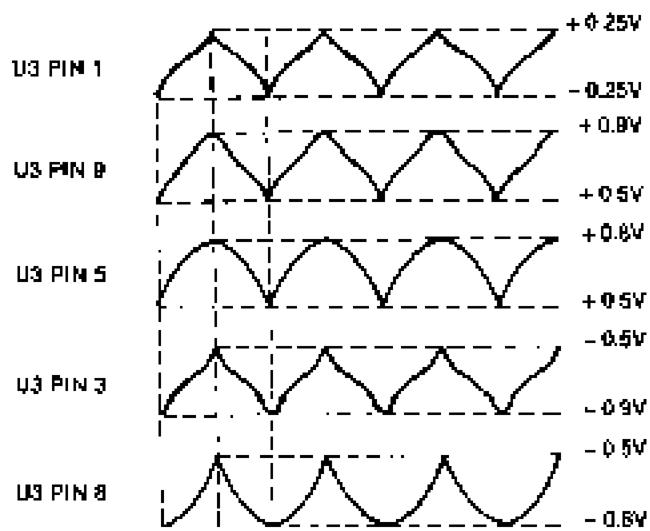


Figure 6-20. Sine Converter Waveforms

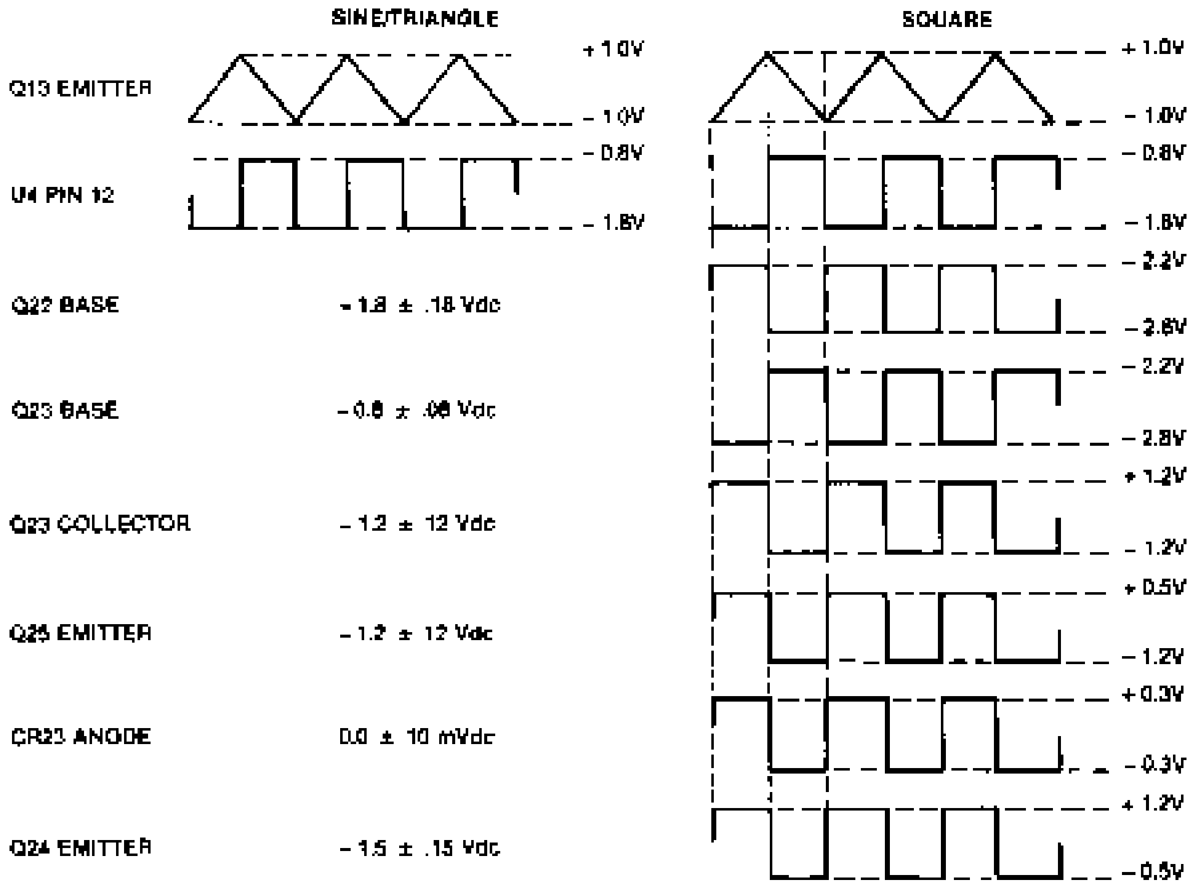


Figure 6-19. Square Shaper Waveforms

Function Problems: Set the controls as shown; then take the waveform measurements. Refer to figure 6-21.

Controls	Settings
FREQ/START FREQ	2.0
FREQ MULT	1K
SYM	Off
MODE	CONT
FUNCTION	Square

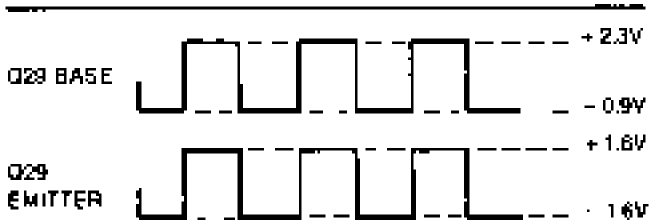


Figure 6-21. Preamplifier Waveforms

6.4.15 Output Amplifier Guide

Set the controls as shown; then take the waveform measurements. Refer to table 6-15.

Controls	Settings
FUNCTION	DC
DC OFFSET	Off

Table 6-15. Output Amplifier Checks

Test Point		Desired Results
Q30	Base	+ 11.7 ± 1.2 Vdc
	Emitter	+ [illegible] ± 1 [illegible] Vdc
	Collector	+ 19 ± 1.9 Vdc
Q32	Collector	+ 22.8 ± 2.3 Vdc
Q31	Base	− 12 ± 1.2 Vdc
	Emitter	− 11.3 ± 1.1 Vdc
	Collector	− 19 ± 1.9 Vdc

Table 6-15. **Output Amplifier Checks (Continued)**

Test Point		Desired Results
Q33	Collector	−22.7 ± 2.3 Vdc
Q36	Base	+18.3 ± 1.8 Vdc
	Emitter	+19 ± 1.9 Vdc
	Collector	+0.7 ± .07 Vdc
Q37	Emitter	+0.05 ± .005 Vdc
	Collector	+22.5 ± 2.3 Vdc
Q38	Emitter	+0.05 ± .005 Vdc
CR27	Cathode	+23 ± 2.3 Vdc
	Anode	+0.6 ± .06 Vdc
VR5	Input	+31 ± 3.1 Vdc
	Output	+24 ± 2.4 Vdc
Q34	Collector	−22.8 ± 2.3 Vdc
Q39	Base	−18.3 ± 1.8 Vdc
	Emitter	−19 ± 1.9 Vdc
	Collector	−0.05 ± .005 Vdc
Q40	Emitter	−0.05 ± .005 Vdc
	Collector	−21 ± 2.1 Vdc
Q41	Emitter	−0.05 ± .005 Vdc
CR28	Anode	−23 ± 2.3 Vdc
Q35	Base	−0.6 ± .06 Vdc
VR6	IN	−31 ± 3.1 Vdc
	ADJ	−21.3 ± 2.1 Vdc
	OUT	−23.6 ± 2.4 Vdc
U2	Pin 2	0.0 ± 10 mVdc
	Pin 6	−0.05 ± .005 Vdc

6.5 SWEEP/MOD BOARD TROUBLESHOOTING

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

Table 6-16 gives an index of common sweep/mod board symptoms. For each symptom a troubleshooting guide is referenced (Paragraphs 6.5.1 through 6.5.11) that, when correctly followed, will lead to a solution to the problem.

The troubleshooting guide is arranged in three (3) levels:

1. Identify improperly set controls.
2. Isolate the faulty functional blocks.
3. Identify the faulty circuit or component.

Individual component troubleshooting is given in paragraph 6.7, recommended test equipment is given in paragraph 5.2 and circuit schematics are in the back of this manual.

In all problems:

1. Double check for proper control settings.
2. Calibrate or rule out calibration as a problem.
3. Inspect components, wiring and circuit boards for heat damage.
4. Recalibrate as necessary after circuit repair.

Find the instrument symptom in table 6-16 and proceed as directed to the proper troubleshooting paragraph.

Table 6-16. **Sweep/Mod Board Related Problems**

Symptom	Paragraph
Amplitude Modulation At FUNC OUT Distorted or Missing	6.5.1
All Waveforms At AUX OUT Distorted or Missing	6.5.2
Output At AUX SYNC OUT Distorted or Missing	6.5.3
Loop Will Not Oscillate	6.5.4
Abnormal Waveforms (AUX OUT)	6.5.5
Waveform Symmetry Out of Specification	6.5.6
Incorrect Frequencies	6.5.7
Loop Oscillates In AUX GEN OFF MODE	6.5.8
AUX VCG Input Has No Effect	6.5.9
Variable Symmetry Bad	6.5.10
No Internal FM	6.5.11

6.5.1 Amplitude Modulation at FUNC OUT Distorted or Missing

Improperly set controls:

1. AUX GEN MODE and FUNC (Main Generator) switches must be set to AM.
2. WIDTH/ΔF/AM vernier must not be fully ccw.
3. AUX GEN and main generator frequency too low.
4. MODE (Main Generator) switch incorrectly set to TRIG or GATE.
5. Combination of OUTPUT ATTEN and AMPLITUDE controls excessively reducing signal.
6. DC OFFSET overdriving amplifier.

Functional block isolation:

If the amplitude modulated signal at the function out is distorted or missing, refer to figure 6-22.

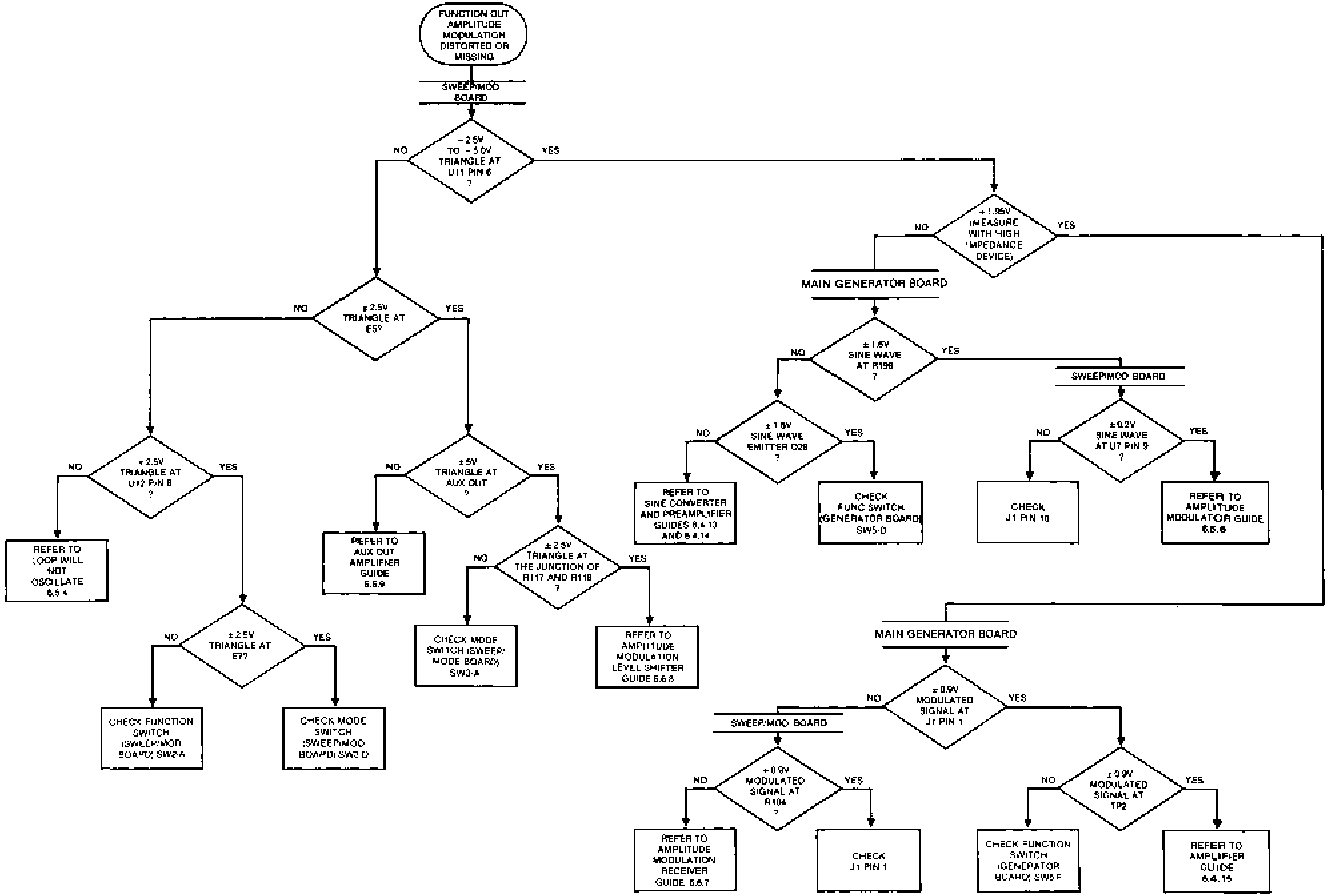


Figure 6-22. Amplitude Modulation Troubleshooting

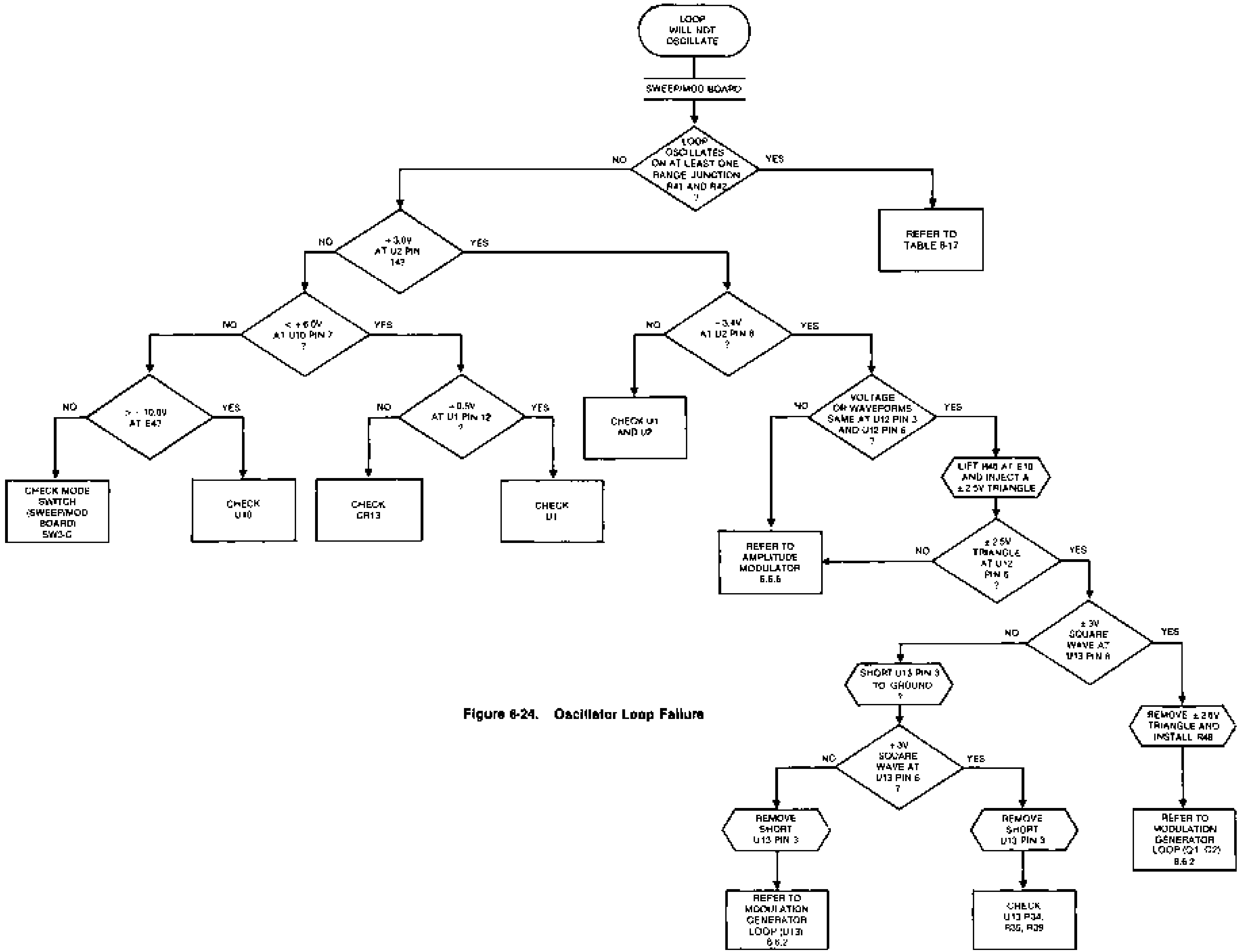


Figure 6-24. Oscillator Loop Failure

6.5.2 All Waveforms At AUX OUT Distorted or Missing

Improperly set controls.

1. AUX GEN frequency set too low.
2. AUX GEN MODE must be set to FM, SWEEP, AM, or AUX OUT ONLY.
3. WIDTH/ΔF/ΔM must not be fully ccw.

Functional block isolation

If all waveforms at AUX OUT remains distorted or missing, refer to figure 6-23.

6.5.3 Output At AUX SYNC OUT Distorted or Missing

Improperly set controls:

1. AUX GEN frequency too low
2. AUX GEN MODE incorrectly set to SET FREQ or SET WIDTH

Functional block isolation:

If a ± 3.0V square wave is at U13 pin 2, refer to paragraph 6.6.4; if not, refer to paragraph 6.5.4

6.5.4 Loop Will Not Oscillate

Improperly set controls:

1. AUX GEN frequency set too low
2. AUX GEN MODE incorrectly set to SET FREQ or SET WIDTH

Functional block isolation:

If the loop still does not oscillate, refer to figure 6-24.

6.5.5 Abnormal Waveforms At AUX OUT

1. Abnormal square wave, sine and triangle normal: If a + 2.8V square wave is present at the cathode of CR4, check function switch (Sweep/Mode board) SW2-A.

   If not, refer to paragraph 6.6.3
2. Abnormal sine wave, square and triangle normal. If a ± 2.5V sine wave is present at U6 pin 6, check the function switch (Sweep/Mod board) SW2-A.

   If not, refer to paragraph 6.6.5.
3. Abnormal triangle, square and sine normal:

   Check function switch (Sweep/Mod board) SW2-A.

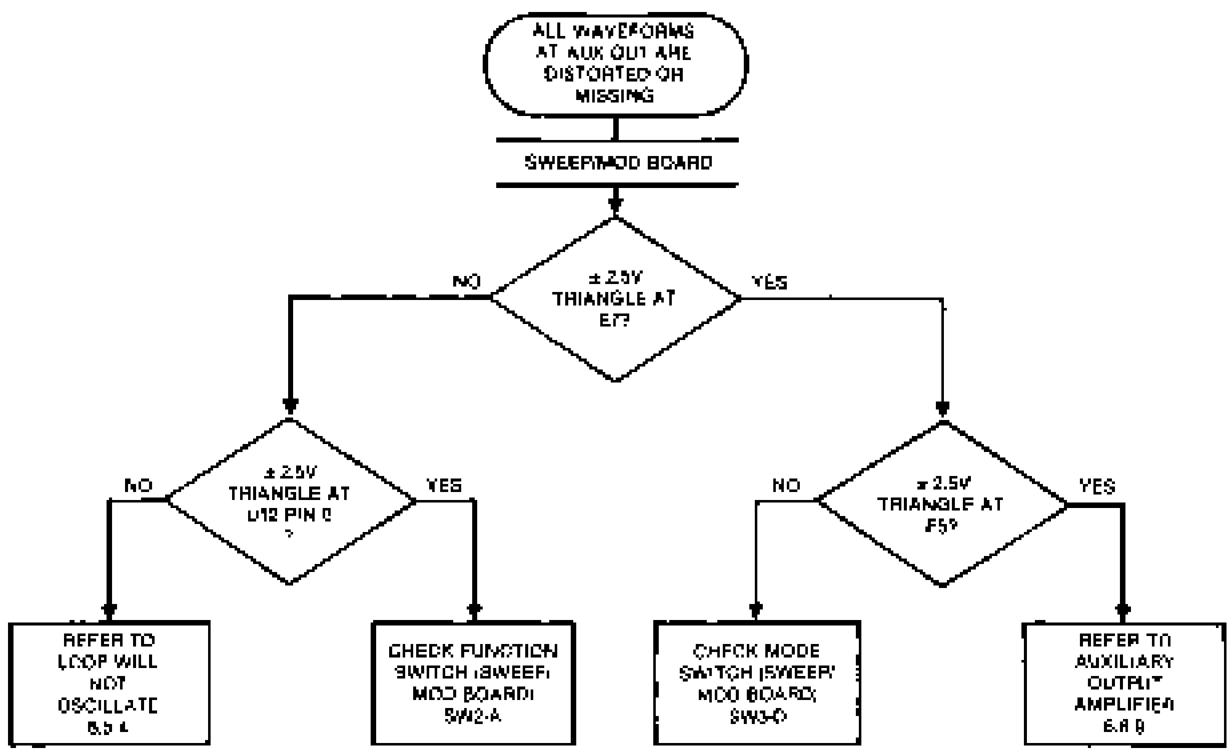


Figure 6-23. Distorted or Missing Waveforms at AUX OUT

Table 6-17. Oscillator Range Check

Inoperative Range	Check
3K–100K and 100–3K ranges only	C6 and SW1-A
3–100 and 1–3 ranges only	C5 and SW1-A
1–3 and 100–3K range only	R46, R47 and SW1-B

6.5.6 Waveform Symmetry Out of Specification

Improperly set controls:

1. AUX GEN FUNC switch incorrectly set to ⊓⊔ or ⩘.
2. Signal incorrectly connected to AUX VCG input.

Functional block isolation:

1. Verify 0V across R19. If not, check AUX GEN FUNC switch SW2-C.
2. Refer to paragraph 6.6.1, especially U1 and U2.

6.5.7 Incorrect Frequencies

Improperly set controls:

1. AUX GEN FUNC switch incorrectly set to ⊓ or ⟋.
2. Signal incorrectly connected to AUX VCG input.
3. WIDTH/ΔF/ΔM incorrectly set full ccw.

Functional block isolation:

If the frequencies are still incorrect, refer to table 6-18.

6.5.8 Loop Oscillates in AUX GEN OFF MODE

Improperly set controls:

AUX GEN MODE switch not set to AUX GEN OFF.

Functional block isolation:

If the Sweep/Mod generator continues to oscillate, refer to figure 6-25.

6.5.9 AUX VCG Input Has No Effect

Functional block isolation:

If the sweep/mod generator frequencies are correct

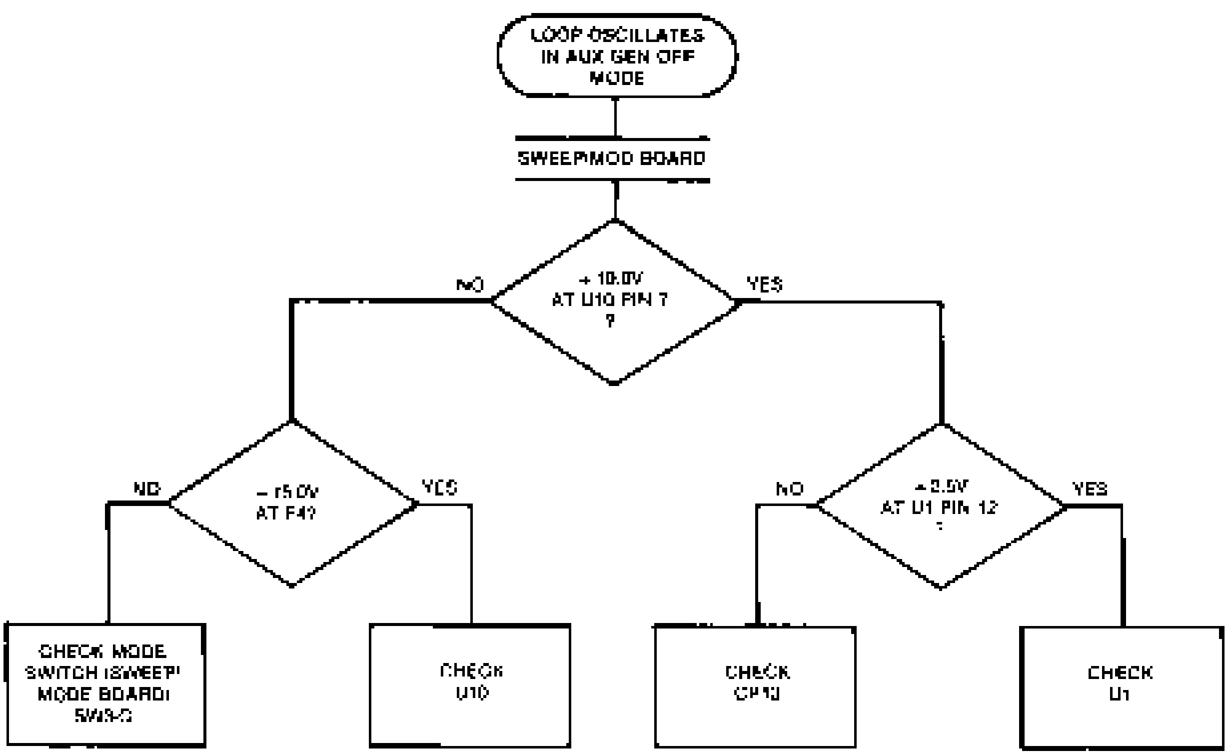


Figure 6-25. Loop Oscillates In AUX GEN OFF Mode

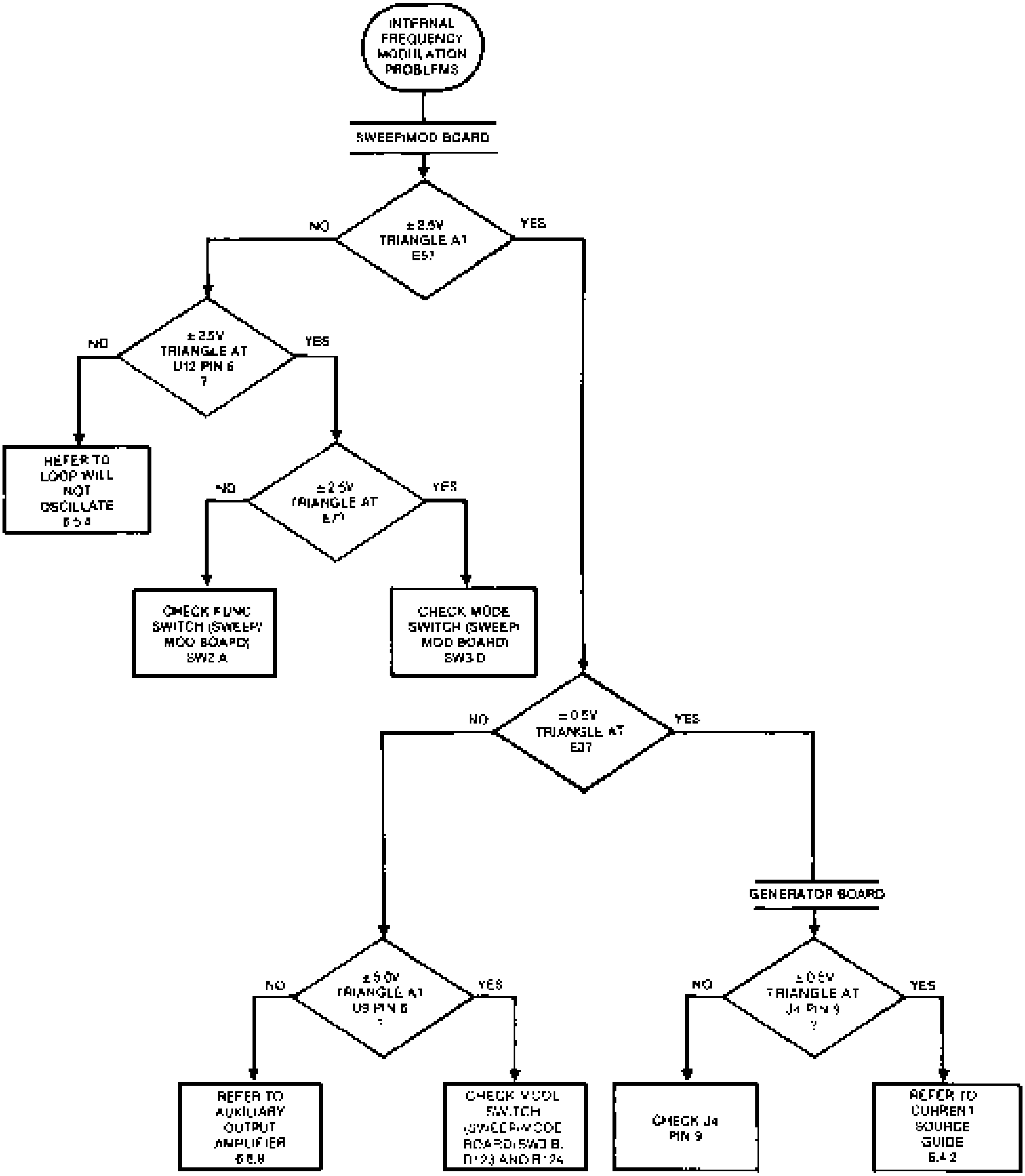


Figure 6-26. No Internal Frequency Modulation

(no AUX VCG input), check J16, J5 pin 1 and 2 and R5. If not, refer to paragraph 6.5.7.

Table 6-18. Incorrect Frequency Check

Incorrect Range	Check
3K/100K and 100/3K ranges only	C6 and SW1-A
3/100 and .1/3 ranges only	C5 and SW1-A
.1/3 and 100/3K range only	R46, R47 and SW1-B
All ranges	Modulation Generator VCG System 6.6.1 and SW1-B

6.5.10 Variable Symmetry (Sweep/Mod Board) Bad

Function block isolation:

If symmetry is normal in ∿, ⋀, or ⊓ functions, check SW2-B, SW2-C and R19. If not, refer to paragraph 6.6.1.

6.5.11 No Internal Frequency Modulation

Improperly set controls:

1. FREQ/START FREQ set to 2.0
2. WIDTH/ΔF/ΔM incorrectly set full ccw

Functional block isolation:

If the sweep/mod board still does not frequency modulate the generator board, refer to figure 6-26.

6.6 SWEEP/MOD BOARD CIRCUIT GUIDES

Circuit guides provide listings of voltage levels, waveforms, and hints that, when used with the schematics, are helpful in isolating faulty circuits. Table 6-19 is an index of circuit guides.

Table 6-19. Circuit Guide Index

Circuit Guide	Paragraph
Modulation Generation VCG System	6.6.1
Modulation Generator Loop	6.6.2
Square Wave Limiter	6.6.3
Modulation Gen Sync Out Amp	6.6.4
Sine Converter	6.6.5
Amplitude Modulator	6.6.6
Amplitude Modulation Receiver	6.6.7
Amplitude Modulation Level Shifter	6.6.8
Auxiliary Output Amp	6.6.9

6.6.1 Modulation Generator VCG System Guide

Set the controls as shown below, then perform the checks in table 6-20.

Control	Settings
AUX GEN FUNC	∿, ⋀, or ⊓
AUX GEN MODE	AM
AUX VCG Input	Disconnected

Table 6-20. VCG System Checks

Test Point	Desired Results AUX GEN VERNIER	
	ccw	cw
J1 pin 7 and 10	10 ± 1 mV	−550 ± 55 mV
J1 pin 1	+10 ± 1 mV	+550 ± 55 mV
J1 pin 14	+8 ± .8V	−8.9 ± .9V
J1 pin 12	0 ± 10 mV	+500 ± 50 mV
U2 pin 10 and 13	+4.5 ± .45V	+4.5 ± .45V
U2 pin 1	+14 ± 1.4V	+3.3 ± .3V
CR1 anode	+8.3 ± .8V	−3 ± .3V
U1 pin 9	−7.4 ± .7V	+8.7 ± .9V
U2 pin 4 and 7	4.6 ± .46V	−4.6 ± .46V
U2 pin 5	13.9 ± 1.4V	−3.4 ± .34V
CR2 cathode	−7.8 ± .8V	+3 ± .3V

6.6.2 Modulation Generator Loop Guide

Set the AUX GEN MODE switch to AM; then take the waveform measurements. Refer to figure 6-27.

6.6.3 Square Wave Limiter Guide

Set the AUX GEN MODE switch to AM; then take the waveform measurements. See figure 6-28.

6.6.4 Modulation Generator Sync Output Amplifier Guide

Set the AUX GEN Mode switch to AM, then take waveform measurements. Refer to figure 6-29.

6.6.5 Sine Converter Guide

Set the AUX GEN MODE switch to AM; then perform the checks in table 6-21 and take waveform measurements. Refer to figure 6-30.

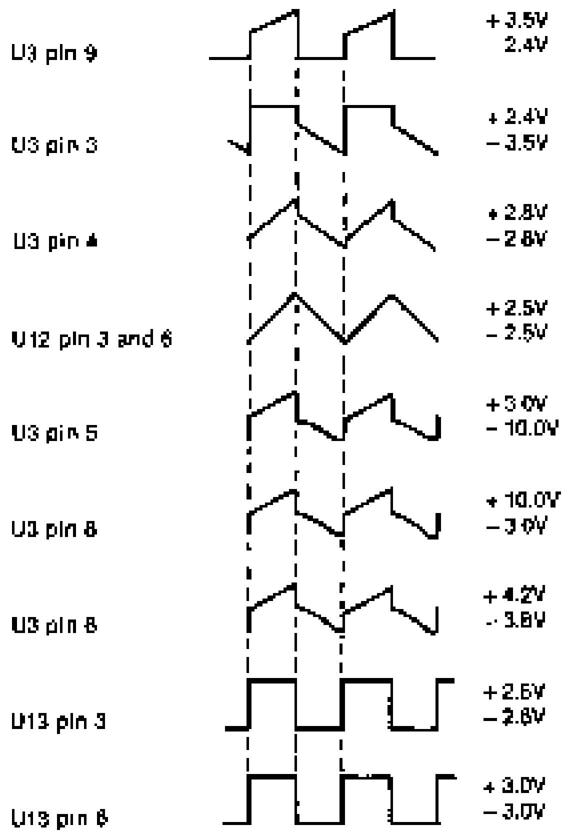


Figure 6-27. Modulation Generator Waveform

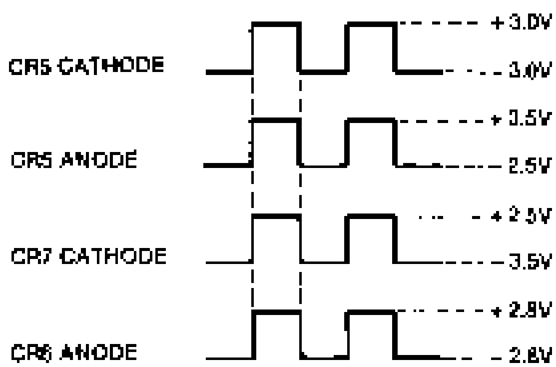


Figure 6-28. Square Wave Limiter Waveforms

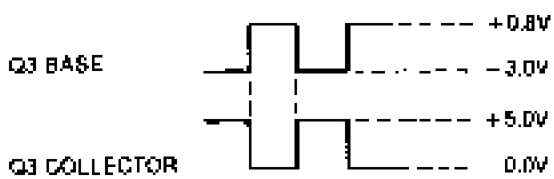


Figure 6-29. Mod Gen Sync Out Amp. Waveforms

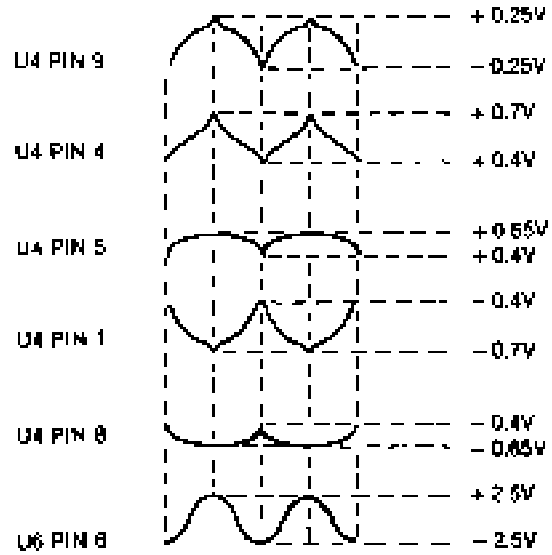


Figure 6-30. Sine Converter Waveforms

Table 6-21. Sine Converter Checks

Test Point	Desired Results
R57/RT1 junction	−2.3 ± .02 Vdc
U6 pins 2 and 3, U5 pins 2 and 6	0 ± 10 mVdc

6.6.6 Amplitude Modulator Guide

Set the controls as shown; then perform the checks in table 6-22 and take the waveform measurements. Refer to figure 6-31.

Control	Setting
AUX GEN MODE	AM
WIDTH/ΔF/ΔM	Full cw
AM CARRIER LEVEL/NULL	Full cw
SUPPRESSED CARRIER	Off
FUNC (Main Generator)	AM

6.6.7 Amplitude Modulation Receiver Guide

Set the controls as shown; then perform the checks in table 6-23 and take waveform measurements. Refer to figure 6-32.

Control	Settings
AUX GEN MODE	AM
WIDTH/ΔF/ΔM	Full cw
AM CARRIER LEVEL/NULL	Full cw
SUPPRESSED CARRIER	Off
AUX GEN FUNC	Sine
FUNC (Main Generator)	AM

Table 6-22. Amplitude Modulator Checks

Test Point	Desired Results
U7 pin 1	+1.45 ± 0.14 Vdc
U7 pin 2	+1.95 ± 0.19 Vdc (measured with high impedance device)
U7 pin 3	−13.0 ± 1.3 Vdc
U7 pin 4	−2.5 ± 0.25 Vdc
U7 pin 5	−3.8 ± 0.38 Vdc
U7 pin 11	−1.35 ± 0.13 Vdc
U7 pin 12	0 ± 10 mVdc
U7 pin 13	−12 ± 1.2 Vdc
U7 pin 14	+1.95 ± 0.19 Vdc

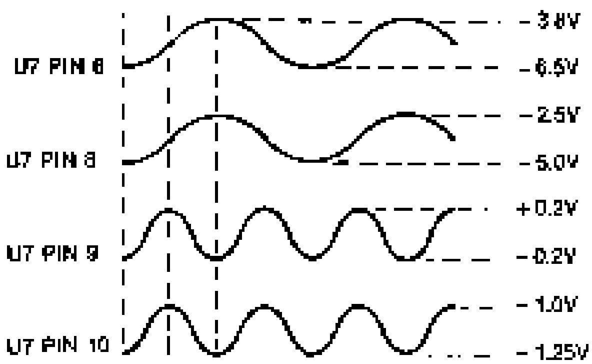


Figure 6-31. Amplitude Modulator Waveforms

Table 6-23. AM Receiver Guide

Test Point	Desired Results
U8 pin 3	−14.7 ± 1.4 Vdc
U8 pin 4	+1.25 ± .12 Vdc
U8 pins 5 and 8	+2 ± .2 Vdc
U8 pins 10 and 13	+14.1 ± 1.4 Vdc
U8 pin 11	+13.3 ± 1.3 Vdc
Q4 collector	+13.8 ± 1.3 Vdc

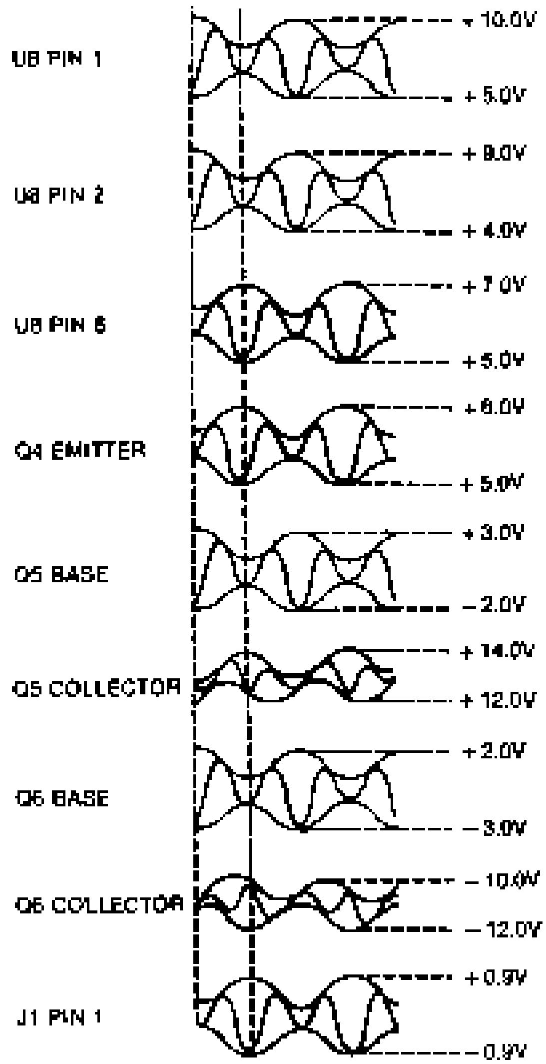


Figure 6-32. AM Receiver Waveforms

6.6.8 Amplitude Modulation Level Shifter Guide

Set the controls as shown; then take the waveform measurements. Refer to figure 6-33.

Control	Setting
AUX GEN MODE	AM
WIDTH/ΔF/ΔM	Full cw
AM CARRIER LEVEL/NULL	Full cw
SUPPRESSED CARRIER	Off
AUX GEN FUNC	Triangle
FUNC (Main Generator)	AM

6.6.9 Auxiliary Output Amplifier Guide

Set the controls as shown; then take the waveform measurements. Refer to figure 6-34.

Control	Setting
AUX GEN MODE	AM
WIDTH/ΔF/ΔM	Full cw
AM CARRIER LEVEL/NULL	Full ccw
SUPPRESSED CARRIER	Off
FUNC (Main Generator)	AM
AUX GEN FUNC	Triangle

Figure 6-33. AM Level Shifter Waveforms

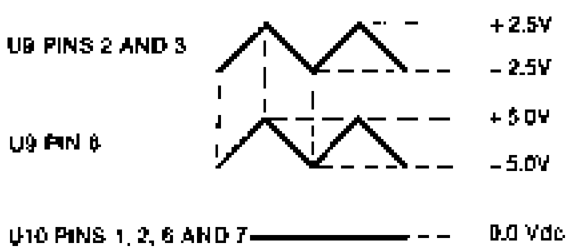


Figure 6-34. Auxiliary Output Amplifier Waveforms

6.7 TROUBLESHOOTING INDIVIDUAL COMPONENTS

6.7.1 Transistor

1. A transistor is defective if more than one volt is measured across its base-emitter junction in the forward direction.
2. A transistor when used as a switch may have a few volts reverse bias voltage across base emitter junction.
3. If the collector and emitter voltages are the same, but the base emitter voltage is less than 500 mV forward voltage (or reversed bias), the transistor is defective.
4. A transistor is defective if its base current is larger than 10% of its emitter current (calculate currents from voltage across the base and emitter series resistors).
5. In a transistor differential pair (common emitter stages) either their base voltages are the same in normal operating condition, or the one with less forward voltage across its base emitter junction should be off (no collector current); otherwise one of the transistors is defective.

6.7.2 Diode

A diode (except a zener) is defective if there is greater than one volt (typically 0.7 volt) forward voltage across it.

6.7.3 Operational Amplifier

1. The "+" and "−" inputs of an operational amplifier will have less than 15 mV voltage difference when operating under normal conditions.
2. When the output of the amplifier is connected to the "−" input (voltage follower connection), the output should be the same voltage as the "+" input voltage, otherwise, the operational amplifier is defective.
3. If the output voltage stays at maximum positive, the "+" input voltage should be more positive than "−" input voltage, or vice versa; otherwise, the operational amplifier is defective.

6.7.4 FET Transistor

1. No gate current should be drawn by the gate of an FET transistor. If so, the transistor is defective.
2. The gate-to-source voltage is always reverse biased under a normal operating condition, e.g., the source voltage is more positive than the gate voltage for 2N5485, and the source voltage is more negative than gate voltage for a 2N5462. Otherwise, the FET is defective.
3. If the device supplying gate voltage to an FET saturates, the FET has too large a Vgs (pinch off) for the circuit and should be replaced.

6.7.5 Capacitor

1. Shorted capacitors have 0V across their terminals.
2. Opened capacitor can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.
3. Leaky capacitors will often have a decreased voltage across their terminals.

6.7.6 Digital ECL ICs

1. The device is operating correctly if the output high state is −0.81 to −0.96V and low state is −1.65 to −1.85V.
2. The input must show the same two levels as in step 1.

SECTION 7
PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

7.2 ADDENDA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to sumarize the changes made and are inserted immediately inside the rear cover. If no such pages exist, the manual is correct as printed.

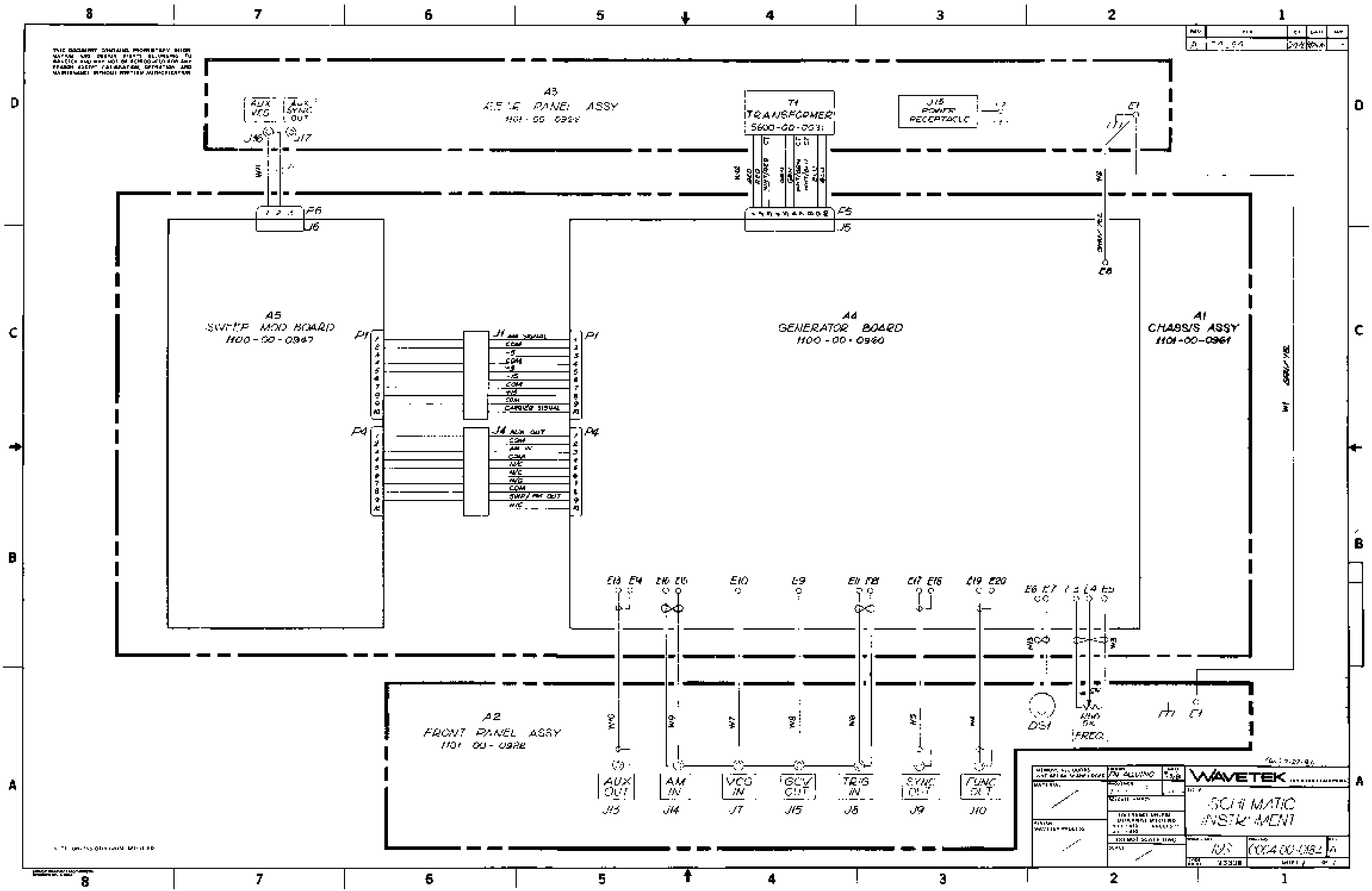
7.3 ORDERING PARTS

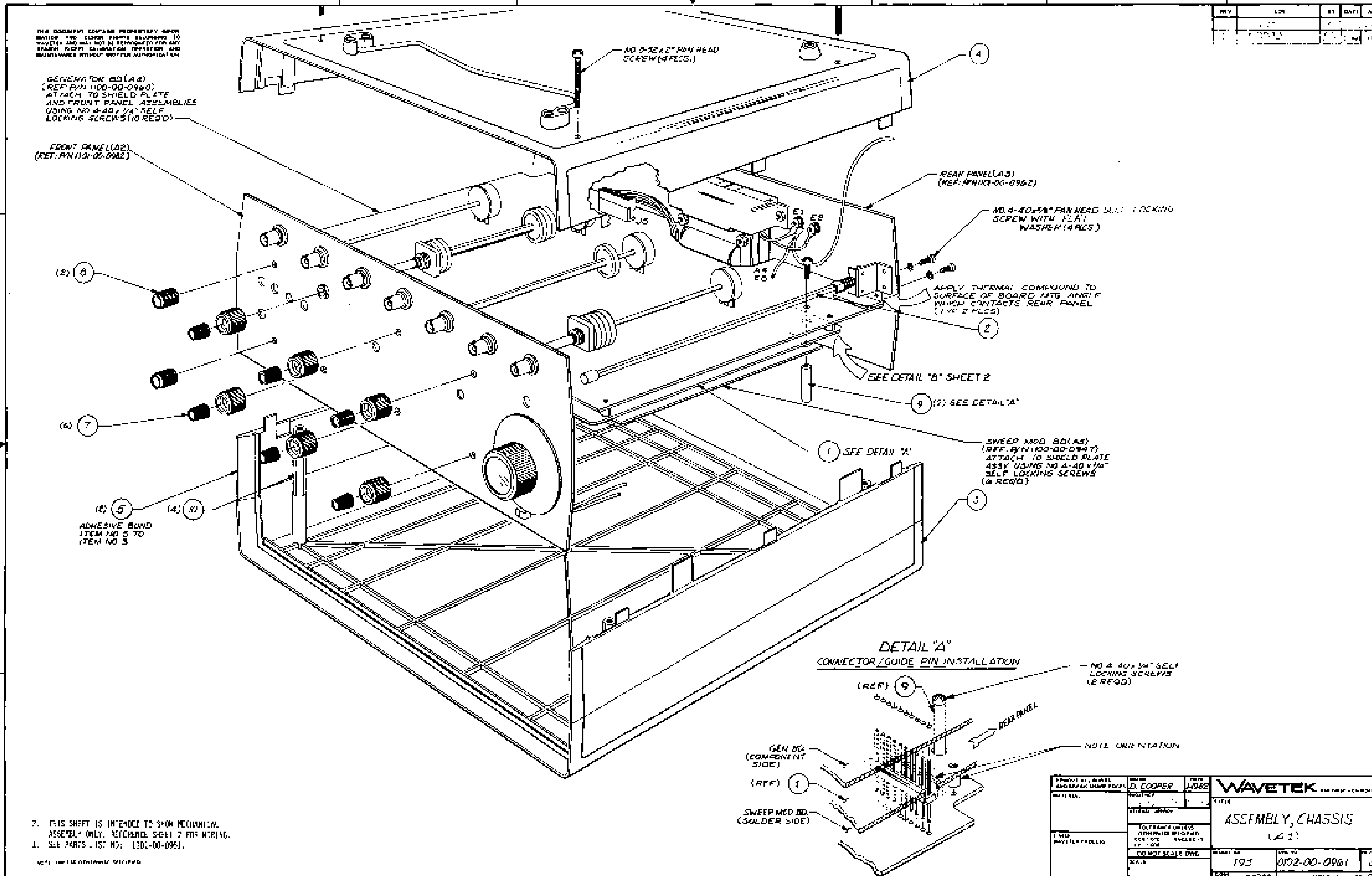
When ordering spare parts, please specify part number, circuit reference, board, serial number of unit, and, if applicable, the function performed.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

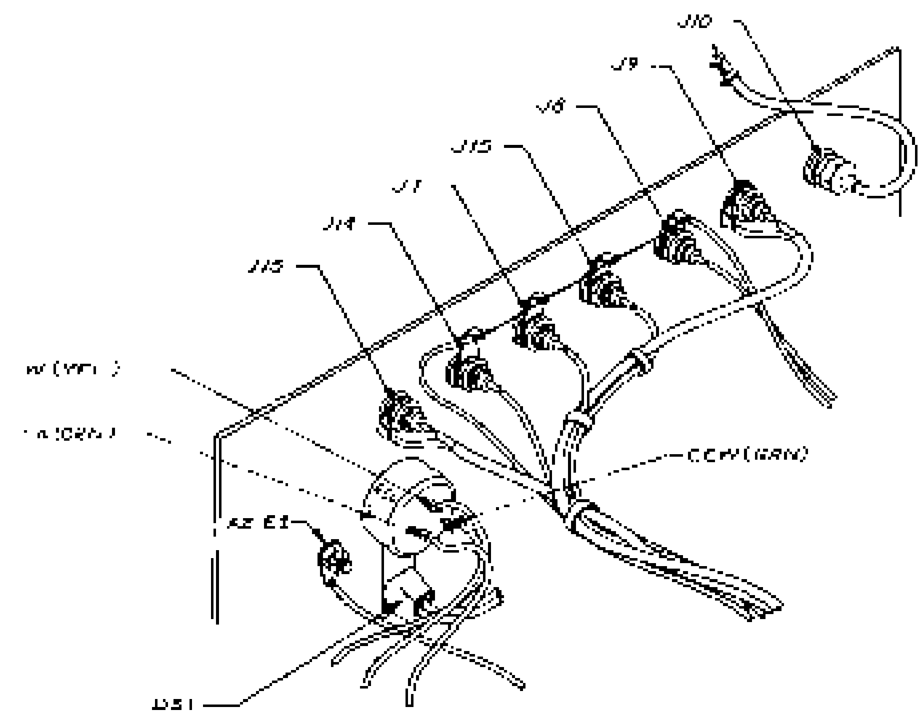
DRAWING	DRAWING NUMBER
Instrument Schematic	0004-00-0182
Chassis Assembly	0102-00-0961
Chassis Parts Lists	1101-00-0961
Generator Board Schematic	0103-00-2926
Generator Board Assembly	1100-00-0834
Generator Board Parts List	1100-00-0960
Generator Board Switch Detent	0102-00-0963
Generator Board Switch Parts List	1202-00-0963
Sweep/Mod Board Schematic	0103-00-0947
Sweep/Mod Board Assembly	1100-00-0947
Sweep/Mod Board Parts List	1100-00-0947
Sweep/Mod Switch Detent	0102-00-0965
Sweep/Mod Switch Parts List	1202-00-0965
Rear Panel Assembly	0102-00-0962
Rear Panel Parts List	1101-00-0962
Front Panel Assembly	0102-00-0982
Front Panel Parts List	1101-00-0982


A3
REAR PANEL ASSY
AUX VCG
AUX SYNC OUT
J16
J17
T1
TRANSFORMER
5600-00-0031
J15
POWER RECEPTACLE
E1
A5
SWEEP MOD BOARD
1100-00-0947
A4
GENERATOR BOARD
1100-00-0960
A1
CHASSIS ASSY
1101-00-0961
P6
J6
P5
J5
E8
P1
J1
AM SIGNAL
COM
-15
COM
+5
-15
COM
+15
COM
CARRIER SIGNAL
P4
J4
AUX OUT
COM
AM IN
COM
N/C
N/C
N/C
COM
SWP/FM OUT
N/C
A2
FRONT PANEL ASSY
1101-00-0922
AUX OUT
J15
AM IN
J14
VCO IN
J7
GCV OUT
J15
TRIG IN
J8
SYNC OUT
J9
FUNC OUT
J10
DS1
FREQ
WAVETEK
SCHEMATIC
INSTRUMENT
0004-00-0182

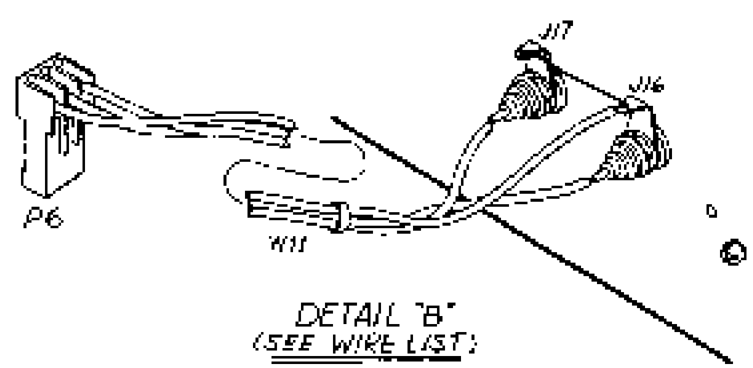


GENERATOR BD (A4)
(REF P/N 1100-00-0960)
ATTACH TO SHIELD PLATE
AND FRONT PANEL ASSEMBLIES
USING NO 4-40 x 1/4" SELF
LOCKING SCREWS (10 REQ'D)
FRONT PANEL (A2)
(REF: P/N 1101-00-0962)
NO 8-32 x 2" PAN HEAD
SCREW (4 PLCS.)
4
REAR PANEL (A3)
(REF: P/N 1103-00-0962)
NO. 4-40 x 5/8" PAN HEAD SELF LOCKING
SCREW WITH FLAT
WASHER (4 PLCS)
APPLY THERMAL COMPOUND TO
SURFACE OF BOARD MTG ANGLE
WHICH CONTACTS REAR PANEL
(TYP 2 PLCS)
2
SEE DETAIL "B" SHEET 2
9 (2) SEE DETAIL "A"
1 SEE DETAIL "A"
SWEEP MOD BD (A5)
(REF. P/N 1100-00-0947)
ATTACH TO SHIELD PLATE
ASSY USING NO 4-40 x 1/4"
SELF LOCKING SCREWS
(4 REQ'D)
3
(8) 6
(6) 7
(8) 5
(4) 10
ADHESIVE BOND
ITEM NO 5 TO
ITEM NO 3
J5
E1
E8
A4
E6
DETAIL "A"
CONNECTOR / GUIDE PIN INSTALLATION
NO 4-40 x 1/4" SELF
LOCKING SCREWS
(2 REQ'D)
(REF) 9
REAR PANEL
NOTE ORIENTATION
GEN BD
(COMPONENT
SIDE)
(REF) 1
SWEEP MOD BD.
(SOLDER SIDE)
2. THIS SHEET IS INTENDED TO SHOW MECHANICAL
ASSEMBLY ONLY. REFERENCE SHEET 2 FOR WIRING.
1. SEE PARTS LIST NO: 1102-00-0961.
NOTES: UNLESS OTHERWISE SPECIFIED
D. COOPER
DO NOT SCALE DWG
WAVETEK
ASSEMBLY, CHASSIS
195
0102-00-0961
C
33338
SHEET 1 OF 2

CHASSIS ASSEMBLY WIRE & CABLE HOOK-UP			
REF DES	DESTINATION FROM	DESTINATION TO	COLOR
W1	REAR PANEL - A3 E1	FRONT PANEL - A2 E1	GRN/YEL
W2	REAR PANEL - A3 E1	GEN BD - A1 E6	GRN/YEL
W3	GEN BD - E3	FRONT PANEL - R56-CW	ORN
	GEN BD - E4	FRONT PANEL - R56-W	YEL
	GEN BD - E5	FRONT PANEL - R56-CCW	GRN
W4	GEN BD - E19	FRONT PANEL - J10	BLK
	GEN BD - E20 ⏚	FRONT PANEL - J10 ⏚	
W5	GEN BD - E17	FRONT PANEL - J9	BLK
	GEN BD - E18 ⏚	FRONT PANEL - J9 ⏚	
W6	GEN BD - E11	FRONT PANEL - J8	WHT/BRN
	GEN BD - E21 ⏚	FRONT PANEL - J8 ⏚	BLK
W7	GEN BD - E10	FRONT PANEL - J7	WHT/BLU
W8	GEN BD - E9	FRONT PANEL - J15	WHT
W9	GEN BD - E15	FRONT PANEL - J14	WHT/GRN
	GEN BD - E16 ⏚	FRONT PANEL - J14 ⏚	BLK
W10	GEN BD - E13	FRONT PANEL - J13	BLK
	- E14	FRONT PANEL - J13 ⏚	
W11	REAR PANEL - J16	SWEEP MOD BD J6	N/A
	REAR PANEL - J17	SWEEP MOD BD J6	N/A
	REAR PANEL - ⏚	SWEEP MOD BD J6 ⏚	N/A
W12	REAR PANEL - A2	GEN BD J5	N/A
W13	GEN BD - A1 E5	FRONT PANEL DS1	N/A
	GEN BD - A1 E7	FRONT PANEL DS1	N/A



FRONT PANEL WIRING
AND ROUTING
(SEE WIRE LIST)



DETAIL "B"
(SEE WIRE LIST)

1. THIS SHEET IS INTENDED TO LIST WIRING HOOK UP. SEE SHEET 1 FOR MECHANICAL ASSEMBLY.

WAVETEK

ASSEMBLY, CHASSIS (A1)

DRAWN CHERMACK

0102-00-0961

23338

SHEET 2 OF 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	ASSY, DRAW CHASSIS	0102-00-0961	WVTK	0102-00-0961	[illegible]
2	BRK, MACH, POWER SUP	[illegible]	WVTK	[illegible]	1
1	ASSY, SHIELD PLATE	190-1048	WVTK	1206-00-1048	[illegible]
NONE	ASSY, CHASSIS CABLE KIT	190-0964	WVTK	[illegible]	1
NONE	PLATE, NAME	139-305	WVTK	[illegible]	1
NONE	COVER, TOP	180-300-1	WVTK	[illegible]	1
[illegible]	[illegible]	[illegible]	WVTK	1400-00-5010	2
NONE	COVER, BOTTOM	180-300-2	WVTK	1400-00-5500	1
[illegible]	GUIDE PIN	[illegible]	WVTK	[illegible]	[illegible]
7	[illegible]	[illegible]	ROGAN	2400-01-0007	6
8	KNOB, SMALL	[illegible]	ROGAN	2400-01-0010	2
10	STANDOFF, MALE/FEMALE [illegible]	[illegible]	[illegible]	[illegible]	4
NONE	RAIL, ASSY [illegible]	180-50C	WVTK	[illegible]	1
NONE	SPEEDNUT, SELF RETAIN	[illegible]	[illegible]	[illegible]	[illegible]

WAVETEK PARTS LIST

ASSY CHASSIS

ASSEMBLY NO 1101-00-0961

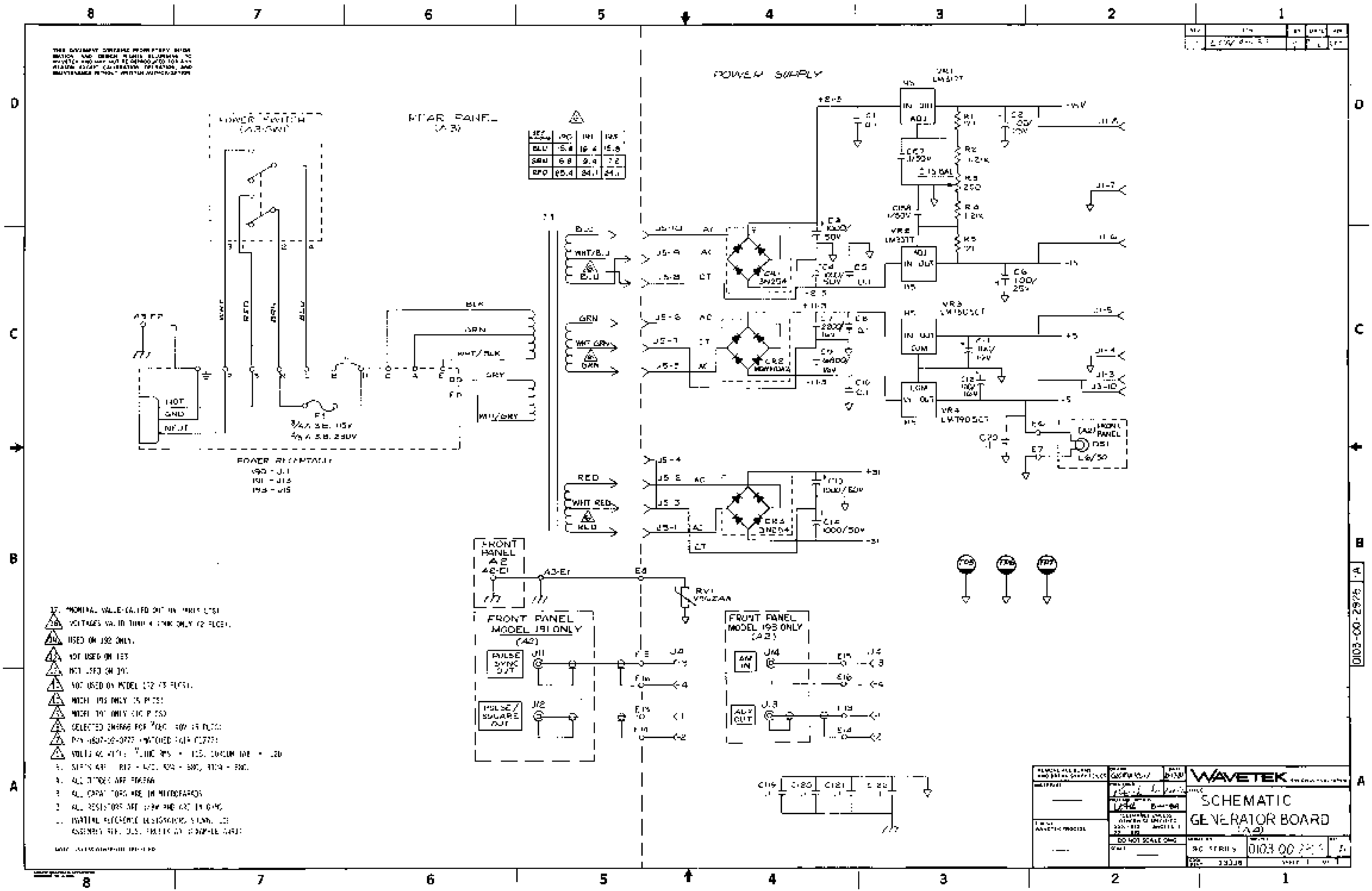
PAGE 2

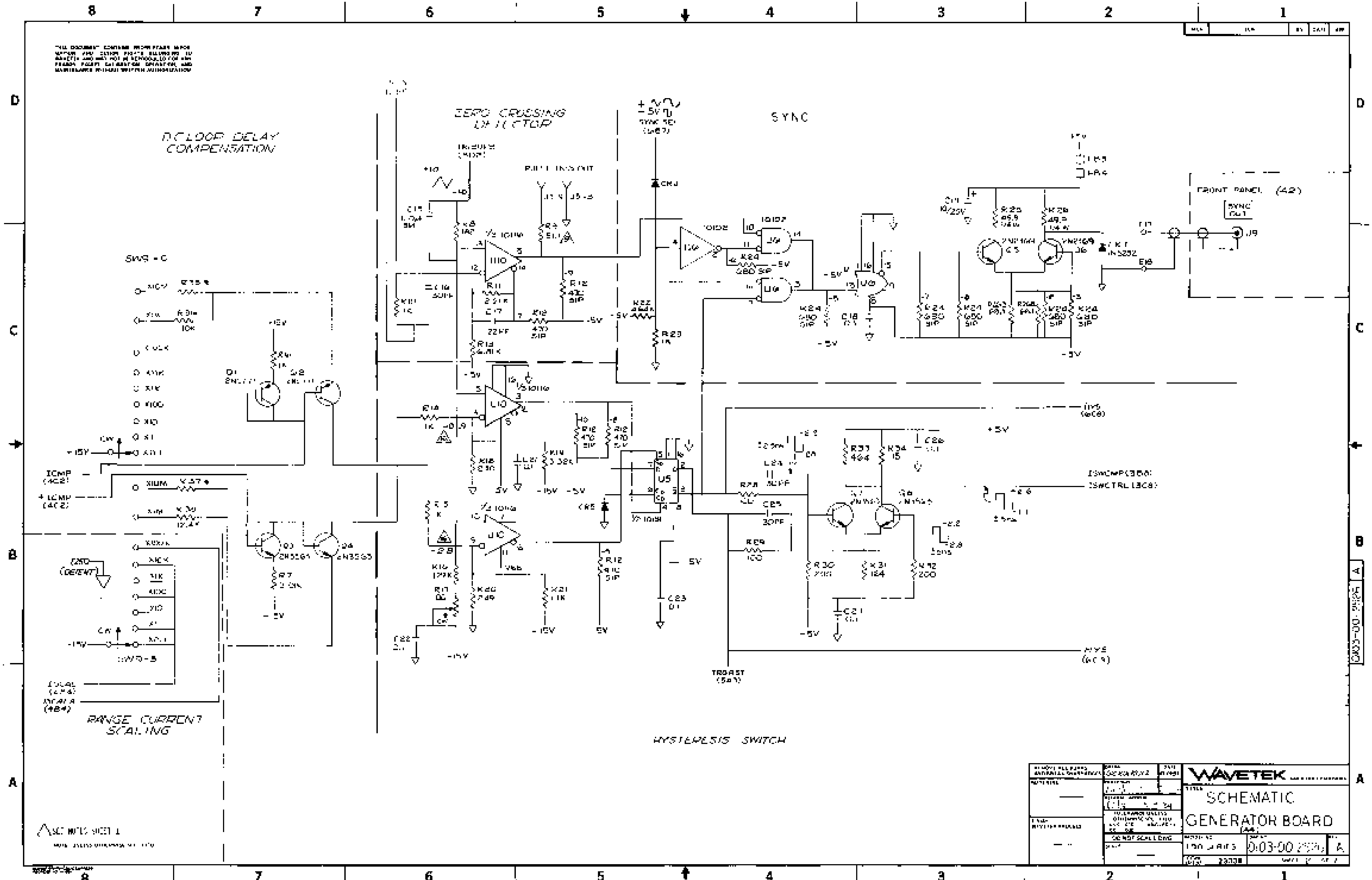
WAVETEK

PARTS LIST
ASSY, CHASSIS

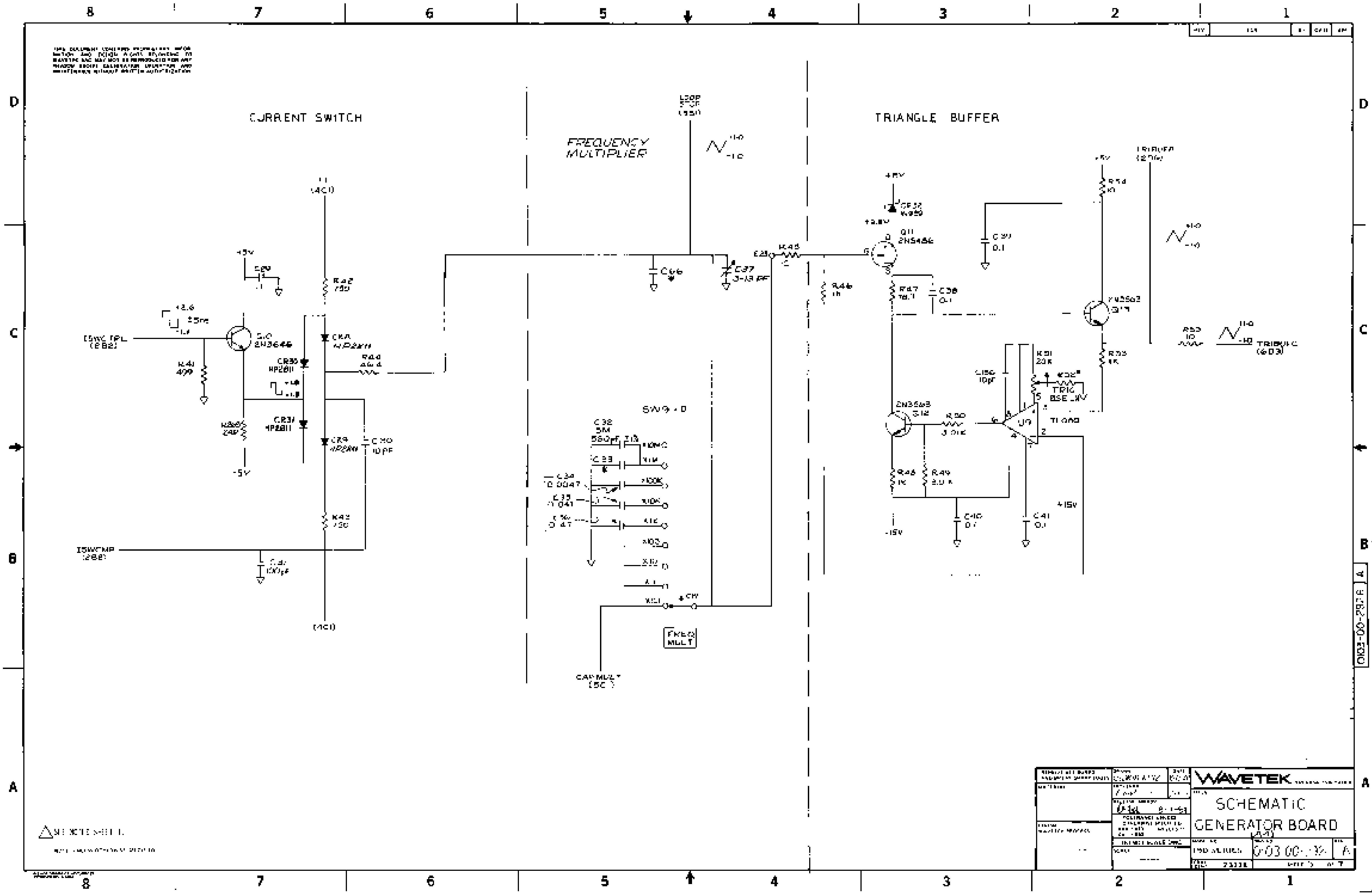
193 | 1101-00-0961 | A

SHEET 1 OF 1

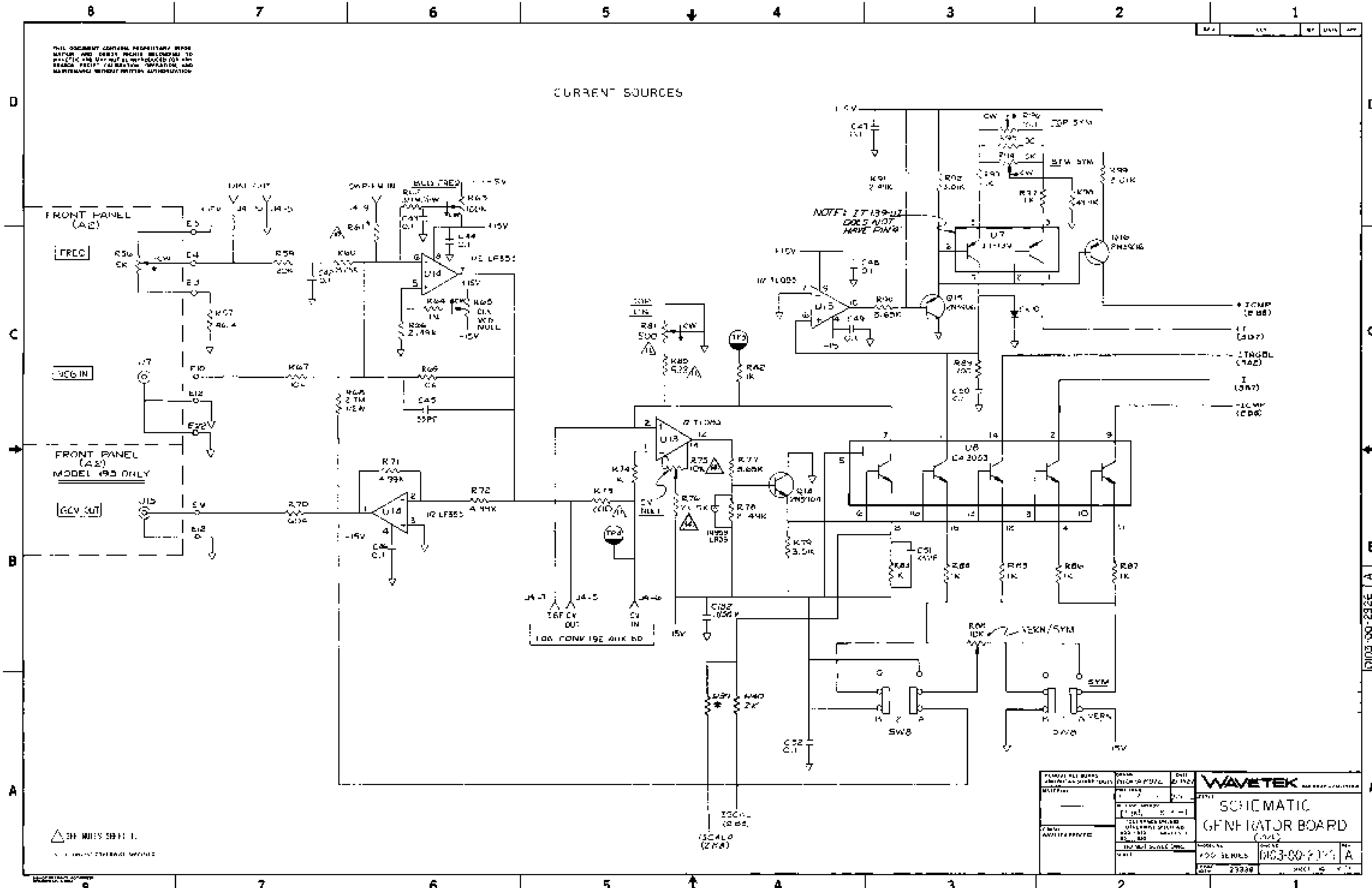

POWER SUPPLY
POWER SWITCH
REAR PANEL
(A3)
POWER RECEPTACLE
FRONT PANEL
A2
FRONT PANEL
MODEL 191 ONLY
(A2)
PULSE SYNC OUT
PULSE/SQUARE OUT
FRONT PANEL
MODEL 193 ONLY
(A2)
AM IN
ADJ OUT
VR1
LM317T
VR2
LM337T
VR3
LM340CT
VR4
LM7905CT
3/4A S.B. 115V
3/8A S.B. 230V
F1
+15V
-15
+5
-5
1000/50V
WAVETEK
SCHEMATIC
GENERATOR BOARD
(A2)
DO NOT SCALE DWG
0103-00-2975

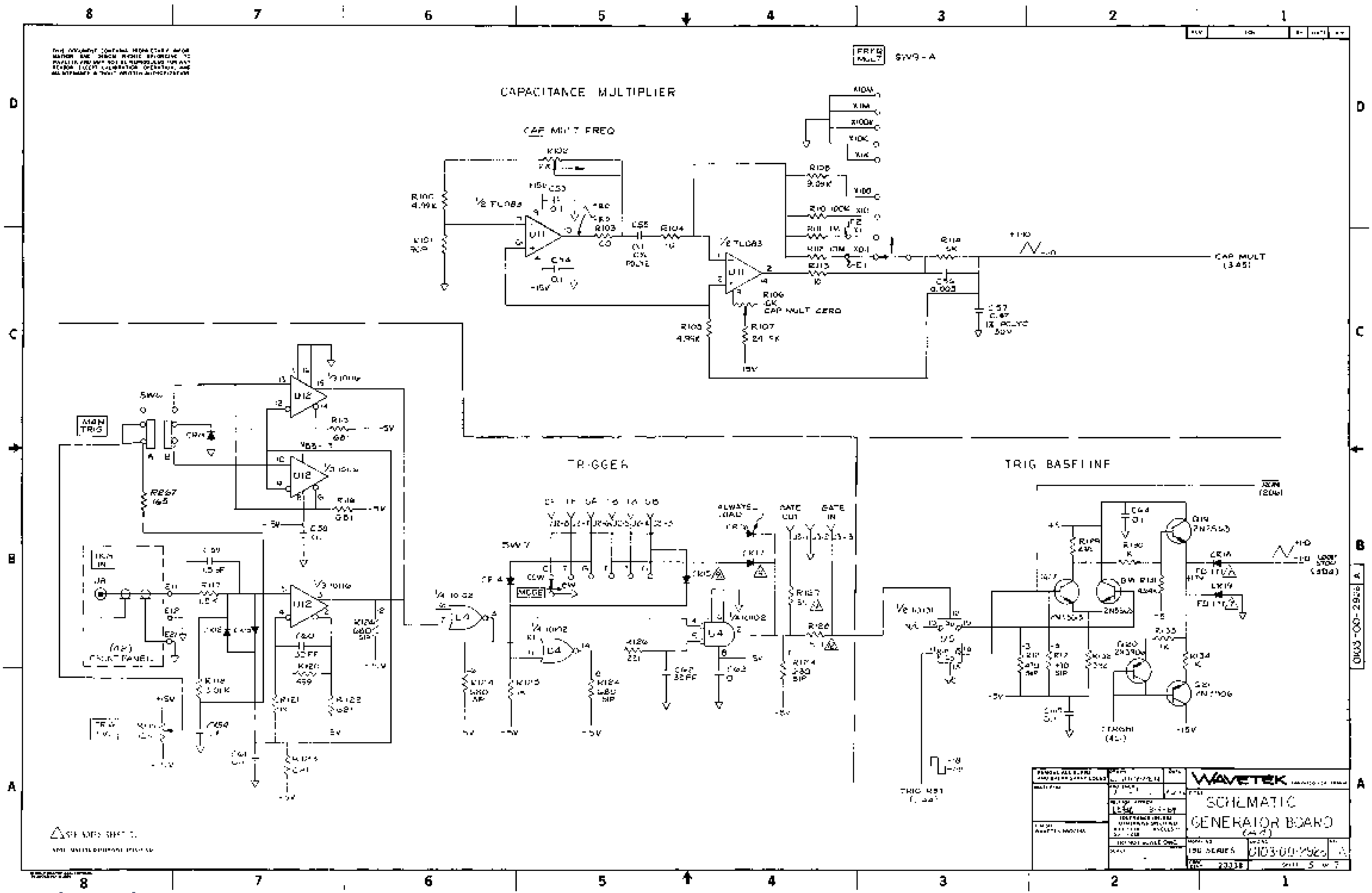


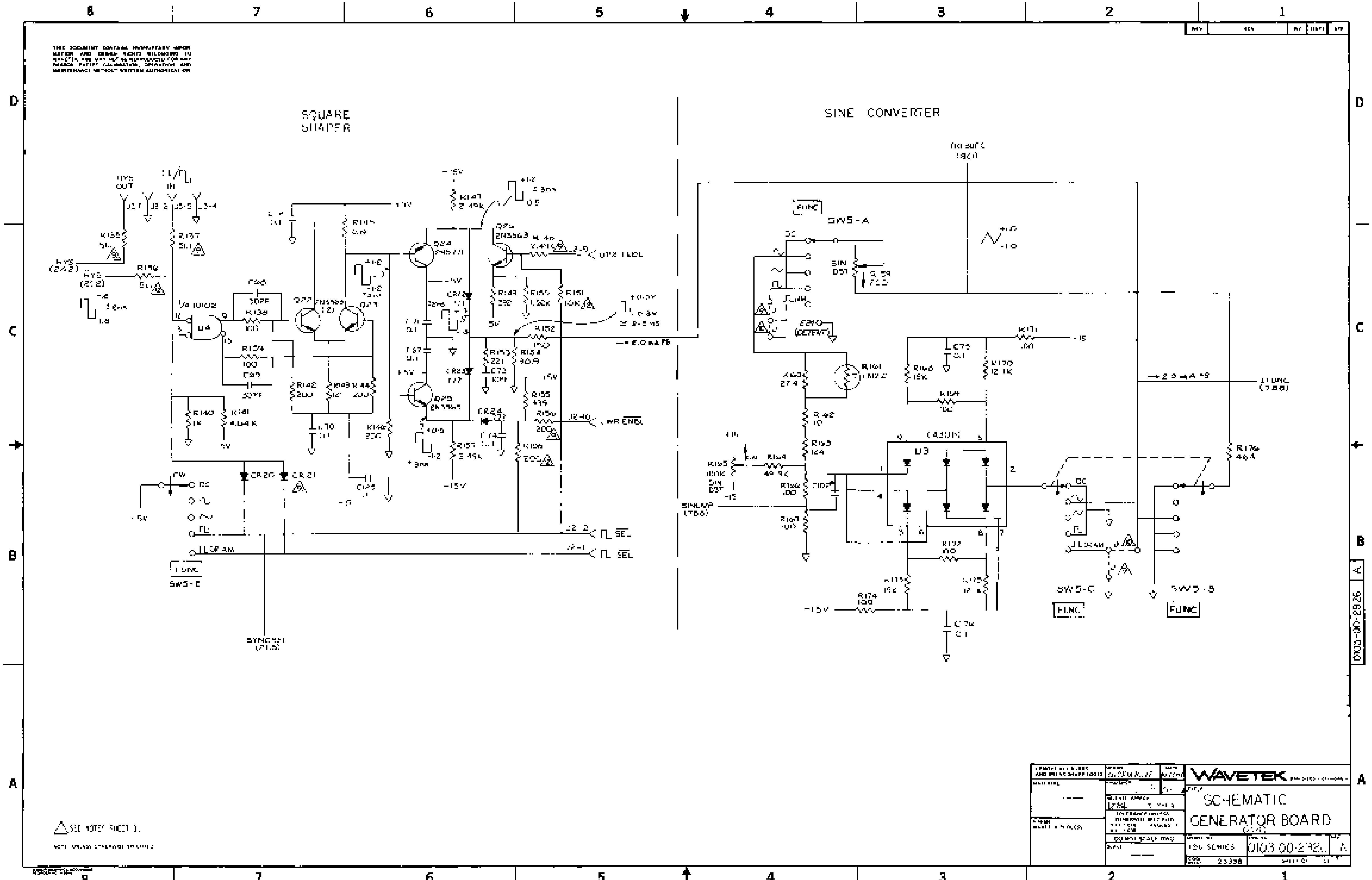
DC LOOP DELAY COMPENSATION
ZERO CROSSING DETECTOR
SYNC
PULL TO SYNC OUT
FRONT PANEL (A2)
SYNC OUT
SWG - C
SWG - B
ZERO (DETENT)
RANGE CURRENT SCALING
HYSTERESIS SWITCH
TRG/AST
WAVETEK
SCHEMATIC
GENERATOR BOARD
DO NOT SCALE DWG

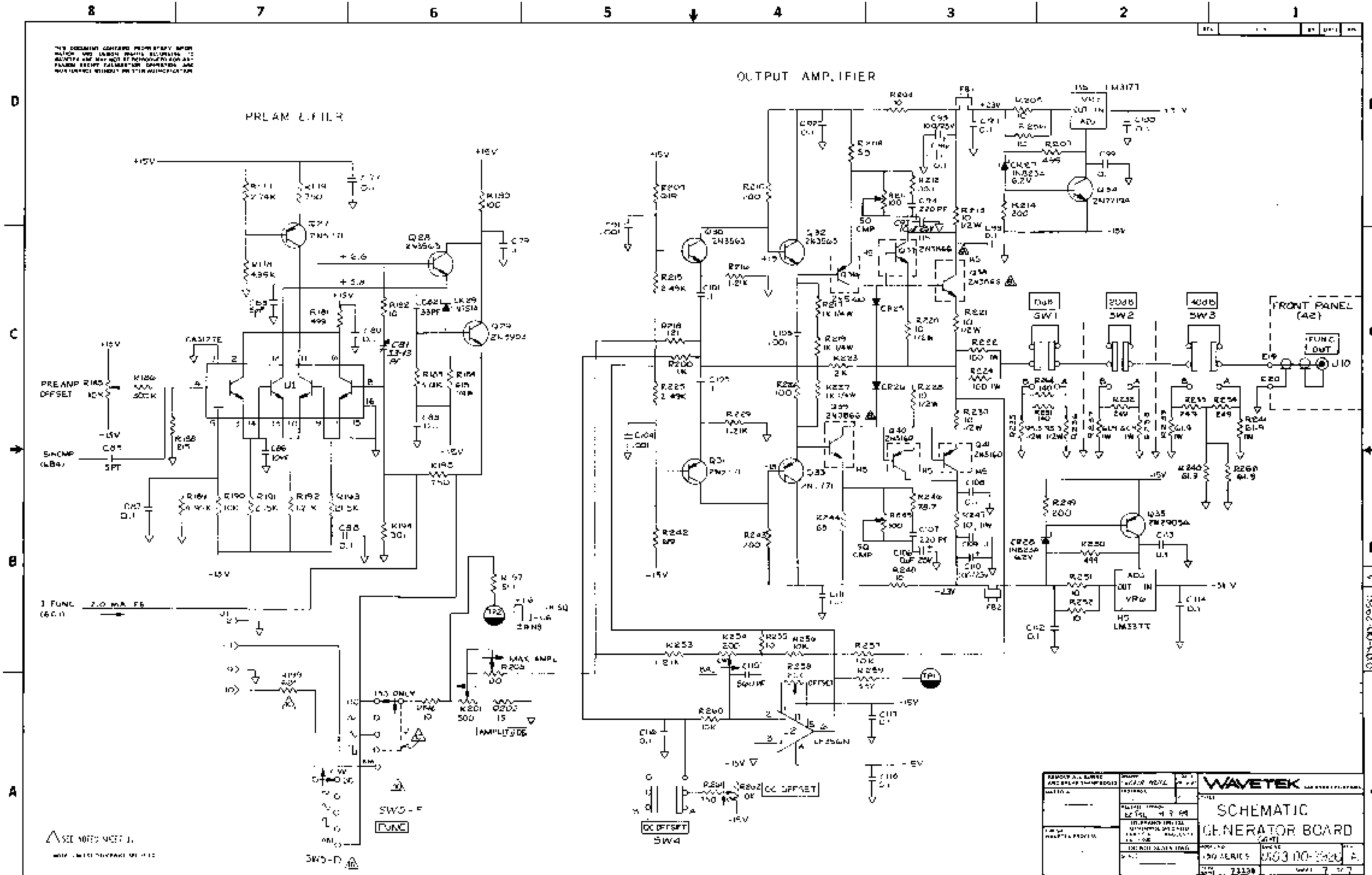


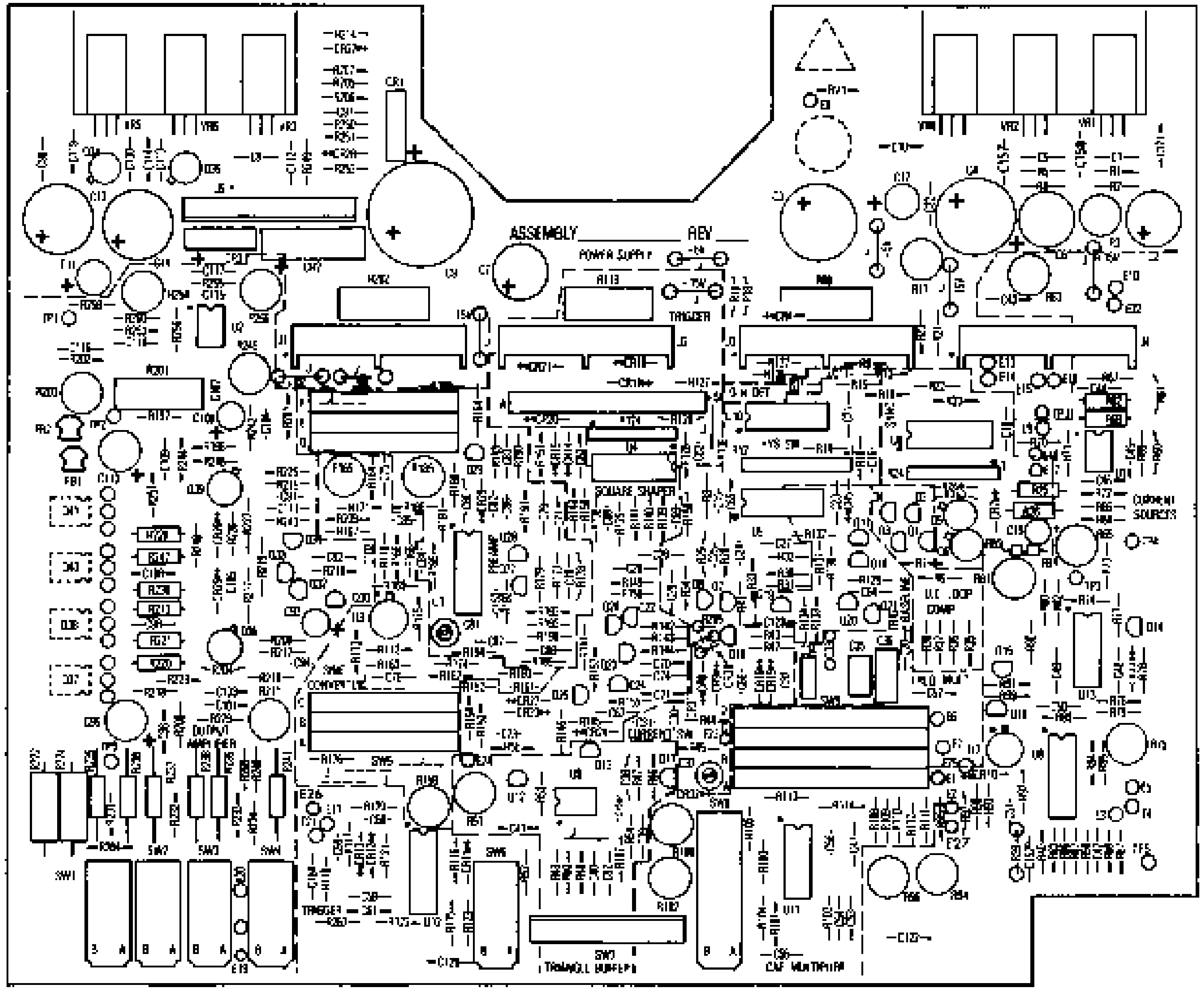
CURRENT SWITCH
FREQUENCY MULTIPLIER
TRIANGLE BUFFER
2N3646
R41
499
R42
R44
R43
+15V
-15V
+5V
CR36
CR37
CR39
HP2811
C40
10PF
ISWCMP
CAP MULT
SW9-D
FREQ MULT
C32
C33
C34
C35
C37
Q11
2N5486
R45
R46
R47
C38
C39
0.1
R54
R53
R55
1K
2N3563
Q13
Q12
R50
R51
R48
R49
C41
TL080
U9
TRIBUFC
SCHEMATIC
GENERATOR BOARD
WAVETEK


CURRENT SOURCES
FRONT PANEL (A2)
FREQ
VCG IN
FRONT PANEL (A2) MODEL 193 ONLY
GCV OUT
U14
1/2 LF353
U13
1/2 TL082
U15
1/2 TL082
U7
U8
CA 3083
SW8
VERN/SYM
SYM
VERN
TO A CONN 192 AUX BD
NOTE: IF 139-U7 DOES NOT HAVE PIN 4
SEE NOTES SHEET 1
WAVETEK
SCHEMATIC
GENERATOR BOARD
190 SERIES
0103-00-2326
A


CAPACITANCE MULTIPLIER
CAP MULT FREQ
FREQ MULT
SW9-A
1/2 TL083
CAP MULT ZERO
CAP MULT
TRIGGER
TRIG BASELINE
MAN TRIG
(A2) FRONT PANEL
MODE
ALWAYS LOAD
GATE OUT
GATE IN
TRIG RST
WAVETEK
SCHEMATIC
GENERATOR BOARD (A2)
190 SERIES
0103-00-2926


SQUARE SHAPER
SINE CONVERTER
WAVETEK
SCHEMATIC
GENERATOR BOARD
0103-00-2926


OUTPUT AMPLIFIER
PREAMPLIFIER
FRONT PANEL (42)
FUNC OUT
J10
SW1
SW2
SW3
SW4
DC OFFSET
SW5-E
FUNC
SW5-D
MAX AMPL
AMPLITUDE
PREAMP OFFSET
LF356N
LM317T
LM337T
2N3866
2N5160
2N2905A
U1
CA3127E
SEE NOTES SHEET 1
WAVETEK
SCHEMATIC
GENERATOR BOARD
0103-00-2926



MADE FROM 0100-00-0834-3H

WAVETEK

GENERATOR BOARD

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THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY PURPOSE EXCEPT CALIBRATION OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG MFGR PART NO	MFGR	WAVETEK NO	QTY/PT
NONE	ASSY, ?, GENERATOR	0101-00-0960	WVTK	0101-00-0960	1
NONE	ASSY, SHIELDED, GEN	193-0960	WVTK	1100-00-0960	1
NONE	SPL ASSY, [illegible] BRACKET	190-0996	WVTK	7206-00-0996	1
NONE	SPL ASSY, GUARD [illegible]	190-1094	WVTK	1206-00-1094	1
C153 C167 C85	CAP, CER, 3PF, 1KV	DD-030	CRL	1500-00-3011	3
C156 C20 C70 C??	CAP, CER, 10PF, 1KV	DD-100	CRL	1500-01-0011	4
C??	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	1
C108 C109 C91	CAP, CER, .001MF, 1KV	DD-102	CRL	1500-01-?011	3
C1 C10 C100 C101 C103 C109 ... [illegible]	CAP, CER, MON, .1MF, 50V	[illegible]	CORNG	1500-01-0405	70
C1051	CAP, CER, 150PF, 1KV	DD-151	CRL	1500-01-5111	1

WAVETEK PARTS LIST — TITLE: PCA, GENERATOR — ASSEMBLY NO: 1100-00-0960 — REV: H — PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG MFGR PART NO	MFGR	WAVETEK NO.	QTY/PT
C94	CAP, CER, 3.3PF, 1KV	10TCC-V33	MPEAC	1500-01-3397	1
C17	CAP, CER, 20PF, 1KV	DD-220	CRL	1500-02-2011	1
C107 C98	CAP, CER, 220PF, 1KV	DD 221	CRL	1500-02-2111	2
C16 C24 C25 C40 C48 C49	CAP, CER, 30PF, 1KV	DD-300	CRL	1500-03-0011	6
C45 C33 C44 C82	CAP, CER, 30PF, 1KV	DD-300	CRL	1500-03-3011	4
C96	CAP, CER, .005MF 50V	CF 502	CRL	1500-05-0210	1
C115	CAP, CER, 560PF, 1KV	DD 561	CRL	1500-05-6101	1
C25	CAP, MICA, 100PF 500V	DM15-101J	ARCO	1500-11-0100	1
C??	CAP, MICA, 7.5PF, 500V	DM15-7R5J	ARCO	1500 15 0000	1
C??	CAP, MICA, 5.6PF, 500V	CD15FC5R6FO3	CDE	1500-15-6102	1
C104 C19 C93	CAP, ELECT, 10MF/25V RADIAL LEAD, MF 10	CPE SERIES 10/25	CAPAR	1500-21-0004	3
C?? C110 C12 C2 C6 C95	CAP, ELECT, 100MF, 25V RADIAL LEAD, MF 30	ULB5V101M	NICH	1500-21-0102	6
C13 C18 C3 C4	CAP, ELECT, 1000MF/50V RADIAL LEAD, MF 50	CPE SERIES 1000/50	CAPAR	1500-31-0203	4
C7	CAP, ELECT, 2200MF 16V RADIAL LEAD, MF 30	CPE SERIES 2200/16	CAPAR	1500 32 2201	1
C8	CAP, ELECT, 4800MF, 16V	CPE SERIES 4800/16	CAPAR	1500 36 4801	1

WAVETEK PARTS LIST — TITLE: PCA, GENERATOR — ASSEMBLY NO: 1100-00-0960 — REV: H — PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG MFGR PART NO	MFGR	WAVETEK NO	QTY/PT
	RADIAL LEAD, SP .50				
C55	CAP, MYLAR, 1MF, 100V	[illegible]	MPEAC	1500-41-0444	1
C34	CAP, MYLR .0047MF, 50V	C5E472F	ELPAC	1500-44-7200	1
C35	CAP, MYLR .047MF, 50V	C5E473F	ELPAC	1500 44 7300	1
C36 C37	CAP, MYLR .47MF, 50V	C5E474F	ELPAC	1500-44-7400	2
C57 C81	VARI, 1.5-10PF, 250V	[illegible]	TRIKO	1500-51-5000	2
NONE	GENERATOR BOARD	190-0834	WVTK	1700-00-0834	1
U5	HEADER	1-640388-0	AMP	2100 02 6079	1
J1 J4	CONN, BOTTOM ENTRY, PC	09-52-3102	MOLEX	2100-02-0128	2
NONE	SOCKET, PIN	MS-430-25	ROBAU	2100-03-0044	8
NONE	TERM	20X08L	UBOCO	2100-05-0009	20
TP1 TP2 TP3 TP4 TP5 TP6 TP7	BUSS BAR STANDOFF	31-D-001	NATAH	2100-05-0004	7
U	STANDOFF, SWAGE .187L .250DIA, 4-40, NYLON	[illegible]-0 187-??	LYNTR	2600-06-0018	6
NONE	TRANSIPAD	10:378	NATRN	2600-11-0003	2
NONE	TRANSIPAD	10140	METRS	2600-11-0004	2
NONE	HEATSINK	900	WAKE	2800 11 0008	2

WAVETEK PARTS LIST — TITLE: PCA, GENERATOR — ASSEMBLY NO: 1100-00-0960 — REV: H — PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG MFGR PART NO	MFGR	WAVETEK NO.	QTY/PT
FB3 FB4	FERRITE BEAD	56-590-65/3B	FERXC	3100-00-0001	2
FB1 FB2	BALUN CORE	2873000202	FAIRIT	3100-00-0002	2
R17 R200 R221 R245 R96	POT, TRIM, 10K	91AR10K	BECK	4600-01-0303	5
R106 R185 R94	POT, TRIM, 1KA	91AR1KA	BECK	4600-01-0313	3
R143 R41 R92	POT, TRIM, 100K	91AR100K	BECK	4600-01-0402	3
R159 R254 R3	POT, TRIM, 200	91AR200	BECK	4600 02 0202	3
R102	POT, TRIM, 2K	91AR2K	BECK	4600-02-0302	1
R208 R51	POT, TRIM, 20K	91AR20K	BECK	4600-02-0301	2
R81	POT, TRIM, 500	91AR500	BECK	4600-05-0104	1
R201	POT, CONT, 500 FROM 4600-05-0105	4609-75-5106	WVTK	4609-75-5106	1
R213 R220 R221 R120 R230 R247	RES C, 1/2W, 5%, 10	RC 1/2 100J	STKPL	4700 25 0100	6
R48	RES C, 1/2W, 5%, 2.7M	RC 1/2 275J	STKPL	4700 25 2704	5
R42	RES C, 1/2W, 5%, 3.9M	RC 1/2-395J	STKPL	4700 25 3904	1
R103 R138 R127 R144 R167 R164 R171 R172 R174 R180 R236 R38 R39 R44 R45	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	15
R50 R121 R125 R130 R133	RES, MF, 1/8W, 1%, 1K	RN55D 1001F	TRW	4701 03 1001	24

WAVETEK PARTS LIST — TITLE: PCA, GENERATOR — ASSEMBLY NO: 1100-00-0960 — REV: H — PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG MFGR PART NO	MFGR	WAVETEK NO	QTY/PT
R124 R15 R145 R13 R250 R25 R46 R49 R53 R6 R74 R82 R83 R84 R85 R86 R87 R93 R97					
R151 R190 R256 R257 R260 R36 R42 R49	RES, MF 1/8W 1%, 10K	RN55D-1002F	TRW	4701-03-1002	8
R310	RES, MF 1/8W 1%, 100K	RN55D-1003F	TRW	4701-03-1003	1
R211 R227 R44	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	3
R104 R113 R142 R183 R196 R204 R205 R206 R240 R251 R252 R235 R43 R54 R55	RES, MF, 1/8W, 1%, 10	RN55D-10R0F	TRW	4701 03 100?	15
R33	RES, MF, 1/8W, 1%, 1.1K	RN55D-1101F	TRW	4701-03-1101	1
R1 R140 R216 R5	RES, MF, 1/8W, 1%, 121	RN55D-1210F	TRW	4701 03 1210	4
R16 R193 R2 R214 R229 R253 R4	RES, MF, 1/8W, 1%, 1.21K	RN55D 1211F	TRW	4701-03-1211	7
R177 R175	RES, MF, 1/8W, 1%, 12.1K	RN55D 1212F	TRW	4701-03-1212	2
R163 R31	RES, MF, 1/8W, 1%, 124	RN55D-1240F	TRW	4701-03-1240	2
R??	RES, MF, 1/8W, 1%, 12.4K	RN55D-1242F	TRW	4701-03-1242	1
R231 R268	RES, MF, 1/8W, 1%, 140	RN55D-1400F	TRW	4701-03-1400	2
R192	RES, MF, 1/8W, 1%, 150	RN55D-1500F	TRW	4701-03-1500	1
R114 R317	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	2

WAVETEK PARTS LIST — TITLE: PCA, GENERATOR — ASSEMBLY NO: 1100-00-0960 — REV: H — PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG MFGR PART NO	MFGR	WAVETEK NO	QTY/PT
R158 R173	RES, MF, 1/8W, 1%, 15K	RN55D 1502F	TRW	4701-03-1502	2
R202 R34	RES, MF, 1/8W, 1%, 15	RN55D-15R0F	TRW	4701-03-1509	2
R150	RES, MF, 1/8W, 1%, 1.62K	RN55D-1621F	TRW	4701-03-1621	1
R247	RES, MF, 1/8W, 1%, 165	RN55D-1650F	TRW	4701-03-1650	1
R8	RES, MF, 1/8W, 1%, 182	RN55D-1820F	TRW	4701-03-1820	1
R617	RES, MF, 1/8W, 1%, 19.6K	RN55D-1962F	TRW	4701-03-1962	1
R142 R244 R146 R138 R238 R214 R243 R249 R30 R32 R73	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	11
R232 R257 R40	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	3
R??	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701 03 2002	1
R100	RES, MF, 1/8W, 1%, 215	RN55D-2150F	TRW	4701-03-2150	1
R141 R293	RES, MF, 1/8W, 1%, 21.5K	RN55D-2152F	TRW	4701-03-2152	2
R136 R333	RES, MF, 1/8W, 1%, 221	RN55D-2210F	TRW	4701-03-2210	2
R15 R??	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701 03 2211	2
R???	RES, MF, 1/8W, 1%, 2.37K	RN55D-2371F	TRW	4701-03-2371	1
R18	RES, MF, 1/8W, 1%, 240	RN55D-2400F	MEPCO	4701-03-2400	1
R?? R?? R??? R??? R265	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	5

WAVETEK PARTS LIST — TITLE: PCA, GENERATOR — ASSEMBLY NO: 1100-00-0960 — REV: H — PAGE 6

WAVETEK

PARTS LIST
PCA, GENERATOR

103 | 1100-00-0960 | V

23238 | SHEET 1 OF 2

8	7	6	5	4	3	2	1

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R147 R132 R117 R[illegible] R46 R78 R91	RES, MF, 1/8W, 1%, 2.49K	RN55D 2491F	TRW	4701-03-2491	7
R107	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	1
R177	RES, MF, 1/8W, 1%, 2.74K	RN55D-2741F	TRW	4701-03-2741	1
R160	RES, MF, 1/8W, 1%, 27.4	RN55D-27R4F	TRW	4701-03-2749	1
R194	RES, MF, 1/8W, 1%, 301	RN55D-3010F	TRW	4701-03-3010	1
R118 R183 R54 R50 R7 R79 R44 R57	RES, MF, 1/8W, 1%, 3.01K	RN55D 3011F	TRW	4701-03-3011	8
R186	RES, MF, 1/8W, 1%, 301K	RN55D 3013F	TRW	4701-03-3013	1
R212	RES, MF, 1/8W, 1%, 30.1	RN55D-30R1F	TRW	4701 03 3009	1
R259	RES, MF, 1/8W, 1%, 33.2	RN55D-[illegible]	TRW	4701-03-[illegible]	1
R39	RES, MF, 1/8W, 1%, [illegible]	[illegible]	TRW	4701-03-[illegible]	1
R88	RES, MF, 1/8W, 1%, 33.2K	RN55D 3322F	TRW	4701-03-3322	1
R77 R90	RES, MF, 1/8W, 1%, 3.48K	RN55D-3481F	TRW	4701 03-3481	2
R108 R149	RES, MF, 1/8W, 1%, [illegible]	RN55D-[illegible]	TRW	4701-03-[illegible]	2
R176 R62	RES, MF, 1/8W, 1%, 464	RN55D-4640F	TRW	4701-03-4640	2
R131 R151 R20	RES, MF, 1/8W, 1%, 4.64K	RN55D 4641F	TRW	4701-03-4641	3

WAVETEK PARTS LIST — TITLE: PCA, GENERATOR — ASSEMBLY NO: 1100-00-0960 — REV: M — PAGE 7

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R101	RES, MF, 1/8W, 1%, 909	RN55D-9090F	TRW	4701-03-9090	1
R100	RES, MF, 1/8W, 1%, 9.09K	RN55D-9091F	TRW	4701-03-9091	1
R154	RES, MF, 1/8W, 1%, 90.9	RN55D-90R9F	TRW	4701-03-9099	1
R201 R204 R207	RES, MF, 1/8W, 1%, 1M	RN55D1003F	TRW	4701-13-1001	3
R25 R26	RES, MF, 1/8W, 1%, 49.9	RN60D-49R9F	TRW	4701-13-49R9	2
R184	RES, MF, 1/8W, 1%, 619	RN60D-6190F	TRW	4701 13 6190	1
R231 R236	RES, MF, 1/2W, 1%, 95.3	RN65D-95R3F	TRW	4701-23-9539	2
R222 R224	RES, MF, 1W, 1%, 100	RN70D 1000F	TRW	4701-33-1000	2
R242 R248 R249 R243	RES, MF, 1W, 1%, 61.9	RN70D-61R9F	TRW	4701-33-61R9	4
R12	RES MODULE	4116R-103-471	BOURN	4770-00-0009	1
R124 R24	RES MODULE	4308R-101-681	BOURN	4770-00-0031	2
R112	RES, MF, 1/4W, 1%, 10M	ML 10L	CADDO	4799-00-0003	1
RV1	VARISTOR	4899-00-0045	W-TK	4799 00-0045	1
CR29	DIODE	1N751A	FAIR	4803-03-0751	1
CR27 CR28	DIODE, ZENER 6.2V	1N821A	MOT	4803-03-0823	2
CR32 CR33	DIODE	1N5[illegible]	GISM	4803-03-0[illegible]	2
CR7	DIODE	1N5282	FAIR	4803 05-5282	1

WAVETEK PARTS LIST — TITLE: PCA, GENERATOR — ASSEMBLY NO: 1100-00-0960 — REV: M — PAGE 9

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
Q36 Q40 Q41	TRANS	2N5160 18	MOT	4901-05 1600	3
Q31	TRANS	2N5[illegible]	MOT	4901-05-[illegible]	1
Q1 Q2 Q34 Q27 Q21 Q33	TRANS	2N5771	NSC	4901-05-7710	6
U7	TRANS	IT 139	INTSL	4902-00 1390	1
Q37 Q38 Q39	TRANS, MULT, CHIP, QTY 1 4701 03-0440	4498-00-0001	W-TK	4498-00-0001	3
SW4 SW5 SW6 SW8	SWITCH	5102-05-00UP	W-TK	5102-05-0007	4
[illegible]	SWITCH, SPST, MOM	5102-00-0010	W-TK	5102-00-0010	1
SW9	SWITCH, SPDT, P-P	5102-00-0011	W-TK	5102 00 0011	1
NONE	BUTTON, CONICAL	FOS-C1-BLACK	[illegible]	5103-04-0001	4
RT1	THERMISTOR	135-[illegible]	FENWL	5300-00-0001	1
U8	IC, OP-AMP	TL082CP	TI	7900-00-8008	1
U11 U12	IC	TL080CN	TI	7900 00 8300	2
U14	IC	LF353N	NSC	7900-00-3530	1
U5	IC, OP-AMP	LF356N	NSC	7900-00-3560	1
U3	IC	CA-3019	RCA	7900-00-1906	1
U6	IC	CA3080	FAIR	7900 00 8300	1

WAVETEK PARTS LIST — TITLE: PCA, GENERATOR — ASSEMBLY NO: 1100-00-0960 — REV: M — PAGE 11

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R41 R47	RES, MF, 1/8W, 1%, 46.4	RN55D-46R4F	TRW	4701-03-4649	2
R120 R129 R188 R181 R207 R208 R98	RES, MF, 1/8W, 1%, 499	RN55D 4990F	TRW	4701-03-4990	7
R190 R106 R173 R187 R71 R72	RES, MF, 1/8W, 1%, 4.99K	RN55D 4991F	TRW	4701-03-4991	6
R144 R98	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701 03 4992	2
R128 R136 R197	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-51R9	3
R90	RES, MF, 1/8W, 1%, 523	RN55D-5230F	TRW	4701-03-5230	1
R206 R214	RES, MF, 1/8W, 1%, 59	RN55D-59R0F	TRW	4701-03-59R9	2
R75	RES, MF, 1/8W, 1%, 604	RN55D-6040F	TRW	4701 03 6040	1
R143 R404 R442	RES, MF, 1/8W, 1%, 619	RN55D-6190F	TRW	4701-03-6190	3
R210 R36A	RES, MF, 1/8W, 1%, 61.9	RN55D-61R9F	TRW	4701-03-6199	2
R135 R116 R122 R123 R192	RES, MF, 1/8W, 1%, 681	RN55D 6810F	TRW	4701-03-6810	5
R13	RES, MF, 1/8W, 1%, 6.81K	RN55D-6811F	TRW	4701-03-6811	1
R[illegible] R[illegible]	RES, MF, 1/8W, 1%, 68.1	RN55D-68R1F	TRW	4701 03 6819	2
R179 R158 R[illegible] R82 R43	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	5
R246 R47	RES, MF, 1/8W, 1%, 78.7	RN55D-78R7F	TRW	4701-03-7879	2
R4C	RES, MF, 1/8W, 1%, 8.25K	RN55D-8251F	TRW	4701-03-8251	1

WAVETEK PARTS LIST — TITLE: PCA, GENERATOR — ASSEMBLY NO: 1100-00-0960 — REV: M — PAGE 8

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
CR1 CR3	DIODE	1N4731	MOT	4803-03-0734	2
CR22 CR23 CR24	DIODE, ULTRA FAST	FE[illegible]	FAIR	4807-02-0777	3
CR30 CR31 CR18 CR19 CR14 CR16 CR20 CR25 CR26 CR4 CR5	DIODE	1N4148	FAIR	4807 02 4444	11
CR50 CR51 CR8 CR9	DIODE	5082-2811	HP	4809 03-2811	4
CR10 CR15	DIODE, MULT, 2-4807-777 QTY 2: 4807-02 0777	[illegible]	W-TK	4898-00-0003	1
U13	BRIDGE ASSY, 1.4 AMP	[illegible]	DIODE	4899-00 0037	1
Q18	TRANS	[illegible]	NSC	4901-03-2171	1
Q5 Q6	TRANS	2N2369A	MOT	4901-03-3691	2
Q35	TRANS	2N2905A	NSC	4901 03 9051	1
Q16 Q12 Q17 Q19 Q20 Q22 Q23 Q25 Q26 Q28 Q3 Q30 Q32 Q4 Q7 Q8	TRANS	2N3563	FAIR	4901-03-5630	16
Q10	TRANS	2N3640	NSC	4901-03-6400	1
Q29	TRANS	2N3903	NSC	4901 03 9030	1
Q14	TRANS	2N3904	FAIR	4901-03-9040	1
Q13 Q15 Q20 Q21	TRANS	2N3906	FAIR	4901-03-9060	4

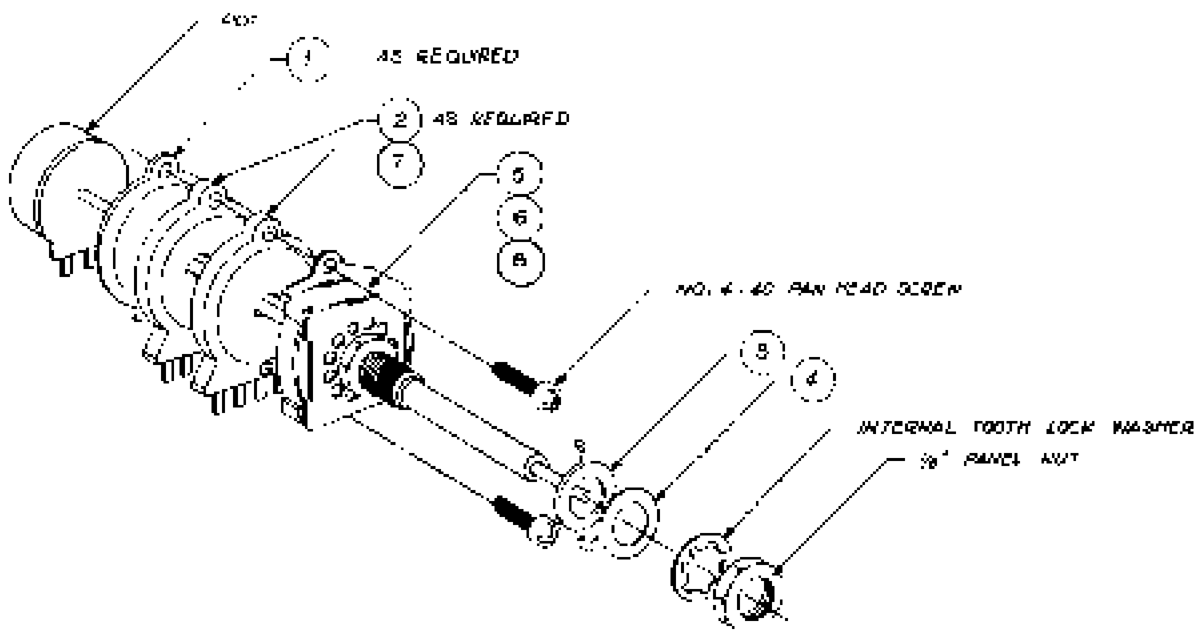
WAVETEK PARTS LIST — TITLE: PCA, GENERATOR — ASSEMBLY NO: 1100-00-0960 — REV: M — PAGE 10

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
U1	IC	CA3127E	RCA	7900 01-2700	1
U4 U9	ECL NOR, QUAD 2INP	MC10102	MOT	8601-01-0202	2
U10 U2	ECL NOR/NOR, TRI, 2INP	MC10105P	MOT	8601-01-1050	2
U1	ECL D-F/F, DUAL	MC10131	MOT	8601-01-3102	1

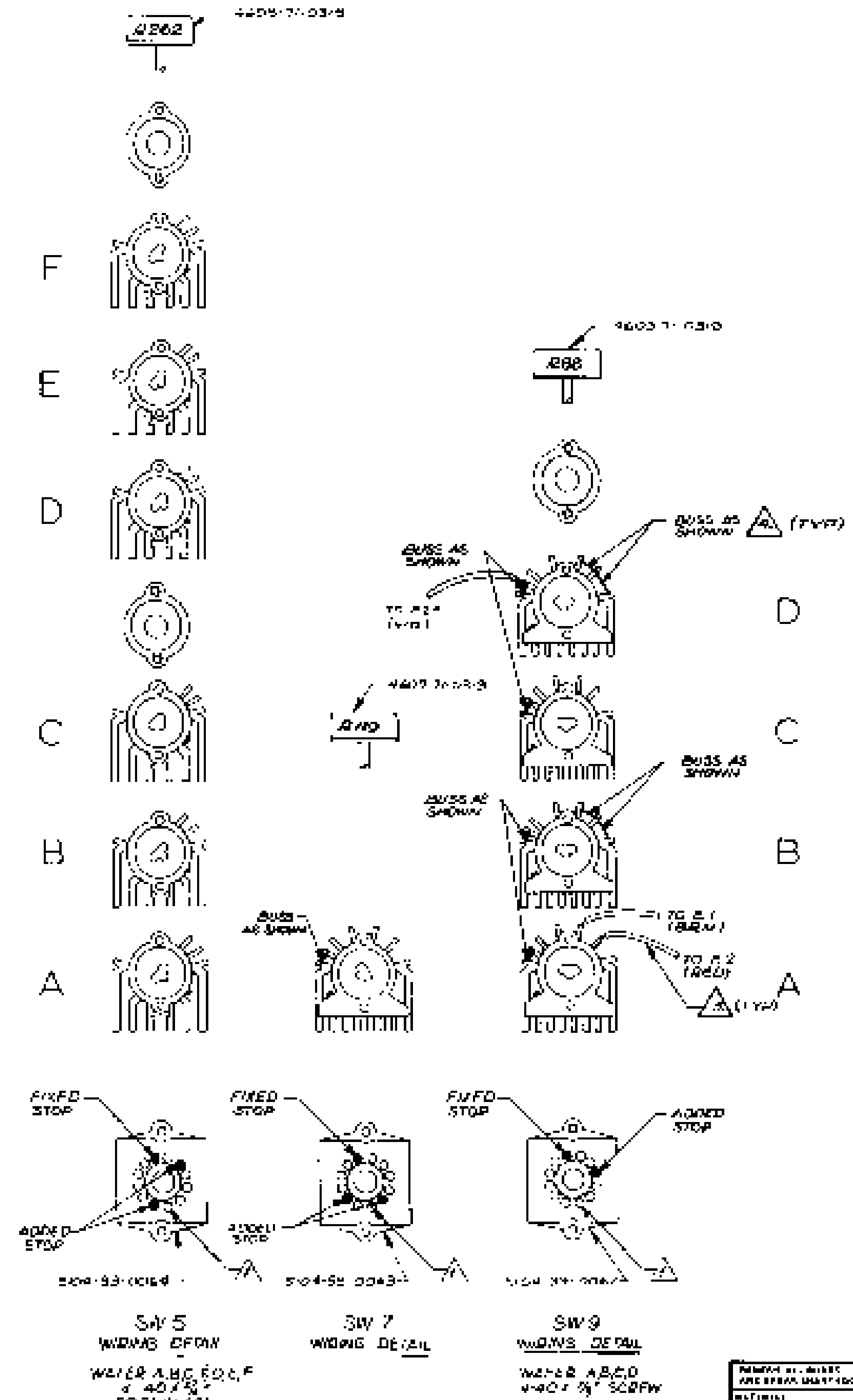
WAVETEK PARTS LIST — TITLE: PCA, GENERATOR — ASSEMBLY NO: 1100-00-0960 — REV: M — PAGE 12

WAVETEK — TITLE: PARTS LIST PCA, GENERATOR — MODEL: 193 — DWG NO: 1100-00-0960 — REV: M — CODE: 23338 — SHEET 2 OF 2

DO NOT SCALE DWG



TYPICAL SWITCH HARDWARE STACK-UP



ALL BUSS WIRE #24 AWG

WIRES OBTAINED FROM CHASSIS CABLE KIT

ALL WAFERS SHOWN IN CCW POSITION

PLACE DETENT & POSITIONS AS SHOWN FROM CCW FIXED STOP BEFORE INSTALLING ADDED STOP

WAVETEK	
TITLE	ASSEMBLY SWITCH DETENT GENERATOR BOARD
DRAWN	C.N. AQUINO
	DO NOT SCALE DWG
	193
	0?2-?0-0?63
	23338

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	ASSY DRWG, SWITCHES GENERATOR	0102-00-0963	WVTK	0102-00-0963	1
NONE	[illegible]	133 309	WVTK	1400-00-1473	1
1	PLATE SW	009-054	WVTK	1400-00-2130	3
R1,9 4262 R08	POT, CONT, LIN FROM 4500-01-0312	4609-71-0319	WVTK	4609 71-0319	5
2	WAFER	322-[illegible]-1	WVTK	5104-02-0008	[illegible]
7	WAFER	347-[illegible]	WVTK	5104-04-[illegible]	2
3	SWITCH STOP	211 33 001	CTB	5104-07-0001	1
4	SWITCH STOP	212-33-004	CTB	5104-07-0002	1
5	DETENT, MOD FROM 5104-01-0012	5104-99-0062	WVTK	5104-99-0062	1
6	DETENT, MOD FROM 5104-01-0012	5104-99-0063	WVTK	5104 99 0063	1
8	DETENT, MOD FROM 5104-01-0012	5104-99-0064	WVTK	5104-99 0064	1

WAVETEK PARTS LIST

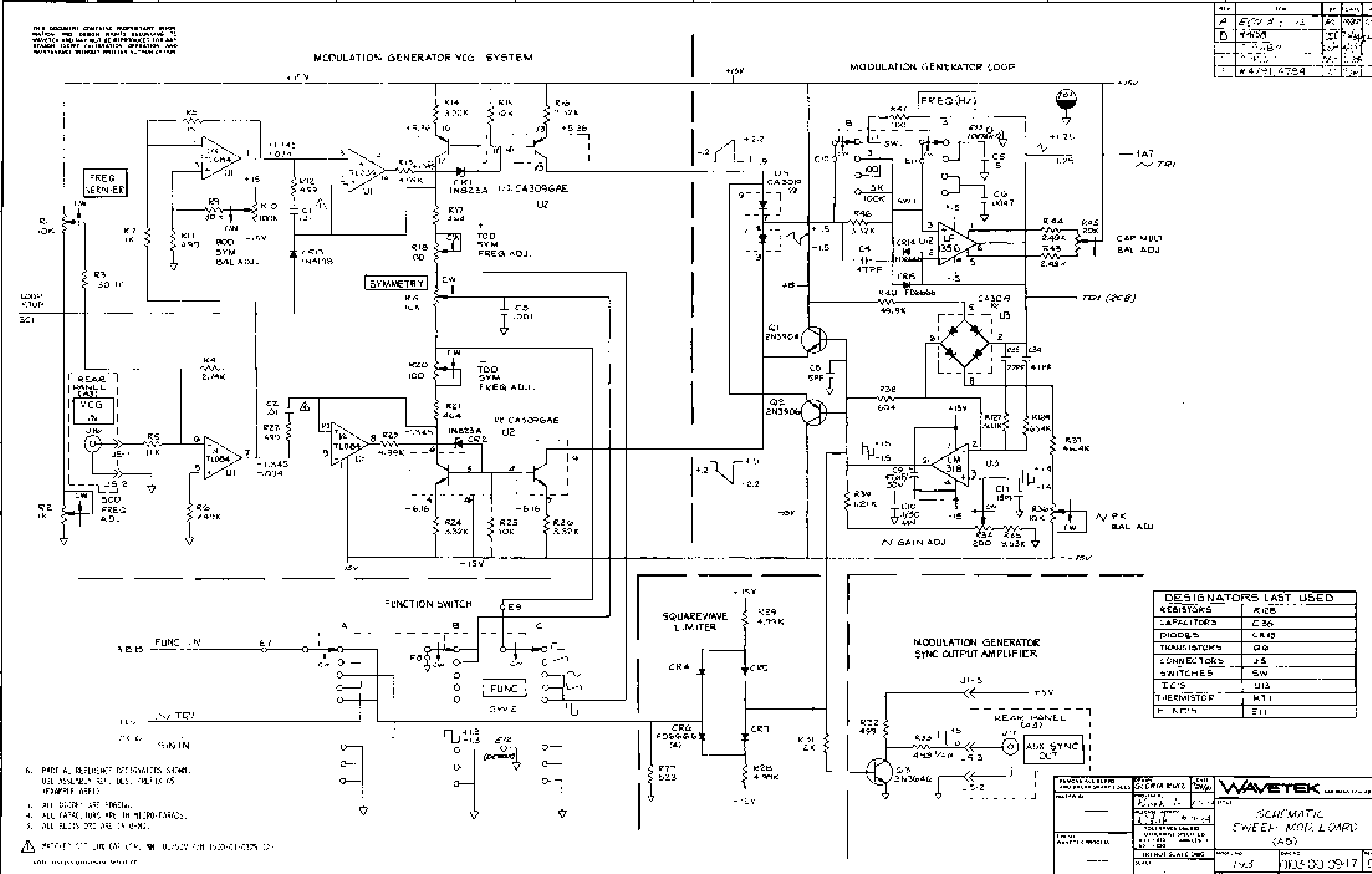
ASSY SWITCHES GEN

WAVETEK

PARTS LIST
ASSY, SWITCHES, GEN

193 | 1202-00-0963 | A

SHEET 1 OF 1



DESIGNATORS LAST USED	
RESISTORS	R128
CAPACITORS	C36
DIODES	CR15
TRANSISTORS	Q9
CONNECTORS	J5
SWITCHES	SW
IC'S	U13
THERMISTOR	RT1
E NOTES	E11

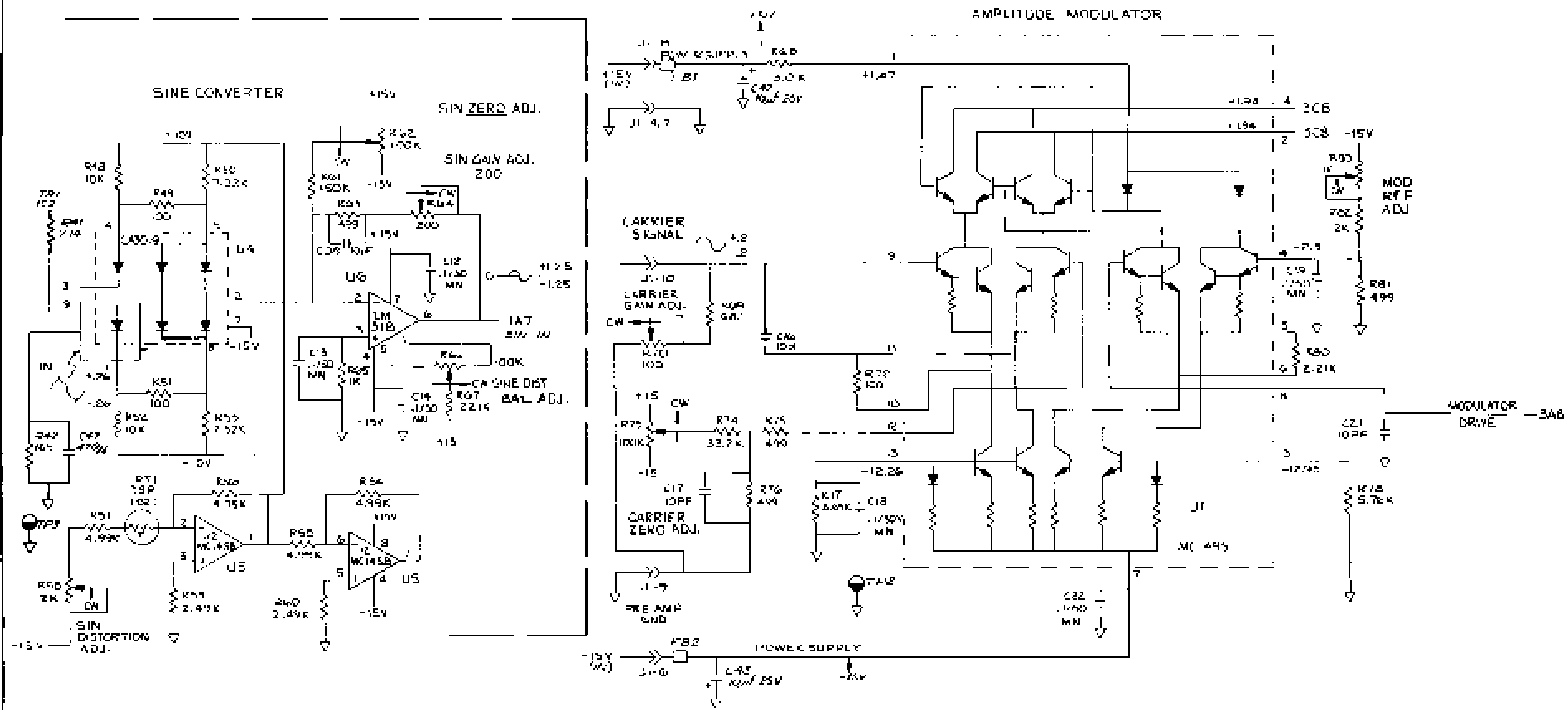
1. PARTIAL REFERENCE DESIGNATIONS SHOWN. USE ASSEMBLY REF. DES. PREFIX AS (EXAMPLE A5R1)
3. ALL DIODES ARE 1N914A.
4. ALL CAPACITORS ARE IN MICRO-FARADS.
5. ALL RESISTORS ARE IN OHMS.

WAVETEK

SCHEMATIC SWEEP MOD BOARD (A5)

0103-00-0947

SHEET 1 OF 3



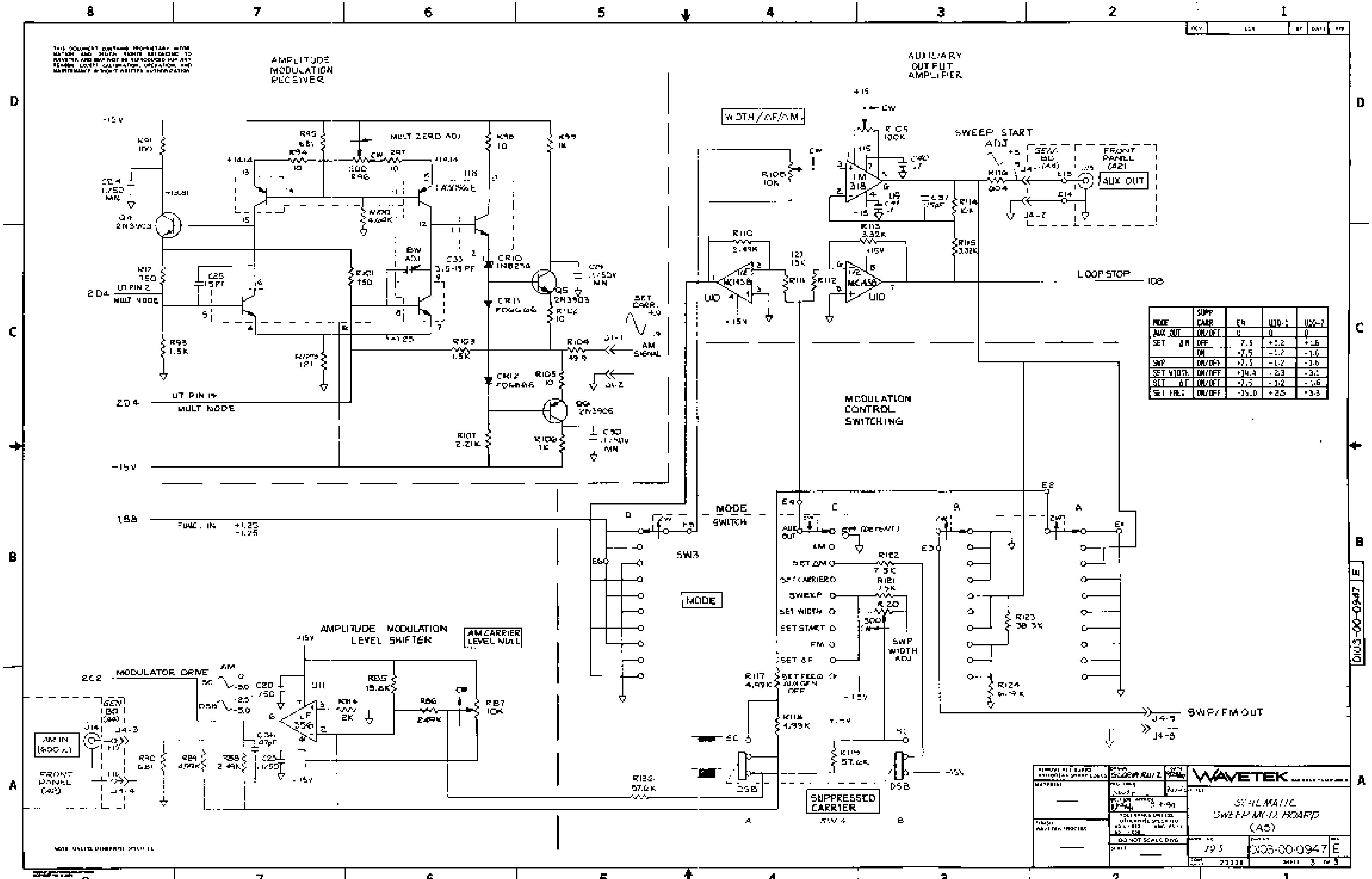
WAVETEK

SCHEMATIC
SWEEP MOD BOARD
(A5)

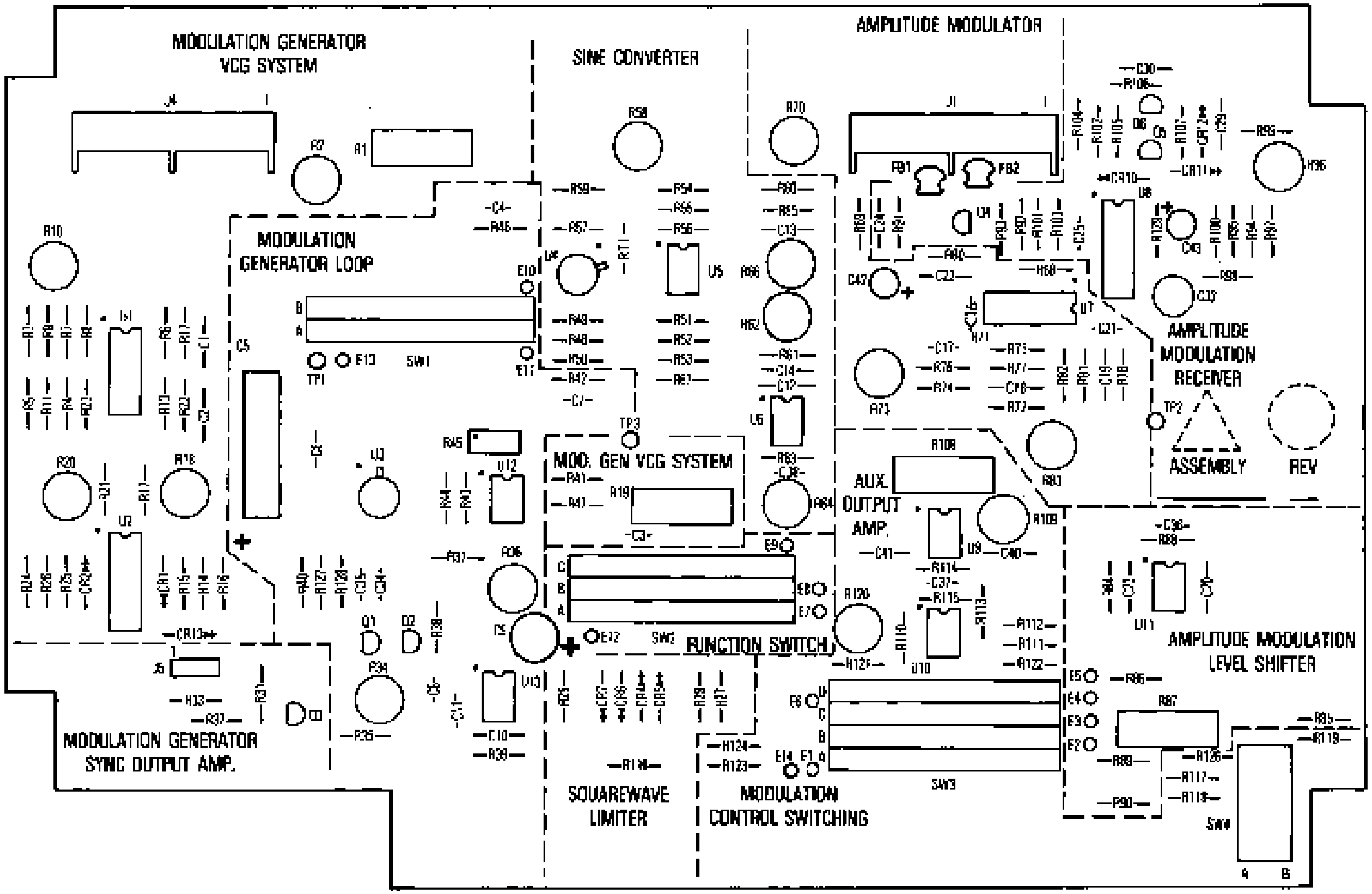
DO NOT SCALE DWG

SHEET 2 OF 3

0103-00-0947 E



MODE	SUPP CARR	E4	U10-1	U10-7
AUX OUT	ON/OFF	0	0	0
SET AM	OFF	7.5	+1.2	+1.6
	ON	+7.5	-1.7	-1.6
SWP	ON/OFF	+7.5	-1.2	-1.6
SET WIDTH	ON/OFF	+14.4	-2.3	-3.1
SET ΔF	ON/OFF	+7.5	-1.2	-1.6
SET FREQ	ON/OFF	-15.0	+2.5	+3.3



MADE FROM 0100-00-0947-3F

WAVETEK

SWEEP/MOD BOARD

193

1100-00-0047

F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG MFGR PART NO	MFGR	WAVETEK NO	QTY/PT
NONE	ASSY DRWG SWEEP/MOD	0101-00-0947	WVTK	0101-00-0947	1
NONE	SCHEMATIC SWEEP/MOD	0103-00-0947	WVTK	0103-00-0947	1
NONE	[illegible]	1401-0945	WVTK	1404-00-0945	1
NONE	SPR ASSY, SWITCH [illegible]	1400-0784	WVTK	1406-00-0784	2
NONE	ASSY, POT [illegible]	1400-0988	WVTK	[illegible]	1
C8	CAP,CER,5PF,1KV	DD 050	CRL	1500 00 5011	1
C16 C17 C21 C30	CAP,CER 10PF 1KV	DD-100	CRL	1500-01-0011	4
C3	CAP,CER, 100PF,1KV	DD-102	CRL	1500-01-0011	1
C1 C2	CAP,CER,MN, .01MF,50V	8050 10334	MURAT	1500-01-0310	2
C15 C12 C13 C14 C20 C19 C25 C23 C27 C24 C29 C31	CAP,CER MONO .1MF,50V	CAC02[illegible]050A	CORNG	1500-01-0405	12
C11 C37	CAP,CER 15PF 1KV	DD-150	CRL	1500 01 5011	2
C35	CAP,CER 1.5PF,1KV	[illegible]	[illegible]	1500-01-5507	1
C33	CAP,CER,22PF,1KV	DD-220	CRL	1500-02-2011	1
C34 C36 C4	CAP,CER,47PF,1KV	DD 470	CRL	1500-04-7011	3
C7	CAP,CER,470PF,1KV	DD-471	CRL	1500-04-7101	1
C41 C42	CAP,ELECT,10MF/35V	[illegible]	[illegible]	1500-31-0004	2

WAVETEK PARTS LIST — TITLE: PCA, SWEEP/MOD — ASSEMBLY NO 1100-00-0947 — REV 0 — PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R45	POT,TRIM,20T,20K	[illegible]	BECK	4607 00 0502	1
R47 R49 R51 R74 R91	RES,MF,1/8W,1%,100	RN55D-1000F	TRW	4701-03-1000	5
R104 R48 R7 R8 R99	RES,MF,1/8W,1% 1K	RN55D-1001F	TRW	4701-03-1001	5
R114 R15 R25 R46 R52	RES,MF 1/8W,1%,10K	RN55D-1002F	TRW	4701-03-1002	5
R102 R105 R94 R97 R98	RES,MF,1/8W,1% 10	RN55D-10R0F	TRW	4701-03-1009	5
R5	RES,MF,1/8W,1%,110	RN55D-1100F	TRW	4701-03-1101	1
R529	RES,MF,1/8W,1% 121	RN55D 1210F	TRW	4701-03-1210	1
R39	RES,MF,1/8W,1% 1.21K	RN55D-1211F	TRW	4701 03 1211	1
R103 R92	RES,MF,1/8W,1% 1.3K	RN55D-1301F	TRW	4701-03-1301	2
R113 R112	RES,MF,1/8W,1% 15K	RN55D-1502F	TRW	4701-03-1502	2
R53	RES,MF,1/8W 1% 150K	RN55D 1503F	TRW	4701-03-1503	1
R95	RES,MF,1/8W,1% 15.8K	RN55D-1582F	TRW	4701 03 1582	1
R44	RES,MF,1/8W,1% [illegible]	[illegible]	TRW	4701-03-[illegible]	1
R33 R87 R88	RES,MF,1/8W,1%,2K	RN55D-2001F	TRW	4701-03-2001	3
R107 R80	RES,MF,1/8W,1% 2.21K	RN55D 2211F	TRW	4701-03-2211	2
R67	RES,MF,1/8W,1% 22.1K	RN55D-2212F	TRW	4701-03-2212	1

WAVETEK PARTS LIST — TITLE: PCA, SWEEP/MOD — ASSEMBLY NO 1100-00-0947 — REV 0 — PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R117 R118 R17 R23 R26 R29 R34 R35 R37 R89	RES,MF,1/8W,1% 4.99K	RN55D 4991F	TRW	4701 03 4991	10
R40	RES MF,1/8W,1% 49.9K	RN55D-4992F	TRW	4701-03 4992	1
R27	RES,MF,1/8W,1% 523	RN55D-5230F	TRW	4701-03-5230	1
R78	RES,MF 1/8W,1% 5.76K	RN55D-5761F	TRW	4701-03-5761	1
R115 R126	RES,MF,1/8W,1% 57.6K	RN55D-5762F	TRW	4701 03 5762	2
R111 R38	RES,MF,1/8W,1% 604	RN55D-6040F	TRW	4701-03-6040	2
R125	RES,MF,1/8W,1% 6.19K	RN55D-6191F	TRW	4701-03-6191	1
R128	RES,MF,1/8W,1% 63.4K	RN55D-6342F	TRW	4701-03-6342	1
R70 R93	RES,MF,1/8W,1% 681	RN55D-6810F	TRW	4701-03-6810	2
R69	RES,MF,1/8W,1% [illegible]	[illegible]	TRW	4701-03-[illegible]	1
R30 R31	RES,MF,1/8W,1% 7.32K	RN55D-7321F	[illegible]	4701-03-7321	2
R101 R92	RES,MF,1/8W,1% 750	RN55D-7500F	TRW	4701-03-7500	2
R121 R122	RES,MF,1/8W,1% 7.5K	RN55D 7501F	TRW	4701 03-7501	2
R43	RES,MF,1/8W,1% 9.53K	RN55D-9531F	TRW	4701-03-9531	1
R104 R99	RES,MF,1/8W,1% [illegible]	[illegible]	TRW	[illegible]	2
CR1 CR10 CR2	DIODE,ZENER 6.2V	1N823A	MOT	4801-03 0823	3

WAVETEK PARTS LIST — TITLE: PCA, SWEEP/MOD — ASSEMBLY NO 1100-00-0947 — REV 0 — PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	RADIAL LEAD, MP 10				
C9	CAP,ELECT,47MF,50V RADIAL LEAD, MP 20	[illegible]	NICH	1500-24-7051	1
C6	CAP,POLY, [illegible]MF,50V	[illegible]	ELPAC	1500-44-7303	1
C5	CAP,POLYC,.5MF,100V	[illegible]	[illegible]	1500 45 0554	1
C22	VAR,C 3.5-13PF,250V	[illegible] 3.5/13PF	JOHNS	1500-51-3000	1
NONE	SWEEP/MOD BOARD	[illegible]-0947	WVTK	[illegible]-00-0947	1
J1 J4	CONN,BOTTOM ENTRY,PC	09-52-7102	MOLEX	2100-02-0129	2
J5	3 POS HEADER	22 10 2031	MOLEX	2100 03-0052	1
R18 R20 R73	POT,TRIM,100	91AR100	BECK	4600-01-0103	3
R9 R84	POT,TRIM,1K	91AR1K	BECK	4600-01-[illegible]	2
R36	POT,TRIM,10K	91AR10K	BECK	4600-01-0312	1
R10 R109 R42 R66 R72	POT,TRIM,100K	91AR100K	BECK	4600 01 0402	5
R19 R64 R65	POT,TRIM,200	91AR200	BECK	4600-02-0101	3
R58	POT,TRIM,2K	91AR2K	BECK	4600-02-0201	1
R120	POT,TRIM,500	91AR500	BECK	4600-05-0101	1
R82	POT CONT 10K FROM 4600-01-0312	[illegible]	WVTK	4609-71-0321	1

WAVETEK PARTS LIST — TITLE: PCA, SWEEP/MOD — ASSEMBLY NO 1100-00-0947 — REV 0 — PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG MFGR-PART NO	MFGR	WAVETEK NO.	QTY/PT
R130 R43 R44 R59 R6 R62 R68	RES,MF,1/8W,1% 2.49K	RN55D 2491F	TRW	4701-03-2491	7
R86	RES,MF,1/8W 24.9K	RN55D-2492F	TRW	4701-03-2492	1
R41	RES,MF,1/8W,1% 274	RN55D-2740F	TRW	4701-03-2740	1
R4	RES,MF,1/8W,1% 2.74K	RN55D-2741F	TRW	4701-03-2741	1
R68	RES,MF,1/8W,1% 3.01K	RN55D 3011F	TRW	4701-03-3011	1
R127 R3	RES,MF,1/8W,1% 30.1K	RN55D-3012F	TRW	4701-03-3012	2
R9	RES,MF,1/8W,1% 301K	RN55D-3013F	TRW	4701-03-3013	1
R110 R116 R11 R16 R24 R28 R48	RES,MF,1/8W,1% 3.32K	RN55D-3321F	TRW	4701-03-3321	7
R76	RES,MF,1/8W,1% [illegible]	[illegible]	TRW	4701-03-[illegible]	1
R77	RES,MF,1/8W,1% 3.65K	RN55D-3651F	TRW	4701-03-3651	1
R123	RES,MF,1/8W,1% 38.3K	RN55D-3832F	TRW	4701 03 3832	1
R17 R83	RES,MF,1/8W,1% 464	RN55D-4640F	TRW	4701-03-4640	2
R100	RES,MF,1/8W,1% 4.64K	RN55D-4641F	TRW	4701-03-4641	1
R77	RES,MF,1/8W,1% 46.4K	RN55D-4642F	TRW	4701-03-4642	1
R56	RES,MF,1/8W,1% 4.75K	RN55D-4751F	TRW	4701 03 4751	1
R1 R12 R32 R63 R75 R76 R81 R83	RES,MF,1/8W,1% 499	RN55D-4990F	TRW	4701-03-4990	8

WAVETEK PARTS LIST — TITLE: PCA, SWEEP/MOD — ASSEMBLY NO 1100-00-0947 — REV 0 — PAGE 5

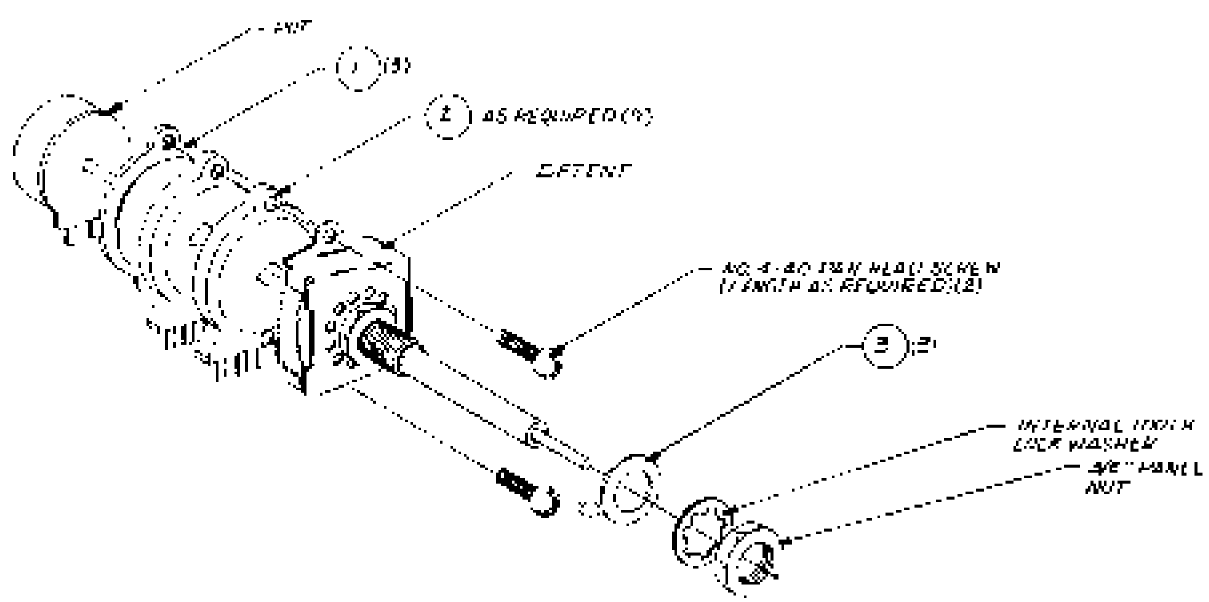
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR11 CR12 CR13 CR14 CR15 CR4 CR5 CR6 CR7	DIODE	1N4148	FAIR	4802-03-4148	9
Q3	TRANS	[illegible]	NSC	[illegible]	1
Q4 Q5	TRANS	[illegible]	NSC	[illegible]	2
Q1	TRANS	2N3904	FAIR	4901-03-9040	1
Q6	TRANS	2N3905	[illegible]	4903-03-9050	1
Q2	TRANS	2N3906	FAIR	4903-03-9060	1
SW4	SWITCH	[illegible]	WVTK	5103-00-0004	1
NONE	BUTTON,CONICAL	F03-01 BLACK	[illegible]	5103-04-0004	1
RT1	THERMISTOR	TSP102J	TI	[illegible]	1
U6	IC	TL084CN	TI	[illegible]	1
U10 U6 U9	IC	[illegible]	[illegible]	7000-03-1800	3
U11 U12	IC,OP AMP	LF356N	NSC	7000 03 5600	2
U10 U5	IC	MC1458P1	MOT	[illegible]	2
U7	IC	[illegible]	MOT	[illegible]	1
U3 U4	IC	CA-3019	RCA	7000-30-1900	2
U1 U8	IC	CA 3096AE	RCA	7000 30-9600	2

WAVETEK PARTS LIST — TITLE: PCA, SWEEP/MOD — ASSEMBLY NO 1100-00-0947 — REV 0 — PAGE 6

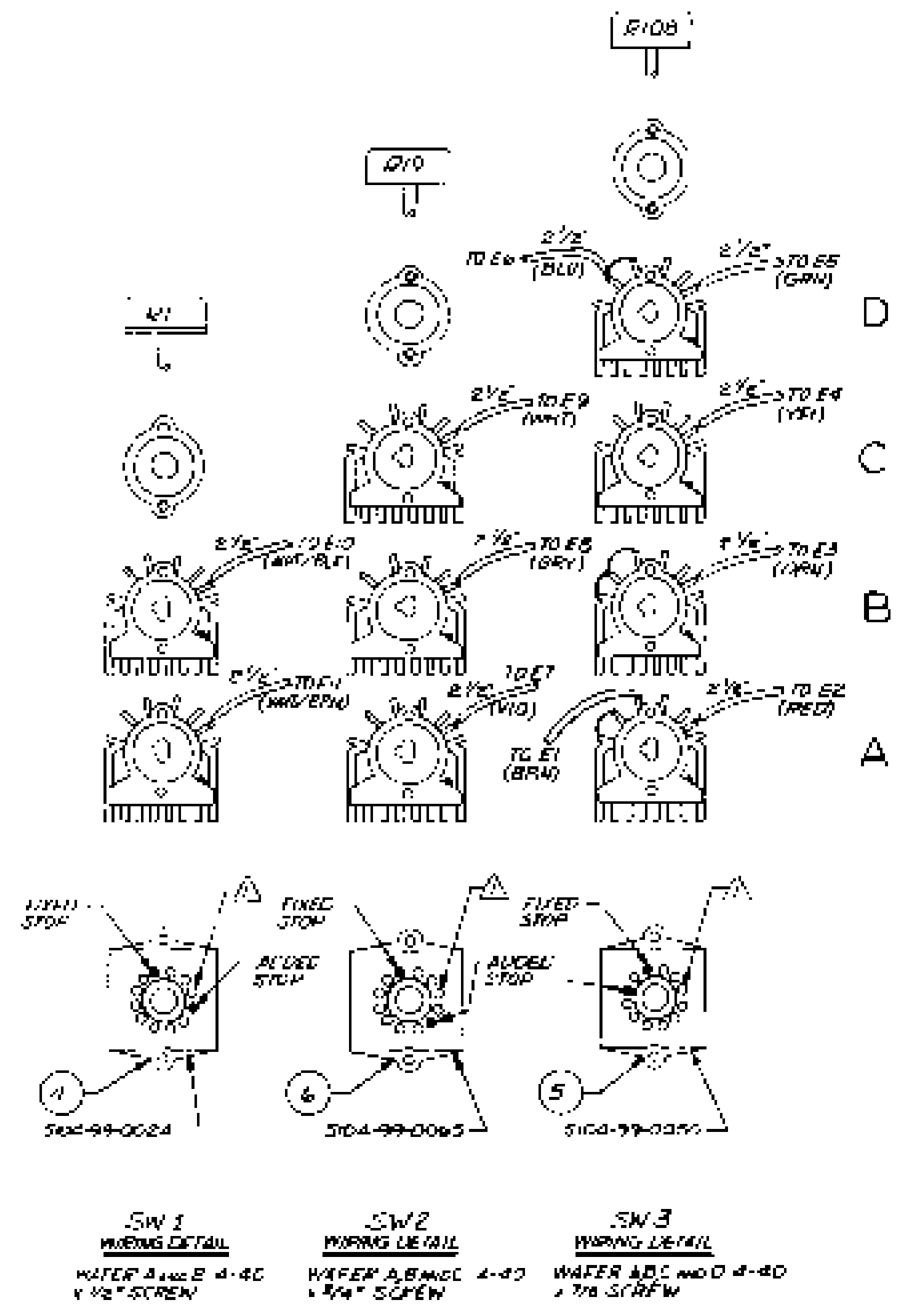
WAVETEK

PARTS LIST
PCA, SWEEP/MOD

193 | 1100-00-0947 | 0



TYPICAL SWITCH
HARDWARE STACK-UP



3. #24 AWG ... WIRE
2. ALL WAFERS SHOWN IN CCW POSITION.
1. ROTATE DETENT ... POSITIONS AS SHOWN BEFORE INSTALLING ADDED STOP

WAVETEK

ASSEMBLY
DETENT SWEEP BOARD

DO NOT SCALE DWG

193

0102-00-0965

REFERENCE DESIGNATOR	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/UNIT
NONE	ASSY DRWG. SWEEP/MOD SWITCHES	0102-00-0965	WVTK	0102-00-0965	1
1	PLATE, SW	[illegible]	WVTK	1400-00-2820	
[illegible]	POT, CONT. [illegible] FROM 4600-01-0312	4609-71-0307	WVTK	4609-71-0307	1
[illegible]	POT, CONT. [illegible] FROM 4600-01-0312	4609-71-0311	WVTK	4609-71-0311	1
[illegible]	POT, MOD FROM: 4600-01-0312	[illegible]	WVTK	4609-71-0317	1
2	WAFER	[illegible]	WVTK	[illegible]	[illegible]
3	SWITCH STOP	[illegible]	CTS	5104-07-0001	[illegible]
4	DETENT MOD FROM 5104-01-0010	[illegible]	WVTK	[illegible]	1
5	DETENT MOD FROM 5104-01-0010	5104-99-0050	WVTK	5104-99-0050	1
6	DETENT, MOD FROM 5104-01-0010	5104-99-0065	WVTK	5104-99-0065	1

WAVETEK PARTS LIST

TITLE: ASSY, SWITCHES SWEEP/MOD

1202-00-0965

WAVETEK

PARTS LIST
ASSY, SWITCHES SWEEP/MOD

DO NOT SCALE DWG

193 | 1202-00-0965

SHEET 1 OF 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG MFGR PART NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY, DRNG, REAR PANEL	0102-00-0962	WVTK	0102-00-0962	1
4	SPACER	[illegible]	WVTK	[illegible]	2
5	END BRKT	172-300-[illegible]	WVTK	1400-00-[illegible]	1
11	POST	100 302	WVTK	1400 00 5020	4
15	INSULATOR, PWR SWITCH REF 1600-[illegible]-0001	801-8370	WVTK	[illegible]	1
17	I.D. LABEL	801-9890	WVTK	[illegible]	1
3	BRACKET, SWITCH [illegible]	189-[illegible]	WVTK	1400-01-[illegible]	1
19	REAR PANEL	173-3870	WVTK	1400 01 3870	1
2	SHIELD, VOLTAGE	191-5190	WVTK	1400-01-5190	1
12	CONN BNC	[illegible]	[illegible]	2100-01-[illegible]	2
20	HOUSING	1-640433-0	AMP	2100-02-0080	1
16	HEADER, CONN 3 POS	640440-3	AMP	2100-02-0137	1
7	RECEPTACLE	[illegible]	CORCM	2100-03-0026	1
14	SOLDER LUG	1497	SMITH	2300-04-[illegible]	2
6	SOLDER LUG	11A14[illegible]	ZIER	2300-04-0026	3
8	FUSE, 3/4A, 250V, 3-B	313-750	LITFU	2400-05-0013	1

WAVETEK PARTS LIST

TITLE: ASSY, REAR PANEL

ASSEMBLY NO: 1101-00-0962

REV: B

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG MFGR PART NO	MFGR	WAVETEK NO	QTY/PT
10	WASHER, SHOULDER	2560	SMITH	2800-27-0004	4
3	SWITCH ASSY, PB	5100-00-0020	WVTK	5100-00-0003	1
11	TRANSFORMER	2400-00-0011	COIL	6400-00-0031	1

WAVETEK PARTS LIST

TITLE: ASSY, REAR PANEL

ASSEMBLY NO: 1101-00-0962

REV: B

PAGE 2

WAVETEK

TITLE: PARTS LIST ASSY, REAR PANEL

MODEL NO: 195

DRAWING NO: 1101-00-0962

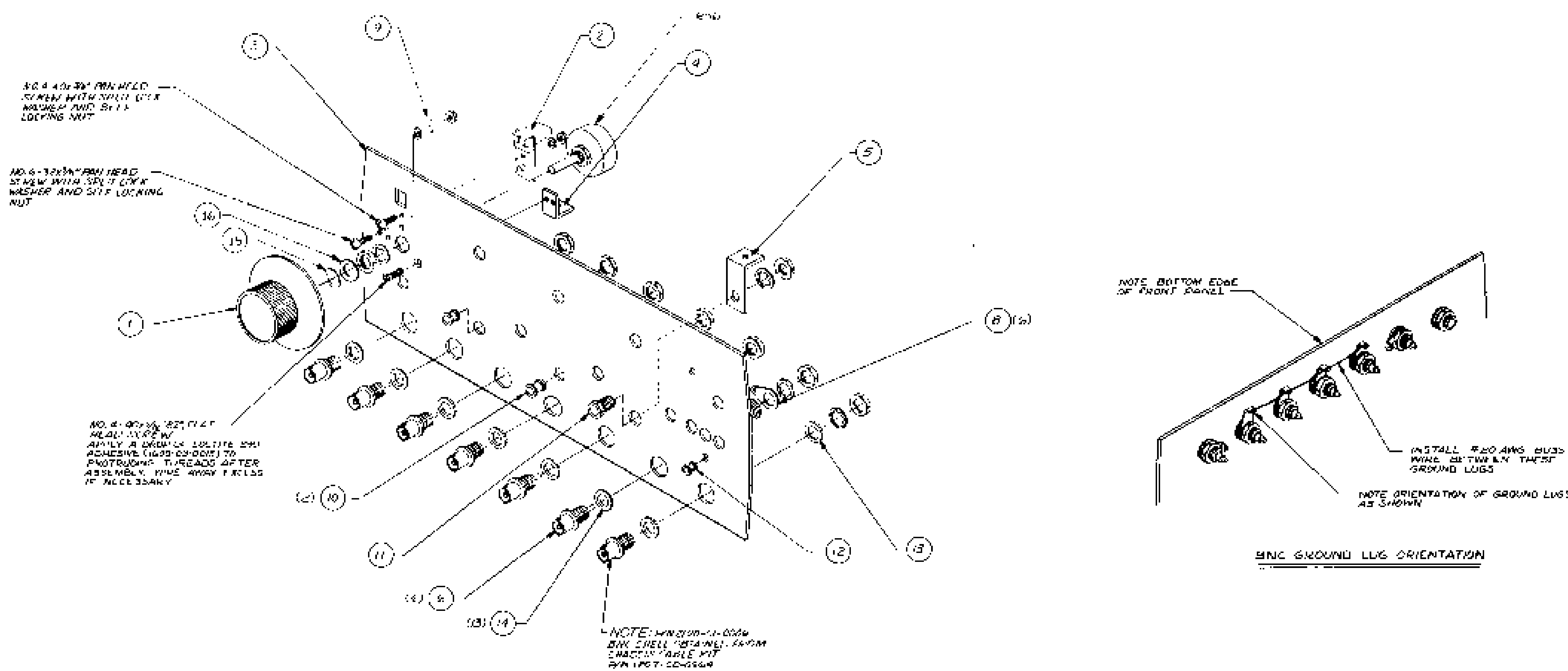
REV: B

CODE IDENT: 23338

SHEET 1 OF 1

DO NOT SCALE DWG

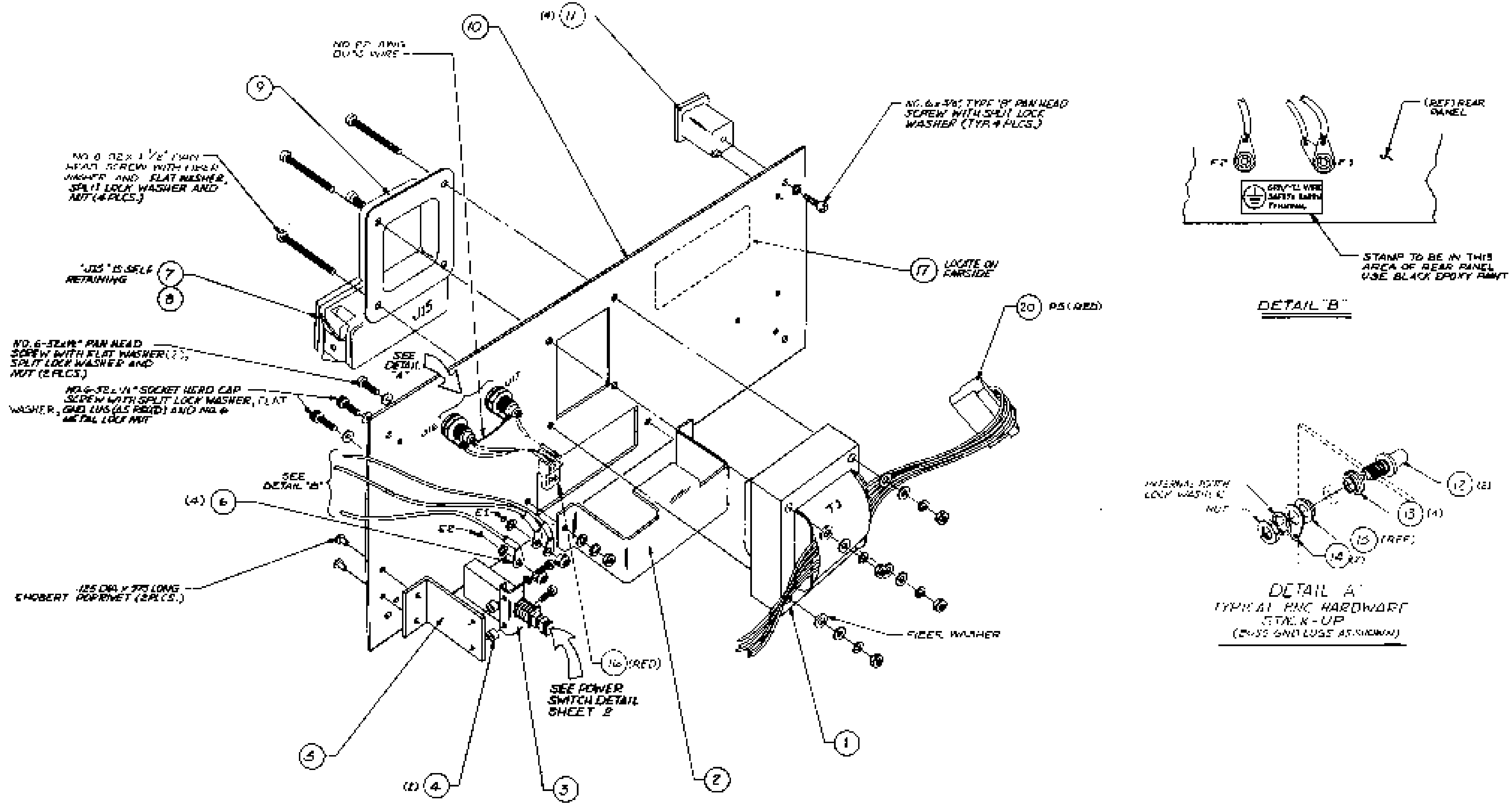
NOTE: UNLESS OTHERWISE SPECIFIED



WAVETEK

ASSEMBLY FRONT PANEL (A2)

DO NOT SCALE DWG



2. THIS SHEET IS INTENDED TO SHOW MECHANICAL ASSEMBLY ONLY - REFERENCE SHEET 2 OF 2 FOR WIRING.

1. SEE PARTS LIST NO. 1501-00-0962

WAVETEK

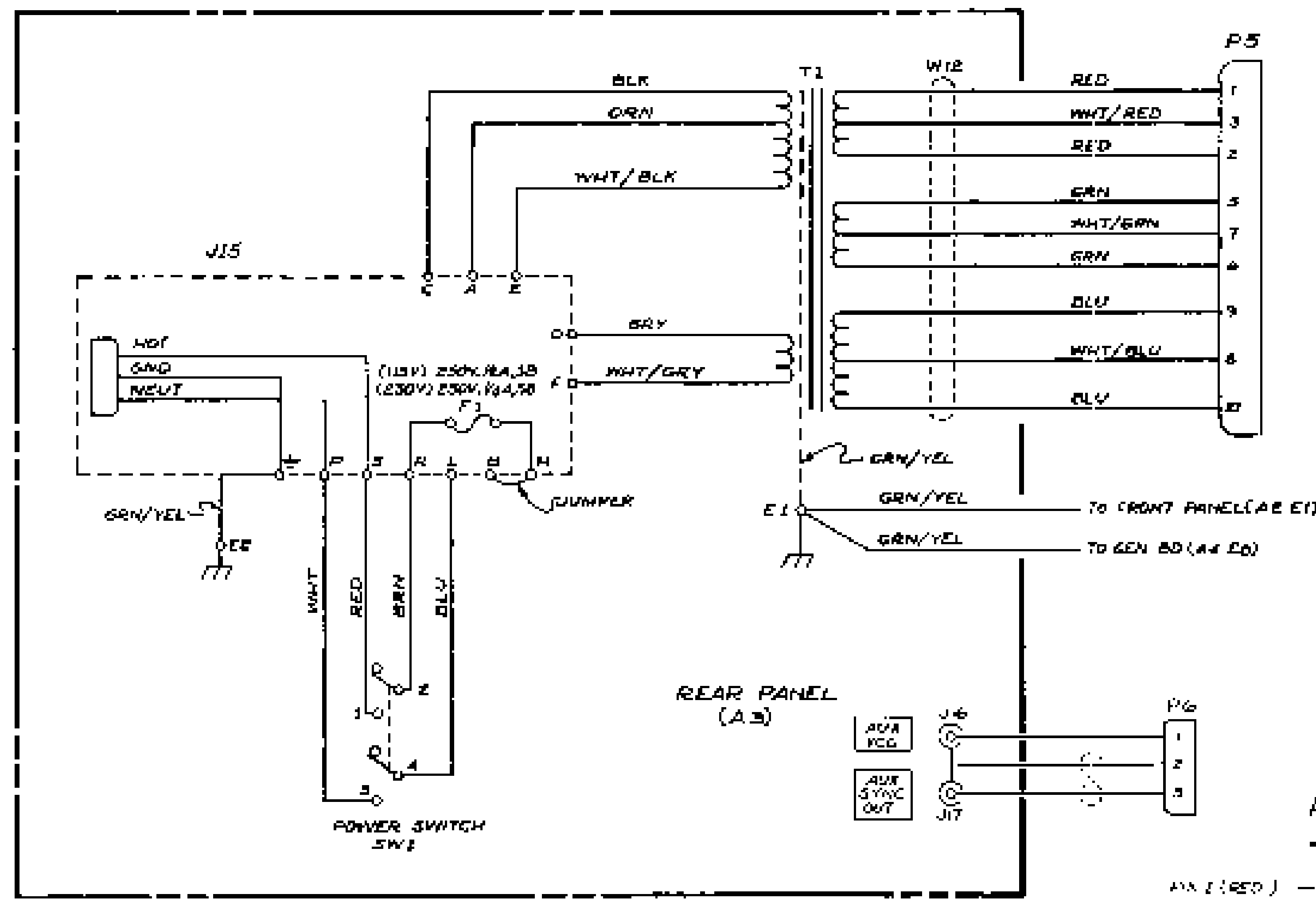
ASSEMBLY REAR PANEL (A3)

DO NOT SCALE DWG

193 | 0102-00-0962 | B

23338

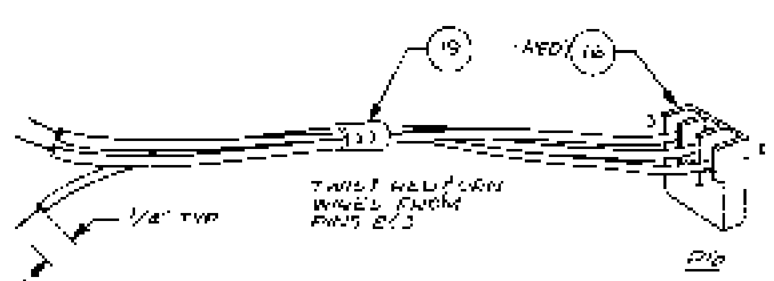
SHEET 1 OF 2

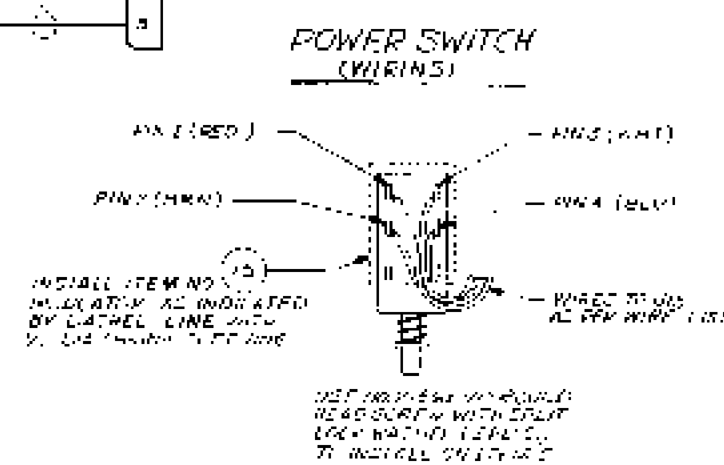


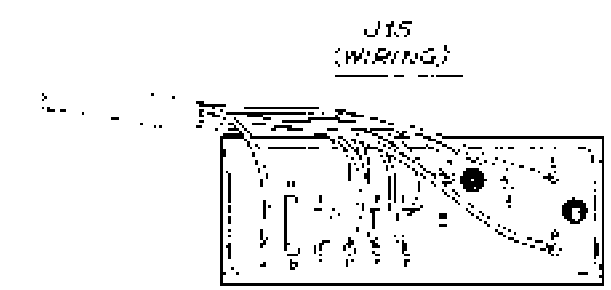
WIRE LIST				
			DESTINATION	
AWG	COLOR	LENGTH	FROM	TO
22	RED	5"	T1	P5-1
22	RED	5"	T1	P5-2
22	WHT/RED	5"	T1	P5-3
		5"		P5-4
22	GRN	5"	T1	P5-5
22	GRN	5"	T1	P5-6
22	WHT/GRN	5"	T1	P5-7
22	WHT/BLK	5"	T1	P5-8
22	BLU	5"	T1	P5-9
22	BLU	5"	T1	P5-10
22	GRN/YEL	3 1/2"	T1 (SHIELD)	A3 E1
24	BLK	4 3/4"	T1	J15-C
24	ORN	4 3/4"	T1	J15-A
24	WHT/BLK	4 3/4"	T1	J15-E
24	GRY	4 3/4"	T1	J15-D
24	WHT/GRY	4 3/4"	T1	J15-F
22	WHT	3 1/4"	J15-P	SW1-3
22	RED	3 1/4"	J15-S	SW1-1
22	BRN	3 1/4"	J15-R	SW1-2
22	BLU	3 1/4"	J15-L	SW1-4
22	BUSS	———	J15-B	J15-H
18	GRN/YEL	1 3/4"	J15-⏚	A3 E2
18	GRN/YEL	11 1/2"	A3 E1	A2 E1
18	GRN/YEL	9 1/2"	A3 E1	A4 E8
22	BUSS	———	J16 ⏚	J17 ⏚
22	BRN	8 1/2"	J16	P6-1
22	RED	8 1/2"	J16 ⏚	P6-2
22	GRY	8 1/2"	J17	P6-3

W1, W2: WIRE MARKER (19)

TWISTED GRP: W11 (REF)







1. THIS SHEET IS INTENDED TO SHOW WIRE HOOK UP ONLY - REFERENCE SHEET 1 OF 2 FOR MECHANICAL ASSEMBLY.

WAVETEK

ASSEMBLY, REAR PANEL (A3)

DO NOT SCALE DWG

0102 00-0962

SHEET 2 OF 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG MFGR PART NO	MFGR	WAVETEK NO	QTY/PT
NONE	ASSY DRAW, FRONT PANEL	0102-00-0982	WVTK	0102-00-0982	1
NONE	DIAL ASSY	WVTK	[illegible]	1201-00-1833	1
2	INDICATOR, DIAL	180-803	WVTK	1400-00-4970	1
3	FRONT PANEL	190-3800	WVTK	1400-01-3800	1
4	ANGLE, PANEL MNTG	190-4523	WVTK	1400-01-4523	1
5	ANGLE, PANEL MNTG	190-4522	WVTK	1400-01-4522	1
6	CONN BNC	KC-7945	KINGS	2100-01-0007	6
8	SOLDER LUG	1497	SMITH	2100-04-0012	6
9	SOLDER LUG	[illegible]	[illegible]	2100-04-0035	1
10	BUSHING NYLON	[illegible]	THOMAS	2800-01-0003	2
11	BEARING, PANEL	167	SMITH	2800-01-0004	1
12	BUSHING, CYLINDER 1/4	[illegible]	THOMAS	2800-01-0005	1
14	WASHER, SHOULDER	[illegible]	SMITH	2800-27-0004	10
15	NYLON FLAT WASHER	[illegible]	[illegible]	2800-28-0009	1
NONE	WASHER, WAVE SPRING	5904 133 1	SEA	2800-28-0021	1
NONE	WASHER, FLAT, BRASS, .025 ID, .400 OD	SEA	[illegible]	2800-28-0022	1

WAVETEK PARTS LIST

TITLE ASSY, FRONT PANEL

ASSEMBLY NO 1101-00-0982

REV A

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG MFGR PART NO	MFGR	WAVETEK NO	QTY/PT
NONE	POT, [illegible] PRECISION LINEAR	[illegible]	[illegible]	4600-08-0017	1

WAVETEK PARTS LIST

TITLE ASSY, FRONT PANEL

ASSEMBLY NO 1101-00-0982

REV A

PAGE 2

WAVETEK

PARTS LIST
ASSY, FRONT PANEL

1101-00-0982

REV A