Instruction Manual

Tektronix

TSG 371
Component/PAL Television Generator

070-7707-01

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WARRANTY

Tektronix warrants that this product will be free from defects in materials and workmanship for a period of one (1) year from the date of shipment. If any such product proves defective during this warranty period, Tektronix, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

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EC Declaration of Conformity

We

Tektronix Holland N.V.
Marktweg 73A
8444 AB Heerenveen
The Netherlands

declare under sole responsibility that the

TSG371 Component/Composite TV Signal Generator

meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities:

EN 50081-1 Emissions:

EN 55022	Class B Radiated and Conducted Emissions

EN 50082-1 Immunity:

IEC 801-2	Electrostatic Discharge Immunity
IEC 801-3	RF Electromagnetic Field Immunity
IEC 801-4	Electrical Fast Transient/Burst Immunity

High-quality shielded cables must be used to ensure compliance to the above listed standards.

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LIST OF ILLUSTRATIONS

SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

In This Manual


This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment


DANGER — High voltage.


Protective ground (earth) terminal.


ATTENTION — refer to manual.

Power Source

This product is intended to operate from a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Ground the Product

This product is grounded through the grounding conductor of the power module power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power module power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Fuse

To avoid fire hazard, use only the fuse of correct type, voltage rating, and current rating as specified in the parts list for your product.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Operate Without Covers

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

SECTION 1
INTRODUCTION

The TSG 371 is a test signal and sync generator designed for the operation and maintenance of facilities working in analog component and PAL formats. The fully independent test signal generators provide continuous component and composite colour bars as well as a stable, accurate reference black for post production operations. The test signal set is designed to satisfy routine equipment setup and maintenance requirements.

These features make the TSG 371 the perfect choice for today's analog component/PAL environment and a wise selection for PAL houses where analog component is possible in the future.

Test Signal Generators

The TSG 371 has two completely separate and independent test signal generators. Both use 10 bit signal generation and precision digital-to-analog converters to ensure signal accuracy and long-term stability.

The component generator provides test signals at 700 mV in all channels for 100% amplitude. The test signal complement includes:

- 75% and 100% full field color bars over red
- 5-step gray scale
- Crosshatch pattern
- Multiburst
- Line sweep
- Bowtie

The PAL composite generator provides:

- 75% and 100% full field color bars over red
- 5-step gray scale
- Pulse & bar with window
- Multiburst
- Modulated ramp
- Pluge

Sync Generator

The TSG 371 contains a high stability, correctly SCH phased internal sync generator with a full color genlock. These features make it ideal for system master applications and easily integrated into a system where a master SPG already exists. The composite outputs maintain proper SCH phase in both internal and genlock operation modes.

There are six black burst outputs and one each comp sync and comp blanking outputs. In small systems such as component edit suites, the multiple black outputs may eliminate the need for a distribution amplifier. In addition, the sync and blanking outputs may be converted to black burst, providing a total of eight outputs.

Automatic detection of incoming reference and a versatile output timing control system simplify genlock operation. In the auto mode, the TSG 371 operates in external lock when the incoming reference signal is present. When reference is absent, the generator switches to its own internal standard. The generator's output timing controls provide for phasing all generator outputs relative to the reference signal. In addition, the sync and blanking outputs may be phase offset from the composite and component outputs. This is useful in integrating the generator into a system where one or more devices lack sync phasing controls. Up to eight different timing settings may be stored in non-volatile memory.

Remote Control

Remote selection of test signal internal/external reference and the genlock and sync timing presets may be made with ground closures through a rear-panel connector.

SECTION 2
OPERATING INSTRUCTIONS

This section explains how to operate the TSG 371. It also describes each of the test signals and the rear-panel connector outputs.

CONTROLS, INDICATORS, AND CONNECTORS

Front-Panel Controls

Nine click-dome switches control the TSG 371 (See Fig. 2-1).

The MODE SELECT switch on the far right selects from the three operating modes:

SELECT TEST SIGNAL,
SET GENLOCK TIMING, and
SET SYNC TIMING.

There are also eight multifunction switches which have different functions depending upon the Operating Mode selected by the MODE SELECT switch. See Fig. 2-2.

Indicators

There are fourteen LED indicator lamps on the front-panel.

The set of three LEDs on the far right indicate the Operating Mode. One of these will be on at all times.

The LED under the right set of four switches should only be lit in conjunction with either the SET GENLOCK TIMING or SET SYNC TIMING Operating Mode LED. This LED indicates that these switches are operating and available to advance or delay timing.

The four LEDs above the right buttons indicate which PAL test signal is available at the rear panel. Only one should be lit at a time depending upon which PAL test signal is selected. These LEDs should only be lit in conjunction with the SELECT TEST SIGNAL Operating Mode LED.

The four LEDs above the left buttons indicate which component test signal is available at the rear panel. Only one of them should be lit at a time depending upon which component test signal is selected. These LEDs should only be lit in conjunction with the SELECT TEST SIGNAL Operating Mode LED.

The far left set of LEDs indicates whether the TSG 371 is operating in the genlocked external reference state or using its internally generated clock as the reference. Only one of these LEDs should be lit at a time.

If more LEDs are lit than are appropriate or they are flashing, this indicates an error condition. Have a qualified service technician see Section 7, Maintenance, to interpret the LED's meaning.

Fig. 2-1. TSG 371 Front Panel.

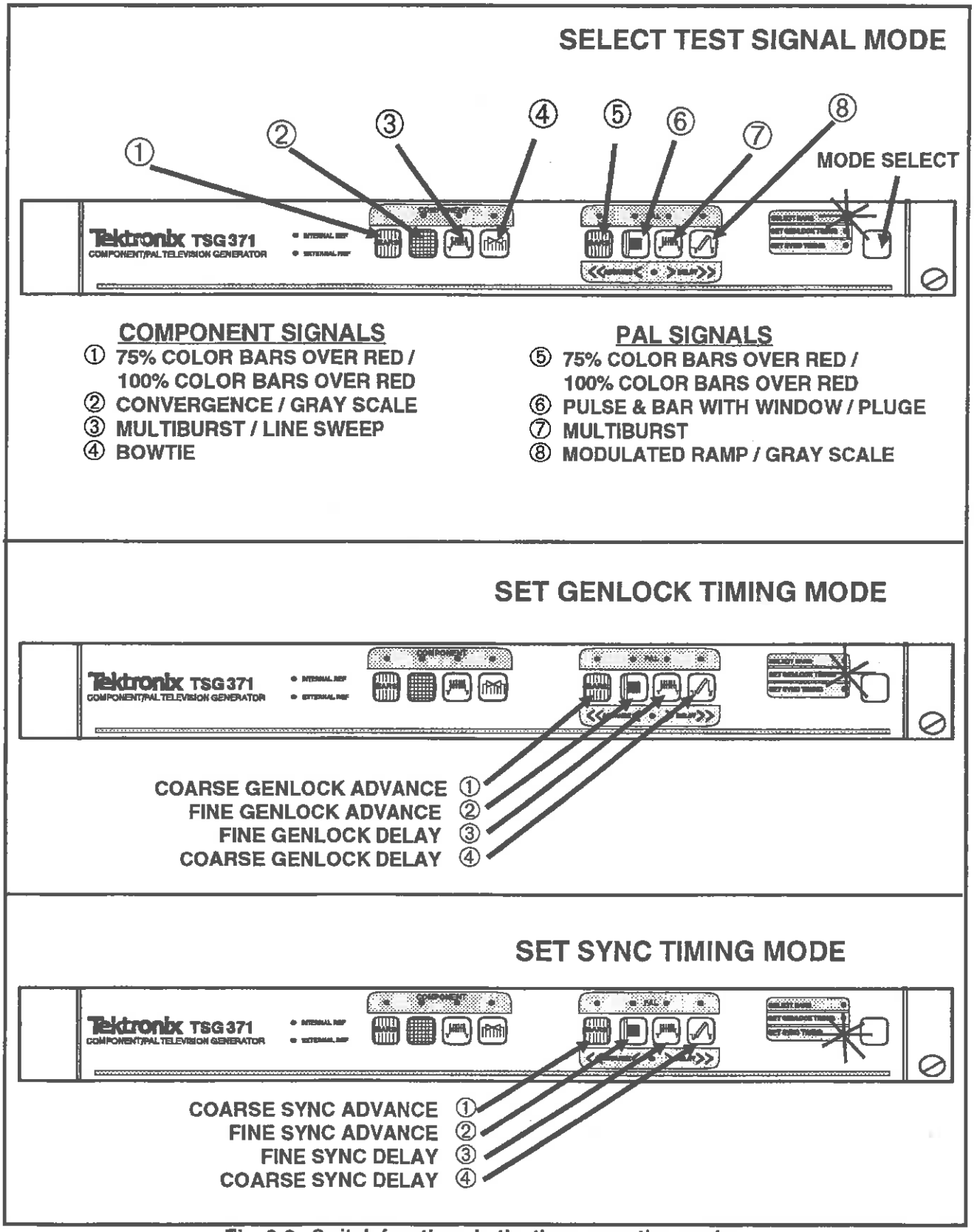


Fig. 2-2. Switch functions in the three operating modes.

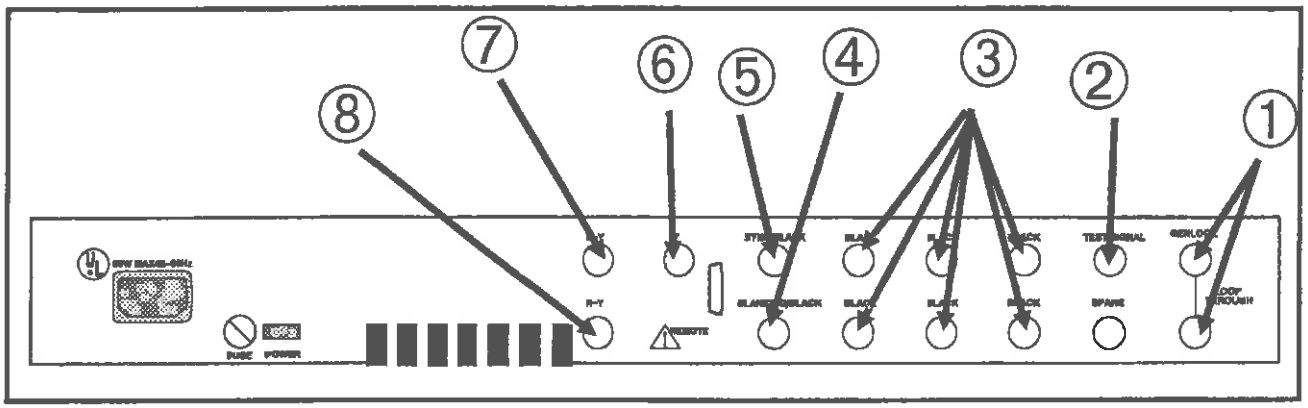


Fig. 2-3. The rear panel of the TSG 371.

Rear-Panel Connectors

The rear-panel has fifteen BNC video connectors, one 9-pin remote control connector, and one power socket. Fig. 2-3 shows the rear panel, and Table 2-1 lists the rear panel outputs.

Rear-Panel Controls

POWER - ON/OFF push-push switch.

Table 2-1. Rear Panel Outputs.

CONNECTOR	STANDARD SIGNAL	OPTIONAL SIGNAL (Jumper Selectable)
① GENLOCK LOOP-THROUGH	Genlock Input	--------
② TEST SIGNAL	PAL Test Signal Output	--------
③ BLACK	Black Burst	--------
④ BLANKING/BLACK	Composite Blanking	-2 V or -4 V level Jumper switchable to Black Burst output.
⑤ SYNC/BLACK	Composite Sync	-2 V or -4 V level Jumper switchable to Black Burst output.
⑥ Y	EBU level signals	
⑦ B-Y	EBU level signals	
⑧ R-Y	EBU level signals	
SPARE	not used	

USING THE CONTROLS

Operating Modes

SELECT TEST SIGNAL MODE

NOTE

The PAL and component signals are selected independently.

To get into this mode, press the MODE SELECT switch on the far right of the front-panel until the SELECT TEST SIGNAL LED is lit. (See Fig. 2-4). Now new test signals can be selected using the click-dome switches.

The eight switches select between the available test signals listed in Table 2-2 and Table 2-3.

Table 2-2. Composite Signals.

SWITCH	SIGNALS AVAILABLE
BARS	100% COLOR BARS over RED 75% COLOR BARS over RED
PULSE & BAR with WINDOW	PULSE & BAR with WINDOW PLUGE
MULTIBURST	MULTIBURST
MODULATED RAMP	MODULATED RAMP GRAY SCALE

Table 2-3. Component Signals.

SWITCH	SIGNALS AVAILABLE
BARS	100% COLOR BARS over RED 75% COLOR BARS over RED
CONVERGENCE	CONVERGENCE GRAY SCALE
MULTIBURST	MULTIBURST LINE SWEEP
BOWTIE	BOWTIE

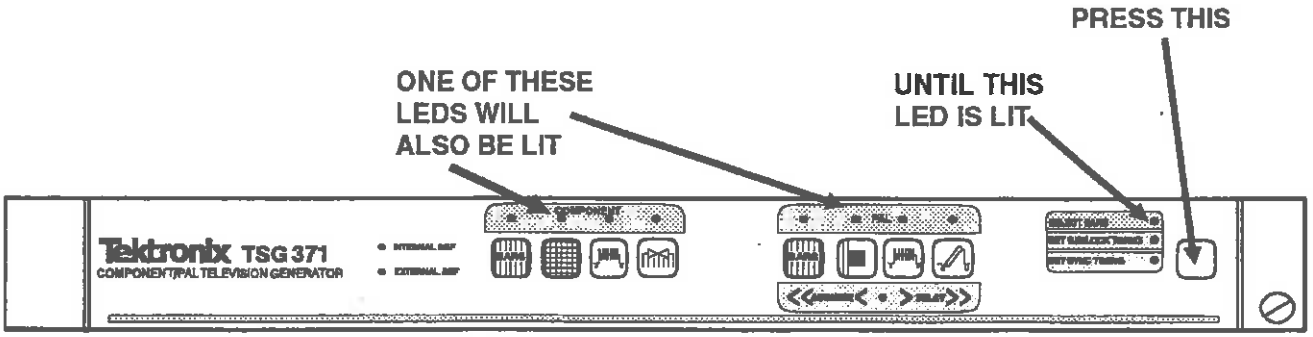


Fig. 2-4.
How to put the TSG 371 in the SELECT TEST SIGNAL mode.

SET GENLOCK TIMING MODE

In the SET GENLOCK TIMING mode, the four right switches shift the timing of the test and sync pulse signals together with respect to the Genlock Input.

While the front panel is in this mode, the four right switches assume the following functions (from left to right): Coarse Genlock Advance, Fine Genlock Advance, Fine Genlock Delay, and Coarse Genlock Delay.

Fine Genlock Advance and Fine Genlock Delay provide adjustment of genlock test signals and sync timing over a total timing range of about ±55° in 0.2° steps. Coarse Genlock Advance and Coarse Genlock Delay provide coarse adjustment over a total range of approximately ±7 µs in 28 ns (45°) steps. Arrows below the switches indicate the direction (advance or delay) and amount of timing offset.

Setting Genlock Timing

To adjust genlock timing, first press the MODE SELECT switch until the SET GENLOCK TIMING LED is lit. Note the red LED under the right four switches indicates that these switches now control genlock timing. (See Fig. 2-5.)

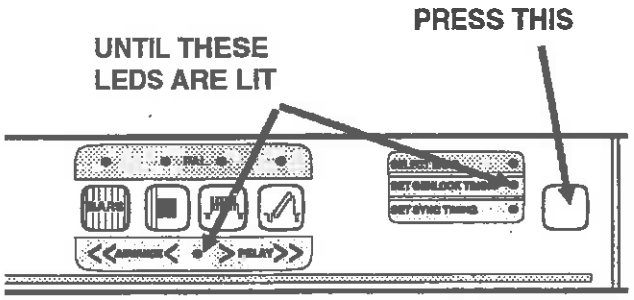


Fig. 2-5.
How to put the TSG 371 in the Set Genlock Timing mode.

To advance genlock timing, press the Fine Genlock Advance switch for fine increments of advance (steps of 0.2°) or press the Coarse Genlock Advance switch for coarse increments (steps of 45°). To delay genlock timing, press and hold down the Fine Genlock Timing switch for fine increments of delay or press the Coarse Genlock Delay switch for coarse increments of delay. (See Fig. 2-6.)

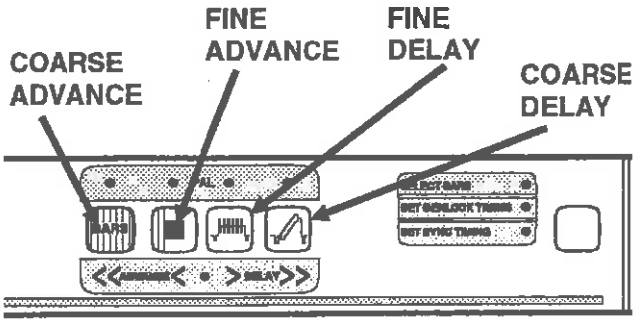


Fig. 2-6.
How to advance and delay the genlock timing.

If the end of the fine adjustment range is reached and more adjustment is needed, push the coarse adjustment switch to change the phase by a whole coarse step. If this introduces more change than is desired, then press the opposite fine switch to reduce the amount of desired change.

Note that when the genlock timing switches are held down, they shift genlock timing at a rate of three steps per second for the first three seconds and then speed up to 25 steps per second.

If a timing selection is not made within 30 seconds of entering the SET GENLOCK TIMING Mode, the front panel automatically reverts to the SELECT TEST SIGNAL mode.

Storing Genlock Setting

The front panel will automatically store the genlock timing when returning to the SELECT TEST SIGNAL Mode, through either 30 second time-out or cycling with the MODE SELECT switch to the SELECT TEST SIGNAL Mode.

SET SYNC TIMING MODE

In the SET SYNC TIMING Mode, the four right switches advance or delay the generator's sync pulse outputs relative to the test signal output. (Fig. 2-7 shows this timing relationship.) While the front-panel is in SET SYNC TIMING Mode, these switches take on the following functions (from left to right): Coarse Sync Timing Advance, Fine Sync Timing Advance, Fine Sync Timing Delay, and Coarse Sync Timing Delay.

Fine Sync Timing Advance and Delay provide fine adjustment of sync timing over a range of about ±50° in approximately ±0.2° steps. Coarse Sync Timing Advance and Delay provide coarse adjustment over a range of approximately ±3.5 µs in 28 ns (45°) steps. Arrows below the switches indicate the direction and amount of timing shift.

Setting Sync Timing

To adjust the timing offset of the sync pulse signals with respect to the test signal output, press the MODE SELECT switch until the SET SYNC TIMING LED is lit. Note that the red LED under the four right switches indicates that these switches control sync pulse timing. (See Fig. 2-8.)

TO GET INTO SYNC TIMING MODE:

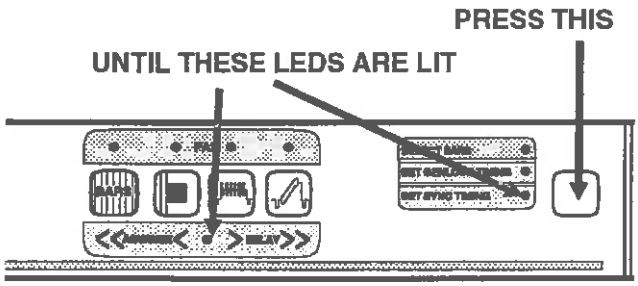


Fig. 2-8.
How to enter Sync Timing mode.

Press and hold down the Fine Sync Advance switch to select small increments (approximately 0.2°) of advance, or press Coarse Sync Advance to SELECT coarse increments (45°). Press the Fine Sync Timing Delay and Coarse Sync Timing Delay switches to add fine and coarse amounts of delay, respectively. (See Fig. 2-9.)

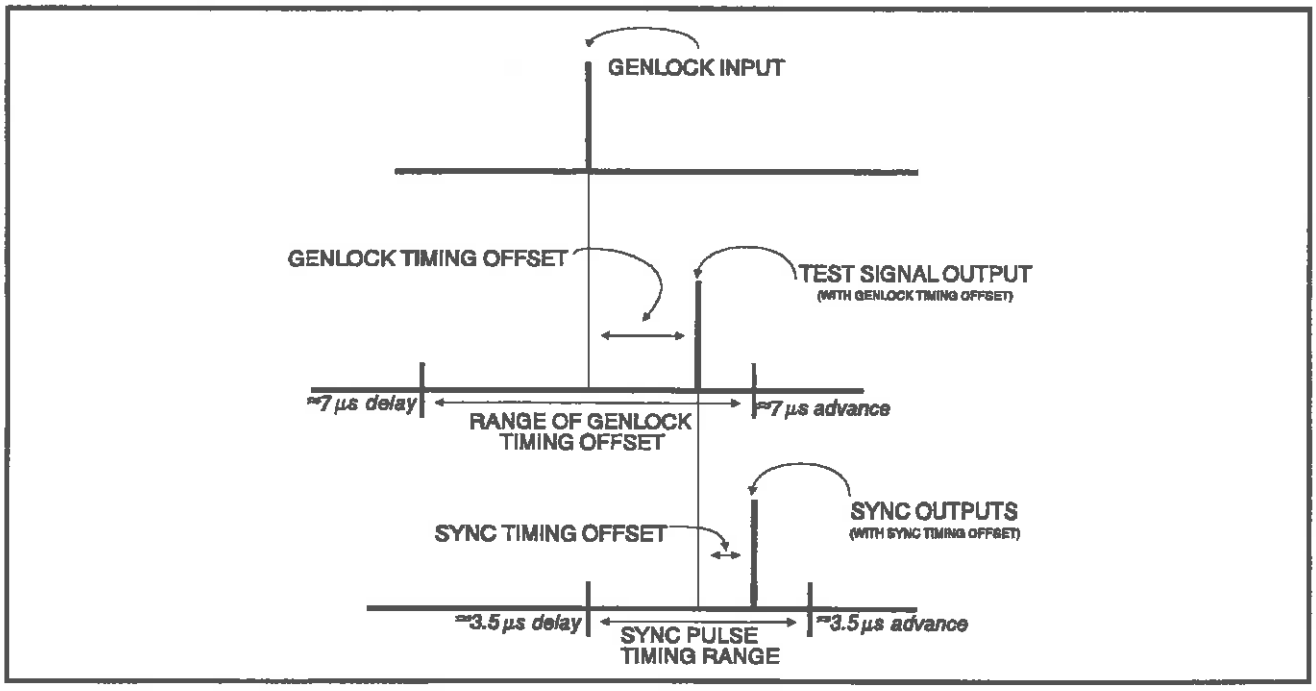


Fig. 2-7. Relative Timing.

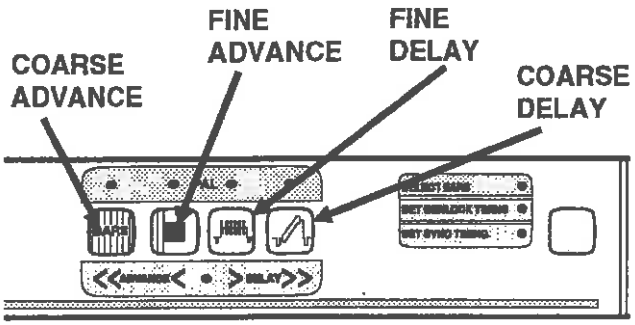


Fig. 2-9.
How to advance and delay the sync timing.

If the end of the Fine Advance range is reached and more adjustment is needed, push the Coarse Sync Timing Advance switch to advance the phase by a whole coarse step. If this introduces more advance than wanted, press the Fine Sync Timing Switch to reduce the amount of advance.

When the advance or delay switches are held down, they shift sync timing at a rate of three steps per second for the first three seconds and then speed up to 25 steps per second.

If a timing selection is not made within 30 seconds after entering the SET SYNC TIMING Mode, the front panel automatically reverts to the SELECT TEST SIGNAL Mode.

Storing Sync Setting

The front panel will automatically store the sync timing when returning to the SELECT TEST SIGNAL Mode, through either 30 second time-out or cycling with the MODE SELECT switch to the SELECT TEST SIGNAL Mode.

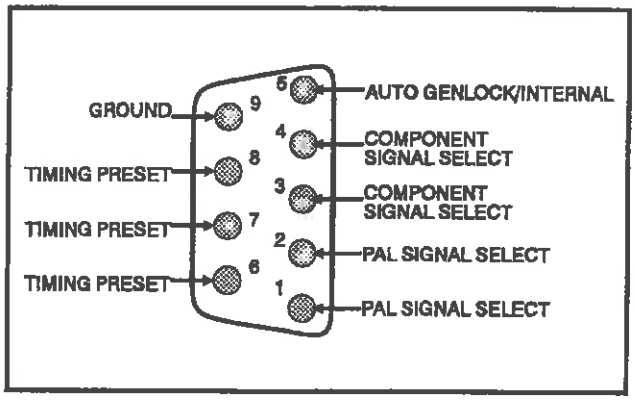
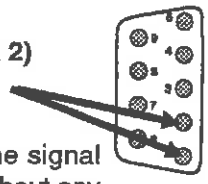


Fig. 2-10. Pinout of the REMOTE connector.

Remote Control

The TSG 371 can be remotely controlled through the 9-pin REMOTE CONTROL connector located on the rear panel. Through TTL-compatible ground closures, these pins control the functions described in Table 2-4. Typically the pins would be grounded through user supplied switches, using pin 9 as ground. The instrument can be locked into a fixed operating mode by wiring directly to the connector. To do this, attach a male 9-pin DIN plug to the REMOTE connector and solder the appropriate pins to ground. Fig. 2-10 shows the connector's pin out.

PAL SIGNAL SELECT (pins 1 & 2)



Remote pin setting 11 selects the signal last selected at the front panel (without any setup procedure). Any other pin setting chooses the signal programmed for that setting.

How to Reprogram the Select PAL Test Signal Pins:

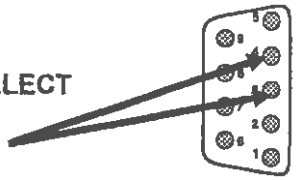
1. Turn the power off.
2. Set jumper J208 on the Digital Board to position 2-3 (program position).
3. Turn the power on.
4. Set the Remote Pins to their desired position from 00, 01, or 10 (1=open, 0=ground).
5. Select the desired signal from the front panel. This signal is now programmed for the given pin setting.
6. If more signals are desired repeat steps 4 and 5 until the desired number of signals are programmed (up to three).

Table 2-4. List of Remote Control Pins and Functions.

FUNCTION	PINS	DESCRIPTION
PAL Signal Select	1 & 2	Two binary-coded control lines programmed to select a set of three PAL test signals plus the last signal selected from the front panel. These pins can be reprogrammed to select a different set.
Component Signal Select	3 & 4	Two binary-coded control lines programmed to select a set of three component test signals plus the last signal selected from the front panel. These pins can be reprogrammed to select a different set.
Auto Genlock/(Internal)	5	Selects Internal Sync Generator Reference Mode when grounded. Otherwise, the TSG 371 automatically switches to Genlock Mode whenever a valid Genlock Input is present.
Timing Preset	6 - 8	Binary-coded control lines programmed to select one of eight timing presets. (Both sync and genlock timing are set.)
Ground	9	Ground.

7. Turn the power off.
8. Return J208 to the non-program position.
9. Turn the power on.

COMPONENT SIGNAL SELECT (pins 3 & 4)

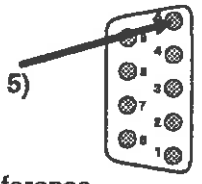


Remote pin setting 11 selects the signal last selected at the front panel (without any setup procedure). Any other pin setting chooses the signal programmed for that setting.

How to Reprogram the Select Component Test Signals Pins:

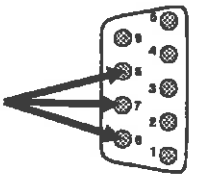
1. Turn the power off.
2. Set jumper J208 on the Digital Board to position 2-3 (program position).
3. Turn the power on.
4. Set the Remote Pins to their desired position from 00, 01, or 10 (1=open, 0=ground).
5. Select the desired signal from the front panel. This signal is now programmed for the given pin setting.
6. If more signals are desired repeat steps 4 and 5 until the desired number of signals are programmed (up to three).
7. Turn the power off.
8. Return J208 to the nonprogram position.
9. Turn the power on.

AUTO GENLOCK/INTERNAL (pin 5)



Selects Internal Sync Generator Reference Mode when grounded. Otherwise, the TSG 371 automatically switches to Genlock Mode whenever a valid Genlock input is present.

TIMING PRESET (pins 6, 7, & 8)



The REMOTE CONTROL's Genlock Preset chooses one of four advance or delays to add to the test signals.

To set a Genlock Preset perform the following steps:

1. Set the Remote Pins to their desired position from 000 to 111 (1=open, 0=ground).
2. Set the amount of advance or delay for both the genlock and sync timing from the front panel. This timing is now programmed for the given pin setting.
3. Cycle the MODE SELECT Button back to the SELECT TEST SIGNAL mode.
4. If others are desired, repeat steps 1, 2 and 3 until the desired number of timing presets are programmed (up to eight).

SECTION 3

TABLE OF SPECIFICATIONS

The performance requirements are valid within the environmental limits if the TSG 371 is adjusted at 25°C ±5°C, and a minimum warm-up of 20 minutes is allowed.

Safety Features

This product is designed and tested in accordance with the requirements for industry safety standards. These standards include the following:

UL1244 — Second Edition — Standard for Electrical and Electronic Measuring and Testing Equipment.

ANSI C39.5 — Safety Requirements for Electrical and Electronic Measuring and Controlling Instrumentation, 1984, Draft #11.

CSA — Electrical Bulletin No. 556B.

IEC 348 — Second Edition — Safety Standards for Electronic Measuring Apparatus.

FCC EMI Compatability – 47 CFR Part 15, Subpart B, Class A

Table 3-1
PAL Test Signal Generator — General Test Signal and Black Burst Characteristics

Characteristics	Performance Requirements	Supplemental Information
Luminance Amplitude Accuracy	±1%.	Measured at 700 mV.
DC Output Level	Test Signal: 0 Vdc ±50 mV. Black Burst: 0 Vdc ±5 mV.	Measured at blanking.
Chrominance-to-Luminance Gain	±1%.	Measured at 980 mV p-p, at 500 kHz, and 4.43 MHz referenced to 500 kHz.
Frequency Response	±1% to 5 MHz.	
Chrominance-to-Luminance Delay	≤5 ns.	5 mV p-p = 9 μs delay once 20T pulse.
SCH Phase Accuracy		±2.5 ns typical.
Luminance Rise Time	250 ns ±25 ns.	Except color bars, 2T bar, and convergence.
Chrominance Rise Time	350 ns ±35 ns.	
Burst Amplitude	300 mV ±6 mV p-p.	
Burst Rise Time	350 ns ±35 ns.	Slower than BBC spec to avoid ringing.
Sync Amplitude	300 mV ±3 mV.	
Sync Rise Time	250 ns ±25 ns.	
Horizontal Timing	See Fig. 3-1 to 3-9.	All signals comply with PAL timing specs.
Front Porch Duration	1.55 μs minimum, except narrow blanking test signal.	1.65 μs typical; narrow blanking front porch is 1.425 μs.
Line Blanking Interval		
Nominal Blanking	12.05 μs nominal for all test signals except narrow blanking signal.	Beginning at 50% point of active video.
Narrow Blanking	11.60 μs ±0.1 μs for narrow blanking signal.	For blanking width measurement.
Breezeway Duration	900 ns ±50 ns.	
Horizontal Sync Duration	4.7 μs ±50 ns.	50% amplitude point.
Vertical Serration Duration	4.7 μs ±50 ns.	50% amplitude point.
Equalizing Pulse Duration	2.35 μs ±50 ns.	50% amplitude point.
Burst		
Delay from Sync	5.6 μs ±50 ns.	From 50% point of sync.
Burst Duration	2.255 μs ±0.1 μs.	10 cycles of subcarrier.

Table 3-1 (cont.)
PAL Test Signal Generator — General Test Signal and Black Burst Characteristics

Characteristics	Performance Requirements	Supplemental Information
Output Impedance	75Ω.	
Return Loss	36 dB to 5 MHz.	
Crosstalk	≥60 dB down.	
Residual Subcarrier	≥60 dB down.	
Glitches	≤2 mV.	

Table 3-2
PAL Test Signal Generator — Test Signals

Characteristics	Performance Requirements			Supplemental Information
75% Color Bars over Red				
Luminance Rise Times	150 ns ±25 ns.			
	Lum Ampl. (mV)	**Subc. Ampl. (mV p-p)**	**Subc. Phase (deg)**	
White	700.0	0.0	0.0	
Yellow	465.1	470.5	167.1	
Cyan	368.0	663.8	283.5	
Green	308.2	620.1	240.7	
Magenta	216.8	620.1	60.7	
Red	157.0	663.8	103.5	
Blue	59.9	470.5	347.1	
Field Timing				
Color Bars	Lines 23 – 166.			
Red	Lines 167 – 310.			

Table 3-2 (cont.)
PAL Test Signal Generator — Test Signals

Characteristics	Performance Requirements			Supplemental Information
100% Color Bars over Red				
Luminance Rise Times	150 ns ±25 ns.			
	Lum Ampl. (mV)	**Subc. Ampl. (mV p-p)**	**Subc. Phase (deg)**	
White	700.0	0.0	0.0	
Yellow	620.2	627.3	167.1	
Cyan	490.7	885.1	283.5	
Green	410.9	826.8	240.7	
Magenta	289.1	826.8	60.7	
Red	209.3	885.1	103.5	
Blue	79.8	627.3	347.1	
Field Timing				
Color Bars	Lines 23 – 166.			
Red	Lines 167 – 310.			
Pulse & Bar With Window				
20T Modulated Pulse				
HAD	2000 ns ±20 ns.			
Chroma Phase	60.7°.			
Amplitude	700 mV.			
2T Pulse				
HAD	200 ns ±20 ns.			
Amplitude	700 mV.			
2T Bar				50% amplitude point.
Width	26 μs.			
Rise Time	192.9 ns ±20 ns.			
White Bar Amplitude	700.0 mV.			
Field Tilt	≤0.5%.			
Line Tilt	≤0.5%.			
Window Field Timing	Lines 89 – 244.			
Pulse-to-Bar Ratio	1:1 ±0.5%.			
Ringing	≤1% peak.			

Table 3-2 (cont.)
PAL Test Signal Generator — Test Signals

Characteristics	Performance Requirements	Supplemental Information
Multiburst		
White Reference Bar Amplitude	560.0 mV.	
Packet Amplitudes	420.0 mV p-p.	Equal width packets.
Pedestal	350.0 mV.	
Burst Frequencies	500 kHz, 1.0 MHz, 2.0 MHz, 4.0 MHz, 4.8 MHz, 5.8 MHz.	
Packet Rise Time	350 ns typical.	Sine squared shaped packets.
5-Step Gray Scale		
Amplitude	700.0 mV.	
Linearity Error	≤1%.	Relative step matching.
Modulated Ramp		
Luminance Amplitude	700.0 mV.	
Linearity Error	≤1%.	
Chrominance Amplitude	280.0 mV p-p.	
Phase Angle	60.65°.	
Diff Gain	0.6% maximum.	
Diff Phase	0.3° maximum.	
Pluge (BBC Version 2)		
Pluge Levels	−14 mV and +14 mV.	
Lum Ref Levels	700 mV, 450 mV, 200 mV, and 110 mV.	
Field Timing		
700 mV	Lines 63-114.	
450 mV	Lines 115-166.	
200 mV	Lines 167-218.	
110 mV	Lines 219-270.	

Table 3-3
PAL Test Signal Generator — Diagnostic Signals

Characteristics	Performance Requirements	Supplemental Information
DAC Test 1	Split field: 500 kHz followed by 4.43 MHz (980 mV p-p).	Non-composite signal.
25 Hz Offset Test	25 Hz sine wave, 980 mV p-p.	Non-composite signal.
Nonburst Color Bars		75% bars with no burst.

Table 3-4
PAL Test Signal Generator — Black Burst Output

Characteristics	Performance Requirements	Supplemental Information
Black (or Blanking) Level	0 V ±5.0 mV.	
Blanking Width	< 11.2 μs.	
Glitch Amplitude	< 10 mV.	
Phasing	< 2°.	Compared to test signal output.
Return Loss	≥ 36 dB to 5 MHz.	

Table 3-5
PAL Sync Generator — General Pulse Output Characteristics

Characteristics	Performance Requirements	Supplemental Information
Amplitude	–2.0 ±0.2 V.	Jumper selectable to –4 V.
Impedance	75Ω.	
Return Loss	≥ 30 dB to 5 MHz.	
Rise and Fall Times	250 ns ±50 ns.	

Table 3-6
PAL Sync Generator – Pulse Output Signals

Characteristics	Performance Requirements	Supplemental Information
Composite Sync		
Horizontal Sync Duration	4.70 μs ±0.1 μs.	
Vertical Serrations	4.70 μs ±0.1 μs.	
Equalizing Pulse Duration	2.35 μs ±0.1 μs.	
Blanking		
Horizontal Blanking Duration	12.01 μs ±0.1 μs.	Factory set to 12.01; Jumper selectable for 11.79 or 12.24 μs.
Vertical Blanking Duration	25 lines.	Jumper selectable for 24 or 25 lines. Factory set to 25.

Table 3-7
Genlock Function

Characteristics	Performance Requirements	Supplemental Information
Burst Lock		
Genlock Phase Change with Input Amplitude	≤1° burst phase change for input sync or burst amplitude range of 300 mV +3 to –3 dB.	For either composite video or burst amplitude errors.
	≤2° burst phase change for amplitude range of 300 mV +6 to –6 dB.	
Genlock Phase Change with Input Signal APL	≤1° burst phase change over 10% to 90% APL.	
Phase Dependence on Input Burst Frequency	≤1° burst phase change for ±10 Hz change in incoming subcarrier.	Factory tested to ≤1° burst phase change for ±20 Hz change in incoming subcarrier.
Lock Range	4.43361875 MHz ±10 Hz.	Factory tested to 4.43361875 MHz ±20 Hz.
Genlock Phase Jitter		Typically ≤0.3° peak for input sync or burst amplitude range of 300 mV +3 to –3 dB. No noise on input signal.
		Typically ≤0.4° peak for input amplitude range of 300 mV +6 to –6 dB. No noise on input signal.

Table 3-7 (cont.)
Genlock Function

Characteristics	Performance Requirements	Supplemental Information
Horizontal Timing Range Genlock Timing		≈7 μs advance and delay relative to Genlock Input. 55° of fine sync in 0.175° steps. (Front-panel control.)
Sync Timing		≈3.5 μs advance and delay relative to Genlock Input. At least 50° of fine sync in ≈0.2° steps. (Front-panel control.)
Color Framing Decisions	Will be correct for input SCH of 0° ±40°.	
Sync Lock Jitter	<10 ns for input sync amplitude range of 300 mV +3 to –3 dB.	No noise on input signal.
Noise Performance		Remains locked to 29 dB S/NR.
Genlock Stability with Gross Input Amplitude Variations	≤40° for input sync or burst amplitude range of 300 mV +7 to -12 dB.	
Vertical Timing Range	0, 1, or 2 lines advance. 1 line delay.	
Input Configuration	75Ω loop-through.	
Return Loss (Genlock Input)	≥40 dB to 5 MHz.	

Table 3-8
Component Test Signal Generator — General Test Signal Characteristics

Characteristics	Performance Requirements	Supplemental Information
Amplitude Accuracy	±1%.	Measured at 100% amplitude.
Channel Matching	±0.5% between channels, referenced to Y Channel.	
Frequency Response	±1% to 5 MHz. ±2% to 5.5 MHz.	
Delay Channel Matching	Within 5 ns relative to Y Channel.	
Sine Squared Pulses Accuracy	HADs accurate within ±10 ns.	

Table 3-8 (cont.)
Component Test Signal Generator — General Test Signal Characteristics

Characteristics	Performance Requirements	Supplemental Information
Sync Amplitude	300 mV ±1%.	
Line Timing	See Figs. 3-10 to 3-21.	
Front Porch Duration	1.55 μs ±0.1 μs.	Measured at 50% of active video to 50% of sync.
Blanking Level	0 Vdc ±50 mV.	
Line Blanking Interval	12.05 μs ±0.1 μs for all test signals.	Beginning at 20 IRE point of active video.
Line Sync Duration	4.7 μs ±50 ns.	50% amplitude point.
Output Impedance		75Ω.
Return Loss	≥36 dB to 5 MHz.	
Luminance Rise Time	200 ns ±10%.	
Color Difference Rise Time	400 ns ±10% on Color Bars. 200 ns ±10% on other signals.	
Spurious Signals	<2 mV for frequencies up to 5.5 MHz. <7 mV for frequencies from 5.5 MHz and up.	
Component to Composite Timing Error	<25 ns.	

Table 3-9
Component Test Signal Generator — Test Signals

Characteristics	Performance Requirements	Supplemental Information
100% Color Bars over Red		See Figs. 3-10 to 3-12.
75% Color Bars over Red		See Figs. 3-13 to 3-15.
Convergence		
Amplitude	525 mV (75%).	
Pattern	Crosshatch, 14 horizontal lines and 19 vertical lines per field.	
Pulse HAD	225 ns ±25 ns.	
5-Step Gray Scale		
Amplitude	700 mV.	
Linearity Error	≤1%.	Relative step matching.

Table 3-9 (cont.)
Component Test Signal Generator — Test Signals

Characteristics	Performance Requirements	Supplemental Information
60% Multiburst		
Amplitude	420 mV p-p centered on 350 mV pedestal.	
White Flag	420 mV p-p.	Y channel centered on 350 mV pedestal.
Frequencies		
Y Channel	0.5 MHz, 1 MHz, 2 MHz, 3 MHz, 4 MHz, and 5 MHz.	Centered on 350 mV pedestal.
B–Y, R–Y Channels	0.25 MHz, 0.5 MHz, 1.0 MHz, 1.5 MHz, 2 MHz, and 2.5 MHz.	Centered around 0 Vdc.
60% Line Sweep		
Amplitude	420 mV.	
Frequency Range		
Y Channel	200 kHz to 5.5 MHz.	
B–Y, R–Y Channels	100 kHz to 2.75 MHz.	
Flatness		
Y Channel	1% flatness to 5 MHz. 2% flatness to 5.5 MHz.	
R–Y, B–Y Channels	1% flatness to 2.5 MHz.	
Markers		
Y Channel	At 0.5 MHz, 1 MHz, 2 MHz, 3 MHz, 4 MHz, and 5 MHz.	
B–Y, R–Y Channels	At 0.25 MHz, 0.5 MHz, 1 MHz, 1.5 MHz, 2 MHz, and 2.5 MHz.	
Bowtie		
Y Channel	500 kHz sine wave.	
R–Y, B–Y Channels	502 kHz sine wave.	
Channel Amplitudes		
Y	825 mV.	Sync tip to peak.
B–Y and R–Y	350 mV.	
Timing Markers (Y Channel only)	11 timing markers indicate 20 ns delay/advance between channels.	
	Two timing markers centered about center marker indicate 5 ns delay/advance between channels.	

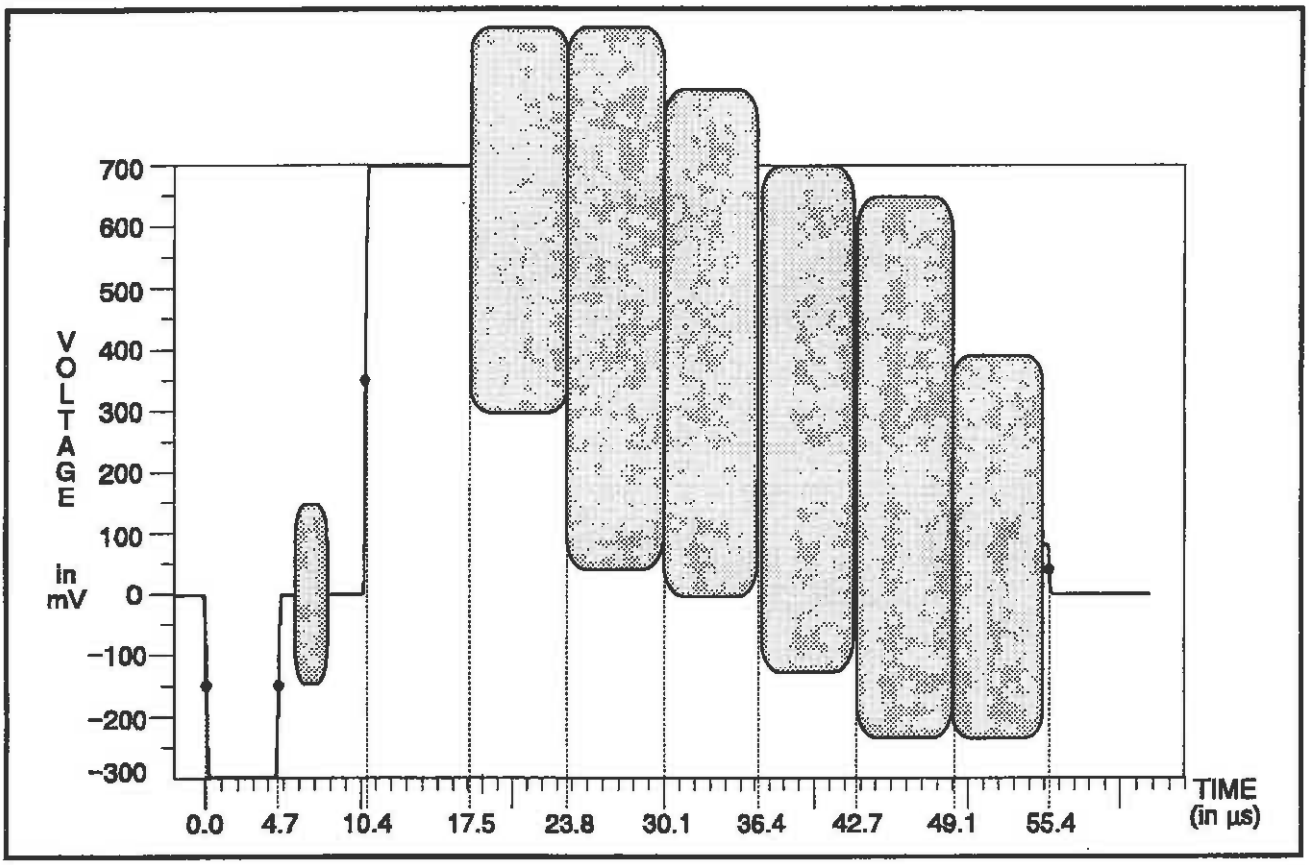


Fig. 3-1. 100% Color Bars.

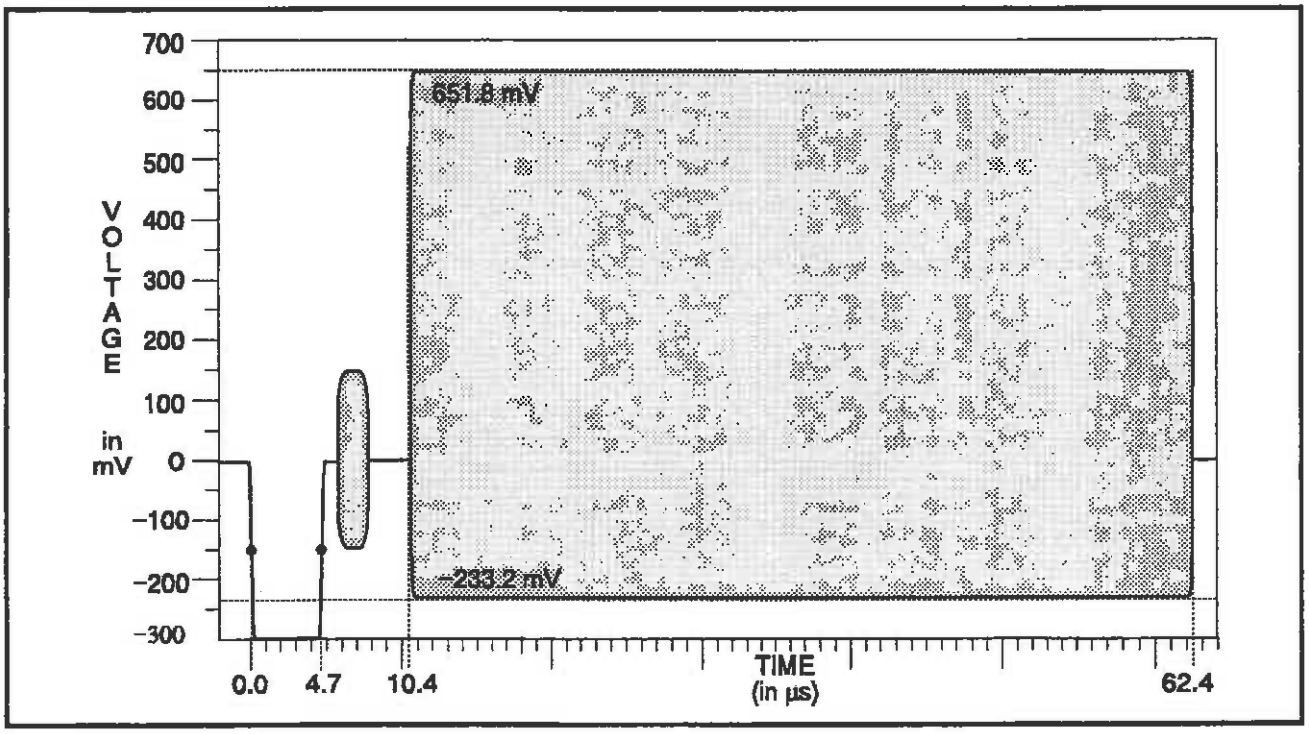


Fig. 3-2. 100% Red.

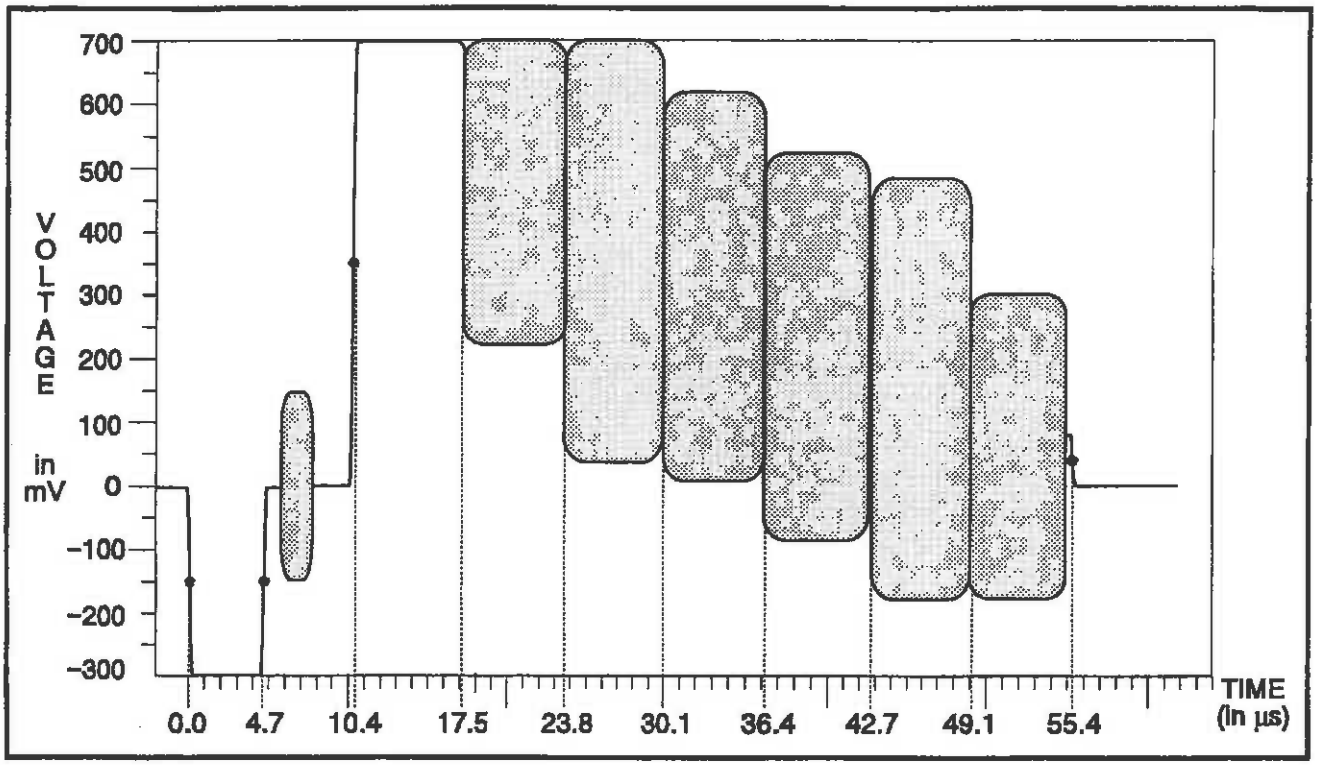


Fig. 3-3. 75% Color Bars.

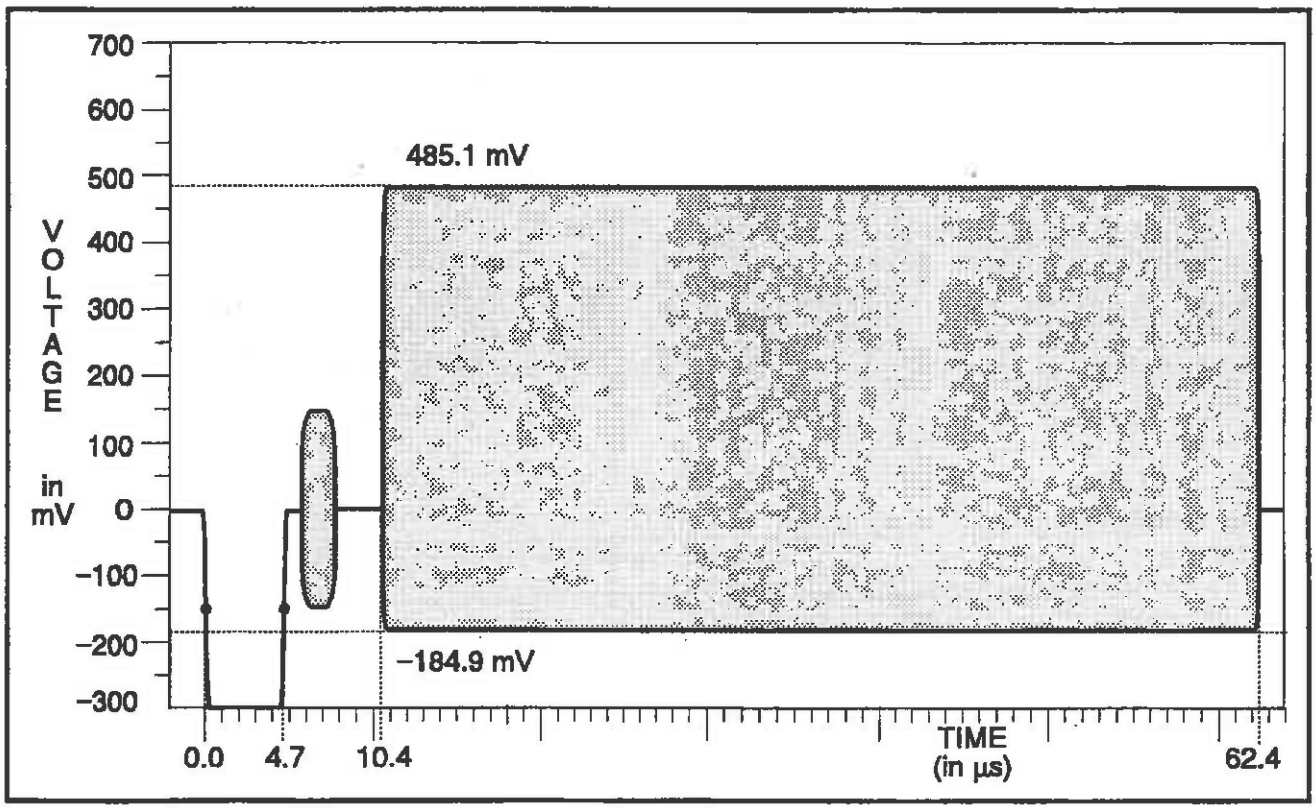


Fig. 3-4. 75% Red.

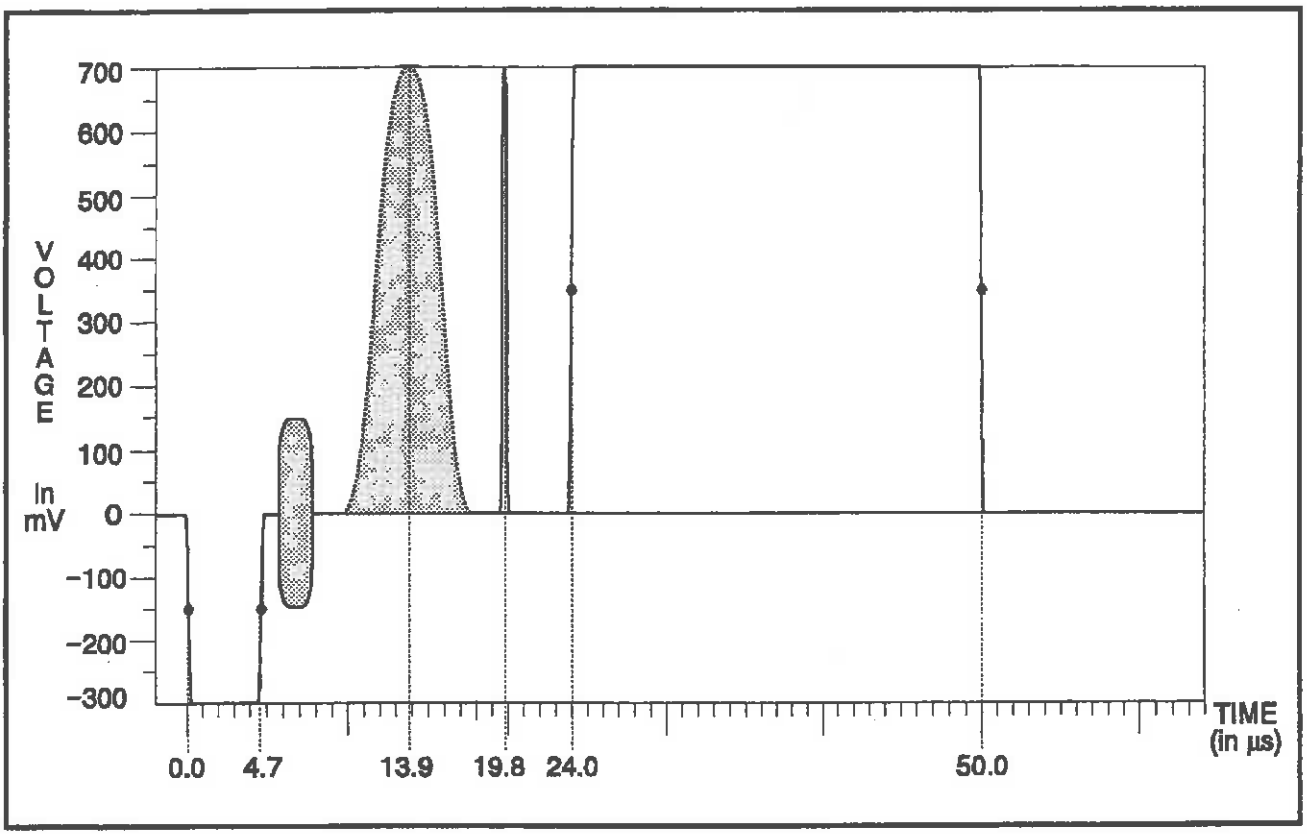


Fig. 3-5. Pulse and Bar with Window.

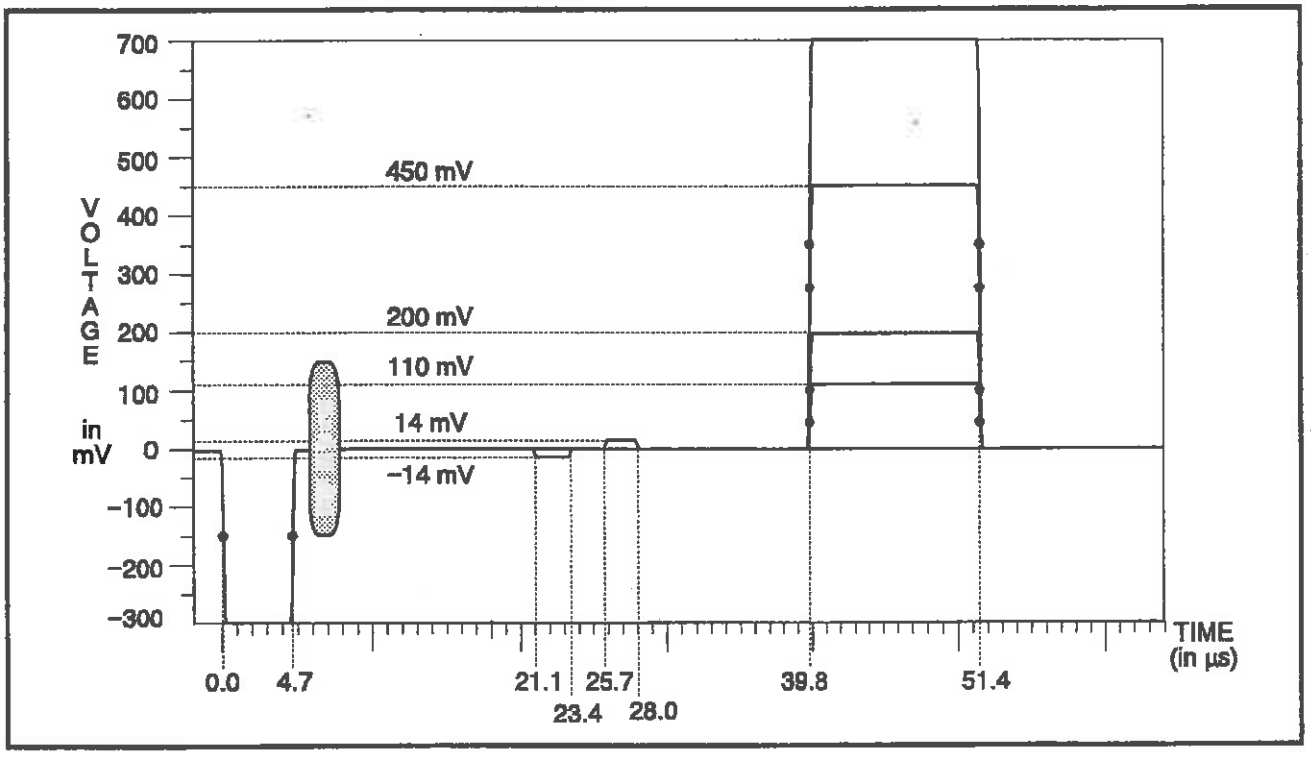


Fig. 3-6. Pluge.

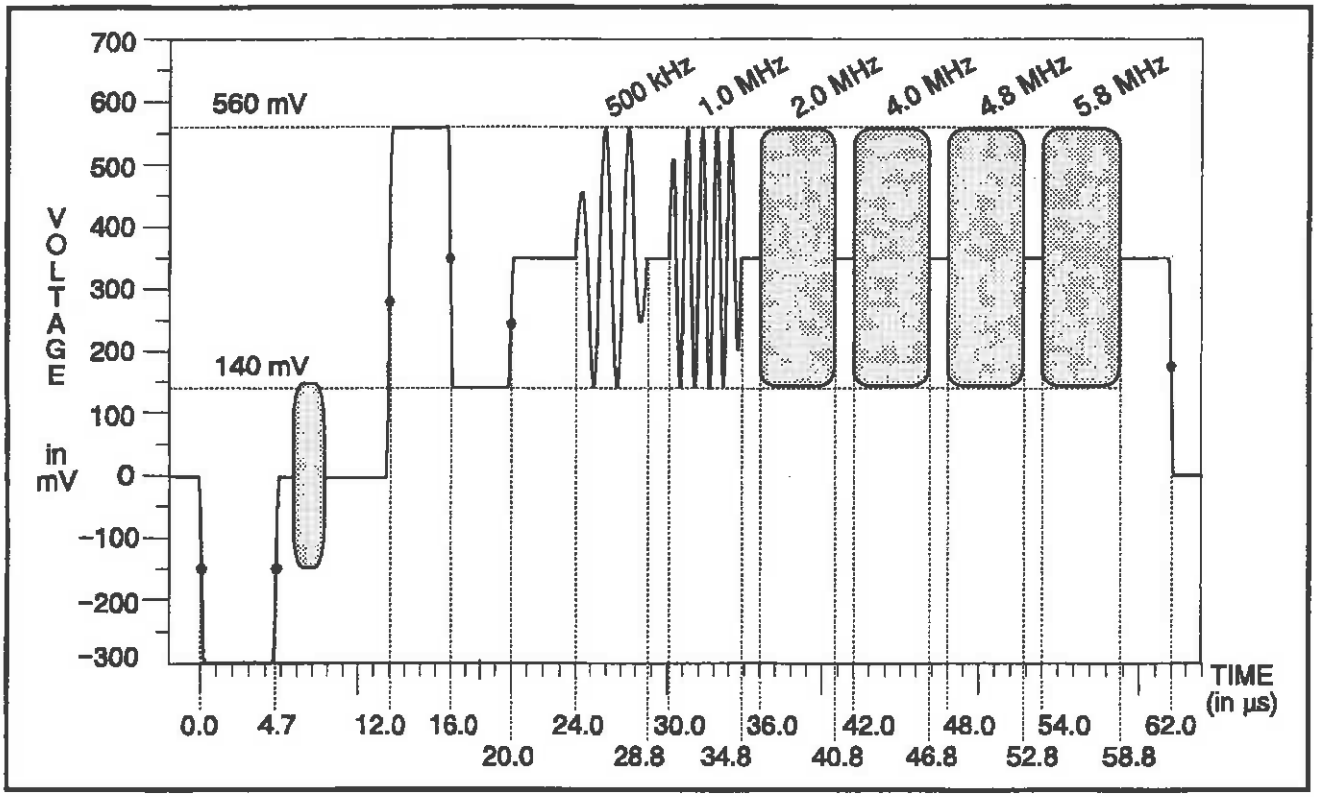


Fig. 3-7. Multiburst.

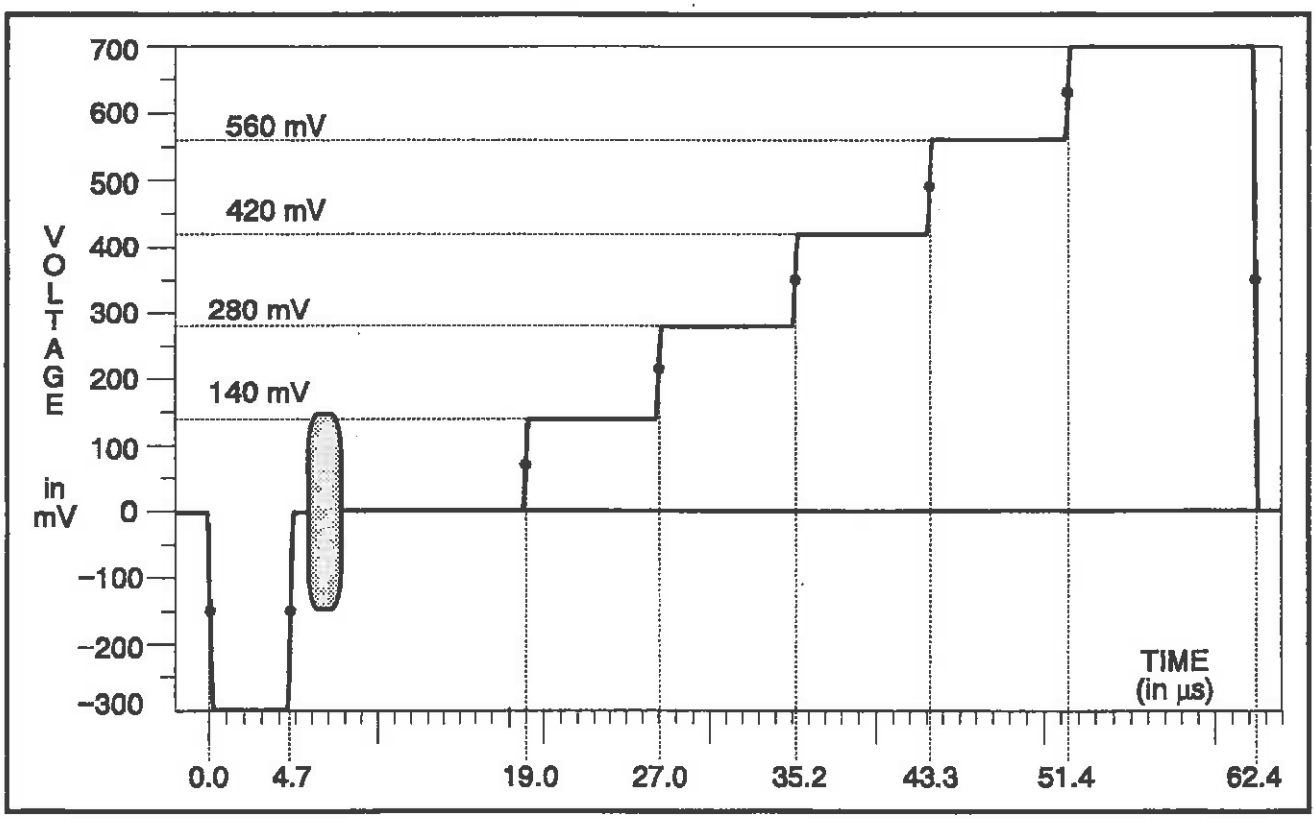


Fig. 3-8. 5-Step Gray Scale.

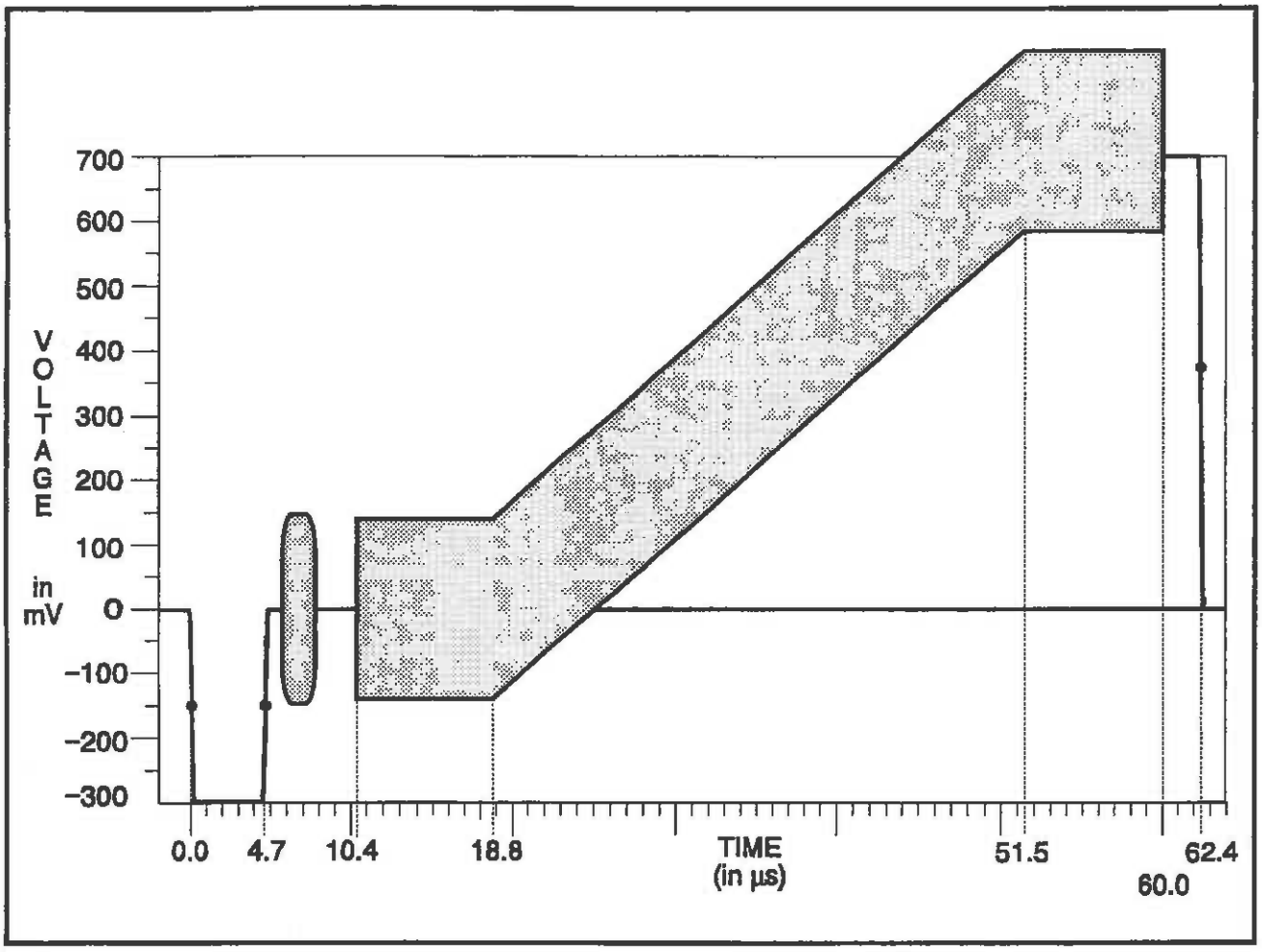


Fig. 3-9. Modulated Ramp.

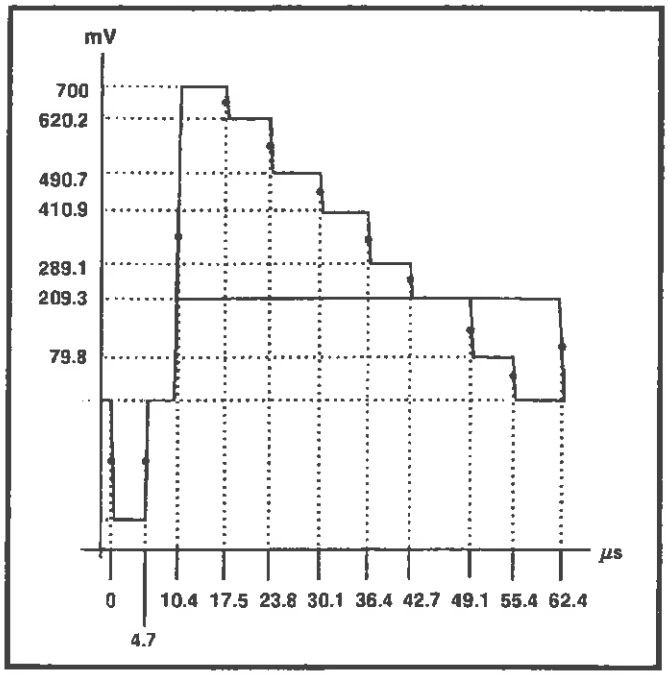


Fig. 3-10. 100% Color Bars, Y Channel over Red.

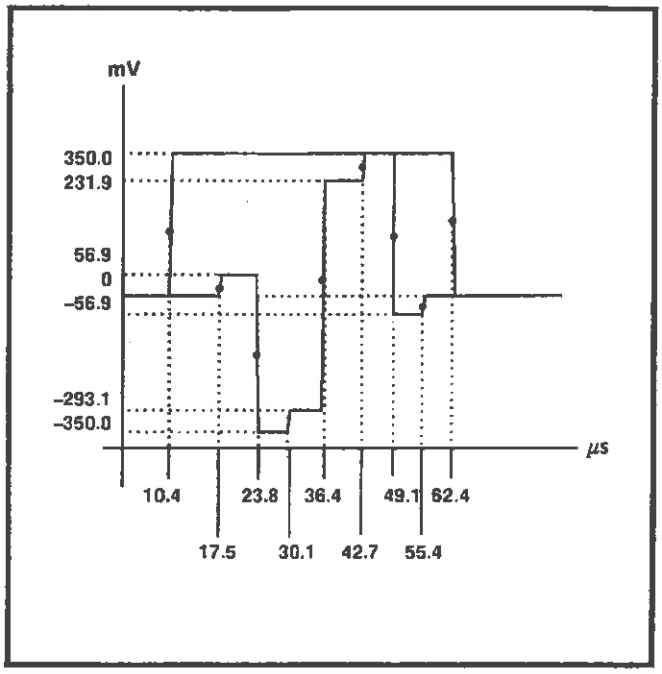


Fig. 3-12. 100% Color Bars, R–Y Channel over Red.

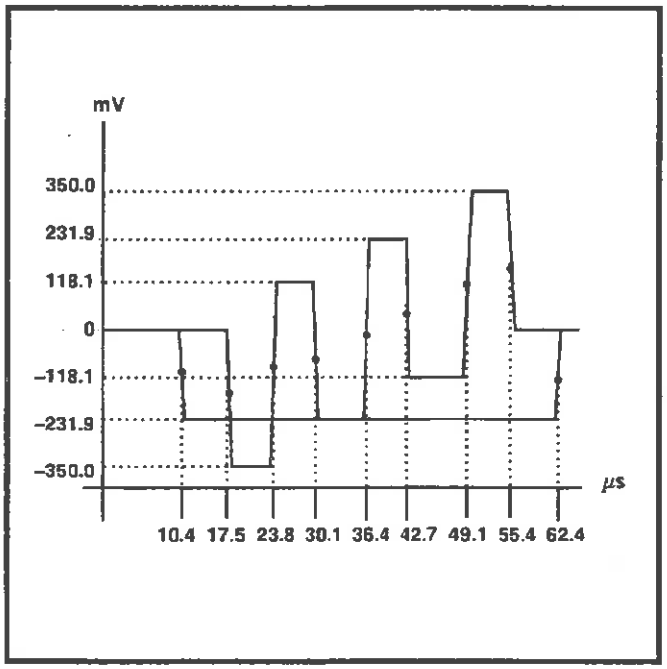


Fig. 3-11. 100% Color Bars, B–Y Channel over Red.

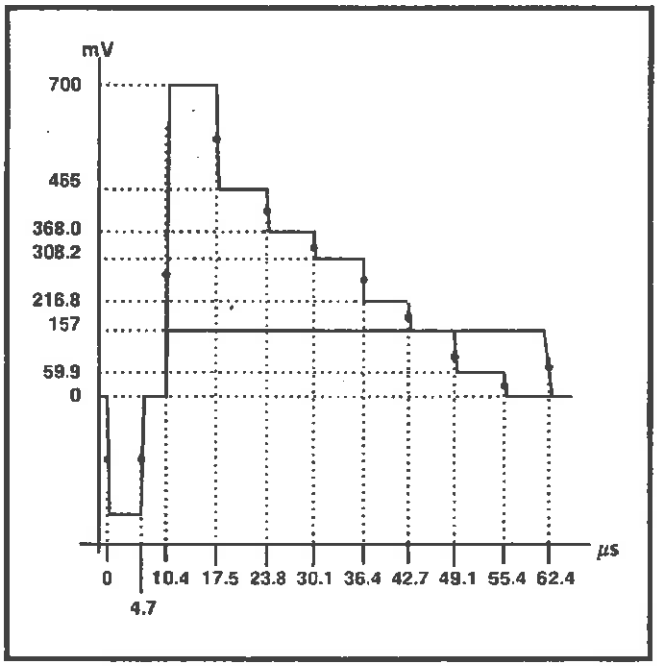


Fig. 3-13. 75% Color Bars, Y Channel.

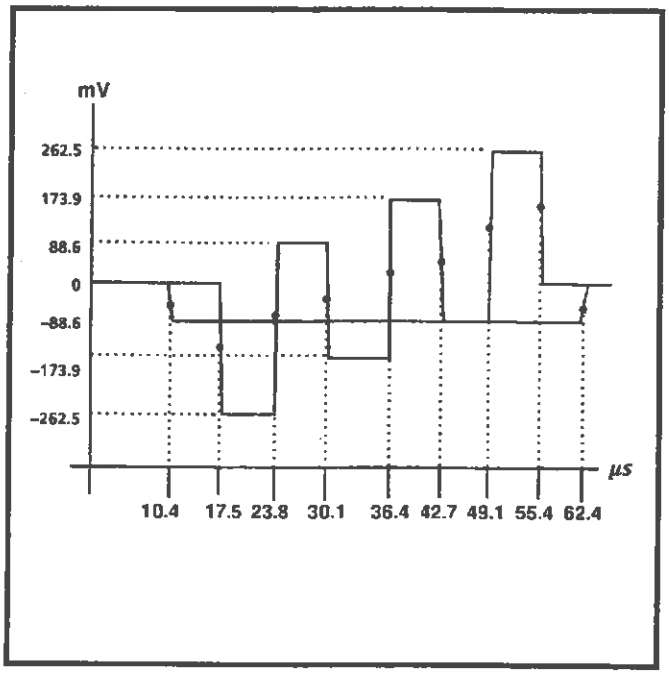


Fig. 3-14. 75% Color Bars, B–Y Channel over Red.

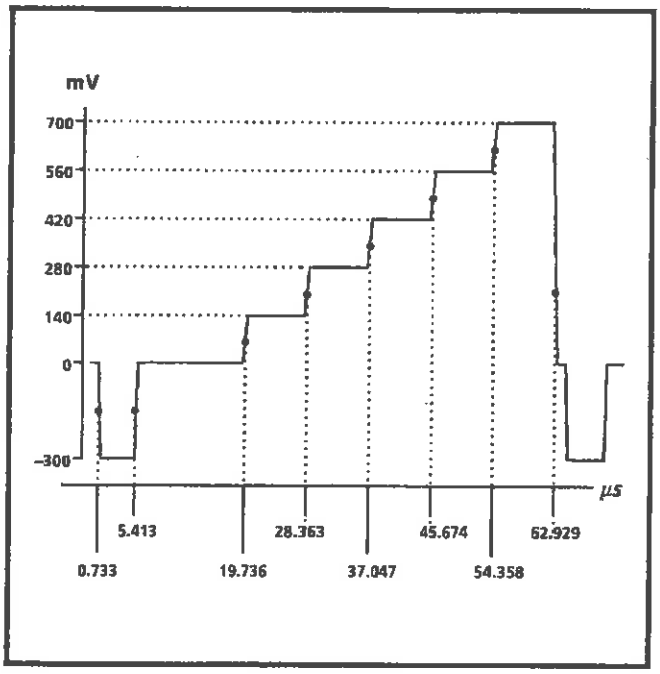


Fig. 3-16. Gray Scale.

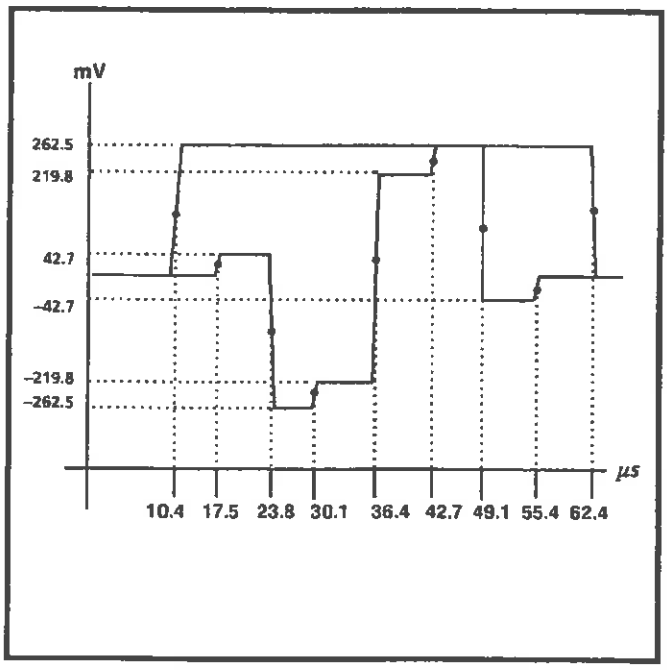


Fig. 3-15. 75% Color Bars, R–Y Channel over Red.

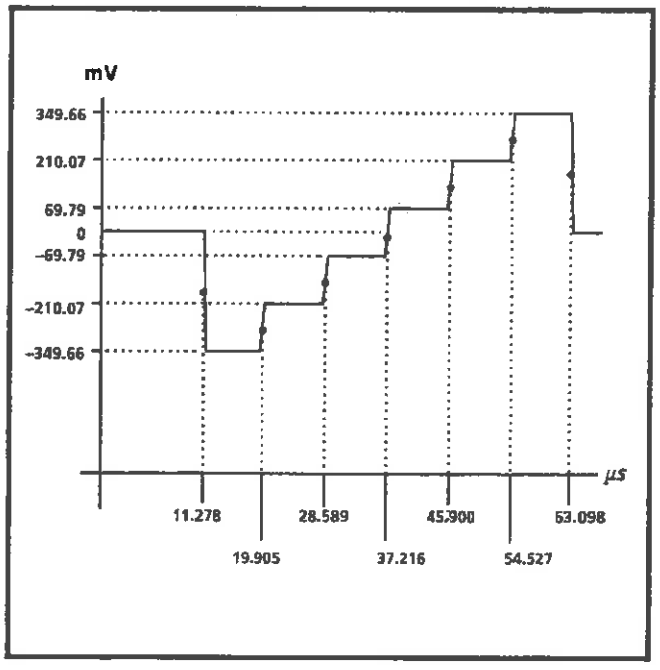


Fig. 3-17. Red–Y and B–Y.

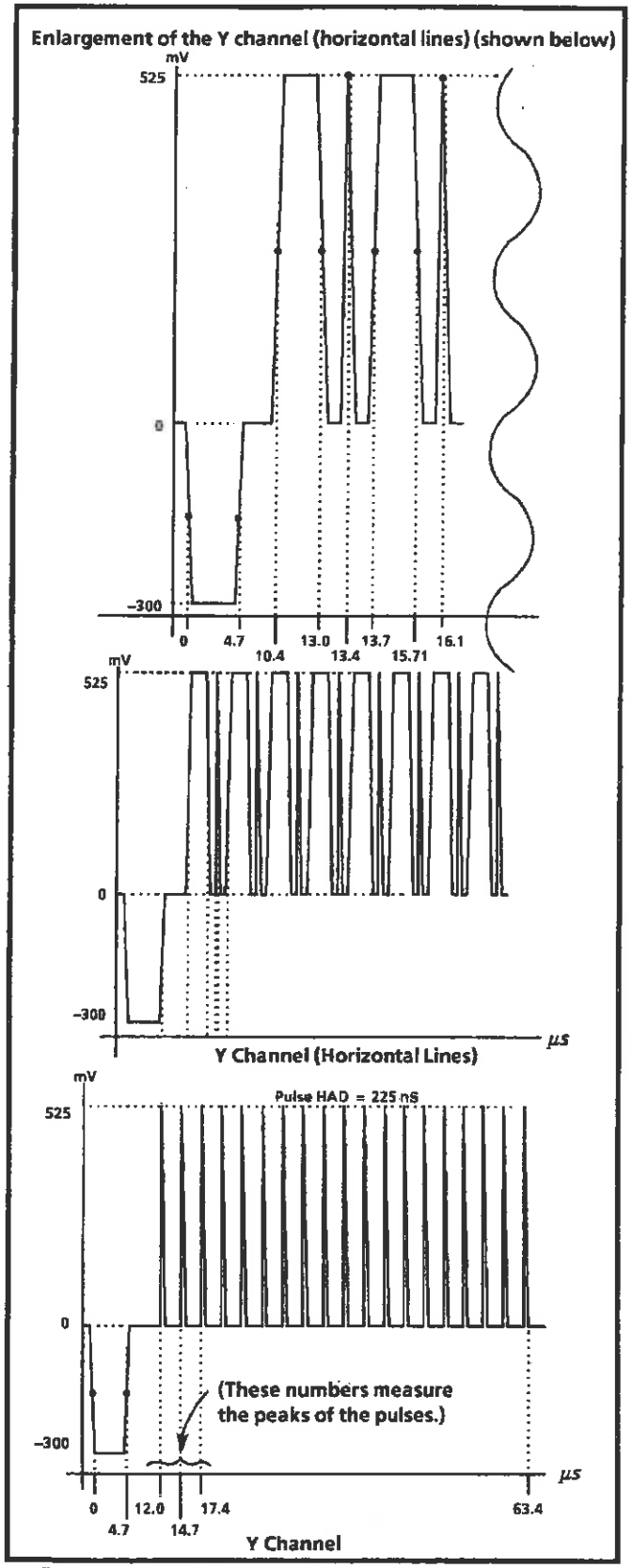


Fig. 3-18. Convergence (generated in Channel 1 only).

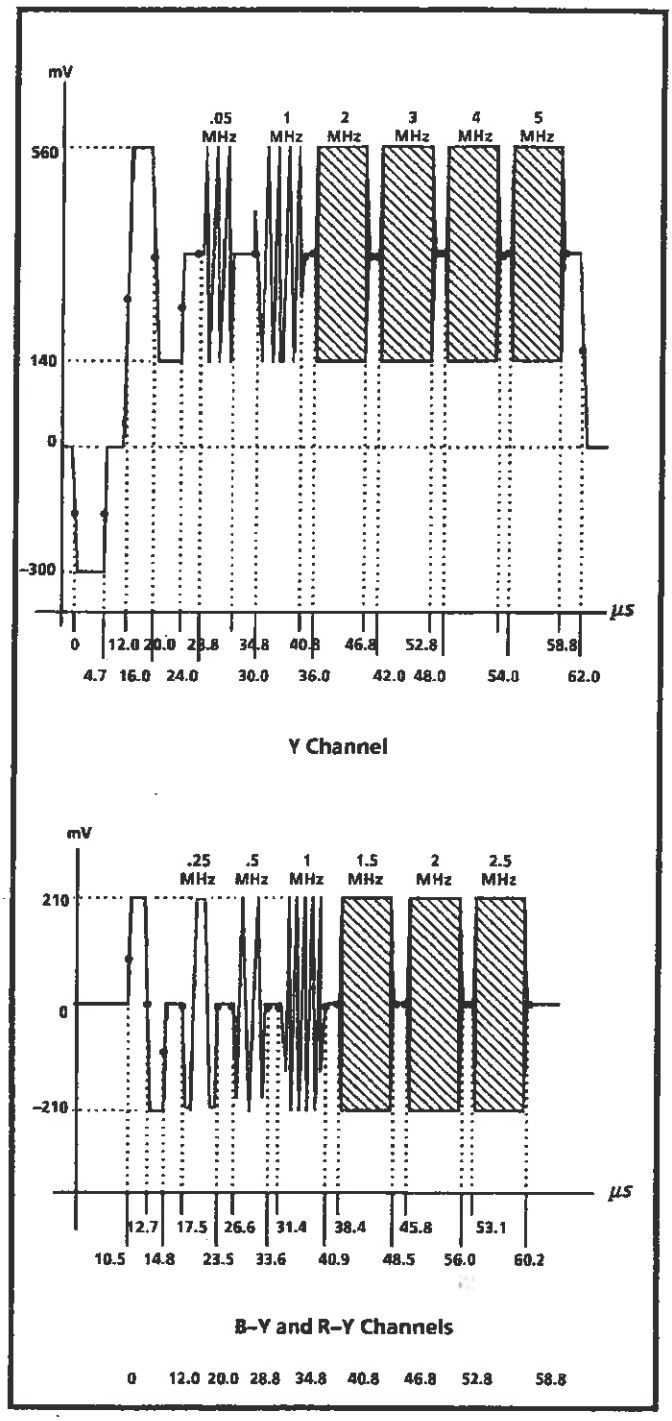


Fig. 3-19. Multiburst.

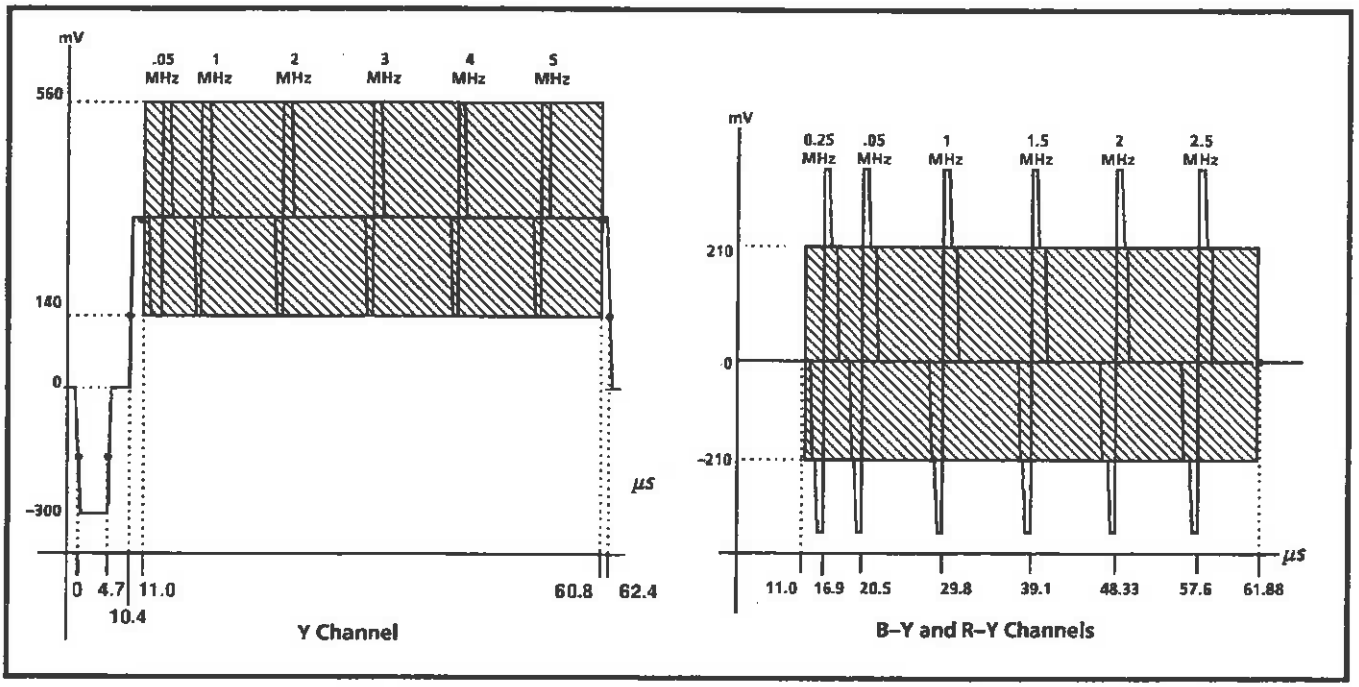


Fig. 3-20. 60% Line Sweep.

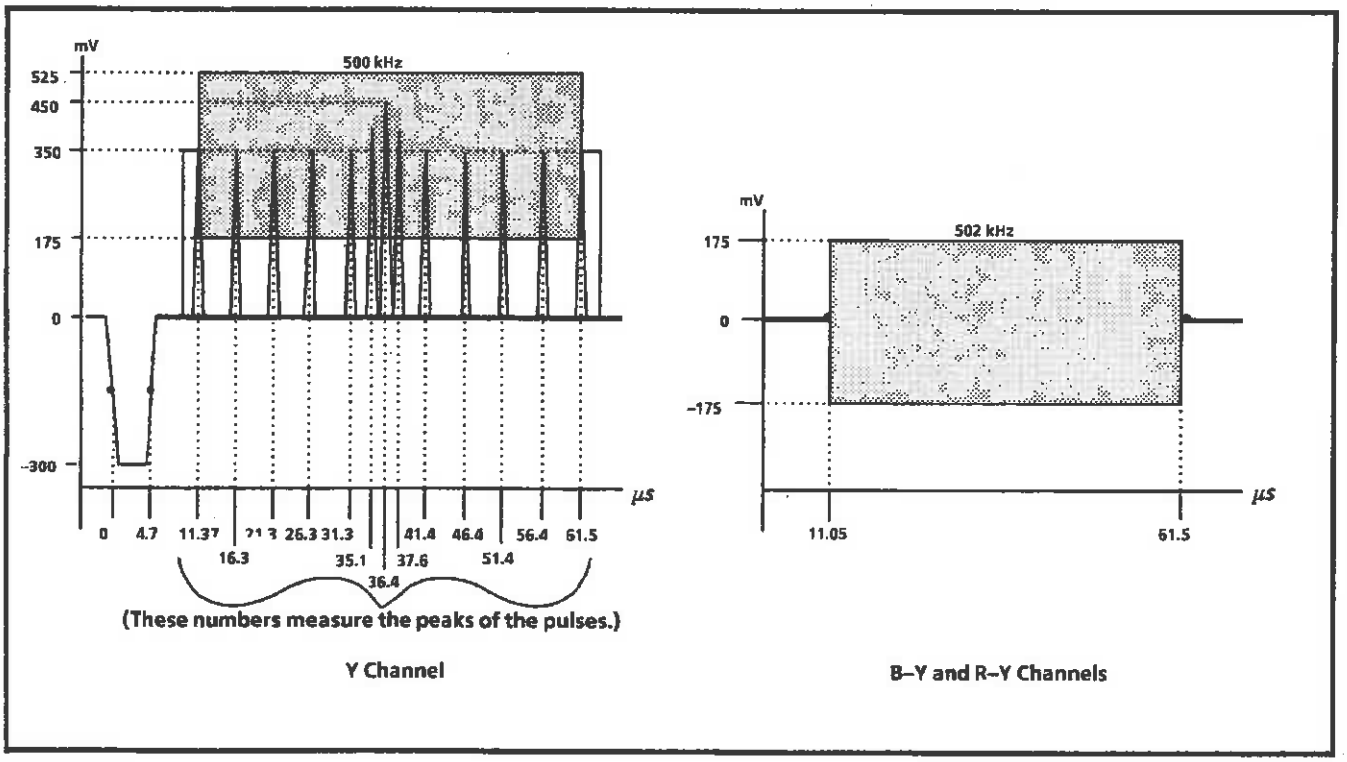


Fig. 3-221. 50% Bowtie.

Table 3-10
Power Supply

Characteristics	Performance Requirements	Supplemental Information
Supply Accuracy +12 V +5 V –5.2 V –12 V		 +12 V ±300 mV +5 V ±100 mV –5.2 V ±300 mV –12 V ±300 mV
Current Limit +12 V +5 V –5.2 V –12 V		Total power limited to 75 W.
Hum +12 V +5 V –5.2 V –12 V		**Typical** 10 mV 10 mV 20 mV 10 mV
Noise +12 V –12 V +5 V –5.1 V		 ≤50 mV (5 MHz bandwidth) ≤50 mV (5 MHz bandwidth) ≤50 mV (5 MHz bandwidth) ≤50 mV (5 MHz bandwidth)
Line Voltage Range 110 Vac 220 Vac	 90 – 132 Vac. 180 – 250 Vac.	
Crest Factor		≥1.35
Fuse Data 115 V Setting 230 V Setting		 2 A Med-Blow 1 A Med-Blow
Power Consumption Typical Maximum		 40 W 60 W
Line Frequency		48 Hz to 62 Hz

Table 3-11
Physical Characteristics

Characteristics	Information
Dimensions Rackmount Height	1.734 inches (4.4 cm).
Width	19.0 inches (48.3 cm).
Length	22.1 inches (56.1 cm).
Net Weight	13.5 lbs (6.14 kg).
Shipping Weight	22 lbs, 14 oz (10.4 kg).

Table 3-12
Environmental Characteristics

Characteristics	Information
Temperature Non-Operating	–40°C to +65°C.
Operating	0°C to +50°C.
Altitude Non-Operating	To 50,000 feet.
Operating	To 15,000 feet.
Vibration (Operating)	15 minutes each axis at 0.025 inch, frequency varied from 10-55-10 c/s in 4-minute cycles with instrument secured to vibration platform. Ten minutes each axis at any resonant point or at 55 c/s.
Shock	50 g's, 1/2 sine, 11 ms duration, 3 guillotine-type shocks per side.
Transportation	Qualified under PAL Test Procedure 1A, Category II (24-inch drop).

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

SECTION 4
INSTALLATION

PACKAGING

At installation time, save the shipping carton and packaging materials for repackaging in case reshipment becomes necessary. See Fig. 4-1.

ELECTRICAL INSTALLATION

Power Supply Frequency and Voltage Ranges

The power supply in this instrument operates over a line frequency range of 48 to 62 Hz and is set by jumper J810). The power cord option ordered determines which rating of fuse and which power supply voltage the generator is set for. Table 4-1 describes these options.

MECHANICAL INSTALLATION

Rack Mounting

The TSG 371 is shipped with hardware for rack mounting. The instrument fits in a standard 19-inch rack. Spacing between the front rails of the rack must be at least 17-3/4 inches to allow clearance for the slide-out tracks.

Rack slides conveniently mount in any rack that has a front-to-rear rail spacing between 15–1/2 and 28 inches. Six inches of clearance between the instrument's rear panel and any rear cabinet panel is required for connector space and to provide adequate air circulation.

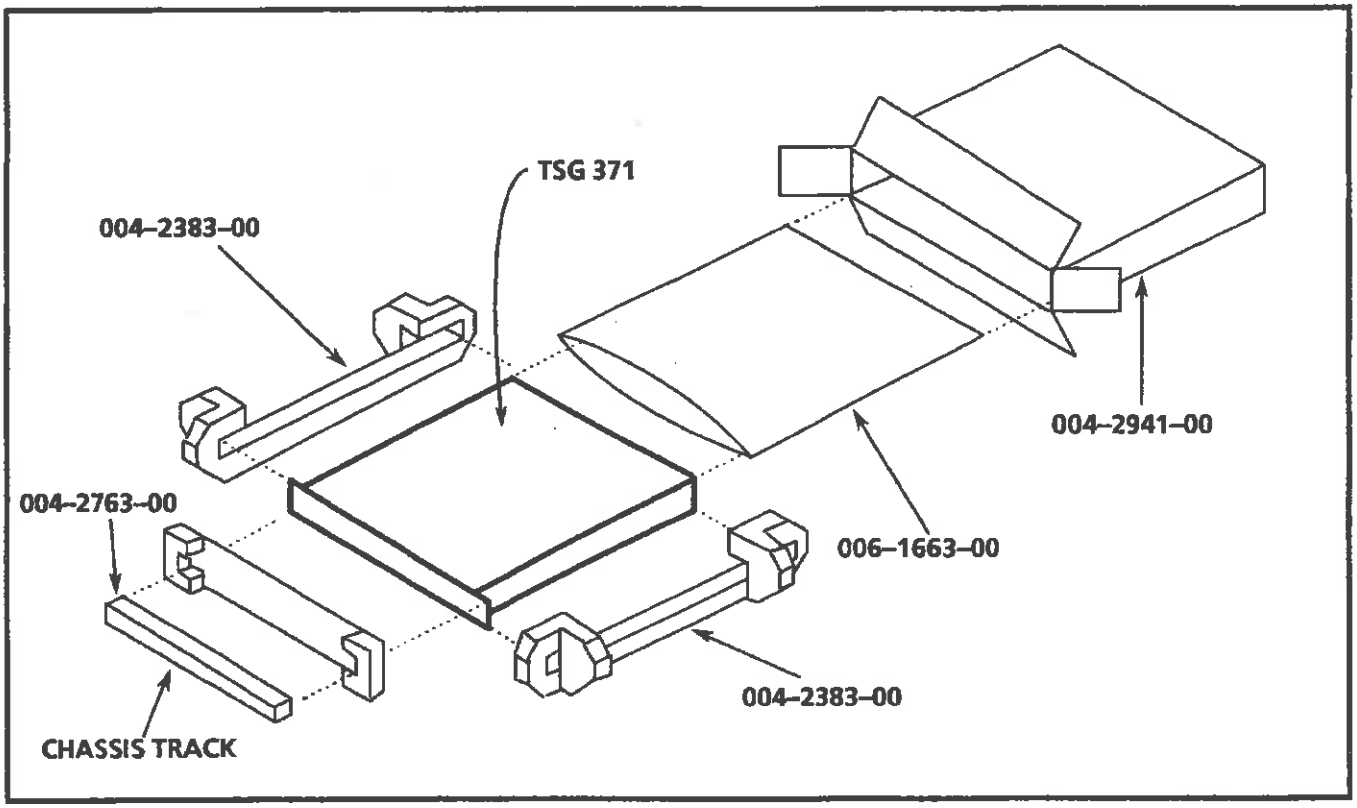


Fig. 4-1. Repacking Instructions.

Table 4-1
Jumper Settings for Power Cord Options

Power Cord Option	Fuse Rating	J810, Power Supply (115 / 230 V Select)
Option A1 (Universal Euro), Option A2 (UK), Option A3 (Australia)	1 Amp Medium Blow	Pin 1 aligned with 230 V
Standard North American	2 Amp Medium Blow	Pin 1 aligned with 115 V

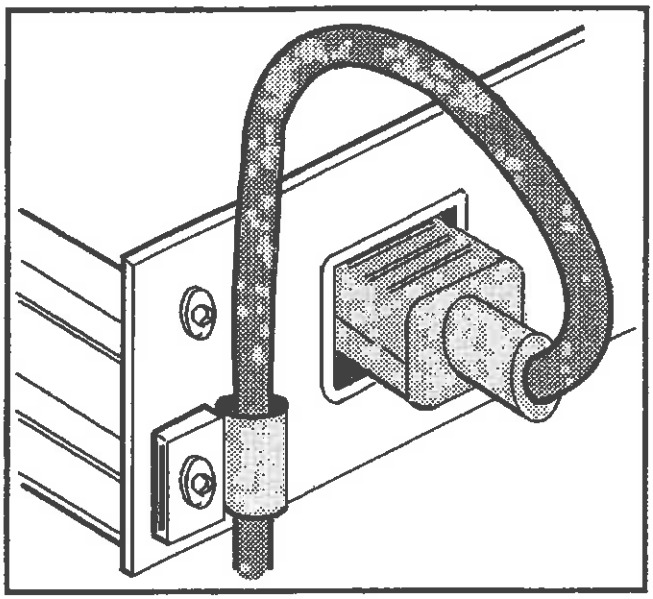


Fig. 4-2. Mounting the power cord.

Mounting the Slide Tracks

Locate the proper rack holes as shown in Fig. 4-3. Notice that the hole spacing varies with the type of rack. When installing the slides in EIA-type racks, make certain that the slides are attached to the 1/2–inch-spaced holes.

Mount the rails using enclosed hardware as shown in Fig. 4-4. Fig. 4-5 shows the rail mounting details for both deep and shallow racks. Make sure the stationary sections are horizontally aligned and are level and parallel.

Installing the Instrument

Install the instrument in the rack, as shown in Fig. 4-6.

Rack Adjustments

After installation, the slide tracks may bind if they are not properly adjusted. To adjust the tracks, slide the instrument out about 10 inches, slightly loosen the screws holding the tracks to the front rails, and allow the tracks to seek an unbound position. Retighten the screws and check the tracks for smooth operation by sliding the instrument in and out of the rack several times.

Once the instrument is in place within the rack, tighten the knurled retaining screw to fasten it securely into the rack.

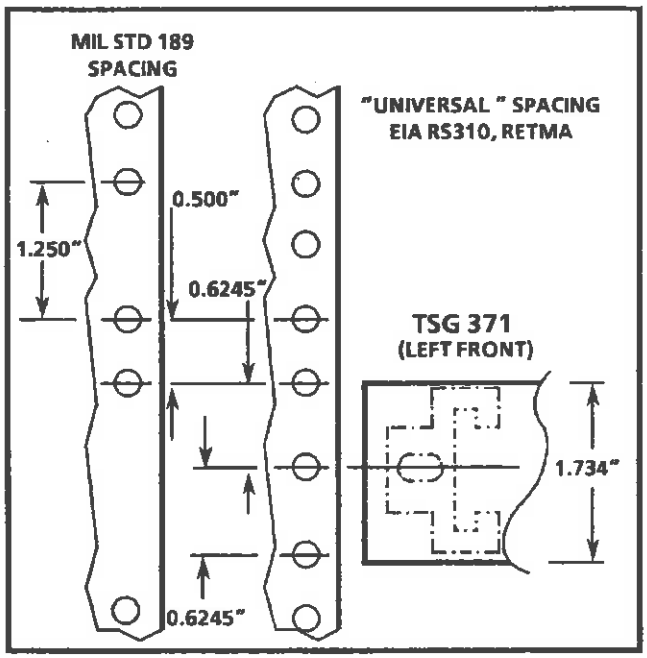


Fig. 4-3. Rail detail for mounting slide tracks.

Table 4-4
Power Supply Board (A4) Operating Mode Selection Jumpers

Function	Jumper #	Description	Factory Set
115 V/230 V Line Voltage Select	J810 <15>	Pin 1 aligned with 115 V: Power Supply accepts 115 V line voltage. Fuse rating must be 2 A, medium blow. Pin 1 aligned with 230 V: Power Supply accepts 230 V line voltage. Fuse rating must be 1 A, medium blow.	115 V

Table 4-5
Digital Board (A2–1) Test Jumpers

Function	Jumper #	Description	Factory Set
Manual Reset	J229 <2>	Pins 1–2: No reset. Pins 2–3: Resets μP.* *J2273 must be in 1–2 position.	Pins 1–2
Hard Reset	J223 <2>	Pins 1–2: Allows hard reset of μP. Pins 2–3: Forced reset of μP. Pins 3–4: Disables hard reset of μP.	Pins 1–2
VCO Test	J180 <4>	Pins 1–3: Sets VCO control voltage to mid-range (ground) so VCO can be tuned to $4F_{SC}$ with C387. Pins 2–3: μP controls genlock loop response. Pins 4–3: Fixed test voltage (–10 V) decreases VCO frequency. Pins 5–3: Fixed test voltage (+10 V) increases VCO frequency.	Pins 2–3
Crystal Oven Heater	J497 <4>	Pins 1–2: Enabled. Pins 2–3: Disabled.	Pins 1–2

Table 4-5 (cont.)
Digital Board (A2–1) Test Jumpers

Function	Jumper #	Description	Factory Set
Field Reference Disable	J570 <5>	Pins 1–2: Enables FLD REF signal to provide a genlocked field reference (field 1, line 7) pulse to the timing circuits. Pins 2–3: Disables FLD REF signal.	Pins 1–2
Luminance Disable	J551 <6>	Pins 1–2: Normal luminance. Pins 2–3: Forces luminance to 350 mV (mid-scale).	Pins 1–2
Chrominance Level	J470 <6>	Pins 1–2: Normal chrominance level. Pins 2–3: Zero chrominance level.	Pins 1–2
For Future Use	J939 <7>		No jumper installed
Offset Disable	J523 <7>	Pins 1–2: Enables 25 Hz offset. Pins 2–3: Disables 25 Hz offset.	Pins 1–2
Soft Reset Circuit Disable	J423 <2>	Pins 1–2: Enables soft reset circuit. Pins 2–3: Disables soft reset circuit.	Pins 1–2

Table 4-6
Analog Board (A3) Test Jumpers

Function	Jumper #	Description	Factory Set
Input Clamp Disable	J511 <9>	Pins 1–2: Enables clamp timing circuit. Pins 2–3: Disables clamp timing circuit.	Pins 1–2
Test Signal Disable	J440 <9>	Pins 1–2: Enables test signal at TEST SIGNAL connector and black burst at BLACK BURST connectors. Pins 2–3: Disables test signal at TEST SIGNAL connector and black burst at BLACK BURST connectors to allow for testing of return loss.	Pins 1–2

SHORT FORM PERFORMANCE CHECK

SYNC LOCK

1. Jitter
   (≤ 10 ns for Genlock Input Sync Amplitude Range of 300 mV ± 3 dB)

BURST LOCK

2. Genlock Phase vs. Input Burst/Sync Amplitude
   (≤ 1° change for nominal ± 3 dB;
   ≤ 2° change for nominal ± 6 dB.)

3. Genlock Phase vs. Input Frequency
   (≤ 1° change from 4.433599 MHz to 4.433639 MHz)

4. Genlock Phase vs. Input APL
   (≤ 1° change from 10% to 90% APL.)

GENLOCK AND SYNC TIMING

5. Genlock Advance and Delay Ranges (Coarse) for both Composite and Component Signals
   (7 µs)

6. Sync Advance and Delay Ranges
   (3.5 µs, coarse)
   (50°, fine)

7. Vertical Timing Range
   (0, 1, and 2 line advance or 1 line delay)

8. Genlock Timing Range (Fine)
   (55°)

BLANKING LEVELS

9. TEST SIGNAL Blanking Level
   (0 V ± 50 mV)

10. BLACK Blanking Level
    (0 V ± 5 mV)

11. Component Blanking Level
    (0 V ± 50 mV)

PULSE OUTPUTS

12. Sync Amplitude
    (2.0 V ± 200 mV)

13. Sync Rise and Fall Times
    (250 ns ± 50 ns)

SIGNAL AMPLITUDE LEVELS

14. BLACK Sync Amplitude
    (300 mV ± 3 mV)

15. BLACK Burst Amplitude
    (300 mV ± 6 mV)

16. TEST SIGNAL Sync Amplitude
    (300 mV ± 3 mV)

17. TEST SIGNAL Luminance Amplitude Accuracy
    (700 mV ± 7 mV)

18. TEST SIGNAL Burst Amplitude
    (300 mV ± 6 mV)

19. Componet Luminance Amplitude Accuracy
    (700 mV ± 7 mV)

20. Component Sync Amplitude
    (300 mV ± 3 mV)

21. Component Amplitude
    (±1% of 100% amplitude)

22. Linearity Error
    (±1%)

23. Field Tilt
    (≤ 0 .5%)

24. Line Tilt
    (≤ 0.5%)

25. Pulse-to-Bar Ratio
    (1:1 ± 0.5%)

CHANNEL MATCHING

26. Amplitude
(0.5% between channels referenced to channel Y)

27. Timing
(Within 5 ns relative to Y Channel)

28. Component to Composite Timing Error
(< 25 ns)

SIGNAL CHROMINANCE CHARACTERISTICS

29. BLACK Phase Matching
(within ± 2°)

30. Component Frequency Response
(Y channel: 1% flatness to 5 MHz,
2% flatness to 5.5 MHz
R-Y and B-Y channels: 1% flatness to 2.5 MHz)

31. TEST SIGNAL Chrominance-to-Luminance Delay
(≤ 5 ns)

32. Differential Gain
(6% maximum)

33. Differential Phase
(0.3° maximum)

34. TEST SIGNAL Ringing
(≤ 7 mV)

35. TEST SIGNAL Frequency Response
(± 7 mV to 5 MHz)

36. TEST SIGNAL Chrominance-to-Luminance Gain
(≤ 9.8 mV)

RETURN LOSS

37. GENLOCK loop-through
(≥ 40 dB to 5 MHz)

38. TEST SIGNAL, Component, and BLACK Outputs
(≥ 36 dB to 5 MHz)

39. SYNC and BLANKING Outputs
(≥ 30 dB to 5 MHz)

LONG FORM PERFORMANCE CHECK

SYNC LOCK

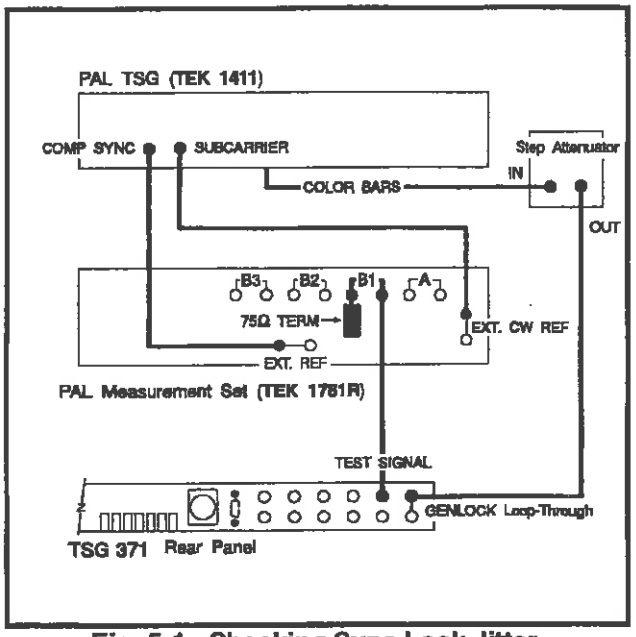


Fig. 5-1. Checking Sync Lock Jitter.

1. Jitter

a. Connect test equipment as in Fig. 5-1.

b. Select Color Bars with no burst from the PAL TSG and 75% Color Bars from the TSG 371.

c. Use the 1781R PHASE SHIFT mode and variable Vector gain to normalize one of the burst vectors to the 0° position on the vector graticule. Press REFERENCE SET to zero the readout.

NOTE

To obtain the range of signal levels required for the following tests, the GENLOCK loop-through of the TSG 371 must remain ***UN-terminated****. This results in an input signal which is 6 dB above nominal levels, or 6dB above that indicated by the Step Attenuator. Subtracting the Attenuator reading from +6 will yield the true signal change, in dB, from nominal. Setting the Step Attenuator to read 6 (indicating 6 dB attenuation), then, results in a normal signal level.*

d. Set the step attenuator to read 3 (+ 3 dB signal).

e. CHECK — for ≤ 16° (10 ns) of jitter.

f. Set the step attenuator to read 9 (– 3 dB signal).

g. CHECK — for ≤ 16° (10 ns) of jitter.

BURST LOCK

2. Jitter and Phase Shift with Change in Incoming Amplitude

a. Restore burst to the Color Bars signal at the PAL signal generator.

b. With the attenuator set to 6 (nominal signal level), confirm that the TSG 371 burst vector remains normalized to 0° dϕ.

c. Set the step attenuator to read 0 (+ 6 dB).

d. CHECK — for typical jitter of ≤ 0.4° and for ≤ 2° burst phase change.

e. Set the step attenuator to read 3 (+ 3 dB).

f. CHECK — for typical jitter of ≤ 0.3° and for ≤ 1° burst phase change.

g. Set the Step Attenuator to read 9 (– 3 dB).

h. CHECK — for typical jitter of ≤ 0.3° and for ≤ 1° burst phase change.

i. Set the step attenuator to read 12 (– 6 dB).

j. CHECK — for typical jitter of ≤ 0.4° and for ≤ 2° burst phase change.

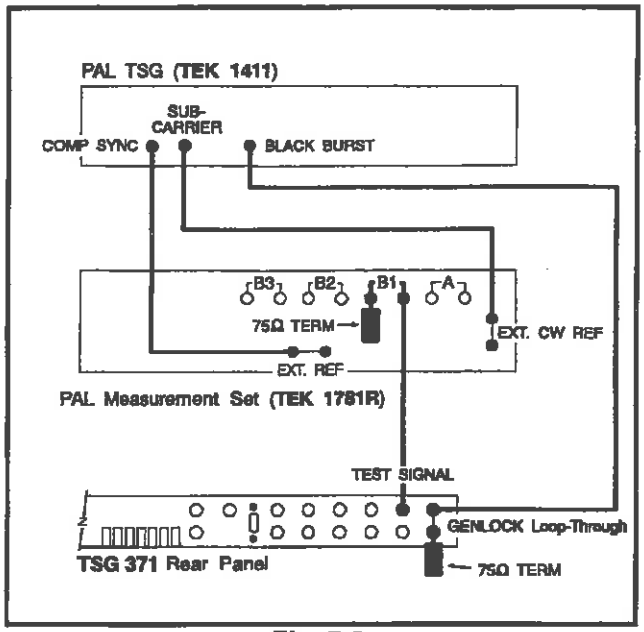


Fig. 5-2.
Setup to check burst phase shift with change in incoming burst frequency and phase shift with change in incoming APL.

3. Burst Phase Shift with Change in Incoming Burst Frequency

a. Replace the Color Bars signal to the TSG 371 GENLOCK Input with a Black Burst signal. Bypass the step attenuator and connect a termination to the TSG 371 GENLOCK loop-through (see Fig. 5-2).

b. Confirm that the Test Signal burst vector remains normalized to 0° dϕ. Readjust the 1781R if necessary.

c. Offset the frequency of the Black Burst Genlock input by + 20 Hz.

d. CHECK — that the TSG 371 re-acquires lock, and that burst phase has shifted ≤ 1°.

e. Offset the Genlock input frequency by – 20 Hz.

f. CHECK — that the TSG 371 re-acquires lock, and that burst phase has shifted ≤ 1°.

g. Reset the input frequency to zero offset.

4. Phase Shift with Change in Incoming APL

a. Replace the Black Burst GENLOCK input with a Variable Amplitude Flat Field (or Bounce) signal.

b. Vary the Flat Field signal between 10% and 90% Peak White.

c. CHECK — for a burst phase change of ≤ 1°.

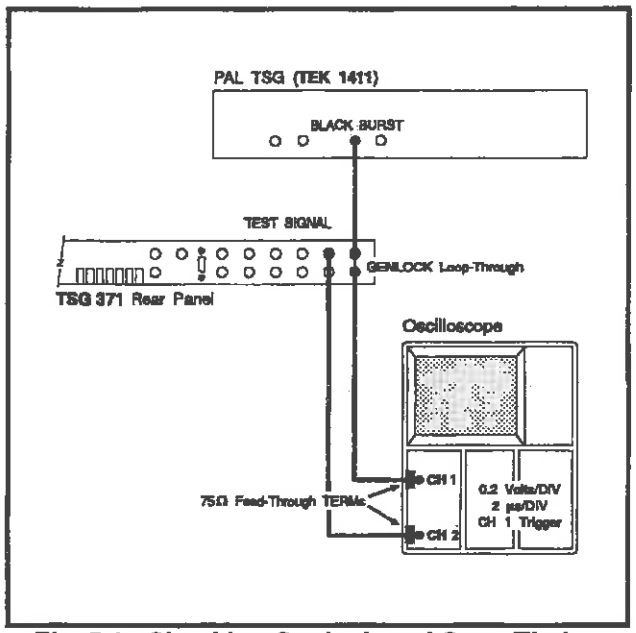


Fig. 5-3. Checking Genlock and Sync Timing Ranges.

GENLOCK AND SYNC TIMING

5. Genlock Timing Range (Coarse)

a. Connect test equipment as shown in Fig. 5-3.

b. Set the oscilloscope to display both signals at a horizontal rate. (Use Channel 1 as the trigger source.)

c. At the TSG 371 front panel, advance and delay the Test Signal output as far as it will go (with the coarse timing buttons).

d. CHECK — that the Test Signal advances and delays approximately 7 µs relative to the GENLOCK input (Black Burst) signal.

e. Replace the TEST Signal with Y and repeat steps c and d.

f. Replace the Y with B-Y and repeat steps c and d.

g. Replace B-Y with R-Y and repeat steps c and d.

h. Replace R-Y with BLACK and repeat steps c and d.

6. Sync Timing Range

a. Connect the TSG 371 SYNC output to the oscilloscope in place of the BLACK.

b. At the TSG 371 front panel, advance and delay the Sync output as far as it will go.

c. CHECK — that the sync pulse advances and delays approximately 3.5 µs relative to the Black Burst input signal.

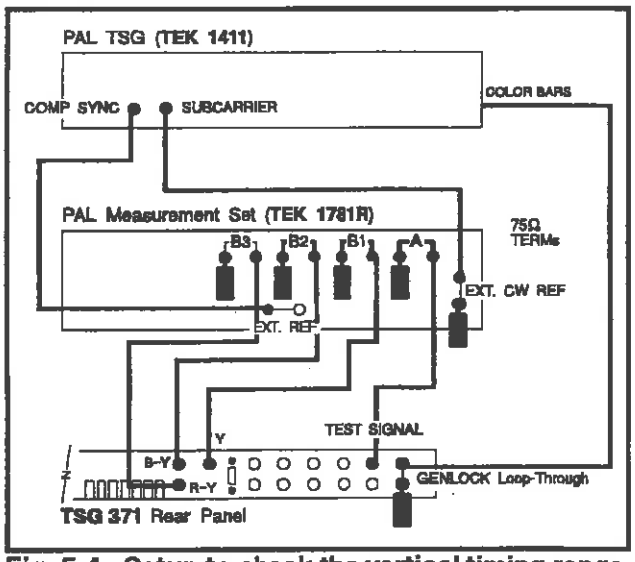


Fig. 5-4. Setup to check the vertical timing range.

7. Vertical Timing Range

a. Connect the test equipment as shown in Fig. 5-4. Select the Pluge signal from the from panel of the TSG 371.

b. Set the waveform monitor to: external reference, two field display, full horizontal magnification (display five or six lines).

c. Adjust the trace on the waveform monitor (using the Line Select feature) to display the lines where the transition between the 450 and 200 mV levels occurs.

d. Move jumpers J885 and J985 and CHECK that the lines are advanced and delayed according to the following table:

Table 5-1. Vertical timing jumper placement.

J885	J985	RESULT
1-2	1-2	0 (no change)
1-2	2-3	1 line advance
2-3	1-2	2 lines delay
2-3	2-3	1 line delay

8. Genlock Timing Range (Fine)

a. Use the same equipment setup as in the previous check, only display the signal on the vectorscope and get out of Line Select mode.

b. Select Color Bars from the TSG 371 front panel.

c. Adjust the phase control on the waveform monitor as needed to set the Color Bar vectors in their reference boxes.

d. At the TSG 371 front panel, use the Fine Advance and Delay genlock controls to advance and delay the signal as much as possible.

e. CHECK — that the FINE button advances and delays the signal about 55° on the vectorscope.

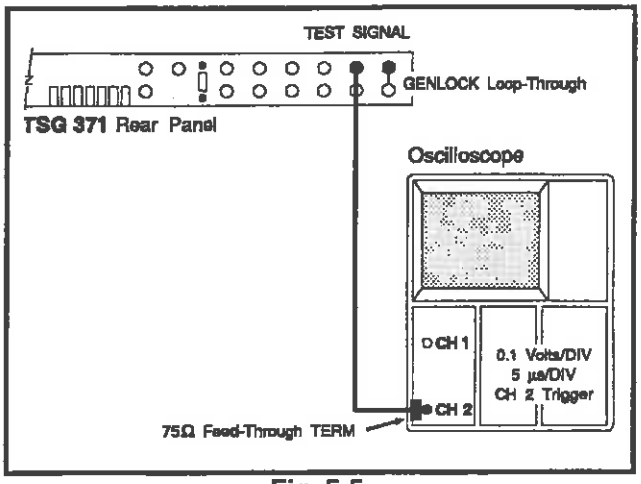


Fig. 5-5.
Checking TEST SIGNAL blanking and Pulse amplitude levels.

BLANKING LEVELS

9. Test Signal Blanking Level

a. Connect the equipment as shown in Fig. 5-5.

b. Set the oscilloscope to display and trigger off the Test Signal (CH 2).

c. Switch the oscilloscope to ground-coupled to establish a 0 V reference, then return to DC coupling and view the test signal.

d. CHECK — that the blanking level is 0 V ± 50 mV.

10. Black Blanking Level

a. Move the cable to the top BLACK output.

b. CHECK — for a blanking level (horizontal blanking interval) of 0 V ± 5 mV.

c. CHECK — for glitch amplitudes of < 10 mV.

d. Repeat steps (b) and (c) for the other BLACK outputs.

11. Component Blanking Level

a. Move the cable to the Y output.

b. CHECK — for a blanking level of 0 V ± 50 mV.

PULSE OUTPUTS

12. Amplitudes

a. Connect the TSG 371 SYNC/BLACK output to the oscilloscope.

b. Make sure that P13 is on J983 and P14 in on J982 on the Analog board.

c. Set the oscilloscope to display the SYNC/BLACK output at a line rate.

d. CHECK — that the amplitude of the SYNC/BLACK output is – 2.0 V ± 200 mV (with J780 on the Analog board in the 1-2 position) and – 4.0 V ± 400 mV (with J780 in the 2-3 position).

e. Connect the TSG 371 BLANKING/BLACK output to the oscilloscope.

f. Set the oscilloscope to display the BLANKING/BLACK output at a line rate.

g. CHECK — that the amplitude of the BLANKING/BLACK output is – 2.0 V ± 200 mV (J678 in 1-2) and – 4.0 V ± 400 mV (J678 in 2-3).

13. Rise and Fall Times

a. Set the oscilloscope to display sync transitions.

b. CHECK — that the rise and fall times (between 10%. and 90% amplitude) are 250 ns ± 50 ns.

c. Repeat for the SYNC/BLACK output.

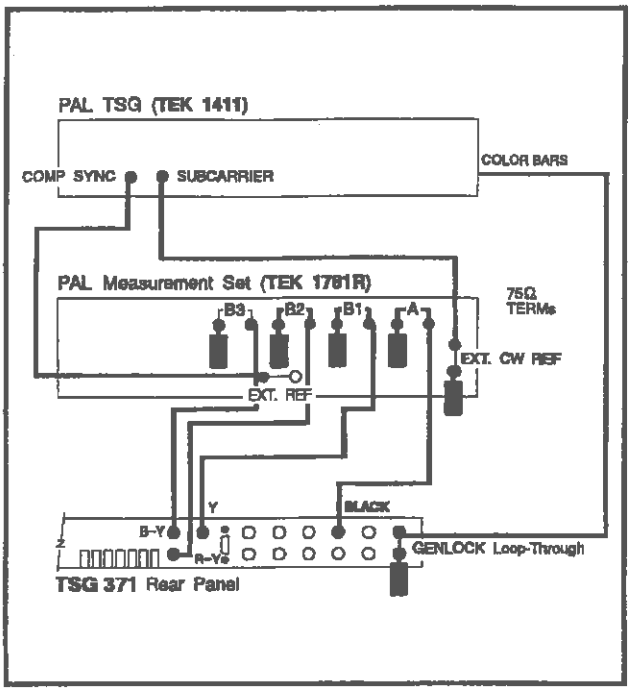


Fig. 5-6. Setup to test the BLACK output.

SIGNAL AMPLITUDE LEVELS

14. BLACK Sync Amplitude

a. Connect test equipment as in Fig. 5-6, select WFM + CAL and CH A INPUT.

b. CHECK — for a sync amplitude of 300 mV ± 3 mV (1%).

15. BLACK Burst Amplitude

a. CHECK — for a peak-to-peak burst amplitude of 300 mV ± 6 mV (2%).

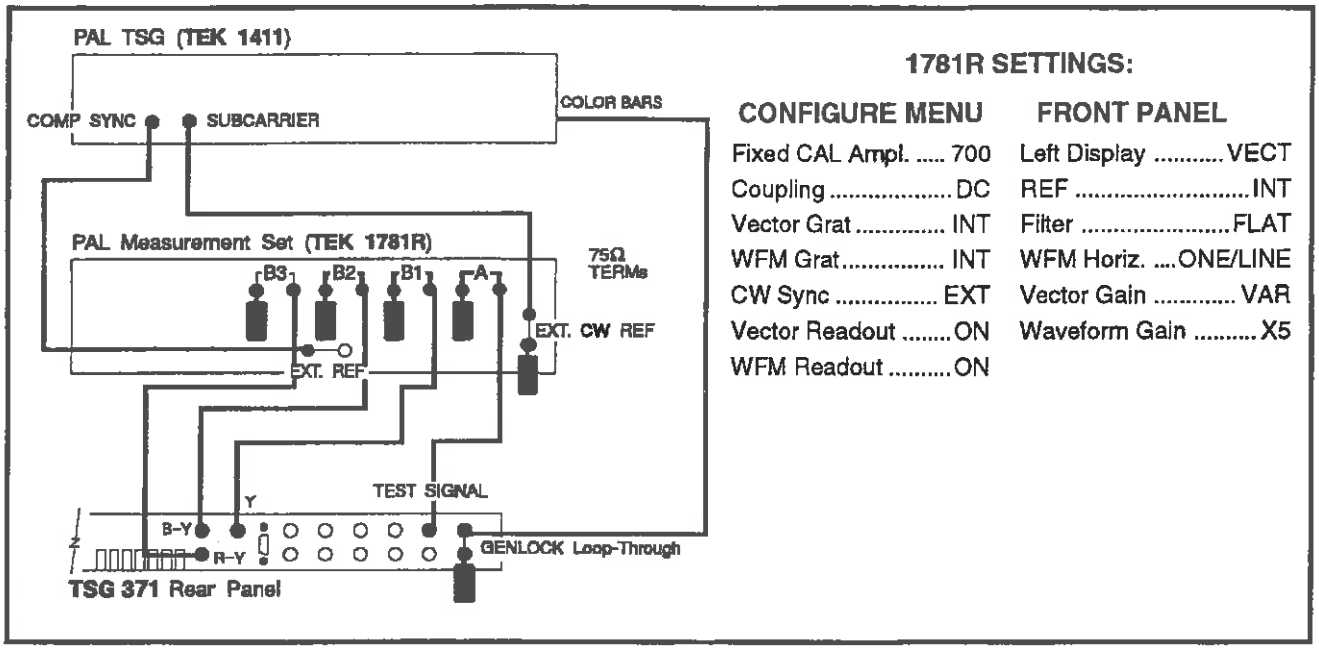


Fig. 5-7 Reference Setup for Procedures 16 through 35.

16. TEST SIGNAL Sync Amplitude

a. Replace BLACK with TEST SIGNAL (as shown in Fig. 5- 7) and select WFM + CAL Display and CH A INPUT.

b. CHECK - for a sync amplitude of 300 mV ± 3 mV (1%).

17. Test Signal Luminance Amplitude

a. Select WFM + CAL Display and CH A INPUT.

b. Select Fixed CAL (700 mV).

c. CHECK — that the White Level of the lower waveform matches the Blanking Level of the upper waveform within 7 mV.

18. TEST SIGNAL Burst Amplitude

a. CHECK — for a peak-to-peak burst amplitude of 300 mV ± 6 mV (2%).

19. Component Luminance Amplitude

a. Select WFM + CAL Display and CH B1 input (Y).

b. Select Fixed CAL (700 mV).

c. CHECK — that the White Level of the lower waveform matches the Blanking Level of the upper waveform within 7 mV.

20. Component Sync Amplitude

a. Select WFM + CAL and CH B1 input (Y).

b. CHECK — for a sync amplitude of 300 mV ± 3 mV (1%).

21. Component Amplitude

a. Select the 100% Component Bars signal from the front panel of the TSG 371 and display the B2 input (R-Y) using WFM + CAL.

b. CHECK — that the peak to peak amplitude is 700 mV ± 7mV.

c. Display the B3 (B-Y) input using WFM + CAL.

d. CHECK — that the peak to peak amplitude is 700 mV ± 7mV.

22. Linearity Error

a. Select the 5-Step Gray Scale signal from the from panel of the TSG 371 for both the composite and component signals.

b. Display CH A (TEST SIGNAL) on the waveform monitor using the DIFF filter.

c. CHECK — for < 8.5 mV variation in the step spikes.

d. Display CH B1(Y).

e. CHECK — for < 9 mV variation in the step spikes.

f. Display CH B2 (R-Y).

g. CHECK — for < 9 mV variation in the step spikes.

h. Display CH B3 (B-Y).

i. CHECK — for < 9 mV variation in the step spikes.

23. Field Tilt

a. Select the Pulse & Bar with Window signal from the from panel of the TSG 371.

b. Display CH A (TEST SIGNAL) with the filter back to FLAT at a field horizontal rate.

c. CHECK — that the window is at 700 mV ± 3.5 mV using the voltage cursor.

24. Line Tilt

a. Display CH A (TEST SIGNAL) at a line horizontal rate.

b. CHECK — that the window is at 700 mV ± 3.5 mV using the voltage cursor

25. Pulse-to-Bar Ratio

a. Display CH A (TEST SIGNAL) at a line horizontal rate using the WFM + CAL display.

b. CHECK — that both the pulse and bar are at 700 mV ± 3.5 mV and they are within 3.5 mV of each other using the voltage cursors.

CHANNEL MATCHING

26. Amplitude

a. Use the 100% component Bars as the output from the TSG 371 and put the waveform Monitor in OVERLAY displaying B1, B2, and B3.

b. Using the voltage cursor mark the peak to peak amplitude of the Y signal (disregard sync). Then set the cursors to track.

c. Move the cursors to the peaks of the B-Y signal.

d. CHECK — that the difference is < 0.5%.

e. Move the Cursors to the peak-to-peak of the R-Y signal.

f. CHECK — that the difference is < 0.5%.

27. Timing

a. Using the same equipment setup from the previous check, display the Bowtie signal.

b. Put the waveform monitor in parade, B1-B2 B1-B3 mode.

c. CHECK — that both bowties are nulled around the center timing markers as shown in Fig. 5-8.

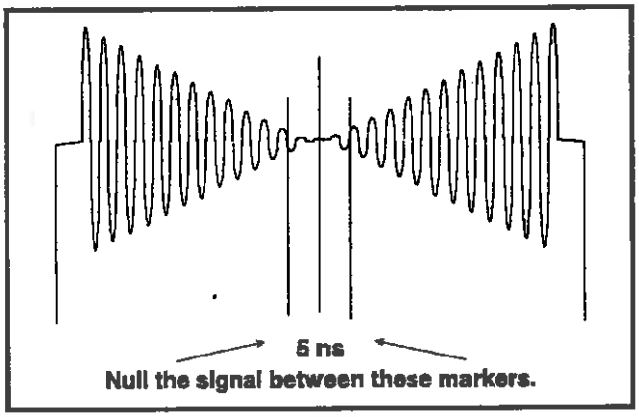


Fig. 5-8. Illustration of the bowtie.

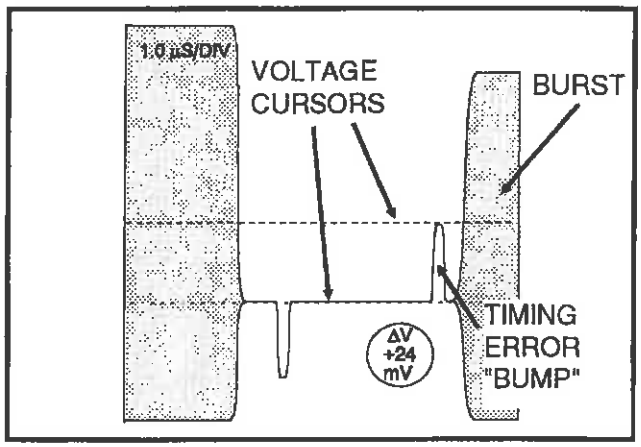


Fig. 5-9.
How to measure the composite/component timing error.

28. Component to Composite Timing Error

a. Connect the equipment as shown in Fig. 5-7. From the TSG 371 front panel, select the color bars for both composite and component.

b. Display the A-B1 mode.

c. CHECK - the display for any "bumps" or "dips" immediately before the burst. (See Fig. 5-9.) The maximum value allowed is 24 mV.

d. Set the waveform monitor to overlay CH A (TEST SIGNAL) and CH B1 (Y). Set the horizontal magnifier at maximum.

e. Display the rising edge of sync just before burst.

f. Use the voltage cursors to find the midpoint of the rising edge of sync.

g. Set the timing cursors at the midpoint of the sync as found by the voltage cursor.

h. CHECK — that the time cursors are 64.000 ± 0.025 µs apart as shown in Fig. 5-10.

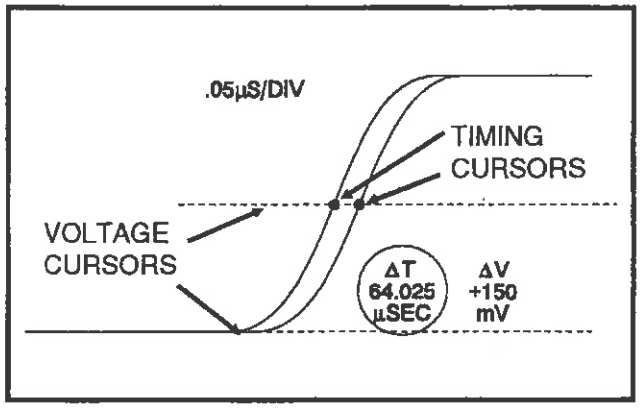


Fig. 5-10. Placement of the timing and voltage cursors.

SIGNAL CHROMINANCE CHARACTERISTICS

29. BLACK Phase Matching

a. Begin with the equipment setup shown in Fig. 5-7. Select CH A input (TEST SIGNAL).

b. Confirm that the 1781R is set to EXT CW Sync, then exit the Configure menu to view the vector display.

c. Select Phase Shift and align the burst vectors to 0° and 90° on the vector graticule. Press the Reference Set button to zero the phase. Adjust Vector Gain to normalize the 0° vector to the vector graticule.

d. At the rear panel of the TSG 371, move the cable from the TEST SIGNAL output to the lower BLACK output (see Fig. 5-11).

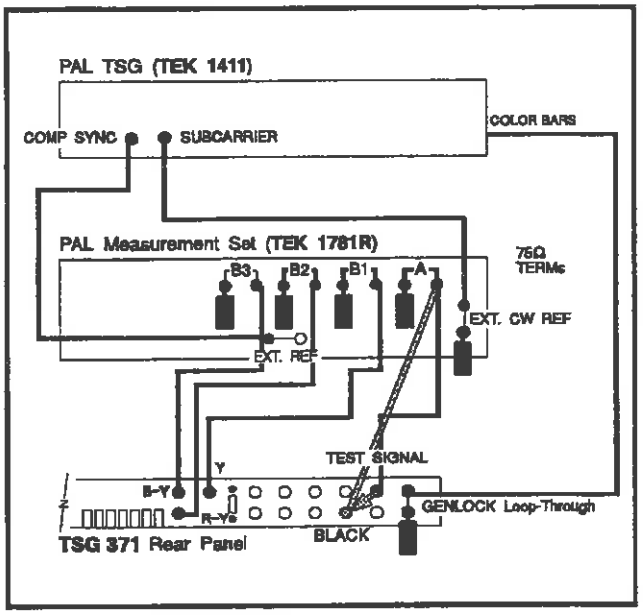


Fig. 5-11. Move the cable as shown to measure the BLACK .

e. CHECK — on the vector display, that the black burst vector is within ± 2° of the 0° graticule.

f. Repeat for the other BLACK outputs.

g. Replace BLACK with TEST SIGNAL on the waveform monitor's CH A input (return the equipment to the setup shown in Fig. 5-7).

30. Component Frequency Repsonse

a. Begin with the equipment setup in Fig. 5-7. Select the CH B1 (Y) input.

b. Select the 60% Line Sweep signal from the TSG 371.

c. CHECK — that the line sweep amplitude is flat within 1% (± 4.2 mV) out to 5 MHz (last marker).

d. CHECK — that the line sweep is flat within 2% (8.2 mV) out to the the end of the sweep (5.5 MHz).

e. Select the B2 (R-Y) input.

f. CHECK — that the line sweep is flat within 1% (4.2 mV) out to 2.5 MHz (the last marker).

g. Select the B3 (B-Y) input.

h. CHECK — that the line sweep is flat within 1% (4.2 mV) out to 2.5 MHz (the last marker).

31. TEST SIGNAL Chrominance-to-Luminance Delay

a. Select the Pulse & Bar with Window signal from the front panel of the TSG 371. Display CH A on the waveform monitor.

b. Use the 1781R and the modulated pulse to measure the Chrominance-to-Luminance Delay.

c. CHECK — that the C-Y delay is < 5 ns.

32. Differential Gain

a. Select the Modulated Ramp from the front panel of the TSG 371 and display CH A on the waveform monitor.

b. Using the 1781R to measure the Differential Gain.

c. CHECK — that the Differential Gain is < 6%.

33. Differential Phase

a. Use the 1781R to measure the Differential Phase.

b. CHECK — that the Differential Phase is < 0.3°.

NOTE

Before performing checks 34 through 36, close switches 6, 4, and 3 on S156 (Digital board) and reset the TSG 371 by turning it OFF, then back ON. This will make three diagnostic signals — Y-C test, Multipulse, and Line Sweep — available at the TEST SIGNAL output.
When the TSG 371 is in this mode, the COMPONENT BARS switch is used to choose among the three signals.

34. TEST SIGNAL Ringing

a. Begin with the equipment setup shown in Fig. 5-7. Select WFM Display and CH A input.

b. Select the Multipulse signal from the TSG 371 (with the Component BARS switch).

c. Set the waveform monitor to view the bottom of the 2T pulse.

d. CHECK — for ≤ 7.0 mV (1%) of ringing.

35. TEST SIGNAL Frequency Response

a. Select the Line Sweep signal from the TSG 371 (with the Component BARS switch).

b. CHECK — that the line sweep amplitude is 700 mV ± 7 mV (1%) out to 5 MHz (last marker).

36. TEST SIGNAL Chrominance-to-Luminance Gain

a. Connect an oscilloscope to the TEST SIGNAL output of the TSG 371 as shown in Fig. 5-12.

b. Select the DAC Test signal from the TSG 371 with the Component BARS switch (the 1781R will not lock to this signal).

c. Adjust the oscilloscope triggering to view both the 500 kHz and 4.43 MHz sine waves.

d. CHECK — that the sine wave amplitudes are equal within 9.8 mV_{p-p}.

NOTE

Before proceding, return the TSG 371 to normal operation. To disable the diagnostic signals open switches 6, 4, and 3 on S156, then turn the instrument OFF momentarily.

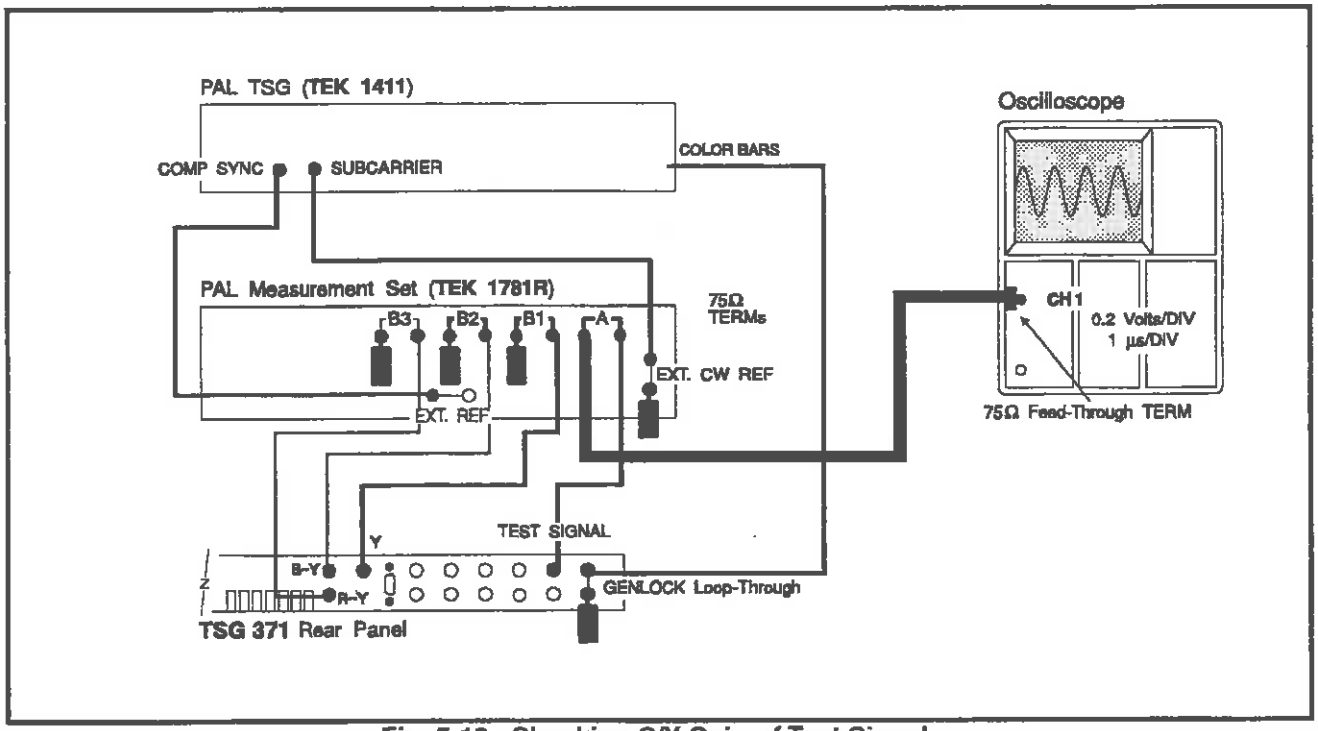


Fig. 5-12. Checking C/Y Gain of Test Signal.

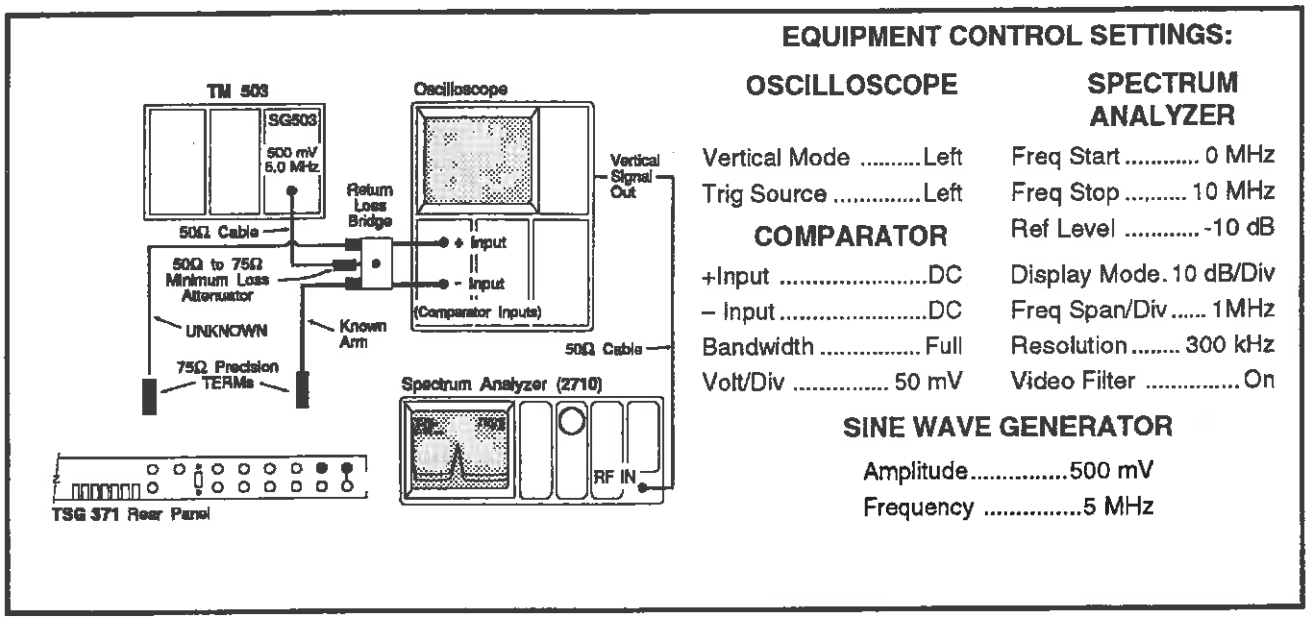


Fig. 5-13 Setup for Return Loss Measurements.

RETURN LOSS

Preparation for Return Loss Measurements

a. Connect the equipment as shown in Fig. 5-13.

b. With both precision terminators connected, adjust the Return Loss Bridge to null the 5 MHz response displayed on the spectrum analyzer.

c. Remove the terminator from the UNKNOWN cable.

d. Place the peak of the displayed 5 MHz response at the top line of the graticule by choosing "marker to reference level" from the MKR/FREQ menu of the 2710.

NOTE

All return loss checks will be measured in dB below this 5 MHz reference level.

37. GENLOCK Loop-through

a. Connect the 75Ω precision term to one of the TSG 371 GENLOCK loop-through connectors.

b. Connect the UNKNOWN cable to the other TSG 371 GENLOCK loop-though connector.

c. CHECK — that the return loss is > 40 dB (4 major divisions) as the SG503 frequency is varied between 5 MHz and 500 kHz.

38. TEST SIGNAL, Component, and BLACK Outputs

a. Move jumper J440 (Analog board) to pins 2 and 3 to disable the TEST SIGNAL.

b. Connect the UNKNOWN cable to the TEST SIGNAL output.

c. CHECK — that the return loss is > 36 dB as the SG503 frequency is varied between 5 MHz and 500 kHz.

d. Connect the UNKNOWN cable to the top BLACK output.

e. CHECK — that the return loss is > 36 dB as the SG503 frequency is varied between 5 MHz and 500 kHz.

f. Move the UNKNOWN cable to the other BLACK outputs and repeat step e.

g. Remove the UNKNOWN cable from the BLACK output and return J440 to pins 1 and 2.

h. Move Jumpers J2, J4, and J5 on the Component Board to the 2-3 position.

i. Connect the UNKNOWN cable to the Y output.

j. CHECK — that the return loss is > 36 dB as the SG503 frequency is varied between 5 MHz and 500 kHz.

k. Repeat steps i and j with the B-Y and R-Y outputs.

l. Return jumpers J2, J4, and J5 to the 1-2 position.

39. SYNC and BLANKING Outputs

a. Connect the UNKNOWN cable to the SYNC/BLACK and BLANKING/BLACK outputs in turn and, for each output, check that the return loss is > 30 dB as the SG503 is varied between 5 MHz and 500 kHz.

SHORT FORM
CALIBRATION PROCEDURES

POWER SUPPLY

1. +5 V Output (R510)

SUBCARRIER

2. Sync Timing Range Center (R469)
3. Output Frequency (C19)

DC OFFSET

4. Black and Test Signal (R322)
5. Channel 1 Y (R20)
6. Channel 2 B-Y (R37)
7. Channel 3 R-Y (R54)

SIGNAL GAIN

8. Black (R771)
9. Test Signal (R758)
10. Channel 1 Y (R19)
11. Channel 2 B-Y (R36)
12. Channel 3 R-Y (R53)

FREQUENCY RESPONSE— COMPOSITE SIGNALS

13. Black Burst Amplitude (C775)
14. Black/Test Signal Phase Matching (L751)
15. Chrominance-to-Luminance Gain (C753)

NOTE

Inductors L450, L550, L551, L650, L750, and L751 are factory set.
Only perform steps 16 and 17 if the Test Signal output cannot be brought into frequency spec using C753.

16. Test Signal Frequency Response (L450, L550, L551, L650, and L750)
17. Group Delay (L450 and L550)

FREQUENCY RESPONSE — COMPONENT SIGNALS

18. Channel 1 Fine Frequency Response (C11)
19. Channel 2 Fine Frequency Response (C32)
20. Channel 3 Fine Frequency Response (C53)

NOTE

The following inductors are factory set.
Only perform steps 21, 22, and 23 if the Component outputs cannot be brought into frequency spec.

21. Channel 1 Coarse Frequency Response (L3, L4, L5, L6, and L7)
22. Channel 2 Coarse Frequency Response (L8, L9, L10, L11, and L12)
23. Channel 3 Coarse Frequency Response (L13, L14, L15, L16, and L17)

COMPONENT INTERCHANNEL TIMING

24. Channel 1 (Y) to Channel 2 (B-Y) (C4)
25. Channel 1 (Y) to Channel 3 (R-Y) (C3)

LONG FORM
CALIBRATION PROCEDURES

NOTE

Calibration of the TSG 371 should be attempted only after the instrument has reached normal operating temperature, usually after 30 minutes warm-up.

POWER SUPPLY

NOTE

The Power Supply voltage should be adjusted only if it is out of tolerance. The adjustment is not necessary during routine maintenance.

1. +5 V Output

a. Connect power to the TSG 371 through a Variac set to 90 Volts AC.

b. Turn the TSG 371 ON.

c. Set the Variac to 115 Volts.

d. Adjust R510 (on the Power Supply board) to make the voltage at pin 24 of U667 (Digital Board) 5.00 V ± 50 mV.

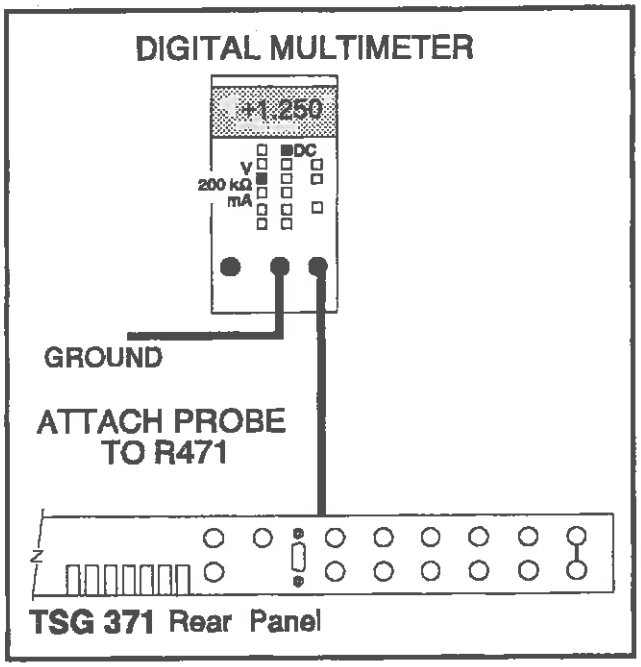


Fig. 5-14. Setup to adjust R469.

SUBCARRIER

2. Sync Timing Range Center

a. Connect the equipment as shown in Fig. 5-14.

b. Attach the probe to R471 as shown in Fig. 5-15.

c. Adjust R469 for +1.25 V on the DMM.

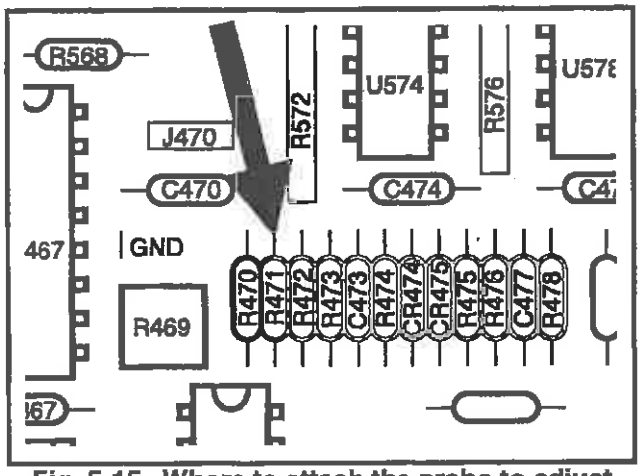


Fig. 5-15. Where to attach the probe to adjust R469.

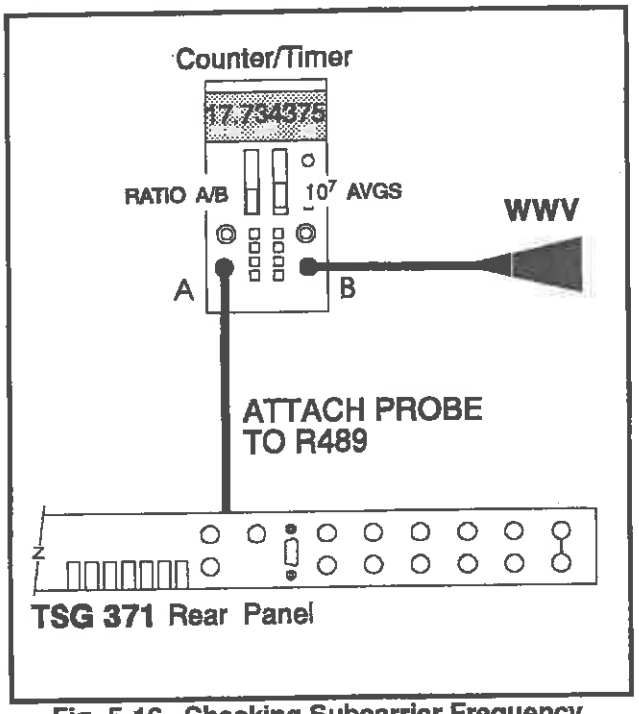


Fig. 5-16. Checking Subcarrier Frequency.

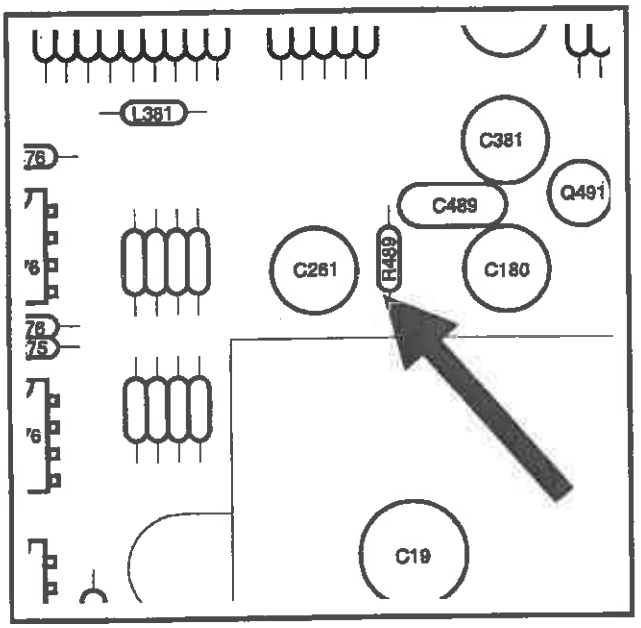


Fig. 5-17. Where to attach the probe to adjust C19.

3. **Output Frequency**

   a. Connect the equipment as shown in Fig. 5-16. Confirm that there are no connections to the TSG 371 outputs.

   b. Attach probe to R489 as shown in Fig. 5-17.

   c. Adjust C19 for a Subcarrier Frequency of 17.734375 MHz ± 1 Hz.

Steps 4 Through 17 Share the Same Basic Equipment Setup and Settings. This Reference Setup is Shown in Fig. 5-18 .

DC OFFSET

4. Test Signal and Black

a. Begin with the 1781R Reference Setup (Fig. 5-18). Select WFM display and CH A input.

b. Select 100% Color Bars from the TSG 371 composite front panel.

c. Set the 1781R to GND coupling and center the trace on the display graticule.

d. Switch back to DC coupled. Adjust R322 for a blanking level of 0 Volts ± 25 mV.

e. Replace the Test Signal with Black on CH A.

f. Check that the inserted black level is also 0 Volts ± 25 mV. Adjust R322 as needed.

5. Channel 1 (Y)

a. Begin with the 1781R Reference Setup (Fig. 5-18). Select WFM display and CH B1 input (Y).

b. Select the component 100% Color Bars from the front panel of the TSG 371.

c. Adjust R19 for a blanking level of 0 Volts ± 50 mV.

6. Channel 2 (B-Y)

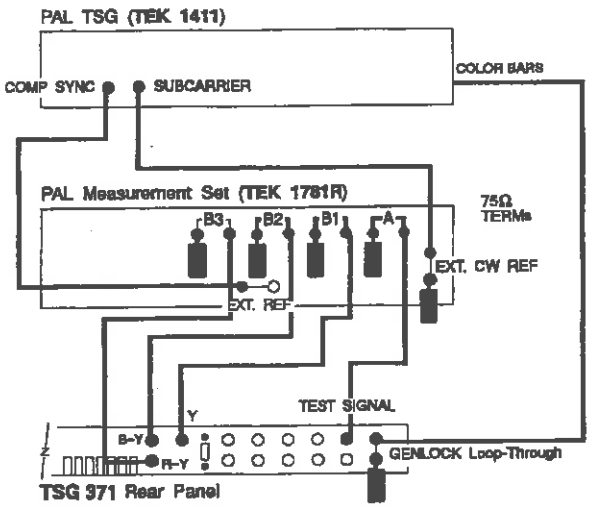
a. Begin with the 1781R Reference Setup (Fig. 5-18). Select WFM display and CH B2 input (B-Y).

b. Adjust R37 for a blanking level of 0 Volts ± 50 mV.

7. Channel 3 (R-Y)

a. Begin with the 1781R Reference Setup (Fig. 5-18). Select WFM display and CH B3 input (R-Y).

b. Adjust R53 to match the blanking levels of the Y and B-Y signals (0 Volts ± 50 mV).



1781R SETTINGS:

CONFIGURE MENU		FRONT PANEL	
Fixed CAL Ampl.	700	Left Display	VECT
Coupling	DC	REF	INT
Vector Grat	INT	Filter	FLAT
WFM Grat	INT	WFM Horiz.	ONE/LINE
CW Sync	EXT	Vector Gain	VAR
Vector Readout	ON	Waveform Gain	X5
WFM Readout	ON		

Fig. 5-18 Reference Setup for Procedures 4 through 14.

SIGNAL GAIN

8. Black

a. Begin with the 1781R Reference Setup (Fig. 5-18). Replace TEST SIGNAL with BLACK at the CH A input.

b. Select WFM + CAL display and CH A input (BLACK).

c. Set CAL to 300 mV.

d. Adjust R771 to match the sync tip of the upper waveform to the blanking level of the lower.

9. Test Signal

a. Begin with the 1781R Reference Setup (Fig. 5-18). Replace BLACK with TEST SIGNAL on CH A. Select WFM + CAL display and CH A input (TEST SIGNAL).

b. Select Fixed CAL (700 mV).

c. Adjust R758 to match the White Level of the lower waveform to the Blanking Level of the upper (700 mV).

10. Channel 1 (Y)

a. Begin with the 1781R Reference Setup (Fig. 5-18). Select WFM + CAL Display and CH B1 INPUT.

b. Select Fixed CAL (700 mV).

c. Adjust R19 to match the White Level of the lower waveform to the Blanking Level of the upper.

11. Channel 2 (B-Y)

a. Begin with the 1781R Reference Setup (Fig. 5-18). Select WFM + CAL Display and CH B1 INPUT.

b. Select Fixed CAL (700 mV).

c. Adjust R36 to match the peak of the lower waveform to the valley of the upper.

12. Channel 3 (R-Y)

a. Begin with the 1781R Reference Setup (Fig. 5-18). Select WFM + CAL Display and CH B1 INPUT.

b. Select Fixed CAL (700 mV).

c. Adjust R53 to match the peak of the lower waveform to the valley of the upper.

FREQUENCY RESPONSE — COMPOSITE SIGNALS

13. Black Burst Amplitude

a. Begin with the 1781R Reference Setup (Fig. 5-18). Replace the Test Signal with Black to the CH A input. Select WFM + CAL Display and CH A INPUT.

b. Set CAL to 300 mV.

c. Adjust C775 to match the bottom of the upper burst to the top of the lower on the right display.

14. Black/Test Signal Phase Matching

a. Display the Black on the vectorscope using EXT CW REF.

b. Normalize the vector so that it extened to the edge of the graticule and adjust the phase to align the vector on a graticule.

c. Remove the Black from the CH A input and replace it with Test Signal.

d. Adjust L751 so that the vector aligns on the same graticule as the Black signal.

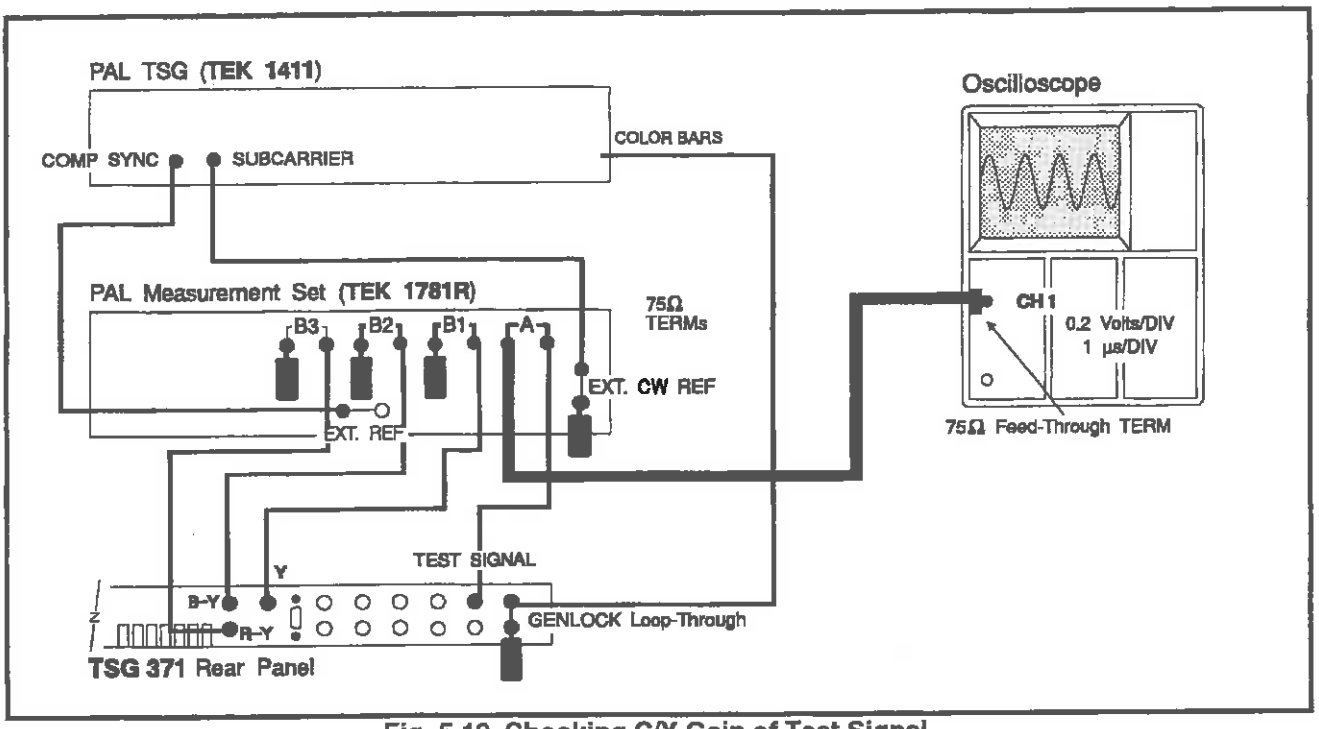


Fig. 5-19 Checking C/Y Gain of Test Signal.

NOTE

Before performing steps 15 through 17, close switches 6, 4, and 3 on S156 and reset the TSG 371 by turning it OFF, then back ON. This will make three diagnostic signals — DAC Test, Multipulse, and Sweep — available at the TEST SIGNAL output. When the TSG 371 is in this mode, the COMPONENT BARS switch is used to choose among the three signals.

NOTE

Steps 15 through 17 are interactive and should be repeated, in sequence, until satisfactory results are obtained.

15. Chrominance-to-Luminance Gain

a. Connect an oscilloscope to the CH A loop-through of the 1781R as shown in Fig. 5-19.

b. Select the DAC Test signal from the TSG 371 with the COMPONENT BARS switch (the 1781R will not lock on to this signal).

c. Adjust the oscilloscope triggering to view both the 500 kHz and 4.43 MHz sine waves.

d. Adjust C838 to match the sine wave amplitudes within 5 mV.

e. Select the Line Sweep signal using the component Bars button.

f. Use the waveform monitor to check for a flat (±1%) frequency response out to 5 MHz. Adjust C838 as needed.

NOTE

Inductors L450, L550, L551, L650, and L750 are factory set. Only perform steps 16 and 17 if the Test Signal output cannot be brought into frequency spec using C753.

16. Test Signal Frequency Response

a. Begin with the 1781R Reference Setup (Fig. 5-18). Select WFM + CAL Display, Fixed CAL, and CH A INPUT.

b. Select the Sweep signal from the TSG 371 (with the COMPONENT BARS switch).

c. Adjust L450, L550, L551, L650, and L750 for as flat a response as possible. The line sweep should be flat within 2% (± 7 mV) out to 5 MHz (last marker).

17. **Group Delay**
    a. Return the Measurement Set to WFM Display.
    b. Select the Multipulse signal from the TSG 371 (with the Component BARS switch).
    c. Adjust L450 and L550 for the smallest possible distortion envelopes at the base of each modulated pulse. The 20T pulse will have no more than 2.8 mV_{p-p} distortion, and the 10T pulses no more than 5.5 mV_{p-p} distortion when the delay is 5 ns or less.

FREQUENCY RESPONSE — COMPONENT SIGNALS

NOTE

Steps 18 through 23 are interactive and should be repeated, in sequence, until satisfactory results are obtained.

18. **Channel 1 (Y) Fine Frequency Response**
    a. Begin with the 1781R Reference Setup (Fig. 5-18). Select WFM + CAL Display and CH B1 INPUT.
    b. Select the 60% Line Sweep signal from the front panel of the TSG 371.
    c. Set the waveform monitor for 5x vertical magnification and adjust the vertical position to display the top of the line sweep.
    d. Set the voltage calibrator for 8.4 mV.
    e. Move the voltage calibrator to the top of the sweep.
    f. Adjust C11 for as flat a waveform as possible (within the calibrators) out to 5.0 MHz (the last marker).

19. **Channel 2 (B-Y) Fine Frequency Response**
    a. Using the same setup as above display CH B2.
    b. Select the 60% Line Sweep signal from the front panel of the TSG 371.
    c. Set the waveform monitor for 5x vertical magnification and adjust the vertical position to display the top of the line sweep.
    d. Set the voltage calibrator for 8.4 mV.
    e. Move the voltage calibrator to the top of the sweep.
    f. Adjust C32 for as flat a waveform as possible (within the calibrators) out to 2.5 MHz (the last marker).

20. **Channel 3 (R-Y) Fine Frequency Response**
    a. Using the same setup as above display CH B3.
    b. Select the 60% Line Sweep signal from the front panel of the TSG 371.
    c. Set the waveform monitor for 5x vertical magnification and adjust the vertical position to display the top of the line sweep.
    d. Set the voltage calibrator for 8.4 mV.
    e. Move the voltage calibrator to the top of the sweep.
    f. Adjust C53 for as flat a waveform as possible (within the calibrators) out to 2.5 MHz (the last marker).

NOTE

The following inductors are factory set. Only perform steps 21, 22, and 23 if the Component outputs cannot be brought into frequency spec using steps 18, 19, and 20.

21. **Channel 1 (Y) Coarse Frequency Response**
    a. Begin with the 1781R Reference Setup (Fig. 5-18). Select WFM + CAL Display and CH B1 INPUT.
    b. Select the 60% Line Sweep signal from the front panel of the TSG 371.
    c. Set the waveform monitor for 5x vertical magnification and adjust the vertical position to display the top of the line sweep.
    d. Set the voltage calibrator for 8.4 mV.
    e. Move the voltage calibrator to the top of the sweep.
    f. Adjust L3, L4, L5, L6, and L7 for as flat a waveform as possible (within the calibrators) out to 5.0 MHz (the last marker).
    g. Repeat step 17.

22. **Channel 2 (B-Y) Coarse Frequency Response**
    a. Using the same setup as above display CH B2.

b. Select the 60% Line Sweep signal from the front panel of the TSG 371.

c. Set the waveform monitor for 5x vertical magnification and adjust the vertical position to display the top of the line sweep.

d. Set the voltage calibrator for 8.4 mV.

e. Move the voltage calibrator to the top of the sweep.

f. Adjust L8, L9, L10, L11, and L12 for as flat a waveform as possible (within the calibrators) out to 2.5 MHz (the last marker).

g. Repeat step 18.

23. Channel 3 (R-Y) Coarse Frequency Response

a. Using the same setup as above display CH B3.

b. Select the 60% Line Sweep signal from the front panel of the TSG 371.

c. Set the waveform monitor for 5x vertical magnification and adjust the vertical position to display the top of the line sweep.

d. Set the voltage calibrator for 8.4 mV.

e. Move the voltage calibrator to the top of the sweep.

f. Adjust L13, L14, L15, L16, and L17 for as flat a waveform as possible (within the calibrators) out to 2.5 MHz (the last marker).

g. Repeat step 19.

h. Repeat Steps 17 through 23 as needed to bring the instrument into spec.

COMPONENT INTERCHANNEL TIMING

24. Channel 1 (Y) to Channel 2 (B-Y)

a. Begin with the 1781R Reference Setup (Fig. 5-18). Select B1-B2 input.

b. Adjust the waveform display with horizontal and vertical magnification to zoom in on the center of the bowtie.

c. Adjust C4 on the Component board to center and null the bowtie as shown in Fig. 5-20.

25. Channel 1 (Y) to Channel 3 (R-Y)

a. Begin with the 1781R Reference Setup (Fig. 5-18). Select B1-B3 input.

b. Adjust the waveform display with horizontal and vertical magnification to zoom in on the center of the bowtie.

c. Adjust C3 on the Component board to center and null the bowtie as shown in Fig. 5-20.

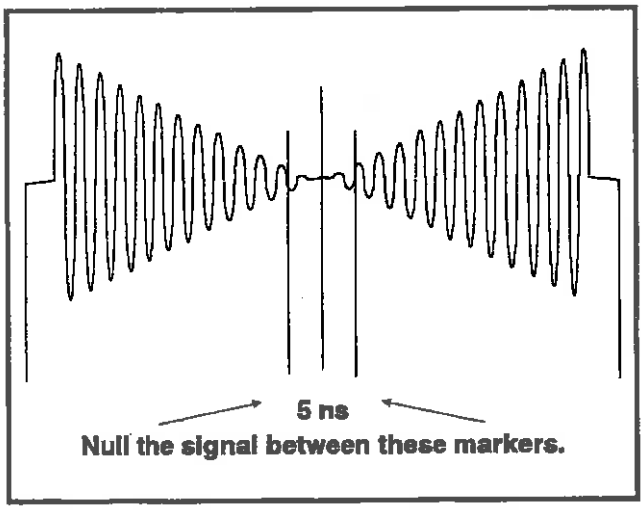


Fig. 5-20. Example of a properly adjusted bowtie signal.

SECTION 6
THEORY OF OPERATION

NOTE

The following conventions are used throughout this manual for signal names:

(1) (B_DITHER) is equivalent to $\overline{\text{B\_DITHER}}$ *-- negation.*

(2) [CLK_C] is an aside.

(3) [(B_DITHER)] is an aside of (B_DITHER).

OVERVIEW

The TSG 371 Theory of Operation is made up of two parts. First, the Block Diagram describes the basic architecture of the TSG 371 via function blocks. The Circuit Descriptions are second. These describe the schematic diagrams that make up the function blocks.

BLOCK DIAGRAM

This section divides the TSG 371 into seven functions: Input Processing, Genlock Loop, Signal Timing, Signal Generation, Output Processing, Component Signal Generator, and Power Supply. Refer to Fig. 6-1 or the more detailed block diagram in Section 9 when reading the description of these functions.

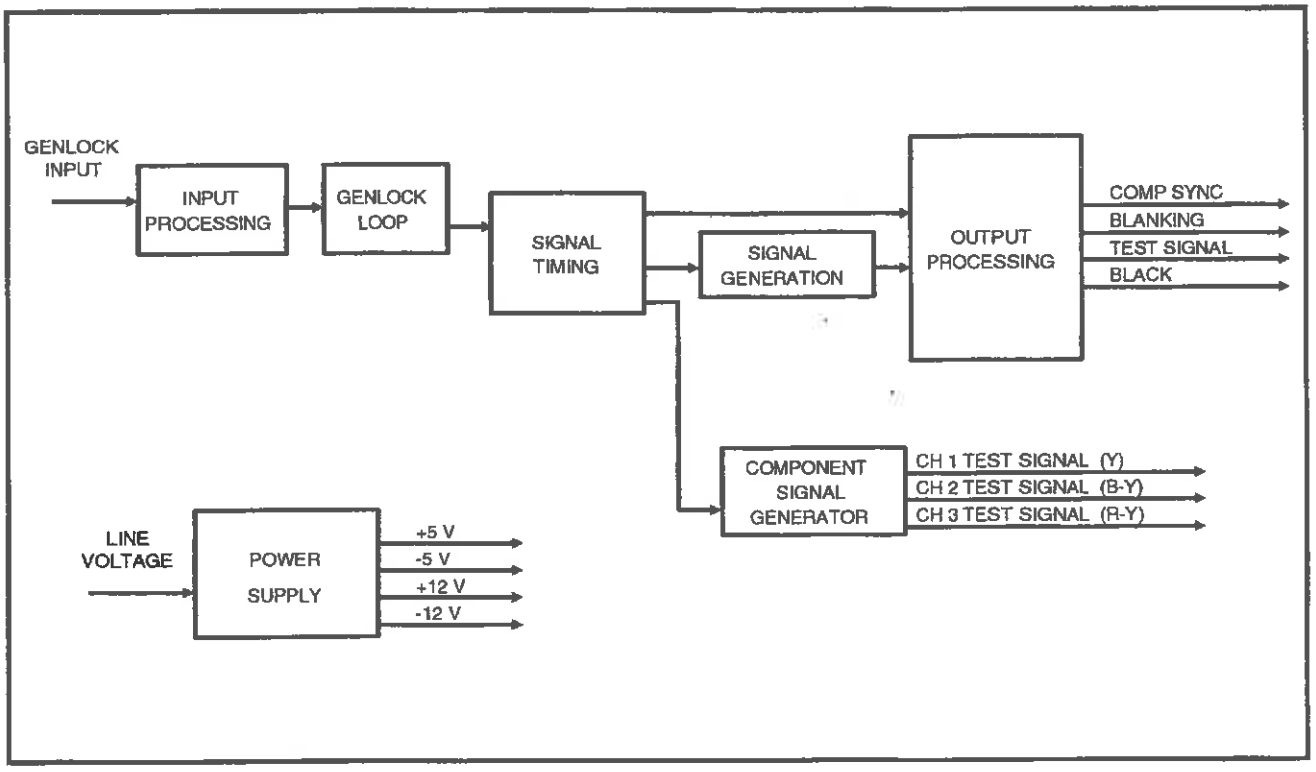


Fig. 6-1. Basic block diagram of the TSG 371.

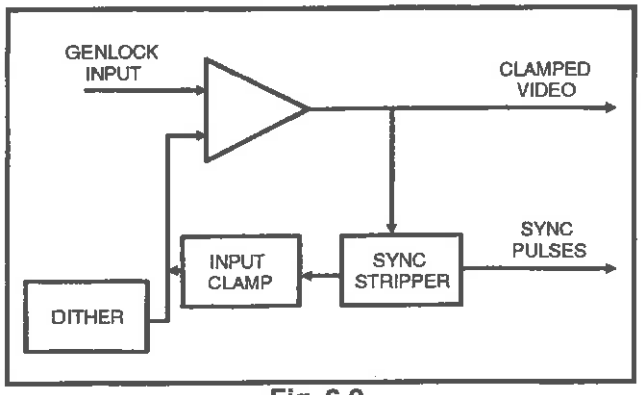


Fig. 6-2.
Block Diagram of the Input Processing circuit.

Input Processing (See Fig. 6-2)

To prepare the reference input (GENLOCK Input) for ADC sampling, the Input Processing circuit inverts it, clamps the sync tip to -50 mV, and filters it. The Sync Separator extracts composite sync from the Genlock Input signal, then supplies it to the Input Clamp and the Memory Controller (in the Genlock Loop). Both of these circuits use the composite sync as a timing reference. The processed Genlock Input signal is passed to the Genlock Loop, where it is continuously sampled by the ADC.

Genlock Loop (See Fig. 6-3)

The Genlock Loop locks the TSG 371 outputs to the Genlock Input signal. It does this by generating two signals [CLK1 and FLD_REF] which control the timing of the Signal Generation circuits. CLK1 is the 1135F_H system clock and FLD_REF (field reference) is a field timing reference signal from which the Signal Generation circuits derive vertical and horizontal timing when the instrument is genlocked to composite video.

To lock to composite video, the Genlock circuit finds the sync and burst portion of the incoming composite video signal (called the sync and burst window) and stores it in the Sample RAM every line. Using this data, the µP calculates sync timing and burst phase, so the Genlock Loop can lock to sync and burst, as described below.

Locking to Sync

Initially, the Genlock Loop acquires horizontal sync by locking its Line Counter in the Address Control circuits directly to the incoming sync. This allows the µP to sample the sync and burst window to find vertical sync. Once it has found vertical sync, the Genlock Loop obtains a more accurate horizontal sync lock as follows: (1) First, the µP switches the Line Counter to internal timing, and synchronizes the Line Counter

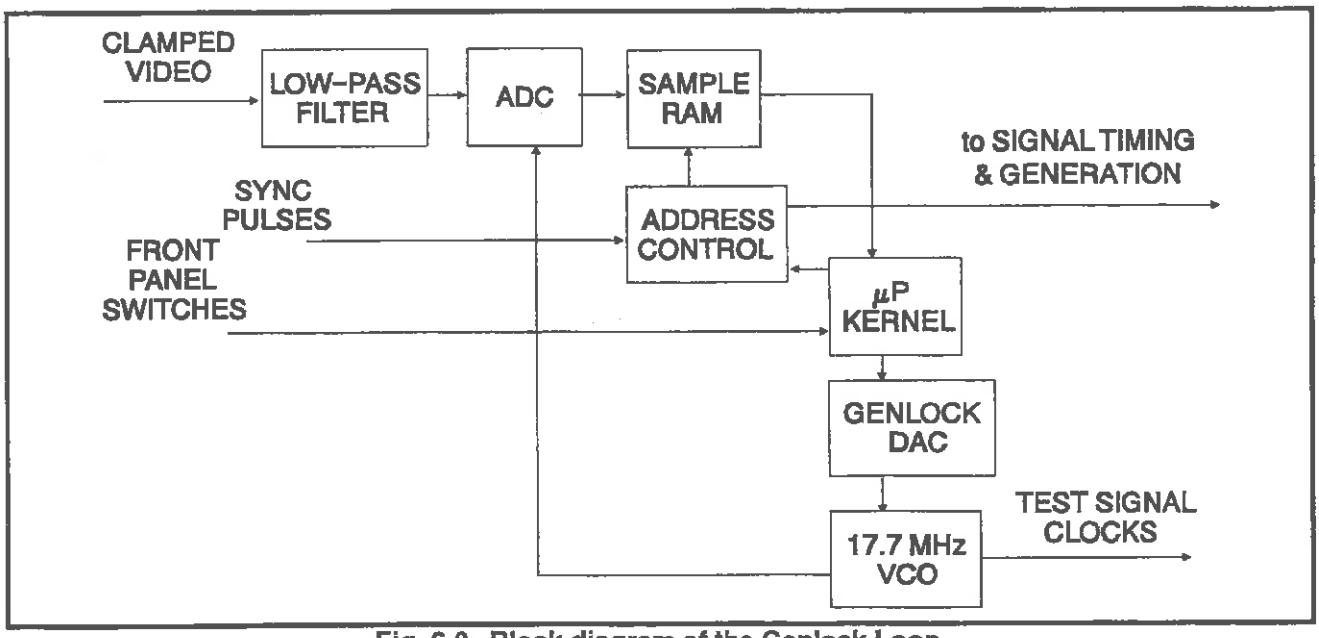


Fig. 6-3. Block diagram of the Genlock Loop.

timing with incoming sync timing as calculated from the window data. (Since internal timing has less jitter than incoming sync, it provides a more accurate reference.) (2) Once the Address Control is set to internal timing, the μP begins locking the VCO to either incoming burst or sync samples, depending on whether the incoming composite video signal has burst or is monochrome.

Locking to Burst

When the Genlock Input is composite video with burst, the μP uses burst samples contained in the sync and burst window to lock the VCO to incoming burst. Four cycles of burst on a line of video are sampled and averaged together.

Because the ADC is clocked by the VCO, samples of incoming burst indicate VCO phase relation to the incoming burst phase. The μP extracts the burst-to-VCO phase information during the next four video lines and uses it to generate a VCO correction word on the fifth. The Genlock DAC converts the correction word to a voltage. This voltage is integrated and used to keep the VCO and its CLK1 output phase-locked to incoming burst by shifting the VCO frequency.

Because the Genlock Clock is line-locked and the PAL burst frequency is offset from the line-locked frequency by 25 Hz, the burst-to-VCO phase varies throughout the video field. As the phase calculations are done, a phase offset value is read from a line offset look-up table.

The phase calculations executed by the μP include an arctangent trigonometric function. To improve the execution speed, the arctangent calculation is replaced with a table look-up from the Arctangent PROM. Once the VCO is burst locked, the μP calculates the timing for line 7 of field 1 and indicates it with a pulse to the Address Decoder. The Address Decoder gates this pulse with the 50% point of sync to generate the FLD_REF signal.

When the Genlock Input is monochrome composite video, the μP uses incoming sync samples to calculate the VCO phase relative to the incoming sync. It then generates a correction word to shift the VCO frequency (which shifts phase accordingly). Thus, the VCO output (CLK1) is locked to incoming sync.

Fine Genlock Timing

Adjustment of the fine genlock timing is done inside the Genlock Loop. When fine genlock timing is adjusted at the front panel, the μP adds an offset to its VCO correction word to shift VCO phase in the desired direction. This results in new ADC sample timing, and consequently, new sample values. When analyzing the new values, the μP takes into account the timing offset. Hence, it does not attempt to "correct" its own offset.

Signal Timing
(See Fig. 6-4)

The Signal Timing section puts out two sets of signals: the sync pulses and the line-locked test signal timing data. All the signals are locked to the Genlock Input signal. The circuits that generate these signals are described below.

Test Signal Timing

The main job of the Test Signal Generation circuitry is to produce the front-panel-selectable test signals. It does this by using two genlocked timing signals [CLK1 and FLD_REF] plus delay information from the µP to drive its signal selection and timing circuits. These circuits control the Test Signal PROMs, which contain the test signals. The circuit blocks which generate the timing and signal selection are: the Genlock Timing Offset, the H Timing Counter, the Vertical Counter, the H and V Timing PROMs, and the Signal Selector.

The Genlock Timing Offset is controlled by the µP. When coarse genlock timing is adjusted at the front panel, the Genlock Timing Offset shifts the timing of the H and V Counters, thus shifting the timing of the whole Test Signal Timing circuitry by up to ± 7 µs.

The H Timing Counters provide timing to the Test Signal PROMs [in the Signal Generation circuitry] by addressing the horizontal components of the selected signal. The Vertical Counter provides vertical timing to the V Timing PROM, which in turn provides vertical timing to the Signal Selector [also in the Signal Generation circuitry].

Signal Selection is updated during the vertical interval. The µP sends out a selection code that, combined with V Timing PROM outputs, tells the Signal Selector which signal to select and when to select it. The V Timing PROM also tells the Selector which elements of the signal to select. The V Pulse PROM tells the Selector when to select vertical sync.

The signals selected at the Test Signal PROMs are sent on to the Video Synthesizer and the Output Processing.

Sync Pulse Generation

The main job of the Sync Pulse Generation section is to produce correctly timed sync pulse signals. It does this by using the two genlock signals [CLK1 and FLD_REF] plus delay information from the µP to generate timing for its H and V Pulse PROMs. The output of these PROMs makes up the sync pulse signals sent to the Analog and Component boards. The circuit clocks that generate timing for the H and V Sync Pulse PROMs are: the Sync Phase Shifter, Phase Shift DAC, H Pulse Counter, and V Pulse Latch.

The Sync Phase Shifter and Phase Shift DAC allow the µP to match the pulse output timing with the Test Signal output. The Sync Phase Shifter adjusts the phase of the clocks which drive the Sync Pulse Generation circuit blocks.

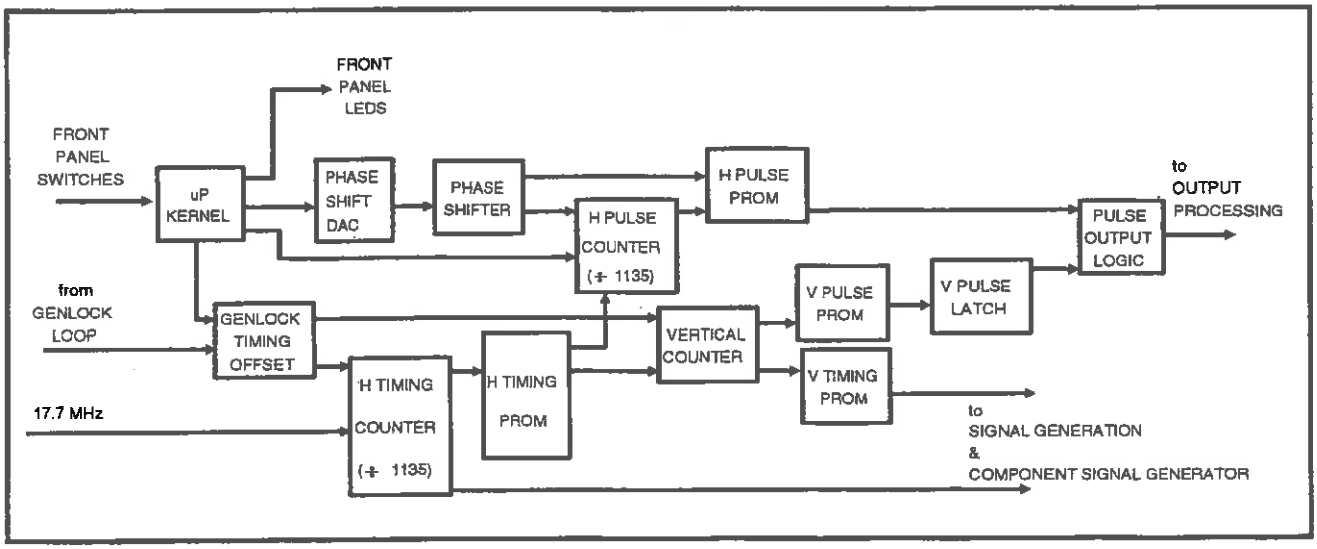


Fig. 6-4.
Block diagram of the Signal Timing & Generation circuit.

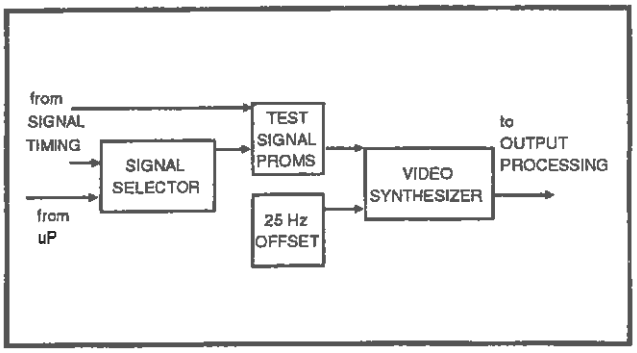


Fig. 6-5. Block diagram of the Signal Generation.

Deriving its timing from the H Timing PROM, the H Pulse Counter divides the clock by 1135 to address the horizontal sync pulse components in the H Pulse PROM. The coarse sync timing from the µP is added to the H Pulse PROM through this counter. The µP adds this offset by changing the counter's reset count.

The Vertical Counter generates vertical timing for the V Pulse PROM. However, the Vertical Counter does not have sync timing offset, so the H Pulse PROM aligns the timing of the V Pulse PROM outputs with its own timing by controlling the timing of the V Pulse Latch.

Signal Generation (See Fig. 6-5)

Signal Selection is updated during the vertical interval. The µP sends out a selection code that, combined with V Timing PROM outputs, tells the Signal Selector which signal to select and when to select it. The V Timing PROM also tells the Selector which elements of the signal to select. The V Pulse PROM tells the Selector when to select vertical sync.

The signals selected at the Test Signal PROMs are sent on to the Video Synthesizer and the Output Processing.

Output Processing (See Fig. 6-6)

Test Signal Output

The test signal output from the Signal Generation circuitry is converted to analog by the Test Signal DAC, then low-pass filtered to remove out-of-band components. The Output Amplifier provides the signal with the correct power and amplitude levels. It also boosts the high end of the signal frequency spectrum to compensate for sin(x)/x roll-off.

Black Generation

Black is generated by switching the currently-selected test signal to blanking level during active video and then switching back to the sync and burst portion of the test signal during the sync and burst time.

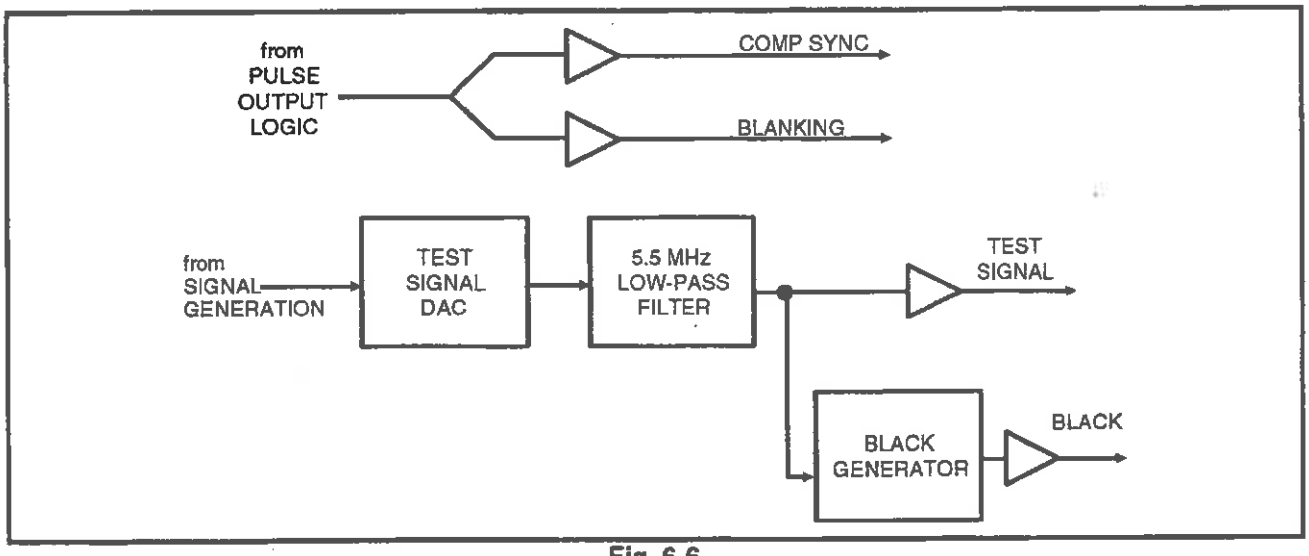


Fig. 6-6.
Block diagram of the Output Processing circuit.

Pulse Outputs

The functions of the Pulse Output circuits are to convert the TTL level outputs from the Pulse Output Logic to standard TV levels and to supply the necessary power to drive a 75Ω load.

Component Signal Generator (See Fig. 6-7)

The Component Signal Generator is very similar to the Signal Generation and Output Processing in function.

Signal Selection is updated during the vertical interval. The µP sends out a selection code that tells the Signal Selector which signal to select and when to select it.

The H Timing Counters [Signal Timing Circuitry] provide timing to the Channel Signal Memories by addressing the horizontal components of the selected signal. The Vertical Timing PROM [Signal Timing circuitry] provides vertical timing, addressing the vertical components of the signal.

The Channel Signal Memory output is converted to analog, then low-pass filtered to remove out-of-band components. The Output Amplifiers provide the signals with the correct power and amplitude levels. They also boosts the high end of the signal frequency spectrum to compensate for sin(x)/x roll-off.

Power Supply

The switching power supply generates ± 5 V for TTL and ECL devices. A stable linear supply of ± 12 V is provided for powering the analog circuitry.

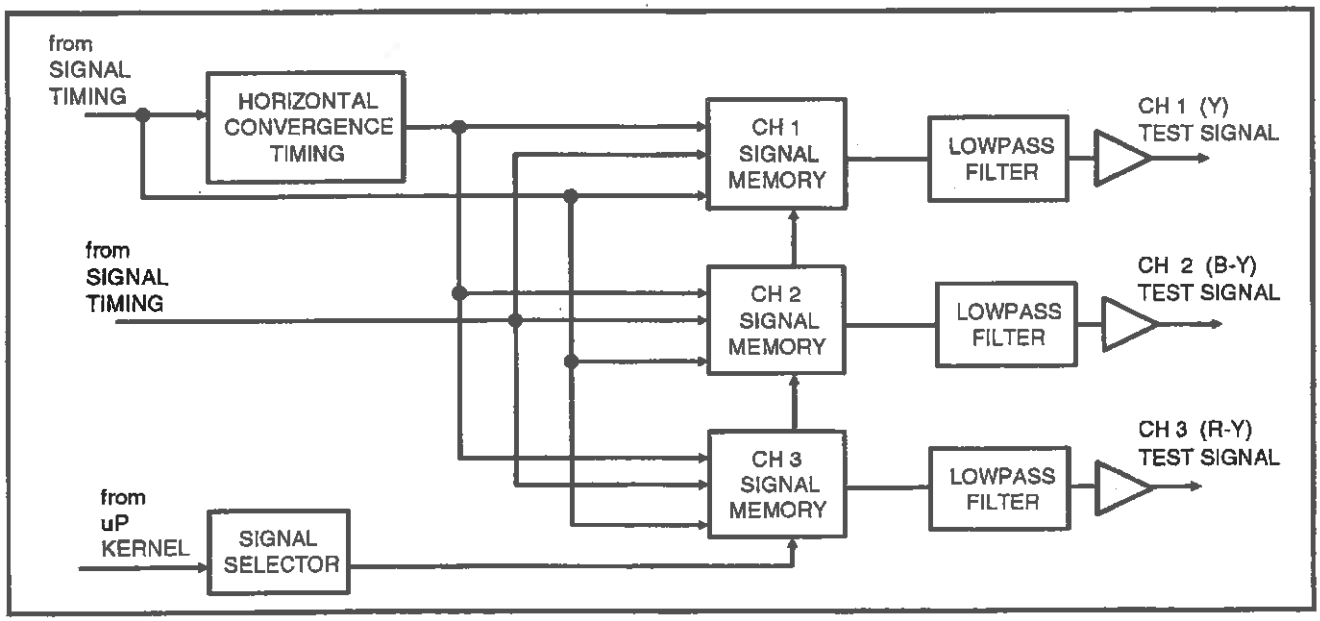


Fig. 6-7. Block diagram of Component Signal Generator

CIRCUIT DESCRIPTIONS

FRONT PANEL ① (See Fig. 6-8)

The five main functions of the Front Panel I/O circuitry are (1) to transfer front-panel user selections to the µP, (2) to transfer signal timing offset data from the µP to the Digital board, (3) to transfer diagnostic switch data to the µP, (4) to transfer remote control data to the µP, and (5) to transfer operating status and diagnostic data from the µP to the front-panel LEDs. Each of these is described below.

Front-Panel Selection

Decoder U205 converts the front-panel data selected by the 11 switches into a 4-bit word and applies it to buffer U208. During the vertical interval, the µP checks the front panel by asserting (KEYBOARD). This loads the 4-bit word onto the data bus. To determine if a new selection has been made at the front panel, the µP checks for a high level on the ED4 line. The Data Available output (U205, pin 13) pulls this line high for about 20 ms whenever a new front-panel selection is made.

The (OPT_1_PRESENT) line is pulled high (tied to +5 V) at the Component board to indicate that the audio and character ID generators are not available on this instrument.

Jumpers J111, J208, and J308 are shipped in the 1-2 position. These positions select the normal front-panel operation. Jumper J111, in the 2-3 position, disables the front panel selection of operating modes. In the 2-3 position, jumper J208 enables the programming of remote controlled test signal selection. In the 2-3 position, J308 disables any attempts to change genlock timing.

Timing Offset Latches

The µP sends the coarse sync-timing and genlock-timing offsets to the Signal Generation circuits through two latches (U880 and U364, respectively). The genlock timing offset is sent to the Genlock Timing Offset circuit ⑤. The sync timing offset is sent to the H Pulse Counter circuit ⑤. The LSB of the sync timing offset is the PHASE FLIP line which is sent to the Phase Flip circuit ④.

Diagnostic Switches

The user selects the diagnostic routines through the Diagnostic Switches (S156). Immediately after the µP is reset, it checks the diagnostic switch buffer (U161) by asserting the (DIAG_PORT) line, and performs the selected diagnostic routine(s). When all switches are open, the instrument is in normal operation. Refer to Diagnostics in the Maintenance section for a full description of the diagnostic routines.

Remote Control Port

The remote control and front panel can both operate simultaneously, but the remote has priority. That is, during the vertical interval, the µP first checks the remote control buffers (U846 and U849) and then the front-panel buffer (U208). But if a new selection since

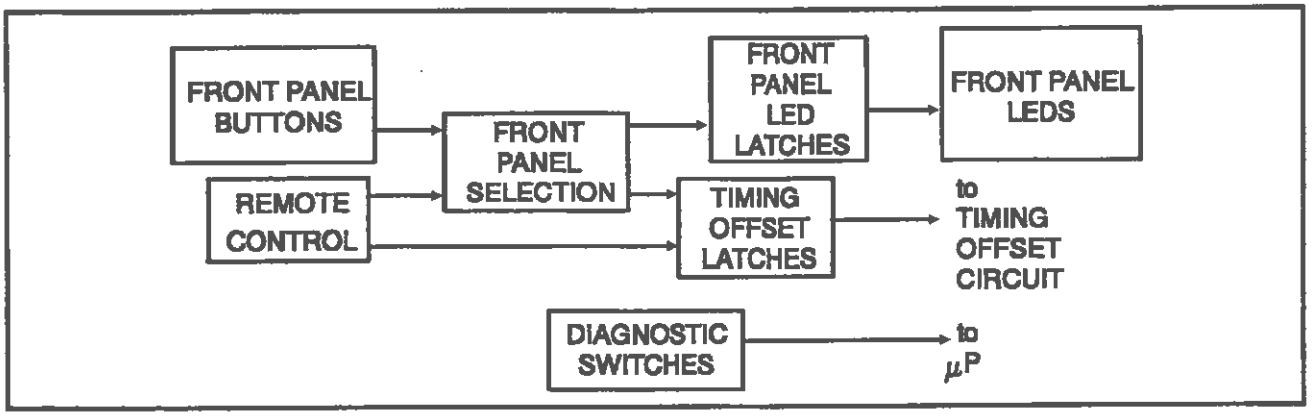


Fig. 6-8.
Block diagram of the Front Panel Interface.

the previous vertical interval has been made at the remote control, the μP executes the new selection and does not check for the front-panel input.

Front-Panel LED Latches and LEDs

The front-panel LEDs are all controlled by the μP through the three latches (U302, U211, and U214). The μP enables these latches with the (LED_0), (LED_1), and (CONTROL) signals. U214 also puts out five additional signals: CLAMP_DISABLE, (CHAR_EN), (BLACK_EN), (INT)/GENLOCK, and (HOLD)/ACQUIRE. CLAMP_DISABLE disables the test signal output clamp. (CHAR_EN) provides μP control over the Character ID Generator. (BLACK_EN) forces the test signal output to black and shuts off the audio tone. When the (INT)/GENLOCK line is high, the instrument is forced to use the internal reference; when the line is low, the instrument will genlock to the reference input (if it is available). (HOLD)/ACQUIRE controls the loop response of the Genlock Loop.

MICROPROCESSOR (μP) KERNEL ◇2◇ (See Fig. 6-9)

This section briefly describes the functions of the μP Kernel and its components. For a description of the diagnostics executed by the μP, refer to the Maintenance section.

The μP Kernel has four main functions: (1) to acquire and maintain genlock with the incoming reference signal, (2) to service the front panel and remote control, (3) to control the test signal timing, and (4) to execute diagnostics. The components of the Kernel are described as follows.

Microprocessor

The Microprocessor (μP) (U427) is the heart of the Kernel. Receiving its program instructions from the EPROM (U333), the μP controls the Kernel through address lines (A0-A15), data lines (D0-D7), and various other control lines.

The clock that drives the μP is derived from the 17.7 MHz CLK_B. PAL U129 divides this clock by 3 to obtain a 5.9 MHz clock, named μP_CLK, for the μP and the CTCs. U232B, U232C, and the associated parts shape the clock signal and apply it to the μP.

When the instrument is being powered up, the (RESET) pulse from U321 goes low, resetting the μP Kernel. The μP can be manually reset by momentarily moving jumper J229 to the 2-3 position.

During normal operation, the CTCs (U240 and U245) monitor the μP. If the μP is not sending correct data and addresses to the CTCs, the CTCs put out (SOFT_RESET) to interrupt and re-initialize the μP. The CTC's (SOFT_RESET) pulse can be prevented from interrupting the μP by moving jumper J423 to the 2-3 position.

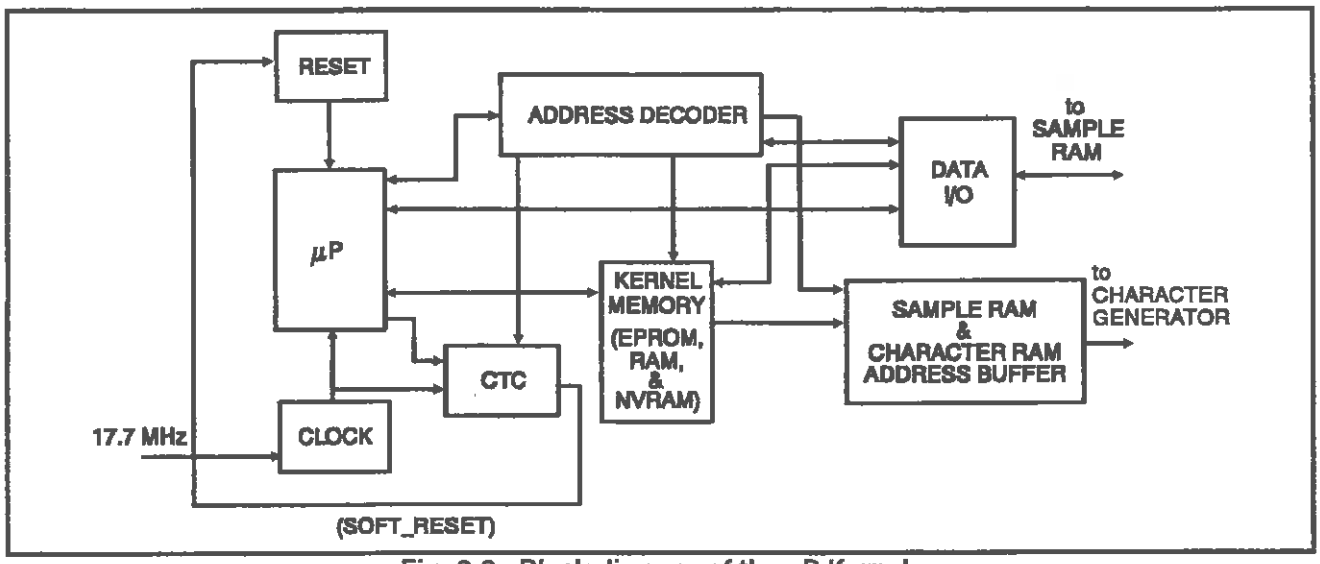


Fig. 6-9. Block diagram of the μP Kernel.

U321 also contains a timer circuit. During normal operation, the µP keeps this timer reset by asserting (AWAKE) repeatedly. If for some reason, the µP fails to reset the timer, U321 resets the µP. Moving jumper J223 to the 2-3 position forces (RESET) low and moving J223 to the 2-4 position disables µP resets for troubleshooting purposes.

Kernel Memory

EPROM (U333) contains the instructions that control the µP. The EPROM occupies the µP's address space between 0000 and 7FFF (hex).

RAM (U340) stores temporary data and program variables for the µP. The RAM occupies addresses A000-A7FF (hex).

The Arctangent PROM (U122) is a look-up table of the trigonometric arctangent function of a ratio of two numbers. While doing genlock calculations, the µP looks up the solution to the arctangent calculation in the PROM instead of calculating it.

The µP first outputs the divisor of the calculation to latch U217. This provides the lower half of the PROM address. Then the µP reads from the ATAN I/O location. By virtue of the µP architecture, the upper 8 address lines contain the I/O port address. These 8 bits form the upper 8 bits of the PROM address. The PROM outputs are then available on the external data bus ED0-ED7. NVRAM (U345) is a combined non-volatile memory and a static RAM. The NVRAM contains genlock timing presets, character ID presets, and remote control signal selection data. The NVRAM occupies addresses E000-E07F.

Immediately following a µP reset, the µP loads the front-panel data from the non-volatile portion of the NVRAM into the RAM portion. Then, from the RAM portion, it loads the timing offset into the H and V Timing circuits ⑤, and loads the character ID data into the Character RAM on the Component board.

If a new timing offset or character ID is selected at the front panel, the µP loads the new data into the RAM portion of the NVRAM during the vertical interval. When the MODE SELECT switch is cycled back to the SELECT TEST SIGNAL position or the mode times out, the new data is stored in the non-volatile part of the NVRAM.

The NVRAM is controlled by the µP via the NVRAM Controller PAL (U236). The Controller PAL decodes the µP address and control lines to generate read, write, and chip select pulses for the NVRAM. Consisting of Q541, U232D, and the associated parts, the NVRAM Save Control prevents the NVRAM from saving data during power-up and power-down. During power-up, (RESET) forces the output of U232D high to keep the (NV_SAVE) line high (inactive). During power-down, Q541 and its associated components keep the (NV_SAVE) line high until the NV_PWR power supply has dropped below 3 V.

CTCS

CTC0 and CTC1 (U240 and U245, respectively) are 4-channel programmable counter/timer chips configured as programmable event counters. Their job is to count pulse signals generated by the Genlock circuit and indicate to the µP the sequence in which these signals occur. The µP instructs each channel clock to count a specified number of input pulses and to interrupt the µP when it has reached this count. In this manner, the µP can determine the sequence in which the genlock signals are occurring.

The CTC input signals are synchronized with the system clock. uP_CLK latches the Genlock Loop pulses ③, and CLK_2.95 latches the (ASYNC) in U519A. The CTCs are daisy-chained (with their IEI and IEO lines) so that CTC0 has interrupt priority. This means that interrupts caused by channels 0 through 3 of CTC0 have higher priority than those caused by channels 0 through 3 of CTC1. When CTC0 interrupts, its IEO line goes low, disabling CTC1 interrupts. When CTC0 is not interrupting, its IEI line is high, enabling CTC1 to interrupt the µP.

Address Decoders

PAL U126 decodes the µP address and control lines to generate chip select signals for: the Kernel Memories, the Sample RAM, CTCs, the I/O Decoder, the Character ID Memory, and the External Data Bus Buffer.

The I/O Decoder (U320) decodes the µP I/O port addresses 0-15 to enable the Front-Panel, Remote Control and Diagnostic Switch Input Buffers ①; Front-Panel LED and Timing Offset Latch Outputs ①; the Genlock Line Counter ③; the Sync Timing and VCO Control DACs ④; and the Signal Select Latch ⑥.

Address Buffers

When reading from or writing to the Sample RAM, the µP uses the Sample RAM and Character RAM Address Buffer (U415) [enabled by (SAMPL_RAM_EN)] as a port.

The Character ID Address Buffer (U723) isolates the Character ID Generator from the Kernel. It sends the Character ID RAM addresses and control signals to the Character Generator.

Data I/O Buffers

The External Data Bus transceiver (U405) isolates the Kernel while allowing two-way communication with external devices.

The Sample RAM Data transceiver (U402) sends data to and receives data from the Sample RAM (U503, ◈3). Normally, U402 receives data samples on every video line.

GENLOCK DATA ACQUISITION CONTROLLER 3

The Genlock Data Acquisition circuit is the part of the Genlock Loop that acquires samples of the incoming reference signal for the µP to analyze. See Fig. 6-10 for a block diagram of the circuit. For a general description of the Genlock Loop, refer to the Genlock Loop section in the Block Diagram description.

Input Filter

Made up of C905, C906, C907, and L902, this filter attenuates spectral components above the video band to prevent aliasing of the Genlock Input signal when it is quantized by the ADC.

Data Acquisition

Analog-To-Digital Converter (ADC)

The ADC (U802) converts the clamped and inverted video signal from the Analog board into 6-bit data. Dither is inserted into the signal on the Analog board to increase the resolution. U605 provides a regulated +2.5 V reference that U808 inverts and scales down to provide a precise -1 V reference to the ADC.

Because the ADC is clocked by the VCO with CLK_A, the ADC output indicates the VCO-to-burst phase relationship. During each field, the µP repeatedly checks this phase relationship and, if necessary, shifts the VCO frequency to keep it in phase with incoming burst.

The data from the ADC is latched in U602 and sent to the Sample RAM.

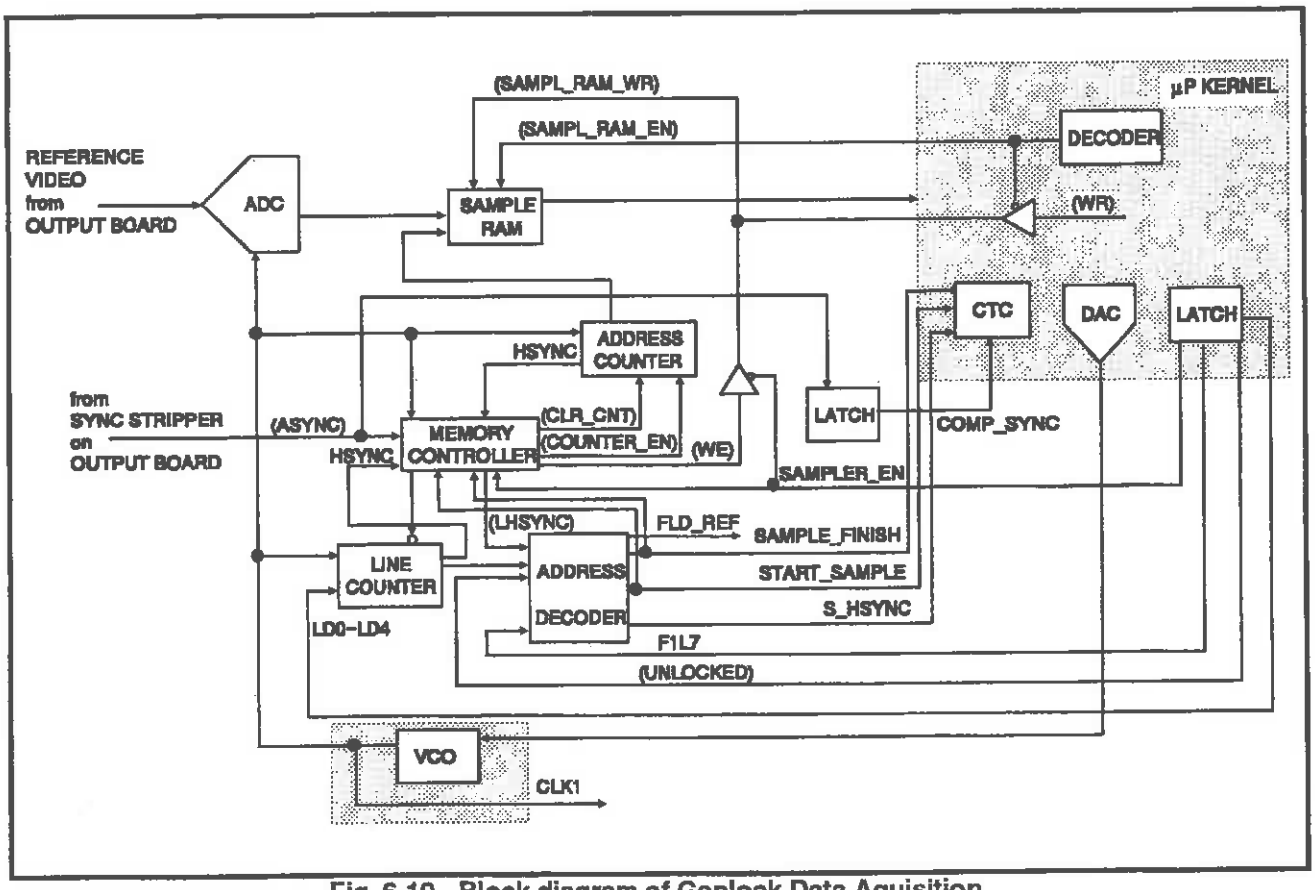


Fig. 6-10. Block diagram of Genlock Data Aquisition.

Sample RAM

The main function of the Sample RAM (U503) is to store samples, in real time, of the Genlock Input sync and burst. Each acquisition stores 256 samples of sync and burst. The µP uses these samples to obtain and maintain lock with the Genlock Input. The Sample RAM occupies addresses C000-C0FF (hex). Both the µP (U427, ◈2) and Memory Controller (U615) control the Sample RAM, but the µP has priority. When the µP needs to analyze the sync and burst samples stored in the Sample RAM, it asserts SAMPLER_EN to gain control. The µP then asserts (SAMPL_RAM_EN) to read the RAM and also asserts (WR) to write to the RAM.

When the µP is not looking at sync and burst samples, it pulls SAMPLER_EN low to give control of the Sample RAM to the Memory Controller. Storage of sync and burst data in the Sample RAM is described under Memory Controller in this section.

Address Control

Five circuits make up the Address Control section: the Line Counter (U509, U609, and U709), the Line Counter Offset latch (U409), the Address Decoder (U612), the Memory Controller (U615), and the Address Counter (U512 and U515). The combined function of these circuits is to provide timing to the Sample RAM such that the RAM's 28th sample (out of 256 samples) is coincident with the 50% point of horizontal sync.

Line Counter and Address Decoder

By counting 1135 cycles of CLK_A on every line, the Line Counter provides the Address decoder with unique addresses for each sample on the line. The Address Decoder generates timing pulses from these addresses. On the 1135th count, the S_HSYNC pulse is generated. Twenty-eight counts before S_HSYNC, the START_SAMPLE pulse is generated. During burst time, the Address Decoder generates the (B_DITHER) output.

To provide correct timing, the Line Counter should be accurately locked to incoming sync. When the instrument is powered up, or when the µP has lost the position of sync, the µP asserts (UNLOCKED). In this condition, the Address Decoder generates the (LOAD) pulse, deriving it from (ASYNC), since this is the most accurate timing available. This pulse loads the Line Counter with a nominal starting count of B92 (hex). Once the µP has found the vertical interval, it can provide a more accurate sync reference by locking the Line Counter to the 50% point of the leading edge of incoming sync. The µP calculates this point by analyzing the samples of the sync window stored in the Sample RAM. To lock the Line Counter to the 50% point of sync, the µP waits until the end of the vertical interval and pulls (UNLOCKED) high. This allows the Memory Controller to use the HSYNC signal to produce the (LOAD) pulse. The µP then analyzes the sampled data and shifts (in 212 ns increments) the Line Counter offset until HSYNC coincides with the 50% of incoming sync. At this point, the µP returns the offset to B92 (hex).

At the start of line 7 of field 1, the µP asserts (F1L7). The Address Decoder gates this signal with (L_HSYNC) to generate FLD_REF for the Signal Generation circuits.

Memory Controller and Address Counter

The Memory Controller (U615) controls the storage of ADC data in the Sample RAM. The Address Counter (U512) generates 256 addresses (0 to 255) in which the Sample RAM stores the ADC samples. Fig. 6-11 shows the timing for the Memory Controller and Address Counter outputs.

When START_SAMPLE is high and SAMPLER_EN and (COUNTER_EN) are low, the Memory Controller enables the Address Counter on the next rising edge of the clock. The Memory Controller then asserts (WE) and a sample point is written into the Sample RAM. The Memory Controller repeats this sequence of (COUNTER_EN) followed by (WE) until the Address Counter generates SAMPLE_FINISH pulse on the 256th count.

During the vertical interval, START_SAMPLE never occurs if (UNLOCKED) is low. Remember, when (UNLOCKED) is low, the Address Decoder uses (ASYNC) to derive the (LOAD) pulse for the Line Counter. In the vertical interval, this pulse occurs at a half-line rate. Because this prevents the counter from reaching a full line count, the Address Decoder cannot generate START_SAMPLE.

Memory Controller outputs START_SAMPLE, SAMPLE_FINISH, and S_HSYNC are sent to the CTCs along with (S_HSYNC). The µP continuously analyzes the sequence of these four signals to find and keep track of the vertical interval.

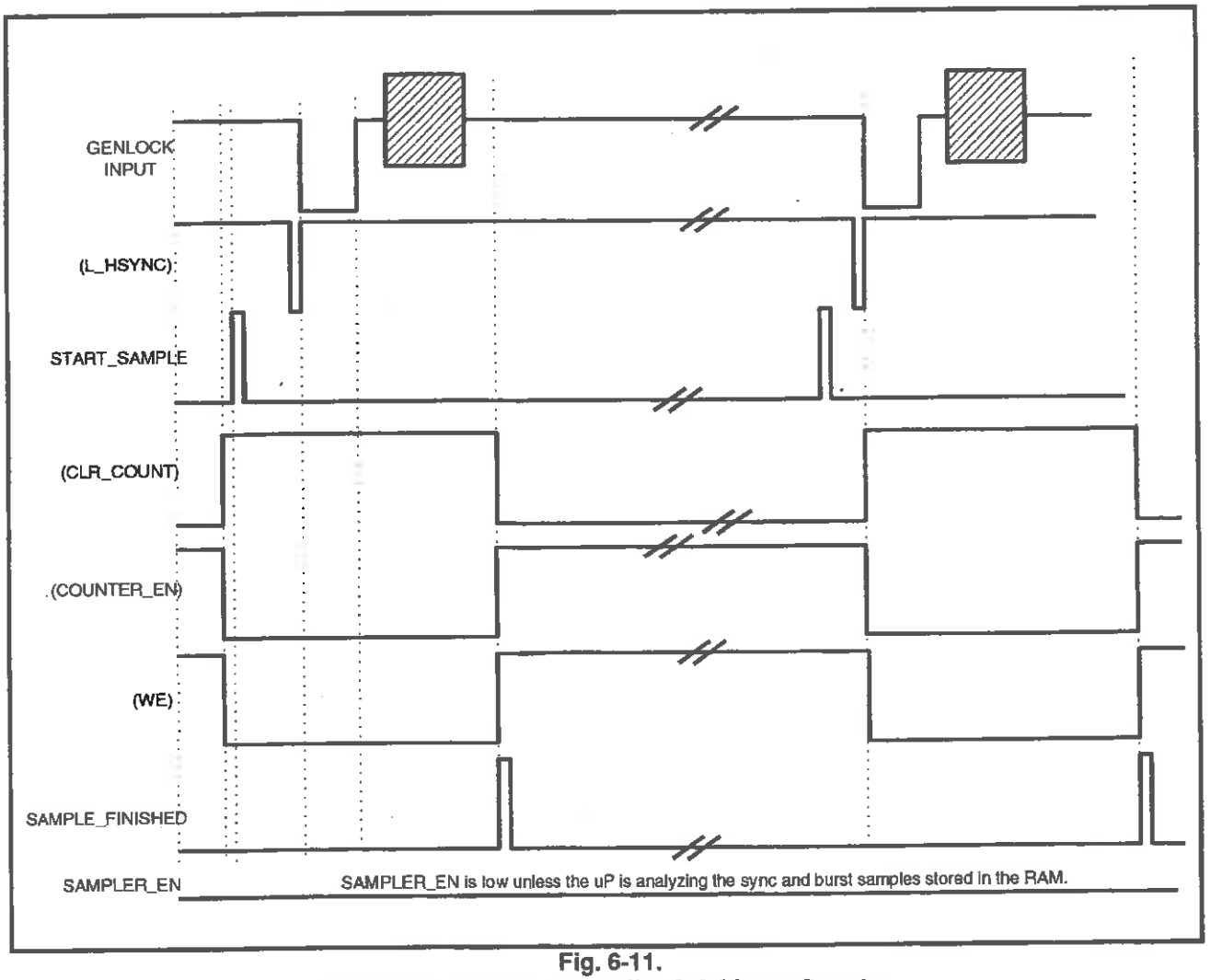


Fig. 6-11.
Timing for Memory Controller & Address Counter.

CLOCK CIRCUIT 4
(See Fig. 6-12)

The Clock Circuit generates several 1135F_H clock signals that it distributes throughout the instrument. It has four main sections: (1) VCO and Oven Heater, (2) DAC Integrator, and Switcher, (3) Clock Shaper and Drivers, and (4) Phase Flip and Fine Sync Phase Shifter.

At the heart of the Clock circuit is the Voltage Controlled Oscillator (VCO). Controlled by the µP, the VCO generates an 1135F_H signal that is either free-running or locked to the Genlock Input.

The Clock Shaper circuit converts the VCO output to an ECL square wave and ensures its duty cycle is exactly 50%. The Drivers distribute this square wave throughout the instrument.

The Phase Flip circuit inverts the Clock Shaper output to produce a clock that has the smallest increment of coarse sync advance/delay. The Fine Sync Phase Shifter delays the inverted Clock Shaper outputs to generate a pair of delayed clocks. These two clocks provide timing for the sync pulse outputs.

Voltage-Controlled Oscillator (VCO)

CAUTION

If it becomes necessary to remove Q293 from its heat sink, move jumper J497 to the 2-3 position to prevent Q293 from overheating.

The VCO circuit generates the 1135F_H signal from which the test signal generation clocks in the instrument are derived.

Capacitor C19 and the series combination of C15, C8, and C6 appear in parallel with crystal Y11. This parallel circuit is the heart of the oscillator. The series combination of varactor CR14 and C16 also appear in parallel with the crystal and determine the frequency correction range of the oscillator. As the µP changes the VCO correction voltage (at J286 pin 4), the reverse-biased diode shifts the frequency over a correction range centered around the oscillator's

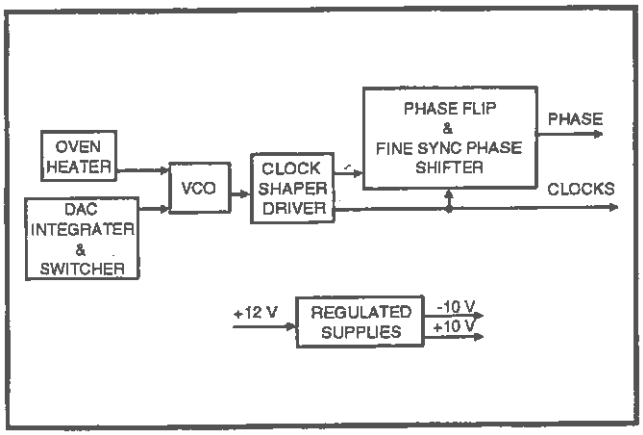


Fig. 6-12. Block diagram of the Clock Circuit.

free-running frequency. Jumper J180 (in the 1-3 position) allows the VCO correction voltage to be grounded when the free-running frequency is being adjusted with C19. Jumper positions 3-4 and 3-5 select the minimum and maximum correction voltages to check the full VCO correction range.

Oven Heater Circuit

Thermistor RT11, U495B, Q293, and associated parts makeup the Oven Heater circuit which is a feedback loop that keeps the crystal oven at a constant 60°C.

When the oven is cold, the resistance of RT11 is high, placing a more negative voltage at pin 6 of U495B. This causes the output of U495B to rise and biases Q293 on. As current flows in the transistor, it heats up. As the oven heats up, the resistance of RT11 decreases. This decreases the bias at the base of Q293 and consequently, the transistor power dissipation.

Diode CR395 prevents U495B from excessively reverse biasing Q293 by limiting the negative voltage to -5.6 V. Diodes CR394 and DS494 current limit Q293 when U495B is at its maximum value. This current limiting occurs only when the oven is cold. This allows DS494 to act as an "Oven Cold" indicator.

DAC Integrator and Switcher

The µP controls the VCO through the VCO DAC (U170). Enabled by the (VCO_DAC) signal, the VCO DAC converts the µP correction words to current pulses and applies them to integrator U270A. The correction word ranges from 00 to FF (hex).

Integrator U270A has two main functions. First, it works as a current-to-voltage converter for the correction pulses generated by the VCO DAC. These pulses shift the VCO frequency to correct VCO phase. Second, the integrator produces an average of the correction pulses. This average is essentially a DC level that changes only to track the input burst frequency.

The switches in U176 put the Genlock Loop in one of four operating modes: Internal, Genlock, Acquire, and Hold. Each is described below. The µP controls the switches through the (INT)/GENLOCK and (HOLD)/ACQUIRE lines.

Internal Mode

When the µP cannot detect a valid Genlock Input signal, it switches the Genlock Loop into Internal mode by pulling the (INT)/GENLOCK line low. This pulls the correction voltage at the integrator output to midrange or zero volts by closing three switches. The first switch shorts out the integrator capacitor; the second and third switches short out any residual voltage to ensure the correction voltage applied to the VCO is truly zero or midrange.

Genlock Mode

When the µP detects a valid Genlock Input signal, it pulls the (INT)/GENLOCK line high to apply the VCO correction voltage to the VCO.

Acquire Mode

To acquire lock with the Genlock Input, the Genlock Loop needs to be faster than when it is just holding lock. To speed up the Genlock Loop, the µP increases integrator gain by pulling the (HOLD)/ ACQUIRE line high. This adds a large resistance (R174) to the integrator feedback loop.

Hold Mode

To hold lock, the µP slows down the Genlock Loop by pulling the (HOLD)/ACQUIRE line low to remove R174 from the integrator feedback loop.

Clock Shapers and Drivers

Q491 buffers the VCO output. ECL driver U592A converts the buffered output into a complementary pair of square-wave clocks. Two RC circuits (R596 with C598 and R595 with C597) average the square waves. Op amp U495A amplifies the difference between these averages and shifts the bias of the VCO output to correct the duty cycle to 50%.

Through U588A and U588C, a pair of corrected differential ECL clocks are applied to the Analog and Component boards. U719 and U749 convert the clock signals to TTL levels and distribute them throughout the Digital board.

Phase Flip and Fine Sync Phase Shifter

These circuits are used by the µP to align the sync pulse outputs with the analog test signal outputs. The Phase Flip circuit (U636, U585B, and U585C) generates phase offsets in increments of 28 ns (45° of subcarrier) by inverting the clock when the PHASE-FLIP line is high. The phase-flipped clock signal is applied to the Fine Phase Shifter.

The Fine Phase Shifter provides up to ± 27° of fine sync phase advance/delay relative to the test signal output. The µP advances or delays the clock with timing data it applies to the DAC (U370). Converted to an analog voltage by the DAC and op amp U270B, this data reverse-biases the varactor diodes in two tank circuits connected to the inputs of U578B and U578C. The resulting change in tank capacitance changes the tank resonant frequency and advances or delays the phase-flipped clock by up to 27° in each tank circuit.

The outputs of the Phase Flip and each tank are also applied to the Fine Sync Pulse Timing Offset circuit ⑤.

Variable resistor R469, labeled SYNC TIMING RANGE CENTER, centers the tank circuits so that a half scale on DAC U370 causes 0° advance or delay.

SIGNAL GENERATION 5 - 7

The Signal Generation section consists of three schematics: Pulse & Test Signal Timing 5, Signal Selection 6, and Signal Memory & Multiplexing 7. See Fig. 6-13 for a block diagram of the Signal Generation circuits.

Overview

The H Pulse Counter and Vertical Counter provide timing to the H Pulse and V Pulse PROMs. The Pulse Output Logic combines the outputs of these two PROMs to generate the various Pulse Outputs.

The H Timing Counter and Vertical Counter provide timing to the H Timing and V Timing PROMs, respectively. These PROMs provide timing to the Signal Selection Logic, which uses this timing, along with a code generated by the µP, to select the test signal in the Test Signal PROMs. The test signal components are selected and combined by the Video Synthesizer. The test signal output is a digital representation of the test signal, sampled at $1135F_H$. This signal is applied to the Analog board.

PULSE & TEST SIGNAL TIMING 5

Genlock Timing Offset

The Genlock Timing Offset circuit is comprised of two 4-bit counters (U267 and U367) and two D flip-flops (U570A and U570B). The job of this circuit is to add the front-panel offset to the Signal Generation circuits. It does this by delaying the time at which the FLD_REF signal loads the Horizontal and Vertical Timing Counters. Normally, counters U267 and U367 are in the load mode (disabled). But on line 7 of field 1, the FLD_REF pulse enables the counters through flip-flop U570A, and counters count to 255, beginning from the offset value at their load inputs (GEN_OFF[0..7]). At the end of the count, the Carry output from U267 loads the Horizontal and Vertical Counters (through U570B) with their fixed offset values. In addition, the Carry output disables counters U267 and U367 through U570B and U570A. Jumper J570 can be moved to the 2-3 position to disable the FLD_REF input to U570A.

When coarse genlock timing is adjusted at the front panel, the µP sends a new 8-bit offset word (GEN_OFF[0..7]) to U267 and U367 via U364. On line 7 of field 1, the word is loaded into U267 and U367. As a result, U267 and U367 start their count at a different value, thus changing the time that the Horizontal and Vertical Timing Counters are loaded.

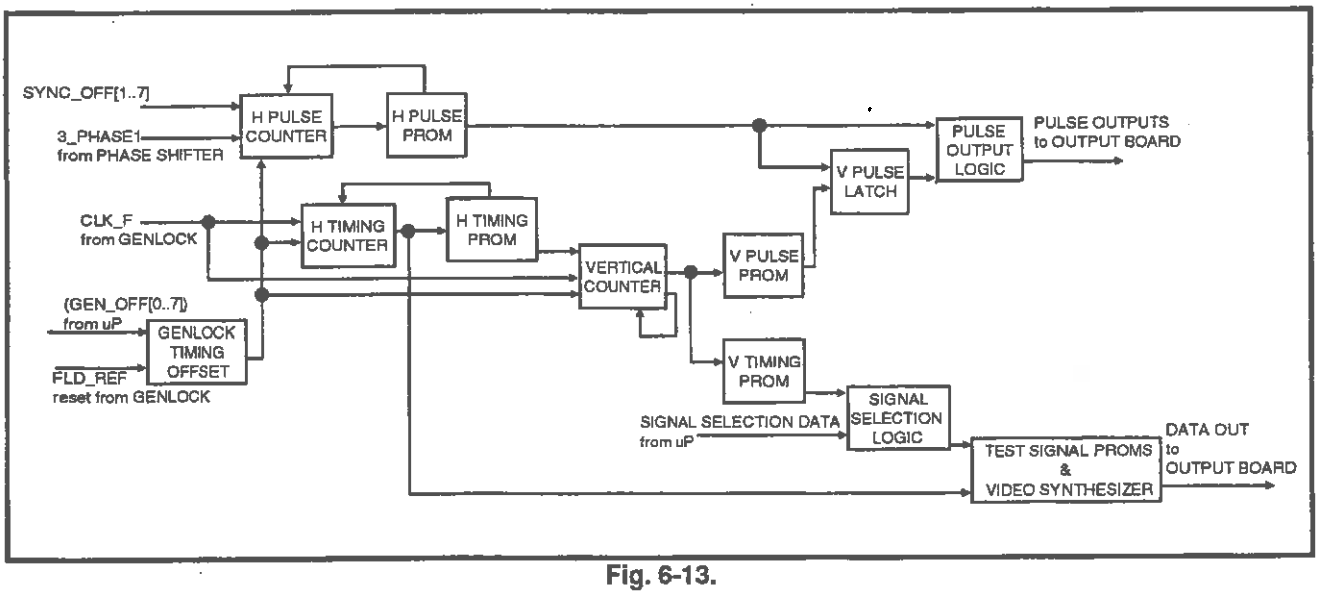


Fig. 6-13.
Block diagram of the Signal Generation circuits.

Horizontal Timing

Table 6-1. Horizontal Timing PROM. (U773)

OUTPUT	SIGNAL NAME	FUNCTION
D0	V_LATCH1	Positve pulse twice/line used to latch vertical information from the V Timing PROM, V pulse PROM, and the Signal Selection PROM.
D1	(PHASE_H1_CLR)	25 Hz Offset Generator Phase Clear.
D2		Unused.
D3	(H_BLANK)	Horizontal Blanking timing.
D4	H_CNT_CLR	Positive, 56 ns pulse to clear the H Timing Counter to zero at count 1133.
D5	V_CNT_EN	Positive, 70 ns pulse twice/line enables the Vertical Counter to count twice/line.
D6	(BURST_TIMING)	Negative pulse that is NORed with V DR to provide the BURST GATE signal. This signal is used on the Output board to clamp the test signal output.
D7	(HP_LOAD)	Negative, 56 ns pulse used to load the H Pulse Counter once/line with a count specified by the µP.

H Timing Counter

Loaded by the delayed FLD_REF signal and clocked at the 1135F_H rate, the Horizontal Timing Counter (U870, U770, and U670) provides horizontal timing to the H Timing PROM and the Luminance and Chrominance Segment PROMs ◈. It does this by addressing the PROMs at a rate of 1135 words per video line.

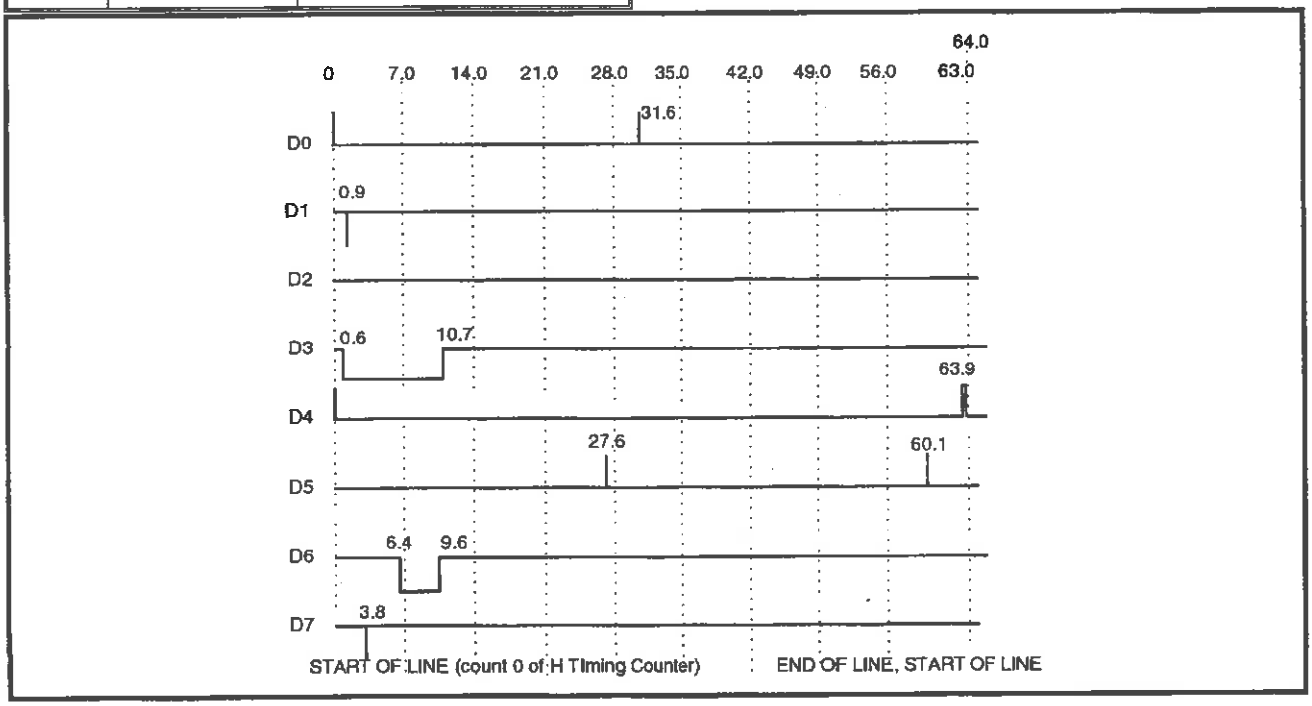
When the H Timing Counter has reached count 1134, the H Timing PROM (U773) clears it with the (H_CNT_CLR) signal. This signal is gated at U994A to prevent the H Timing Counter from being cleared while a genlock timing offset is being loaded.

The load inputs to the H Timing Counter present a fixed offset of 09F (hex). This offset allows the Genlock Timing Offset circuit to both advance and delay genlock timing.

H Timing Decoder

See Table 6-1 and Fig. 6-14 for a summary of the H Timing Decoder outputs.

Fig. 6-14.
Horizontal Timing Decoder (Numbers are in µs.)



Addressed by the genlocked H Timing Counter, the H Timing PROM (U773) and the H Timing Decoder (U873) have four functions: (1) to generate the TS_B_GATE and BB_ENABLE pulses coincident with burst and active video for the Analog board, (2) to generate timing control signals for the H and V Timing circuits, (3) to generate timing signals for the Signal Selection Logic ◈, and (4) to align the vertical timing inputs of latch U673 with the H Timing Counter.

H Pulse Counter

The H Pulse Counter (U977, U877, and U777) provides horizontal timing for the H Pulse PROM. It does this by addressing the H Pulse PROM at a rate of 1135 words per video line. The (HP_LOAD) output from the H Timing PROM is delayed by four flip-flops (U685, U682, U679, and U676). This delayed pulse loads the H Pulse Counters, thus locking the H Timing and H Pulse Counters together.

Fine Sync Pulse Timing Offset

Even though the counters are locked together, the H Pulse Counter is offset by the µP coarse and fine sync timing. The µP applies all but the smallest increment of the coarse sync offset to the load inputs of the H Pulse Counter through the SYNC_OFF[1..7] lines. The phase-flipped and fine-sync-delayed clocks delay the load pulse as it passes through U682, U679, and U676.

H Pulse PROM

The H Pulse PROM (U780) has three functions: (1) to clear the H Pulse Counter after it has counted a line of addresses, (2) to provide horizontal timing pulses to the Pulse Output Logic, and (3) to provide latch timing for V Pulse PROM outputs.

Table 6-2. Horizontal Pulse PROM Output

Output	Signal Name	Function
D0	(PC_CLR)	Negative pulse to clear the V Pulse Counter at count 1133.
D1	(PHASE_H2_CLR)	Subcarrier phase clear timing.
D2	(H_BLKNG)	Timing for H Blanking portion of Blanking output. Low from start of blanking until end of blanking.
D3	SERRATION	Timing for vertical sync serrations in SYNC output.
D4	(EQUALIZER)	Timing for equalizing pulses in SYNC output.
D5	(H_SYNC)	Timing for horizontal sync portion of SYNC output.
D6	(B_FLAG)	Timing for BURST FLAG output.
D7	V_LATCH2	Positive (twice/line) 70 ns signal to latch the V Pulse PROM outputs, aligning them with the H Pulse PROM timing.

Output D0 of the H Pulse PROM clears the H Pulse Counter. U690A prevents this counter from being cleared and loaded simultaneously. Outputs D1-D6 provide the timing pulses to the Pulse Output Logic. Output D7 controls the timing of the V Pulse Latch (U783). Table 6-2 and Fig. 6-15 summarize the outputs of this PROM.

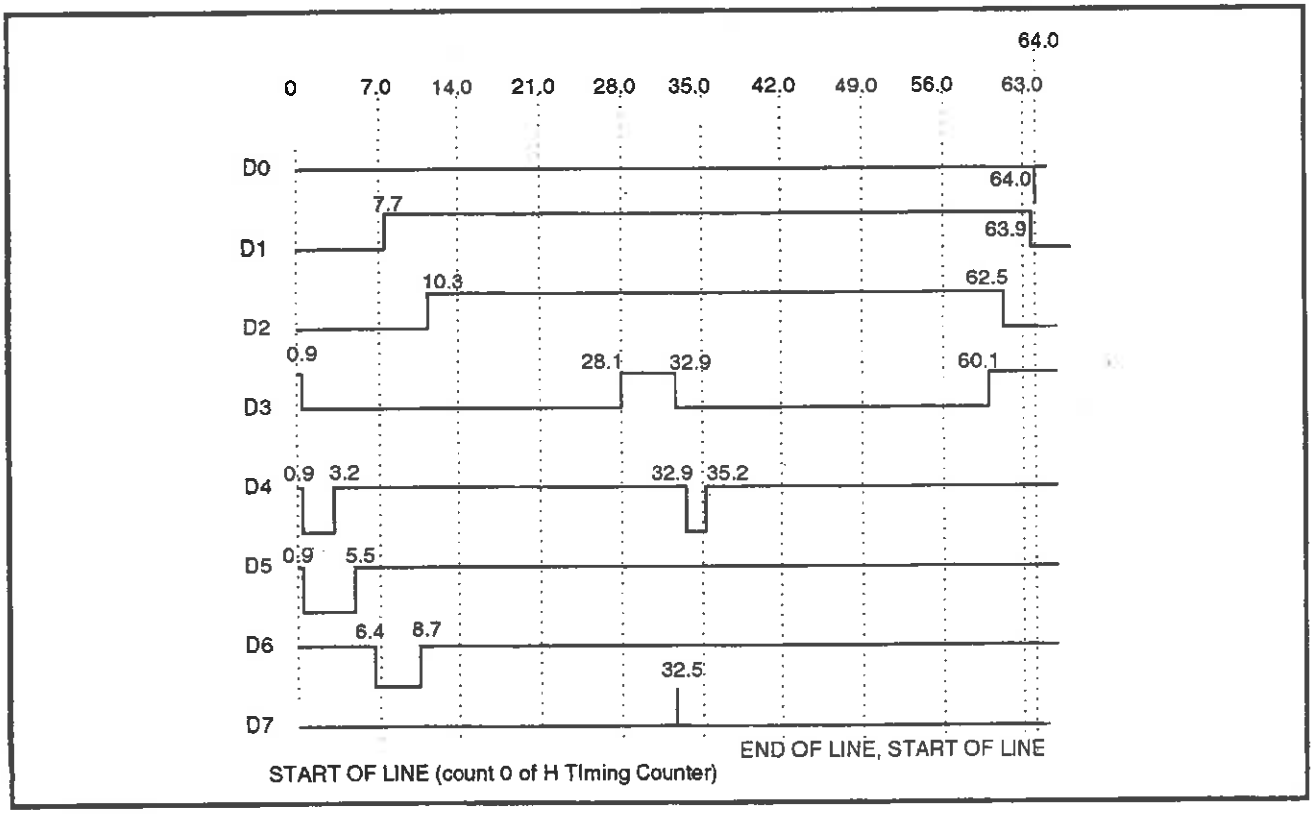
Vertical Timing

Vertical Counter

Four 4-bit counters (U988, U886, U786, and U687) make up the 13-bit Vertical Counter. Clocked by the 1135F_H clock, the Vertical Counter provides vertical timing for the V Pulse PROM (U796) and the V Timing PROM (U791). It does this by addressing the PROMs at a rate of 5000 counts per color frame [(625 counts/field)(8 fields)=5000 counts], one count occurring every half line. The counting cycle for the Vertical Counter is as follows:

Every half line, the V_CNT_EN output of the H Timing Decoder enables the counters for one clock cycle, allowing the clock to increment the counters once. This is repeated until the counters have reached a

Fig. 6-15. Horizontal Pulse PROM Output.



count of 5000 (9C4 hex), at which point gate U997 clears the counters with (VERT_CNT_CLR) to start a new color frame.

The V_CNT_EN signal is combined with 1H8 and 1V0 (in U994B, U994C, and U994D) to prevent the counters from clearing in the middle of a line when the instrument is operating as a master generator, i.e., when the Genlock Input is without sync.

When the Vertical Counter attempts to clear in the middle of the line, its timing is a half line off, and the 1V0 bit is high. Consequently, the 1V0 input locks out VERT_CNT_EN, making the Vertical Counter skip a count and thus shifting its timing by half a line.

When the instrument is operating in genlocked mode, the delayed FLD_REF signal inserts the genlock timing into the Vertical Counter just as it does for the H Timing Counter. That is, it delays the loading of the Vertical Counter's fixed offset. When the instrument is operating in internal mode, the delayed FLD_REF signal never occurs and the Vertical Counter is never loaded.

Jumpers J985 and J885 together advance vertical timing by as much as two lines or delay it by one line. The Vertical Timing table in Schematic ⑤ shows the appropriate jumper positions for advance/delay.

V Timing PROM

Addressed by the genlocked Vertical Counter, the V Timing PROM (U791) has two functions: (1) to provide vertical timing for the Signal Selection PROM (U356, ⑧) and (2) to provide vertical timing for the Component board.

Output D0 provides timing for APL & bounce signals. This signal has the following pattern throughout active video: high for 18 lines & low for 6 lines. Output D1 provides the timing pattern for the selection of horizontal lines in the convergence signal: low for 1 line every 20 lines. Outputs D2-D6 provide ITS selection, test signal matrix, & vertical sync timing as summarized in Table 6-3.

Table 6-3. Vertical Timing PROM. (U791)

DDDDD 65432	Signal Selected	Matrix Timing (lines in Field 1 shown)
00000	Equalizers	
00001	Serrations	
00010	Blanking	
00011	F1L7 White Flag	
00100	CCIR 17ITS	
00101	CCIR 18 ITS	
00110	CCIR330 ITS	
00111	CCIR 331 ITS	
01000	UK 1 ITS	
01001	UK 2 ITS	
01010	Unused	
01011	Unused	
01100	Unused	
01101	Unused	
01110	Unused	
01111	Unused	
10000		23.5 - 62
10001		63 - 82
10010		83 - 88
10011		89 - 104
10100		105 - 114
10101		115 - 145
10110		146 - 156
10111		157 - 166
11000		167 - 176
11001		177 - 187
11010		188 - 218
11011		219 - 228
11100		229 - 244
11101		245 - 250
11110		251 - 270
11111		271 - 310

Table 6-4. Vertical Pulse PROM Outputs.

Output	Signal Name	Function
D0	(PHASE_CLR_V)	Field 1 line 1 vertical phase clear.
D1	1/2_LINE	Half-line signal selection timing.
D2	(V_SYNC)	Timing for Sync output when D3 is low.
D3	V_DRIVE	High during vertical sync time.
D4	(VBL_22)	V-Timing for 24-line V-Blanking portion of Blanking output.
D5	(VBL_23)	Timing for 25-line V-Blanking portion of Blanking output.
D6	(FLD_REF)	Timing for Field Reference output (low during line 7 of field 1)
D7	(COLOR_FRAME_SQ_WAVE)	Timing for Color-Frame Square Wave output (low during fields 1-4; high during fields 5-8)

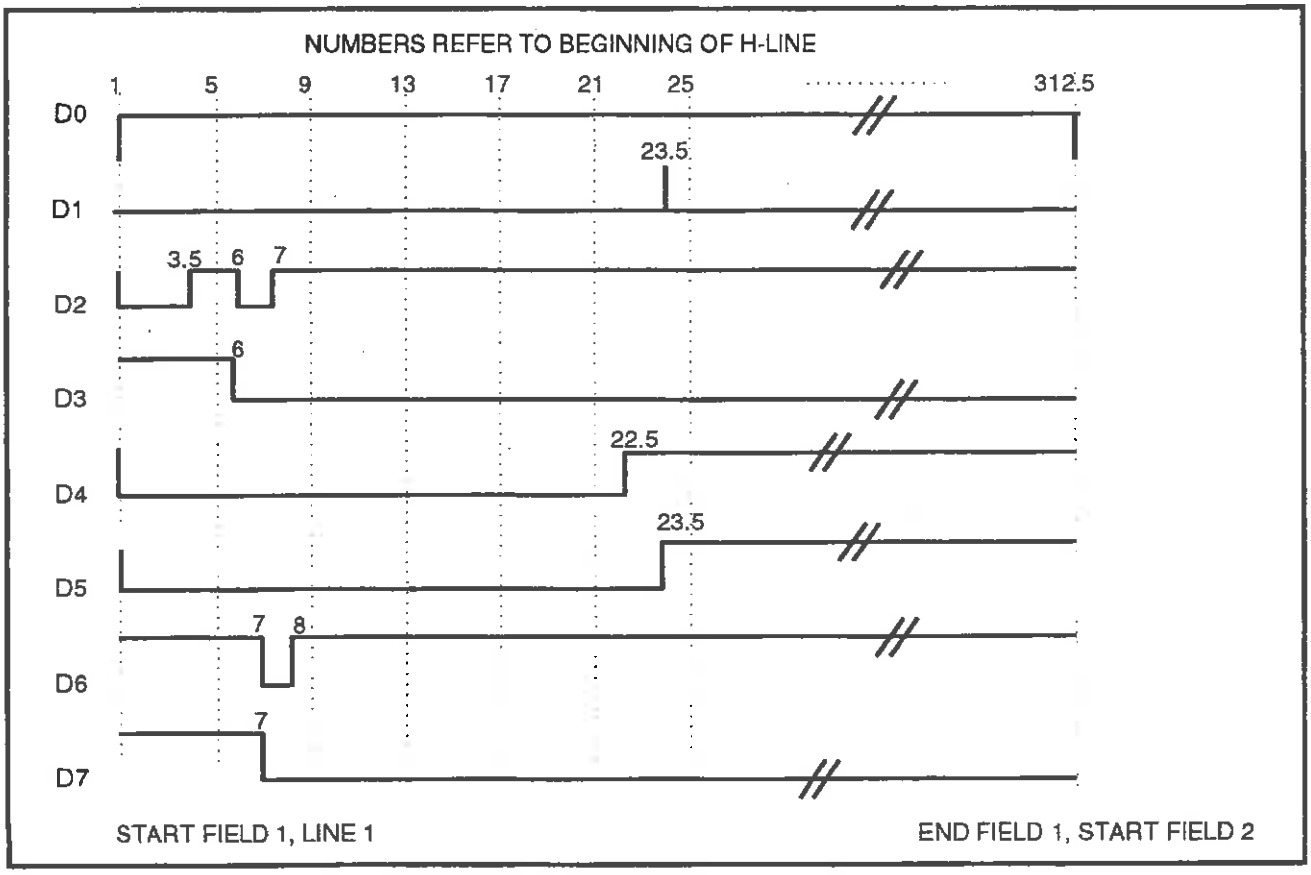
V Pulse PROM

The V Pulse PROM (U796) has three functions: (1) to produce vertical sync pulse components for the Pulse Output Logic, (2) to produce vertical timing for the Test Signal Selection Logic, and (3) to provide a vertical timing interrupt for the µP Kernel ②. Table 6-4 and Fig. 6-16 summarizes the outputs of this PROM.

The outputs of the V Pulse PROM are programmed to have advanced timing. This allows the V_LATCH2 signal from the H Pulse PROM to add the sync timing offset to the genlocked V Pulse PROM outputs applied to the Pulse Output Logic. It does this by either advancing or delaying the time at which these outputs are latched into U783.

Four of these outputs [D1-D3 and D6] are latched in U673 with V_LATCH1 (test signal timing) and are sent to the Test Signal Selection circuits ⑥, where they provide timing for the Signal Selection Logic.

Fig. 6-16. Vertical Pulse PROM Outputs (Field 1 of 4).



The latched D3 output of the V Pulse PROM (LV_DRIVE1 at U673 pin 2) is also sent to CTC1 (U245, ②) where it interrupts the µP to tell it to start servicing the front panel during the vertical interval when there is no Genlock Input signal.

NOTE

When a Genlock Input signal is present, the µP uses the vertical sync of the Genlock Input as a front-panel interrupt, not (LV_DRIVE1).

Pulse Output Logic

The Pulse Output Logic combines the outputs of the H and V Pulse PROMs to produce the sync pulse signals that are applied to the Pulse Output Drivers on the Analog board. It generates the pulse outputs as follows:

The two field reference signals, (PL_FLD_REF) and (L_COLOR_FIELD_SQ_WAVE), are derived from the V Pulse PROM and fed directly to the Analog board through inverting buffer U883.

The H Pulse PROM (U780) puts out the (H_BLKNG) signal slightly ahead of its other outputs. This allow shift register U693 and its associated gates to produce horizontal blanking pulses of different widths (see H Blanking Width table at J690 on ⑤).

Jumper J883 sets the vertical blanking width by selecting between (L_VBL_22) and (L_VBL_23), giving 24 or 25 lines of vertical blanking on the COMP BLANK signal (see V Blanking Window table at J883 on ⑤). Gate U991B combines the selected vertical and horizontal blanking signals and buffer U883 passes the signal to the Component board.

Multiplexer U697 uses L_VDRIVE2 and (PL_VSYNC) as select lines to determine which of three signals [(EQUALIZER), SERRATION, and (H_SYNC)] from PROM U780 make up the (COMP_SYNC) signal applied to the Analog board through buffer U883.

Multiplexer U697 also gates (B_FLAG) off during the vertical interval to produce the BURST_FLAG signal.

SIGNAL SELECTION ⑥

Signal Selection

The heart of the Signal Selection Logic is the Signal Select PROM (U356). Addressed by the µP ② and the Vertical Timing PROMs ⑤, the Signal Selection PROM provides the selection code that determines which test signal is generated.

When a test signal is selected at the front panel, the µP encodes the selection into an 8-bit data word and sends it to the Signal Selection PROM via latch U153. The V Timing PROM (U791 on ⑤) provides the Signal Selection PROM with timing for selecting split-field signals, including the vertical interval. The Signal Selection PROM output is latched in U352.

Luminance and Chrominance Segment Addressing

The Signal Selection codes are pointers into test signal segment look-up tables: the Luminance Segment Addressing PROM and the Chrominance Segment Addressing PROM (U454 and U460, respectively). The Luminance and Chrominance Segment Addressing PROMs are, in turn, pointers into tables of test signal segments. Each Signal Selection code causes the Segment Addressing PROMs to output a series of Segment addresses which describe the selected test signal.

The Luminance Segment Addressing PROM is addressed by: 6 bits from the Signal Selection PROM, the 7 most-significant bits from the Horizontal Timing Counter ⑥, and timing for generating half lines from the V Pulse PROM (U796 on ⑤). The Luminance Segment Addresses are latched in U450 and then presented to the inputs of the Luminance Segment Memory. (For troubleshooting purposes, jumper J551 can be moved to the 2-3 position to force the selection of a half-scale luminance signal.)

The Chrominance Segment Addressing PROM is addressed by: 5 bits from the Signal Selection PROM, the 7 most-significant bits from the Horizontal Timing Counter ⑤, and timing for generating half lines and correct PAL chroma phase from the V Pulse PROM (U796 on ⑤). The Chrominance Segment Addresses are latched in U464 and then presented to the inputs of the Chrominance Segment Memories. (For

troubleshooting purposes, jumper J470 can be moved to the 2-3 position to turn off the chrominance portion of the signal.)

Luminance Segment Memory

The Luminance Segment Memory is a 4K by 12-bit memory array made up of U639, U642, U645, and U648. The array is addressed with the 8-bit Segment Selection code (from U454) and the 4 least-significant bits of the Horizontal Timing Counter ⑤.

U639 contains the lower 8 bits of the lower half of the memory, while U642 contains the lower 8 bits of the upper half of the memory. U645 holds the upper 4 bits of the entire memory. Multiplexer U648 selects the appropriate outputs of U645, depending on which half of the memory is in use.

The 12-bit Luminance output is sent to the Luminance Adder ⑦.

Chrominance Segment Memory

The Chrominance Segment Memory consists of two memory arrays: the Chroma Differential Phase Memory and the Chroma Amplitude Memory.

The Chroma Differential Phase Memory is a 4K by 12-bit memory array made up of U661, U664, U667, and U467. The array is addressed with the 8-bit Segment Selection code (from U460) and the 4 least-significant bits of the Horizontal Timing Counter ⑤.

U661 contains the lower 8 bits of the lower half of the memory, while U664 contains the lower 8 bits of the upper half of the memory. U667 holds the upper 4 bits of the entire memory. Multiplexer U467 selects the appropriate outputs of U667, depending on which half of the memory is in use.

The 12-bit Chroma Differential Phase Memory output is sent to the Chroma Phase Adder ⑦.

The Chroma Amplitude Memory is a 4K by 8-bit memory array made up of U654 and U657. The array is addressed with the 8-bit Segment Selection code (from U460) and the 4 least-significant bits of the Horizontal Timing Counter ⑤.

U654 contains the lower 8 bits of the lower half of the memory, while U657 contains the lower 8 bits of the upper half of the memory.

The 8-bit Chroma Amplitude Memory output is sent to the Chroma Modulator ⑦.

VIDEO SYNTHESIS ⑦

Schematic ⑦ contains two separate but similar circuits: the Video Synthesizer and the CW Subcarrier Generator.

The Video Synthesizer takes the video components (luminance, chroma amplitude, and chroma differential phase) from Schematic ⑥ and combines them to form the composite representation of the test signal. This process is divided into five pieces: (1) the 25 Hz Offset Generator, (2) the Chroma Phase Adder and Chroma Generator, (3) the Chroma Modulator, (4) the Luminance Adder, and (5) the TTL-to-ECL Conversion.

The CW Subcarrier Generator takes timing information from Schematic ⑥ and generates a digital representation of a CW color subcarrier signal. This signal is used to lock the $4F_{SC}$ oscillator on the Analog board.

25 Hz Offset Generator

The 25 Hz Offset Generator (U632, U629, U526, and U726A) generates a pulse which represents the phase offset between the $1135F_H$ clock and the color subcarrier frequency.

If the digitized sine wave (in U861) were accessed at exactly four times the effective digitizing rate, the PROM outputs would represent a sine wave sampled at 0°, 90°, 180°, and 270°. Thus, the output sine wave would be at exactly one-fourth of the sample rate. If the phase increment was slightly above 90°, then the output sine wave would be at a slightly higher frequency.

In this generator, the master oscillator frequency is at 17.734375 MHz. But to generate the PAL subcarrier frequency, it is necessary to add a small phase offset to the phase pointer (enough to raise the generated frequency to 4.43361875 MHz). The output of the

25 Hz Offset Generator (U726A, pin 6) has the proper duty cycle to properly offset the phase in the Chroma Phase Adder.

Moving jumper J523 to the 2-3 position allows the Offset Generator to be disabled for troubleshooting.

Video Synthesizer

Chroma Phase Adder and Chroma Generator

The Chroma Phase Adder (U761, U764, and U767) adds the current chroma phase and the chroma differential phase signal (from ◈). The carry input to the adder is the output of the 25 Hz Offset Generator.

At the beginning of each color frame, the chroma phase in the Phase Accumulator (U864 and U867) is reset by (PHASE_CLR1). On every clock cycle, the 2's-complement Chroma Differential Phase signal is added to the current phase and the output of the 25 Hz Offset Generator, then the Chroma Phase Adder is updated.

The current chroma phase signal is a pointer into the digitized sine wave look-up table, Chroma Generator (U861). Its output is a representation of the phase-modulated subcarrier sine wave.

Chroma Modulator

The chroma sine wave from the Chroma Generator is multiplied (amplitude-modulated) by the Chroma Amplitude data (from ◈) in the digital multiplier (U856). The output of the multiplier is an unsigned representation of the chroma signal modulated on the color subcarrier.

The unsigned chroma signal is converted to a 2's-complement form by the XOR PALs (U752 and U852). Controlled by the chroma phase sign bit, SIGN, the XOR PALs invert the chroma signal and increment the signal by one (in the Luminance Adder) whenever the SIGN bit is asserted.

Luminance Adder

The Luminance Adder (U739, U742, and U745) adds the 2's-complement modulated chroma signal to the luminance signal (from ◈). The Adder's carry input is set whenever the chroma SIGN bit is asserted.

The outputs of the Luminance Adders are latched in U732 and U736.

TTL-to-ECL Conversion

The 12-bit output of the Luminance Adder latches are routed to TTL-to-ECL converters U811, U813, and U816 where they are converted from TTL levels to ECL. The ECL representation of the composite test signal, sampled at $1135F_H$, is then routed to the Analog board for D-to-A conversion.

CW Subcarrier Generator

The CW Subcarrier Generator (U836, U833, U839, U830, and U827) is a simplified version of the Chroma Phase Adder and Chroma Generator circuit. Counter U836 provides a pointer into the sine wave look-up PROMs (U830 and U827). The phase increment is 90° plus the delayed output of the 25 Hz Offset Generator SHIFTED_OFFSET.

Although the PROMs are only 8-bit devices, the bit SC_11 is latched in U726B and becomes the SIGN bit for the sine wave data. The output of the CW Subcarrier Generator is a 9-bit representation of the CW chroma subcarrier.

This signal is converted from TTL to ECL levels in U824, U821, and U819 and sent to the Analog board.

INPUT PROCESSING & TEST SIGNAL OUTPUT

◈9◈

(See Fig. 6-17)

Genlock Input Buffer

The AC-coupled Genlock Input Buffer inverts and amplifies the Genlock Input signal so that sync and burst fill the range of the Genlock ADC on the Digital board.

At the input stage, differential pair Q921 and Q924 isolate and current-amplify the Genlock Input signal. The second stage Q923 inverts and voltage-amplifies the signal. The third stage, an emitter follower (Q920), applies the signal to the input filter on the Digital board.

The signal is fed back to the input of the amplifier, at the base of Q921. Two other signals are also added in at the summing node: the Input Clamp feedback and the Burst Dither.

Input Clamp

By comparing the sync tip voltage of the Genlock Input signal with a -50 mV reference, the Input Clamp circuit generates a DC offset voltage to clamp the incoming signal to -50 mV. It does this as follows:

Monostable multivibrator U411A shortens the incoming 4.7 µs sync pulse detected by the Sync Stripper to about 2 µs. The shortened pulse enables U313, allowing it to generate a voltage equal to the difference between the sync of the input video applied to pin 3 and the -50 mV reference (U720A and associated components) applied to pin 2. The difference is stored in C212 for the remainder of the line. This correction voltage is applied to the base of Q921 through R915. Q951 clamps the sync tip of the Genlock Input to -50 mV.

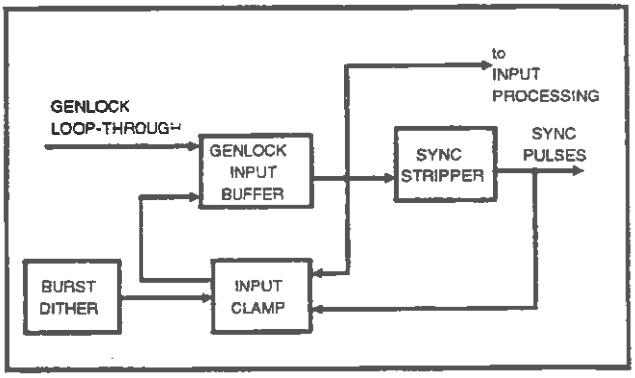


Fig. 6-17.
Block Diagram of the Genlock Input

Burst Dither

NOTE

Burst Dither is active only if a Genlock Input signal is connected and detected.

During burst, a sawtooth wave adds an increasing offset to the Genlock Input signal. This offset dithers the burst samples to improve sampling accuracy in the Genlock Data Acquisition circuits.

Q817 and C823 generate the sawtooth. A low (B_DITHER) pulse turns off Q817 just before burst and leaves it off until just after burst. During this time, resistor R814 charges C823 to produce the sawtooth. This signal feeds to the Genlock Input buffer through R916.

Sync Stripper

The Sync Stripper extracts sync pulses from the buffered Genlock Input signal and applies them to the Input Clamp and the Genlock Data Acquisition circuits ◈3◈. C806 filters off the chrominance portion of the Genlock Input. The remainder of the signal goes to the sync peak detector U710A and inverting op amp U710B. U511 compares the output of these devices and produces the composite sync.

In addition to driving the Clamp circuit, the stripped sync signal is applied to the µP Kernel through U240 ◈2◈.

The second half of this schematic is the Test Signal Output. The block diagram for this section is given in Fig. 6-18.

Output DAC

DACs (U250 and U350) are 6-bit digital-to-analog converters which convert the test signal data into an analog output signal.

The output of the DAC is a current source which is converted to voltage in the resistor network. The resistor network also acts as a weighting summing node to add both the upper and lower set of bits.

Output Clamp

The filtered test signal is applied to Chroma Notch filter (L327 and C330) and to the negative input of U227. During the burst time, Q222 enables U227 to force the test signal blanking level to ground. To do this, U227 generates a correction voltage across C327. The correction voltage is buffered by U427 and applied to the Filter through a resistor network.

Output Filter & Delay

To remove out-of-band signal components, the analog test signal from the Output DAC is filtered by a low-pass filter.

The first three sections of the filter (L551, L650, L750, and associated capacitors) form a 7-pole elliptic low-pass reconstruction filter. The last section (L450, L550, and associated capacitors) is a group-delay corrector. Because the Black signal goes through more processing than the Test Signal; L751, C750, and C752 act like a delay line to phase match the Test Signal output with the Black output.

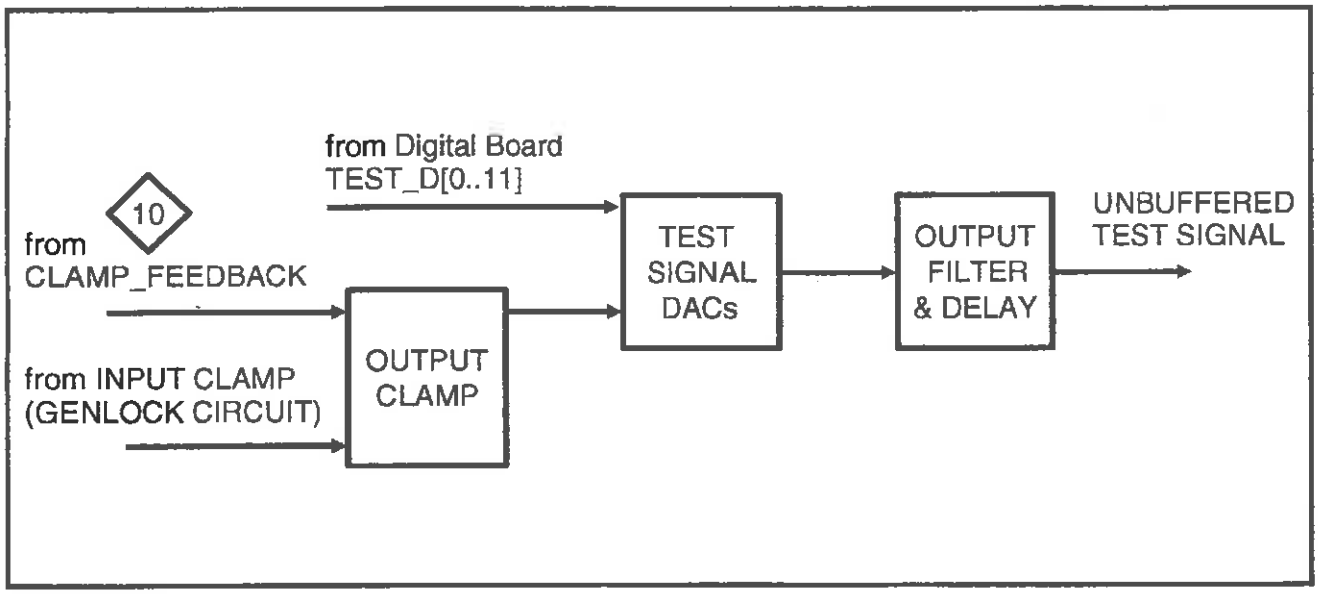


Fig. 6-18. Block diagram of the Test Signal Output.

BLACK BURST GENERATION & PULSE OUTPUTS

(See Fig. 6-19)

Test Signal Output Amplifier

Taken from the Output Filter, the test signal is buffered by an op amp U721. The feedback resistor, R758, adjusts the gain of the amplifier and C753 adjusts the sin x/x compensation.

Black Burst Generation

The Black Amplifier generates the black signal by using the currently-generated test signal and inserting blanking-level during the active video portion of the signal.

Taken from the Output Filter, the test signal is buffered by an op amp U970. The feedback resistor, R771, adjusts the gain of the amplifier and C775 adjust the sin x/x compensation.

It is then applied to a switchable amplifier (U980). The BB_ENABLE (from 

) signal controls the switching on and off of the signal. During the horizontal sync interval, BB_ENABLE switches on allowing the sync and burst to pass. During active video, the test signal is turned off. The output of the switchable amplifier is sent to driver, U755, which amplifies the signal to drive 8 video outputs and provides 75Ω terminations.

PULSE OUTPUTS

The Pulse Outputs are configurable to allow the user to use Comp Sync and Blanking or extra copies of the Black Output.

The Pulse Outputs are generated from the Pulse Output Logic (U883 on 

). Two identical pulse output amplifiers shape the edges of the pulse signals and convert from TTL to -2 V or -4 V levels.

Taking the first amplifier as an example, the pulse is normally low. This shuts off Q785, which in turn shuts off Q872 and the output goes to zero. When the pulse input is high, current source Q 785 charges C888. The rising voltage across the capacitor is buffered by Q878 and amplified by Q872 and the output falls. The capacitor voltage is clamped by Q793 and Q786, limiting the voltage swing to the desired value. The gain of the output is changed by changing the resistance in the emitter of Q872 (via jumper J780).

If more copies of the Black are wanted move P13 to J950 (Black now at Sync/Black output) and/or move P14 to J960 (Black now available at Blanking/Black output).

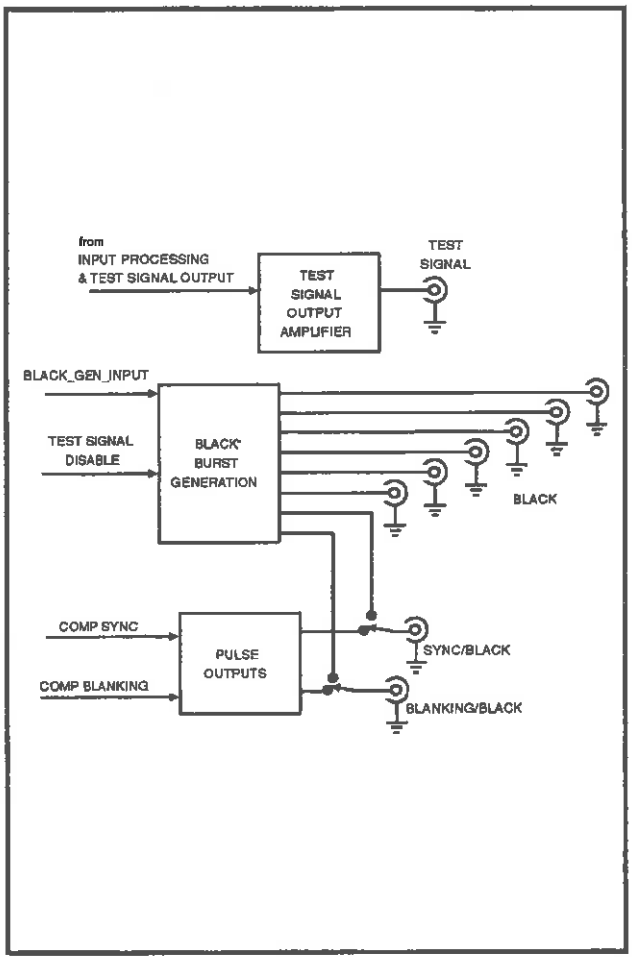


Fig. 6-19. Black Burst Generation & Pulse Outputs.

COMPONENT DIGITAL GENERATION ⑪

(See Fig. 6-20)

Signal Selection

The Signal Selction is one IC, U10, that takes the component test signal selected from the front panel (via the µP Kernel ②)and the vertical count from the V Timing PROM ⑤ and derives control signals for the Signal Address Memory [S[0..2] and VC[0..2]].

Signal Address Memory

The Signal Address Memory takes the Horizontal count from the H Timing Counter ⑤ along with control signals from the Signal Selection to derive the address for the Signal Data Memory in EPROM U1 and U11. The address, AD[0..9], in U29 and U31. U30 Latches the control signals need for the Signal Data Memory.

Signal Data Memory

With the address signals from the Signal Address Memory the Signal Data Memory outputs the digital signal for each of the three channels. The signals are then sent to the Component Channel Analog Output.

Clock Phasing & Level Conversion

The Clock circuit converts the ECL_CLK_1A and (ECL_CLK_1A) signals from the Digital board into three single ended clocks which control the Channel DACs. The two tank circuits for CH2_CLK and CH3_CLK are for channel matching, allowing the other channels to be brought into phase with channel 1.

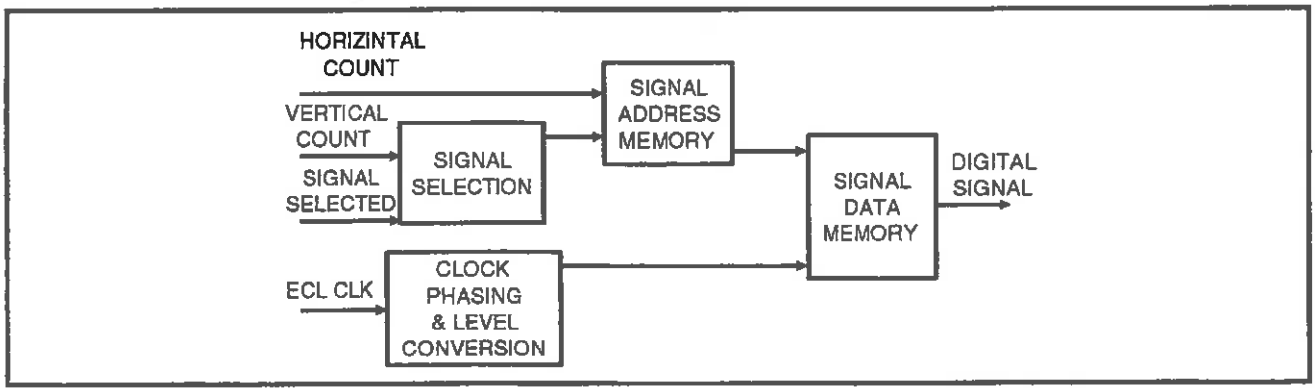


Fig. 6-20.
Block diagram of the Component Digital Generation circuitry.

COMPONENT CHANNEL 1, CHANNEL 2, and CHANNEL 3 ANALOG OUTPUT

◈12◈, ◈13◈, & ◈14◈

(See Fig. 6-21)

NOTE

Since all three channels are identical, only Channel 1 is described.

Channel 1 DAC

DAC U14 takes the digital signal from the Signal Data Memory ◈ CH1D[0..9] and converts it to an analog voltage. The DAC is clocked by the CH1_CLK which is exactly in phase with the other channel clocks keeping all of the channels in phase.

Jumper J2 is for checking the return loss of the Channel Output Amplifier. When J2 is in the 2-3 position, the DAC output is grounded and the test signal is at 0 Volts. This allows the return loss of the Channel Output Amplifier to be tested. In the 1-2 position, the DAC output is passed directly to the Output Filter.

Channel 1 Output Filter

To remove out-of-band signal component, the analog test signal from the Channel DAC is filtered by a low-pass reconstruction filter that is terminated in 75 Ω. The front end of this filter provides group delay correction, and the following stages provide the reconstruction filtering.

Channel 1 Output Amplifier

Taken from the Output Filter, the test signal is buffered and amplified enough to drive a 75 Ω load by op amp U15. The feedback resistor, R19, adjusts the gain of the amplifier and C11 adjusts the sin x/x compensation.

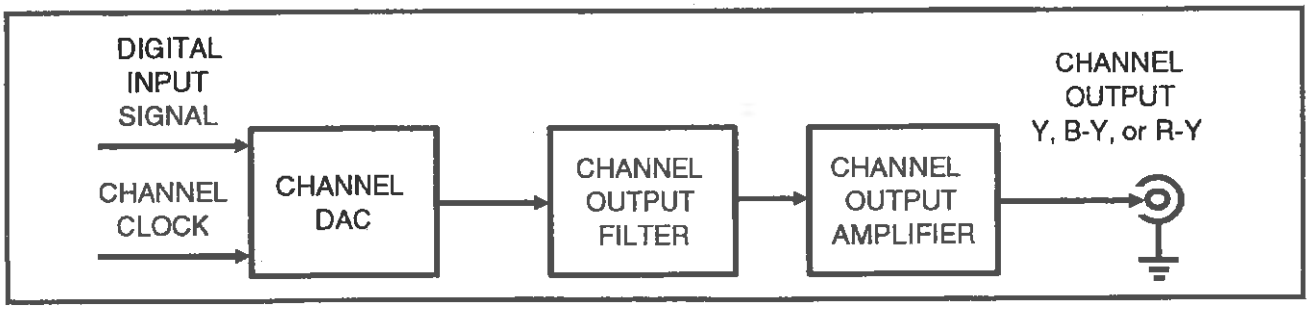


Fig. 6-21. Block diagram of the Component Channel out

POWER SUPPLY CIRCUIT DESCRIPTION 15

This type of power supply is called a current-mode-controlled, discontinuous, flyback, switching power supply. See Fig. 6-22 for a functional block diagram. The current output is distributed between the four supplies as follows:

+ 12 V	0.5 Amps max
+ 5 V	7 Amps max
- 5 V	2 Amps max
- 12 V	0.5 Amps max

The maximum power is limited by the maximum current in the primary of T440. This is also the only current limit for the ± 5 V supplies, as they have no secondary current limit. The ± 12 V supplies are current limited in the secondaries by the ± 12 V linear regulators, U176 and U276.

The power inductor, T440, is driven by switching the current to its primary on and off. T440 is not used as a transformer, but as an energy storage device, storing the energy in the primary while the current is being applied. On the second half of the switching cycle the current in the primary is switched off, and the energy stored in the primary is transferred to the secondaries (flyback). Regulation is accomplished by applying feedback from the +5 V supply to the Pulse Width Modulator controlling the current to the primary. This varies the length of time that the current is applied to the primary, causing it to store either more or less energy.

There is also circuitry to provide for operation from both 110 and 220 V_{ac} supplies, under-voltage shutdown if the ac input is too low, overvoltage protection (crowbar) on the +5 V supply, and shutdown circuitry which forces a restart of the supply if it remains in current limit for more than a short period of time (<1 second).

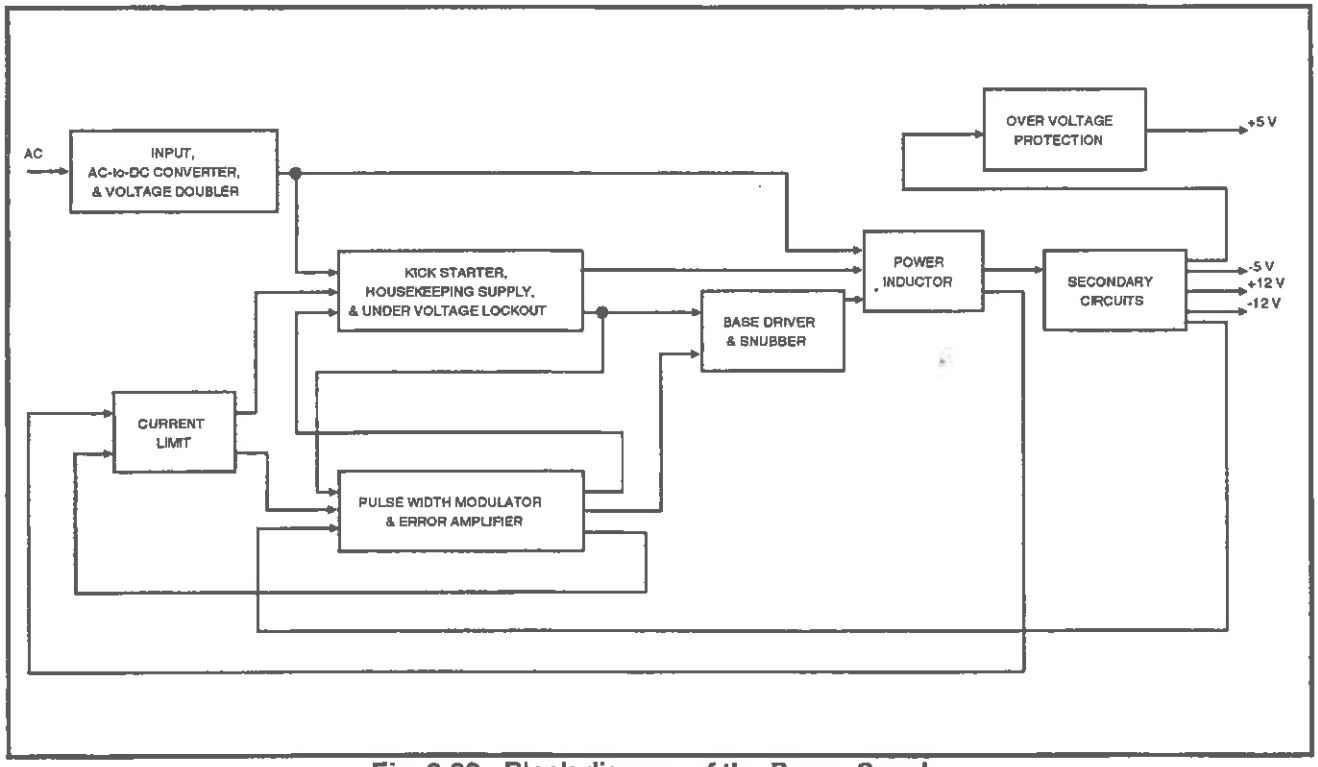


Fig. 6-22. Block diagram of the Power Supply.

WARNING

All primary voltages are referenced to a floating ground, not chassis ground. An isolation transformer or differential amplifier is needed in order to troubleshoot the circuitry in the primary, the Pulse Width Modulator, and their supporting circuitry.

As the current never flows simultaneously in both the primary and the secondary, there is never any actual transformer action. As the magnetic flux in the inductor go to zero at the end of each switching cycle, it is discontinuous.

Input, AC to DC Converter, and Voltage Doubler

This circuitry filters and rectifies the input ac voltage, placing a charge of approximately 320 V_{dc} across capacitors C845 and C865.

The line current passes through line filter LF950, fuse F940, and power switch S930, and is applied to rectifier CR820. At the input of CR820, J810 is used to select between 110 V and 220 V operation. If set to 220 V, CR820 works as a full-wave rectifier and C845 and C865 act in series, charging to the peak voltage (approximately 320 V_{dc}) during the first part of each one-half cycle. They then maintain that voltage through the rest of the cycle, as the input voltage and current falls to zero.

If, on the other hand, J810 is set for 110 V operation, CR820, C845, and C865 act as a half-wave rectifier and voltage doubler. During the positive half-cycle of the ac input, only one of the diodes within CR820 conducts, charging C865 to the peak positive voltage. A different diode within CR820 conducts during the negative half cycle, and charges C845 to the negative peak. The total voltage across C845 and C865 is then approximately 320 V_{dc}. RV920 and RV820 limit voltage surges on the input which might pass the line filter, while R831 and R830 discharge C865 and C845 when the power is off. C830 and C730 bypass switching noise to ground, keeping it out of the input power line. DS720 and associated parts form a relaxation oscillator, so DS720 blinks when the instrument is powered up.

Kick Starter, Housekeeping Supply, and Undervoltage Lockout Circuits

These circuits supply the power to start and maintain oscillation of the Pulse Width Modulator, so long as the input ac voltage is sufficient to maintain regulation. The primary purpose of the undervoltage lockout circuit is to prevent the supply from starting up when set for 220 V operation and 110 V is applied instead, but it will stop oscillation in the Pulse Width Modulator whenever the voltage across C845 and C865 (normally at 320 V) falls below approximately 200 V.

VR765 holds the emitter of Q755 at about 20 V, while the base is controlled by a divider comprised of R766, R676, and R768. So long as the charge across C845 and C865 remains around 320 V, Q755's base is held at approximately +30 V, and the transistor is off. As the voltage across C845 and C865 decreases, the base voltage does as well; when the voltage across the caps is down to approximately 200 V, Q755's base is at about +19 V, and Q755 is turned on. This, in turn, turns on Q727, applying the +5 V reference from U722-8 to U722-2. This disables the Pulse Width Modulator.

When the input voltage is sufficient to maintain the charge across C845 and C865 above 200 V, Q755 is off. This allows the Kick Start circuit to operate, providing the initial power to start up the Pulse Width Modulator. It does this by charging up C656 through Q667 and R560. During start-up, the +5 V reference output of U722 is at 0 V, and Q660 is off. The base current for Q667 during this time is supplied by R667.

When the charge across C656 reaches approximately 16 V, U722 starts to operate. It switches Q638 on and off through the base drive circuitry (Q741, Q750, Q648, and associated circuitry). The +5 V reference voltage at U722-8 is developed, which turn Q660 on. This diverts the base current from Q667, so it turns off and DS670 turns on to indicate normal operation.

The power to maintain the +16 V charge on C656 is now provided by the housekeeping winding of T440, pins 5 and 6 through CR556. If there is insufficient power to maintain the charge on C656 for any reason, such as the removal of J660, then the charge on C656 is quickly depleted. This stops the operation of U772, and the kick start sequence is repeated.

Power Inductor Operation

The heart of this power supply is T440, the multiwinding power inductor. The operation of T440 is as follows: (See Fig. 6-23.) Inductor T440 is initially uncharged (has zero magnetic flux). Q638, acting as a switch, is turned on by the base drive from U722. This places the charge developed on C845 and C865 (approximately 320 V) across the primary winding. The polarity of the charge is such that the voltages induced in the secondaries all reverse bias their respective diodes (note the polarity dots). In this way, there is no current flowing in the secondaries while it is flowing in the primary.

The primary current builds a linear ramp, storing the energy in T440 according to the relation $E=\frac{1}{2}Li^2$, where L is the primary inductance and i is the current flowing through it.

The current path is broken when Q638 is switched off, so current stops flowing in the primary. The flyback action of T440 then causes the voltages in the secondaries linearly ramps down to zero as the energy which was stored in T440's primary is delivered to the load, charging the output capacitors.

When all of the energy which was stored in T440 during the first half of this cycle is delivered to the load, the current in the secondaries is at zero, and the diodes turn off. There is no current flowing in either the primary or the secondaries until Q638 is turned back on to start the next cycle. As there is not a continuous flow of energy in T440, this is called discontinuous flyback operation.

Load regulation is provided by sensing the +5 V supply with a divider comprised of R314, R315, and R415, and using U410 to convert this to an error signal. This error signal is optically coupled through U520 back to the Pulse Width Modulator, U722. U722 uses the error signal to vary the width of the pulse which drives Q638.

When +5 V goes too high, U722 narrows the pulse width. This reduces the amount of energy stored in T440, and therefore the amount transferred to the load, so the +5 V goes down. Inversely, when the +5 V is too low, the pulse width is increased, increasing the amount of energy stored in T440 and then transferred to the load, so the voltage goes up.

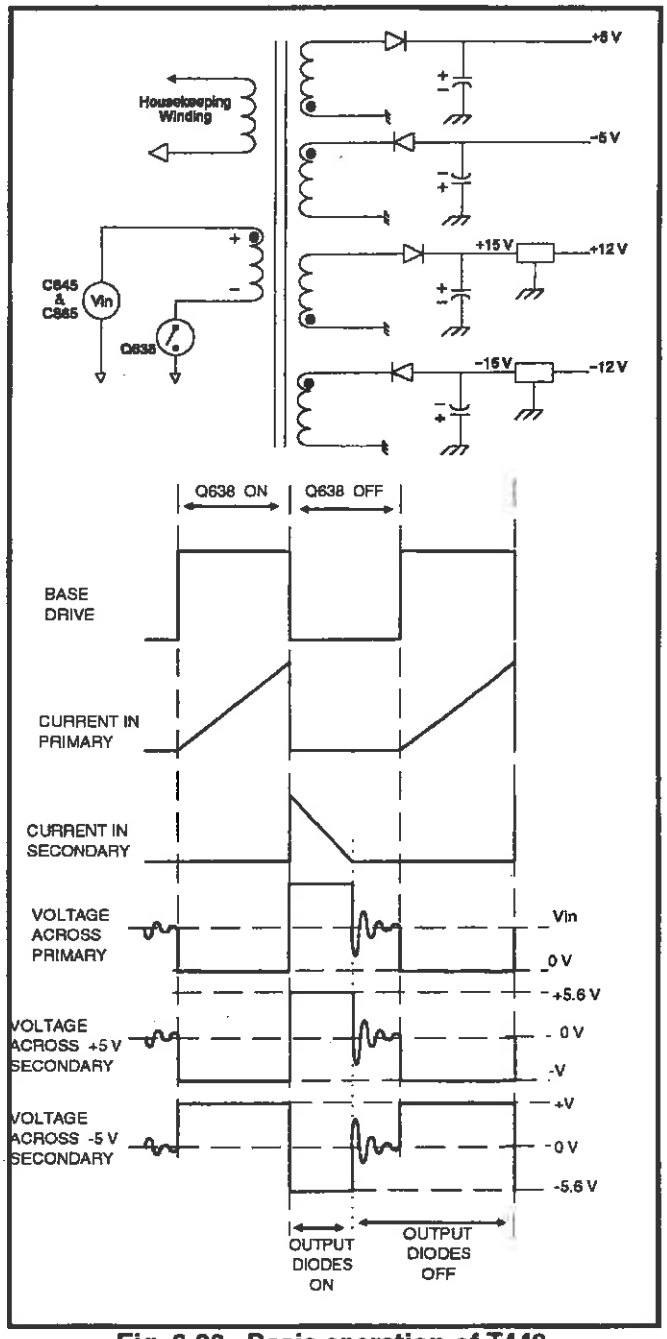


Fig. 6-23. Basic operation of T440.

Pulse Width Modulator and Error Amplifier

The Pulse Width Modulator, U722, is a current-mode controller. It uses inputs from the primary circuit and from the +5 V output to vary the width of the pulse which controls Q638, as mentioned above. This regulates the secondary voltages through variations of input voltage, output load, temperature, etc.

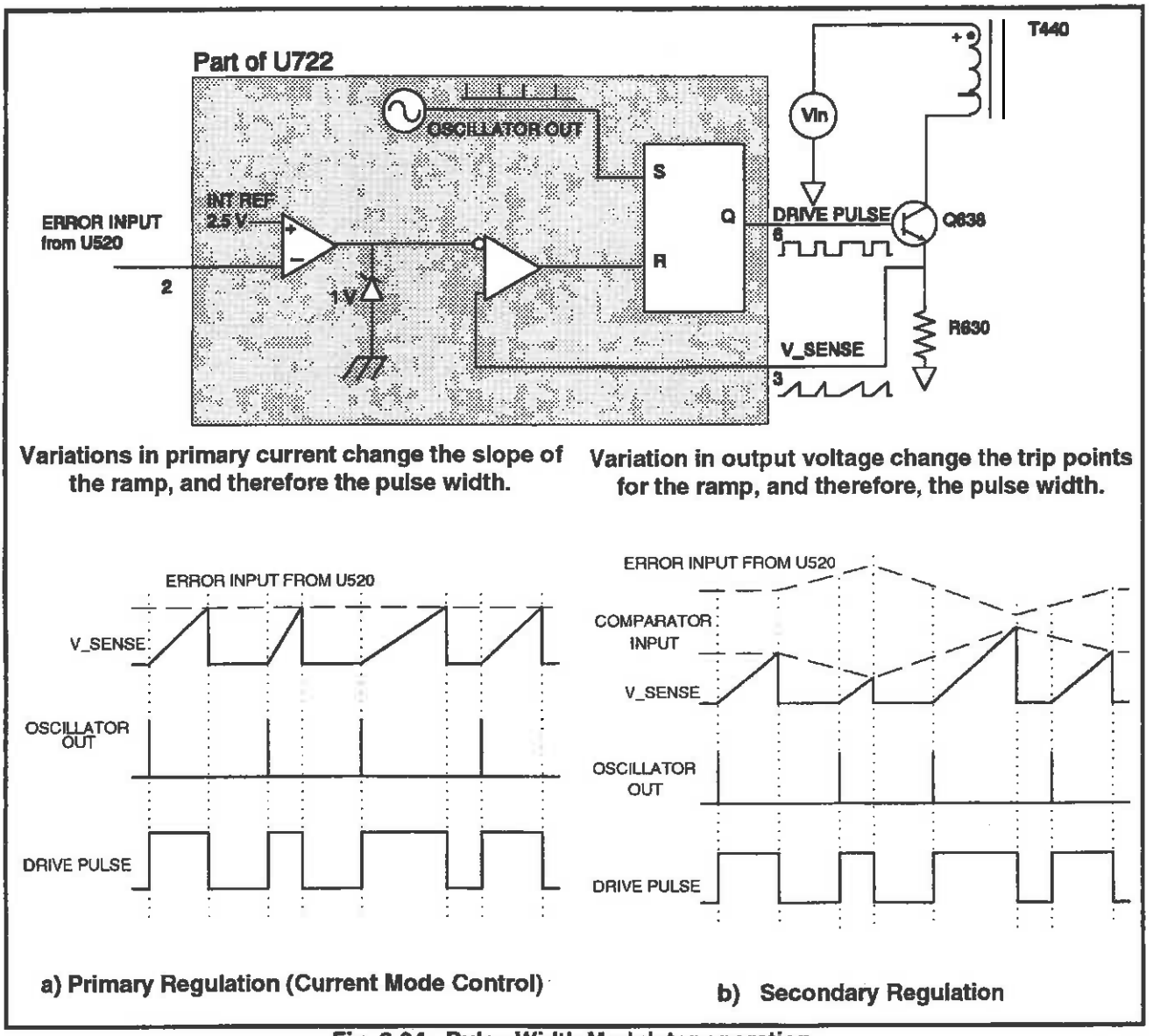


Fig. 6-24. Pulse Width Modulator operation.

Current mode control works by allowing the current flowing in the primary to reach a peak level that is set by the output of the error amp, which is controlled by the +5 V output (see Fig. 6-24). The current in the primary winding is sensed by R630, and applied to U722-3 as a voltage. At the start of the cycle the oscillator sets the flip-flop within U722, which turns on Q638. The primary current, and therefore the voltage to U722-3, ramp up until the I_SENSE level is sufficient to trip the comparator. This resets the flip-flop, ending the drive pulse to Q638, and the energy stored in the transformer is transferred to the secondaries.

Line regulation, then, is a function of line voltage. As the line voltage varies, so will the primary current. An increase in line voltage causes an increase in primary current, so the slope of the ramp increases and the trip point is reached sooner. This results in a shorter pulse width. A decrease in line voltage causes a decrease in primary current, the slope of the ramp decreases, and it takes longer to reach the trip point. However, the same peak current is reached in both cases, so the same amount of energy is transferred to the load. Line regulation is then achieved without having to wait for output voltage variations.

Load regulation is accomplished by sensing the output voltage of the +5 V supply, and applying an error signal through the optoisolator U520 to U722-2. If the load increases, the supply voltage decreases, and so does the error signal at U722-2. This has the following results:

1. The comparator input increases, due to the inversion of the IC.
2. The output pulse width increases, keeping Q638 on for a longer time.
3. I_p increases.
4. Power flow increases.

On the other hand, if the load decreases, the +5 V increases, so the output pulse width decreases along with Ip, and less power is transferred to the secondaries. In this way, the +5 V is kept constant through changes in the load, and, as it varies the amount of energy transferred to the other secondaries too, it regulates them as well.

The error amplifier is U410, a band-gap reference. It keeps the voltage at its cathode at a constant 2.5 V, set by the voltage applied to its reference, pin 2. This reference is set by R314, R315, and R415. R415 is also used to adjust the +5 V supply.

As U410's cathode is held at 2.5 V, the current through R416 will vary with changes in the output voltage, as will the current through the LED within optoisolator, U520. This changes the conductance of the transistor element of the optoisolator, which then varies the voltage applied to the feedback input, U722-2.

Current Limit

Current limit is provided for the primary circuit by the internal circuitry of U722. As the ramp voltage at U722-2 reaches 1 V, the output drive pulse ends. This shuts Q638 off, so no further current is supplied. The maximum primary current is approximately 1.5 Amps, which corresponds to a maximum power level of approximately 75 Watts.

As supply goes into current limit, U615A and Q717 come into play. U615A starts to turn on as the ramp voltage passes approximately 900 mV, and starts to charge C717. If the current limit condition persists long enough for the charge on C717 to reach 700 or 800 mV, Q717 is turned on. This applies the reference voltage from U722-8 directly to U722-3, shutting down the supply and forcing a kick start. The supply will then cycle through kick start, current limit, and shutdown until the problem is corrected.

Base Drive and Snubber

The pulse width modulator drive pulse from U722-6 is amplified by emitter followers Q741 and Q750. When the drive pulse is positive, Q750 is on and Q741 is off. Current flows through R746 and R747, through Q648 and CR649, and turns Q638 on. CR640, CR648, and CR649 form a Baker clamp to keep Q638 out of hard saturation.

As Q638 approaches saturation its collector-emitter voltage differential falls, and it needs less base current to maintain the same collector current. As saturation is approached, then CR640 starts to conduct, providing a path for the excess base current.

When U722-6 goes to 0 V, Q750 is shut off and Q741 is turned on, so current is shunted to ground through CR651. C648 and VR650 speed up the switching off of Q638. The driven side of C648 is charged to approximately 5 V during the positive half-cycle; then, when Q741 is turned on, C748's driven side is pulled down to +0.7 V by CR651, which pulls the base of Q638 down to approximately -3.3 V, through CR684. This abrupt transition draws a large current spike from the base momentarily (approximately 1 A for <0.3 µs), turning off Q638 very rapidly, along with CR640 and CR649.

When Q638 is turned off, there is a voltage spike applied to its collector. A combination of reflected secondary voltages, input voltage, and transformer leakage inductance can combine to produce a spike of over a thousand volts. Since this can exceed the ratings of Q638, a snubber circuit, consisting of C540, CR545, and R647, limits the spike to approximately 800 V.

Secondary Circuits

The secondary circuits all work in the same manner. As mentioned earlier, under basic operation, during the first half of the cycle, all their diodes are reverse-biased, so there is no current flow.

On the second half of the cycle, when Q638 is shut off, the flyback action reverses the polarities of the secondaries, and the diodes are forward-biased. This allows the energy stored within T440 to charge up the capacitors in the secondaries.

The +5 V and the -5 V supplies use LC filters from this point, to further smooth the voltage and eliminate most of the ripple.

The +12 V and -12 V supplies actually start as +15 V and -15 V, at the transformer. These voltages are used for the fan, B100 (-15 V), and for the optoisolator (+15 V) only. Then they are filtered and applied to linear regulators, U176 and U276, which provide clean +12 V and -12 V outputs, respectively. CR169 prevents the +12 V from going negative, while CR170 keeps it from exceeding +15.7 V. CR269 and CR369 perform identical functions for the -12 V output.

Overvoltage Protection

Overvoltage protection is provided on the +5 V output by a crowbar circuit comprised of Q127, VR120, and R120. If the +5 V output exceeds approximately +5.5 V, VR120 will start to conduct. When VR120 is drawing enough current through R120 to raise SCR Q127's gate voltage above its cathode, Q127 will turn on. This shorts the +5 V output to ground, forcing the primary circuit into current limit.