Data Timing Generator

▶ DTG5078 • DTG5274

New serial data standards, expanding networks, and ubiquitous computing continually redefine the cutting-edge of technology. The design engineer is challenged to economize without sacrificing performance.

The DTG5000 Series combines the power of a data generator with the capabilities of a pulse generator in a versatile, benchtop form factor, shortening the duration of complex test procedures and simplifying the generation of low-jitter, high-accuracy clock signals or serial data across multiple channels. Its modular platform allows you to easily configure the performance of the instrument to your existing and emerging needs to minimize equipment costs. Two mainframes and three plug-in output modules combine to cover a range of applications from legacy devices to the latest technologies. In addition, eight low-current, independently-controlled DC outputs can substitute for external power supplies. Each mainframe incorporates a full compliment of auxiliary input and output channels to easily integrate with other instruments, such as oscilloscopes and logic analyzers, to create a flexible and powerful lab.

▶ Features & Benefits

Up to 2.7 Gbps Data Rate Extendable to 3.35 Gbps

From 2 to 96 Data Channels (Master/Slave) and Close to 1,000 Through Clock Synchronization

Class Leading Delay Resolution and Range
- 0.2 ps (DTG5274), 1 ps (DTG5078) Delay Resolution
- Up to 600 ns of Total Delay

Versatile Platform Combines Features of Data Generator, Pulse Generator, and DC Source

Advanced Control over Signal Parameters to Meet Most Current Testing Needs; Like Stressed Eye Generation
- Built-in Jitter Generation and Crossing Point Control
- Level Control with 5 mV Resolution
- Variable Edge Slew Rates

Easy to Use and Learn Shortens Time to Test
- Plug-in Modules Easily Configure Instrument to Your Needs
- Intuitive User Interface Based on Windows 2000
- Convenient Benchtop Form Factor

Up to 32 Mbit Pattern Depth Supports Long Data Patterns

▶ Applications

Semiconductor Device Functional Test and Characterization

Support for Semiconductor Technologies from TTL to LVDS Depending on Output Module

Compliance and Interoperability Testing to Emerging Standards
- PCI-Express
- InfiniBand
- Rapid IO
- DVI
- HDMI

Magnetic and Optical Storage Design
- Characterization and Functional Testing of Next-generation Magnetic and Optical Storage Devices (HD, CD/DVD/Blue-ray)

Jitter Transfer and Jitter Tolerance Testing

Tektronix
Enabling Innovation

▶ Characteristics

Mainframe Characteristics

Basic Features

Platform – Benchtop mainframe with cold swappable plug-and-play plug-in output modules. Mainframes accept any combination of output modules.

Number of slots for output modules –
DTG5078: 8 slots (A, B, C, D, E, F, G, H).
DTG5274: 4 slots (A, B, C, D).

Master-Slave Capabilities –
DTG5078: Up to three DTG5078 mainframes can be connected in Master-Slave configuration.
DTG5274: Up to two DTG5274 mainframes can be connected in Master-Slave configuration.

Operating Modes –
Pulse Generator Mode (slots A to D only).
Data Generator Mode.

Output Patterns –
Slot A to D: NRZ, RZ, R1, Pulse patterns.
Slot E to H: NRZ only.

Timing Parameters

Data Rate Range –
DTG5078:
- NRZ: 50 Kbps to 750 Mbps extendable to 800 Mbps.
- RZ, R1, Pulse Mode: 50 Kbps to 375 Mbps extendable to 400 Mbps.

DTG5274:
- NRZ: 50 Kbps to 2.7 Gbps extendable to 3.35 Gbps.
- RZ, R1, Pulse Mode: 50 Kbps to 1.35 Gbps extendable to 1.675 Gbps.

Data Rate (Setting) Resolution –
Internal Clock: 8 digits.
External Clock: 4 digits.
External Phase Lock In: 4 digits.

Output Timing Controls

Delay Range –
PG Mode: 0 to 3 µs.
DG Mode:
- Long Delay Off: 0 to 5 ns (NRZ, RZ, R1).
- Long Delay On: NRZ:
  - period ≥1.25 ns: 0 to 300 ns (Hardware sequence) or to 600 ns (Software sequence).
  - period <1.25 ns: 0 to (480 ns x period) (Hardware sequence) or to (240 ns x period) (Software sequence).
- Long Delay On: RZ/R1:
  - period ≥2.5 ns: 0 to 300 ns (Hardware sequence) or to 600 ns (Software sequence).
  - period ≥2.5 ns: 0 to (240 x period) (Hardware sequence) or to (120 ns x period) (Software sequence).

Delay Resolution –
DTG5078: 1 ps.
DTG5274: 0.2 ps.

Phase Resolution – 0.1%.

Differential Timing Offset Feature [Between Pair of Two Adjacent Channels (Odd and Even)] –
Range: –1.0 to 1.0 ns.
Resolution:
- DTG5078: 1 ps.
- DTG5274: 0.2 ps.

Semiautomatic Deskew Calibration –
Range: 500 ps.
Accuracy (after skew calibration):
- 100 ps, slots A to D.
- 200 ps, slots E to H.

Duty Cycle Adjustment Range – 0 to 100% (with 0 delay setting, RZ, R1, Pulse mode only).

Duty Cycle Adjustment Resolution – 0.1%.

Pulse Width Maximum Range – 290 ps to (period - 290 ps) (RZ, R1, Pulse mode only). (Range also depends on delay settings)

Pulse Width Resolution – 5 ps.

Jitter Performance (Output Channels)

Clock Pattern ("1010..." Clock Pattern)
Random Jitter –
DTG5078:
- <4 ps_{RMS} (at 750 Mbps with DTGM20, 0.8 V_{p-p}, slew rate: 2.25 V/ns, delay: 0.0 ns).

DTG5274:
- < 3 ps_{RMS} (at 2.7 Gbps with DTGM30, 0.8 V_{p-p}, delay: 0.0 ns).

Data Pattern (PRBS Pattern 2^{15}-1)
Total Jitter –
DTG5078:
- <18 ps, <85 ps_{p-p} (typical) (at 750 Mbps with DTGM20, 0.8 V_{p-p}, slew rate: 2.25 V/ns, delay: 0.0 ns).

DTG5274:
- <16 ps, <60 ps_{p-p} (typical) (at 2.7 Gbps with DTGM30, 0.8 V_{p-p}, delay: 0.0 ns).

Signal Control Features

Cross-point Adjustment (Duty Cycle Distortion) –
Range: 30% to 70%.
Resolution: 2%.
(Slots A to D, and DTGM30 used in NRZ mode)

Jitter Generation –
Jitter All or Partial Pattern.
Jitter Profile: Sine, Gaussian Noise, Square, Triangle.
Jitter Freq./Res.: 0.015 Hz to 1.56 MHz/1 MHz.
Jitter Amplitude: Up to 16.5 UI_{p-p} (depending on data rate and jitter frequency).
(Jitter Generation available on Channel A1 only)

▶ Maximum Number of Output Channels

Number of Like Mainframes	DTG5078			DTG5274		
	DTGM10	DTGM20	DTGM30	DTGM10	DTGM20	DTGM30
1	32	32	16	8	8	8
2	64	64	32	16	16	16
3	96	96	48	—	—	—

Pulse & Data Features

Pulse Generator (PG) Features (Unique to PG Mode) –
Continuous or Burst.
Burst Count: 1 to 65,536.
Pulse Rate: Off, 1/1, 1/2, 1/4, 1/8, 1/16.

Data Patterns

Pattern Length per Channel (Pattern Memory) –
Minimum:
DTG5078: 1 bit (software mode) or 240 bits (hardware mode).
DTG5274: 1 bit (software mode) or 960 bits (hardware mode).
Maximum:
DTG5078: 8,000,000 bits.
DTG5274: 32,000,000 bits (in multiples of four).

Built-in Data Patterns – Binary Counter, Johnson Counter, Graycode Counter, Walking Ones, Walking Zeros, Checker Board, User Defined Patterns.

Pattern Import Capability –
Type/Tools:
Tektronix TLA Data Exchange Format File (*.txt).
Tektronix HFS Vector File (ASCII) (*.vca).
Tektronix HFS Vector File (binary) (*.vcb).
Medium/Pass:
Import data via GPIB, LAN, CD-ROM, floppy drive, USB memory devices.

Pattern Copy and Paste Capability – Copy and paste between data listing/waveform editor and spreadsheet software (e.g. Excel) via clipboard.

PRBS/PRWS Data Patterns –
(Note: memory supports PRBS/PRWS patterns, and user can create errored PRBS)
2^5–1, 2^6–1, 2^7–1, 2^8–1, 2^9–1, 2^{10}–1, 2^{11}–1, 2^{12}–1, 2^{13}–1, 2^{14}–1, 2^{15}–1, 2^{23}–1.

Sequencer Features

Sequence Length –
1 to 8,000 steps for main sequence.
1 to 256 steps for sub-sequence.

Max. Number of Blocks – 8,000.

Max. Number of Sub-sequences – 50.

Repeat Counter – 1 to 65,536 or infinite.

Channel Addition –
AND or XOR (slots A to D only).

Note: DTG5078 slots E, F, G, & H do not support the following: RZ, R1, pulse generation modes which includes controls for trail delay/duty cycle/pulse width, channel addition, and variable cross-points.

Auxiliary Channels

Clock Out

Connector – SMA, complementary output (common offset and ground).

Frequency Range –
DTG5078: 50 kHz to 750 MHz extendable to 800 MHz.
DTG5274: 50 kHz to 2.7 GHz extendable to 3.35 GHz.

Frequency Resolution –
8 digit setting resolution.
Minimum: 1 mHz (e.g. with 50,000.000 Hz setting).

Internal Clock Accuracy – Within ±1 ppm.

Jitter –
DTG5078: < 2 ps_{RMS} at 750 Mbps, at 0.8 V_{p-p} (typical).
DTG5274: < 2 ps_{RMS} at 2.7 Gbps, at 0.8 V_{p-p} (typical).

Amplitude/Resolution –
0.03 V_{p-p} to 1.25 V_{p-p}/10 mV (50 Ω).
0.06 V_{p-p} to 2.5 V_{p-p}/10 mV (1 MΩ).

Output Voltage Window –
–2.0 to 2.47 V (50 Ω).
–2.0 to 7.00 V (1 MΩ).

Max. Output Current – ±80 mA.

Transition Times (20% to 80%) –
DTG5078:
<85 ps (Amplitude = 0.1 V_{p-p}, Offset = 0 V) (typical).
<100 ps (Amplitude = 1.0 V_{p-p}, Offset = 0 V) (typical).
DTG5274:
<70 ps (Amplitude = 0.1 V_{p-p}, Offset = 0 V) (typical).
<80 ps (Amplitude = 1.0 V_{p-p}, Offset = 0 V) (typical).

Overshoot – <10%, at 1 V_{p-p} into (50 Ω) (typical).

Other Output Channels

Auxiliary DC Outputs – –3.0 to 5.0 V/10 mV, Max. Current: ±30 mA, 8 independently controlled outputs, Connector: 2x8 pin header on front panel.

Sync Out – CML (current mode logic), V_{OH}: 0 V, V_{OL}: –0.4 V (50 Ω) (typical), SMA Connector, SE, Front panel, Rise/Fall Time (20 to 80%): 140 ps, Delay to Data Out: –4.5 ns (typical).

10 MHz Reference Out – 1.2 V_{p-p} (50 Ω, AC coupled) (typical), 2.4 V_{p-p} (1 MΩ, AC coupled) (typical), BNC Connector, Rear Panel.

Input Channels

External Clock In –
Input Ranges:
DTG5078: 1 MHz to 800 MHz.
DTG5274: 1 MHz to 3.35 GHz.
0.4 V_{p-p} to 2 V_{p-p} (50 Ω, AC Coupled), 50% ±5% duty cycle, SMA Connector, Rear Panel.

10 MHz Reference In –
Input Ranges:
10 MHz ±0.1 MHz, 0.2 V_{p-p} to 3 V_{p-p} (50 Ω, AC coupled), BNC Connector, Rear Panel.

Phase Lock In –
Input Ranges:
1 MHz to 200 MHz, 0.2 V_{p-p} to 3 V_{p-p} (50 Ω, AC coupled), BNC Connector, Rear Panel.

Skew Cal In – Single-ended, ECL (into 50 Ω to –2 V), SMA Connector, Front Panel.

Trigger In –
Input Ranges:
–5 V to 5 V (50 Ω), 0.1 V resolution, –10 V to 10 V (1kΩ), Min. 0.5 V_{p-p} (50 Ω), 1.0 V_{p-p} (1kΩ), Min. 20 ns pulse width, Positive or Negative edge trigger, Delay timing: see manuals, BNC Connector, Front Panel.

Event In –
Input Ranges:
–5 V to 5 V (50 Ω), 0.1 V resolution, –10 V to 10 V (1 kΩ), 0.1 V resolution, Min. 0.5 V_{p-p} (50 Ω), 1.0 V_{p-p} (1 kΩ), Polarity: Normal or Invert, Delay timing: see manuals, BNC Connector, Front Panel.

▶ Environmental

	Operating	Nonoperating
Temperature	+10 ºC to +40 ºC	–20 ºC to +60 ºC
Humidity	20% to 80% relative humidity with a maximum wet bulb temperature of 29.4 ºC, non-condensing	(no diskette in floppy drive): 5% to 90% relative humidity with a maximum wet bulb temperature of 40 ºC, non-condensing
Altitude	3,000 m (10,000 ft.)	12,000 m (40,000 ft.)
Random Vibration	2.65 m/s^2_{RMS} (0.27G_{RMS}), from 5 Hz to 500 Hz, 10 minutes	22.36 m/s^2_{RMS} (2.28 G_{RMS}) total from 5 Hz to 500 Hz, 10 minutes each axis 3-axes 30 minutes total

Instrument Control/Data Transfer Ports

GPIB – GPIB for remote control and data transfer. (conforms to IEEE-Std 488.1, compatible with IEEE 488.2 and SCPI-1999.0).

LAN – LAN for PC interface and data transfer (conforms to IEEE 802.3).

Computer System & Peripherals

CompactPCI based PC, Celeron 566 MHz CPU, Windows 2000 Professional, 128 MB SDRAM, 20 GB Hard Drive, 1.44 MB floppy drive on front panel, CD-ROM in rear panel, included USB compact keyboard and mouse.

PC I/O Ports

USB 1.1 compliant ports (3 total, 1 front, 2 rear), PS/2 mouse and keyboard connectors (rear panel), RJ-45 Ethernet connector (rear panel) supports 10Base-T and 100Base-TX, VGA out (rear panel), RS-232C.

Physical Characteristics

Display Characteristics – LCD color display, 800 (H) x 600 (V) (SVGA).

Mainframe Dimensions	**mm**	**in.**
Height	266	10.5
Width	445	17.5
Length	462	19.7

Output Module Dimensions	**mm**	**in.**
Height	33	1.3
Width	84	3.3
Length	133	5.2

Weight (approx.)	**kg**	**lbs.**
DTG5078	17.5	38.6
DTG5274	17.0	37.5
DTGM10	0.25	0.55
DTGM20	0.26	0.57
DTGM30	0.27	0.60

▶ Output Module Characteristics

Basic Features	DTGM10	DTGM20	DTGM30
Output Channels & Connectors	4 single-ended (installed in DTG5078) 2 single-ended (installed in DTG5274) 4 SMA connectors	4 single-ended (installed in DTG5078) 2 single-ended (installed in DTG5274) 4 SMA connectors	2 complementary channels 4 SMA connectors
Normal/Complement (Invert)	Selectable		
Source Impedance	50 Ω		
Enable / Disable	Yes (software switch)		
Output Channel Timing			
Transition Times (20% to 80%) (50 Ω)	<540 ps (V_{0L} = 0.0, V_{0H} = 1.0) (typ) <1.5 ns (V_{0L} = –1.0, V_{0H} = 2.0) (typ)	<340 ps (V_{0L} = 0.0, V_{0H} = 1.0) (typ) <760 ps (V_{0L} = -1.0, V_{0H} = 2.0) (typ)	<95 ps (V_{0L} = 0.0, V_{0H} = 0.1) (typ) <110 ps (V_{0L} = 0.0, V_{0H} = 1.0) (typ)
Transition Time Control	Yes	Yes	No
Slew Rate Control Range	0.65 V/ns to 1.3 V/ns into 50 Ω	0.63 V/ns to 2.25 V/ns	—
Setting Resolution	0.01 V/ns	0.01 V/ns	—
Channel Output Levels			
Amplitude/Resolution	0.25 to 3.5 V_{p-p}/5 mV (into 50 Ω) 0.50 to 10.0 V_{p-p}/5 mV (into 1 MΩ)	0.1 to 3.5 V_{p-p}/5 mV (into 50 Ω) 0.2 to 7.0 V_{p-p}/5 mV (into 1 MΩ)	0.03 to 1.25 V_{p-p}/5 mV (into 50 Ω)*1 0.06 to 2.5 V_{p-p}/5 mV (into 1 MΩ)*1
Output Voltage Window	–1.5 V to 2.0 V (into 50 Ω) –3.0 V to 7.0 V (into 1 MΩ)	–1.0 V to 2.5 V (into 50 Ω) –2.0 V to 5.0 V (into 1 MΩ)	–2.0 V to 2.47 V (into 50 Ω) –2.0 V to 7.0 V (into 1 MΩ)
DC Accuracy	±50 mV into 50 Ω to GND (±3% of the set value)	±50 mV into 50 Ω to GND (±3% of the set value)	±50 mV into 50 Ω to GND (±3% of the set value)
Limit Setting	High and low level limits can be set		
Maximum Output Current	±40 mA	±80 mA	±80 mA
Overshoot	<16% (typ)	<15% (typ)	<10% (typ)
Supported Native Logic (Typical)	TTL, CMOS	TTL, CMOS, (P)ECL, LVPECL	LVDS, TMDS, (P)ECL, LVPECL, CML

*1 Depending on offset settings.

Mechanical Cooling – Required Clearance

Top and Bottom – 2 cm.

Side – 15 cm.

Rear – 7.5 cm.

Power Supply

Power Source – 100 to 240 VAC, 47 to 63 Hz.

Power Consumption – 560 W.

Safety –
UL 3111-1, CAN/CSA-22.2 No. 1010.1,
EN61010-1/A2 1995.

Electromagnetic Compatibility (EMC) –
Europe:
EN61326 Class A.
EN61000-3-2, EN61000-3-3.
Australia/New Zealand:
AS/NZS 2064.

▶ Ordering Information

Mainframes

DTG5078
750 Mbps, 8 slot mainframe.

DTG5274
2.7 Gbps, 4 slot mainframe.

Mainframes Include: Windows® 2000 professional operating system recovery disk, DTG5000 Series application software install disk, user manual (volumes I and II), programmers manual, technical reference, registration card, accessory pouch, front cover, compact USB keyboard, USB mouse, lead set for DC Output, 16-CON, twisted pair, 24 in. (60 cm), 50 Ω SMA terminator (male, DC to 18 GHz), SMA connector cap (10 ea. with DTG5078, 8 ea. with DTG5274), power cord, calibration certificate.

Please specify power cord and language option when ordering.

Mainframe Options
Opt. 1R – Rackmount.

International Power Plugs
Opt. A0 – North America power.

Opt. A1 – Universal EURO power.

Opt. A2 – United Kingdom power.

Opt. A3 – Australia power.

Opt. A5 – Switzerland power.

Opt. A6 – Japan power.

Opt. A10 – China power.

Opt. A99 – No power cord or AC adapter.

Language Options
Opt. L0 – English.

Opt. L5 – Japanese.

Output Modules

DTGM10
4 channels (DTG5078), 2 channels (DTG5274),

3.5 V_{p-p} (50 Ω), 10 V_{p-p} (1 MΩ).

Tr/Tf (20% to 80%): <540 ps (1 V_{p-p}, into 50 Ω), variable.

DTGM20
4 channels (DTG5078), 2 channels (DTG5274).

3.5 V_{p-p} (50 Ω), 7 V_{p-p} (1 MΩ).

Tr/Tf (80%) <340 ps (1 V_{p-p}, into 50 Ω), variable.

DTGM30
2 channels.

1.25 V_{p-p} (50 Ω), 2.5 V_{p-p} (1 MΩ).

Tr/Tf (20% to 80%) <110 ps (1 V_{p-p}, into 50 Ω), fixed.

Output Modules Include: Installation sheet (Japanese/English), SMA connector cap (set of 4 with DTGM10/20, set of 2 with DTGM30), 50 Ω SMA terminator (DC to 18 GHz) (set of 2 with DTGM30), registration card.

Service Options
Opt. C3 – Calibration Service 3 Years.

Opt. C5 – Calibration Service 5 Years.

Opt. TDAT – Calibration Data Report (Japanese).

Opt. D1 – Calibration Data Report (English).

Opt. D3 – Calibration Data Report 3 Years (with Option C3).

Opt. D5 – Calibration Data Report 5 Years (with Option C5).

Opt. R3 – Repair Service 3 Years.

Opt. R5 – Repair Service 5 Years.

Recommended Accessories
Service Manual (English) – Order 071-1285-XX.

Transition Time Converters – Output transition time (10% to 90%).

150 ps: Order 015-0710-00.

250 ps: Order 015-0711-00.

500 ps: Order 015-0712-00.

1000 ps: Order 015-0713-00.

2000 ps: Order 015-0714-00.

Test Adapters
HDMI TPA-R Test Adapter Set – HDMI TPA-R TDR (set of 2), HDMI TPA-R DI (differential), HDMI TPA-R SE (single-ended).

Order 013-A012-50.

HDMI TPA-P test adapter set– HDMI TPA-P TDR, HDMI TPA-P DI (differential), HDMI TPA-P SE (single-ended).

Order 013-A013-50.

DVI TPA-R Test Adapter Set – DVI TPA-R TDR (set of 2), DVI TPA-R DI (differential), DVI TPA-R SE (single-ended).

Order 013-A014-50.

▶ Cables

Type	Part Number
Lead set for DC Output, 16-CON, twisted pair, 24 in (60 cm)	012-A229-00
Pin header cable, 20 in. (51 cm)	012-1505-00
Pin header SMB cable, 20 in. (51 cm)	012-1503-00
GPIB Cable, double-shielded, 79 in (200 cm)	012-0991-00
Master/Slave Cable Set for connecting two Mainframes; set of 4 SMA cables, 51 cm, 50 Ω (174-1427-00), and set of 2 BNC cables, 46 cm (012-0076-00)	012-A230-00
Master/Slave Cable Set for connecting three Mainframes; set of 6 SMA cables, 51 cm, 50 Ω (174-1427-00) and set of 3 BNC cables, 46 cm (012-0076-00)	012-A231-00
BNC Cables 50 Ω	
18 in. (46 cm)	012-0076-00
24 in. (61 cm)	012-1342-00
42 in. (107 cm)	012-0057-01
With shield, 98 in. (250 cm)	012-1256-00
SMA Cables 50 Ω	
12 in (30 cm)	174-1364-00
20 in. (51 cm)	174-1427-00
39 in. (100 cm)	174-1341-00
60 in. (152 cm)	174-1428-00
Delay SMA Cables 50 Ω	
1 ns (male to female)	015-1019-00
2 ns	015-0560-00
2 ns (male to female)	015-1005-00
5 ns	015-0561-00
5 ns (male to female)	015-1006-00

▶ Adapters & Connectors

Type	Part Number
SMB – BNC adapter	015-0671-00
50 Ω SMA (male) – BNC (female) Adapter	015-0554-00
50 Ω SMA (female) – BNC (male) Adapter	015-0572-00
50 Ω N (male) – SMA (male) Adapter	015-0369-00
50 Ω SMA Adapter (male – female), DC to 18 GHz, VSWR: 1.2	015-0549-00
50 Ω SMA Adapter (slide on type female – male), DC to 18 GHz, VSWR: 1.05 + 0.002F (GHz)	015-0553-00
50 Ω SMA T-Connector (male – female/female)	015-1016-00
50 Ω SMA Divider (male/male/male), 6 dB, DC to 18 GHz, VSWR: 1.9	015-1014-00
50 Ω BNC DC Block, 500 kHz to 2 GHz	015-0221-00

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Our most up-to-date product information is available at:
www.tektronix.com

Product(s) are manufactured in ISO registered facilities.

Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.

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