ML2010 MINI LAB

OPERATIONS MANUAL

Knight Electronics
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Dallas, TX 75243

Rev. B

REVISION HISTORY

REVISION	RELEASE DATE	COMMENT
-	02-18-11	GENESIS
A	03-21-11	RELEASE TO PRINT
A1	08-06-11	FIGURES (2ND 13 FORWARD) RENUMBERED & REFERENCE CORRECTIONS
B	09-01-11	RELEASE TO PRINT

CONGRATULATIONS

You have just acquired one of the most complete and cost effective pieces of prototype testing equipment available in the market today.

The ML2010 is a complete prototyping station and has been designed to consolidate all of your test equipment needs into one compact package.

This miniature laboratory used in conjunction with an oscilloscope and multimeter puts everything you need at your fingertips for building and testing all types of digital and analog circuits.

The features incorporated in this equipment were selected as a result of an extensive survey of electronic instructors, designers, and technicians wants and needs.

We hope you will enjoy using your new ML2010 and encourage you to contact us with any inputs, changes, or new features you would like to see in the next generation Mini-Lab.

For your convenience PDF full size (11x17) copies of the ML2010 Schematics, as well as this manual, are available for downloading on the Knight Educational Products website at http://www.knightedu.com.

TABLE OF CONTENTS

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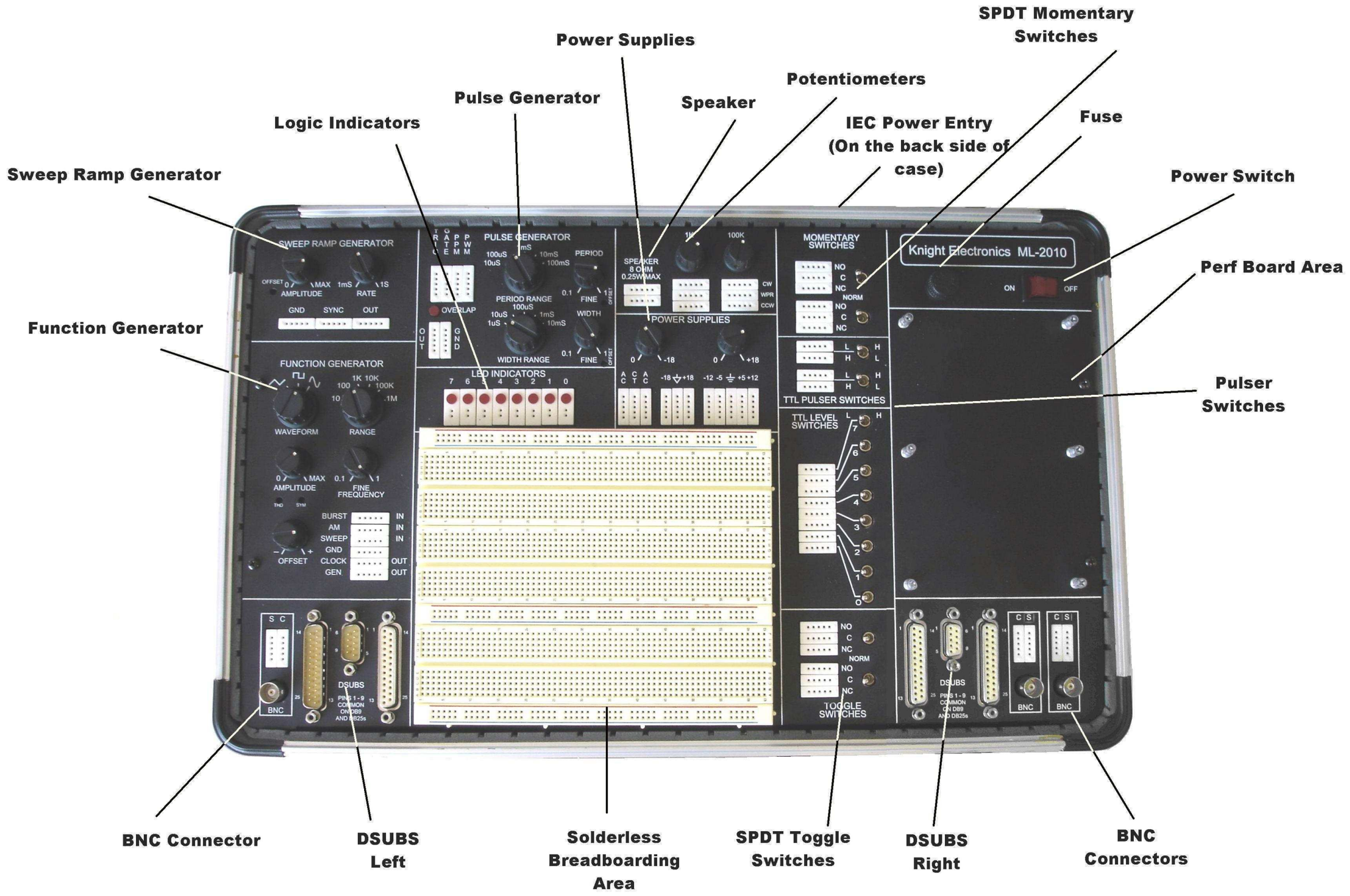


Figure 1.
ML2010 FEATURES

SPECIFICATIONS

POWER INPUT:

120 VOLT AC 50/60 HZ
FUSED (2A 250V, 5x20mm GLASS, FAST ACTING)
LIGHTED POWER ON INDICATOR

DC POWER SOURCES:

+5 VOLTS ±3% @ 1 AMP
-5 VOLTS ±3% @ 1 AMP

+12 VOLTS ±3% @ 1 AMP
-12 VOLTS ±3% @ 1 AMP

0 TO >+18 VOLTS VARIABLE @ 1 AMP
0 TO >-18 VOLTS VARIABLE @ 1 AMP
(ISOLATED GROUND FOR VARIABLE SUPPLIES)

0.1% LINE REGULATION
0.1% LOAD REGULATION

SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTED

AC POWER SOURCE:

15 VOLTS CENTER TAPPED @ 500 MILLIAMPS

PULSE GENERATOR:

CONTINOUSLY VARIABLE IN FIVE DECADE RANGES:
PULSE WIDTH: ≤ 100nSEC TO ≥10mSEC
PULSE REPETITION: ≤ 1uSEC TO ≥ 100mSEC

OVERLAP INDICATOR

CAPABLE OF 100% DUTY CYCLE

PULSE POSITION AND WIDTH MODULATION INPUTS

TTL COMPATIBLE GATE AND TRIGGER INPUTS

RISE AND FALL TIMES LESS THAN 10nSEC

SWEEP RAMP GENERATOR:

ADJUSTABLE PERIOD: ≤ 1mSEC TO ≥ 1SEC

ADJUSTABLE 0 TO 3.7 VOLT OUTPUT AMPLITUDE

NEGATIVE LINEAR RAMP OUTPUT FOR LINEAR SWEEP

SEPARATE TTL/HC COMPATIBLE SYNC OUTPUT

FUNCTION GENERATOR: SINE, SQUARE, OR TRIANGLE WAVE OUTPUT

0 TO 18 VPP OUTPUT AMPLITUDE
~500 OHM OUTPUT IMPEDANCE
SHORT CIRCUIT PROTECTED

DC OFFSET ADJUSTABLE FROM 0 TO ±10 VOLTS

SEPARATE TTL/HC COMPATIBLE CLOCK OUTPUT
(20mA OUTPUT AT 0.33VDC (LOW) OR 4.3VDC (HIGH)
RISE/FALL TIME LESS THAN 20nSEC

CONTINUOUSLY VARIABLE FREQUENCY FROM 1HZ TO 1MHZ
IN SIX DECADE RANGES
(NOTE: DUE TO LIMITATIONS OF THE FUNCTION GENERATOR CHIP, WAVEFORM VARIATIONS, OR ROLL OFF, MAY BE EXPERIENCED AT THE MAXIMUM RANGE.)

DISTORTION: SINE WAVE ≤ 2% TO ≥ 100KHZ
TRIANGLE WAVE ≤ 2% TO ≥ 100KHZ

RISE & FALL: SQUARE WAVE ≤ 20nSEC

FREQUENCY MODULATION INPUT
AMPLITUDE MODULATION INPUT
BURST INPUT
SWEEP INPUT CAPABLE OF 1000:1 SWEEP
(START FREQUENCY DETERMINED BY SWEEP RAMP AMPLITUDE
STOP FREQUENCY DETERMINED BY GENERATOR FREQUENCY SETTING)

SPEAKER: 2-1/4" 8Ω 0.25W

POTENTIOMETERS: UNDEDICATED 1KΩ AND 100KΩ 20%
LINEAR TAPER
0.125W POWER RATING

INDICATORS: EIGHT BUFFERED LED (TTL/HC COMPATABLE)

SWITCHES: EIGHT TTL/HC LEVEL (0V OR +5V) UNBUFFERED TOGGLE SWITCHES
TWO UNDEDICATED SPDT TOGGLE SWITCHES [ON – NONE – ON]
TWO UNDEDICATED SPDT MOMEMTARY [ON – NONE – (ON)]

PULSERS: TWO TTL/HC COMPATIBLE DEBOUNCED PULSERS WITH
COMPLEMENTARY OUTPUTS

INTERFACE:

DB25 MALE – DB9 MALE – DB25 FEMALE
DB25 FEMALE – DB9 FEMALE – DB25 FEMALE
(DB25 TO DB25 PINNED 1 TO 1 WITH DB9 COMMON TO FIRST 9)

THREE BNC TO TIE-POINT BLOCK

PROTOTYPING AREA:

Solderless Breadboarding Area – 3 Terminal Strips (1890 points), 3 Distribution Strips (300 points)

5.4" x 3.6" Perf Board Area with 6 mounting post – Area for dedicated "BLOB" board as well as custom circuit and test modules
(ADDITIONAL FA0005 PERF BOARDS, CUSTOM, AND TEST MODULES AVAILABLE SEPERATELY)

ML 2010 FEATURE DESCRIPTION & CONTROLS

This section will familiarize you with the various controls and their functions. Before starting to use your Mini-Lab, you should read this section carefully and know the location of all the controls and their function.

1. AC AND DC POWER

A. AC Plug: For connection of AC power cord to 120VAC 50/60 Hz power line.
B. Fuse Holder: Houses fuse for protection of your unit. Replace with proper size fuse only (2A 5x20mm).
C. Power Switch: Applies power to the unit. On when lit.
D. Voltage Control: For varying -18VDC tie point output from 0 to -18VDC.
E. Voltage Control: For varying +18VDC tie point output from 0 to +18VDC. (Note: The ground for the ±18VDC supplies is isolated. This permits a ≥36VDC output.)
F. DC Fixed Voltages: For obtaining ±5VDC and ±12VDC.
G. AC Output: Provides access to an isolated 500mA 15VAC center tapped transformer winding.

2. FUNCTION GENERATOR (FG)

The FG section provides sine, square or triangle waveform signals with variable frequency, amplitude and offset. The clock output is TTL/HC compatible and operates at the same frequency as the FG output. It may be used as a general purpose clock or for synchronization to the FG output.

A. Output: ~500Ω impedance, short circuit protected.
B. Waveform: Allows selection of a triangle, sine or square wave at the output.
C. Frequency: Continuously variable from 1Hz to 1MHz in six decade ranges.
   (NOTE: DUE TO LIMITATIONS OF THE FUNCTION GENERATOR CHIP, WAVEFORM VARIATIONS, OR ROLL OFF, MAY BE EXPERIENCED AT THE MAXIMUM RANGE.)
D. Amplitude: Controls the amplitude of the output from to 18 Volts peak to peak (18VPP).
E. Offset: Adds a -10VDC to +10VDC offset to the output signal.
F. Amplitude Modulation (AM) input: Used to vary the amplitude of the FG output relative to the voltage being applied. An AC signal of ~5VPP achieves 100% modulation.
G. Burst Input: Acts as an ON/OFF gate. 0V for off +4V for on.
H. Clock Output: A TTL/HC compatible output with a rise and fall time of 20nSEC maximum. Can sink or source 20mA at 0.33VDC maximum (low) to 4.3VDC minimum (high).
I. Sweep Input: This input is used to frequency modulate (FM) the FG signal. A wide range of frequencies may be linearly swept by applying the signal from the

SG. The start (low) frequency is determined by the gain of the ramp generator. The stop (high) frequency will be the current frequency generator setting.

In conjunction with an oscilloscope, this function may be used to simulate a basic spectrum analyzer in linear mode. Frequency response of other components or circuitry may be observed by applying the swept frequency to the input of the device under test (DUT), attaching the output of the device to a scope, and triggering the scope from the sweep ramp sync output.

Frequency deviation is an inverse linear function of the voltage applied at this input from +3.1VDC, (minimum frequency), to -3.1VDC, (maximum frequency). Applying 0VDC to the sweep input will have no effect on the set frequency. The frequency deviation for a given voltage level may be more precisely determined by applying this voltage to the input and measuring the frequency at the output of the FG.

Other FM applications include radio, television, laser communications and sonar signals. By applying a square wave to this input a frequency shift keying (FSK) signal may be generated which can be used for low speed data communications.

Frequency modulation is a conversion of voltage to frequency, so this portion of the circuitry may also be used to study and experiment with voltage to frequency (V/F) and frequency to voltage (F/V) conversion concepts. V/F and F/V converters are basic electronic I building blocks used in phase locked loops, test equipment, and numerous other applications.

3. SWEEP RAMP GENERATOR (SG)

The SG produces a linear, negative going ramp. This may be used to modulate the pulse or function generator signals, but is designed primarily to frequency sweep the function generator.

A. Amplitude: Varies the amplitude of the ramp from 0V to ~3.7V.
B. Rate: Varies the repetition rate of the ramp from less than 1mSEC to greater than 1SEC.
C. Sync output: Produces a negative pulse of about ~50uSEC wide during the low to high transition of the ramp. It is typically used to trigger an oscilloscope and/or trigger input of the pulse generator for synchronization.

4. PULSE GENERATOR (PG)

This section produces a train of TTL/HC compatible pulses with independently adjustable width and spacing. The maximum duty cycle which is dependent on width and period settings is 100%.

The pulse train may be modulated and observed on an oscilloscope by applying a signal from the SG or FG, (or from an external source), and triggering the scope with the sync or clock pulse, (respectively). Any combination of modulation, gating, or triggering may be selected.

A. Output: The PG output has a rise and fall time of less than 10nSEC and 12mA sink and source capability.
B. Pulse width: The width of the pulses in the pulse train is continuously variable from less than 100nSEC to 10mSEC in five decade ranges.
C. Pulse period: The pulse repetition rate is continuously variable from 1uSEC to 100mSEC in five decade ranges.
D. Overlap indicator: LED is lit when pulse width exceeds pulse period due to incorrect setting or over modulation.
E. Trigger input: Allows the PG to be synchronized to an external signal. A TTL low to high transition on this input triggers the start of the next pulse from the generator.
F. Gate input: This input allows a burst of pulses to be generated when a TTL pulse or square wave is connected. When the applied signal is low, the pulse output is blanked or forced low (off) until this input is disconnected or goes high.

WARNING! TRIGGER AND GATE ARE LV FAMILY TTL DIGITAL INPUTS. DO NOT EXCEED VOLTAGE LEVELS OF GROUND (MIN) OR + 5.5 VOLTS (MAX).

G. Pulse Width Modulation (PWM) input: PWM is a method of converting an analog signal to a digital form by varying the width of the pulses in proportion to the voltage of the modulating signal. Maximum modulation requires an AC signal of ~2VPP. Applications include switching power supply control circuitry, motor speed control, temperature control, communications and radar.
H. Pulse Position Modulation (PPM) input: PPM is a method of converting an analog signal to a digital form by varying the position of the pulses in response to variations in voltage. Maximum modulation requires an AC signal of ~2VPP. Applications include radar, sonar, time domain reflectometry (TDR), communications and tachometers.

5. DIGITAL FUNCTIONS

A. Level Switches: Provides eight unbuffered digital logic outputs (0V for low or +5V for high).
B. Pulser Switches: Two momentary switches provide debounced pulses with TTL/HC complementary outputs.
C. Logic Indicators: Eight buffered inputs for indicating TTL or MOS logic high (on) or logic low (off) levels.

6. INTERFACE

A. DSUBS – Left: Male DB25 (DB25M) connects to the adjacent female DB25 (DB25F) and is connected 1 to 1 for interfacing with the breadboards. This DB25 pair may also be used to change the gender of the mating connector. The male female DB9 (DB9F) between the DB25M and DB25F is connected 1 to 1 on both the DB25M and DB25F first nine pins.
B. DSUBS – Right: DB25F connects to the adjacent DB25F for interfacing to the breadboards. The female DB9 (DB9F) between the two DB25Fs is connected 1 to 1 on both the DB25Fs first nine pins.
C. BNC connector: Three BNC connectors are provided to simplify interfacing to other test equipment.
D. Potentiometers: A 1KΩ and a 100KΩ uncommitted are provided for prototyping. The wiper terminal (middle tie-point block) should be current limited by a series resistor to protect the potentiometer.
E. SPDT toggle switches: Two uncommitted toggle switches [on-none-on] for prototyping. The NORM legend on the cover plate indicates the reference position of the bat handle when using the terms normally open (NO), normally closed (NC), and common (C).
F. SPDT momentary switches: Two uncommitted toggle switches [on-none-(on)] for prototyping. The NORM legend on the cover plate indicates the reference position of the bat handle when using the terms normally open (NO), normally closed (NC), and common (C).
G. Speaker: 8Ω, 0.25 watt.
H. Breadboarding area: 5-1/2" x 6-1/2" provided for prototyping.

ML2010 OPERATIONAL VERIFICATION

This section of the manual provides a step by step method of verifying the operation of each section of your ML2010. It is very strongly recommended that you take the time to perform each of the following procedures upon receiving you ML2010. Doing so will help you become proficient in the operation of the various functions of the ML2010 and verify that your ML2010 is fully operational.

OPERATIONAL VERIFICATION REQUIRED EQUIPMENT

24AWG Solid Wire	As Required - Used to connect test leads to tie point blocks
DMM	Knight K-225 Digital Multifunction Meter or Equivalent
DMM Test Leads	Mini-grabber to banana test leads or Equivalent
Oscilloscope	Rigol DS1102E 2-CH 100MHz/1Gs or Equivalent
Oscilloscope Probes	2 100MHz Oscilloscope Probes

1A. DMM AC AND DC POWER SUPPLY CHECKOUT

1. Insert the AC power cord female (IEC C13) end into the male AC socket (IEC C14) located on the back of the case. Connect the NEMA5-15 end of the power cord to a 120VAC 60Hz outlet.

2. Turn on the red power switch located on the cover plate. The switch indicator should light. Verify that the unit's fan is operational and exhausting air from the rear of the case.

3. Rotate the DMM function/range switch to the 20V function/range and the AC/DC select switch to the DC position. Connect the banana jack end of the red (positive) test lead to the V/Ω/Hz jack. Connect the banana jack end of the black (negative) lead to the COM jack.

4. Connect a length of 24AWG solid wire to the mini-grabber end of the red test lead.

5. Connect a length of 24AWG solid wire to the mini-grabber end of the black test lead.

6. Connect the DMM black test probe 24AWG wire to the fixed power supply GND tie point block.

7. Connect the DMM red test probe 24AWG wire to the +5VDC tie point block. A reading of +5VDC ±3% (+4.85 to +5.15VDC) should be seen on the meter display.

8. Set the DMM AC/DC switch to the AC position. Note the RMS AC ripple voltage. Depending on your DMM, typically, in the unloaded condition, the RMS AC ripple voltage of the supply should read ≤2mV. The actual AC Ripple voltage waveform is

best examined with an oscilloscope. Doing so will allow you to determine the frequency and cyclic nature of the waveform.

9. By moving the red test lead wire to the -5VDC, +12VDC and -12VDC tie point blocks, and switching between AC and DC mode, observe each supply. The readings on your DMM should be:

-5VDC ±3% (-4.85 to -5.15VDC)	AC Ripple (≤2.0mV)
+12VDC ±3%(+11.64 to +12.36VDC)	AC Ripple (≤5.0mV)
-12VDC ±3% (-11.64 to -12.36VDC)	AC Ripple (≤2.0-mV)

10. Rotate the DMM function/range switch to the 200V function/range and set the AC/DC select switch to the DC position.

11. Move the DMM black test lead wire to the variable power supply GND tie point block.

12. Connect the DMM red lead wire to the +18VDC tie point block. Rotate the 0 to +18VDC knob fully clockwise. A reading of ≥+18VDC (typical is +21.4VDC) should be observed on the DMM.

13. Set the DMM AC/DC switch to the AC position. Note the RMS AC ripple voltage. The RMS AC ripple voltage of the supply should read ≤5mV$_{RMS}$.

14. Set the DMM AC/DC switch to the DC position. Rotating the 0 to +18VDC knob fully counterclockwise should yield a DMM reading of 0VDC ±0.2VDC (typical is 0.1VDC).

15. Move the red test lead wire to the -18VDC tie point block. Rotate the 0 to -18VDC knob fully clockwise. A reading of ≤-18VDC (typical is -21.2VDC) should be observed on the DMM.

16. Set the DMM AC/DC switch to the AC position. Note the RMS AC ripple voltage. The RMS AC ripple voltage of the supply should read ≤5mV$_{RMS}$.

17. Set the DMM AC/DC switch to the DC position. Rotating the 0 to -18VDC knob fully counterclockwise should yield a DMM reading of 0VDC ±0.2VDC (typical is -0.1VDC).

18. Move the red test lead wire to the +18V tie point block and connect the black test lead wire to the -18V tie point block. With both the +18V and -18V controls fully clockwise a reading of ≥36VDC should be observed (typical is ~42.4VDC).

19. Remove the DMM leads from the ±18V supply tie point blocks.

20. Rotate the DMM function/range switch to the 20V function/range and the AC/DC select switch to AC position.

21. Connect the DMM red lead wire to the left AC tie point block and connect the DMM black lead wire to the right AC tie block. A reading of 16.5 to 18.15VAC should be

observed (typical is ~17.34VAC). Note: The AC winding of the power transformer is rated at 15VAC ±10% center tapped at a load current of 500mA. When measuring the unloaded value of the winding your reading will be higher than the loaded value. Unless your readings are extremely low or extremely high they should not be considered abnormal.

22. Disconnect the DMM black lead from the right AC tie point block and connect it to the AC CT tie point block. You should observe that the DMM reads approximately half of the reading observed in step 21 (approximately 8.25 to 9.08VAC with typical being ~8.67VAC).

23. Move the DMM red lead from the left AC tie point block to the right AC tie point block. You should observe the same reading as you did in step 22 (approximately 8.25 to 9.08VAC with typical being ~8.67VAC).

24. Remove the DMM leads from the tie point blocks and rotate the DMM function/range switch to the off position.

1B. OSCILLOSCOPE AC AND DC POWER SUPPLY TYPICAL AC WAVEFORMS

The waveforms shown were captured with a Rigol DS1102E 2-CH 100MHz/1Gs with 100MHz probes. These waveforms are to be considered typical unloaded waveforms. Your waveforms may vary due to manufacturing tolerances and measuring equipment specifications. These waveforms are not intended to be used for PASS/FAIL characterization of the ML2010.

1. Set the oscilloscope to the following settings:

a. Horizontal Time Base	500µSEC/DIV
b. CH1 Vertical Gain/Coupling	50mV/DIV - AC Coupled
c. CH1 Base Line	-3V (3 major divisions below center screen)
d. CH2 Vertical Gain/Coupling	OFF
e. CH2 Base Line	Not Applicable
f. Trigger	CH1 - AC Coupled - Rising Edge - Auto Mode
g. Trigger Level	-32mV (Referenced to CH1)

2. In turn connect the CH1 probe to each of the power supply outputs and examine the ripple voltage. The waveforms of Figures 2 through 7 show the typical ripple voltage when the delayed sweep function is enabled and horizontal time base adjusted to 50µSEC (x10).

POWER SUPPLY RIPPLE - TYPCIAL WAVEFORMS

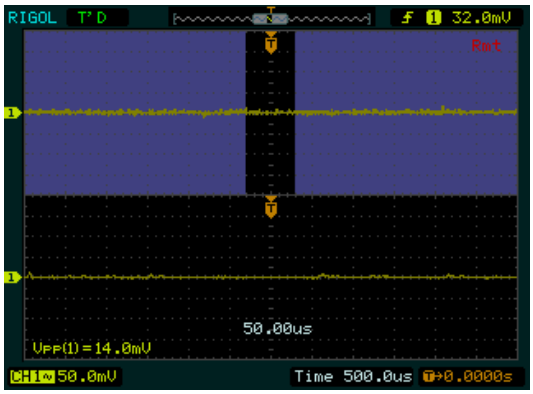


Figure 2. +5V Supply Ripple

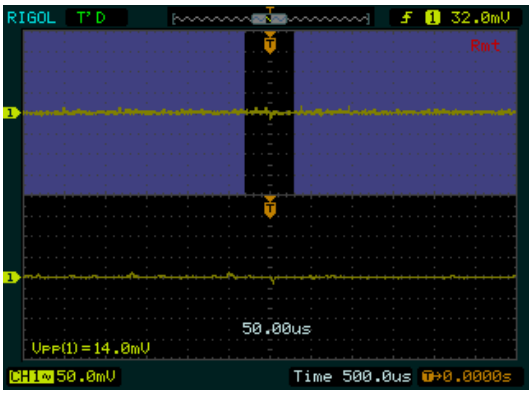


Figure 3. -5V Supply Ripple

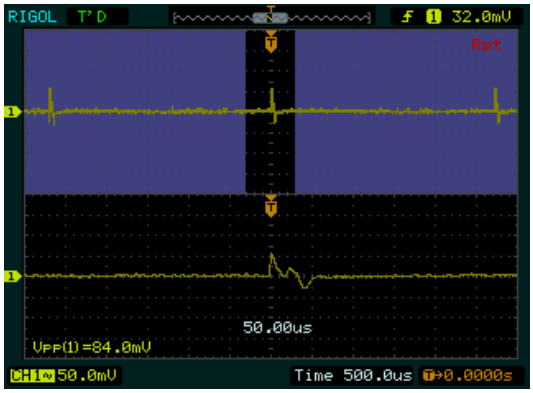


Figure 4. +12V Supply Ripple

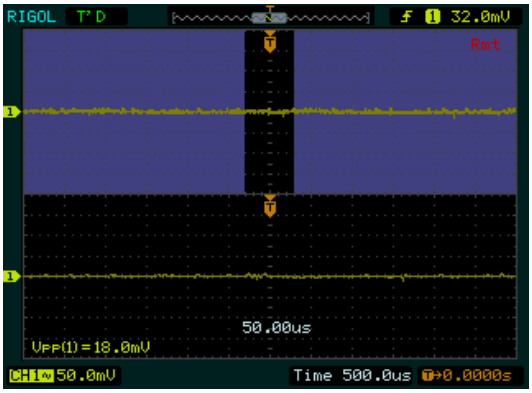


Figure 5. -12V Supply Ripple

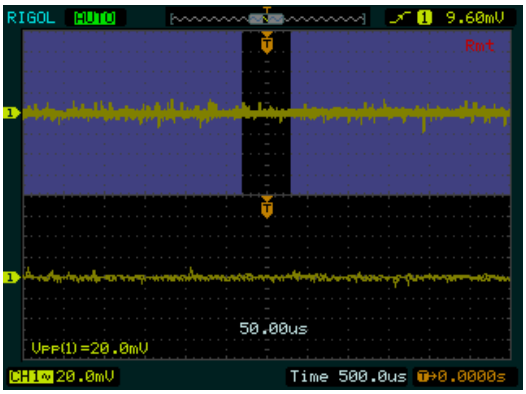


Figure 6. +Adjustable Supply Ripple
(MEASURED AT +18VDC)

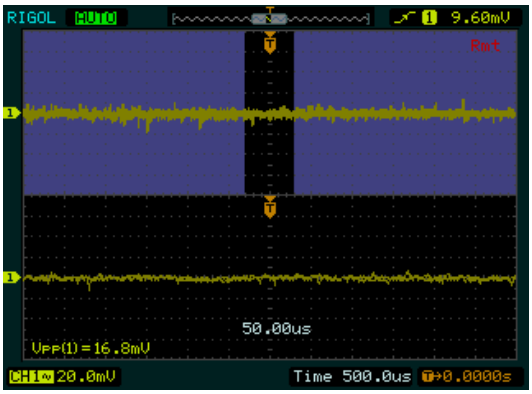


Figure 7. -Adjustable Supply Ripple
(MEASURED AT -18VDC)

2. SWEEP RAMP GENERATOR (SG) CHECKOUT

This procedure is written as a standalone procedure and assumes the Power Supplies of the ML2010 have been tested and deemed to be in proper working order. It is also assumed that the ML2010 is powered on and no connections to other test equipment exist.

1. Set the oscilloscope to the following settings:

a. Horizontal Time Base	200µSEC/DIV
b. CH1 Vertical Gain/Coupling	1V/DIV - DC Coupled
c. CH1 Base Line	-3V (3 major divisions below center screen)
d. CH2 Vertical Gain/Coupling	5V/DIV – DC Coupled
e. CH2 Base Line	+10V (2 major divisions above center screen)
f. Trigger	CH2 - DC Coupled - Rising Edge - Auto Mode
g. Trigger Level	+2V (Referenced to CH2)

2. Connect the probe grounds to the GND tie point block of the SG using 24AWG solid wires.

3. Connect the CH1 probe using 24AWG solid wire to the SG OUT tie point block.

4. Connect the CH2 probe using 24AWG solid wire to the SG SYNC tie point block.

5. Rotate the AMPLITUDE knob to the MAX position (fully clockwise) and rotate the RATE knob to the 1mSEC position (fully counterclockwise).

6. The SG output, a negative ramp waveform signal of ≥3.7VPP, should be observed on CH1 of the oscilloscope. The SG SYNC output, being a negative going ≥50µSEC pulse, should be observed on CH2 of the oscilloscope. Refer to Figure 8.

7. Vary the AMPLITUDE control from 0 to MAX and observe the variation in amplitude of the output. Note that the SYNC pulse (CH2 waveform) is fixed in amplitude and may be used to synchronize other circuits and/or equipment, in this case the oscilloscope, to the start of the negative going ramp.

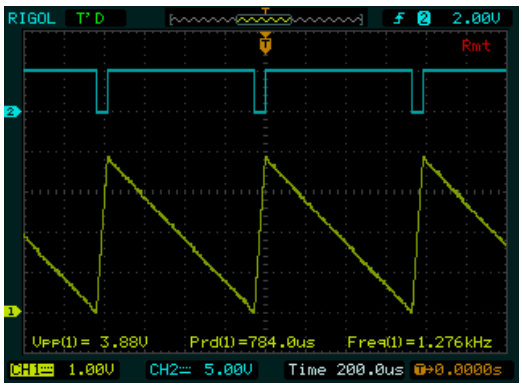


Figure 8. Sweep Generator
(Maximum Amplitude - Minimum Rate)

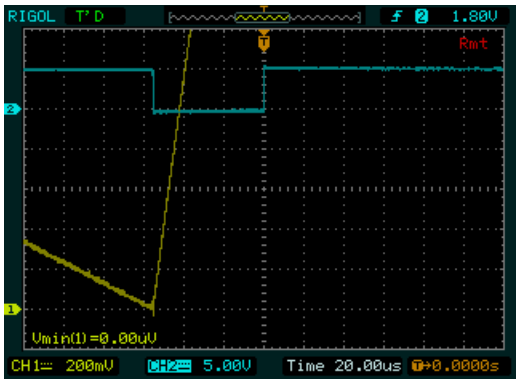


Figure 9. Sweep Generator
(Offset Verification and Adjustment)

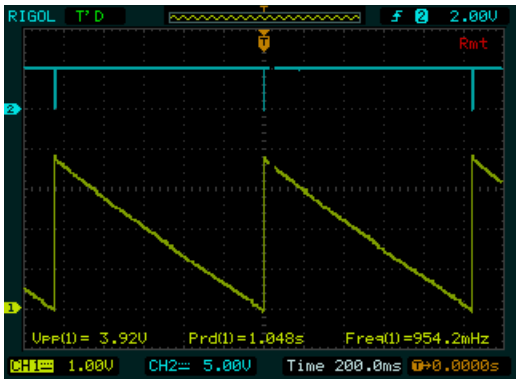


Figure 10. Sweep Generator
(Maximum Amplitude – Maximum RATE)

8. Return the AMPLITUDE to MAX and verify the RATE control is still set to 1mSEC.

9. Set the oscilloscope's CH1 vertical gain to 200mV/DIV and the horizontal time base to 20µSEC/DIV.

10. Verify the negative peak of the ramp is adjusted to 0VDC as shown in Figure 9. If the negative peak of the ramp is not at 0VDC the offset can be adjusted by using a small flat blade screwdriver. The offset potentiometer (R5 on the FA0012 Sweep Generator PCB) can be accessed through the hole labeled OFFSET located at the lower left of the SG AMPLITUDE control.

11. Return the oscilloscope controls to the original settings (CH1 Gain 1V/DIV and horizontal time base to 200µSEC/DIV). Verify that the ramp time is ≤1mSEC (≥1KHz) when in the 1mSEC position (as shown in Figure 8).

12. Vary the RATE control from 1mSEC (1KHz) to 1SEC (1Hz) position and observe the waveforms. Also verify that the ramp time is ≥1SEC (≤1Hz) when the RATE control is in the 1SEC position (as shown in Figure 10). It will be necessary to adjust the horizontal time base in order to see the entire waveform as the RATE control is adjusted.

13. Remove all connections and probes.

3. FUNCTION GENERATOR (FG) CHECKOUT

This procedure is written as a standalone procedure and assumes the Power Supplies and SG of the ML2010 have been tested and deemed to be in proper working order. It is also assumed that the ML2010 is powered on and no connections to other test equipment exist.

1. Set the oscilloscope to the following settings:

a. Horizontal Time Base	20µSEC/DIV
b. CH1 Vertical Gain	5V/DIV - DC Coupled
c. CH1 Base Line	0V (center screen)
d. CH2 Vertical Gain	5V/DIV – DC Coupled
e. CH2 Base Line	+10V (2 major divisions up from center screen)
f. Trigger	CH2 - DC Coupled - Rising Edge - Auto Mode
g. Trigger Level	+2V (Referenced to CH2)

2. Connect the probe grounds to the GND tie point block of the FG using 24AWG solid wires.

3. Connect the CH1 probe using 24AWG solid wire to the FG GEN OUT tie point block.

4. Connect the CH2 probe using 24AWG solid wire to the FG CLOCK OUT tie point block.

5. Set the FG controls to the following setting:

a. Waveform	Triangle
b. Frequency Range	10KHz
c. Amplitude	MAX (Fully Clockwise)
d. Fine Frequency	x1 (Fully Clockwise)
e. Offset	Mid-Range (12 o'clock position)

6. The typical waveform you should observe on the oscilloscope is shown in Figure 11.

7. Verify the peak to peak voltage of the triangle wave (CH1) is ~20Vpp and the peak to peak voltage of the square wave (CH2) is ~5Vpp as shown in Figure 11. Note: The triangle waveform (CH1) should be clipped at this point.

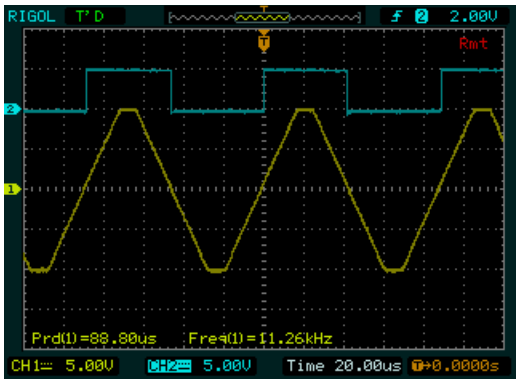


Figure 11. Function Generator
~10KHz Triangle - MAX Amplitude

8. Rotate the AMPLITUDE control fully counterclockwise. Verify that when the OFFSET control is in the fully counterclockwise position the FG output is between -9.5VDC and -10.5VDC.

9. Rotate the OFFSET control fully clockwise and verify the generator output is between +9.5VDC and +10.5VDC. Return the generator output to 0VDC by adjusting the OFFSET control to its mid-range position.

10. Set CH1 vertical gain to 100mV/DIV and if necessary re-adjust the OFFSET so the generator output is at 0VDC. Return the CH1 vertical gain to 5V/DIV.

11. Adjust the AMPLITUDE control to obtain a $12V_{PP}$ triangle waveform as shown in Figure 12.

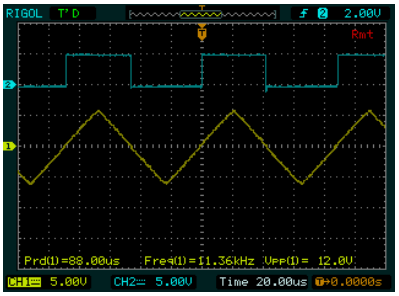


Figure 12. Function Generator
$12V_{PP}$ Triangle – 0VDC Offset

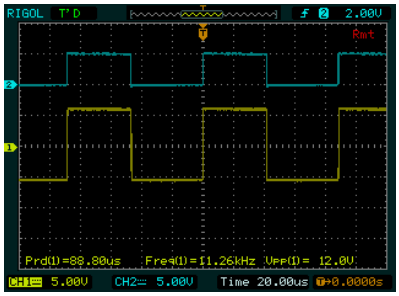


Figure 13. Function Generator
~$12V_{PP}$ Square – 0VDC Offset

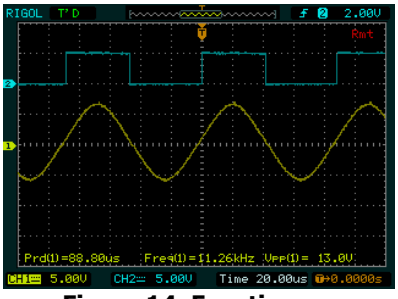


Figure 14. Function Generator
~$13V_{PP}$ Sine – 0VDC Offset

12. Set the WAVEFORM selection to the square wave function and verify that the CH1 waveform is a ~$12V_{PP}$ square wave as shown in Figure 13. Note: You may find the amplitude of the square wave to be slightly higher or lower than that of the triangle wave amplitude. A difference of several tenths of a volt is considered normal and can be attributed to the various tolerances of the function generator components.

13. Set the WAVEFORM selection to the sine wave function and verify that the CH1 waveform is a ~13V_{PP} sine wave as shown in Figure 14. Note: You will find the amplitude of the sine wave to be slightly higher than that of the triangle or square wave amplitude. A difference of approximately 1V is not uncommon and should be considered acceptable. This difference is somewhat inherent in the XR2206 Function Generator IC, circuit design, and component tolerances used in the ML2010 Function Generator circuitry.

14. The ML2010 FG is adjusted for symmetry and minimum distortion at the factory. However, should you find the need to re-adjust the symmetry and distortion without the use of a distortion meter use the following procedure. To adjust for minimum distortion, connect the scope probe the GEN OUT and set the WAVEFORM for the sine wave function. Adjust the AMPLITUDE control to obtain a non-clipping maximum swing sine wave. Then adjust R9 (Symmetry) and R11 (Distortion) on the FA0014 PCB which are accessible through the front panel via the SYM and THD holes located below the AMPLITUDE control. Adjust the THD and SYM controls alternately for minimum distortion and best symmetry by observing the sinusoidal waveform. If a distortion meter is available, you may use it as a final check on the setting of sine-shaping trimmers. The minimum distortion obtained in this manner is typically less than 1% from 1Hz to 10KHz and less than 3% over the entire frequency range.

15. Adjust the Oscilloscope to the following settings:

a. Horizontal Time Base	200mSEC/DIV
b. CH1 Vertical Gain	5V/DIV - DC Coupled
c. CH1 Base Line	+5V (1 major division up from center screen)
d. CH2 Vertical Gain	5V/DIV – DC Coupled
e. CH2 Base Line	-15V (1 major division up from bottom screen)
f. Trigger	CH2 - DC Coupled - Rising Edge - Single Mode
g. Trigger Level	2V (Referenced to CH2)

16. Set the Frequency RANGE to the 10Hz range and the FINE FREQUENCY to the x0.1 position. Trigger a single sweep of the oscilloscope and verify the Sine wave (CH1) and clock output (CH2) frequencies are ≤1Hz (≥1SEC) and are non-distorted as shown in Figure 15.

17. Select the Square wave. Trigger a single sweep of the oscilloscope and verify the Square wave (CH1) and Clock output (CH2) frequencies are ≤1Hz (≥1SEC) and are non-distorted as shown in Figure 16.

18. Select the Triangle wave. Trigger a single sweep of the oscilloscope and verify the Triangle wave (CH1) and Clock output (CH2) frequencies are ≤1Hz (≥1SEC) and are non-distorted as shown in Figure 17.

SCOPE: 200mS Single Sweep, FREQ SETTING: 10Hz x 0.1, LIMIT: ≤1Hz (≥1SEC)

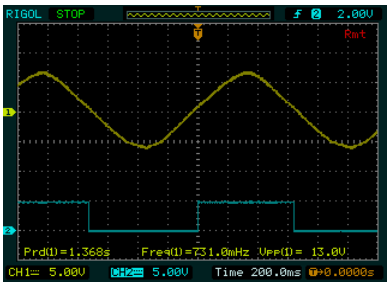


Figure 15. ≤1Hz Sine

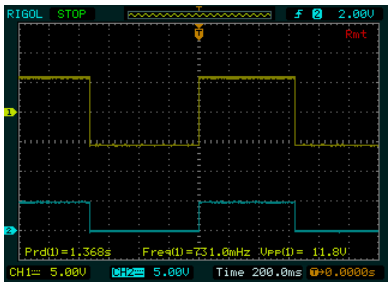


Figure 16. ≤1Hz Square

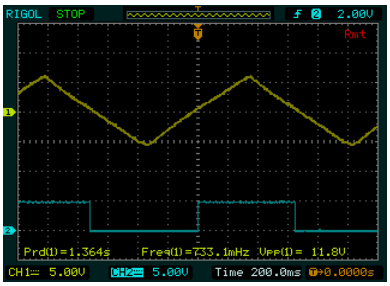


Figure 17. ≤1Hz Triangle

19. Set the oscilloscope trigger mode to auto trigger, time base to 20mSEC/DIV, and rotate the FINE FREQUENCY to the x1 position. Verify each of the waveforms and frequencies as shown in Figures 18, 19, and 20.

SCOPE: 20mS Auto Trigger, FREQ SETTING: 10Hz x 1, LIMIT: ≥10Hz (≤100mSEC)

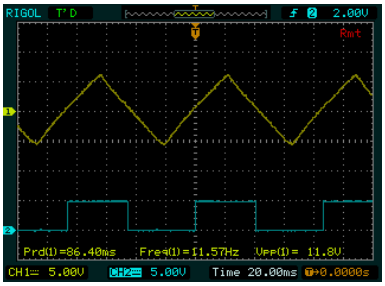


Figure 18. ≥10Hz Triangle

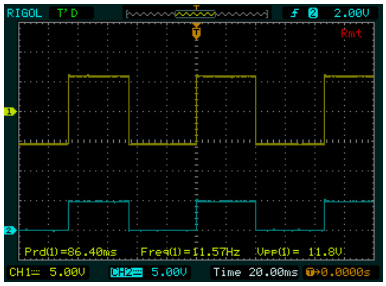


Figure 19. ≥10Hz Square

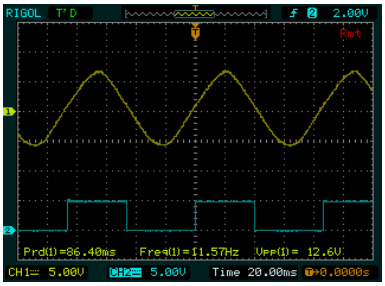


Figure 20. ≥10Hz Sine

20. Verify the minimum and maximum frequency of each waveform on each of the remaining FG range settings. You should observe the waveforms are shown in Figures 21 through 50. Adjust the oscilloscope setting as indicated as you progress through the ranges.

SCOPE: 20mS Auto Trigger, FREQ SETTING: 100Hz x 0.1, LIMIT: ≤10Hz (≥100mS)

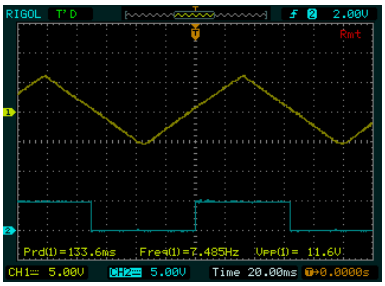


Figure 21. ≤10Hz Triangle

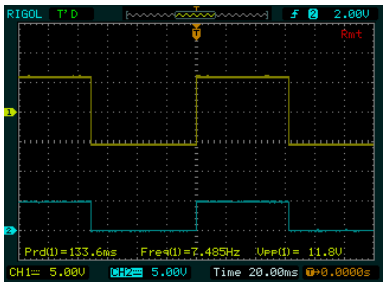


Figure 22. ≤10Hz Square

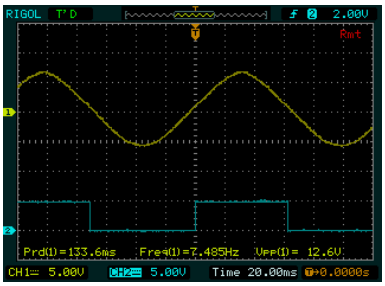


Figure 23. ≤10Hz Sine

SCOPE: 2mS Auto Trigger, FREQ SETTING: 100Hz x 1, LIMIT: ≥100Hz (≤10mS)

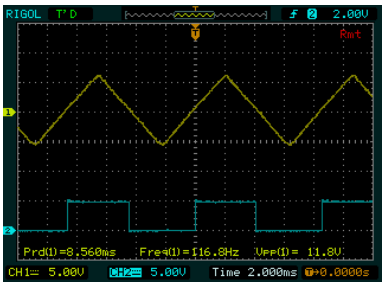


Figure 24. ≥100Hz Triangle

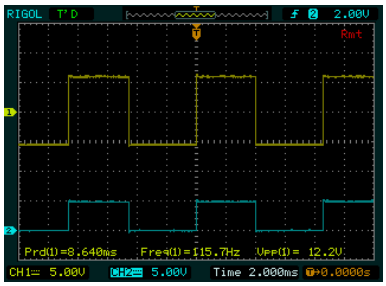


Figure 25. ≥100Hz Square

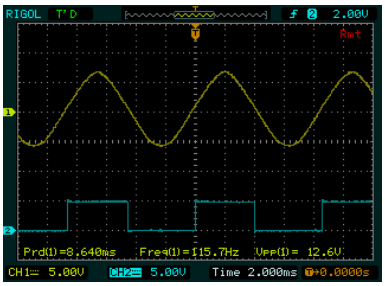


Figure 26. ≥100Hz Sine

SCOPE: 2mS Auto Trigger, FREQ SETTING: 1KHz x 0.1, LIMIT: ≤100Hz (≥10mS)

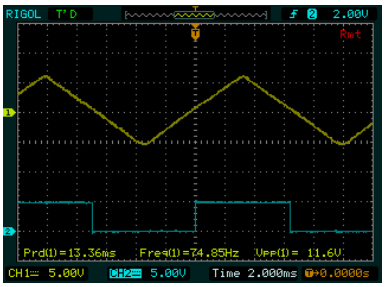


Figure 27. ≤100Hz Triangle

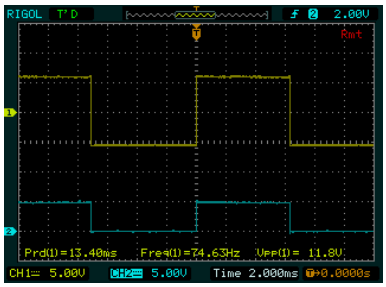


Figure 28. ≤100Hz Square

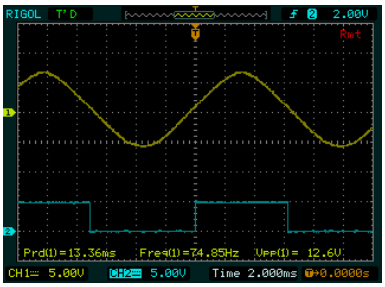


Figure 29. ≤100Hz Sine

SCOPE: 200µS Auto Trigger, FREQ SETTING: 1KHz x 1, LIMIT: ≥1KHz (≤1mS)

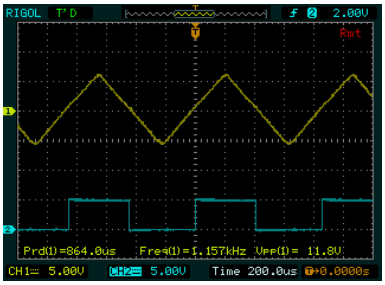


Figure 30. ≥1KHz Triangle

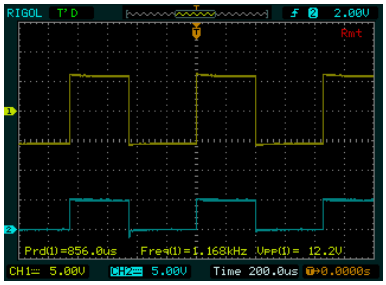


Figure 31. ≥1KHz Square

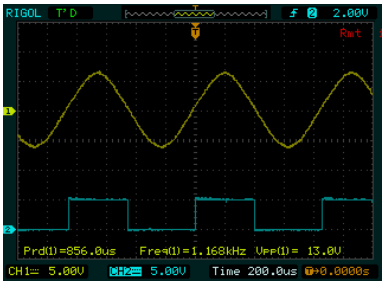


Figure 32. ≥1KHz Sine

SCOPE: 200µS Auto Trigger, FREQ SETTING: 10KHz x 0.1, LIMIT: ≤1KHz (≥10mS)

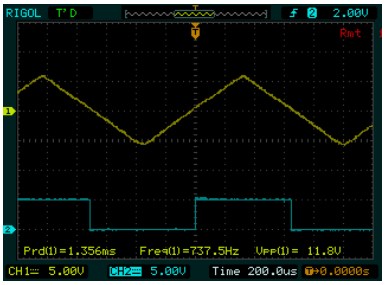


Figure 33. ≤1KHz Triangle

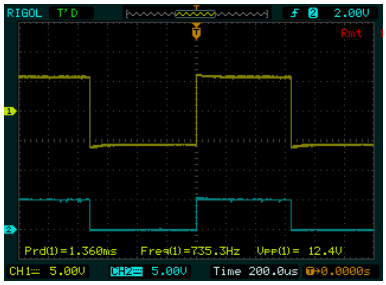


Figure 34. ≤1KHz Square

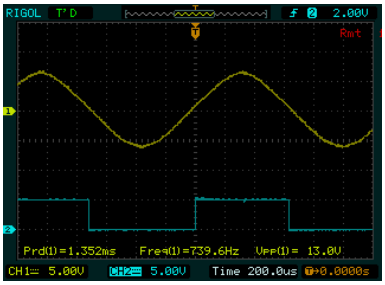


Figure 35. ≤1KHz Sine

SCOPE: 20µS Auto Trigger, FREQ SETTING: 10KHz x 1, LIMIT: ≥10KHz (≤100µS)

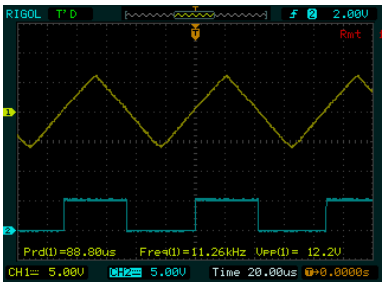


Figure 36. ≥10KHz Triangle

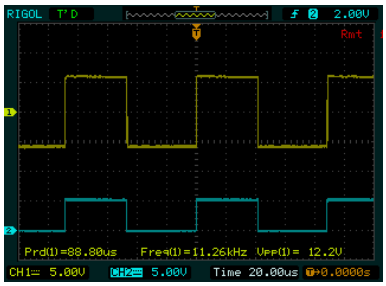


Figure 37. ≥10KHz Square

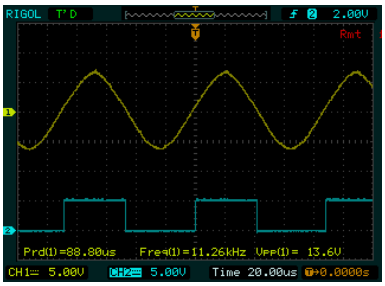


Figure 38. ≥10KHz Sine

SCOPE: 20µS Auto Trigger, FREQ SETTING: 100KHz x 0.1, LIMIT: ≤10KHz (≥100µS)

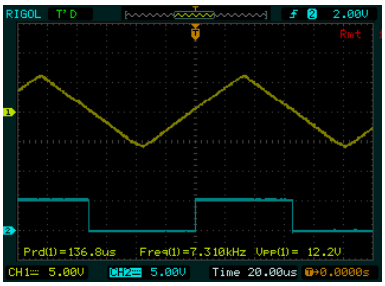


Figure 39. ≤10KHz Triangle

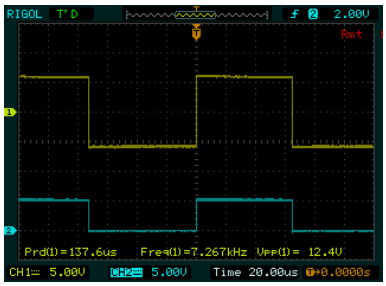


Figure 40. ≤10KHz Square

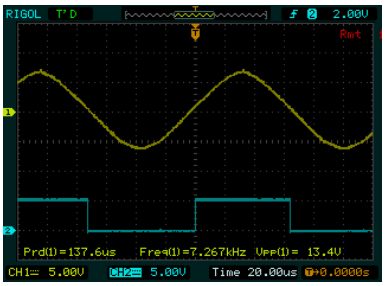


Figure 41. ≤10KHz Sine

SCOPE: 2µS Auto Trigger, FREQ SETTING: 100KHz x 1, LIMIT: ≥100KHz (≤10µS)

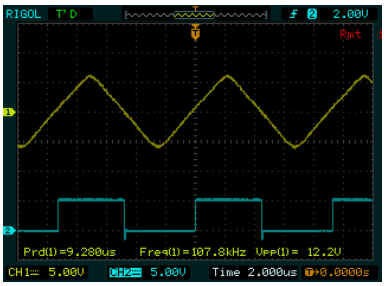


Figure 42. ≥100KHz Triangle

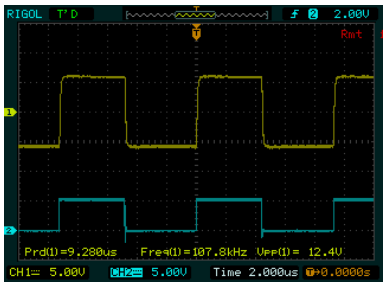


Figure 43. ≥100KHz Square

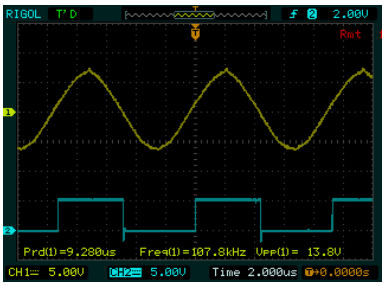


Figure 44. ≥100KHz Sine

SCOPE: 2µS Auto Trigger, FREQ SETTING: 1MHz x 0.1, LIMIT: ≤100KHz (≥10µS)

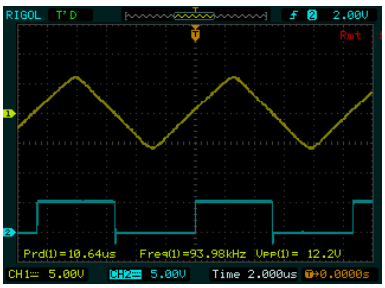


Figure 45. ≤100KHz Triangle

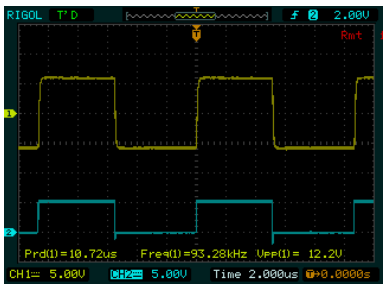


Figure 46. ≤100KHz Square

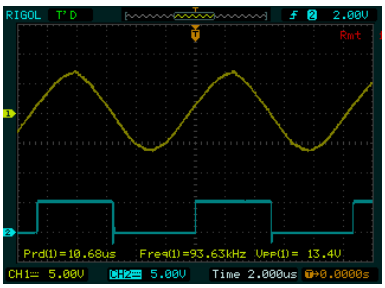


Figure 47. ≤100KHz Sine

The roll off of the Sine, Triangle, and Square wave in Figures 48, 49, and 50 is typical and should not be considered an indication of problem. Likewise the small perturbation at the positive peak of the Sine wave, if present on your ML2010, is primarily due to the intrinsic nature of the XR2206 Function Generator IC and should not be considered as an indication of a problem.

SCOPE: 200nS Auto Trigger, FREQ SETTING: 1MHz x 1, LIMIT: ≥1MHz (≤1µS)

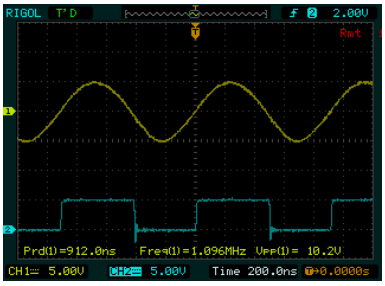


Figure 48. ≥1MHz Triangle

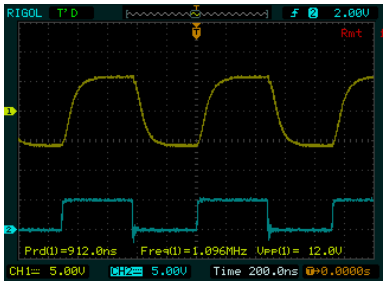


Figure 49. ≥1MHz Square

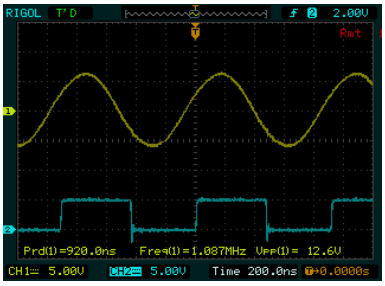


Figure 50. ≥1MHz Sine

21. Set the FG RANGE control to the 10K position and the FINE FREQUENCY to x1 (fully clockwise). Set the FG WAVEFORM to triangle and the oscilloscope horizontal time base to 200µSEC. You should observe the waveform shown in Figure 51 on the oscilloscope.

22. To verify the operation of the BURST IN input connect a 24AWG solid wire from the FG GND tie point block to the BURST IN tie point block. When the BURST IN input is pulled low it disables the FG GEN OUT and CLOCK OUT. When the Sine or Triangle waveform is selected, the FG outputs (GEN OUT and CLOCK OUT) should rest at ~0vdc, as shown in Figure 52. When the Square Wave output is selected the FG outputs should rest at approximately -6VDC as shown in Figure 53.

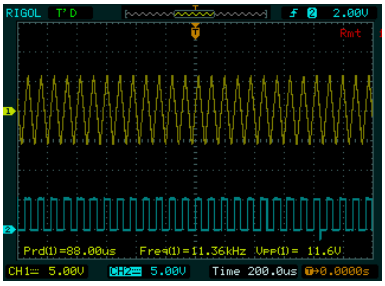


Figure 51. Function Generator
10KHz x 1 Setting

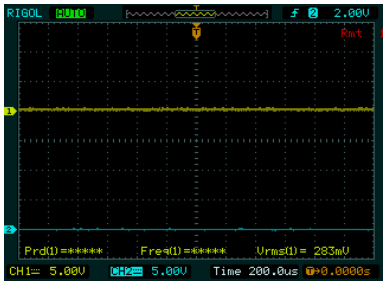


Figure 52. Sine & Triangle Wave
BURST IN Grounded

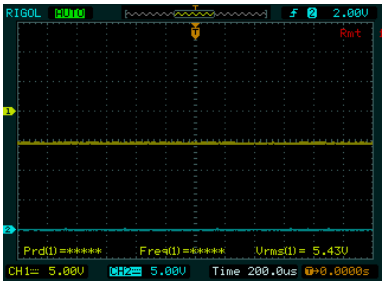


Figure 53. Square Wave
BURST IN Grounded

23. Remove the 24AWG solid wire from the BURST IN and GND tie point blocks.

24. Remove the oscilloscope CH2 probe from the FG GND and CLOCK OUT tie point blocks and make the following connections:

    a. CH2 Oscilloscope Probe ground to the SG GND tie point block.
    b. CH2 Oscilloscope Probe input to the SG OUT tie point block.

25. Adjust the Oscilloscope to the following settings:

a. CH2 Vertical Gain	1V/DIV – DC Coupled
b. CH2 Baseline	-3V (1 major division up from bottom screen)
c. Trigger	CH2 – DC Coupled – Rising Edge – Auto Mode
d. Trigger Level	1V (Referenced to CH2)

26. Adjust the SG for 2Vpp and a period of ~1mSEC as shown in Figure 54 (Since the FG output is not synchronous to the SG output, you should notice that the oscilloscope sweep was stopped to capture Figure 54 through 56.)

27. Connect a 24AWG solid wire from the SG OUT tie point block to the FG AM IN tie point block. You should observe the waveforms as shown if Figure 55.

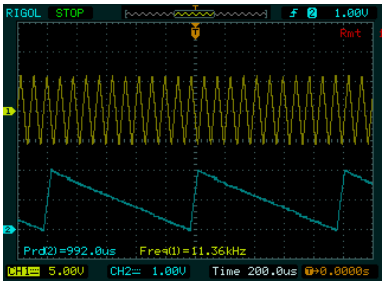


Figure 54. Generator Setups for Test

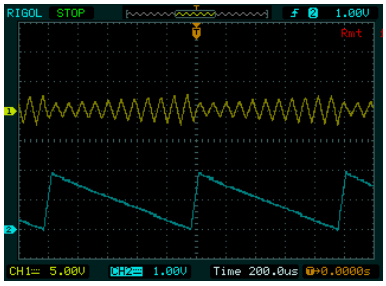


Figure 55 Amplitude Modulation Input Test

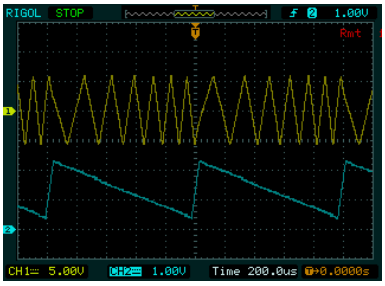


Figure 56. Frequency Modulation Input Test

28. Move the 24AWG wire from the AM IN tie point block to the SWEEP IN tie point block. You should observe the waveforms as shown if Figure 56. Note the DC offset of the SG OUT when connected to the FG FM IN is normal and not an indication of a problem.

29. This concludes the FG checkout. Remove the 24AWG solid wire connecting the SG OUT to the FG AM IN and disconnect the CH1 and CH2 oscilloscope probe connections from the ML2010.

4. PULSE GENERATOR (PG) CHECKOUT

This procedure is written as a standalone procedure and assumes the FG and SG of the ML2010 have been tested, calibrated, and deemed to be in proper working order. It is also assumed that the ML2010 is powered on and no connections to other test equipment exist.

1. Adjust the Oscilloscope to the following settings:

a. Horizontal Time Base	1mSEC/DIV
b. Horizontal Position	5mSEC (5 divisions left of center screen)
b. CH1 Vertical Gain	2V/DIV - DC Coupled
c. CH1 Base Line	0V (center screen)
d. CH2	OFF
e. Trigger	CH1 - DC Coupled - Rising Edge - Auto Mode
g. Trigger Level	2V (Referenced to CH1)

2. Using 24AWG solid wires connect the CH1 probe ground to the PG GND tie point block and the CH1 probe input to the PG OUT tie point block.

3. To verify the PG calibration, set the PG PERIOD RANGE switch to the 10mSEC position and rotate the PERIOD FINE control to the x1 position.

4. Set the PG WIDTH RANGE switch to the 1mSEC position and rotate the WIDTH FINE control to the x1 position. You should observe the waveform shown in Figure 57.

5. Verify that the PG output waveform period is 10mSEC. If necessary the period can be re-calibrated by adjusting R11 on the FA0013 PLS Gen-LED-PS PCB. R11 is accessible through the front cover via the hole labeled CAL to the lower left of the PERIOD FINE control knob.

6. Set the oscilloscope horizontal position to 0 SEC (horizontal center screen) and the horizontal time base to 200µSEC/DIV. Verify that the PG pulse width is 1mSEC as shown in Figure 58. If necessary the pulse width can be re-calibrated by adjusting R15 on the FA0013 PLS Gen-LED-PS PCB. R15 is accessible through the front cover via the hole labeled CAL to the lower left of the WIDTH FINE control knob.

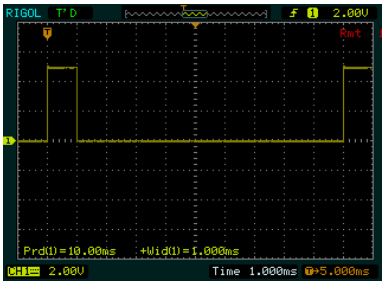


Figure 57. PG 10mSEC Pulse Period

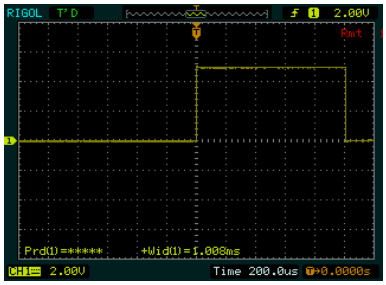


Figure 58. PG 1mSEC Pulse Width

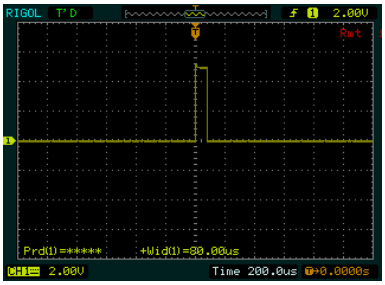


Figure 59. PG ≤100µSEC Pulse Width

7. Rotate the PG WIDTH FINE control to the x0.1 position. Verify the pulse width is ≤100µSEC as shown is Figure 59.

8. Rotate the PG PERIOD RANGE switch to the 10µSEC position and verify that the OVERLAP LED indicator illuminates. Overlap occurs whenever the pulse width settings are greater than the pulse period settings. During an overlap condition the PG output rests at approximately +5VDC.

9. Verify the minimum and maximum pulse periods and pulse widths on each of the pulse period and pulse width ranges. Remember in order to avoid an overlap condition that the PG pulse period must be greater than the pulse width.

10. Make the following connections:

    a. CH2 probe ground to FG GND tie point block and CH2 probe input to FG CLOCK OUT tie point block.
    b. Using a 24AWG solid wire connect the FG CLOCK OUT to the PG TRIG tie point block.

11. Adjust the oscilloscope to the following settings:

    a. Horizontal Time Base — 200µSEC/DIV
    b. CH1 Vertical Gain — 2V/DIV – DC Coupled
    c. CH1 Base Line — 0V (center screen)
    d. CH2 Vertical Gain — 2V/DIV – DC Coupled
    e. CH2 Base Line — -6V (1 major division up from screen bottom)
    f. Trigger — CH2 – DC Coupled – Rising Edge – Auto Mode
    g. Trigger Level — 2V (Referenced to CH2)

12. Set the FG RANGE to 1K and adjust the FG FINE FREQUENCY to obtain a clock signal of 1KHz. Note: If the frequency of the clock is greater than 1KHz you will not be able to obtain the waveforms as shown in Figure 60.

13. Adjust the PG controls to the following settings:

    a. Pulse PERIOD RANGE — 100mSEC
    b. Pulse PERIOD FINE — x1 (fully clockwise)
    c. Pulse WIDTH RANGE — 10mSEC
    d. Pulse WIDTH FINE — x0.1

14. Verify that the rising edge of the FG clock (CH2) triggers the PG output (CH1) as shown in Figure 60. When using the TRIG input of the PG each rising edge of the trigger signal will cause the PG to begin its timing cycle based on the period and width range settings.

15. Using a 24AWG solid wire connect the TRIG tie point block to the GATE tie point block. You should observe the waveforms shown in Figure 61. The PG output should remain low the entire time the GATE input is held low by the FG clock. The function of the GATE input of the PG is to inhibit the output when held low.

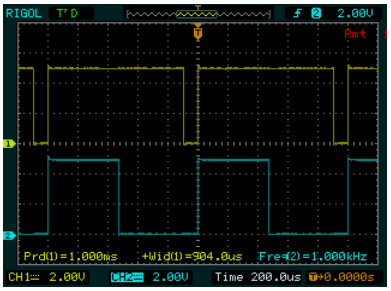


Figure 60. 1KHz Trigger

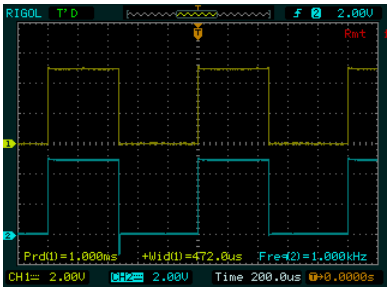


Figure 61. 1KHz Trigger & Gate

16. Disconnect the 24AWG solid wire connecting the TRIG to GATE tie point block. Note: The Overlap Indicator should turn off.

17. Verify the FG CLOCK OUT is still at 1KHz then set the oscilloscope horizontal time base to 10µSEC.

18. Set the PG WIDTH RANGE to 100µSEC and adjust the PG WIDTH FINE control to obtain 30µSEC pulse width.

19. Set the oscilloscope horizontal time base to 50µSEC.

20. Set the PG PERIOD RANGE switch to 100µSEC and adjust the PERIOD FINE RANGE control to obtain a 100µSEC period (10KHz).

21. Set the horizontal time base to 100µSEC and turn on delayed sweep. You should observe the waveforms as shown in Figure 62.

22. Using a 24AWG solid wires connect the FG CLOCK OUT to PG TRIG and PPM.

23. Press the RUN/STOP button on the oscilloscope to capture the waveforms and verify that the waveforms are as shown in Figure 63.

24. Move the 24AWG solid wire from the PG PPM tie point block to the PWM tie point block and capture the waveform using the RUN/STOP button. You waveform should match that of Figure 64.

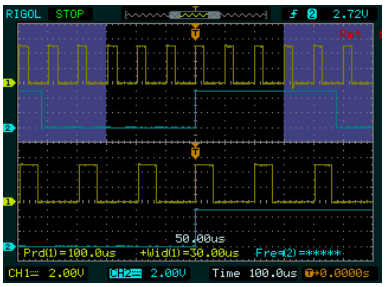


Figure 62. FG/PG Setup

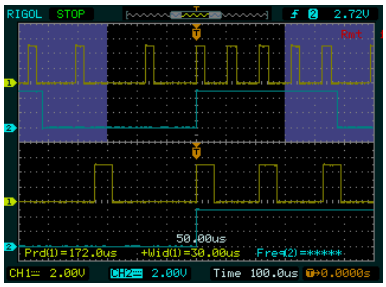


Figure 63. PPM

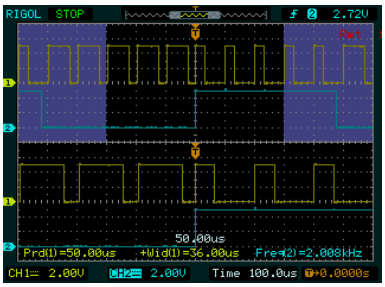


Figure 64. PWM

25. This concludes the PG check out. Remove all equipment connections.

5. LED INDICATOR CHECKOUT

This procedure is written as a standalone procedure and assumes the power supplies of the ML2010 have been tested and deemed to be in proper working order. It is also assumed that the ML2010 is powered on and no connections to other test equipment exist.

1. Verify that all LED indicators are off.

2. Connect one end of a 24AWG solid wire to the +5V tie point block.

3. Connect the other end of the 24AWG solid wire to LED 0 and verify that when connected that LED 0 is on.

4. Remove the 24AWG solid wire from the LED 0 tie point block. LED 0 should turn off.

5. Repeat steps 2 through 4 for each of the remaining seven LED indicators.

6. UNDEDICATED MOMENTARY TOGGLE SWITCH CHECKOUT

This procedure is written as a standalone procedure and assumes the power supplies of the ML2010 have been tested and deemed to be in proper working order. It is also assumed that the ML2010 is powered on and no connections to other test equipment exist.

The at rest position of the bat handle of the momentary switch used on the ML2010 is towards the tie point blocks and labeled NORM. The terms normally open (NO) and normally closed (NC) use the at rest state to derive their meaning. When the switch is at rest, the common pole (C) of the switch is connected to the NC pole and not to the NO pole. Upon activation of the switch this condition is reversed, the C pole is connected to the NO pole and disconnected from the NC pole. When the switch is released the bat handle and continuity of the switch return to the at rest condition.

1. Using 24AWG solid wire connect the normally open (NO) tie point block of the upper undedicated momentary toggle switch to LED 0.

2. Using 24AWG solid wire connect the normally closed (NC) tie point block of the upper undedicated momentary toggle switch to LED 1.

3. Using 24AWG solid wire connect the common (C) tie point block of the upper undedicated momentary toggle switch to the +5V tie point block.

4. With bat handle in the at rest position LED 0 should be off and LED 1 should be on.

5. Actuate the momentary switch and verify that LED 0 turns on and LED 1 turns off.

6. Verify that when the bat handle is released that it returns to the NORM position, LED 0 turns off, and LED 1 turns on.

7. Repeat the procedure for the second (lower) undedicated momentary switch.

7. UNDEDICATED TOGGLE SWITCH CHECKOUT

This procedure is written as a standalone procedure and assumes the power supplies of the ML2010 have been tested and deemed to be in proper working order. It is also assumed that the ML2010 is powered on and no connections to other test equipment exist.

The at rest position of the bat handle of the SPDT toggle switch used on the ML2010 is towards the tie point blocks and labeled NORM. The terms normally open (NO) and normally closed (NC) use the at rest state to derive their meaning. When the switch is at rest, the common pole (C) of the switch is connected to the NC pole and not to the NO pole. Upon activation of the switch this condition is reversed, the C pole is connected to the NO pole and disconnected from the NC pole. When the switch is returned to the NORM position the continuity of the switch is the C pole is connected to the NC pole.

1. Using 24AWG solid wire connect the normally open (NO) tie point block of the upper undedicated toggle switch to LED 0.

2. Using 24AWG solid wire connect the normally closed (NC) tie point block of the upper undedicated toggle switch to LED 1.

3. Using 24AWG solid wire connect the common (C) tie point block of the upper undedicated toggle switch to the +5V tie point block.

4. With bat handle in the at rest position LED 0 should be off and LED 1 should be on.

5. Actuate the switch and verify that LED 0 turns on and LED 1 turns off.

6. Verify that when the bat handle is returned to the NORM position, LED 0 turns off, and LED 1 turns on.

7. Repeat the procedure for the second (lower) toggle momentary switch.

8. Remove all connections.

8. TTL/HC DEBOUNCED PULSER SWITCHES CHECKOUT

This procedure is written as a standalone procedure and assumes the power supplies of the ML2010 have been tested and deemed to be in proper working order. It is also assumed that the ML2010 is powered on and no connections to other test equipment exist.

The at rest position of the bat handle of the momentary switch used for the TTL/HC pulsers on the ML2010 is towards the tie point blocks and labeled L for the upper tie point block and H for the lower tie point block. Those labels indicate the logic level of the tie point blocks when the switch is in the at rest position. When the switch is at rest, the upper tie point block is at a TTL/HC low level (≤0.5VDC) and the lower tie point block is at a TTL/HC high logic level (≥4.4VDC). Upon activation of the switch this condition is

reversed as indicated by the legends on the right side of the switch. When the switch is actuated the upper tie point block is a TTL/HC high logic level and the lower block is a TTL/HC low logic level. When the switch is released the bat handle and logic levels of the switch and tie point blocks return to the at rest condition.

1. Using 24AWG solid wire connect the normally low (L) tie point block of the upper TTL/HC pulser switch to LED 0.

2. Using 24AWG solid wire connect the normally high (H) tie point block of the upper TTL/HC pulser switch to LED 1.

3. With bat handle in the at rest position LED 0 should be off and LED 1 should be on.

4. Actuate the momentary pulser switch and verify that LED 0 turns on and LED 1 turns off.

5. Verify that when the bat handle is released that it returns to the at rest position, LED 0 turns off, and LED 1 turns on.

6. Repeat the procedure for the second (lower) TTL/HC pulser switch.

7. Remove all connections.

9. TTL/HC LEVEL SPDT TOGGLE SWITCH CHECKOUT

This procedure is written as a standalone procedure and assumes the power supplies of the ML2010 have been tested and deemed to be in proper working order. It is also assumed that the ML2010 is powered on and no connections to other test equipment exist.

The TTL/HC Level SPDT toggle switches are numbered 0 through 7 for reference and have a level indicator legend L (low or 0VDC) and H (high or +5VDC). When the switch is to the left or L position the associated tie point block will be at 0VDC. When the switch is to the right or H position the associated tie point block will be at +5VDC. The TTL/HC level switches are not buffered or protected. The +5VDC and 0VDC levels are directly connected to the +5VDC power supply.

1. Position the bat handles of the eight TTL/HC level switches to the L (low, left, or inboard) position.

2. Using 24AWG solid wire connect the level switch 0 tie point block to LED 0 tie point block.

3. Verify that with the level switch in the L position LED 0 is off.

4. Toggle the switch to the H position and verify that LED 0 is now on.

5. Repeat the procedure for each of the remaining TTL/HC level switches.

6. Remove all connections.

10. BNC CONNECTORS

This procedure is written as a standalone procedure. It assumes that the ML2010 is powered on and no connections to other test equipment exist. Also assumed is that the DMM probes are mini-grabber or alligator type probes and are properly connect to the DMM.

1. Connect one end of a 24AWG solid wire the V/Ω input (red lead) of the DMM.

2. Connect one end of a 24AWG solid wire to the COM input (black lead) of the DMM.

3. Set the DMM rotary switch to the 200Ω/Continuity Test position.

4. Connect the 24AWG solid wire attached to DMM COM probe the to the S tie point block of the BNC connector on the left side of the ML2010.

5. Touch the 24AWG solid wire attached to the DMM V/Ω probe to the outer shell of the BNC under test. An audible tone should be heard from the DMM.

6. Touch the 24AWG solid wire attached to the DMM V/Ω probe to the gold center conductor of the BNC under test and the DMM should indicate an open circuit.

7. Touch the 24AWG solid wire attached to the DMM V/Ω probe to the C tie point block of the BNC under test and the DMM should indicate an open circuit.

8. Move the 24AWG solid wire from the S tie point block to the C tie point block of the BNC under test.

9. Touch the 24AWG solid wire attached to the DMM V/Ω probe to the outer shell of the BNC under test and the DMM should indicate an open circuit.

10. Touch the 24AWG solid wire attached to the DMM V/Ω probe to the gold center conductor of the BNC under test. An audible tone should be heard from the DMM.

11. Touch the 24AWG solid wire attached to the DMM V/Ω probe to the S tie point block of the BNC under test and the DMM should indicate an open circuit.

12. Repeat the procedure for the remaining two BNC connectors located on the right hand side of the ML2010 cover plate.

10. DB25/DB9 CONNECTORS

This procedure is written as a standalone procedure. It assumes that the ML2010 is powered on and no connections to other test equipment exist. Also assumed is that the DMM probes are mini-grabber or alligator type probes and are properly connect to the DMM.

1. Connect one end of a 24AWG solid wire the V/Ω input (red lead) of the DMM and one end of a 24AWG solid wire to the COM input (black lead) of the DMM.

2. Set the DMM rotary switch to the 200Ω/Continuity Test position.

3. For left hand DSUB connector group confirm continuity of pins 1 through 25 on the DB25 male (DB25M) and DB25 female (DB25F) connectors.

4. Confirm the continuity of the DB9 male (DB9M) pins to the first nine pins of both the DB25M and DB25F connectors.

5. For the right hand DSUB connector group confirm continuity of pins 1 through 25 on the DB25F to the other DB25F connector.

6. Also confirm continuity of the DB9F pins to the first nine pins of both the DB25F connectors.

7. Remove all connections.

11. POTENTIOMETERS

This procedure is written as a standalone procedure. It assumes that the ML2010 is powered on and no connections to other test equipment exist. Also assumed is that the DMM probes are mini-grabber or alligator type probes and are properly connect to the DMM.

The legends CW (clockwise), WPR (wiper), and CCW (counterclockwise) are used to identify the terminals of the potentiometers. With reference to the wiper (WPR) terminal the terms describe the rotation that causes the resistance to decrease between the two terminals being referenced. This means that when the potentiometer shaft is rotated clockwise the resistance between the WPR and CW terminals will decrease and the resistance between the WPR and CCW terminals will increase. Conversely, when the potentiometer shaft if rotated counterclockwise the resistance between the WPR and CCW terminals will decrease and the resistance between the WPR and CW terminals will increase.

1. Set the rotary dial of the DMM to the 2KΩ range.

2. Rotate the 1KΩ potentiometer fully counterclockwise.

3. Connect one end of a 24AWG solid wire the V/Ω input (red lead) of the DMM and the other end to the 1KΩ tie point block labeled CW.

4. Connect one end of a 24AWG solid wire to the COM input (black lead) of the DMM and the other end to the 1KΩ tie point block labeled CCW. A reading of 1K ±20% should be observed.

5. Move the 24AWG solid wire from the CCW tie point block to the WPR tie point block. With the potentiometer full counterclockwise you should again observe a reading of 1KΩ ±20%. Notice that as you rotate the potentiometer control clockwise the resistance decreases. In the fully clockwise position you should observe a reading of 0Ω ±15Ω.

6. Move the 24AWG solid wire from the CW tie point block to the CCW tie point block. You should observe a reading of 1KΩ ±20% and as you rotate the potentiometer control counterclockwise you should see the resistance value decreasing. In the fully clockwise position you should observe a reading of 0Ω ±15Ω.

7. Set the rotary dial of the DMM to the 200KΩ range.

8. Rotate the 100KΩ potentiometer fully counterclockwise and repeat the procedure above for the 100KΩ potentiometer. The reading should now be 100KΩ ±20% down to 0Ω ±15Ω.

9. Remove all connections.

11. SPEAKER

This procedure is written as a standalone procedure and assumes the FG section of the ML2010 has been tested and deemed to be in proper working order. It is also assumed that the ML2010 is powered on and no connections to other test equipment exist.

1. Set the FG controls as follows:

A. WAVEFORM	Square Wave
b. RANGE	1 KHz
c. AMPLITUDE	0
d. FINE FREQUENCY	x1
d. OFFSET	Midrange

2. Connect one end of a 24AWG solid wire to the upper SPEAKER tie point block and connect the other end to the FG GND tie point block.

3. Connect one end of a 24AWG solid wire to the lower SPEAKER tie point block and connect the other end to the FG GEN OUT tie point block.

4. Turn the AMPLITUDE knob clockwise. A 1 KHz tone should be heard with the intensity increasing as the knob is turned.

5. Remove all connections.

SCHEMATICS

LEFT BLANK INTENTIONALLY

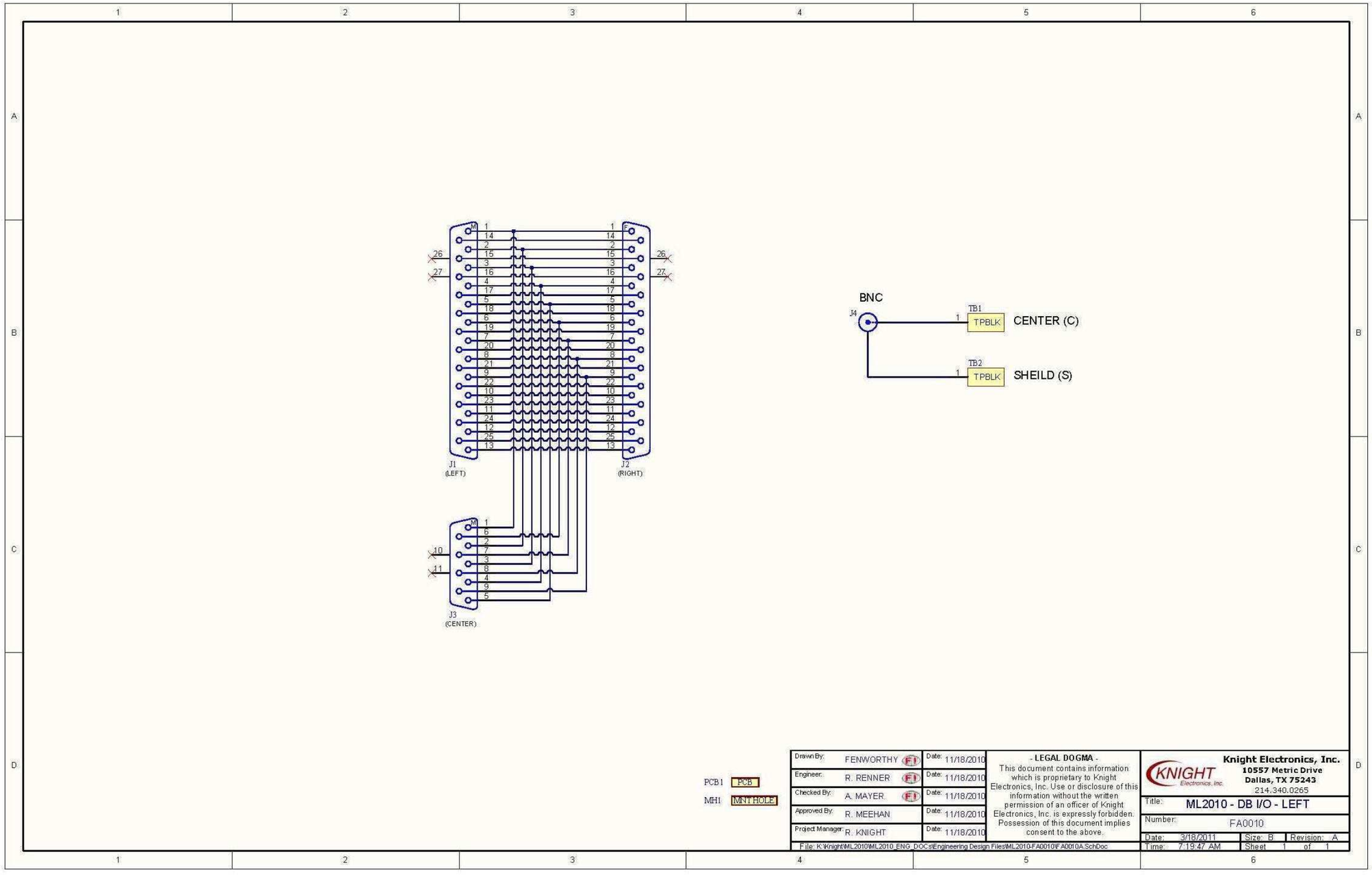


Figure 65. FA0010 ML2010 – DB I/O LEFT SCHEMATIC

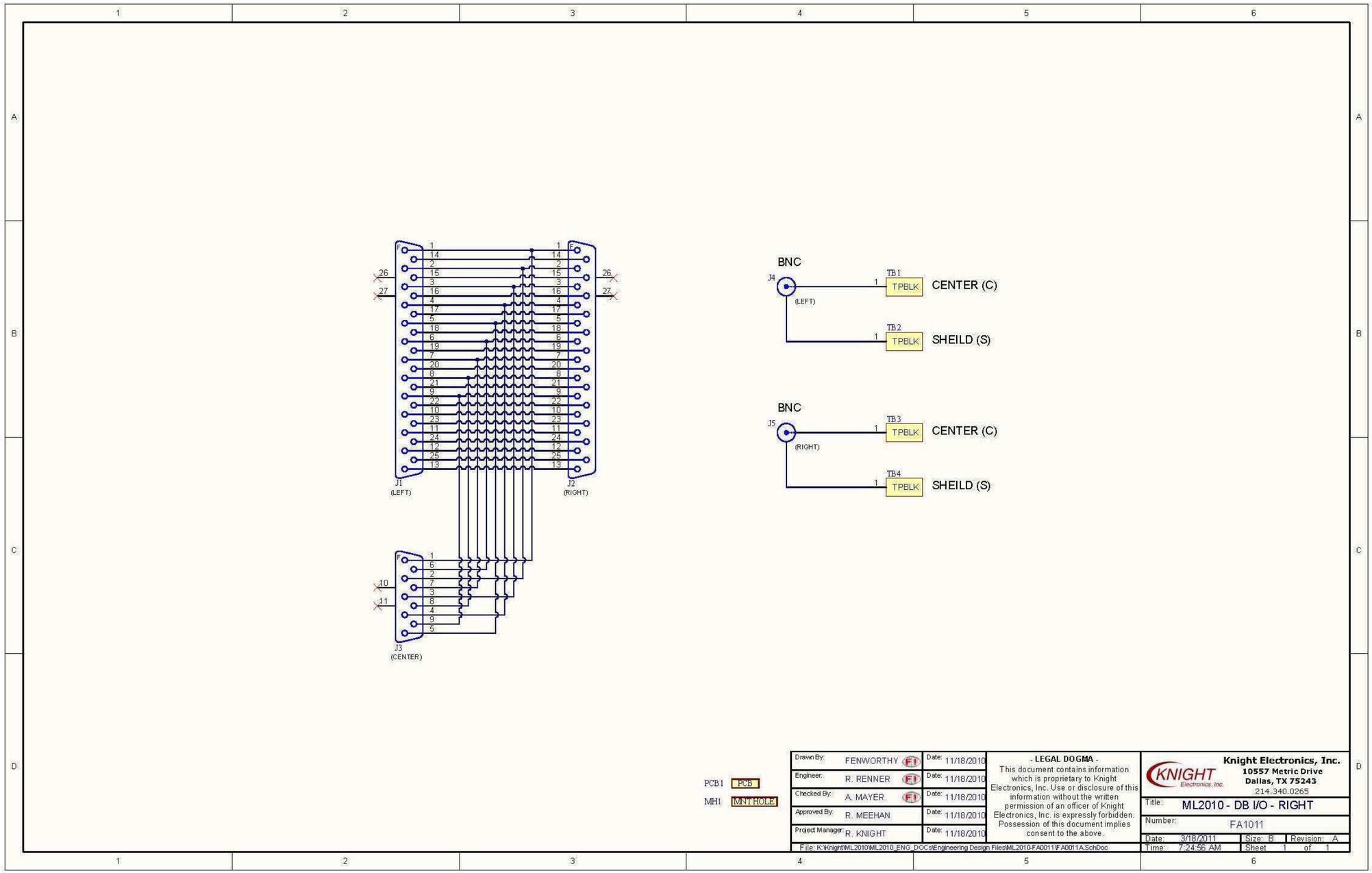


Figure 66. FA0011 ML2010 – DB I/O RIGHT SCHEMATIC

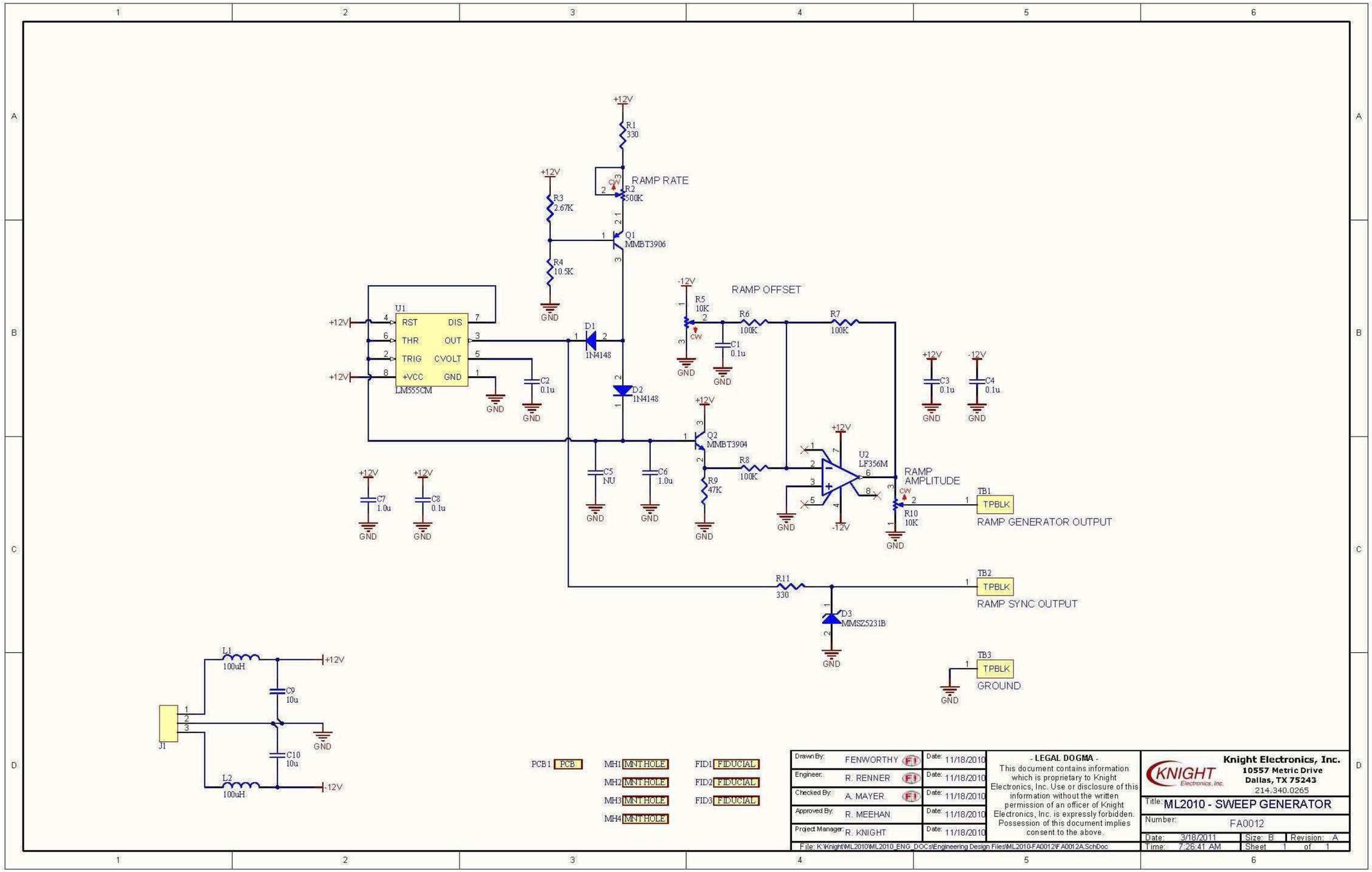


Figure 67. FA0012 ML2010 – SWEEP GENERATOR SCHEMATIC

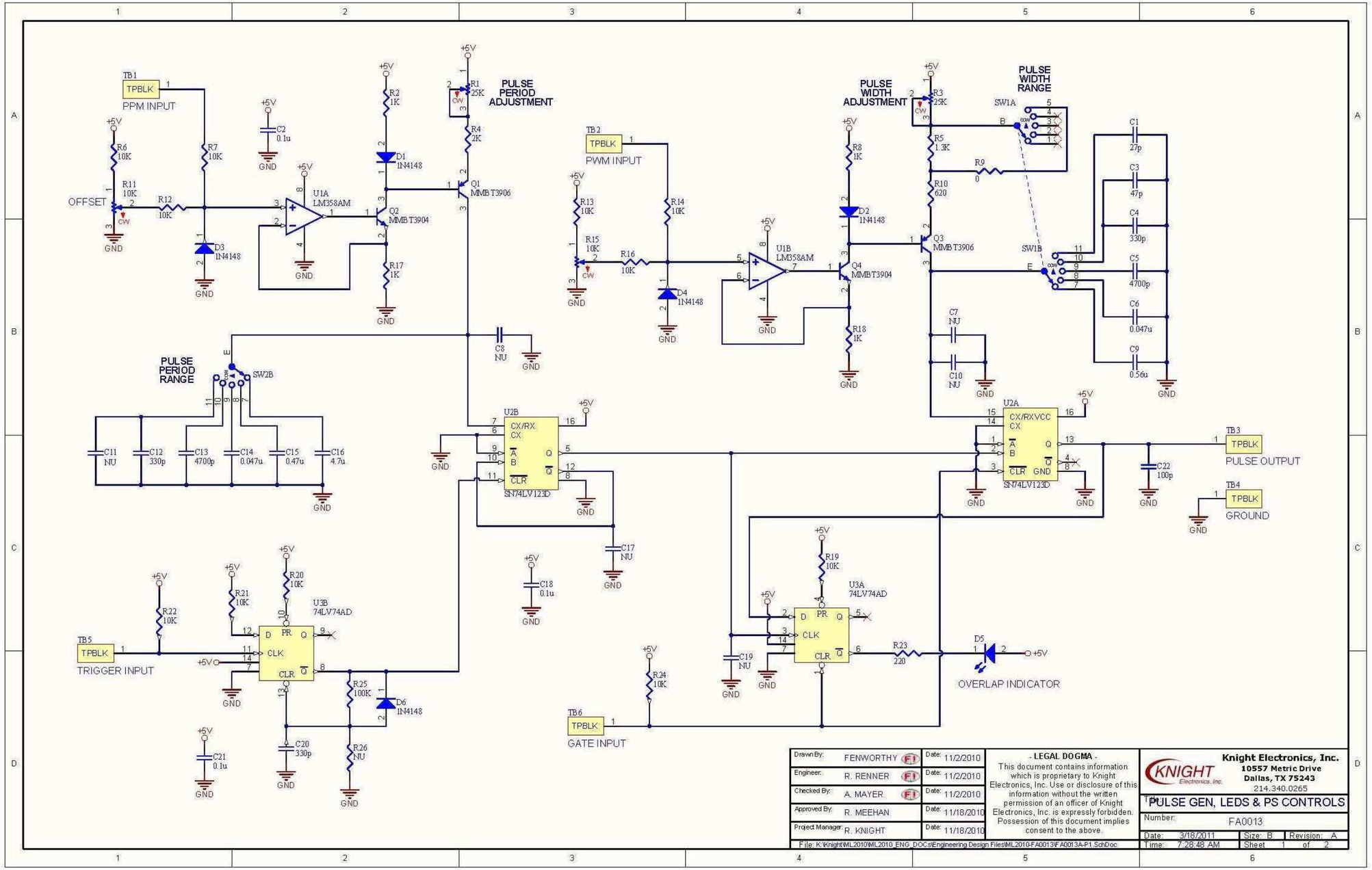


Figure 68. FA0013 ML2010 – PULSE GEN, LEDS & PS CONTROLS PAGE 1 SCHEMATIC

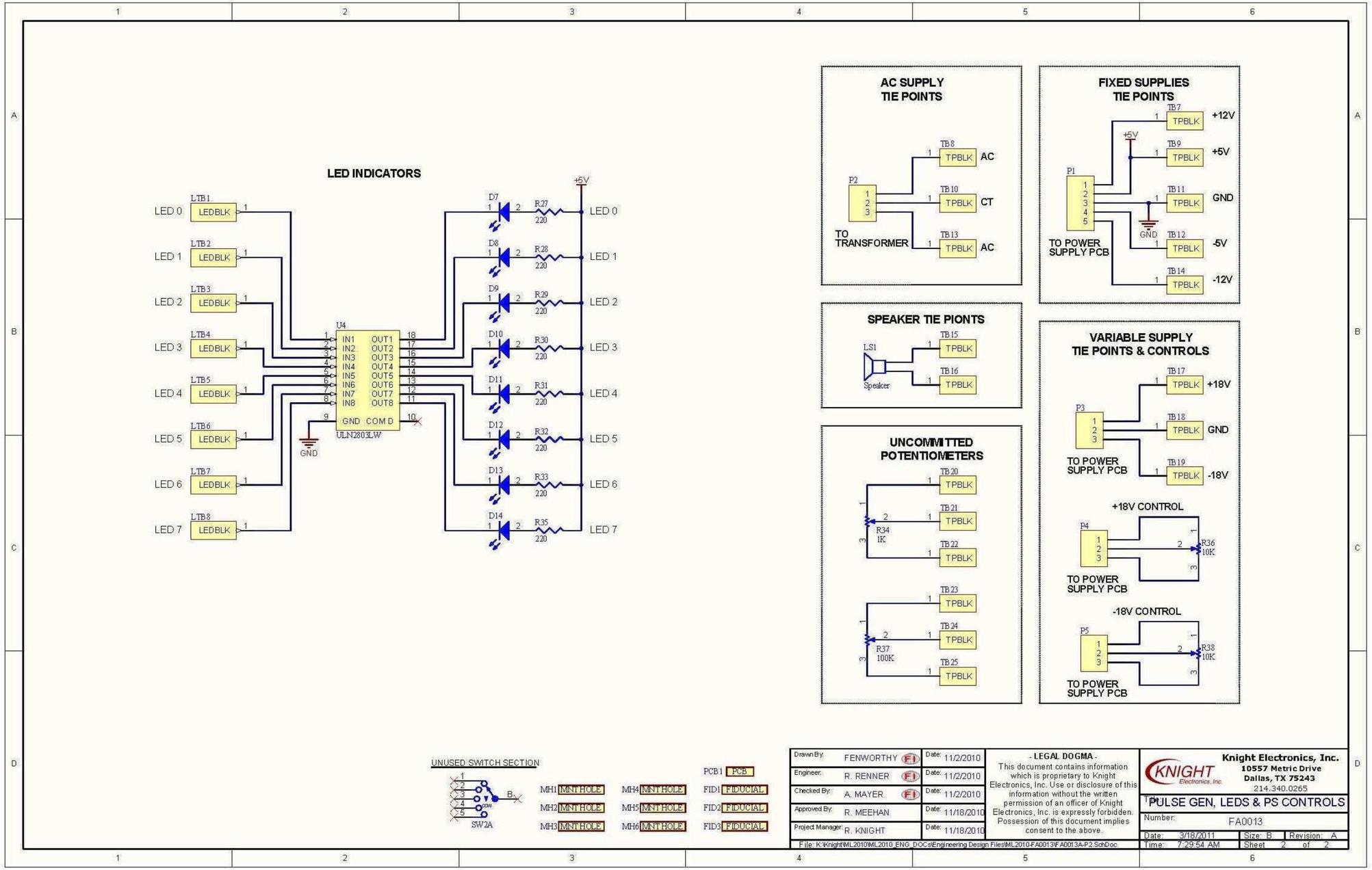


Figure 69. FA0013 ML2010 – PULSE GEN, LEDS & PS CONTROLS PAGE 2 SCHEMATIC

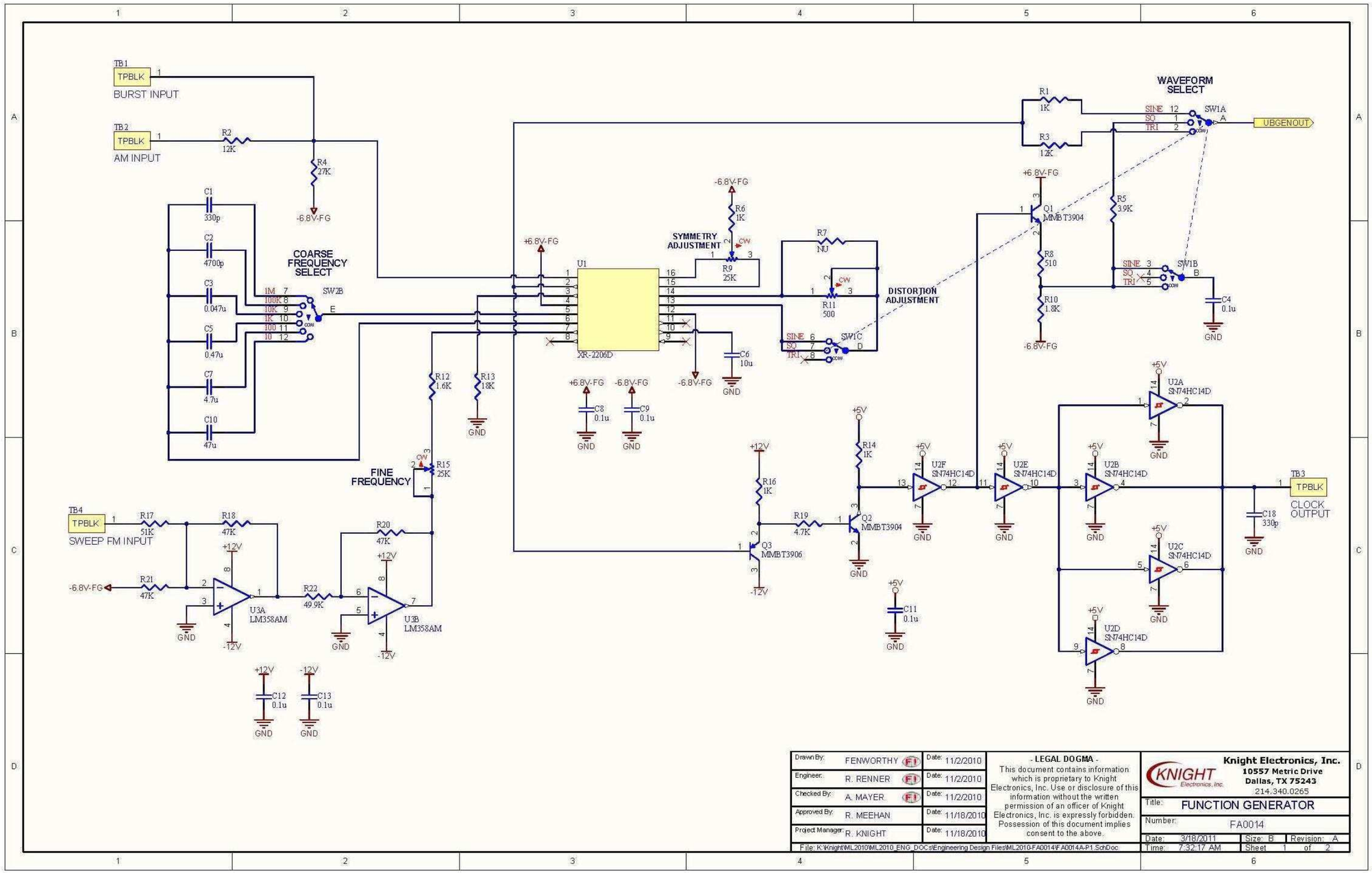


Figure 70. FA0014 ML2010 – FUNCTION GENERATOR PAGE 1 SCHEMATIC

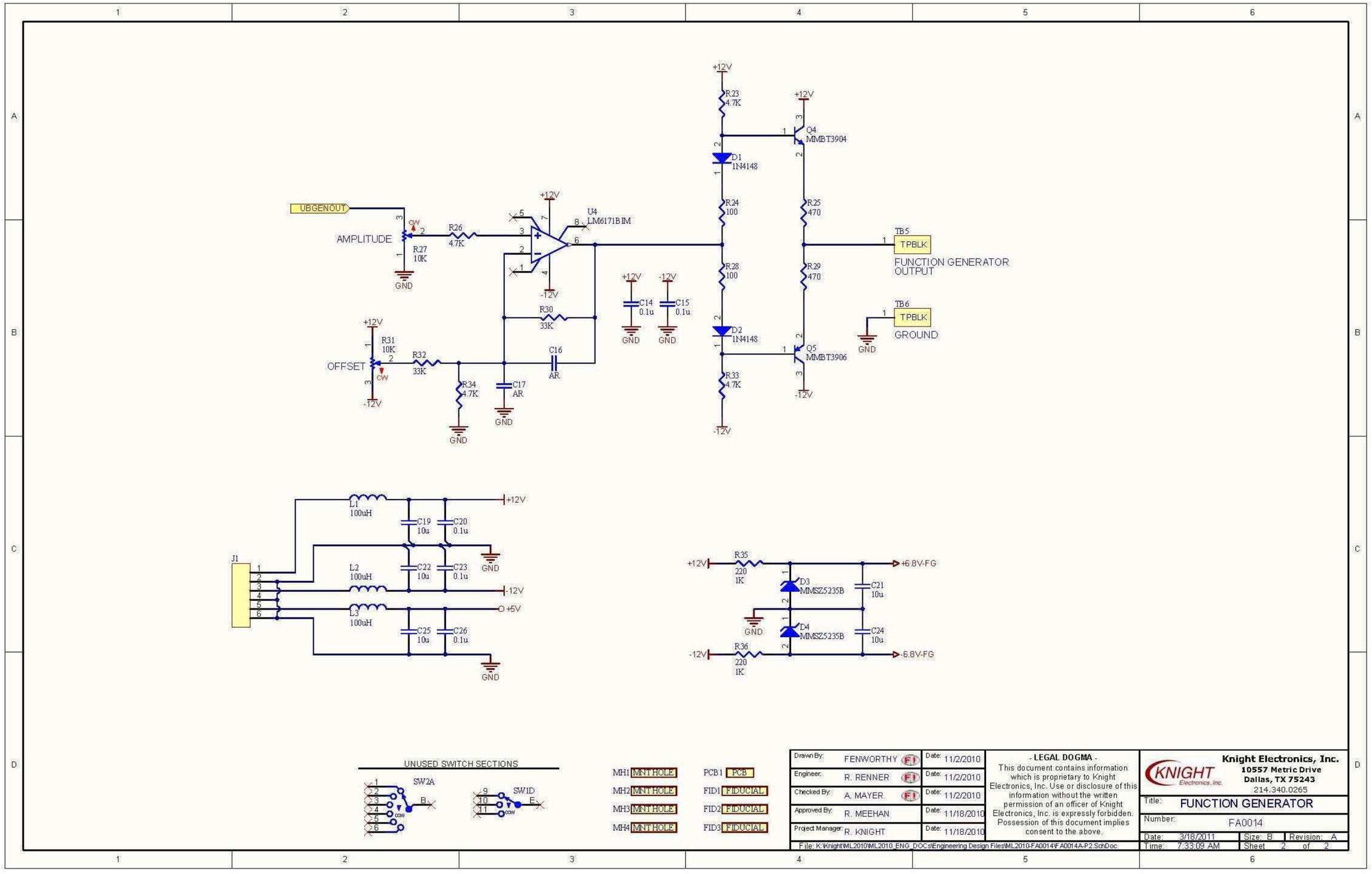


Figure 71. FA0014 ML2010 – FUNCTION GENERATOR PAGE 2 SCHEMATIC

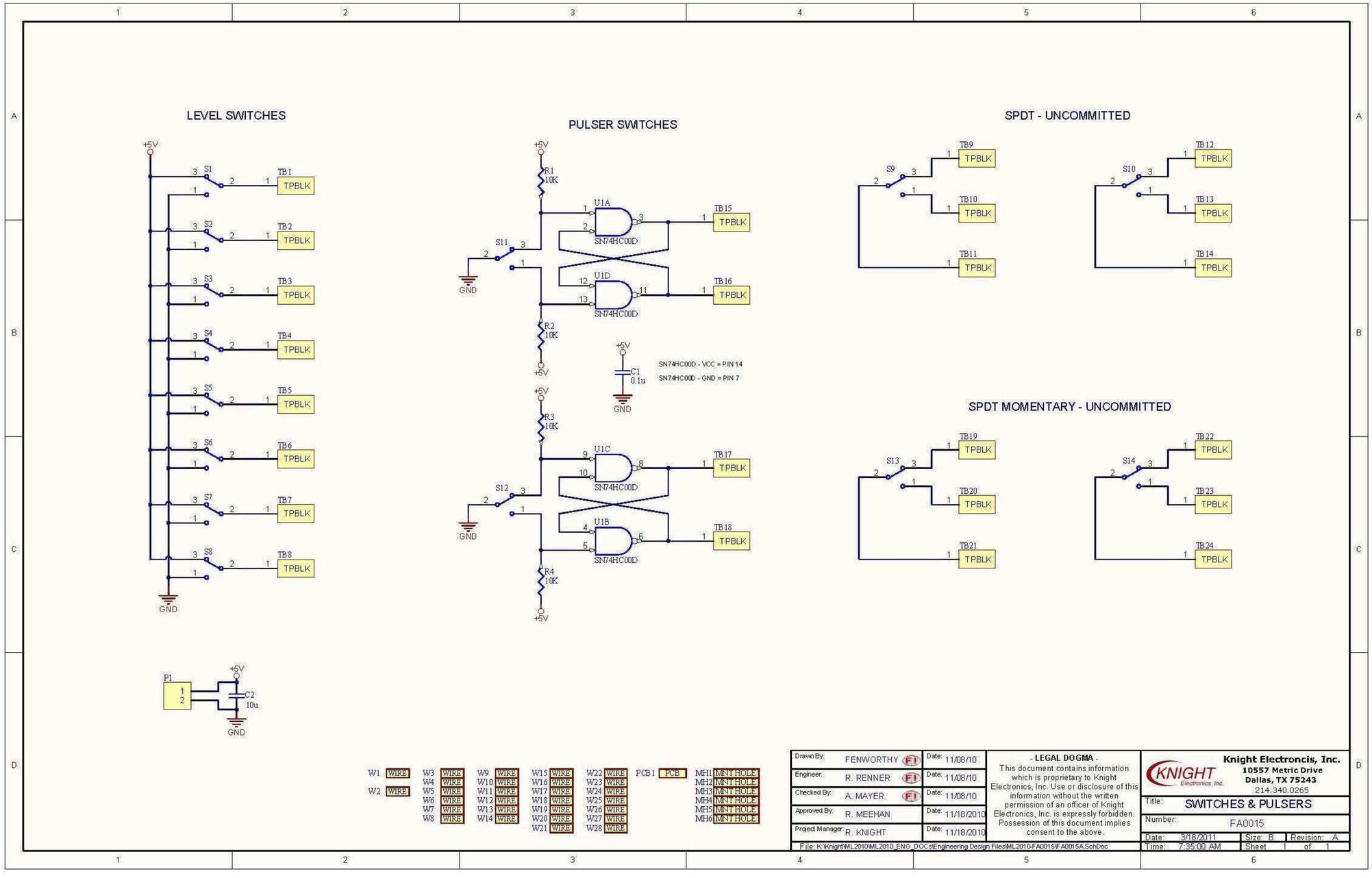


Figure 72. FA0015 ML2010 – SWITCHES & PULSERS SCHEMATIC

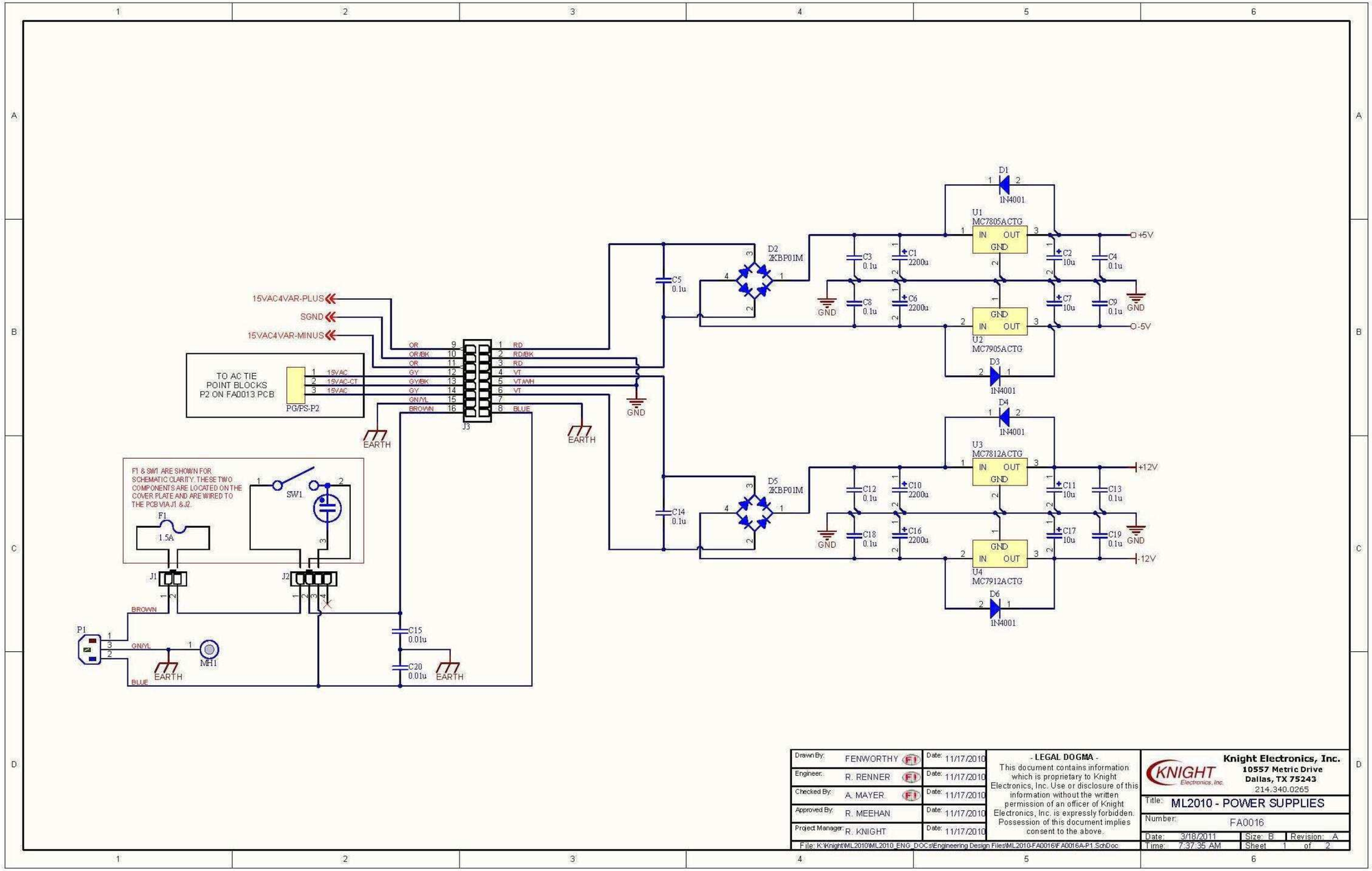
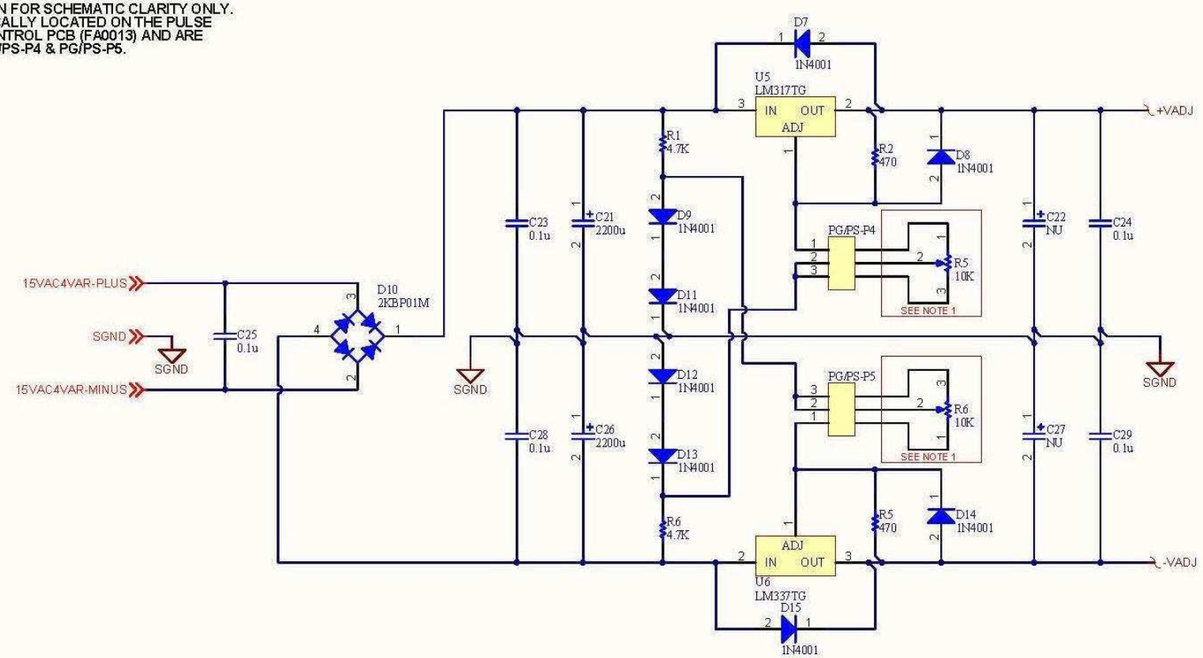
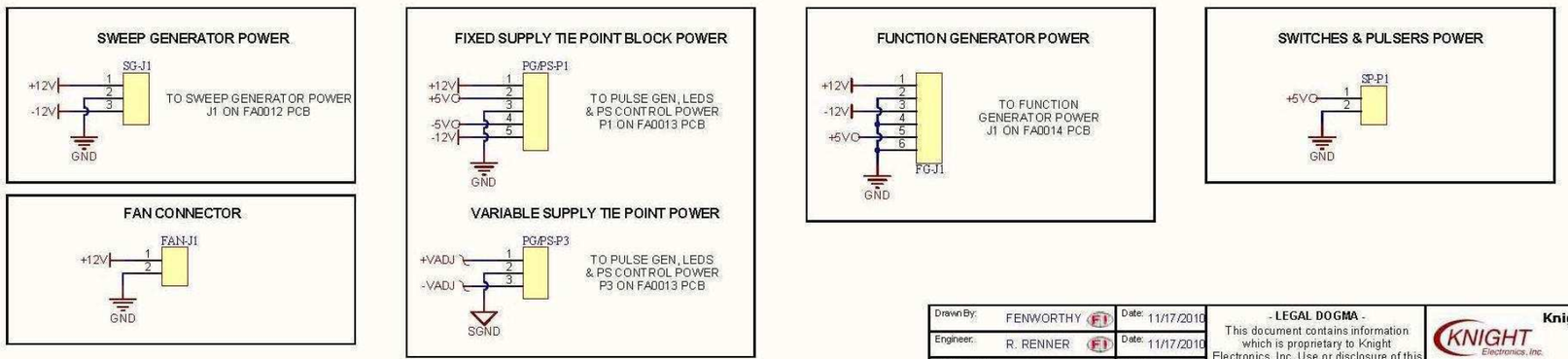


Figure 73. FA0016 ML2010 – POWER SUPPLY PAGE 1 SCHEMATIC

NOTES:

1. COMPONENT SHOWN FOR SCHEMATIC CLARITY ONLY. R5 & R6 ARE PHYSICALLY LOCATED ON THE PULSE GEN, LEDS & PS CONTROL PCB (FA0013) AND ARE CONNECTED VIA PG/PS-P4 & PG/PS-P5.





PCB1 PCB	MH2 MNT HOLE	MH5 MNT HOLE	HW1 HEATSINK	HW4 HEATSINK	HW7 #4 SCREW	HW10 #4 SCREW	HW13 #4 KEP NUT	HW16 #4 KEP NUT	
	MH3 MNT HOLE	MH6 MNT HOLE	HW2 HEATSINK	HW5 HEATSINK	HW8 #4 SCREW	HW11 #4 SCREW	HW14 #4 KEP NUT	HW17 #4 KEP NUT	
	MH4 MNT HOLE	MH7 MNT HOLE	HW3 HEATSINK	HW6 HEATSINK	HW9 #4 SCREW	HW12 #4 SCREW	HW15 #4 KEP NUT	HW18 #4 KEP NUT	

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Engineer: R. RENNER	Date: 11/17/2010	
Checked By: A. MAYER	Date: 11/17/2010	
Approved By: R. MEEHAN	Date: 11/17/2010	
Project Manager: R. KNIGHT	Date: 11/17/2010	

File: K:\Knight\ML2010\ML2010_ENG_DOCs\Engineering Design Files\ML2010-FA0016\FA0016A-P2.SchDoc

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Number: FA0016
Date: 3/18/2011 Size: B Revision: A
Time: 7:38:27 AM Sheet 2 of 2

Figure 74. FA0016 ML2010 – POWER SUPPLY PAGE 2 SCHEMATIC

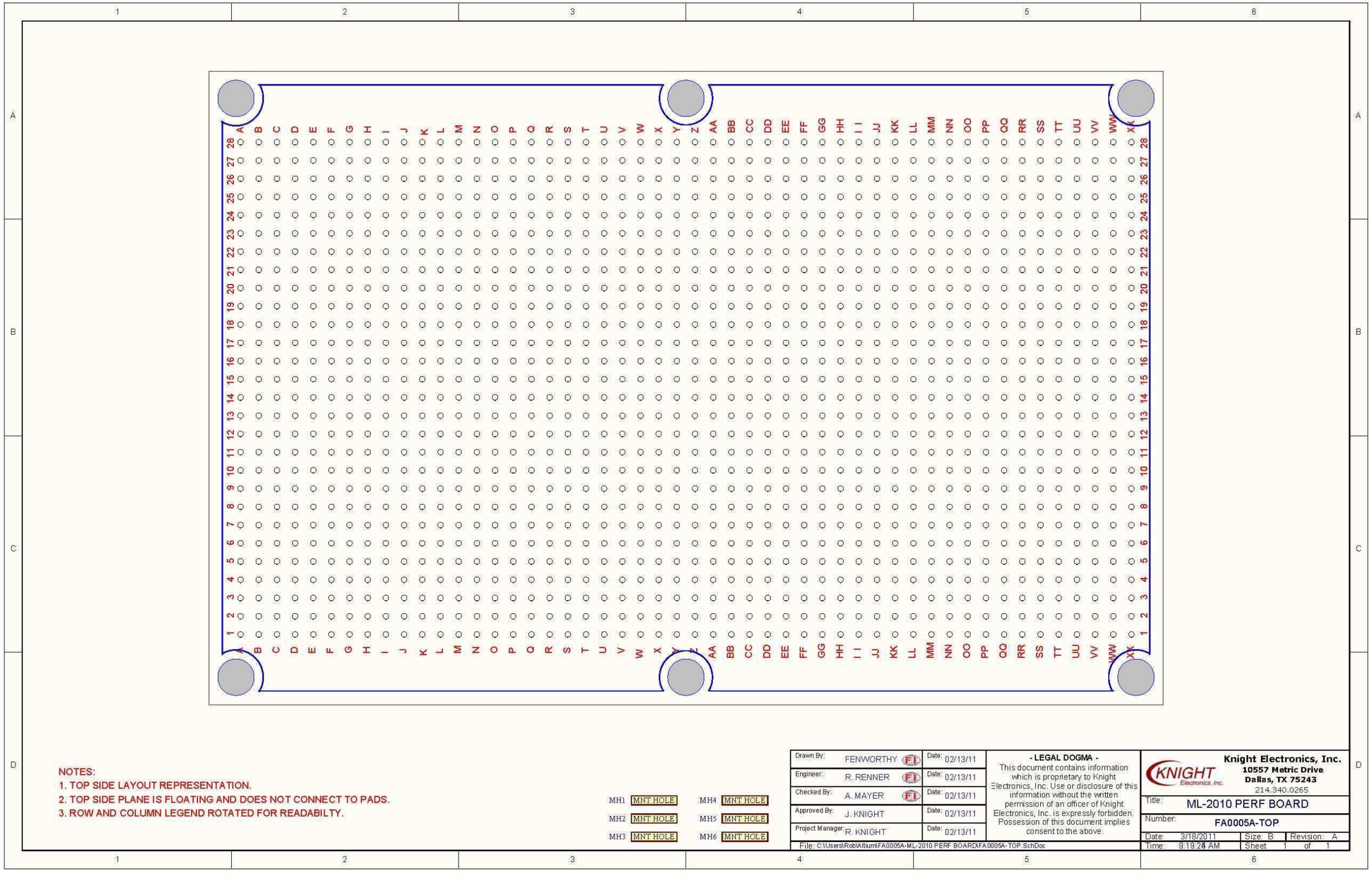

Figure 75. FA0005 ML2010 – PERF BOARD TOP TEMPLATE

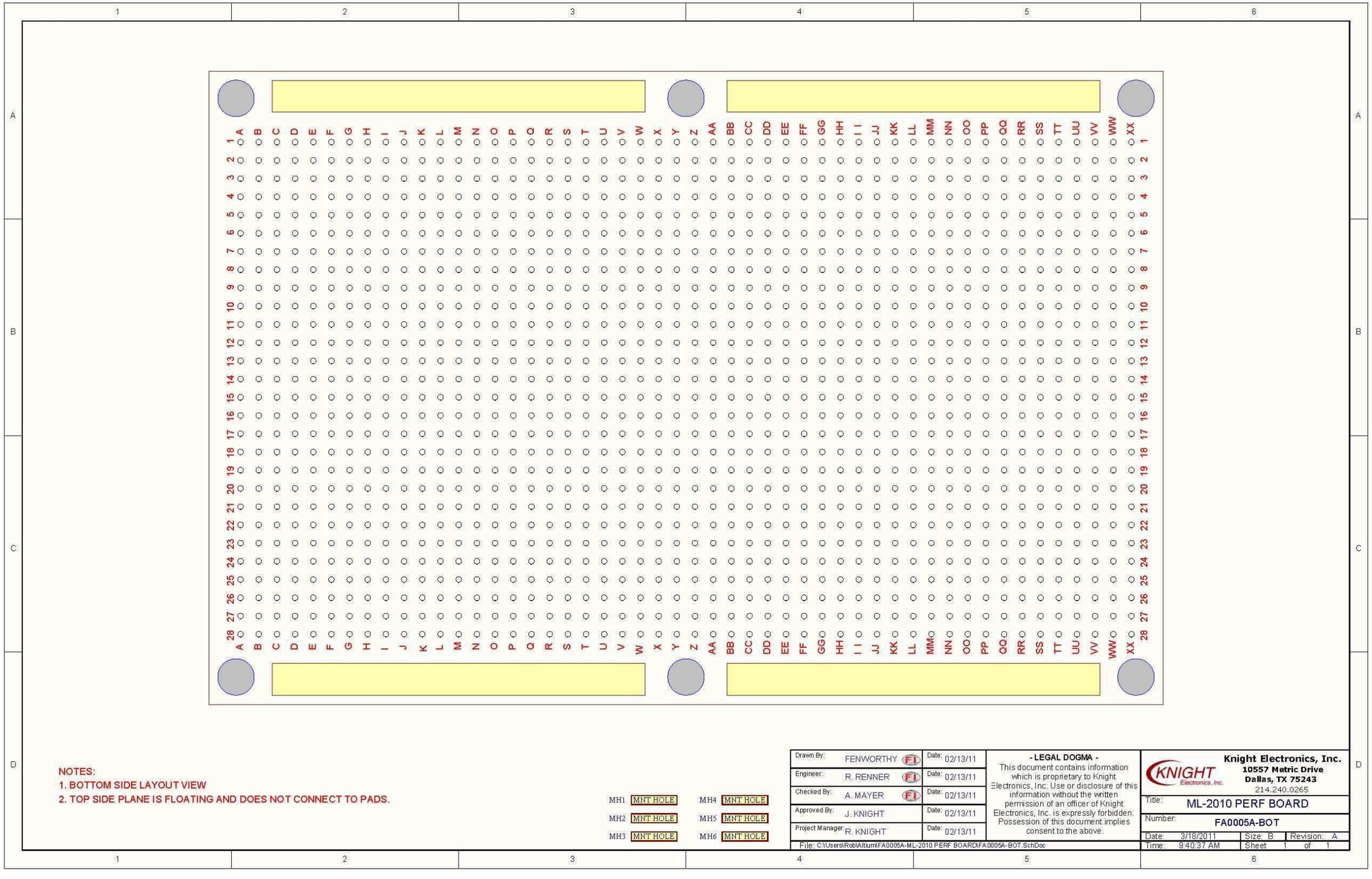

Figure 76. FA0005 ML2010 – PERF BOARD BOTTOM TEMPLATE