Keysight 16800 Series Portable Logic Analyzers

Service Guide

KEYSIGHT TECHNOLOGIES

Notices

Manual Part Number

16800-97014

Edition

Sixth edition, October 2014

Printed in Malaysia

Published by
Keysight Technologies
Plot No. CP-11, Sector- 8,
IMT Manesar, Gurgaon - 122051, India

Warranty

THE MATERIAL CONTAINED IN THIS DOCUMENT IS PROVIDED "AS IS," AND IS SUBJECT TO BEING CHANGED, WITHOUT NOTICE, IN FUTURE EDITIONS. FURTHER, TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW, KEYSIGHT DISCLAIMS ALL WARRANTIES, EITHER EXPRESS OR IMPLIED WITH REGARD TO THIS MANUAL AND ANY INFORMATION CONTAINED HEREIN, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. KEYSIGHT SHALL NOT BE LIABLE FOR ERRORS OR FOR INCIDENTAL OR CONSEQUENTIAL DAMAGES IN CONNECTION WITH THE FURNISHING, USE, OR PERFORMANCE OF THIS DOCUMENT OR ANY INFORMATION CONTAINED HEREIN. SHOULD KEYSIGHT AND THE USER HAVE A SEPARATE WRITTEN AGREEMENT WITH WARRANTY TERMS COVERING THE MATERIAL IN THIS DOCUMENT THAT CONFLICT WITH THESE TERMS, THE WARRANTY TERMS IN THE SEPARATE AGREEMENT WILL CONTROL.

Technology Licenses

The hardware and/or software described in this document are furnished under a license and may be used or copied only in accordance with the terms of such license.

Restricted Rights Legend

If software is for use in the performance of a U.S. Government prime contract or subcontract, Software is delivered and licensed as "Commercial computer software" as defined in DFAR 252.227-7014 (June 1995), or as a "commercial item" as defined in FAR 2.101(a) or as "Restricted computer software" as defined in FAR 52.227-19 (June 1987) or any equivalent agency regulation or contract clause. Use, duplication or disclosure of Software is subject to Keysight Technologies' standard commercial license terms, and non-DOD Departments and Agencies of the U.S. Government will receive no greater than Restricted Rights as defined in FAR 52.227-19(c)(1-2) (June 1987). U.S. Government users will receive no greater than Limited Rights as defined in FAR 52.227-14 (June 1987) or DFAR 252.227-7015 (b)(2) (November 1995), as applicable in any technical data.

Safety Notices

CAUTION

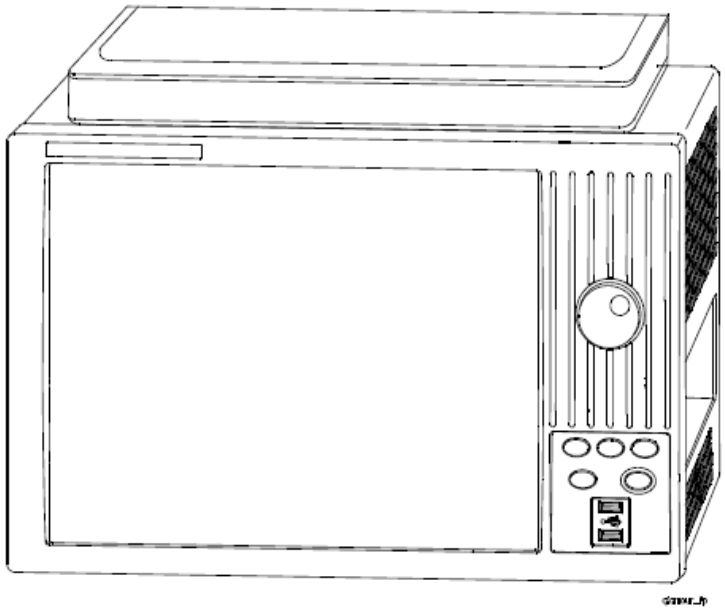
A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

The Keysight 16800 Series Logic Analyzers—At a Glance

The Keysight Technologies 16800 Series logic analyzers are standalone benchtop logic analyzers that range from 34 to 204 logic acquisition channels and 48 pattern generator channels, depending on the model.



Model Comparison

Table 1 Model comparisons

Keysight model number	16801A	16802A	16803A	16804A	16806A	16821A	16822A	16823A
Logic acquisition channels	34	68	102	136	204	34	68	102
Pattern generator channels	0	0	0	0	0	48	48	48

Features, Logic Acquisition

- 1 M to 32 M memory depth per channel (depending on memory option), software upgradeable.
- 250 MHz or 500 Mb/s maximum state data rate (depending on state speed option), software upgradeable. The 500 Mb/s maximum state data rate option is available on the 68-channel and above logic analyzer models.
- 1 GHz, 64 M deep timing analysis on half channels.
- *Eye finder* (automatic threshold and sample position setup) feature.
- 4 GHz timing zoom with 64 K memory depth.

Features, Mainframe

- Built-in 15 inch TFT color LCD display, 1,024 x 768 (XGA) resolution. Touch screen with 16800A Option 103.
- 250 GB hard disk drive (or external hard drive 16800A Option 109).

- 10/100 Base-T LAN port.
- USB 2.0 ports (six total, two on front, four on back).
- One PCI expansion slot.
- One PCI Express x1 expansion slot.
- Windows® XP Professional operating system. The 16800 Logic Analyzers with serial number MY50370000 or greater are shipped with Windows 7 operating system.
- *Keysight Logic Analyzer* application which takes the complexity out of making logic analyzer measurements. You can perform all operations directly from one window.

Features, Pattern Generator

- 24 channels at 300 MHz clock; 48 channels at 180 MHz clock.
- Memory Depth: 16,777,216 vectors in half-channel mode.
- Logic Level (data pods): TTL, 3-state TTL/3.3v, 3-state TTL/CMOS, ECL/PECL/LVPECL terminated, ECL unterminated, and differential ECL (without pod).
- Data Inputs: 3-bit pattern level sensing (clock pod).
- Clock Output: Synchronized to output data, delay of 7 ns in 14 steps (clock pod).
- Clock Input: DC to 300 MHz (clock pod).
- Internal Clock Period: Programmable from 1 MHz to 300 MHz in 1 MHz steps.
- External Clock Period: DC to 300 MHz.
- External Clock Duty Cycle: 1.3 ns minimum high time.

Supplied Accessories

- PS2 mouse.
- PS2 keyboard.
- Accessory pouch and power cord.

Optional Accessories:

- Probes.

Service Strategy

The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the 16800 Series logic analyzer.

This instrument can be returned to Keysight Technologies for all service work, including troubleshooting. Contact your nearest Keysight Technologies Sales Office for more details.

Contacting Keysight Technologies

To locate a sales or service office near you, go to www.keysight.com/find/contactus.

In this Service Guide

This book is the service guide for the 16800 Series logic analyzers and is divided into eight chapters.

Chapter 1, “General Information” contains information about the instrument including accessories, specifications and characteristics, and a list of the equipment required for servicing the instrument.

Chapter 2, “Preparing for Use” tells how to prepare the instrument for use.

Chapter 3, “Testing Performance” gives instructions on how to test the performance of the instrument.

Chapter 4, “Calibrating and Adjusting” contains calibration instructions for the instrument.

Chapter 5, “Troubleshooting” contains self-tests and flowcharts for troubleshooting the instrument.

Chapter 6, “Replacing Assemblies” tells how to replace the instrument and assemblies of the instrument, and how to return them to Keysight Technologies.

Chapter 7, “Replaceable Parts” lists replaceable parts, shows exploded views, and gives ordering information.

Chapter 8, “Theory of Operation” explains how the instrument works and what the self-tests are checking.

Revision History

Table 2 Revision History

Revision	Reason
16800-97014, November 2011 (this version)	Changes in replaceable part numbers and the recovery procedure for the 16800 logic analyzers that are shipped with Windows 7 installation (serial numbers MY50370000 or greater)
16800-97004, June 2007	Module interface board (MIB), chassis, and cover changes. These part changes appear in serial numbers above: MY46000901/SG46000901
16800-97003, August 2006	Changes to Testing Performance procedure.
16800-97002, July 2006	Changes to Testing Performance procedure.
16800-97001, July 2006	First edition.

Contents

5 Troubleshooting

6 Replacing Assemblies

8 Theory of Operation

1 General Information

This chapter contains information on accessories, specifications, characteristics, and recommended test equipment.

See the 16800 Series logic analyzer's online help for a full listing of all specifications and characteristics.

Accessories

Available

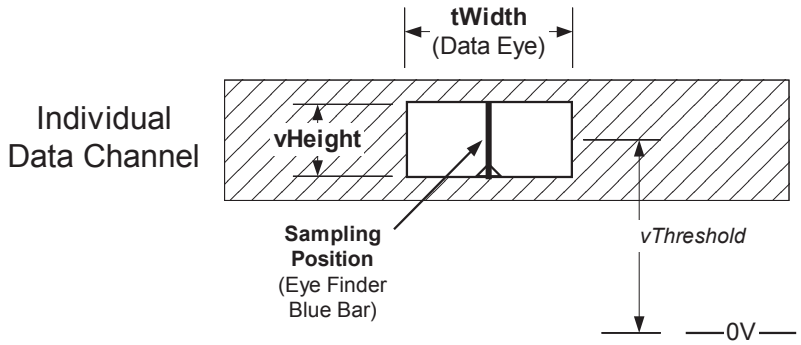
One or more of the following accessories, sold separately, are required to operate the 16800 Series logic analyzers.

Table 3 Logic Analyzer Accessories Available

Accessories	Keysight Part Number
Flying Lead Probe Set	E5383A
17-Channel Single-Ended Soft Touch Probe	E5396A
34-Channel Single-Ended Soft Touch Probe	E5394A
34-Channel Single-Ended Pro-series Soft Touch Probe	E5404A
34-Channel Single-Ended Probe (Samtec)	E5385A
34-Channel Single-Ended Probe (MICTOR)	E5346A
Single-Ended Low Voltage Probe (MICTOR)	E5339A
Single-Ended Probe, No Isolation Networks (MICTOR)	E5351A

Specifications

The specifications are the performance standards against which the product is tested.



Specifications			
Parameter	**250 Mb/s mode**	**500 Mb/s mode**	**Notes**
Minimum master to master clock time	4 ns	2 ns	500 Mb/s mode is available only when Option 500 is installed.
tWidth (minimum)	1.5 ns	1.5 ns	Specified at probe tip. Eye width as measured by *eye finder* may be less.

Specifications verified under the following test conditions:			
Parameter	**250 Mb/s mode**	**500 Mb/s mode**	**Notes**
Vh	1.3 V		600 mVp-p
Vl	0.7 V		
vThreshold	1 V		
rise/fall times	150-180 ps		
Probe	Keysight E5383A		Flying Lead Probe

Characteristics

The following characteristics are not specifications, but are typical characteristics for the 16800 Series logic analyzers.

Electrical

Power Requirements

16801A, 16802A, and 16803A: 115/230 Vac +/- 20%, 48-66Hz, 615 W Max.

16804A, 16806A, 16821A, 16822A, and 16823A: 115/230 Vac +/- 20%, 48-66Hz, 775 W Max.

The line voltage is auto-detected by the instrument.

CAT II (Line voltage in appliance and to wall outlet).

Pollution degree 2.

Trigger In

The Trigger In connector is 5V Max pk and DC, CAT I (line isolated).

Clock In

The Clock In connector is 5.5V Max pk and DC, CAT I (line isolated).

Probes

Maximum Input Voltage: ± 40 V, CAT I, CAT I = Category I, secondary power line isolated circuits.

Operating Environment (for indoor use only)

Table 4 Operating Environment Characteristics

Properties	Description
Temperature	All models: 0° to + 50° C (+32° to +122° F). Probes/cables: 0° to + 65° C (+32° to +149° F).
Humidity	Relative humidity 8% to 80% at 40° C (104° F). Avoid sudden, extreme temperature changes which could cause condensation on the circuit board.
Altitude	0 to 3,000 m (10,000 ft)
Vibration	Operating: random vibration 0-500 Hz, 10 minutes per axis, 0.3 g (rms).

Non-Operating Environment

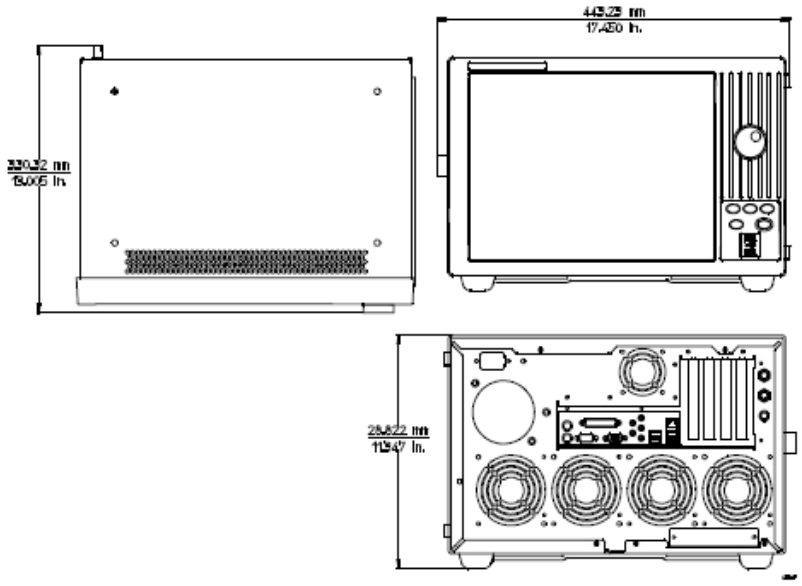
Store or ship the instrument in environments within the following limits:

Table 5 Non-Operating Environment Characteristics

Properties	Description
Temperature	Temperature -40°C to +75°C (-40°F to 167°F). Protect the system from temperature extremes which cause condensation on the instrument.
Humidity	Humidity up to 90% at 65° C (149°F).
Altitude	Altitude up to 3,000 meters (10,000 feet)).
Vibration	Non-operating: random vibration 0-500 Hz, 10 minutes per axis, 2.41g (rms); and swept sine resonant search, 0-500 Hz, 0.75g, 5-minute resonant dwell at 4 resonances per axis.

Dimensions

The following figure provides dimensions for the 16800 Series logic analyzer mainframes in centimeters and inches.



Weight

Table 6 16800 Series Logic Analyzer Weight

Model	Max Net	Max Shipping
16801A	12.9 kg (28.5 lbs)	19.7 kg (43.5 lbs)
16802A	13.2 kg (28.9 lbs)	19.9 kg (43.9 lbs)
16803A	13.7 kg (30.3 lbs)	20.5 kg (45.3 lbs)
16804A	14.2 kg (31.3 lbs)	21.0 kg (46.3 lbs)
16806A	14.6 kg (32.1 lbs)	21.4 kg (47.1 lbs)
16821A	14.2 kg (31.2 lbs)	20.9 kg (46.2 lbs)
16822A	14.2 kg (31.6 lbs)	21.1 kg (46.6 lbs)
16823A	14.5 kg (32.0 lbs)	21.3 kg (47.0 lbs)

Recommended Test Equipment

Table 7 Recommended Test Equipment

Equipment	Critical Specifications	Recommended Keysight Model/Part	Use†
Single-ended Flying Lead Probe Set (Qty 2)	no substitute	E5383A	P, T
Ground Leads (Qty 5)	no substitute	pkg of 5 (Included with E5383A Probe Set)	T
Pulse Generator	260 MHz,1 ns pulse width, two channels, ≤ 150 ps rise time	81134A Option 003 or equivalent	P, T
150 ps Transition Time Converter (Qty 4)	Required if pulse generator's rise time is less than 150 ps (Voffset=1V, ΔV=600 mV). Required for 81134A opt. 003	Keysight or HP 15435A	P
Oscilloscope	≥ 1.5 GHz bandwidth, ≥ 8 GSa/s sampling rate	54845A or 54845B	P
SMA/Flying Lead Test connectors	no substitute	See "To Assemble the SMA/Flying Lead Test Connectors" on page 28	P
2 x 9 Test connectors	no substitute	See "To assemble the 2 x 9 test connectors" on page 92	P
SMA Coax Cable (Qty 2)	≥ 18 GHz bandwidth	8120-4948	P

†P = Performance Tests, T = Troubleshooting

2 Preparing for Use

To inspect the logic analyzer

1 Inspect the shipping container for damage.

If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

WARNING **Hazardous voltages exist in this instrument. To avoid electrical shock, do not apply power to a damaged instrument.**

2 Check the supplied accessories.

Accessories supplied with the logic analyzer are listed on page 4.

3 Inspect the product for physical damage.

Check the logic analyzer and the supplied accessories for obvious physical or mechanical defects. If you find any defects, contact your nearest Keysight Technologies Sales Office. Arrangements for repair or replacement are made, at Keysight Technologies' option, without waiting for a claim settlement. Contact information is located on page 4.

To apply power

1 Connect the supplied power cord to the instrument and to the power source.

This instrument autodetects the line voltage from 115 VAC to 230 VAC. It is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the model ordered and the country of destination. Refer to "Power Cables and Plug Configurations" on page 139 more information on power cables.

2 Turn on the power switch located on the front panel.

For first-time power up considerations and setup steps, refer to the *Installation Guide* that came with your instrument. To get the most up-to-date installation guide:

- Go to www.keysight.com.
- Search for 16800 Series Logic Analyzers.
- Look under Technical Support and then Manuals and Guides.

To clean the instrument

If the instrument requires cleaning:

1 Remove power from the instrument.

2 Clean the external surfaces of the instrument with a soft cloth dampened with a mixture of mild detergent and water.

3 Make sure that the instrument is completely dry before reconnecting it to a power source.

To start the user interface

Start the *Keysight Logic Analyzer* application from the Start menu or using a shortcut. On the desktop, the Keysight Logic Analyzer icon looks like:

Refer to the *Keysight Logic Analyzer* application's on-line help for information on how to operate the user interface.

To test the logic analyzer

- If you require a test to verify the specifications, start at the beginning of Chapter 3, "Testing Performance".
- If you require a test to initially accept the operation, perform the self-tests in chapter 3.
- If the logic analyzer does not operate correctly, go to the beginning of Chapter 5, "Troubleshooting".

3 Testing Performance

To ensure the 16800 Series logic analyzer is operating correctly, you can perform:

- Power-up tests.
- Self-tests that are started from within the *Keysight Logic Analyzer* application. See "To run the self-tests" on page 82.
- Manual performance verification tests to verify that the logic acquisition cards are meeting their specifications.

  There are no specifications associated with the 16800 Series logic analyzer system mainframe or the pattern generator card, so there are no manual performance verification tests for them.

Directions for performing power-up tests and the logic acquisition card's manual performance verification tests (against the specifications listed on page 15) are given in this chapter.

The logic analyzer is considered performance-verified if the power-up tests, the self-tests, and the manual performance tests have passed. The procedures in this chapter indicate what constitutes a "Pass" status for each of the tests.

To perform the power-up tests

The logic analyzer automatically performs power-up tests when you apply power to the instrument. Any errors are reported in the boot dialogue. Serious errors will interrupt the boot process.

The power-up tests are designed to complement the instrument on-line Self-Tests. Tests that are performed during powerup are not repeated in the Self-Tests.

A keyboard and mouse must be connected to the logic analyzer to observe the results of the power-up tests.

1 Exit all logic analysis sessions.

2 Press the power switch for about 1 second and release, wait for the unit to power off.

3 After a few seconds, turn the power switch back on. Observe the boot dialogue for the following:

- Ensure all of the installed memory is recognized.
- Any error messages.
- Interrupt of the boot process with or without error message.

A complete transcript of the boot dialogue is in chapter 8, "Theory of Operation."

4 During initialization, check for any failures.

If an error or an interrupt occurs, refer to Chapter 5, “Troubleshooting”.

Logic Analyzer Test Strategy

Only specified parameters are tested. Specifications are listed on page 15. The test conditions defined in this procedure ensure that the specified parameter is as good as or better than specification. No attempt is made to determine performance which is better than specification. Not all channels of the logic analyzer will be tested; rather a sample of channels is tested. The calibration laboratory may choose to elaborate on these tests and test all channels at their discretion.

To perform a complete test on a logic acquisition module, start at the beginning of the chapter and follow each procedure.

Test Interval

Test the performance of the module against specifications at two-year intervals.

Test Record Description

For recording the results of each procedure, see "Performance Test Record" on page 62.

Test Equipment

Each procedure lists the recommended test equipment. You can use equipment that satisfies the specifications given. However, the procedures are based on using the recommended model or part number.

Instrument Warm-Up

Before testing the performance of the module, warm-up the logic analyzer and the test equipment for 30 minutes.

To Assemble the SMA/Flying Lead Test Connectors

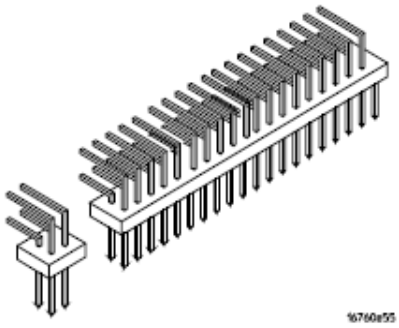
The SMA/Flying Lead test connectors provide a high-bandwidth connection between the logic analyzer and the test equipment. The following procedure explains how to fabricate the required test connectors.

Table 8 Materials Required for SMA/Flying Lead Test Connectors

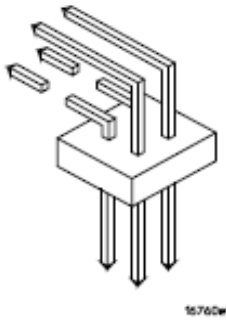
Material	Critical Specification	Recommended Model/Part
SMA Board Mount Connector (Qty 6)		Johnson 142-0701-801 (see www.johnsoncomponents.com)
Pin Strip Header (Qty 1, which will be separated)	.100" X .100" Pin Strip Header, right angle, pin length .230", two rows,.120" solder tails, 2 X 40 contacts	3M 2380-5121TN or similar 2- row with 0.1” pin spacing
SMA 50 ohm terminators (Qty 1)	Minimum bandwidth 2 GHz	Johnson 142-0801-866 50 ohm Dummy Load Plug
SMA m-m adapter (Qty 3)		Johnson 142-0901-811 SMA Plug to Plug or similar

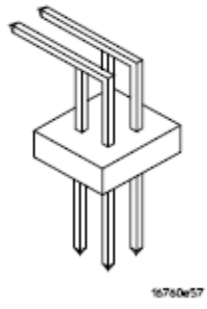
1 Prepare the pin strip header:

a Cut or cleanly break a 2 x 2 section from the pin strip.

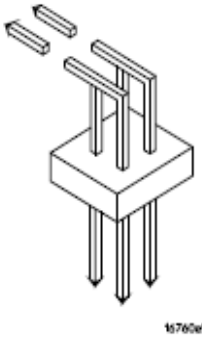


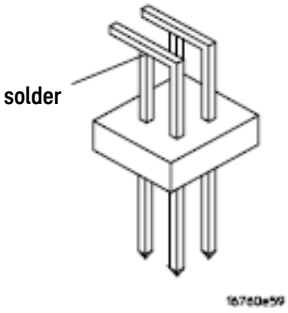
b Trim about 1.5 mm from the pin strip inner leads and straighten them so that they touch the outer leads.





c Trim about 2.5 mm from the outer leads.



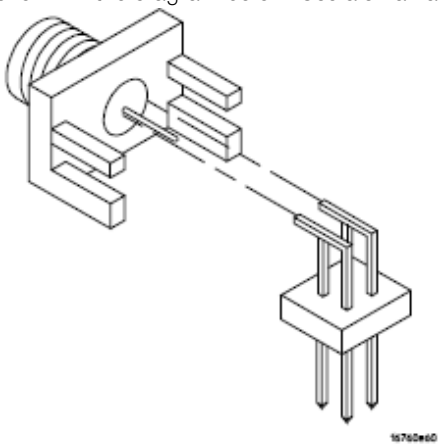


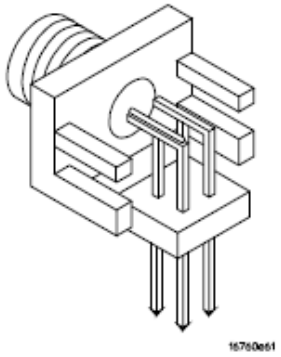
d Using a very small amount of solder, tack each inner lead to each outer lead at the point where they are touching.

2 Solder the pin strip to the SMA board mount connector:

a Solder the leads on the left side of the pin strip to the center conductor of the SMA connector as shown in the diagram below.

b Solder the leads on the right side of the pin strip to the inside of the SMA connector's frame as shown in the diagram below. Use a small amount of solder.

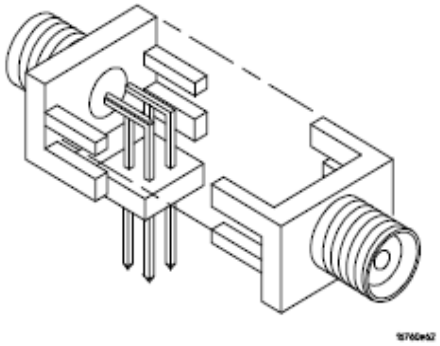


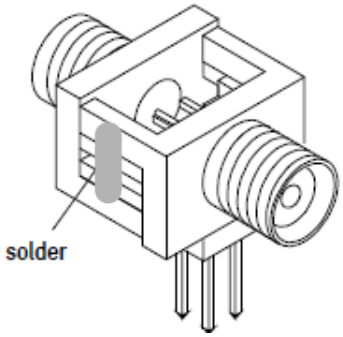


3 Attach the second SMA board mount connector:

a Re-heat the solder connection made in the previous step, and attach the second SMA connector, as shown in the diagram below. Note that the second SMA connector is upside-down, compared to the first. Add a little solder to make a good connection.

b Solder the center conductor of the second SMA connector to the center conductor of the first SMA connector and the leads on the left side of the pin strip.





c Rotate the assembly 180 degrees and solder the two SMA board mount connector frames together.

4 Check your work:

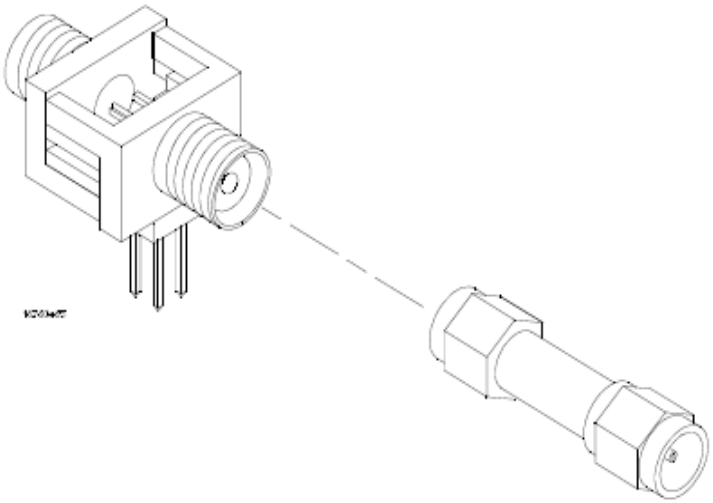
a Ensure that the following four points have continuity between them: The two pins on the left side of the pin strip, and the center conductors of each SMA connector.

b Ensure that there is continuity between each of the two pins on the right side of the pin strip, and the SMA connector frames.

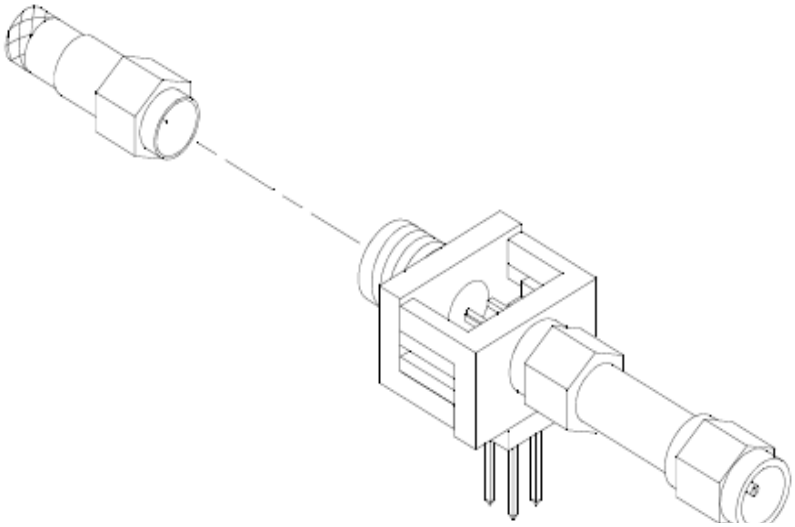
c Ensure that there is NO continuity between the SMA connector center conductor and the SMA connector frame (ground).

5 Finish creating the test connectors:

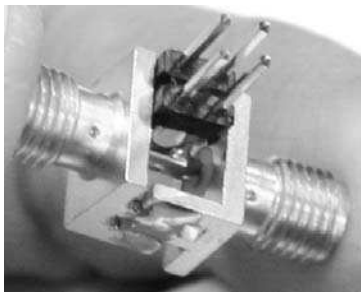
a Attach an SMA m-m adapter to one end of each of the three SMA/Flying Lead test connectors.



b Attach a 50 ohm terminator to the other end of just one of the SMA/Flying Lead test connectors.



c The finished test connector is shown in the pictures below.



To Test the Minimum Master to Master Clock Time and Minimum Eye Width

The specifications for the logic analyzer define a minimum master to master clock time and a minimum data eye width at which data can be acquired. This test verifies that the logic analyzer meets these specifications.

Eye finder is used to adjust the sampling position on every tested channel. *Eye finder* must be used to achieve minimum data eye width performance.

First, the logic analyzer will be tested in the 250 Mb/s state mode. Then it will be tested in the 500 Mb/s state mode.

In the 250 Mb/s state mode each pod will be tested with its respective clock.

The 500 Mb/s mode has only one clock (Clk1). All tests in the 500 Mb/s mode will use clock Clk1.

A sample of four channels on each pod will be tested, one pod at a time, in both 250 Mb/s state mode and 500 Mb/s state mode.

The logic analyzer will be configured to acquire data on both edges of the clock, so the test frequency is set to half of the acquisition speed.

Equipment Required

The following equipment is required for the performance test procedure.

Table 9 Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Pulse Generator	≥ 260 MHz, two channels, differential outputs, 150-180 ps rise/fall time (if faster, use transition time converters)	Keysight or HP 81134A option 003
150 ps Transition Time Converter (Qty 3)	Required if pulse generator's rise time is less than 150 ps. (Pulse generator conditions: Voffset=1V, ΔV=500 mV.) Required for 81134A opt. 003.	Keysight or HP 15435A
Oscilloscope	bandwidth ≥ 1.5 GHz, sampling rate ≥ 8 GSa/s	Keysight or HP 54845A/B or similar
SMA Coax Cable (Qty 2)	>18 GHz bandwidth	Keysight or HP 8120-4948
Flying Lead Probe Set with 5 ground leads (Qty 2)	no substitute	Keysight or HP E5383A
Male BNC to Female SMA adapters (Qty 2)		Cambridge Products CP-AD507 (see www.cambridgeproducts.com)
SMA/Flying Lead test connectors, (f) SMA to (f) SMA to Flying Lead Probe (Qty 3)	no substitute	See "To Assemble the SMA/Flying Lead Test Connectors" on page 28

Prepare the Logic Analyzer for Testing

1 Record the logic analyzer's model and serial number in the Performance Test Record (see page 62). Record your work order number (if applicable) and today's date.

2 Record the test equipment information in the "Test Equipment Used" section of the Performance Test Record.

3 Turn on the logic analyzer.

   a Connect the keyboard to the rear panel of the logic analysis mainframe.

   b Connect the mouse to the rear panel of the mainframe.

   c Plug in the power cord to the power connector on the rear panel of the mainframe.

   d Turn on the main power switch on the mainframe front panel.

   While the logic analyzer is booting, observe the boot dialog for the following:

   - Ensure all of the installed memory is recognized.
   - Any error messages.
   - Interrupt of the boot process with or without error message.

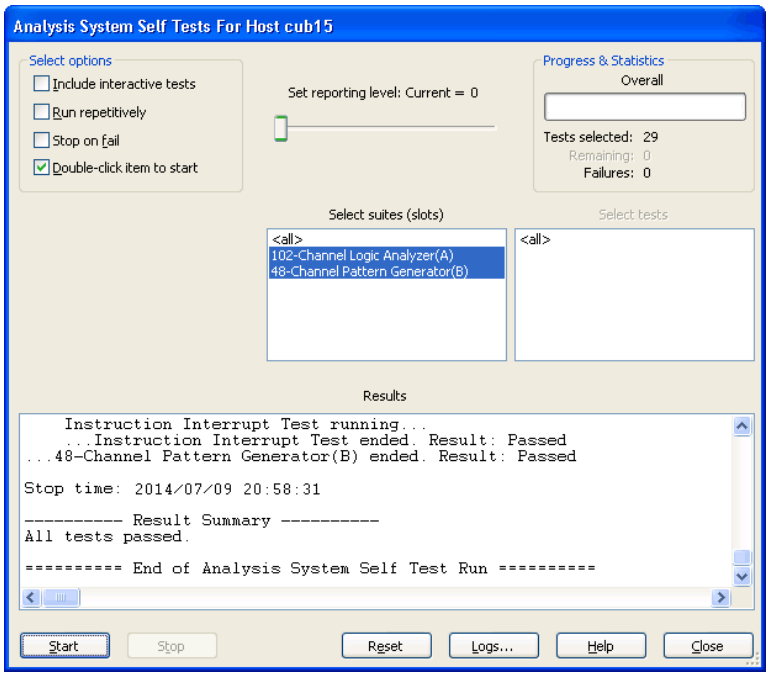
4 During initialization, check for any failures.

   If an error or an interrupt occurs, refer to Chapter 5, "Troubleshooting," starting on page 67.

Perform System Self-Tests

Perform a self-test on the logic analyzer:

1 When the logic analyzer has finished booting, the Waveform window appears. Select **Help→Self-Test...** from the main menu. The Analysis System Self Tests dialog appears.



2 In the Select Suite(s) list, select <all>. This will cause <all> to be selected in the Select Test(s) list.

3 Select **Start**. This will perform a complete system self-test.

The progress of the self tests is displayed in the Progress & Statistics area of the dialog.

4 When the self-tests are complete, check the Results area to ensure that the Result Summary says that all tests passed. If all tests did not pass, refer to Chapter 5, “Troubleshooting,” starting on page 67.

5 Select the **Close** button to close the Analysis System Self Tests dialog.

6 If all module self-tests pass, then record “PASS” in the “Logic Analyzer Self-Tests” section of the Performance Test Record (page 62).

Set Up the Test Equipment

1 Turn on the required test equipment. Let all of the test equipment and the logic analyzer warm up for 30 minutes before beginning any test.

2 Set up the pulse generator according to the following table.

a Set the frequency of the pulse generator. In this test procedure, the logic analyzer uses both edges of the clock to acquire data. The test frequency is half the test clock rate because data is acquired on both the rising edge and the falling edge of the clock. Set the frequency to 125 MHz plus the frequency uncertainty of the pulse generator, plus a test margin of 1%.

For example, if you are using an 81134A pulse generator, the frequency accuracy is ±1% of setting. Use a test margin of 1%. Set the frequency to 125 MHz plus 2% (127.5 MHz).

b Set the rest of the pulse generator parameters to the values shown in the following table.

Table 10 Pulse Generator Setup

Timebase	Pulse Channel 2	Trigger	Pulse Channel 1
Mode: Int	Mode: Pulse ÷ 1	Disable (LED on)	Mode: Square
Freq: 125 MHz plus frequency uncertainty of pulse generator plus 1% test margin.	Delay: (not available in pulse mode)		Delay: 0 ps
	Width: Initially set to 1.5 ns. Change later (on page 42).		Width: (not available in square mode)
	Ampl: 0.6 V		Ampl: 0.6 V
	Offs: 1.0 V		Offs: 1.0 V
	Output: Enable (LED off)		Output: Enable (LED off)
	Comp: Normal (LED off)		Comp: Normal (LED off)
	Limit: Off (LED off)		Limit: Off (LED off)
	$\overline{\text{Output}}$: Enable (LED off)		$\overline{\text{Output}}$: Enable (LED off)

3 Set up the oscilloscope.

a Set up the oscilloscope according to the following tables.

Table 11 Oscilloscope Setup

Setup: Channel 1	Setup: Ch. 1 Probe	Setup: Channel 2	Setup: Ch. 2 Probe
On	Attenuation: 1.00:1	On	Attenuation: 1.00:1
Scale: 100 mV/div	Units: Volts	Scale: 100 mV/div	Units: Volts
Offset: 1 V	Attenuation Units: Ratio	Offset: 1 V	Attenuation Units: Ratio
Coupling: DC	External Gain: (n/a)	Coupling: DC	External Gain: (n/a)
Input: 50 ohm	Skew: (Set later. See page 41)	Input: 50 ohm	Skew: 0.0 seconds
	External Offset: (n/a)		External Offset: (n/a)

Setup: Channel 3	Setup: Channel 4
Off	Off

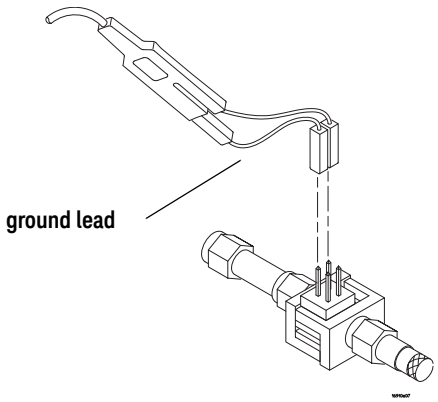
Setup: Horizontal	Setup: Trigger	Setup: Acquisition	Setup: Display
Scale: 2 ns	Mode: Edge	Sampling Mode: Equiv. Time	Waveforms: Connect dots
Position: 725 ps	Source: Channel 1	Memory Depth: Automatic	Persistence: Minimum
Reference: Center	Level: 1.00 V	Averaging: Enabled	Grid: On (and set intensity)
Delayed: not selected	Edge: Rising Edge	# of Averages: 16	Backlight Saver: as preferred
	Sweep: Auto		

Measure: Markers
Mode: Manual placement
All else: (n/a)

Connect the Test Equipment

Connect the Logic Analyzer Pod to the 81134A Pulse Generator

1. Connect a Transition Time Converter (if required—see Table 7, "Recommended Test Equipment," on page 19) to the 81134A pulse generator's Channel 2 OUTPUT, Channel 2 OUTPUT, and Channel 1 OUTPUT.
2. Connect the SMA/Flying Lead test connector (see "To Assemble the SMA/Flying Lead Test Connectors" on page 28) *with* the 50 ohm terminator to the Transition Time Converter at the 81134A pulse generator Channel 1 OUTPUT. (If Transition Time Converters are not required, connect the SMA/Flying Lead test connector directly to the pulse generator output.)
3. Connect the two SMA/Flying Lead test connectors *without* 50 ohm terminators to the Transition Time Converters at the 81134A pulse generator Channel 2 OUTPUT and Channel 2 OUTPUT. (If Transition Time Converters are not required, connect the SMA/Flying Lead test connectors directly to the pulse generator outputs.)
4. Connect an E5383A Flying Lead Probe Set to Pod 1 of the logic analyzer.
5. Connect the E5383A Flying Lead Probe Set's CLK lead to the pin strip of the SMA/Flying Lead connector at the 81134A pulse generator's Channel 1 OUTPUT.



NOTE

For each Flying Lead Probe connection, be sure to use a black ground lead (five are supplied with the E5383A Flying Lead Probe Set) and orient the leads so that the ground leads are connected to the SMA/Flying Lead connector's ground pins!

If you don't have the ground leads, you can push the probe body's ground socket directly onto a ground pin on the SMA/Flying Lead test connector. However, this will bend and could break pins on the SMA/Flying Lead test connector because the probe body spacing is greater than the SMA/Flying Lead test connector pin spacing. It is better to use the black ground leads.

In any case, the probe ground must be connected for each channel.

6. Connect the E5383A Flying Lead Probe Set's bits 2 and 10 to the SMA/Flying Lead test connector's pin strip connector at the 81134A pulse generator's Channel 2 OUTPUT.
7. Connect the E5383A Flying Lead Probe Set's bits 6 and 14 to the SMA/Flying Lead test connector's pin strip connector at the 81134A pulse generator's Channel 2 OUTPUT.

Connect the 81134A Pulse Generator Output to the 54845A Oscilloscope

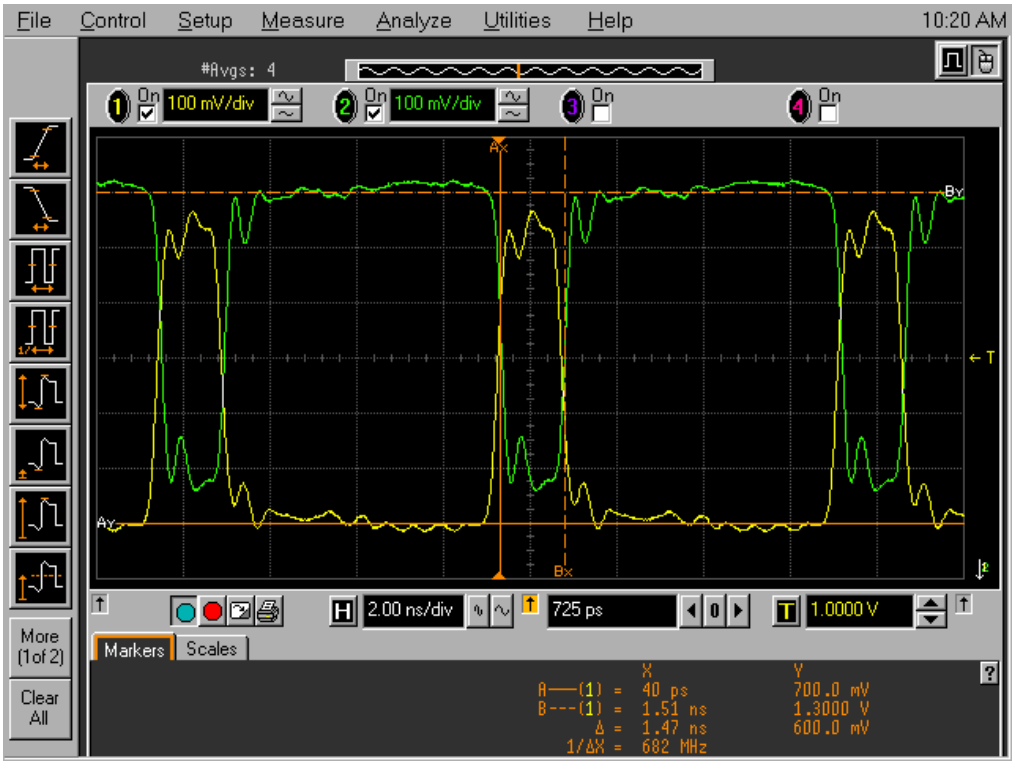
1 Attach Male BNC to Female SMA adapters to Channels 1 and 2 on the 54845A oscilloscope.
2 Attach one end of an SMA cable to the Male BNC to Female SMA adapter on Channel 1 of the oscilloscope.
3 Attach the other end of the SMA cable to the SMA/Flying Lead connector at the Channel 2 OUTPUT of the 81134A pulse generator.
4 Attach one end of the other SMA cable to the Male BNC to Female SMA adapter on Channel 2 of the oscilloscope.
5 Attach the other end of the SMA cable to the SMA/Flying Lead connector at the Channel 2 OUTPUT of the 81134A pulse generator.

Verify and adjust 81134A pulse generator DC offset

1 On the 54845A oscilloscope, select **Measure** from the menu bar at the top of the display.

2 Select **Markers...**

3 In the Markers Setup dialog set marker “Ay” to 0.7 V, and set marker “By” to 1.3 V.

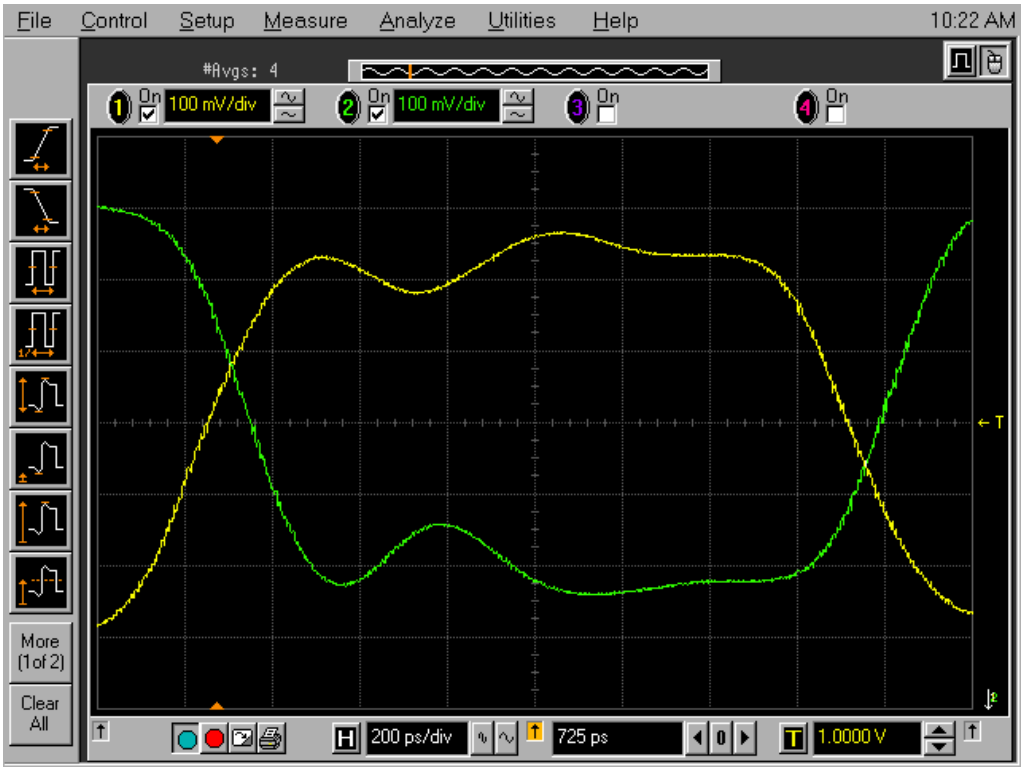


4 Observe the waveforms on the oscilloscope display. If they are not centered within the “Ay” and “By” markers, adjust the 81134A pulse generator’s Channel 2 OFFSET until the waveforms are centered as close as possible. (The resolution of the 81134A OFFSET setting is 10 mV.)

Deskew the oscilloscope

This procedure neutralizes any skew in the oscilloscope's waveform display.

1 On the 54845A oscilloscope, change the Horizontal scale to 200 ps/div. You can do this using the large knob in the Horizontal setup section of the front panel.

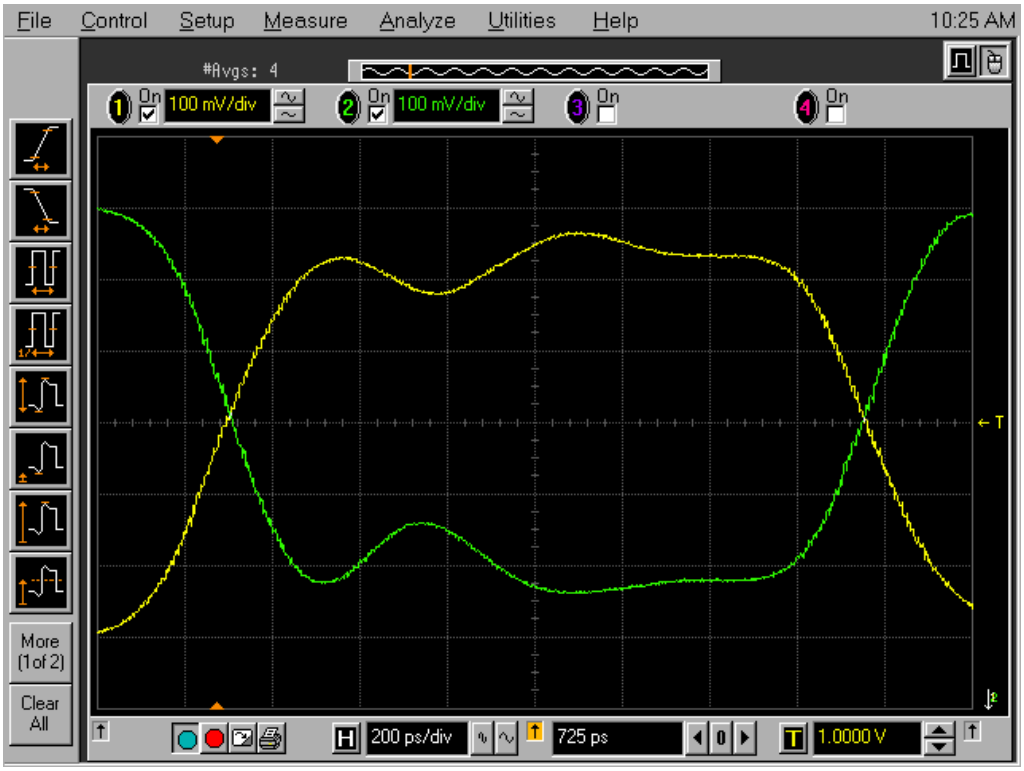


2 Select **Setup** from the menu bar at the top of the display.

3 Select **Channel 1**.

4 Select **Probes**.

5 Click **Skew </>** to deskew Channel 1 and Channel 2 signals so that both channels cross the 54845A horizontal center line at the same time, at both ends of the eye (both crossings of the horizontal center line). The horizontal center of the graticule line is at 1 volt because the vertical offset was set to 1 volt in the oscilloscope setup described on page 36.



6 Select **Close** in the Probe Setup dialog.

7 Select **Close** in the Channel Setup dialog.

Set the 81134A pulse width

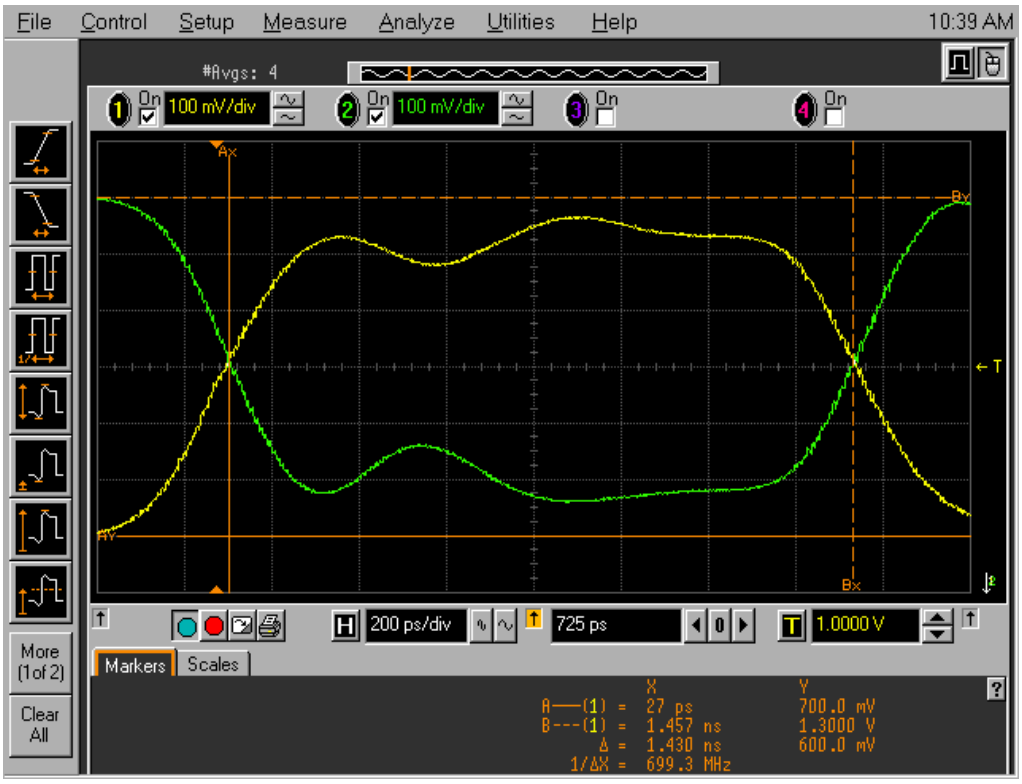
1 On the 81134A pulse generator, set the Channel 2 pulse width to 1.5 ns.

2 Observe the 54845A oscilloscope display. Change the Channel 2 pulse width of the 81134A pulse generator so that the pulse width measured at 1 volt on the oscilloscope is equal to 1.5 ns minus the measurement uncertainty and display resolution of the oscilloscope, further reduced by 35 ps for test margin.

   If you are using the 54845A/B oscilloscope, the measurement uncertainty is ±((0.007% * Δt) + (full scale/2x memory depth) + 30 ps) = ±30.10 ps. Add 5 ps for display resolution. Add 35 ps test margin.

   1.5 ns - 30.10 ps - 5 ps - 35 ps = 1.43 ns. Set the pulse width as measured on the 54845A/B oscilloscope to 1.43 ns.

NOTE On the oscilloscope move the Ax and Bx markers to the crossing points of the pulse and the horizontal center line. Read the pulse width at the bottom of the screen. It is displayed as "Δ=".

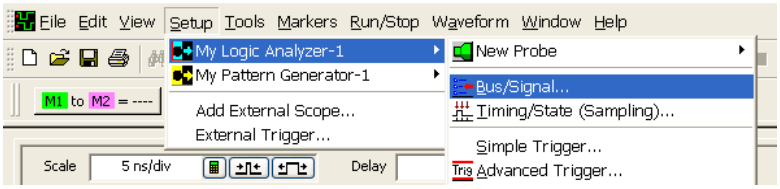


Configure the Logic Analyzer

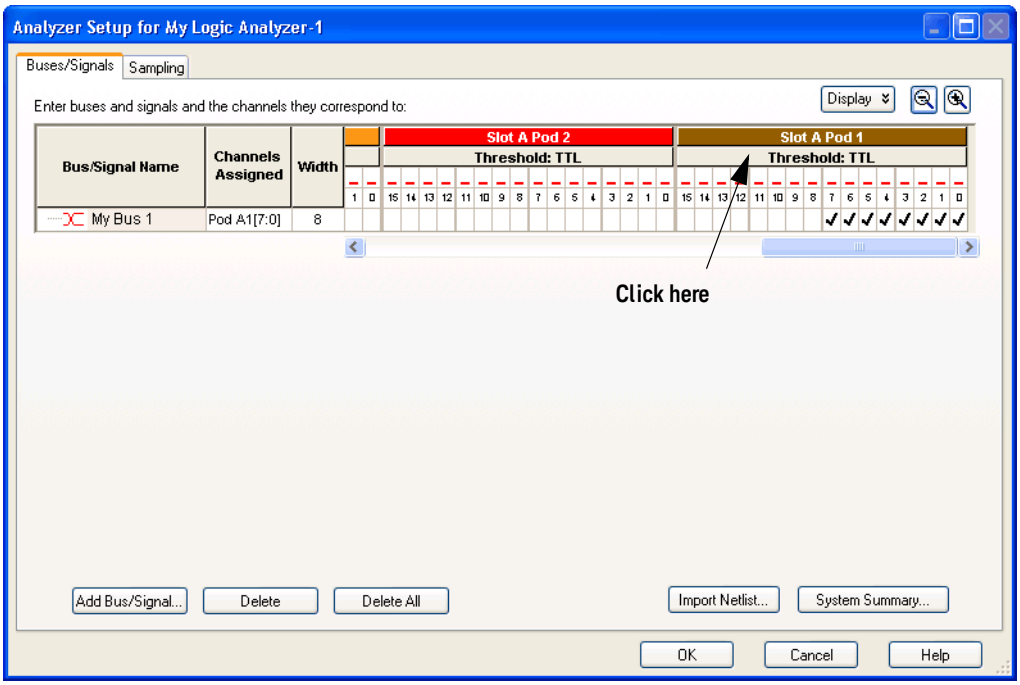
1 Exit the *Keysight Logic Analyzer* application (from the main menu, choose **File→Exit**) and then restart the application. This puts the logic analyzer into its initial state.

2 Specify the threshold voltage and assign channels to the bus name:

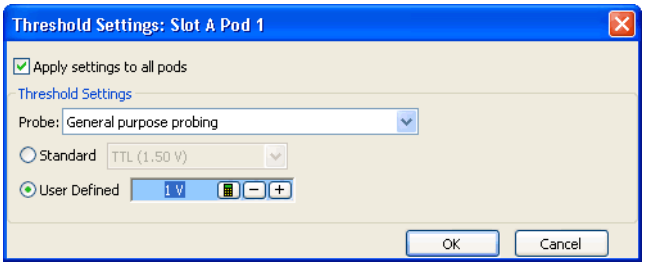
a From the main menu, select **Setup→Bus/Signal...** or **Setup→My Logic Analyzer-1→Bus/Signal...**.



b In the Analyzer Setup dialog, choose the **Threshold** button for Pod 1.

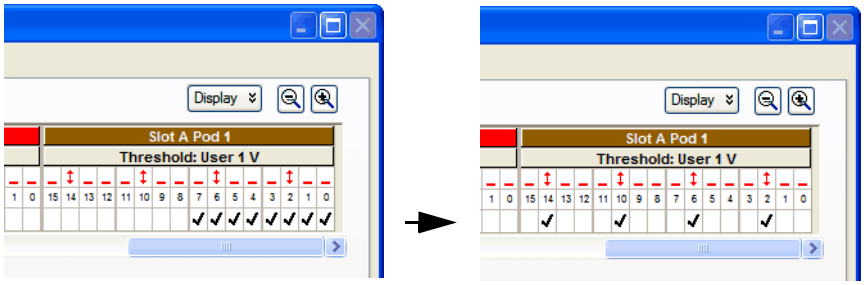


c In the Threshold Settings dialog, set the threshold value for Pod 1 of the logic analyzer to 1 V, and click **OK**.



d The activity indicators now show activity on the channels that are connected to the pulse

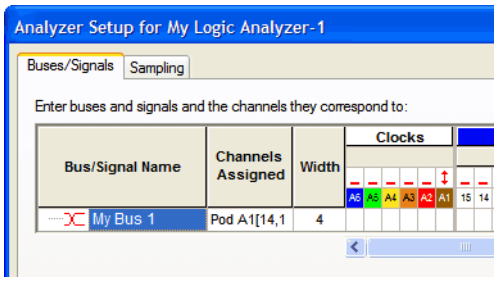
generator.



e Un-assign all channels. Hint: you can do this quickly by clicking on the left-most check mark and dragging to the right across all of the other check marks. If you have a logic analyzer with a touchscreen (Option 103), you can touch the touchscreen and drag across with your finger.

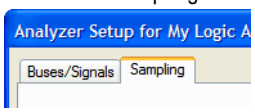
f Click (or touch) to select channels 2, 6, 10 and 14 as shown.

g Drag the scroll bar all the way to the left and ensure that the activity indicator shows activity on clock 1.

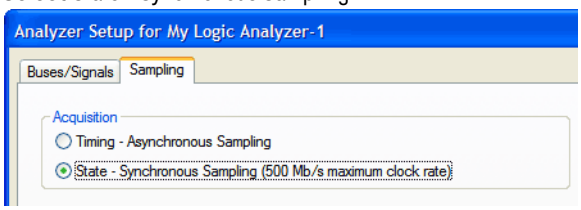


3 Set the sampling mode.

a Select the **Sampling** tab of the Analyzer Setup dialog.

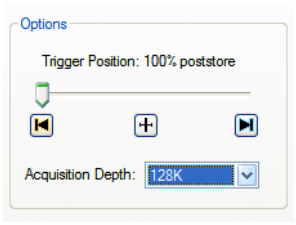


b Select **State - Synchronous Sampling**.

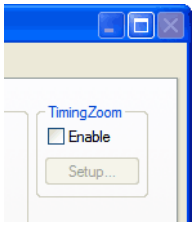


c Set the Trigger Position to **100% Poststore**.

d Set the Acquisition Depth to **128K**.



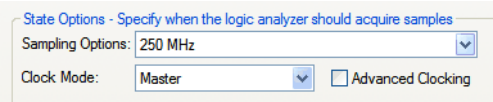
e Clear the Timing Zoom check box to turn Timing Zoom off.



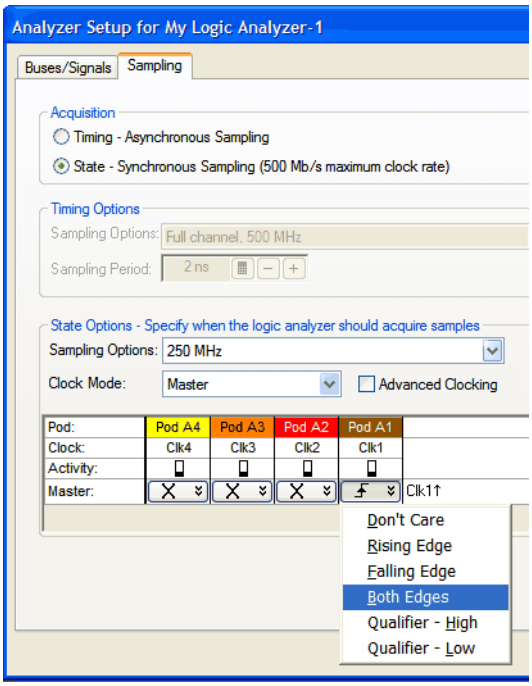
f Ensure that the sampling speed is set to **250 MHz** in the Sampling Options box.

NOTE If option 500 is not installed on the logic analyzer, then 250 MHz will be the only speed available.

g Ensure that the Clock Mode is set to **Master**.

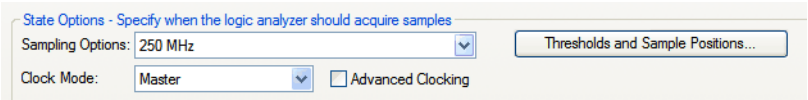


h Set the Pod 1 master clock to **Both Edges**.

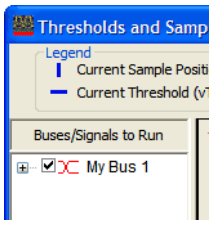


Adjust the sample positions using *eye finder*

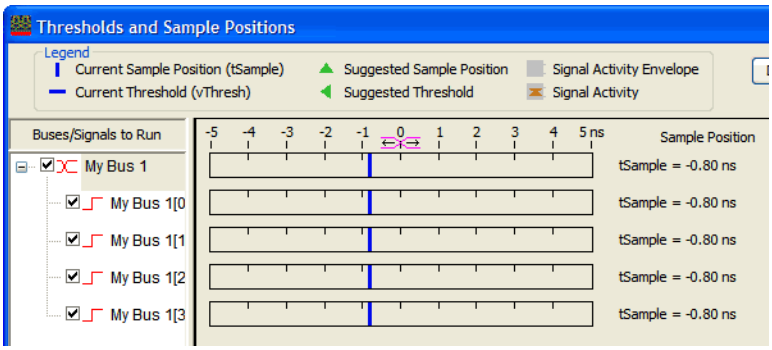
1 Click **Thresholds and Sample Positions...**.



2 In the “Buses/Signals” section of the Thresholds and Sample Positions dialog, ensure that the check box next to “My Bus 1” is checked.



3 Select the plus sign to expand bus “My Bus 1”.



Align the blue bars vertically

The first time you run *eye finder*, the blue bars will already be vertically aligned (as shown above). In this case you can skip to the next section (“Run eye finder”).

After running *eye finder*, the blue bars will not be vertically aligned because an independent sample position will be determined for each channel.

4 If the blue bars in the *eye finder* display are not vertically aligned, grab the right-most blue bar in the “My Bus 1” row with the mouse pointer and move it all the way to the left. Release the mouse button. This will vertically align all of the blue bars.

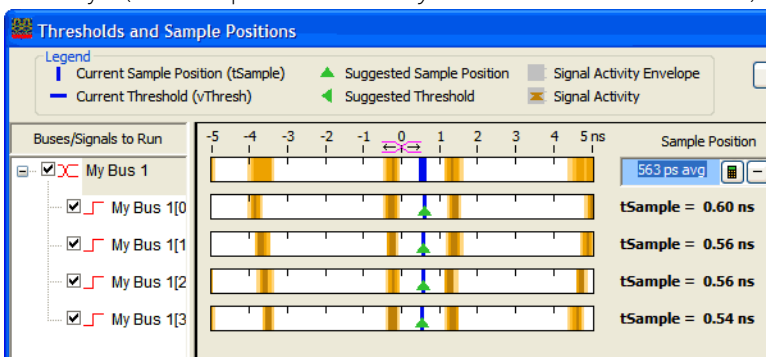
5 Using the mouse pointer, grab the top blue bar for “My Bus 1” and move it to the recommended starting position of 300 ps. All of the blue bars below will follow.

Run *eye finder*

6 Click the **Run** button in the Thresholds and Sample Positions dialog.

7 Ensure that an eye appears for each bit near the recommended starting position. Depending on your test setup, the eye position may vary. Any skew between channel 1 and channel 2 of your pulse generator will cause the eye position to shift to the left or right in the *eye finder* display. A shift of up to 0.5 ns should be considered normal.

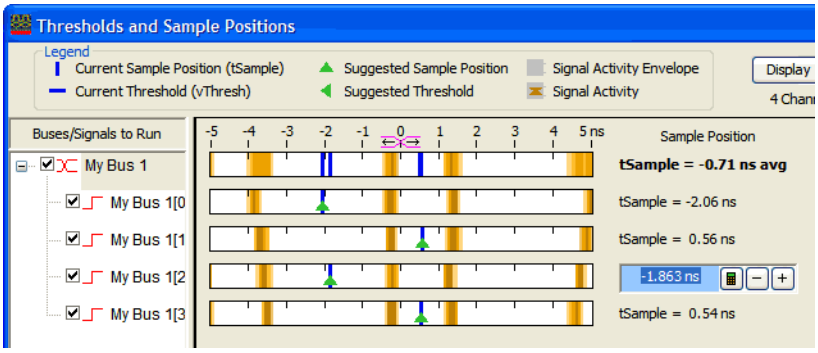
The important point is that your *eye finder* display should look similar to the picture below (although it may be shifted left or right), and *eye finder* must be able to place the blue bars in the narrow eye. (The example below shows *eye finder* in the 250 Mb/s mode.)



To re-align a stray channel

If the blue bar for a particular bit does not appear in its eye near the recommended starting position, then do the following steps to realign the sampling position of the stray channel.

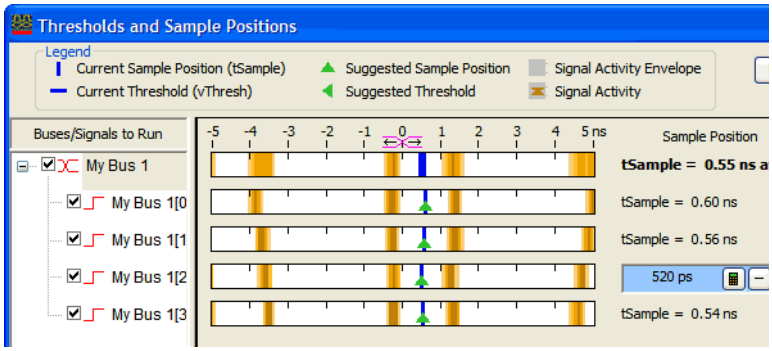
In the following example, the sampling position of two channels (My Bus 1[0] and My Bus 1[2]) must be realigned with the sampling position of the other channels.



8 Using the mouse, drag the sample position (blue bar) of the stray channel (channels “My Bus 1[0]” and “My Bus 1[2]” in the above example) so that it is in the same eye as the other channels. The Suggested Position from *eye finder* (green triangle) will also move to the new eye. Repeat the above step for all remaining stray channels.

9 Click the **Run** button in the Thresholds and Sample Positions dialog again.

The following example shows all sampling positions aligned and in the correct eye.



Test Pod 1 in 250 Mb/s Mode

The steps that follow include pass/fail criteria.

Determine PASS/FAIL (1 of 2 tests)

1 PASS/FAIL: If an eye exists near 300 ps for every bit, and *eye finder* places a blue bar in the narrow eye for each bit, then the logic analyzer passes this portion of the test. Record the result in the "**Test 1 of 2: eye finder locates an eye for each bit**" section of the Performance Test Record (page 62).

2 If an eye does not exist near 300 ps for every bit or *eye finder* cannot place the blue bar in the narrow eye, then the logic analyzer fails the test. Record the result in the "**Test 1 of 2: eye finder locates an eye for each bit**" section of the Performance Test Record (page 62).

Close the *eye finder* and Analyzer Setup dialogs

1 Click **OK** to close the Thresholds and Sample Positions dialog.

2 Click **OK** to close the Analyzer Setup dialog.

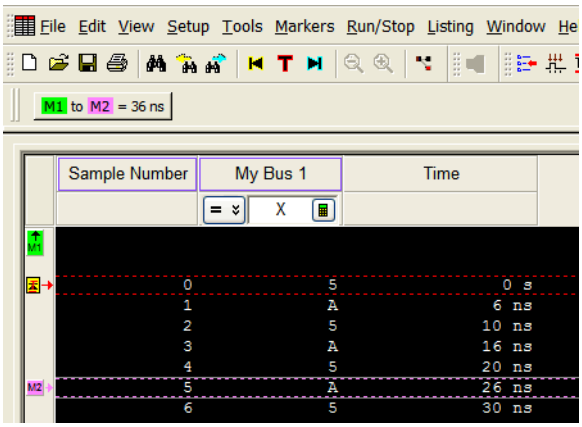
Configure the markers

Data must be acquired before the markers can be configured. Therefore, you will need to run the analyzer to acquire data.

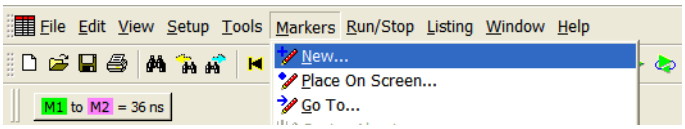
1 Switch to the Listing window by selecting the **Listing** tab at the bottom of the main window.

2 Click the Run icon .

3 Data appears in the Listing window upon completion of the run.



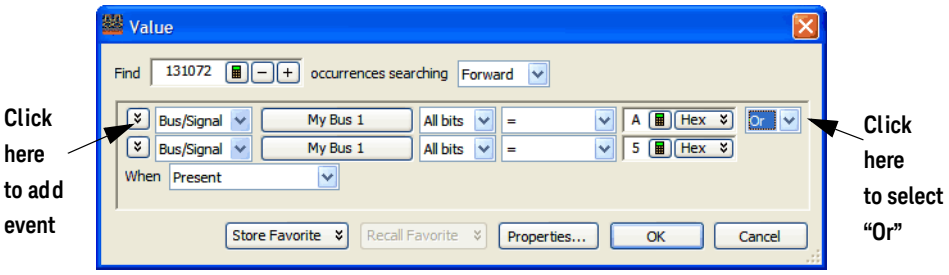
4 From the main menu choose **Markers→New...**.



a You can accept the default name for the new marker.

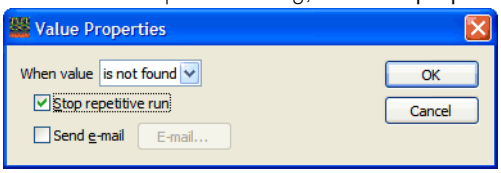
b Change the Position field to **Value**.

c Click **Occurs...**, and create the marker setup shown below.



5 In the Value dialog, click **Properties...**.

6 In the Value Properties dialog, select **Stop repetitive run** when value **is not found**.



7 Click **OK** to close the marker Value Properties dialog.

8 Click **OK** to close the marker Value dialog. The system will search the display for the occurrences specified.

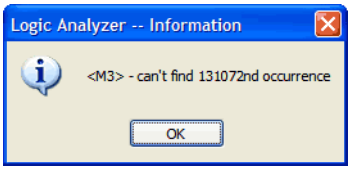
9 Click **OK** to close the New Marker dialog.

Determine PASS/FAIL (2 of 2 tests)

Pass/Fail Point: The Listing window is set up to search for the appropriate number of A's and 5's in the acquisition. If the logic analyzer does not detect the correct number of A's and 5's, an error dialog will appear.

1 Click the Run Repetitive icon . Let the logic analyzer run for about one minute. The analyzer will acquire data and the Listing window will continuously update.

If the "can't find occurrence" dialog appears, then the logic analyzer fails the test.



Check your test setup. If the failure is not the result of a problem with the test setup, record the failure in the "**Test 2 of 2: Correct number of occurrences detected**" section of the Performance Test Record (page 62).

NOTE **Be sure that the black ground lead is making good contact with the ground pin on the test connector.**

2 When about one minute has elapsed, click the **Stop** button to stop the acquisition.

If the "can't find occurrence" dialog does not appear, then the analyzer passes the test. Record "Pass" in the "**Test 2 of 2: Correct number of occurrences detected**" section of the Performance Test Record (page 62).

NOTE

As a point of curiosity, you may want to determine the absolute minimum pulse width and/or absolute maximum frequency at which data can be acquired. The "Performance Test Record" on page 62 does not include places for recording these values because the Performance Verification procedure only verifies that the logic analyzer meets specifications. Determination of additional parameters is not required, but may be performed at the discretion of the calibration laboratory.

On some pulse generators, the signal outputs may become unstable for a short period of time when the signal parameters are adjusted. Adjusting the pulse generator while the logic analyzer is running can cause a false failure.

If the error message is displayed immediately after making an adjustment to the pulse generator, select OK to close the error display dialog and re-run the logic analyzer.

Test the complement of the bits (250 Mb/s mode)

Now test the logic analyzer using complement data.

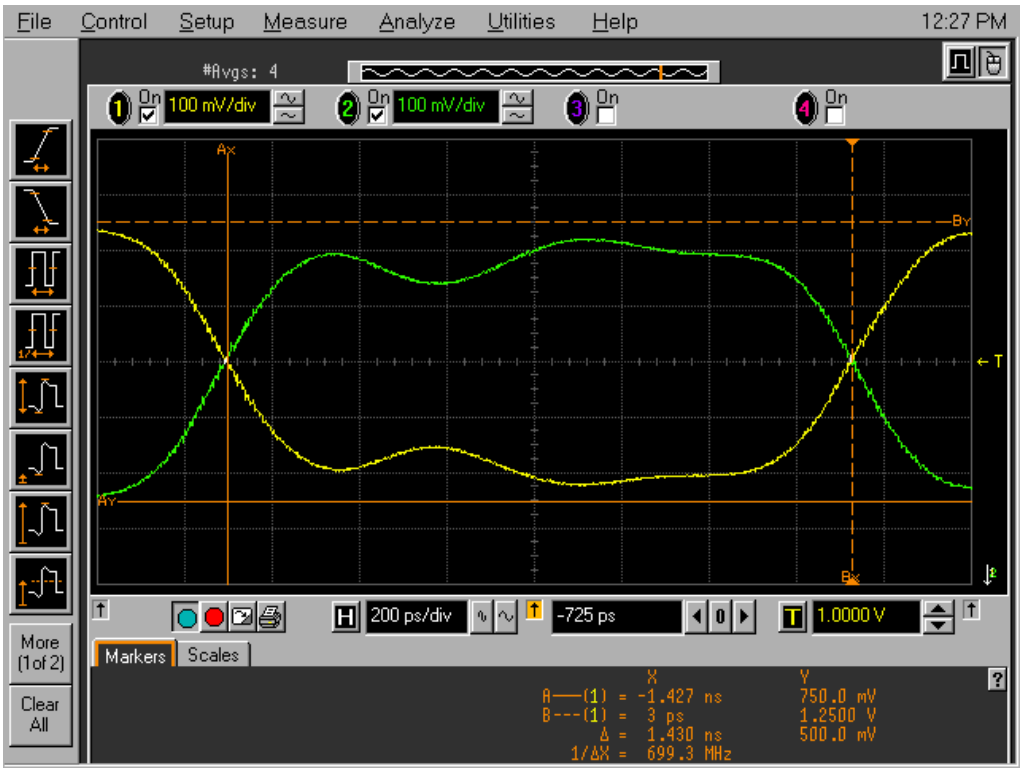
1 On the 81134A pulse generator, in the PULSE setup for CHANNEL 2, select COMP.

2 Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to -725 ps (or as required) to center the measured pulse on the oscilloscope display.

3 Verify the DC offset and adjust it if necessary. See page 40.

4 Deskew the oscilloscope if necessary. See page 41.

5 Adjust the oscilloscope's measurement markers to measure the pulse width. Set the markers so that Δ=1.43 ns (this assumes you are using the 81134A pulse generator and the Infiniium 54845A oscilloscope). Adjust the pulse generator so that the pulse width is 1.43 ns as measured by the markers. See page 42 for details.



6 Adjust the sampling positions using *eye finder*. See page 47.

7 Determine pass or fail (1 of 2 tests). See page 50.

8 Switch to the Listing window by selecting the **Listing** tab at the bottom of the main logic analyzer window.

9 Click the Run Repetitive icon .

10 Determine pass or fail (2 of 2 tests). See page 51.

Test Pod 2 in 250 Mb/s Mode

1 Disconnect the E5383A Flying Lead Probe Set from Pod 1 and connect it to Pod 2 of the logic analyzer. Do not remove the flying leads that are connected to CLK and the data channels.

2 On the 81134A pulse generator, in the PULSE setup for CHANNEL 2, press the COMP button to return the outputs to normal.

3 Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to 725 ps (or as required) to center the measured pulse on the oscilloscope display.

4 Verify the DC offset and adjust it if necessary. See page 40.

5 Deskew the oscilloscope if necessary. See page 41.

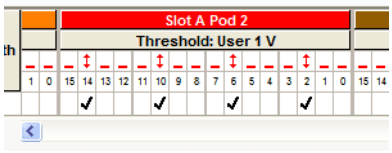
6 Readjust the pulse width from the pulse generator as measured on the oscilloscope. See page 42.

7 From the *Keysight Logic Analyzer* application's main menu, select **Setup→Bus/Signal...** or **Setup→My Logic Analyzer-1→Bus/Signal...**

8 Scroll to the right and unassign all Pod 1 bits.

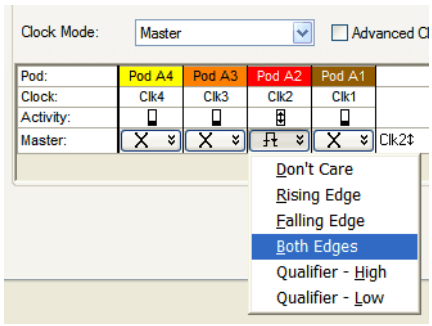
9 Ensure that the Pod 2 threshold is set to 1 volt (see page 44).

10 Assign bits 2, 6, 10, and 14 of Pod 2.



11 Select the Sampling tab (at the top of the dialog). In the State Options area, set clock Clk1 to **Don't Care.**

12 Set Clk2 to **Both Edges**.



13 Adjust the sampling positions using *eye finder*. Be sure to expand "My Bus 1" and use the recommended starting position noted on page 48. Realign any stray channels if necessary. See page 48.

14 Determine pass or fail (1 of 2 tests). See page 50.

15 Click **OK** to close the "Analyzer Setup" dialog.

16 Switch to the Listing window by selecting the **Listing** tab at the bottom of the main logic analyzer window.

17 Click the Run Repetitive icon .

18 Determine pass or fail (2 of 2 tests). See page 51.

Test the complement of the bits (Pod 2, 250 Mb/s mode)

1 Test the complement of the bits. See page 52.

Test Pods 3 and 4 in 250 Mb/s Mode

1 Perform the normal and complement tests for Pod 3 and Pod 4 on the logic analyzer, changing the connection to the pod, channel assignments, thresholds, etc. as appropriate.

Test using clock Clk3 for Pod 3 and clock Clk4 for Pod 4.

Test the Remaining Pods in 250 Mb/s Mode

The logic analyzer master card's Pod 1 clock ("Clk1" in the Sampling setup dialog) is used for testing all Pods above 4 in the 250 Mb/s mode. Therefore, two E5383A Flying Lead Probe Sets are required to test the remaining pods.

Set up the second E5383A Flying Lead Probe Set

1. Disconnect the first E5383A Flying Lead Probe Set from the pod it is currently connected to (Pod 4) and connect it to the pod under test (Pod 5).
2. Remove the pod under test Flying Lead Probe Set's CLK lead from the SMA/Flying Lead test connectors. (Do not remove the channel 2, 6, 10, and 14 leads from the SMA/Flying Lead test connectors.)
3. Connect a second E5383A Flying Lead Probe Set to Pod 1 of the logic analyzer's master card.
4. Connect the Pod 1 Flying Lead Probe Set's CLK lead to the SMA/Flying Lead test connector's pin strip connector at the 81134A pulse generator's Channel 1 OUTPUT.

Test the remaining pods

1. Perform the normal and complement tests for each remaining pod on the logic analyzer, changing the connection to the pod, channel assignments, thresholds, etc. as appropriate.

   Test using the logic analyzer master card's Pod 1 clock, "Clk1", for all Pods above 4.

   Upon completion, the logic analyzer is completely tested in the 250 Mb/s mode.

Test Pod 1 in 500 Mb/s Mode

NOTE **If option 500 is not installed on the logic analyzer, then 250 MHz will be the only speed available. In this case, write "n/a" in the 500 Mb/s mode boxes in the Performance Test Record and proceed to "Conclude the State Mode Tests" on page 61.**

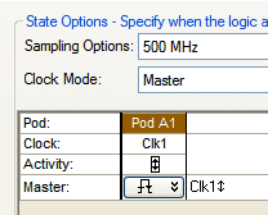
Clock "Clk1" will be used for testing all pods in the 500 Mb/s mode. Therefore two E5383A Flying Lead Probe sets will be required when testing the remaining pods.

You will use a test frequency of 125 MHz (plus test margin) to determine the correct eye in the Thresholds and Sample Positions dialog. Then you will increase the test frequency to 250 MHz (plus test margin) and perform the test.

1 Disconnect the E5383A Flying Lead Probe from the last pod tested in 250 Mb/s mode and connect it to Pod 1 of the logic analyzer.

2 From the *Keysight Logic Analyzer* application's main menu, select **Setup→Timing/State (Sampling)...** or **Setup→My Logic Analyzer-1→Timing/State (Sampling)...**

3 In the State Options section, Sampling Options field, select the "500 MHz" mode. The clock mode will change to "Both Edges". No other mode is available.



4 In the logic analyzer's Buses/Signals dialog, unassign all bits.

5 Assign bits 2, 6, 10, and 14 of Pod 1.

6 Ensure that the Pod 1 threshold is set to 1 volt. See page 44.

Determine and set *eye finder* Position (500 Mb/s mode)

1 On the 81134A pulse generator, in the PULSE setup for CHANNEL 2, press the COMP button to return the outputs to normal.

2 Change the oscilloscope's horizontal position to 725 ps (or as required) to center the measured pulse on the oscilloscope display.

3 Verify the DC offset and adjust it if necessary. See page 40.

4 Verify the oscilloscope Deskew and adjust if necessary. See page 41.

5 Adjust the measured pulse width from the pulse generator to 1.5 ns (minus the test margin) as described on page 42.

Do not change the pulse generator frequency yet.

6 Select the **Sampling** tab.

7 Click **Thresholds and Sample Positions...**. A dialog appears telling you that acquired data will be erased. Select the **Yes** button, erasing acquired data.

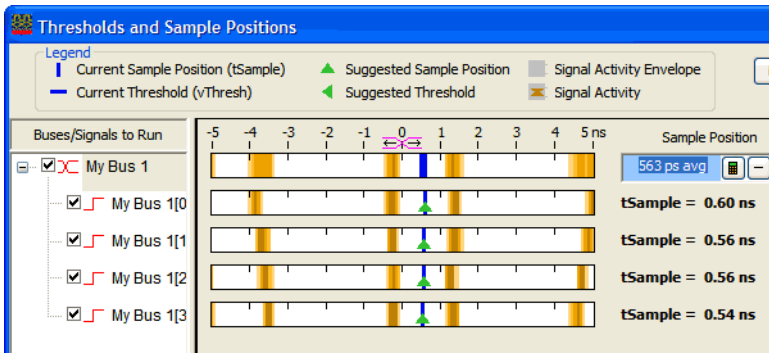
8 In the Thresholds and Sample Positions dialog, expand "My Bus 1".

9 If the blue bars are not vertically aligned, align them. See page 48.

10 Grab the blue bar for "My Bus 1" and move it to approximately 600 ps. All blue bars will follow.

11 Run *eye finder* and note the average sampling position chosen by *eye finder*:_____ps. In the following example, the average sampling position is 600 ps. Note that in this step, you place the blue bars in the narrow window (not the wide window) that appears just to the right of zero in the

eye finder display. Then run *eye finder*. The position may be different based on your test setup. Bring stray channels into alignment if necessary. See page 48.



12 Now set the pulse generator to the new test frequency. The logic analyzer will be tested using a double-edge clock. The test frequency is half the test clock rate because data is acquired on both the rising edge and the falling edge of the clock. Set the frequency to 250 MHz plus the frequency uncertainty of the pulse generator, plus a test margin of 1%.

For example, if you are using an 81134A pulse generator, the frequency accuracy is ±1% of setting. Use a test margin of 1%. Set the frequency to 250 MHz plus 2% (255 MHz).

13 The pulse measured on the oscilloscope may have moved slightly. Verify the DC offset and adjust it if necessary. See page 40.

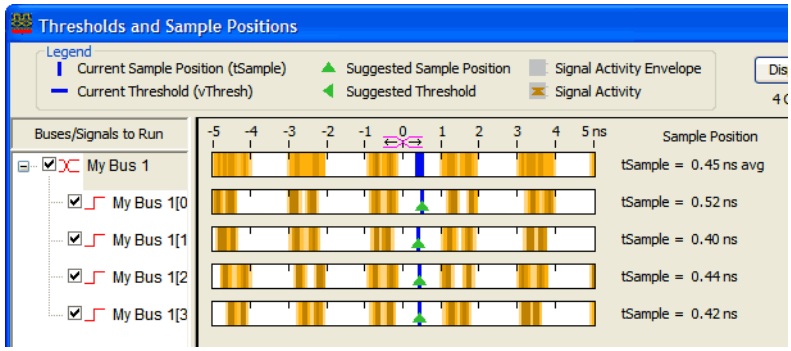
14 Verify the oscilloscope Deskew and adjust if necessary. See page 41.

15 Adjust the measured pulse width from the pulse generator to 1.5 ns (minus the test margin) as described on page 42.

16 Open the Thresholds and Sample Positions dialog, and align the blue bars vertically. See page 48.

17 Grab the blue bar for “My Bus 1” and move it to the recommended starting position you noted on page 57.

18 Run *eye finder* again. Some eyes may close, but the eyes in the sampling position you chose on page 57 should remain open.



When you close the Analyzer Setup dialog a dialog may appear. If so, answer **Yes** to erase the data and continue.

19 Perform the procedure “Determine PASS/FAIL (1 of 2 tests)” on page 50.

20 Click the Run Repetitive icon .

21 Perform the procedure “Determine PASS/FAIL (2 of 2 tests)” on page 51.

Test the complement of the bits (Pod 1, 500 Mb/s mode)

Now test the logic analyzer using complement data.

1 On the 81134A pulse generator, in the PULSE setup for CHANNEL 2, select COMP.
2 Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to -725 ps (or as required) to center the measured pulse on the oscilloscope display.
3 Verify the DC offset and adjust it if necessary. See page 40.
4 Deskew the oscilloscope if necessary. See page 41.
5 Verify that the pulse width is set to 1.5 ns. See page 42.
6 Run *eye finder* and align stray channels if necessary.
7 Perform the procedure "Determine PASS/FAIL (1 of 2 tests)" on page 50.
8 Click the Run Repetitive icon  .
9 Perform the procedure "Determine PASS/FAIL (2 of 2 tests)" on page 51

Test Pod 2 in 500 Mb/s Mode

The logic analyzer master card's Pod 1 clock ("Clk1" in the Sampling setup dialog) is used for testing all Pods above 1 in the 500 Mb/s mode. Therefore, two E5383A Flying Lead Probe Sets are required to test Pod 2 and the remaining pods.

Set up the second E5383A Flying Lead Probe Set

1 Disconnect the first E5383A Flying Lead Probe Set from the pod it is currently connected to (Pod 1) and connect it to the pod under test (Pod 2).
2 Remove the pod under test Flying Lead Probe Set's CLK lead from the SMA/Flying Lead test connectors. (Do not remove the channel 2, 6, 10, and 14 leads from the SMA/Flying Lead test connectors.)
3 Connect a second E5383A Flying Lead Probe Set to Pod 1 of the logic analyzer's master card.
4 Connect the Pod 1 Flying Lead Probe Set's CLK lead to the SMA/Flying Lead test connector's pin strip connector at the 81134A pulse generator's Channel 1 OUTPUT.

Test Pod 2 in 500 Mb/s mode

1 On the 81134A pulse generator, in the PULSE setup for CHANNEL 2, press the COMP button to return the outputs to normal.
2 Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to 525 ps (or as required) to center the measured pulse on the oscilloscope display.
3 Verify the DC offset and adjust it if necessary. See page 40.
4 Deskew the oscilloscope if necessary. See page 41.
5 Readjust the pulse width from the pulse generator as measured on the oscilloscope. See page 42.
6 Unassign all Pod 1 bits.
7 Assign bits 2, 6, 10, and 14 of Pod 2.
8 Ensure that the Pod 2 threshold is set to 1 volt (just as you did for Pod 1 on page 44).
9 Adjust the sampling positions using *eye finder*. Be sure to expand "My Bus 1", align the blue bars vertically, and use the starting position you noted on page 57. Realign any stray channels if necessary. See page 48.
10 Determine pass or fail (1 of 2 tests). See page 50.
11 Switch to the Listing window.

12 Click the Run Repetitive icon .

13 Determine pass or fail (2 of 2 tests). See page 51.

Test the complement of the bits (Pod 2, 500 Mb/s mode)

1 Test the complement of the bits on Pod 2. You can use the procedure "Test the complement of the bits (250 Mb/s mode)" on page 52 as a guideline.

Test the Remaining Pods in 500 Mb/s Mode

1 Perform the normal and complement tests for each additional pod on the logic analyzer, changing the connection to the pod, channel assignments, thresholds, etc. as appropriate.

Again, you must use the logic analyzer master card's Pod 1 clock ("Clk1" in the Sampling setup dialog) for all tests in the 500 Mb/s mode.

Note that in 500 Mb/s mode, one pod pair is reserved for time tag storage; however, you can re-assign pod pairs to test pods that are currently reserved (see "To re-assign pods reserved for time tag storage" on page 60).

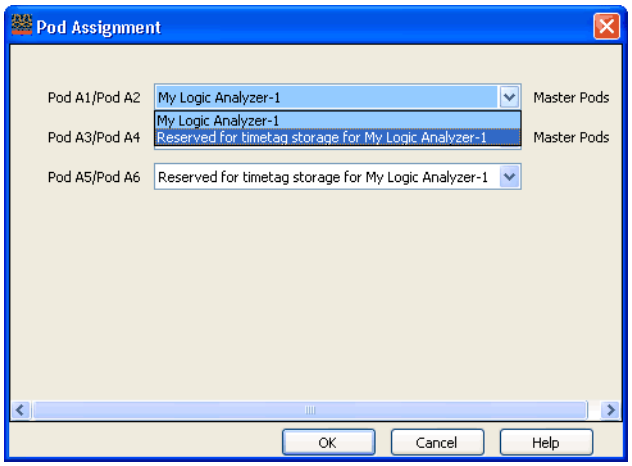
Upon completion, the logic analyzer is completely tested.

2 Complete the Performance Test Record on page 62.

To re-assign pods reserved for time tag storage

1 From the main menu, select **Setup→Pod Assignment...** or **Setup→My Logic Analyzer-1→Pod Assignment...**

2 In the Pod Assignment dialog, select pod pair A1/A2 to be reserved for time tag storage.



3 Click **OK**.

4 Reconfigure the markers to search for 131071 occurrences instead of 131072 (see "Configure the markers" on page 50).

After re-assigning pod pairs, you can test pods that were previously reserved for time tag storage.

Note that you can reserve Pod 1 and Pod 2 on the master card for time tag storage and still use the CLK input on Pod 1.

Conclude the State Mode Tests

Do the following steps to properly shut down the logic analyzer session after completing the state mode tests.

1 End the test.

a In the *Keysight Logic Analyzer* application, select the [X] in the upper right corner to close the window. At the query “Do you want to save the current configuration?” select No.

Ending and restarting the logic analysis session will re-initialize the system.

b Disconnect all cables and adapters from the pulse generator and the oscilloscope.

Performance Test Record

LOGIC ANALYZER MODEL NO. (circle one): 16801A, 16802A, 16803A, 16804A, 16806A, 16821A, 16822A, 16823A	
Logic Analyzer Serial No.	Work Order No.
Date:	Recommended Test Interval - 2 Years
	Recommended next testing:

TEST EQUIPMENT USED	
Pulse Generator Model No.	Oscilloscope Model No.
Pulse Generator Serial No.	Oscilloscope Serial No.
Pulse Generator Calibration Due Date:	Oscilloscope Calibration Due Date:

MEASUREMENT UNCERTAINTY	
Clock Rate	Pulse Width (Eye Width)
Pulse Generator Frequency Accuracy: 81134A: 1% of setting	Oscilloscope Horizontal Accuracy: 54845B: ±[((0.007%) (Δt)+(full scale/(2x memory depth))+30 ps] ≅ 30 ps Oscilloscope Display Resolution: 54845B: ±5 ps
Setting: 125 MHz + 2% = 127.5 MHz 250 MHz + 2% = 255 MHz	Pulse Width setting: 1.43 ns PWmax(worst case) = 1.43 ns+30 ps+5 ps = 1.465 ns

TEST RESULTS				
Logic Analyzer Self-Tests (Pass/Fail):				
Performance Test: Minimum Master to Master Clock Time and Minimum Pulse Width				
	250 Mb/s mode		500 Mb/s mode (if option 500 is installed)	
Pulse Generator Settings	Freq: 125 MHz plus test margin Pulse Width: 1.5 ns less test margin		Freq: 250 MHz plus test margin Pulse Width: 1.5 ns less test margin	
Test Criteria	Test 1 of 2 eye finder locates an eye for each bit	Test 2 of 2 Correct number of occurrences detected	Test 1 of 2 eye finder locates an eye for each bit	Test 2 of 2 Correct number of occurrences detected
Pod 1 Results (pass/fail):				
Pod 2Results (pass/fail):				
Pod 3 Results (pass/fail):				
Pod 4 Results (pass/fail):				
Pod 5 Results (pass/fail):				
Pod 6 Results (pass/fail):				
Pod 7 Results (pass/fail):				
Pod 8 Results (pass/fail):				
Pod 9 Results (pass/fail):				

TEST RESULTS				
Logic Analyzer Self-Tests (Pass/Fail):				
Performance Test: Minimum Master to Master Clock Time and Minimum Pulse Width				
	250 Mb/s mode		500 Mb/s mode (if option 500 is installed)	
Pulse Generator Settings	Freq: 125 MHz plus test margin Pulse Width: 1.5 ns less test margin		Freq: 250 MHz plus test margin Pulse Width: 1.5 ns less test margin	
Test Criteria	Test 1 of 2 eye finder locates an eye for each bit	Test 2 of 2 Correct number of occurrences detected	Test 1 of 2 eye finder locates an eye for each bit	Test 2 of 2 Correct number of occurrences detected
Pod 10 Results (pass/fail):				
Pod 11 Results (pass/fail):				
Pod 12 Results (pass/fail):				

4 Calibrating and Adjusting

Calibration Strategy

The 16800 Series logic analyzers do not require operational accuracy calibration.

5 Troubleshooting

This chapter helps qualified service personnel troubleshoot the logic analyzer to find defective assemblies. The troubleshooting consists of flowcharts, self-test instructions, and tests. This information is not intended for component-level repair.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform other tests. The other tests are located in this chapter after the flowcharts.

The service strategy for this instrument is the replacement of defective assemblies. This instrument can be returned to Keysight for all service work, including troubleshooting. Contact your nearest Keysight Technologies Sales Office for more details.

CAUTION **Electrostatic discharge can damage electronic components. Use grounded wrist straps and mats when you perform any service to this instrument or to the cards in it.**

To use the system troubleshooting flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled references on the charts indicate connections with the other flowcharts or other parts within the same flowchart. A circled alpha references connections within the flowchart. Start your troubleshooting at the top of the first flowchart (Figure 1 on page 69).

Figure 1 System Troubleshooting Flowchart

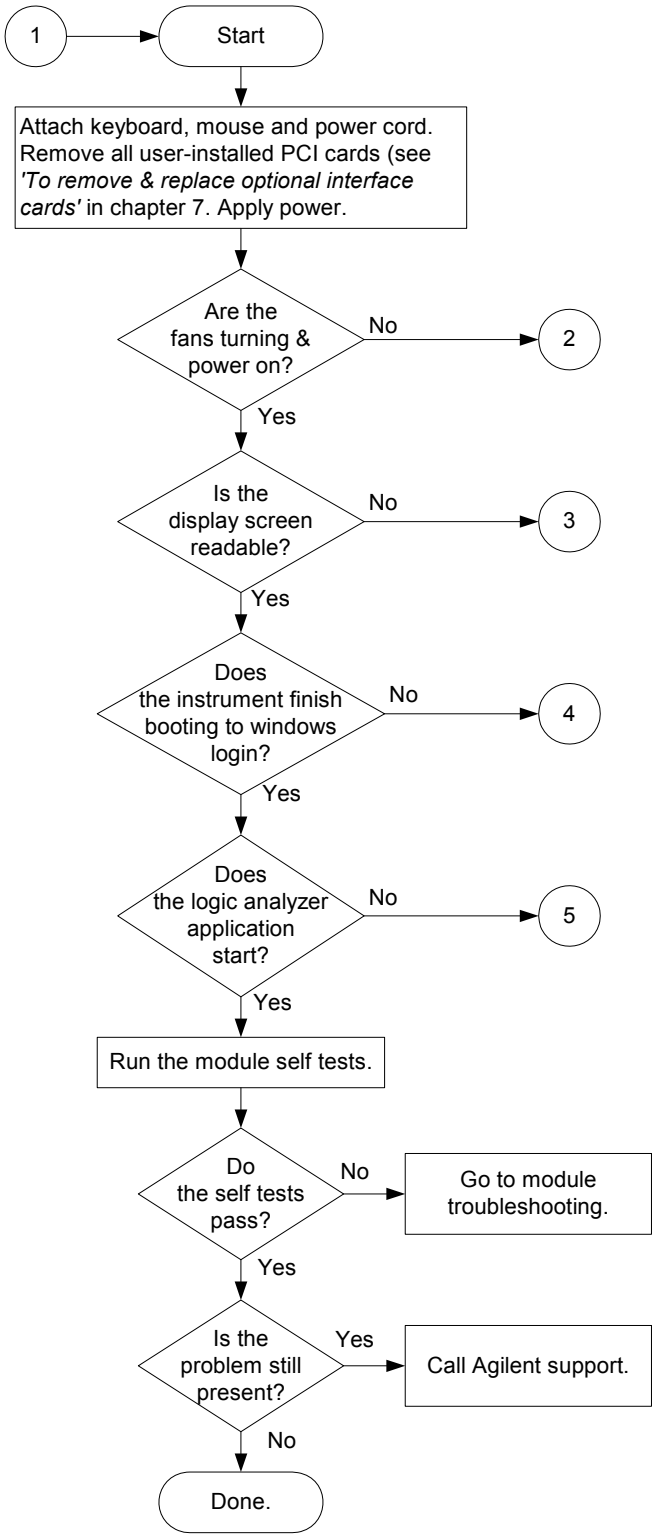


Figure 2 System Power Troubleshooting Flowchart

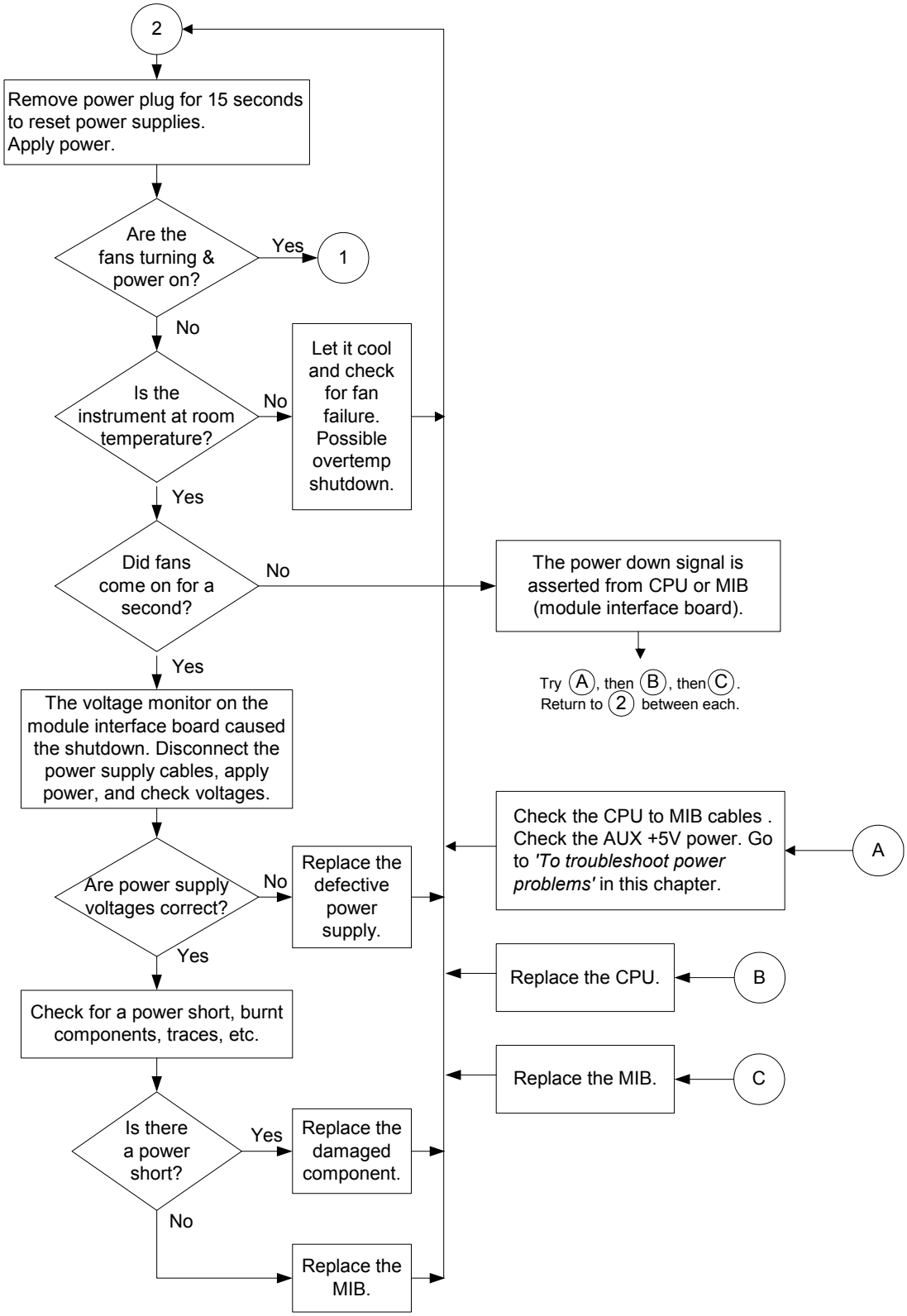


Figure 3 System Display Troubleshooting Flowchart

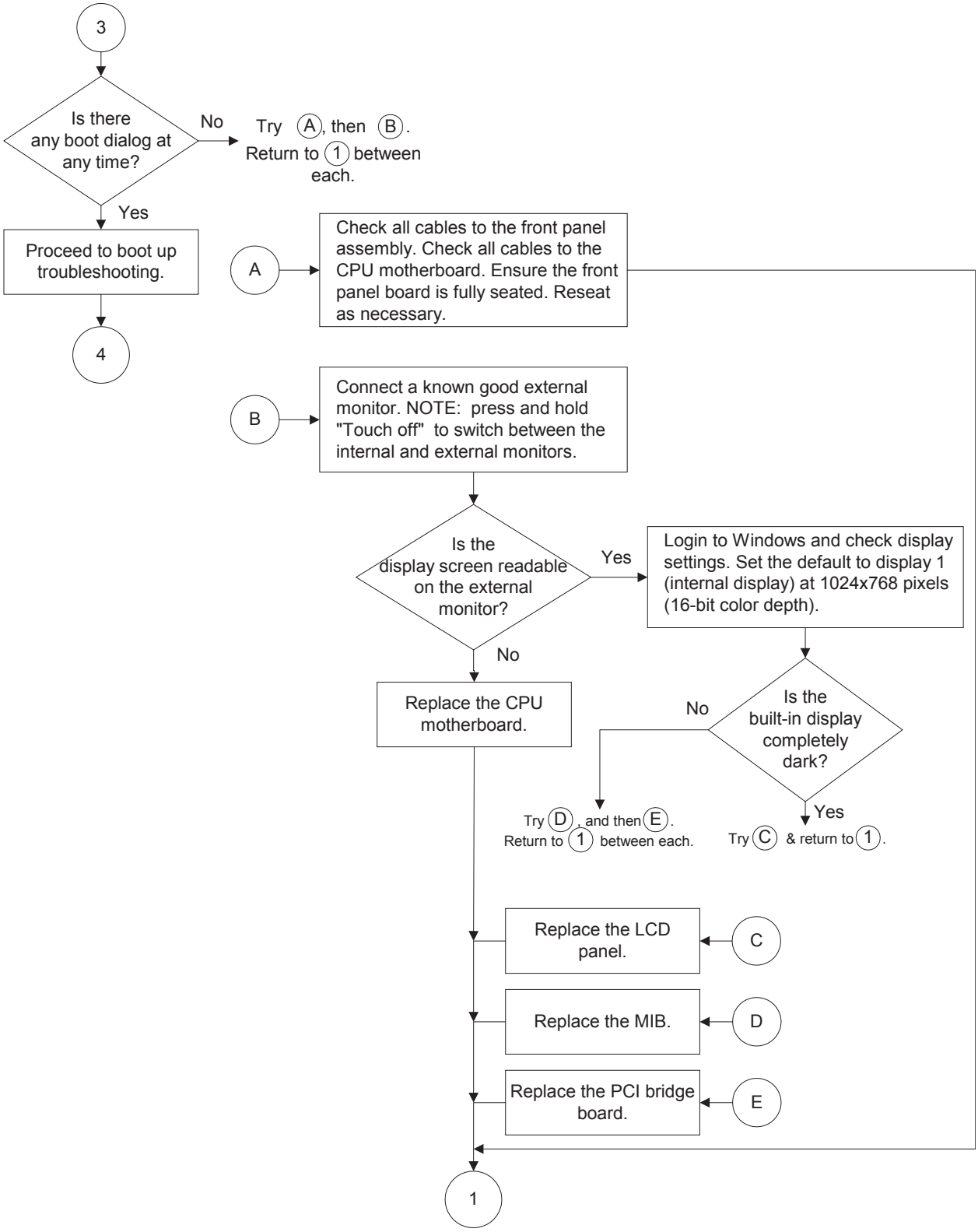


Figure 4 System Boot Up Troubleshooting Flowchart

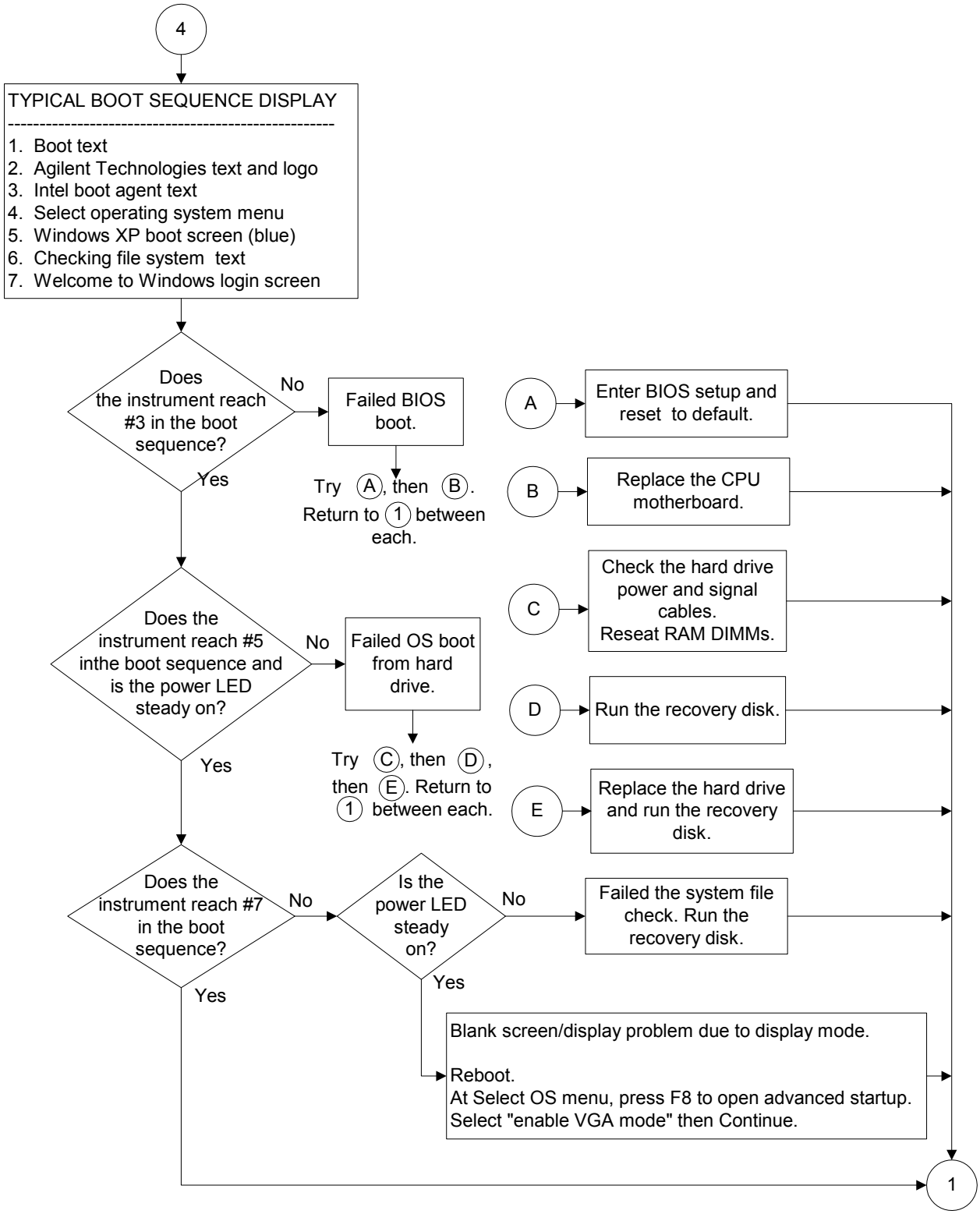
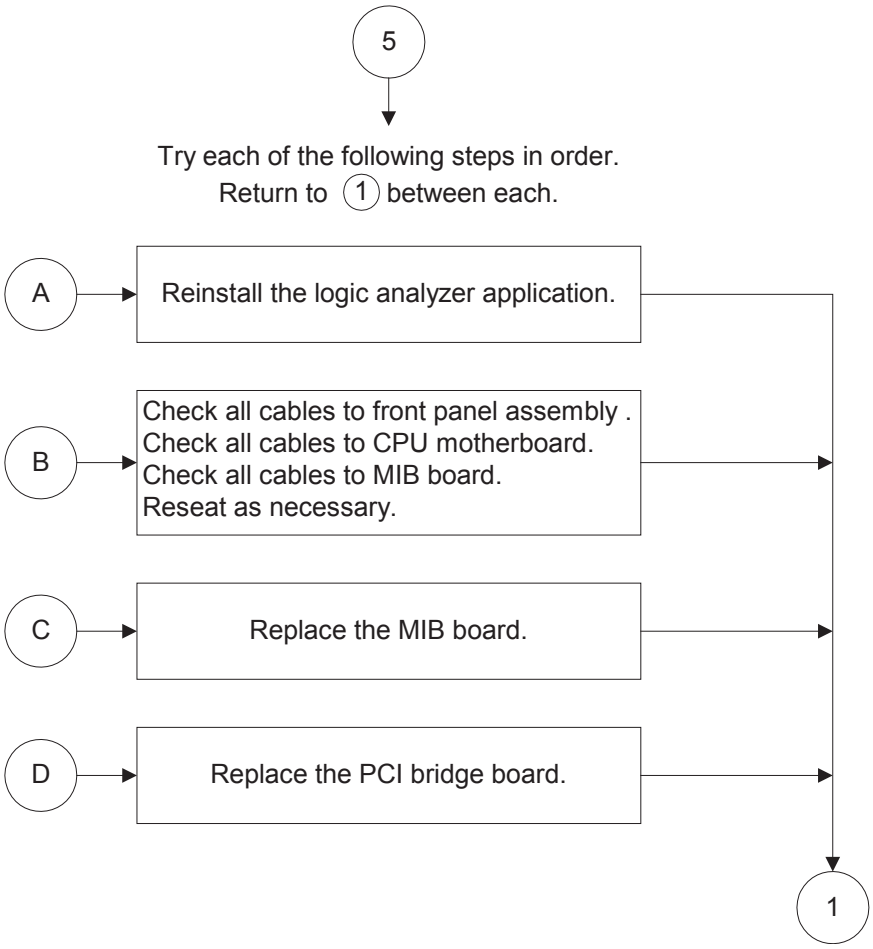


Figure 5 System Application Troubleshooting Flowchart



To use the logic acquisition troubleshooting flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled numbers on the charts indicate connections with the other flowchart. Start your troubleshooting at the top of the first flowchart.

If the module still doesn't work correctly after completing all the procedures described in the flowchart, return it to Keysight Technologies for repair. Be sure to include a note describing the problem in detail.

Figure 6 Logic Acquisition Troubleshooting Flowchart 1

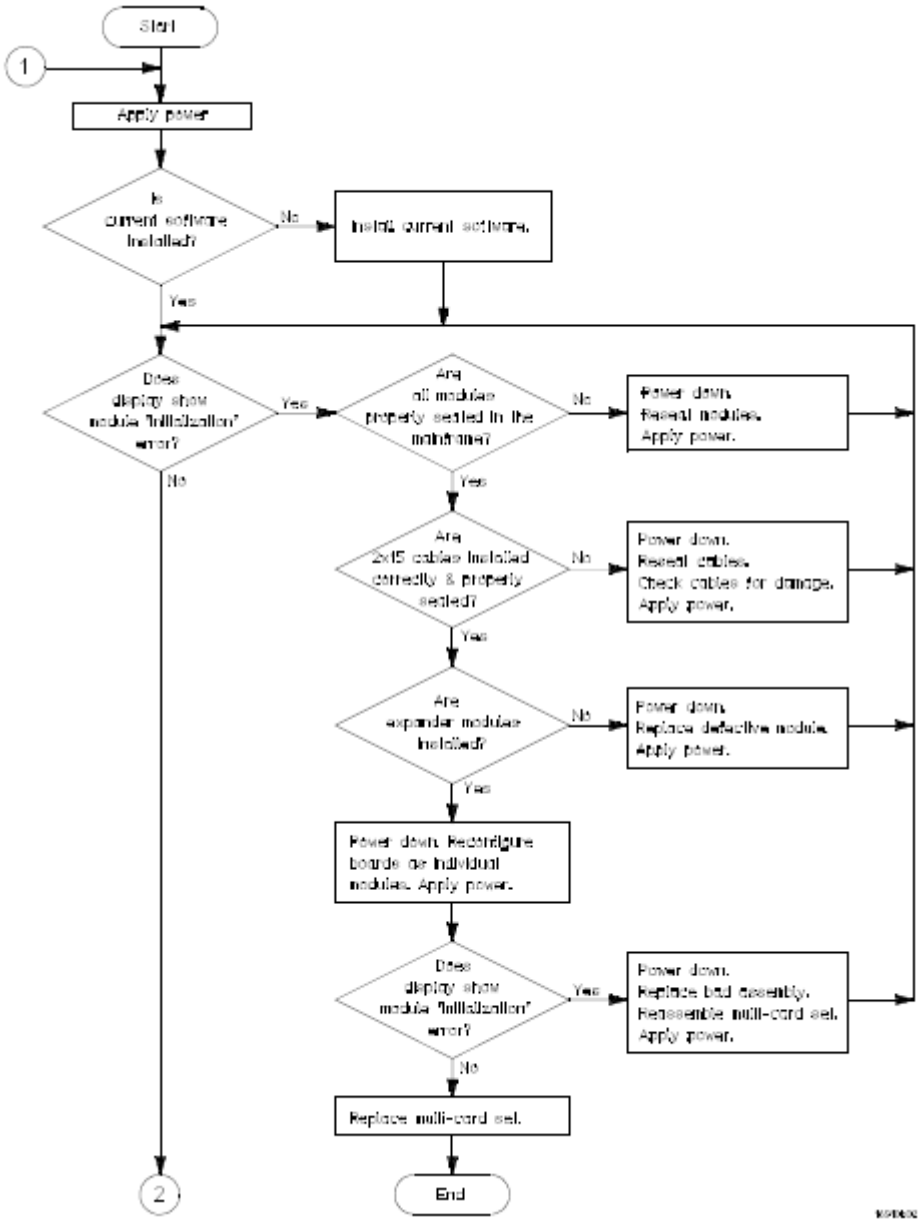
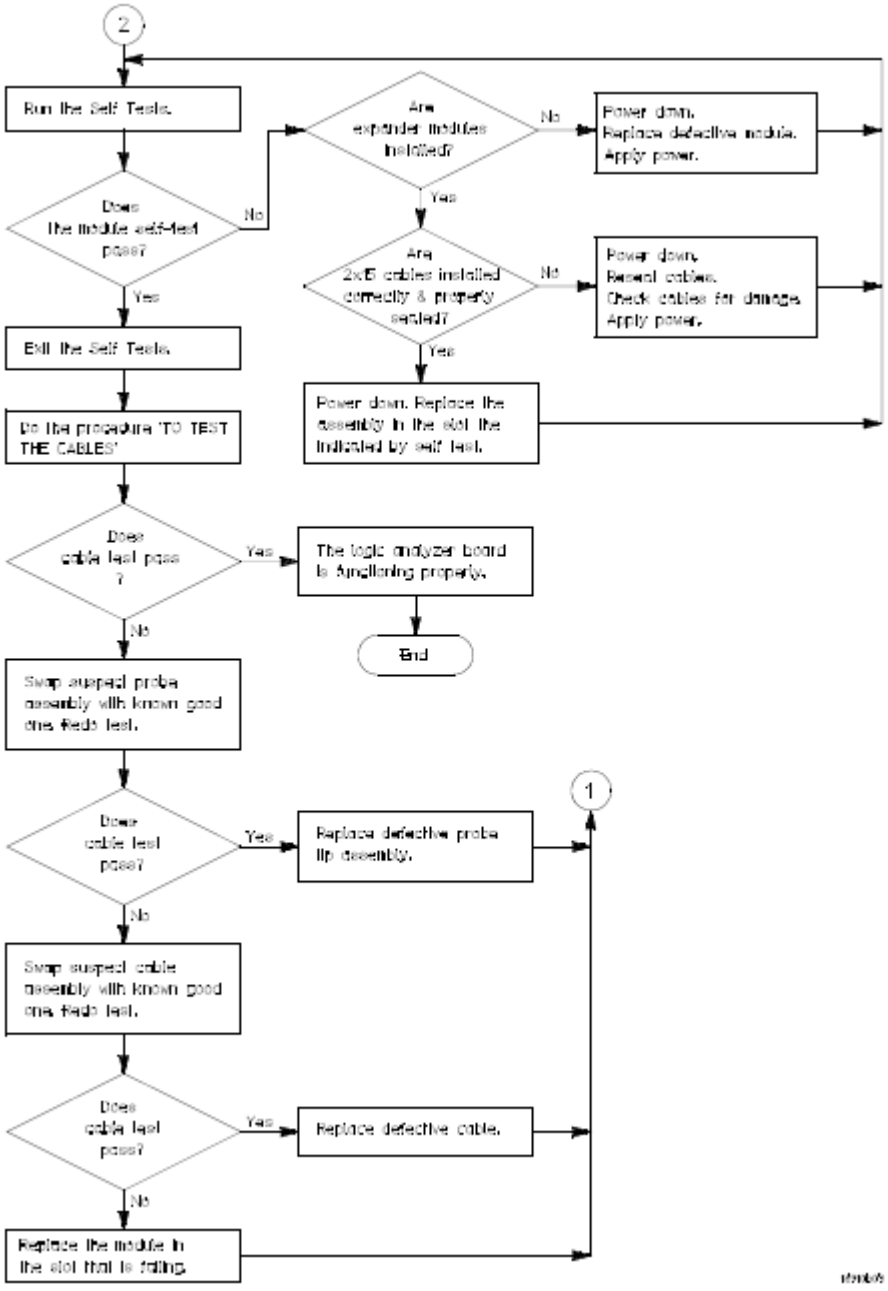


Figure 7 Logic Acquisition Troubleshooting Flowchart 2



To use the pattern generator troubleshooting flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled numbers on the charts indicate connections with the other flowcharts. Start your troubleshooting at the top of the first flowchart.

Figure 8 Pattern Generator Troubleshooting Flowchart 1

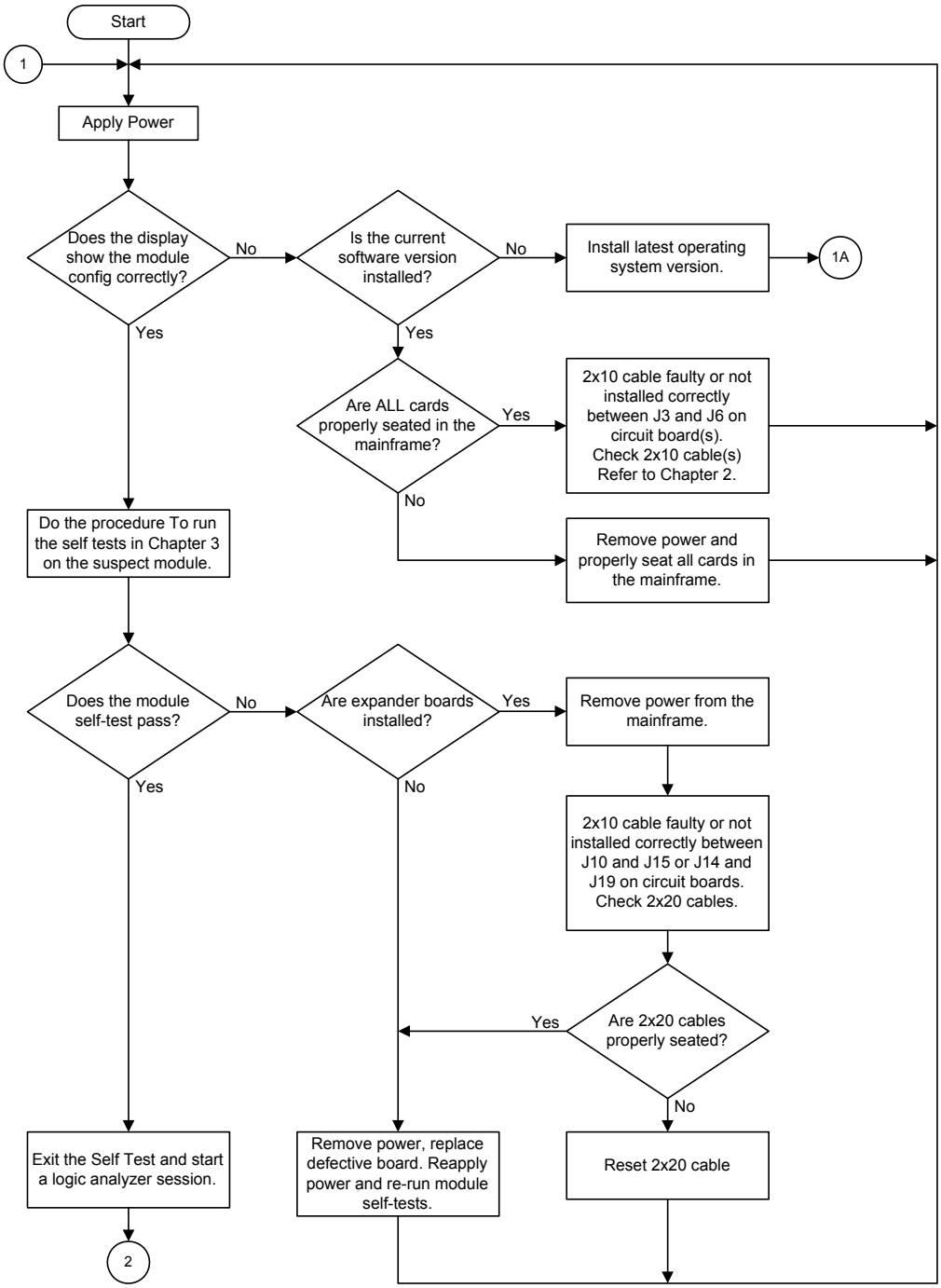
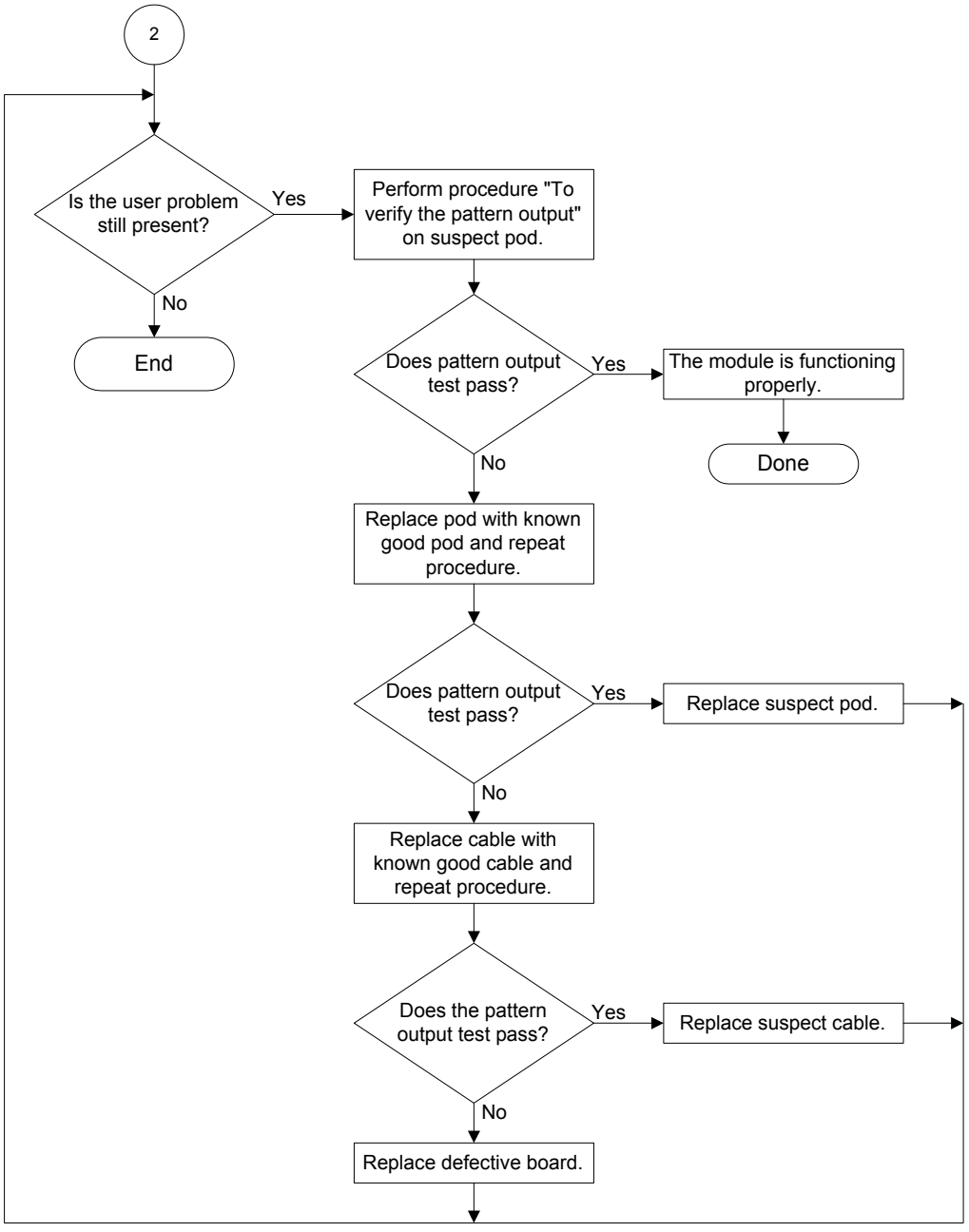


Figure 9 Pattern Generator Troubleshooting Flowchart 2



To troubleshoot system power problems

If the system warns you it is powering down before it powers down, it is a fan/over-temp problem. If it just powers down, it is a power supply problem.

If the lights do not come on and if the system powers up momentarily when you plug it in, make sure the power button hasn't become jammed or stuck in the pushed-in position.

Power Supplies

All 16800 Series logic analyzers have the same 600 W power supply and a second power supply that depends on the type of frame:

- The 1-slot, low-power frame (for 16801A, 16802A, and 16803A logic analyzers) has a second, 15 W power supply.
- The 2-slot, high-power frame (for 16804A, 16806A, 16821A, 16822A, and 16823A logic analyzers) has a second, 175 W power supply.

The power supplies must remain connected in order to test their output voltages. There are power supply test points on the MIB board.

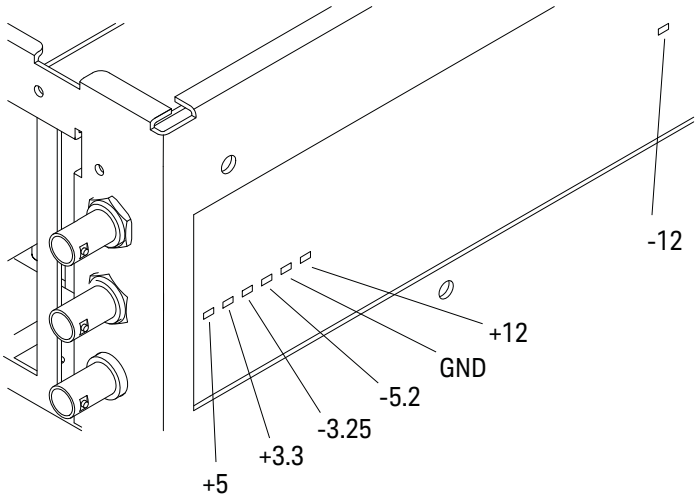
To check the power supply voltages

WARNING **Hazardous voltages exist on the power supply. This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.**

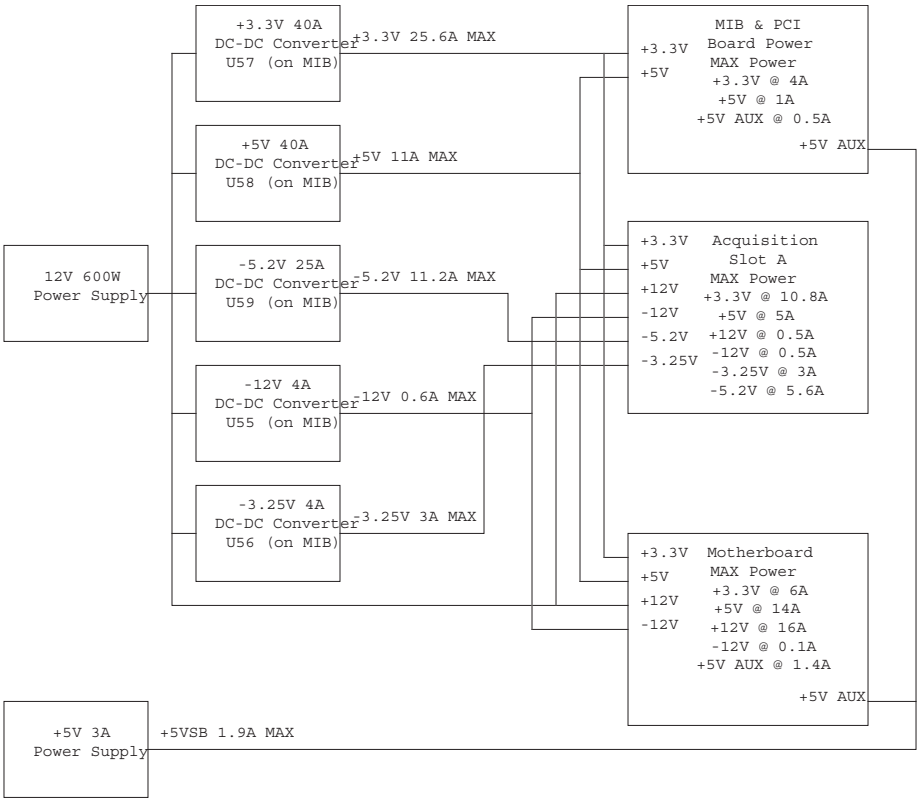
1 Turn off the instrument using one of the methods described in "To power off the system" on page 109.
2 Disconnect the instrument's power cord, move the instrument to a static safe work environment, then remove the cover (instructions in "To remove and replace the cover" on page 111).
3 Ensure that the CPU power cable and reset cables are seated properly.
4 Reconnect the instrument's power cord, then apply power to the instrument.
5 Using a digital voltmeter, measure the DC power supply voltages. Use the following graphics when measuring the voltages.
6 Using a voltmeter, ensure the AUX +5V power on the MIB measures +5V. If it does not, replace the power supply.
7 Referring to the graphics that follow, note problems with the power supply, then return to Figure 2, "System Power Troubleshooting Flowchart," on page 70.

Use the following graphics when measuring the voltages.

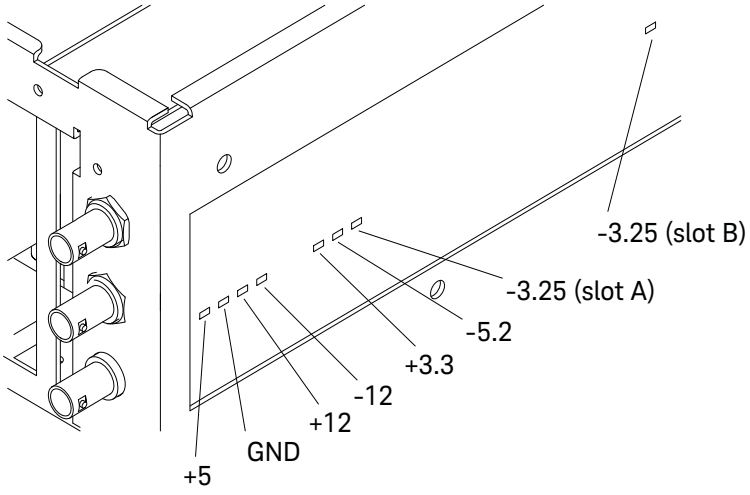
Power Supply Test Points on the 1-Slot, Low-Power Frame



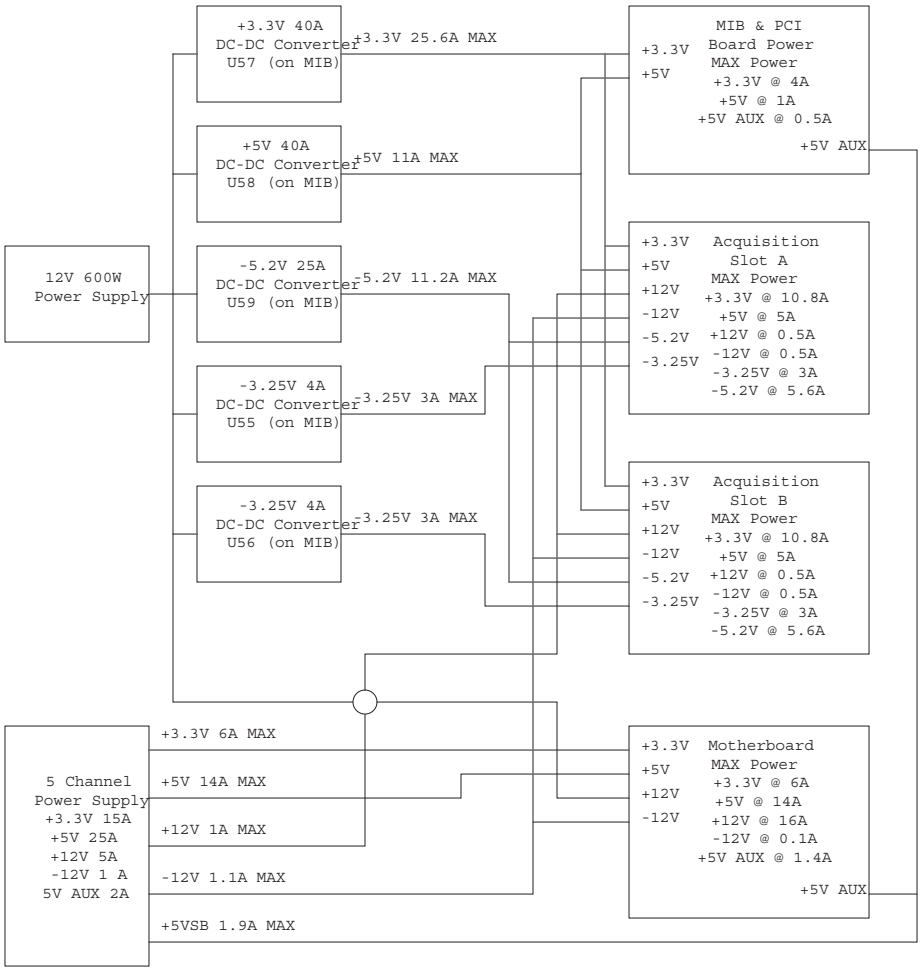
Power Supply Block Diagram of the 1-Slot, Low-Power Frame



Power Supply Test Points on the 2-Slot, High-Power Frame



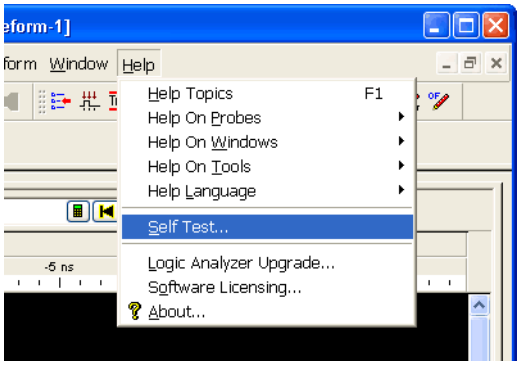
Power Supply Block Diagram of the 2-Slot, High-Power Frame



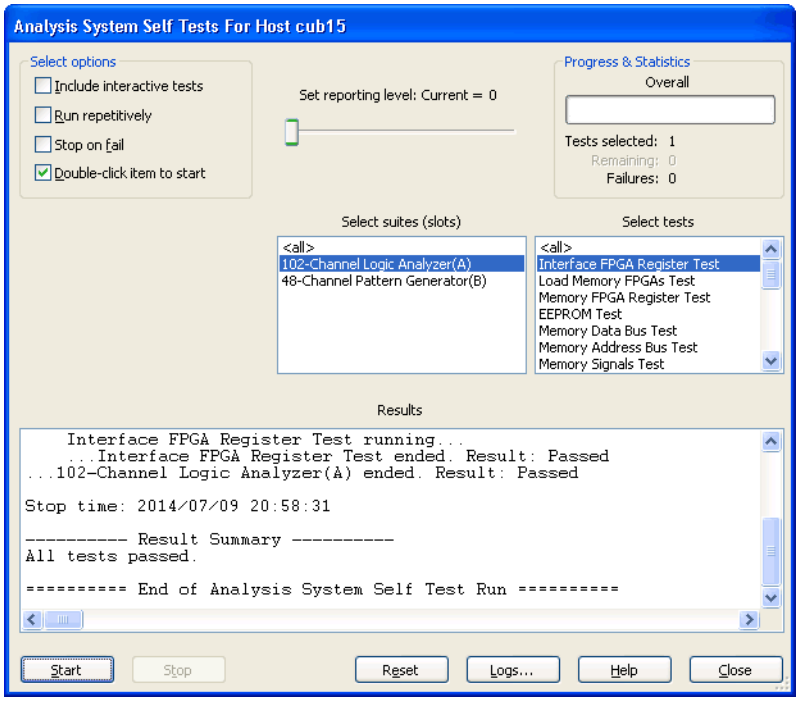
To run the self-tests

The self-tests check the functional operation of the logic analyzer. Perform the self-tests as an acceptance test when receiving the logic analyzer or when the logic analyzer is repaired.

1 In the *Keysight Logic Analyzer* application, click Help>Self Test...



2 In the Analysis System Self Test dialog, double click on the test you want to run.



Logic Acquisition Self-Test Descriptions

The self-tests for the logic analyzer identify the correct operation of major functional areas in the module.

Interface FPGA Register Test

The purpose of this test is to verify that the backplane interface can communicate with the backplane FPGA. This FPGA must be working before any of the other circuits on the board will work. The backplane FPGA is the interface between the backplane and the Memory Controller FPGAs and Analysis Chips. Also, the Backplane FPGA generates the board ID code that is used to identify the module and slot.

Load Memory FPGA Test

The purpose of this test is to verify that the Memory Controller FPGAs can be loaded with their respective configuration data files.

Memory FPGA Register Test

The purpose of this test is to verify that the registers in the Memory Controller FPGAs can be written to and read back.

EEPROM Test

The purpose of this test is to verify:

- The address and data paths to the EEPROM.
- That each cell in the EEPROM can be programmed high and low.
- That individual locations can be independently addressed
  The EEPROM can be block erased.

Memory Data Bus Test

The purpose of this test is to check the data write/read access of the acquisition RAM from the module backplane bus. This test verifies the operation of the RAM data bus as well as some of the operation of the RAM control and address busses. This is the first test that accesses the RAM acquisition memory using the Memory Controller FPGAs.

Memory Address Bus Test

The purpose of this test is to completely verify the acquisition RAM address lines.

Memory Signals Test

The purpose of this test is to verify signal integrity and proper read/write synchronization between the Memory Controller FPGAs and the acquisition RAM memory devices.

HW Assisted Memory Cell Test

The purpose of this test is to fully check all of the addresses in all acquisition RAM memory devices.

Memory Unload Modes Test

The purpose of this test is to check the various modes of unloading data from the acquisition RAM devices. These modes are setup by writing to registers in the Memory Controller FPGAs. These FPGAs sequence the data and perform data decoding based on the mode.

DMA Test

The purpose of this test is to check the various modes of unloading data from the acquisition RAM memories using DMA backplane transfers. This test is essentially the same as the Memory Unload Modes Test except that DMA backplane transfers are used to read the data from the board.

HW Accelerated Search Test

This test verifies the Memory Controller FPGA-based HW Accelerated Search function.

Chip Registers Read/Write Test

The purpose of this test is to verify that each writable bit in each register of the Analysis chips can be written with a 1 and 0 and read back again. The test also verifies that a chip reset sets all registers to their reset condition (all 0s for most registers).

LA Chip Calibrations Test

The purpose of this test is to verify that each analysis chip in the module is able to successfully complete self-calibration.

Analyzer Chip Memory Bus Test

The purpose of this test is to check the Analysis chip memory busses that go between the Analysis chips and the Memory Controller FPGAs.

System Clocks Test

The purpose of this test is to verify that the four clocks (1/2/3/4) are functional between the master board and all Analysis chips, and that the two Psync lines (A/B) are functional between the master board's Analysis chips and all Analysis chips in the module. This test verifies that the four clock lines are driven from the master board and can be received by all Analysis chips, and that the Psync lines can be driven by each master chip on the master board and received by all other Analysis chips in the module.

Turbo Clock Divider Test

The logic analyzer has a clock divider on the board, used for single edge turbo state. This test verifies that the divider routing works, and that it resets low.

System Backplane Clock Test

The purpose of this test is to verify the system backplane 100 MHz clock is functional to each Analysis chip and running at the correct frequency. This test also verifies that the PLL in each chip can be configured in bypass mode (PLL is not used), then verifies that the PLL can be enabled and used to generate additional clock frequencies.

Comparators Test

The purpose of this test is to verify that the front-end signal comparators are able to be set to maximum and minimum thresholds and that they are able to recognize activity on each input using the cal input clock.

Inter-chip Resource Bus Test

The purpose of this test is to verify that the Inter-chip Resource lines (ICRs) can be driven as outputs and received as inputs by each chip in the module.

Inter-module Flag Bits Test

The purpose of this test is to verify that the 4 Inter-module Flag Bit Output lines can be driven out from the master chip in the module and received by each chip in the module.

Global and Local Arm Lines Test

The purpose of this test is to verify that each Analysis chip on the master board can receive the Local Arm signal, and the Global Arm signal can be driven by the bottom and top chips on the master board and received by all chips in the module (master and slave). Note that the middle analysis chip cannot drive the Global Arm signal (left unconnected).

Timing Zoom Memory BIST Test

This test verifies that the timing zoom SRAM embedded in the analysis chips is functional.

Timing Zoom Memory Addr/Data Test

This test verifies connectivity of components within the analysis chip. It verifies that the address, data, and clock lines of the timing zoom circuitry is correct.

Pattern Generator Self-Tests Description

The self-tests for the pattern generator identify the correct operation of major functional areas in the module.

Internal Loopback Test

The internal loopback test verifies the operation of the module backplane interface IC. A walking ones pattern is written into module memory at a specific memory location, read, and compared with known values.

Passing the internal loopback test implies the module backplane interface IC is functioning and the system is able to write to module memory.

In case of error, the following diagnostic integer will be displayed.

Bit#:	39 - 16	15 - 8	7 - 0
	Memory Address	Expected Value	Actual Value

Clock Test

The clock test verifies that three clock modes can be set to verify both phase-locked loop (PLL) clock generators are functioning. Additionally, the clock test verifies the RUN/STOP control circuit is functional. Parts of the module backplane interface IC and the intermodule bus (IMB) are also tested.

Passing the clock test implies that the module can generate clocks through the advertised frequency range.

In case of error, the following diagnostic integer will be displayed.

Bit#:	15 - 12	11 - 8	7 - 4	3 - 0
	300 MHz clock	200 MHz clock	100 MHz clock	not used

The four bit values have the following definition:

- 0 - passed
- 1 - failed to run
- 2 - failed to stop

Simple RAM Test

The RAM test verifies that the entire module memory is functioning. Patterns of all “0”, then all “1”, then alternating “0” and “1” are written, read, and compared with known values.

Bit#:	15 - 7	6	7	4	3	2	1	0
	not used	#7&8	6	5	4	3	2	1

Passing the simple RAM test verifies that all of the module RAM is functioning properly.

In case of error, the following diagnostic integer indicating the status of the memory IC number will be displayed.

The one bit value has the following definition:

- 0 - passed

- 1 - failed

RAM Persistence Test

The RAM persistence test verifies the module memory refresh, addressing and data retention. A pattern sequence is written to blocks in module memory. Because of this pattern writing process, a long delay is introduced before the patterns are read and verified. The patterns are then read and verified, then compared with known values.

Passing the RAM persistence test implies that the module memory retains the data at each memory location that is programmed.

In case of error, the following diagnostic integer indicating the status of the memory IC number will be displayed.

Bit#:	15 - 7	6	7	4	3	2	1	0
	not used	#7&8	6	5	4	3	2	1

The one bit value has the following definition:

- 0 - passed
- 1 - failed

Marching Bits RAM Test

The marching bits RAM test is a very extensive test and may take hours to complete. Therefore this test is not included in “Test All.” If the simple RAM test and RAM persistence test are run and you still suspect a memory problem, then run the marching bits RAM test.

The marching bits RAM test attempts to uncover any possible failure mode of module memory. Several walking “0” and walking “1” patterns are written to memory, read, and compared with known values. A total of five read/write passes are done with each pattern.

Passing the marching bits RAM test implies there is very high confidence that every module memory IC data and address memory pipeline is operating properly.

Wait Test

The wait test verifies the correct operation of the WAIT pattern registers in the module backplane interface IC. Test events are loaded into the WAIT pattern registers, then correct operation of the module is verified.

Passing the wait test implies the module will operate properly to user commands.

In case of error, the following diagnostic integer will be displayed.

Bit#:	15 - 12	11 - 8	7 - 4	3 - 0
	Event D	Event C	Event B	Event A

The four bit values have the following definition:

- 0 - passed
- 1 - failed to stop on break with no event wait
- 2 - failed on wait with setting of no event
- 3 - failed to stop on break or wait with wait any event

Instruction Interrupt Test

The instruction interrupt test verifies the WAIT IMB and SIGNAL IMB instruction decoder. The module is configured for a run, then verified that it is running. The module is again configured for a run, then halted by a break command.

Passing the instruction interrupt test verifies that the module will operate properly to user commands.

In case of error, the following diagnostic integer will be displayed.

Bit#:	15 - 4	3 - 0
	not used	Status

The four bit values have the following definition (errors are or'ed):

- 0 - passed
- 1 - stopped without a break
- 2 - failed to stop from software
- 4 - failed to stop with break
- 8 - stopped by something other than break

To exit the test system

1 Simply close the self-test dialog. No additional actions are required.

To restore the system software

Restoring your system software might be necessary for the following reasons:

- Hard drive failure.
- Virus in the system or unstable system.
- Intentional disk clean - for example if you are passing the system to another team or returning it to a rental company and you do not want any data left on it.

On a Legacy 16800 Series Logic Analyzer with Windows XP Installation

The legacy 16800 series of Logic Analyzers have the Windows XP operating system installed. These systems also have the Keysight Logic Analyzer software preinstalled.

Follow the instructions provided with the recovery CD or DVD that accompanies your Logic Analyzer to restore your system software. You need to have a keyboard, mouse, and USB DVD-ROM drive connected.

CAUTION Running the recovery disks will reformat your hard drive. All data files and programs will be overwritten. Save your license files and data to a CD or to another machine before performing this procedure.

On a 16800 Series Logic Analyzer with Windows 7 Installation

The 16800 series of Logic Analyzers with serial number of MY51420101 or higher have the Windows 7 operating system installed. These systems also have the Keysight Logic Analyzer software version 5.20 or later preinstalled. These systems do not have any recovery CD or DVD in their shipment.

If you need to restore the logic analysis system software, you run the recovery process on the hard drive of the system. This recovery process uses the hidden partition on the hard drive to restore the hard disk drive back to its original state in which it was shipped. When you run this process, the recovered hard disk drive contains:

- the Windows 7 operating system
- the version of the Logic Analyzer software which was installed when the system was originally shipped and not the latest or upgraded version of the software that might be available at the time of system recovery.
- the license files of any licensed optional products that you had purchased with the Logic Analyzer and that were installed when the system was originally shipped.

NOTE When you run the recovery process, the software licensing Host ID of your logic analyzer may change. If this happens, the restored license files will not work with the new host ID and you will need rehosted license files. To get these files, you can contact your nearest Keysight sales/service office. To locate a sales or service office, go to www.keysight.com/find/contactus.

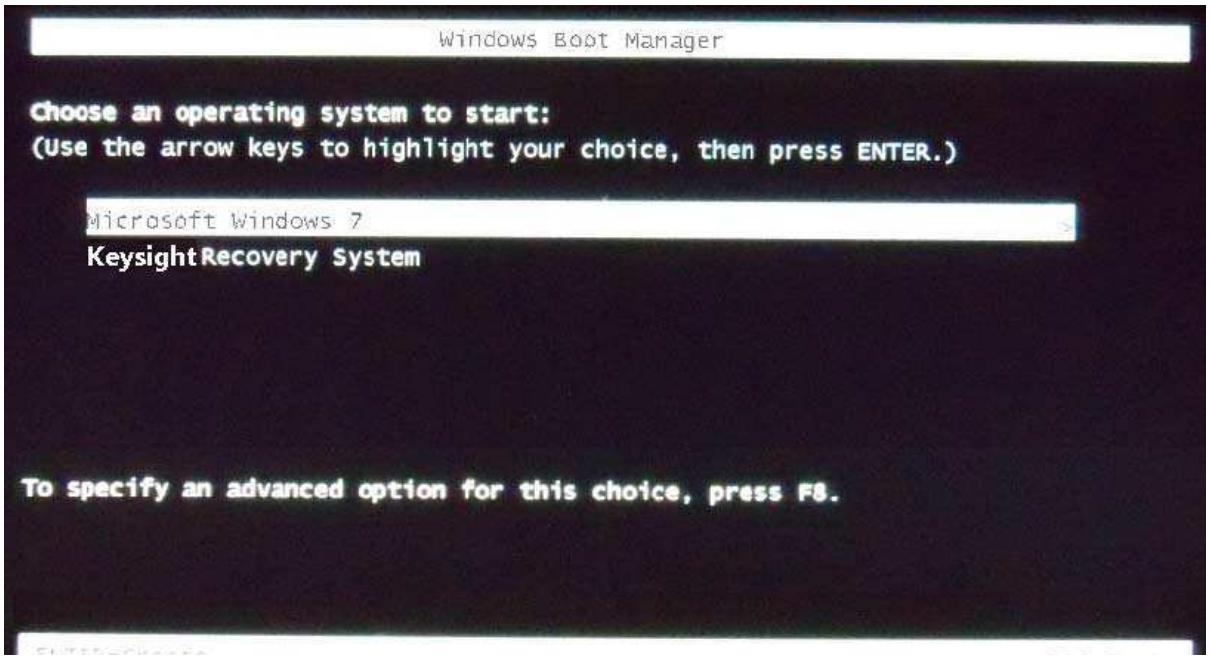
CAUTION Running the recovery process reformats your logic analyzer's hard disk drive to the state in which it was originally shipped to you. All user data files and programs are overwritten when the recovery process runs. Therefore, save your data to a CD or to another machine before you start recovering the system software.

To run the recovery process

1 Shut down and then restart your Logic Analyzer.

While booting up, the Logic Analyzer displays the Windows Boot Manager screen. This screen provides you the following options:

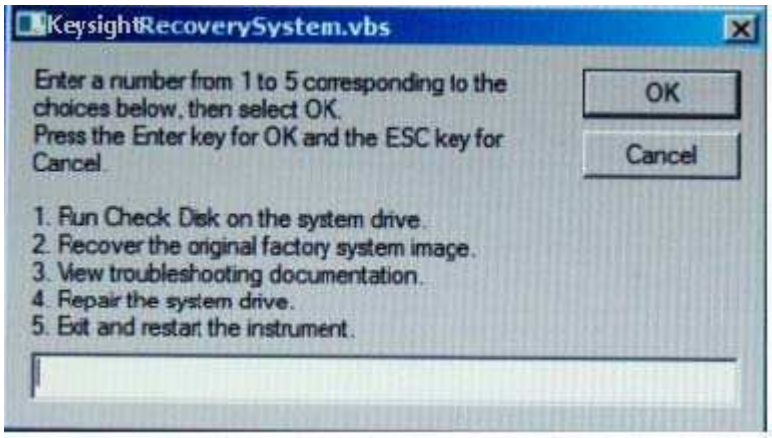
- Microsoft Windows 7 - This is the default selected option. This option starts the Logic Analyzer with the Windows 7 operating system. This is the normal startup of the system.
- Keysight Recovery system - You should select this option when you want to restore/repair your Logic Analyzer software by running the Keysight recovery process.



2 After a few seconds, Logic Analyzer automatically starts with the option selected in the Windows Boot Manager. Select the **Keysight Recovery system** option in the Windows Boot Manager screen using the arrow keys and then press Enter.

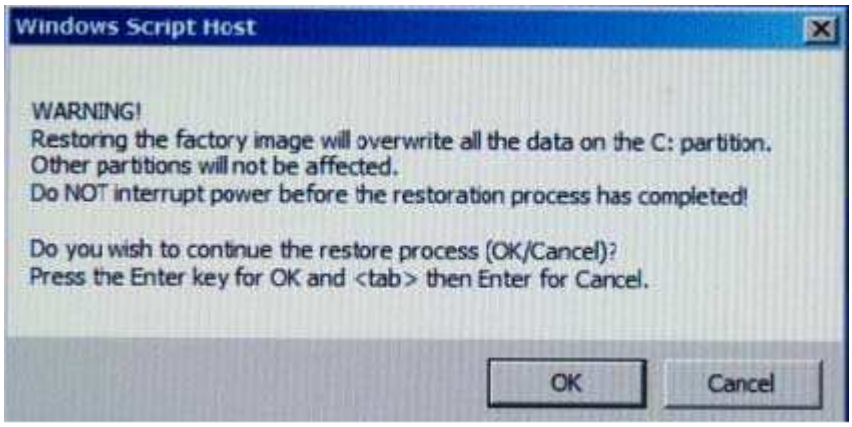
The recovery process starts preparing the system for recovery and displays the following screen with options to choose. You can enter:

- **1** to run Check Disk on the Logic Analyzer's hard disk drive. If the recovery process encounters any problems while running Check Disk, it reports these problems else it returns to the Keysight Recovery system prompt on completion of Check Disk.
- **2** to restore your Logic Analyzer software back to its original state in which it was shipped.
- **3** to view a document that provides information on the recovery process.
- **4** to repair the Logic Analysis system hard disk drive.
- **5** to exit the recovery process and restart the Logic Analyzer in the normal mode.



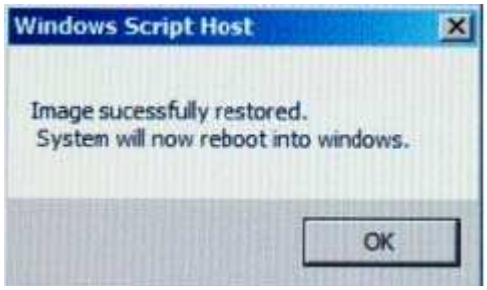
3 Select the second option in the above screen by entering **2** in the text box and clicking **OK**.

4 A warning message is displayed stating that the recovery process overwrites the data on C: drive. If you want to save your data to a CD or to another machine before you proceed further, then exit the recovery process and save your data. Else, click **OK** to proceed with the recovery process.



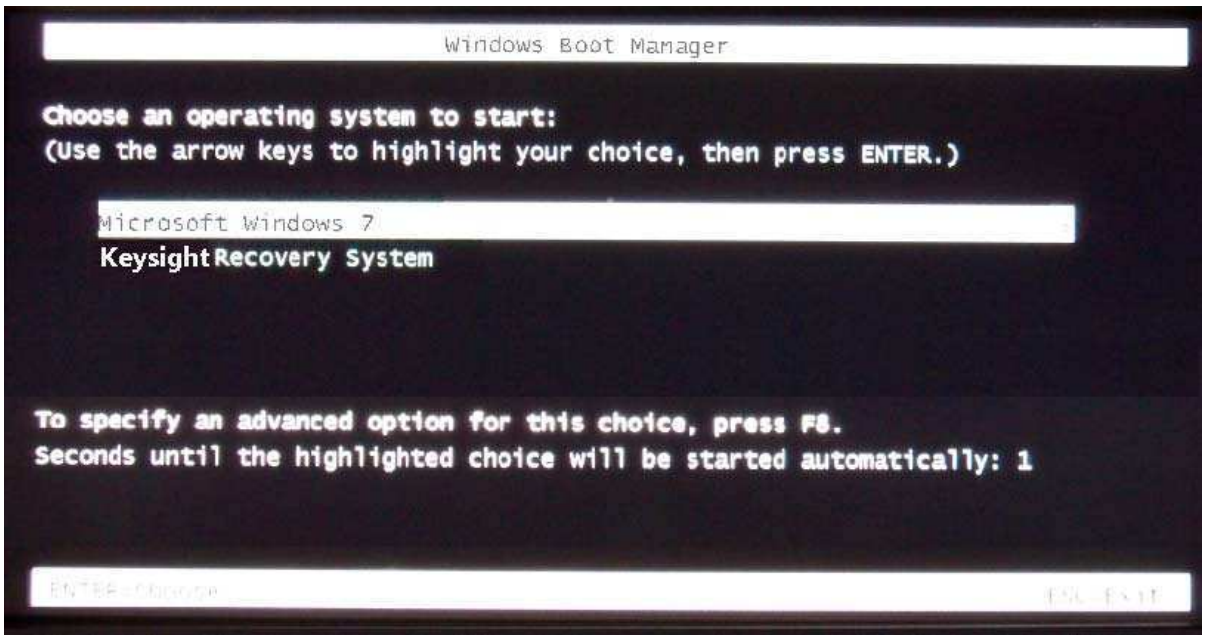
The recovery process starts.

If the recovery process is able to restore the system software successfully, then the following screen is displayed.



5 Click **OK** to proceed. You Logic Analysis system now reboots to Windows 7.

6 The Windows Boot Manager screen is displayed with Microsoft Windows 7 as the default selection. The system automatically starts with this default selection. Alternatively, you can press Enter to proceed with the default selection.



NOTE There are situations when you are not able to run the recovery process, (for instance, when the hard disk drive of your system fails) or when running the recovery process does not recover your system software. In such situations, you can send your Logic Analysis system for hard disk repair/replacement to Keysight. Alternatively, you can contact your nearest Keysight sales/service office. To locate a sales or service office, go to www.keysight.com/find/contactus.

Contacting Keysight Service/Support

To locate a sales or service office near you, go to: http://www.keysight.com/find/contactus

To test the logic acquisition cables

This test allows you to functionally verify the logic analyzer cable and the flying lead probe of any of the logic analyzer pods. Only one probe and cable can be tested at a time. Repeat this test for each probe and cable to be tested. Two Flying Lead Probes are required if you need to test pods other than Pod 1 because the clock from Pod 1 will be used to acquire data.

Table 12 Equipment Required to Test Cables

Equipment	Critical Specification	Recommended Model/Part
Pulse Generator	40 MHz, 3 ns pulse width, < 600 ps rise time	81134A Option 003
2 x 9 Test Connectors (Qty 2)	no substitute	See "To assemble the 2 x 9 test connectors" on page 92.
SMA m-m adapter (Qty 2)		Johnson 142-0901-811 SMA Plug to Plug or similar
Flying Lead Probe (Qty 2)	no substitute	HP or Keysight E5383A

To assemble the 2 x 9 test connectors

The 2 x 9 test connectors are used to connect all 16 channels and the clock of the logic analyzer to the pulse generator so you can test the flying lead probe and cables. (See "To test the logic acquisition cables" on page 92.)

Table 13 Materials Required for the 2 x 9 Test Connectors

Material	Critical Specification	Recommended Model/Part
Pin Strip Header (Qty 1, which will be separated)	.100" x .100" Pin Strip Header, straight, pin length.230", two rows,.120" solder tails, 2 x 40 contacts	3M 2380-6121TN or similar 2- row with 0.1" pin spacing
Jumper wire	<6 inches, approximately 22 gauge	
Resistor, 100 ohm 1% (Qty 4)		
SMA Board Mount Connector (Qty 2)		Johnson 142-0701-801 (see www.johnsoncomponents.com)

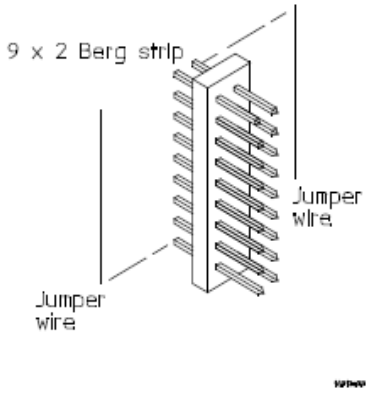
Build two test connectors using SMA connectors and 2-by-9 sections of pin strip.

1 Prepare the pin strip header:

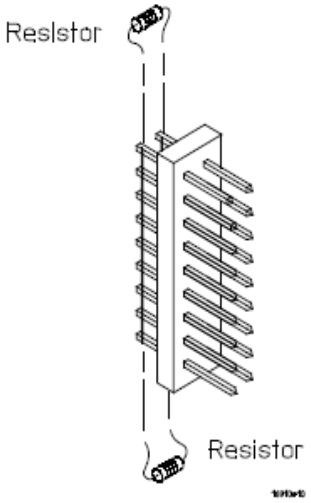
a Cut or cleanly break two 2 x 9 sections from the pin strip.

b Solder a jumper wire to all nine pins on one side of the pin strip.

c Solder a jumper wire to all nine pins on the other side of the pin strip.



d Solder two resistors to the pin strip, one at each end between the end pins.

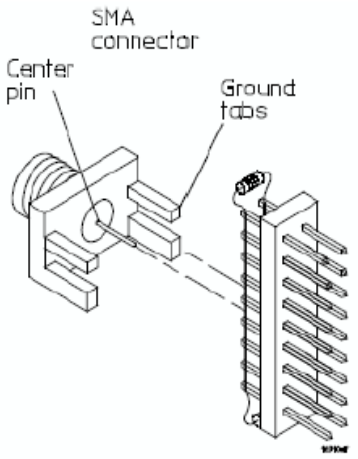


e Repeat for the second 2 x 9 pin strip.

2 Attach the SMA connector:

a Solder the center pin of the SMA connector to the center pin of one row on the pin strip.

b Solder the ground tab of the SMA connector to the pins of the other row on the pin strip.



c Repeat for the second 2 x 9 pin strip.

3 Check your work and de-flux the assemblies if desired.

Set up the test equipment

1 If you have not already done so, do the procedure "To run the self-tests" on page 82.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table:

Table 14 Pulse Generator Setup for Testing Cables

Timebase	Pulse Channel 2	Trigger	Pulse Channel 1
Mode: Int	Mode: Pulse ÷ 1	Disable (LED on)	Doesn't matter, not used in this test.
Freq: 40 MHz	Delay: (not available in pulse mode)		
	Width: 4 ns		
	Ampl: 3 V		
	Offs: 1.5 V		
	Output: Enable (LED off)		
	Comp: Normal (LED off)		
	Limit: Off (LED off)		
	$\overline{\text{Output}}$: Enable (LED off)		

Connect the test equipment

1 Using two 2 x 9 test connectors, connect the logic analyzer to the pulse generator channel outputs.

a Connect the even-numbered channels to the pulse generator Channel 2 OUTPUT.

b Connect the odd-numbered channels the pulse generator Channel 2 $\overline{\text{OUTPUT}}$.

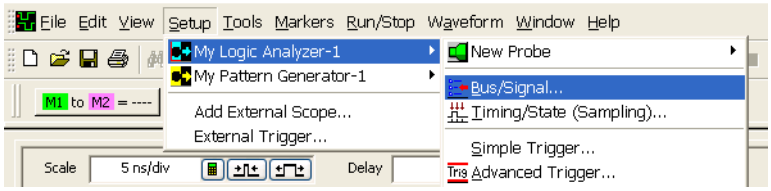
2 Connect Clk1 to the pulse generator Channel 2 $\overline{\text{OUTPUT}}$.
3 Enable the pulse generator Channel 1 and Channel 2 outputs (LEDs off).

Configure the logic analyzer to test Pod 1

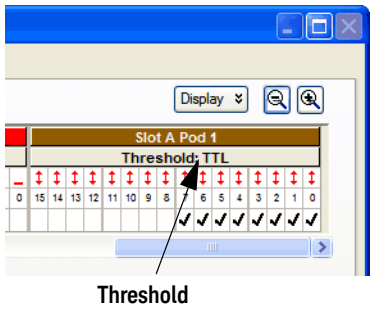
1 Exit the logic analysis application (from the main menu, choose **File→Exit**) and then restart the application. This puts the logic analyzer into its initial state.

2 Set up the bus and signals to test Pod 1.

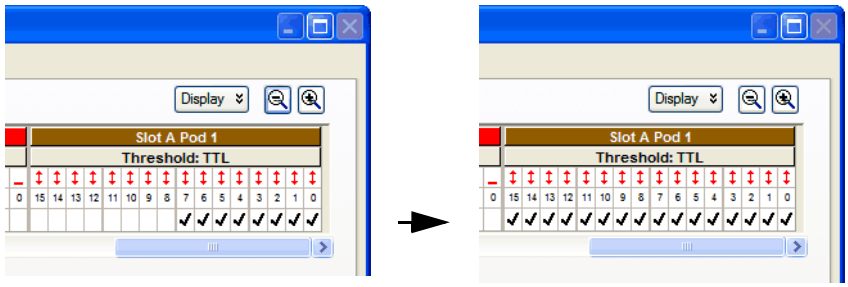
a From the *Keysight Logic Analyzer* application's main menu, select **Setup→Bus/Signal...** or **Setup→My Logic Analyzer-1→Bus/Signal...**.



b In the Analyzer Setup dialog, ensure that the **Threshold** button for Pod 1 is set to **TTL (1.50 V)**.

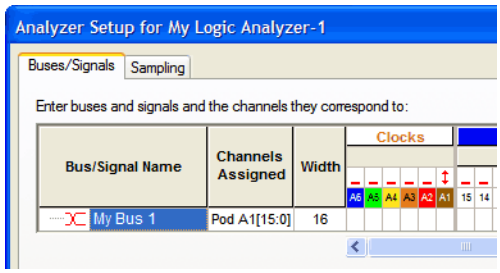


c Verify that the activity indicators (the red arrows) show activity on all 16 channels that are connected to the pulse generator.



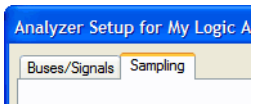
d Assign all channels. Hint: you can do this quickly by clicking on the left-most channel, then dragging to the right across all of the other channels. If you have a touch screen model (Option 103), you can touch the touchscreen and drag across with your finger.

e Drag the scroll bar all the way to the left and ensure that the activity indicator shows activity on clock 1.

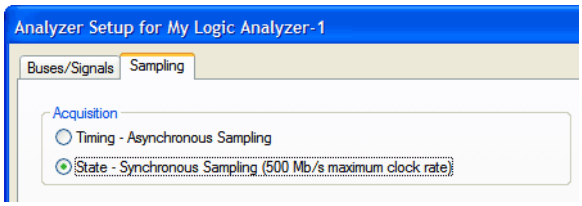


3 Set the sampling mode.

a Select the **Sampling** tab of the Analyzer Setup dialog.

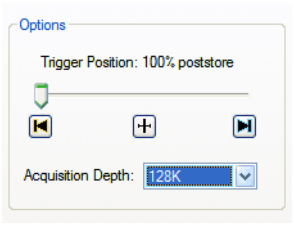


b Select **State - Synchronous Sampling**.

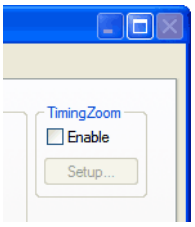


c Set the Trigger Position to **100% Poststore**.

d Set the Acquisition Depth to **128K**.



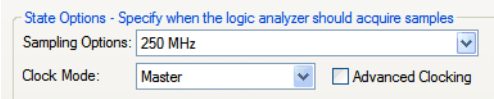
e Clear the Timing Zoom check box to turn Timing Zoom off.



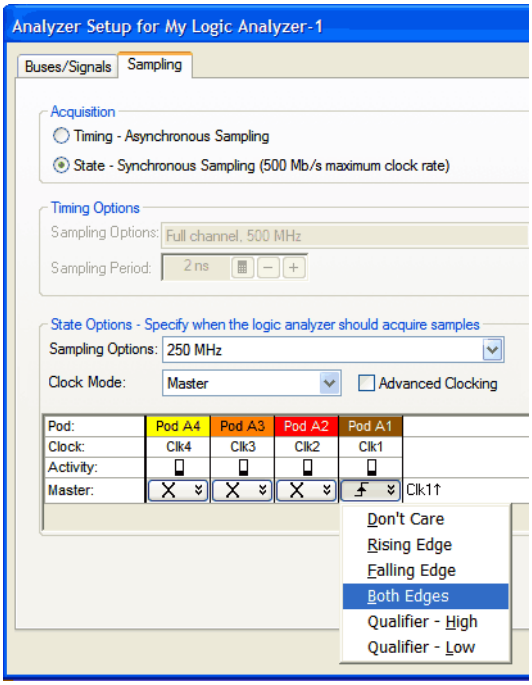
f Ensure that the sampling speed is set to **250 MHz** in the Sampling Options box.

NOTE If option 500 is not installed on the logic analyzer, then 250 MHz will be the only speed available.

g Ensure that the Clock Mode is set to **Master**.

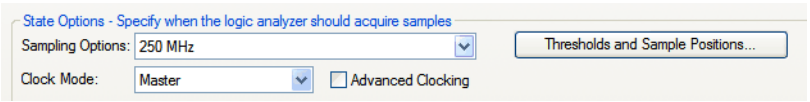


h Set the clock mode to **Both Edges**.

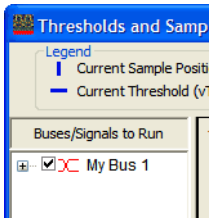


Adjust sampling positions using *eye finder*

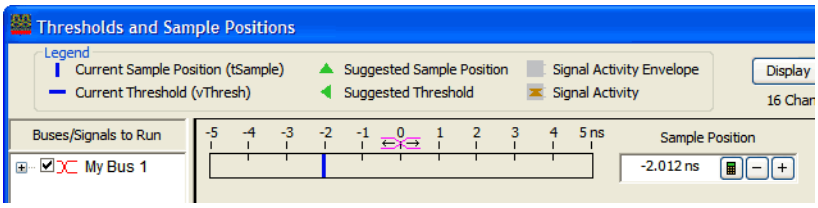
1 Select the **Thresholds and Sample Positions...** button. The Thresholds and Sample Positions dialog will appear.



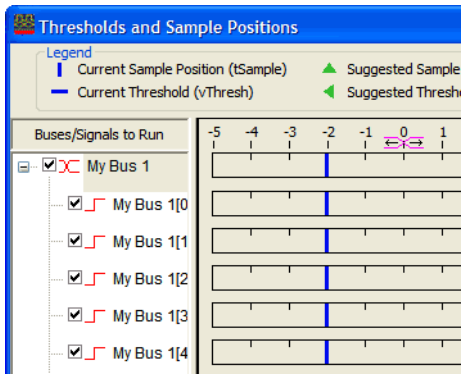
2 In the “Buses/Signals” section of the Thresholds and Sample Positions dialog, ensure that the check box next to “My Bus 1” is checked.



3 Drag the blue bar for “My Bus 1” to approximately -2 ns.

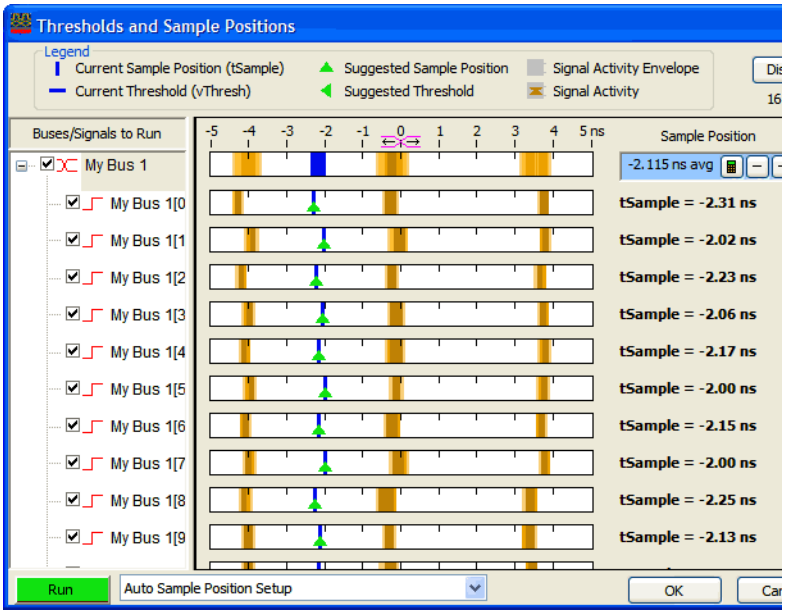


4 Select the plus sign to expand bus “My Bus 1”.



5 Click the **Run** button in the Thresholds and Sample Positions dialog.

6 Ensure that an eye appears for each bit. Depending on your test setup, the eye position may vary. Ensure that all blue bars in the individual channel rows (excluding the top row) are to the left of the orange transition region. If not, see “To re-align a stray channel" on page 48.



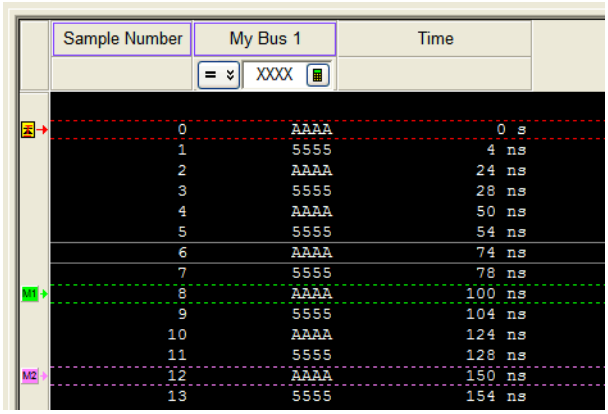
7 Click **OK** to close the Thresholds and Sample Positions dialog.

8 Click **OK** to close the Analyzer Setup dialog.

9 Switch to the Listing window by selecting the **Listing** tab at the bottom of the main window.

10 Click the Run icon .

11 Data appears in the Listing window upon completion of the run.



Sample Number	My Bus 1	Time
	= XXXX	
0	AAAA	0 s
1	5555	4 ns
2	AAAA	24 ns
3	5555	28 ns
4	AAAA	50 ns
5	5555	54 ns
6	AAAA	74 ns
7	5555	78 ns
8	AAAA	100 ns
9	5555	104 ns
10	AAAA	124 ns
11	5555	128 ns
12	AAAA	150 ns
13	5555	154 ns

12 If the listing shows that the data alternates between AAAA and 5555, then the probe and cable pass the test.

If the listing does not look similar to the figure, then there is a possible problem with the cable or probe tip assembly. Causes for cable test failures include:

- Open channel.
- Channel shorted to a neighboring channel.
- Channel shorted to either ground or a supply voltage.

Connect and configure the logic analyzer to test other pods

1 On the E5383A Flying Lead Probe set you have been using, move Clk1 to the pulse generator Channel 2 OUTPUT (from OUTPUT).

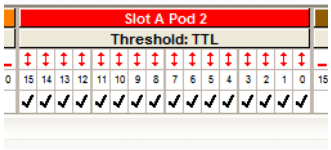
2 Disconnect the logic analyzer Pod 1 cable from the flying lead probe set and connect the logic analyzer Pod 2 cable.

3 Connect the second E5383A Flying Lead Probe set to the logic analyzer Pod 1 cable.

4 Connect the second flying lead probe set's Clk1 to the 2 x 9 test fixture at the pulse generator Channel 2 OUTPUT.

5 In the Analyzer Setup dialog's Buses/Signals tab, un-assign all channels of Pod 1.

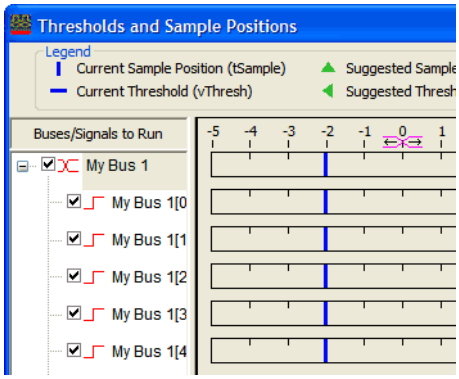
6 Assign all channels of the pod to be tested. If the pod to be tested has a clock, assign it too (place a check mark in the box under the channel name).



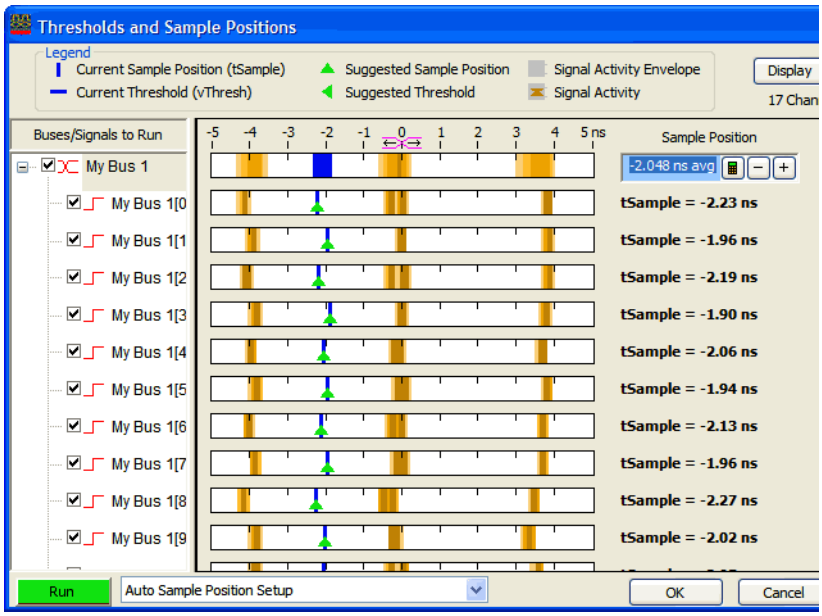
7 Select the Sampling tab.

8 Click the **Thresholds and Sampling Positions...** button.

9 Move the starting position to -2 ns.



10 Click **Run**, and ensure that an eye is found for each bit.

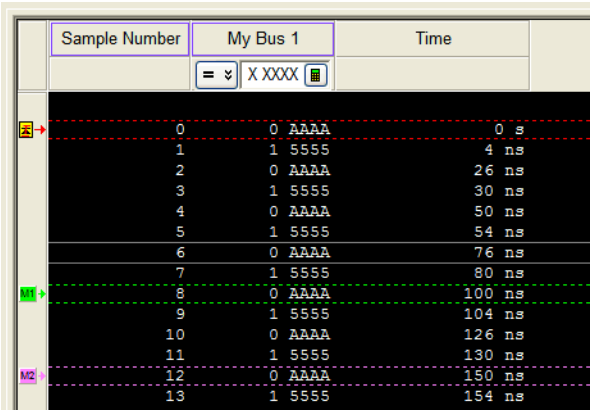


11 Click **OK** to close the Thresholds and Sample Positions dialog.

12 Click **OK** to close the Analyzer Setup dialog.

13 Switch to the Listing window and run the logic analyzer.

14 Examine the listing. If the listing shows that the data alternates between 0 AAAA and 1 5555, then the probe and cable pass the test.



If the listing does not look similar to the figure, then there is a possible problem with the cable or probe tip assembly. Causes for cable test failures include:

- Open channel.
- Channel shorted to a neighboring channel.
- Channel shorted to either ground or a supply voltage.

15 Perform the test on all remaining pods, always using both edges of Pod 1 Clk 1 to clock in the data.

16 Return to the troubleshooting flow chart.

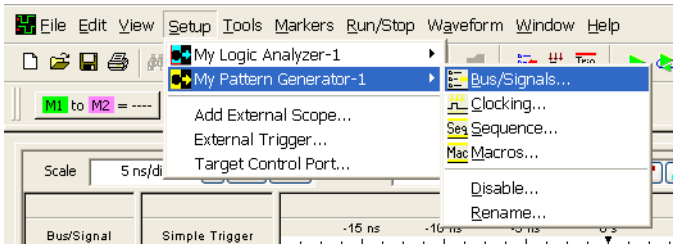
To verify pattern generator output

Table 15 Equipment Required to Verify Pattern Output

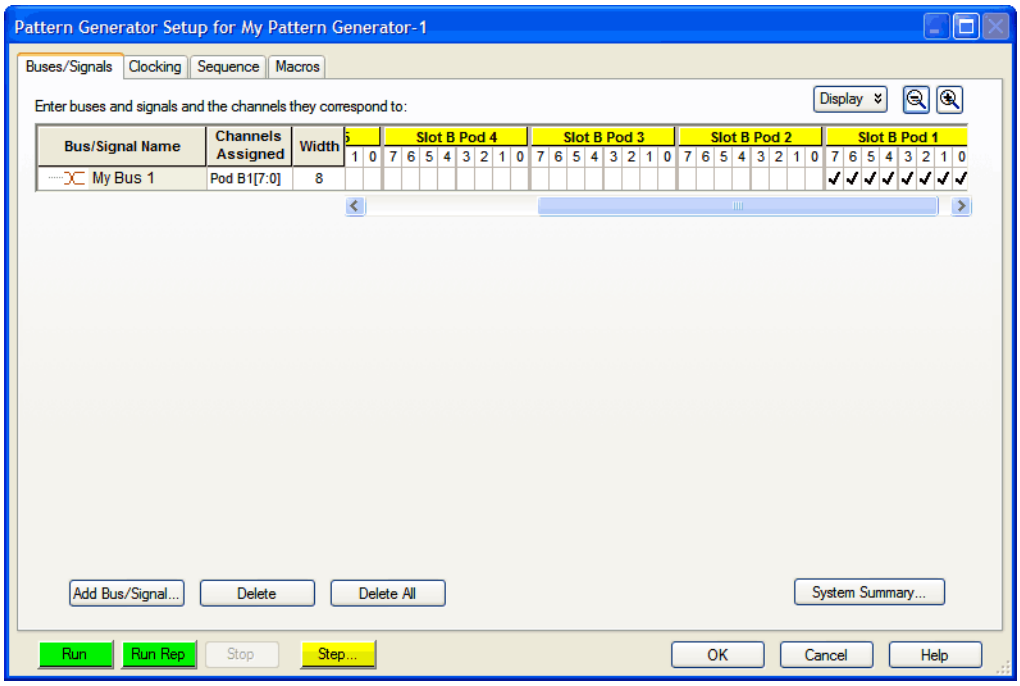
Equipment	Critical Specification	Recommended Model/Part
Oscilloscope	≥ 500 MHz Bandwidth	54820A
Probe	500 MHz Bandwidth	1160A
Output Data Pod	no substitute	10460A-series

1 Connect one of the 10460-series data pods to the end of the pattern generator Pod 1 cable.

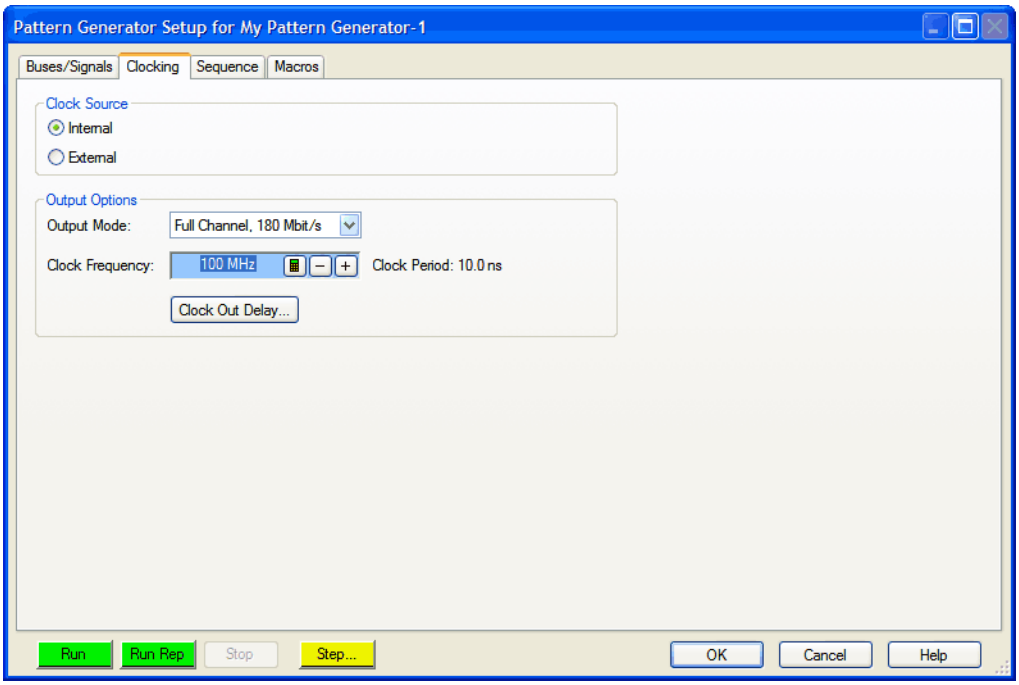
2 From the *Keysight Logic Analyzer* application's main menu, select **Setup→My Pattern Generator-1→Bus/Signals...**.



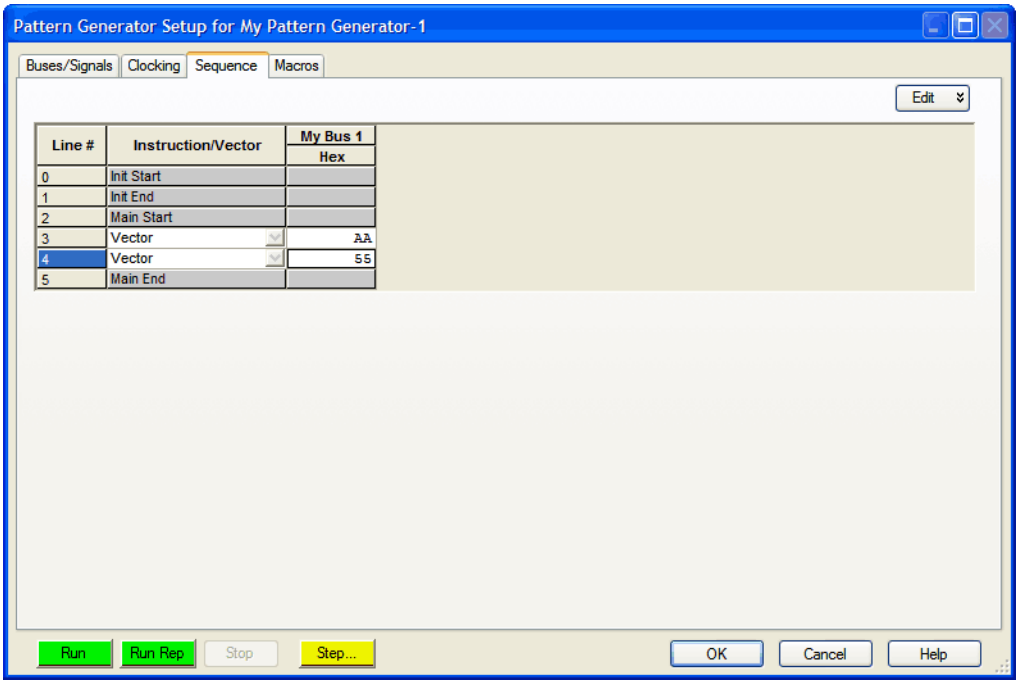
3 In the Pattern Generator Setup dialog's Buses/Signals tab, assign channels to Pod 1.



4 In the Clocking tab, select the Internal clock source and a Clock Frequency of 100 MHz.



5 In the Sequence tab, enter the two pattern vectors AA and 55 hex.



6 Click **Run Rep**.

7 Using an oscilloscope, verify the existence of logic-level transitions by touching the oscilloscope probe to each channel of Data Pod 1 and doing an Autoscale.

The signal levels that appear on the oscilloscope display should correspond with the logic levels represented by the 10460-series pod being used.

8 When you are done testing the pod channels, click **Stop** in the Pattern Generator Setup dialog.

9 Repeat steps 1 through 8 for each of the remaining data pods.

10 Connect one of the 10460-series clock pods to the end of the pattern generator clock cable.

11 Using the oscilloscope, as in step 7, verify the existence of logic-level transitions by touching the oscilloscope probe to each clock output of the clock pod.

12 When you are done testing the pod channels, click **Stop** in the Pattern Generator Setup dialog.

13 Click **OK** to close the Pattern Generator Setup dialog.

6 Replacing Assemblies

16800 Series Logic Analyzer Disassembly/Assembly

This chapter contains the instructions for removing and replacing the assemblies of the logic analyzer. Also in this chapter are instructions for returning assemblies.

WARNING Hazardous voltages exist on the power supply. To avoid electrical shock, disconnect power from the instrument before performing the following procedures. After disconnecting the power, wait at least six minutes for the capacitors on the power supply board to discharge before servicing the instrument.

CAUTION Damage can occur to electronic components if you remove or replace assemblies when the instrument is on or when the power cable is connected. Never attempt to remove or install any assembly with the instrument on or with the power cable connected.

Replacement Strategy

Some procedures in this section tell you to remove other assemblies of the instrument, but do not give complete instructions. In these cases, refer to the procedure for that specific assembly for the instructions. The drawings here are representative. Your parts may look different.

CAUTION Electrostatic discharge can damage electronic components. Use grounded wrist straps and mats when performing any service to this logic analyzer.

Tools Required

- T6, T10, T15, T25 TORX screwdrivers.
- #1 Pozi-drive screwdriver.
- 13/16 inch, deep-well nut driver.
- 5 mm nut driver.
- 1/4-inch hollow-shaft nut driver.

To save the license file

Before doing any major repairs to the instrument, it is recommended that you back up any data and license files to a USB flash drive if possible. You will need a backup copy if you encounter any problems that require re-imaging the hard drive.

The license files contain keys for licensed software features, and is located in the directory:

C:\Program Files\Keysight Technologies\Logic Analyzer\License\

C:\Program Files\Keysight Technologies\License Server\License Files

If for some reason, you lose the license file, you can obtain new licenses from Keysight, given the licensing host ID.

To obtain the licensing host ID

From the *Keysight Logic Analyzer* application's main menu, choose **Help>Software Licensing...**. The Licensing Host ID is displayed in the Software Licensing dialog's Activation tab.

To prepare the instrument for disassembly

Do this procedure before doing any disassembly procedure on the instrument.

1 Close the *Keysight Logic Analyzer* application.
2 Power off the system using one of the methods explained below.
3 Remove the power cord.
4 Move the instrument to a static safe work environment.

WARNING Hazardous voltages exist on the power supply. To avoid electrical shock, disconnect power from the instrument before performing the following procedures. After disconnecting the power, wait at least six minutes for the capacitors on the power supply board to discharge before servicing the instrument.

CAUTION Damage can occur to electronic components if you remove or replace assemblies when the instrument is on or when the power cable is connected. Never attempt to remove or install any assembly with the instrument on or with the power cable connected.

To power off the system

There are several ways to power off the logic analyzer.

NOTE When powering off the logic analyzer, wait until the fans stop turning (about 15 seconds) before turning the logic analyzer back on. This ensures that internal circuitry restarts in a known state.

Using the Windows Shutdown

On the logic analyzer desktop click **Start>Shut Down** or if you are running remote desktop, click **Start>Settings>Windows Security>Shut Down**. This software power off does the following:

- Closes all programs that are running.
- Writes all data to the disk.
- Turns off the power supply.
- If the system is unplugged while it is off and then plugged back in, the system will not power on until the power button is pressed.

Using a Short Press of the Power Button

Pressing the power button on a frame for a short time (less than 2 seconds or so):

- Closes all programs that are running.
- Writes all data to the disk.
- Turns off the power supply.

If the power button is depressed for a short time (less than 2 seconds or so) while another instrument has an open Remote Desktop connection to this instrument, a message on the logic analyzer screen (not on the remote desktop) will pop up asking if you really want to power down. Clicking the 'yes' button results in the above events. Clicking 'no' will prevent the shutdown and not answering the dialog box (neither clicking "Yes" or "No") will have no effect. Further short presses on the power button will have no effect.

Using a Long Press of the Power Button

Pressing the power button for more than 4 seconds will power the system down abruptly. Use this method only when other methods have not responded:

- Programs that are running will not be shut down. Any data that has not been written to the disk will be lost.
- Turns off the power supply.
- If the system is unplugged while it is off and then plugged back in, the system will not power on until the power button is pressed.
- If the system does not boot, the hard disk drive will need to be re-imaged.

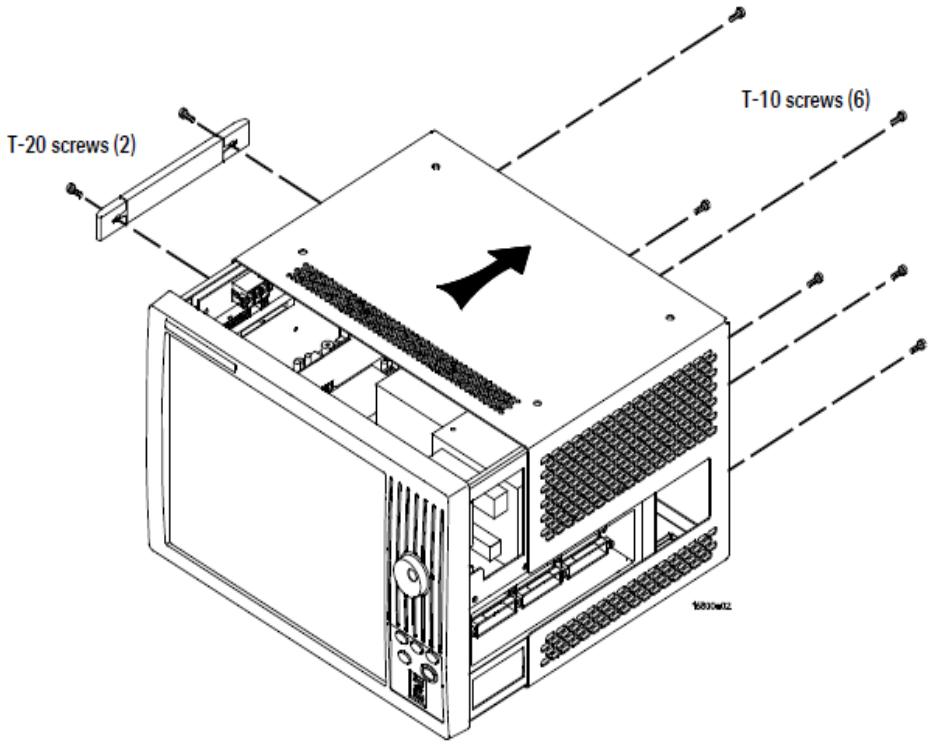
Unplugging the Power Cord or Power Loss

Unplugging power while the instrument is turned on or a power loss is similar to the long press of the power button with one exception:

- When the system is plugged back in, it will power up and boot into Windows.

To remove and replace the cover

1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
2 Using a Torx T20 screwdriver, remove the handle assembly.
3 Using a Torx T10 screwdriver, remove 6 screws that secure the cover to the chassis.
4 Slide the cover back to remove.



5 Reverse this procedure to replace the cover.

CAUTION When reinstalling the handle assembly, ensure that the screws are torqued to 2.372 Newton meters (21 inch pounds) so that they do not work themselves loose.

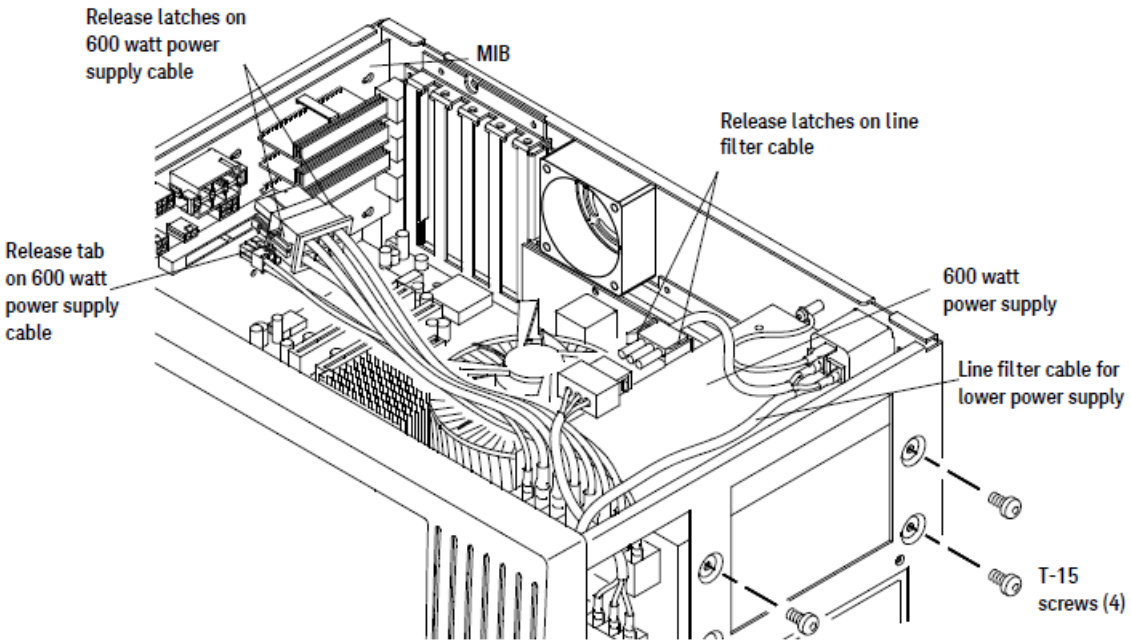
To remove and replace the power supplies

WARNING Hazardous voltages exist on the power supply. To avoid electrical shock, disconnect the power from the instrument before performing the following procedures. After disconnecting the power, wait at least six minutes for the capacitors on the power supply board to discharge before servicing the instrument.

600 watt power supply

The 600 watt power supply is on all models but may look different than the one shown here.

1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
   - "To remove and replace the cover" on page 111.
2 Press the release latches on the sides of the connector to disconnect the top 600 watt power supply cable from the module interface board (MIB).
3 Press the single release tab to disconnect the lower 600 watt power supply cable from the MIB.
4 Press the release latches to disconnect the 600 watt line filter cable.

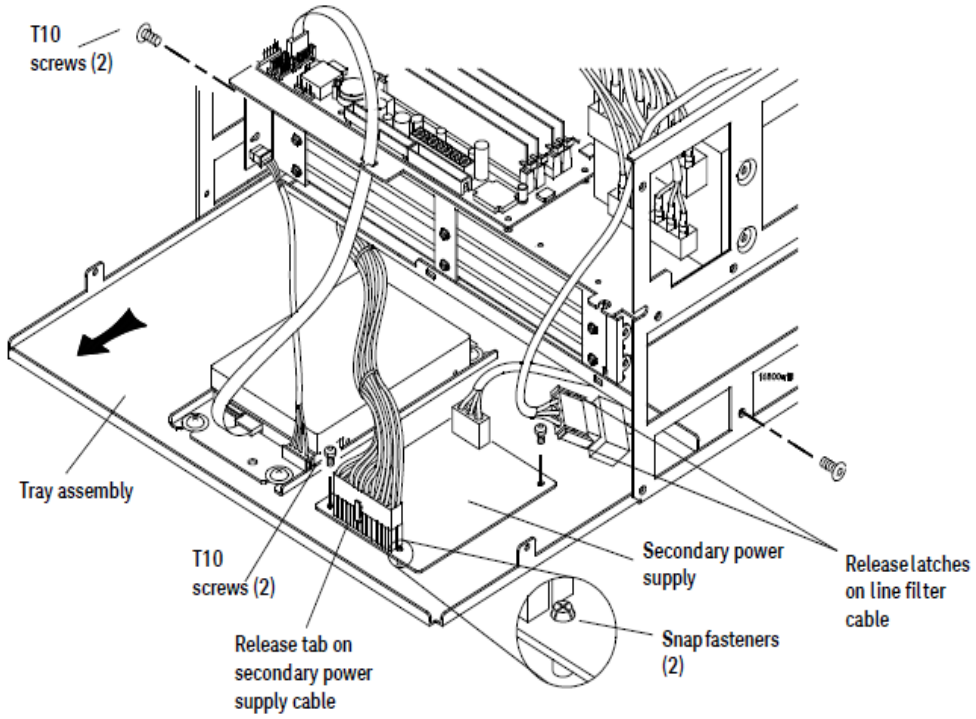


5 Using Torx T20 screwdriver, remove the 4 screws that secure the 600 watt power supply to the chassis.
6 Slide the power supply toward the front panel and lift it out of the frame while holding the line filter cable for the lower power supply out of the way.
7 Reverse this procedure to replace the 600 watt power supply.

Secondary power supply

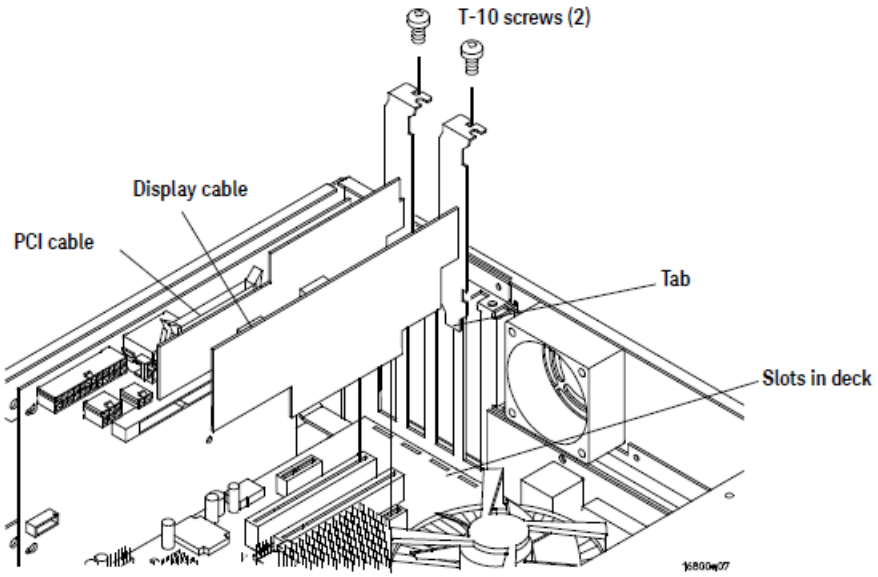
Depending on the model you ordered, your secondary power supply may be 175 watts or 15 watts and may look different than the one shown here.

1 Perform the procedures:
   - "To prepare the instrument for disassembly" on page 109.
   - "To remove and replace the cover" on page 111.
   - "To remove and replace the front panel assembly" on page 117.
2 Using a Torx T10 screwdriver remove the 2 side screws securing the tray assembly to the frame.
3 Slide the tray out far enough to disconnect the following cables:
   - Line filter cable for 600 watt power supply (press release latches).
   - Secondary power supply cable (press release tab).
4 Using a Torx T10 screwdriver, remove the 2 screws that secure the secondary power supply to the tray.
5 Snap the power supply off the tray assembly (see enlargement of snap-in fastener).
6 Reverse this procedure to install the power supply.



To remove and replace the PCI or display board

1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
   - "To remove and replace the cover" on page 111.
2 Disconnect the cable from the board you are replacing.
3 Using a Torx T10 screwdriver, remove the screws securing the board to the rear panel.
4 Lift the board out of the socket to remove.

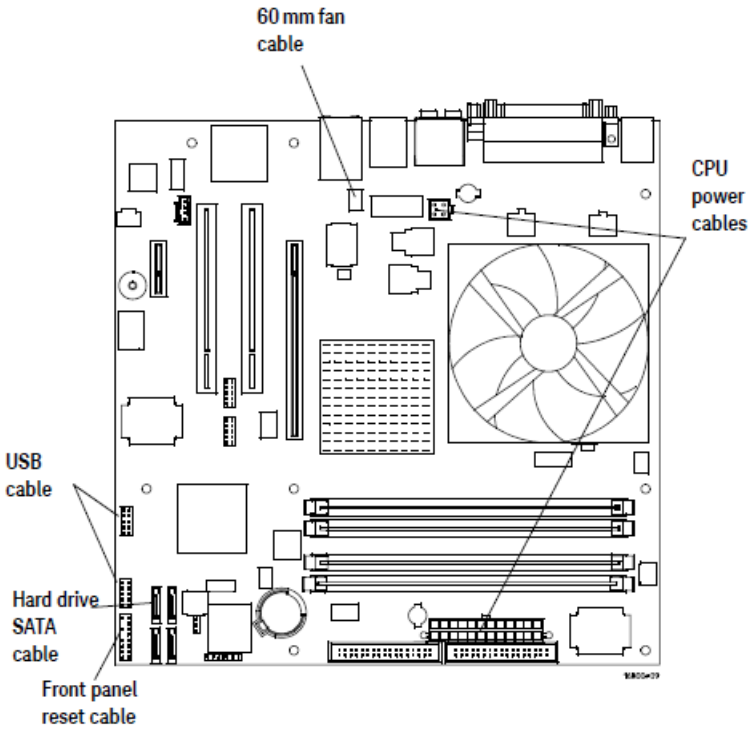


5 To replace a board:
   a Ensure that the tab on the board's rear panel is aligned with the slot in the deck.
   b Press the board securely into the socket on the motherboard.
   c Replace the screw.

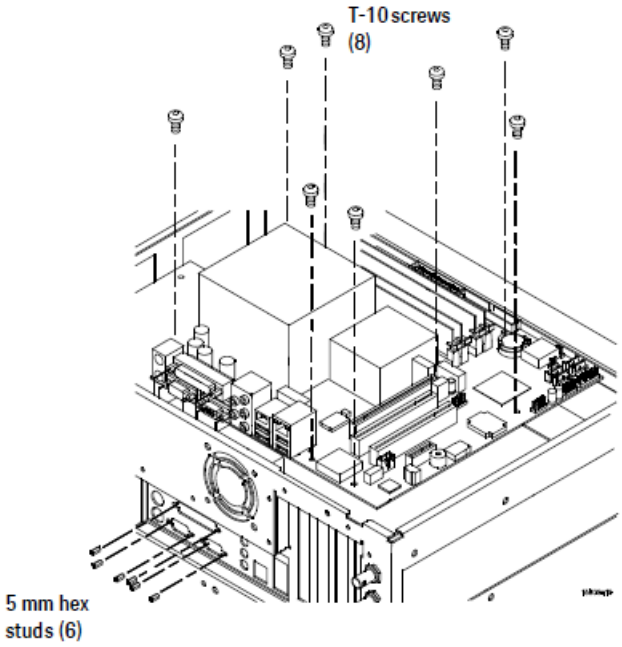
To remove and replace the motherboard

The following graphics of the motherboard are representative. Yours may look different.

1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
   - "To remove and replace the cover" on page 111.
   - "To remove and replace the PCI or display board" on page 114.
2 Disconnect the following cables from the motherboard:
   - 60 mm fan cable.
   - CPU power cables.
   - USB cables.
   - Hard drive SATA cable.
   - Front panel reset cable.



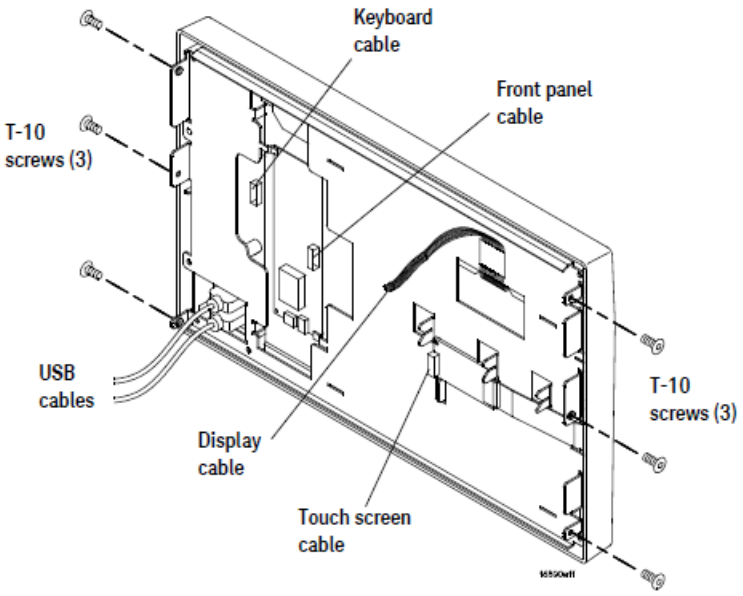
3 Using a 5 mm hex nut driver, remove the 6 Hex Studs securing the connectors to the rear panel.
4 Using a Torx T10 screwdriver, remove the 8 screws that secure the motherboard to the deck.



5 Reverse this procedure to install the motherboard.

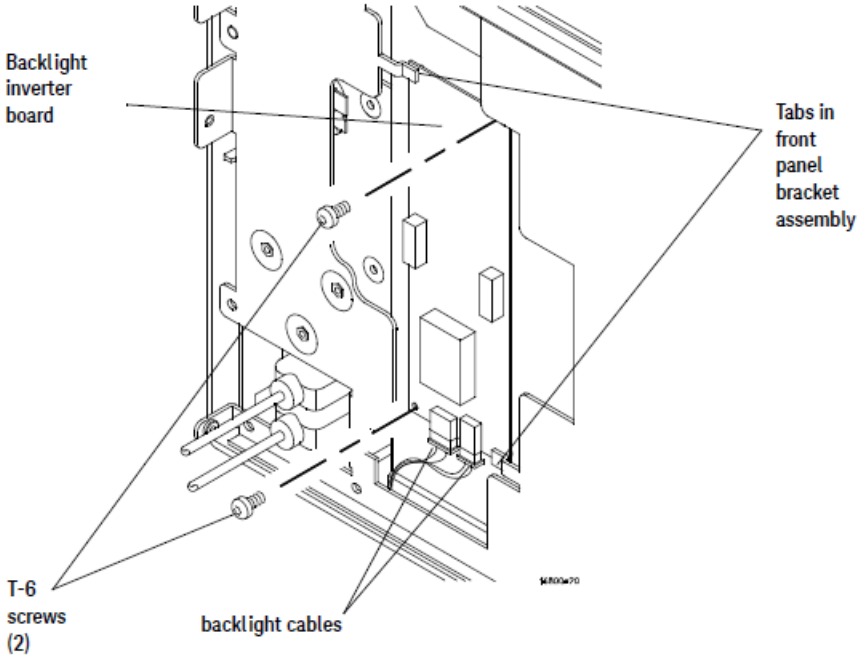
To remove and replace the front panel assembly

1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
   - "To remove and replace the cover" on page 111.
2 Disconnect the following cables:
   - USB cables from the motherboard.
   - Display cable from the display board (use care when disconnecting to avoid damage).
   - Optional touch screen cable from the touch screen controller board.
   - Keyboard cable from the keypad board.
   - Front panel cable from the backlight inverter board.
3 Using a Torx T10 screwdriver, remove 6 screws that secure the front panel to the chassis.
4 Remove the front panel assembly.
5 Reverse this procedure to install the front panel assembly.



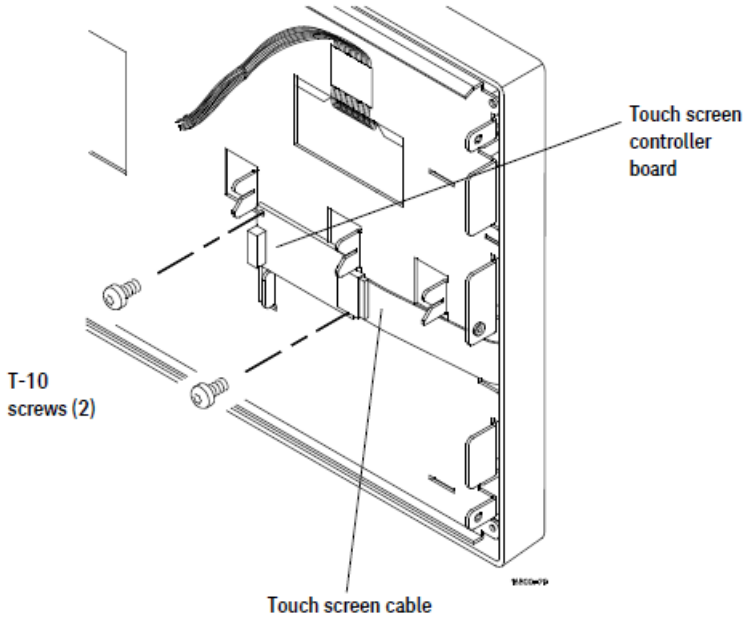
To remove and replace the backlight inverter board

1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
   - "To remove and replace the cover" on page 111.
   - "To remove and replace the front panel assembly" on page 117.
2 Disconnect the backlight cables from the inverter board.
3 Using a Torx T6 screwdriver, remove the 2 screws securing the board to the front panel.
4 Slide the inverter board out from under the tabs in the front panel bracket assembly.
5 Reverse this procedure to install the backlight inverter board.



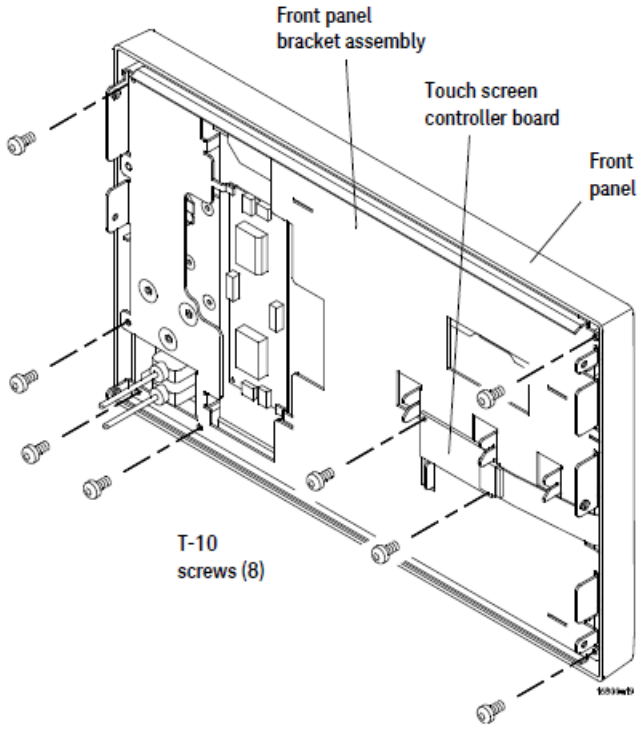
To remove and replace the touch screen controller board

1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
   - "To remove and replace the cover" on page 111.
   - "To remove and replace the front panel assembly" on page 117.
2 Disconnect the touch screen cable from the touch screen controller board.
3 Using a Torx T10 screwdriver, remove the 2 screws securing the board to the front panel board.
4 Reverse this procedure to install the touch screen controller board.



To remove and replace the front panel bracket assembly

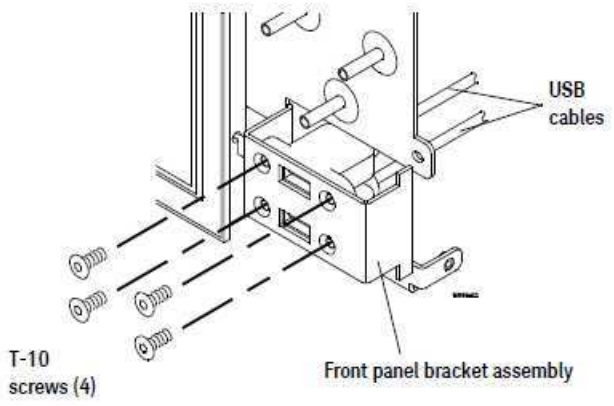
1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
   - "To remove and replace the cover" on page 111.
   - "To remove and replace the front panel assembly" on page 117.
2 Using a Torx T10 screwdriver, remove the 2 screws securing the touch screen controller board to the front panel bracket assembly.
3 Using a Torx T10 screwdriver, remove the 6 screws securing the front panel bracket assembly to the front panel.
4 Remove the bracket assembly.



5 Reverse this procedure to replace the front panel bracket assembly.

To remove and replace the USB cables

1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
   - "To remove and replace the cover" on page 111.
   - "To remove and replace the front panel assembly" on page 117.
   - "To remove and replace the front panel bracket assembly" on page 120.
2 Using a Torx T10 screwdriver, remove the 4 screws securing the USB cables to the front panel bracket assembly.

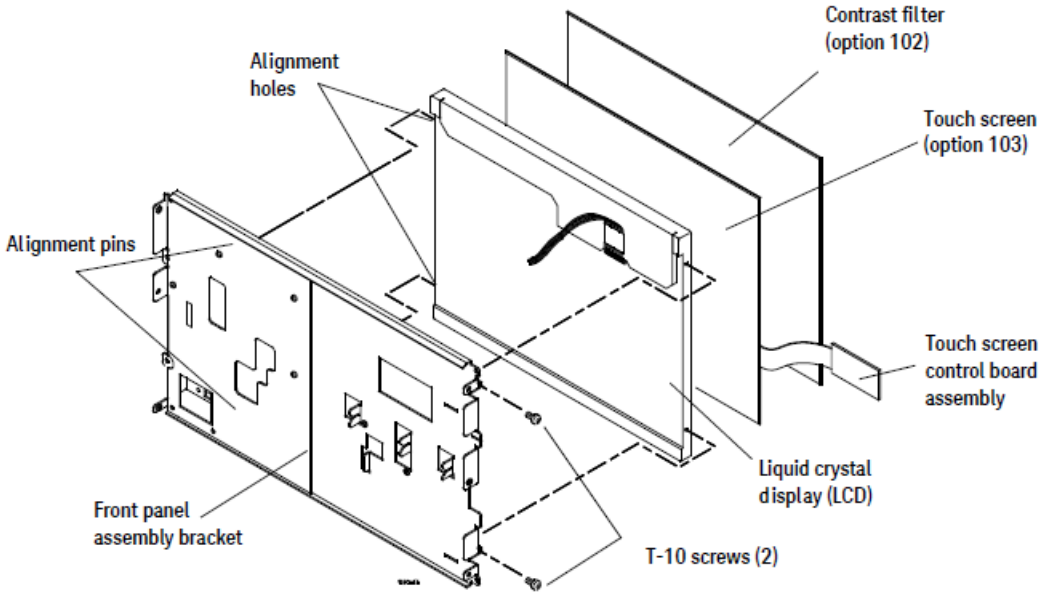


3 Reverse this procedure to replace the USB cables.

To remove and replace the display assembly

Your logic analyzer may have either a contrast filter or a touch screen depending on the option you ordered.

1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
   - "To remove and replace the cover" on page 111.
   - "To remove and replace the front panel assembly" on page 117.
   - "To remove and replace the backlight inverter board" on page 118.
   - "To remove and replace the front panel bracket assembly" on page 120.
2 Using a Torx T10 screwdriver, remove the 2 screws securing the display assembly to the front panel bracket assembly.
3 Remove the alignment pins on the bracket from the holes on LCD.



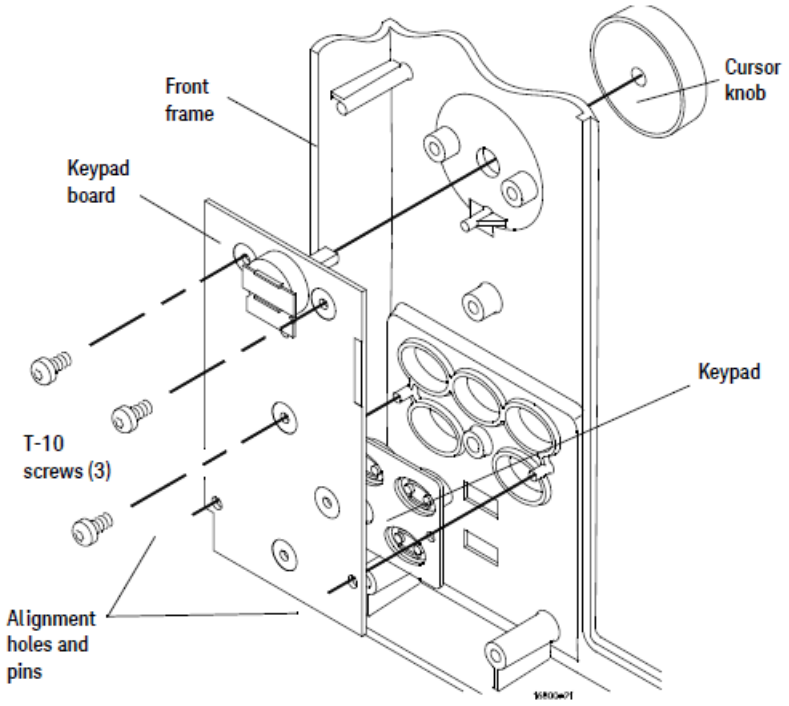
CAUTION Handle the touch screen and LCD display by the edges only. If necessary, clean with alcohol and a lint-free wipe or remove any airborne contamination with ionized air.

4 If you have the contrast filter, it sets in a groove in the front panel.
5 If you have the touch screen option, gently pry the touch screen from the LCD. It is held on with double-sided tape.
6 Reverse this procedure to replace the display assembly.

To remove and replace the keypad and keypad board

1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
   - "To remove and replace the cover" on page 111.
   - "To remove and replace the front panel assembly" on page 117.
2 Pull to remove the cursor knob from the front of the frame.
3 Using a Torx T10 screwdriver, remove the 3 screws securing the keypad board to the front frame.
4 Remove the keypad board and keypad from the frame.

CAUTION Wear ESD finger cots or use care not to touch the black pads on keypad and on the keypad board. Finger oils can impair contact. If necessary, carefully clean the contacts using alcohol and lint-free swabs or wipes.

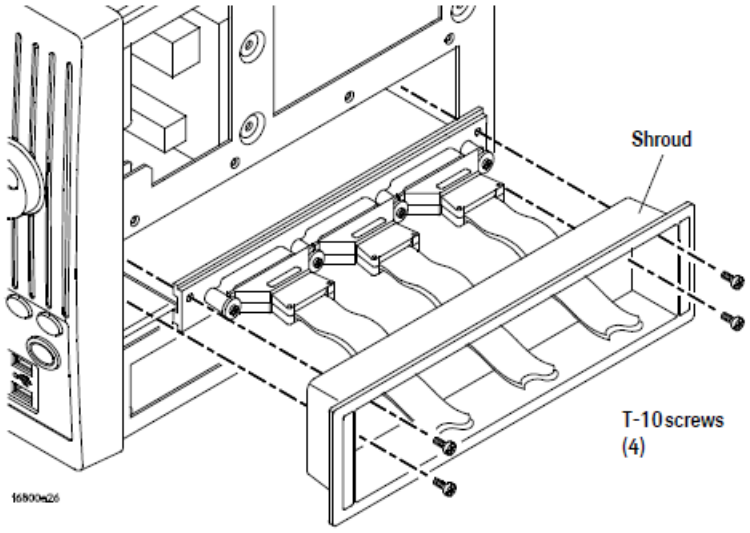


5 Reverse this procedure to install the keypad and keypad board. Note the alignment pins on the frame and the holes in the board.

To remove and replace a measurement card

Your product may consist of 1 or 2 measurement cards.

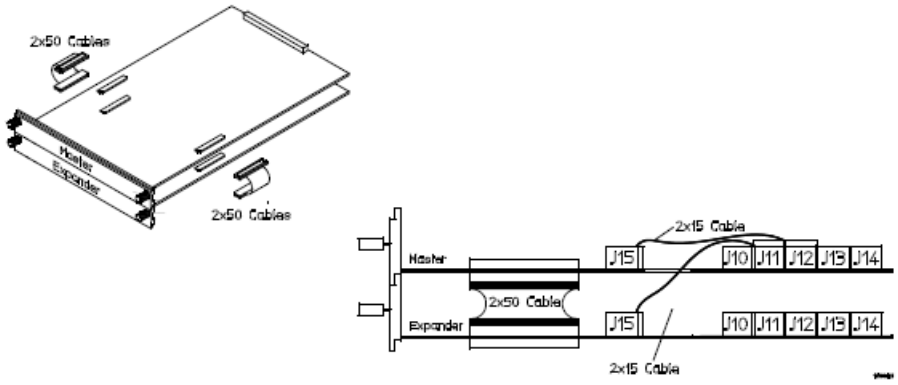
1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
2 Use a Torx T10 screwdriver to remove the 4 screws securing the shroud to the frame.
3 Slide the shroud over the cables.
4 Use a gentle back-and-forth motion as you pull to disconnect the card(s) from the connector on the module interface board and then pull the card(s) out of the frame.



5 Replace the measurement card(s).

   If there is a pattern generator card in the frame, it always goes in the lower position. If there are two logic analyzer cards in the frame, the expander card goes in the lower position.

   a If your model has two logic analyzer (measurement) cards, connect them as shown.



b Seat the lower card first.

c Press firmly to ensure the cards are fully seated in the connector on the module interface board.

d Slide the shroud over the cables.

e Use a Torx T10 screwdriver and 4 screws to secure the shroud to the frame.

To remove and replace measurement cables

1 Use a Torx T10 driver to remove the screws that secure the measurement cable(s) to the back panel of the card.

2 Gently pull the measurement cable end connector(s) from the circuit board connector(s).

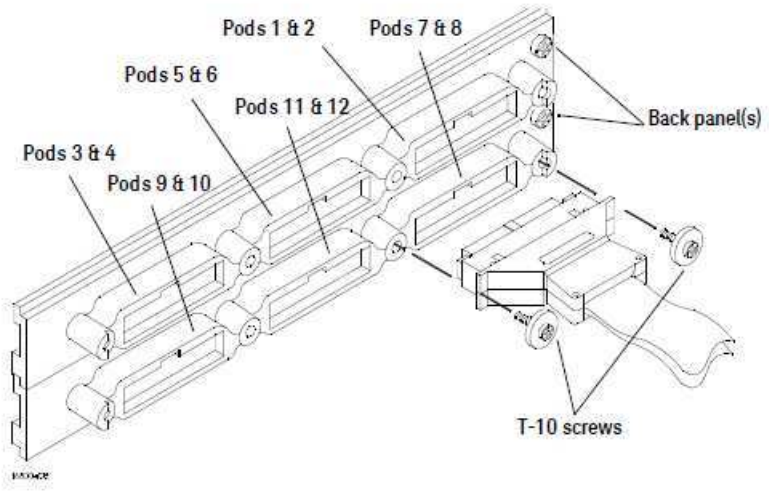
3 If a measurement cable is faulty, replace the cable.

If you order a measurement cable, you also need to order new labels. Probe cables shipped with the card are already labeled. For part numbers and ordering information, see "Measurement Card Replaceable Parts List" on page 148.

4 Connect the measurement cable(s).

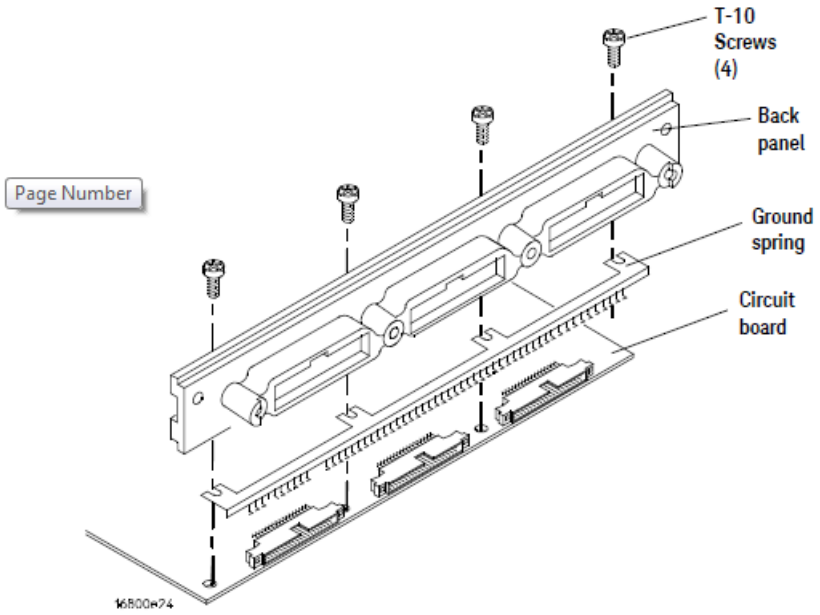
a Align the logic analyzer cable end connector with the circuit board connector and gently apply pressure to seat the cable.

b Install the Torx T10 screws (two per cable) and tighten to 5 in/lb to secure the cable to the back panel of the card.



To remove and replace a measurement circuit board

1 Remove the 4 screws attaching the ground spring and back panel to the circuit board, then remove the back panel and the ground spring.



Page Number

2 Replace the faulty circuit board with a new circuit board. On the new board, ensure the 2x15 (30-pin) ribbon cable is connected between J15 and J12.

3 Position the ground spring and back panel on the back edge of the replacement circuit board. Install 4 screws to connect the back panel and ground spring to the circuit board.

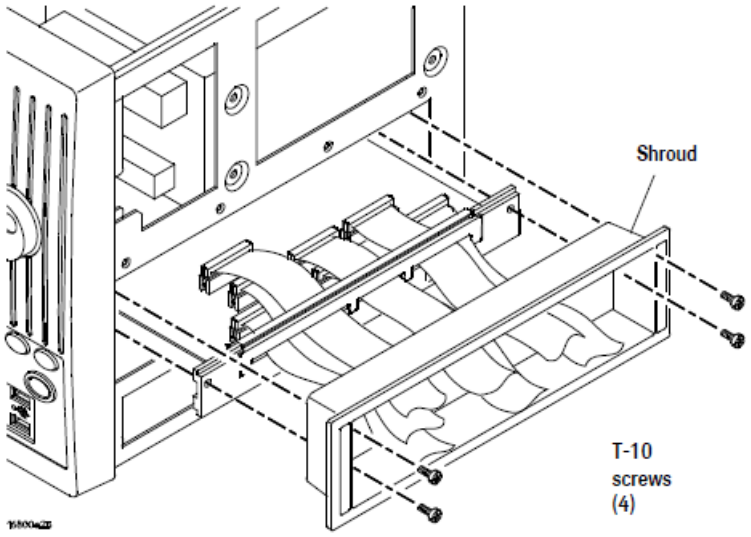
4 Install the logic analyzer cables using the procedure "To remove and replace measurement cables" on page 125.

5 Install the logic analyzer card using the procedure "To remove and replace a measurement card" on page 124.

To remove and replace a pattern generator card

Your product may consist of 1 pattern generator card and 1 measurement card.

1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
2 Use a Torx T10 screwdriver to remove the 4 screws securing the shroud to the frame.
3 Slide the shroud over the cables.
4 Use a gentle back-and-forth motion as you pull to disconnect the cards from the connector on the module interface board and then pull the cards out of the frame.



5 Replace the cards.
   a Seat the lower card first. The pattern generator card goes in the lower position.
   b Press firmly to ensure the cards are fully seated in the connector on the module interface board.
   c Slide the shroud over the cables.
   d Use a Torx T10 screwdriver and 4 screws to secure the shroud to the frame.

To remove and replace the pattern generator probe cable

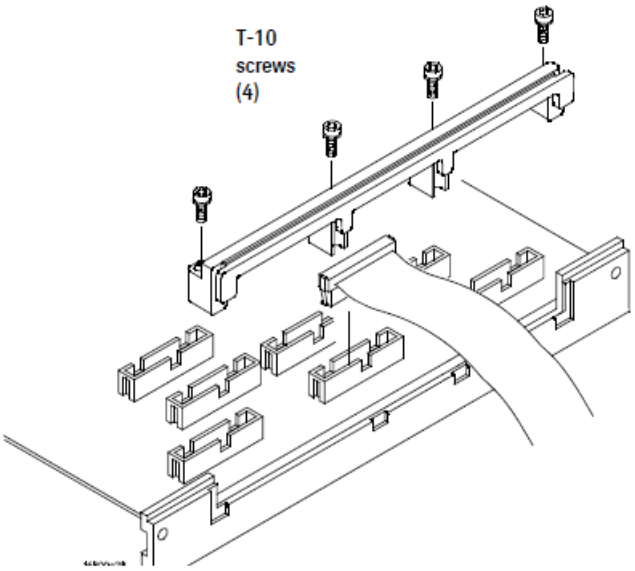
1. Use a Torx T10 screwdriver to remove the screws that hold the cable clamp to the back panel of the card.
2. Remove the faulty probe cable from the connector and install the replacement cable.
3. Install the label on the new probe.

   If you order a new probe cable, you also need to order new labels. Probe cables shipped with the card are already labeled. For part numbers and ordering information, see "Pattern Generator Card Replaceable Parts" on page 150.
4. Install the 4 screws that secure the cable clamp to the back panel of the card.
5. Reverse this procedure when replacing the cards.

   The pattern generator card goes in the lower position.

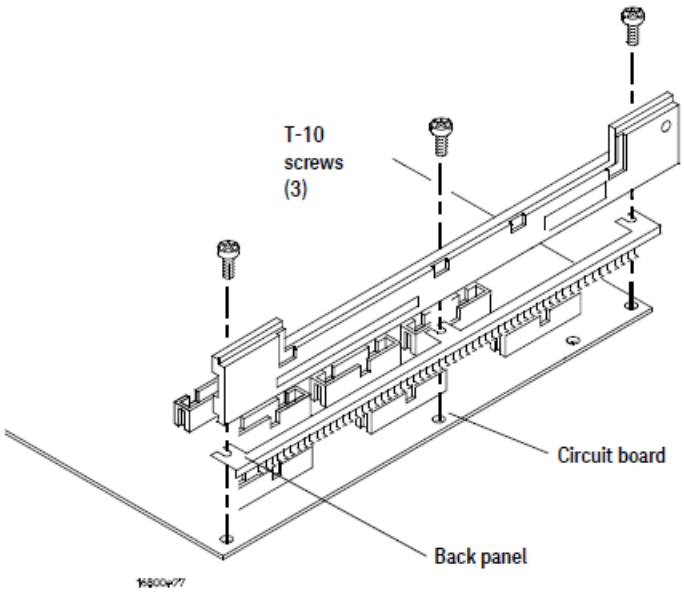
   a. Seat the lower card first.

   b. Press firmly to ensure the cards are fully seated in the connector on the module interface board.



To remove and replace the pattern generator circuit board

1 Use a Torx T10 screwdriver to remove the 3 screws attaching the back panel and ground spring to the circuit board, then remove the back panel and ground spring.
2 Replace the faulty circuit board with a new circuit board. On the circuit board, ensure the 20-pin ribbon cable is connected between J7 and J8.
3 Position the ground spring and back panel on the back edge of the replacement circuit board. Install 3 screws to connect the back panel and ground spring to the circuit board.
4 Install the cables and cable clamp using the procedure "To remove and replace the pattern generator probe cable" on page 128.
5 Install the pattern generator card using the procedure "To remove and replace a pattern generator card" on page 127.



To replace the hard disk drive

In case of a hard disk failure, you send your Logic Analyzer unit to Keysight for repair/replacement of the failed/defective hard disk. See "Returning Assemblies" on page 136 to know more about how to return the unit to Keysight for repair.

If you have a 16800 series Logic Analyzer with Windows XP installation

For 16800 series logic analyzers with Windows XP installation, the replaced hard disk (part number 0950-5301) does not have the operating system or the Logic Analyzer software pre-installed. Therefore, once you get back your logic analyzer with the replaced hard disk, you need to:

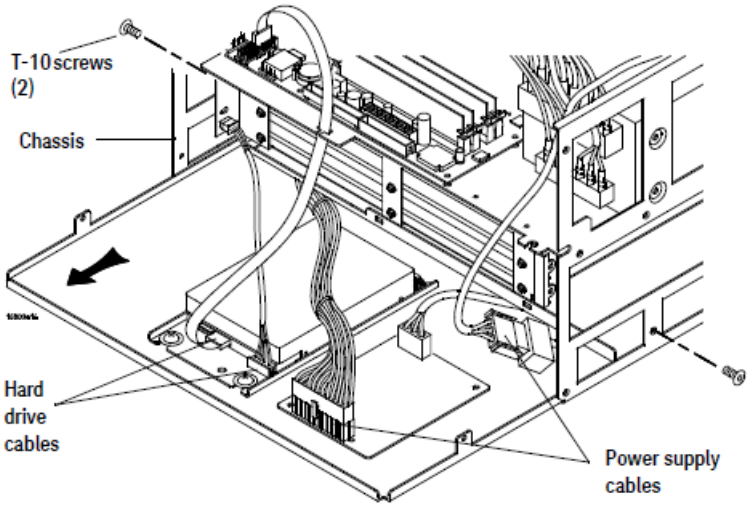
- first restore your system software, see "To restore the system software" on page 88.
- then install the Logic Analyzer software from www.keysight.com/find/la-sw-download.

If you have a 16800 series Logic Analyzer with Windows 7 installation

For 16800 series logic analyzers with Windows 7 installation, the replaced hard disk (part number 16800-68712) will come preformatted and preimaged with Windows 7 operating system and Logic Analyzer software. Therefore, once you get back your logic analyzer with the replaced hard disk, you need not perform any steps to restore your system software. You can download and install the latest Logic Analyzer software from www.keysight.com/find/la-sw-download.

To remove and replace the tray assembly

1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
   - "To remove and replace the cover" on page 111.
   - "To remove and replace the front panel assembly" on page 117.
2 Using a Torx T10 screwdriver, remove the 2 side screws securing the tray assembly to the chassis.
3 Slide the tray assembly out far enough to disconnect the hard drive and power supply cables. Use the release tab(s) to help disconnect the power supply cables.
4 Slide the tray out of the chassis.

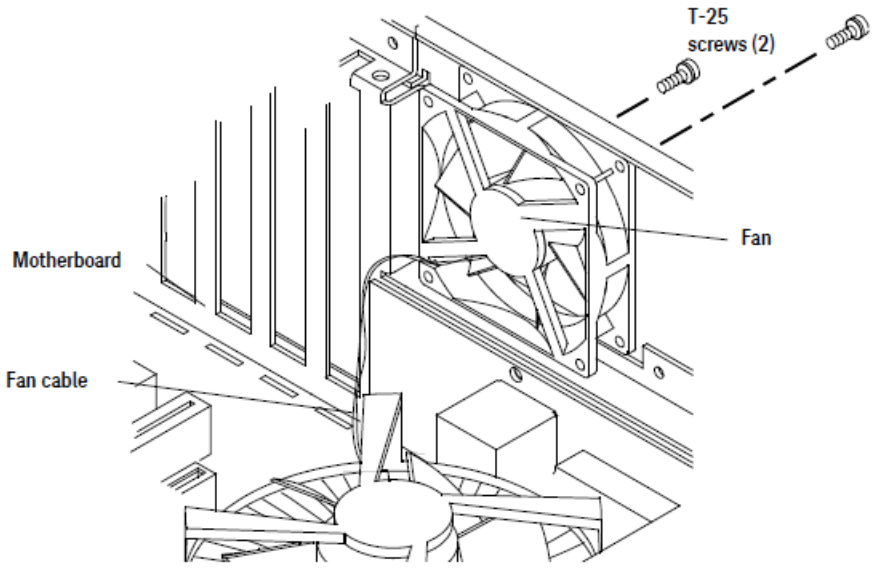


5 Reverse this procedure to replace the tray assembly.

To remove and replace the fans

60 mm fan

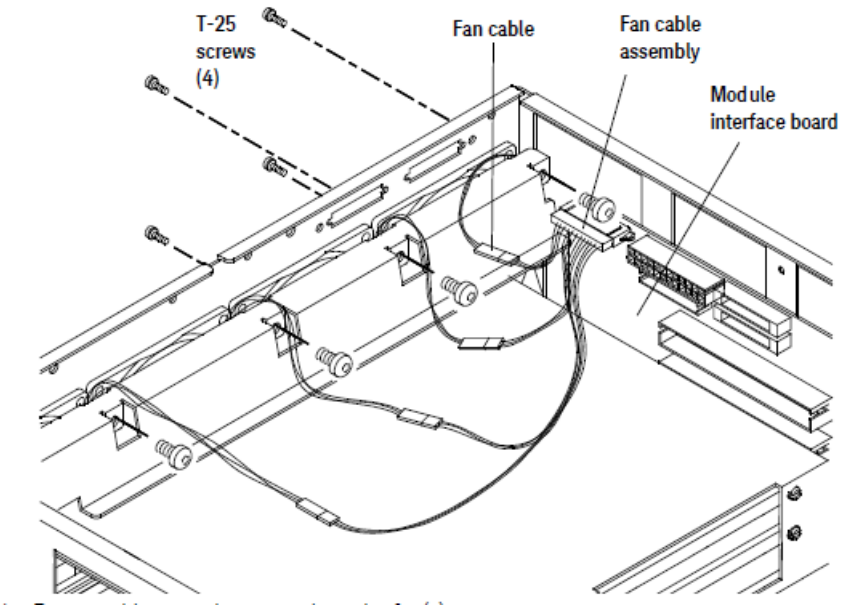
1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
   - "To remove and replace the cover" on page 111.
2 Disconnect the fan cable from the module interface board (MIB).
3 Using a Torx T25 screwdriver, remove the 2 screws holding the fan to the rear of the chassis.



4 Reverse this procedure to replace the fan.

92 mm fans

1 Perform previous procedures:
   - "To prepare the instrument for disassembly" on page 109.
   - "To remove and replace the cover" on page 111.
   - "To remove and replace the front panel assembly" on page 117.
   - "To remove and replace the tray assembly" on page 131.
2 Disconnect the fan cable for the fan you are replacing from the fan cable assembly. If replacing all fans, disconnect the fan cable assembly from the module interface board.
3 Using a Torx T25 screwdriver, remove the 4 screws securing the fan to the rear of the chassis.



4 Reverse this procedure to replace the fan(s).

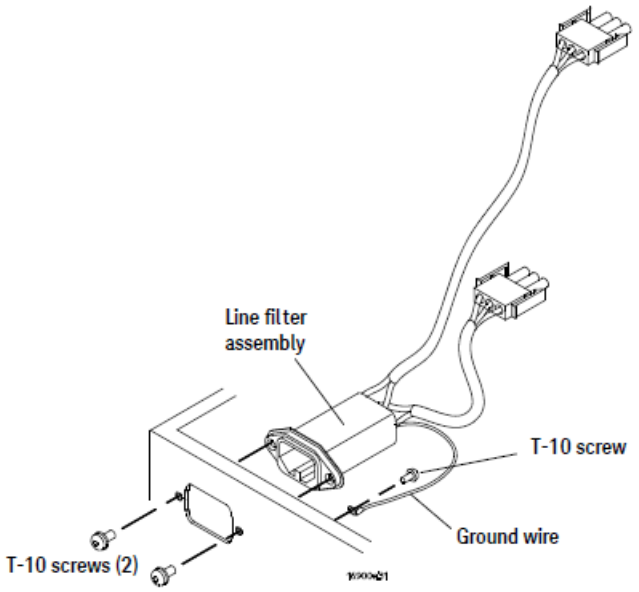
To remove and replace the line filter assembly

Perform previous procedures:

- "To prepare the instrument for disassembly" on page 109.
- "To remove and replace the cover" on page 111.
- "To remove and replace the front panel assembly" on page 117.

1 Disconnect the line filter assembly cables from the power supplies. In order to press the release latches on the lower cable connection, you may need to slide the tray assembly part way out following the procedure "To remove and replace the tray assembly" on page 131

2 Using a Torx T10 screwdriver, remove the 2 screws securing the power socket to the frame and the 1 screw to the ground wire.



3 Reverse this procedure to replace the power line filter assembly.

To replace the module interface board

To replace the module interface board of your 16800 logic analyzer, you send your logic analyzer unit to Keysight for repair/replacement of the module interface board. See "Returning Assemblies" on page 136 to know more about how to return the unit to Keysight for repair.

Ensure that all cables are disconnected from the module interface board.

Returning Assemblies

Before shipping the logic analyzer or assemblies to Keysight Technologies, contact your nearest Keysight Technologies Sales Office for additional details. To locate the sales or service office near you, go to www.keysight.com/find/contactus.

1 Write the following information on a tag and attach it to the part to be returned.
   - Name and address of owner.
   - Model number.
   - Serial number.
   - Description of service required or failure indications.

2 Remove accessories from the logic analyzer.

   Only return accessories to Keysight Technologies if they are associated with the failure symptoms.

3 Package the logic analyzer or assemblies.

   You can use either the original shipping containers, or order materials from an Keysight sales office.

CAUTION **For protection against electrostatic discharge, package the logic analyzer in electrostatic material.**

4 Seal the shipping container securely, and mark it FRAGILE.

7 Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for your 16800 Series logic analyzer.

Ordering Replaceable Parts

To order a part, visit us on the web at www.parts.keysight.com or call us in the United States at 1-877-447-7278. Or, you can contact your nearest Keysight Technologies Sales Office for assistance. To locate a sales office near you, go to www.keysight.com/find/contactus.

Exchange Assemblies

Some assemblies are part of an exchange program with Keysight Technologies.

The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Keysight Technologies.

After you receive the exchange assembly, return the defective assembly to Keysight Technologies. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Keysight Technologies will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest Keysight Technologies Sales Office for information. To locate a sales office near you, go to www.keysight.com/find/contactus.

For more information on returning assemblies, see "Returning Assemblies" on page 136.

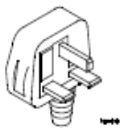
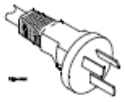
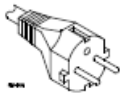
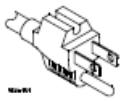
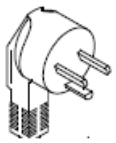
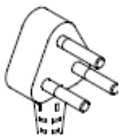
Power Cables and Plug Configurations

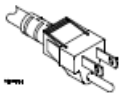
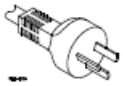
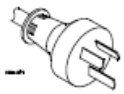
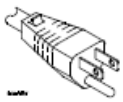
This instrument is equipped with a three-wire power cable. The type of power cable plug shipped with the instrument depends on the instrument model number country of destination.

In Table 16, the plug orientation number is the industry identifier for the plug only.

These cords are included in the CSA certification approval of the equipment.

Table 16 Power Cables and Plug Configurations

Plug Type (male connector)		Keysight Part No.	Plug Orientation (female connector)	Cable Length	Cable Color	Country
Option 900 250V		8120-1703	IEC 320-1 C13 (90°)	2.3 meters	Mint Gray	United Kingdom, Cyprus, Nigeria, Zimbabwe, Singapore, Malaysia
Option 901 250V		8120-0696	IEC 320-1 C13 (90°)	2.2 meters	Gray	Australia, New Zealand
Option 902 250V		8120-1692	IEC 320-1 C13 (90°)	2.0 meters	Mint Gray	East and West Europe, Saudi Arabia, (unpolarized in many nations)
Option 903 125V		8120-1521	IEC 320-1 C13 (90°)	2.2 meters	Jade Gray	United States, Canada, Mexico, Philippines, Taiwan
Option 906 250V		8120-2296	IEC 320-1 C13 (90°)	2.0 meters	Gray	Switzerland
Option 912 250V		8120-2957	IEC 320-1 C13 (90°)	2.0 meters	Gray	Denmark
Option 917 250V		8120-4600	IEC 320-1 C13 (90°)	2.0 meters	Mint Gray	Republic of South Africa, India

Plug Type (male connector)		Keysight Part No.	Plug Orientation (female connector)	Cable Length	Cable Color	Country
Option 918 100V		8120-4754	IEC 320-1 C13 (90°)	2.3 meters	Gray	Japan
Option 919 250V		8120-6799	IEC 320-1 C13 (90°)	2.0 meters	Flint Gray	Israel
Option 920 250V		8121-6871	IEC 320-1 C13 (90°)	2.0 meters	Flint Gray	Argentina
Option 921		8120-6979	IIEC 60320-1 C13 (90°)	4.5 meters	Flint Gray	Chile
Option 922		8120-8377	IEC 320-1 C13 (90°)	2.2 meters	Flint Gray	People's Republic of China
Option 927		8120-8871	IEC 60320-1 C13 (Straight)	2.3 meters	Flint Gray	Brazil, Thailand

System Replaceable Parts List

The replaceable parts lists in this chapter are organized by reference designation. The exploded views do not show all of the parts in the replaceable parts lists.

Information included for each part in the list consists of the following:

- Reference designator
  - A – Assembly
  - H – Hardware
  - MP – Mechanical Part
  - W – Cable
- Keysight Technologies part number
- Total quantity included with the instrument (Qty)
- Description of the part

Cover and Front Panel Assemblies

The cover assembly is the same for all 16800 Series logic analyzer models.

The 16800 Series logic analyzers have a built-in color display (touch screen with Option 103) and also support external displays.

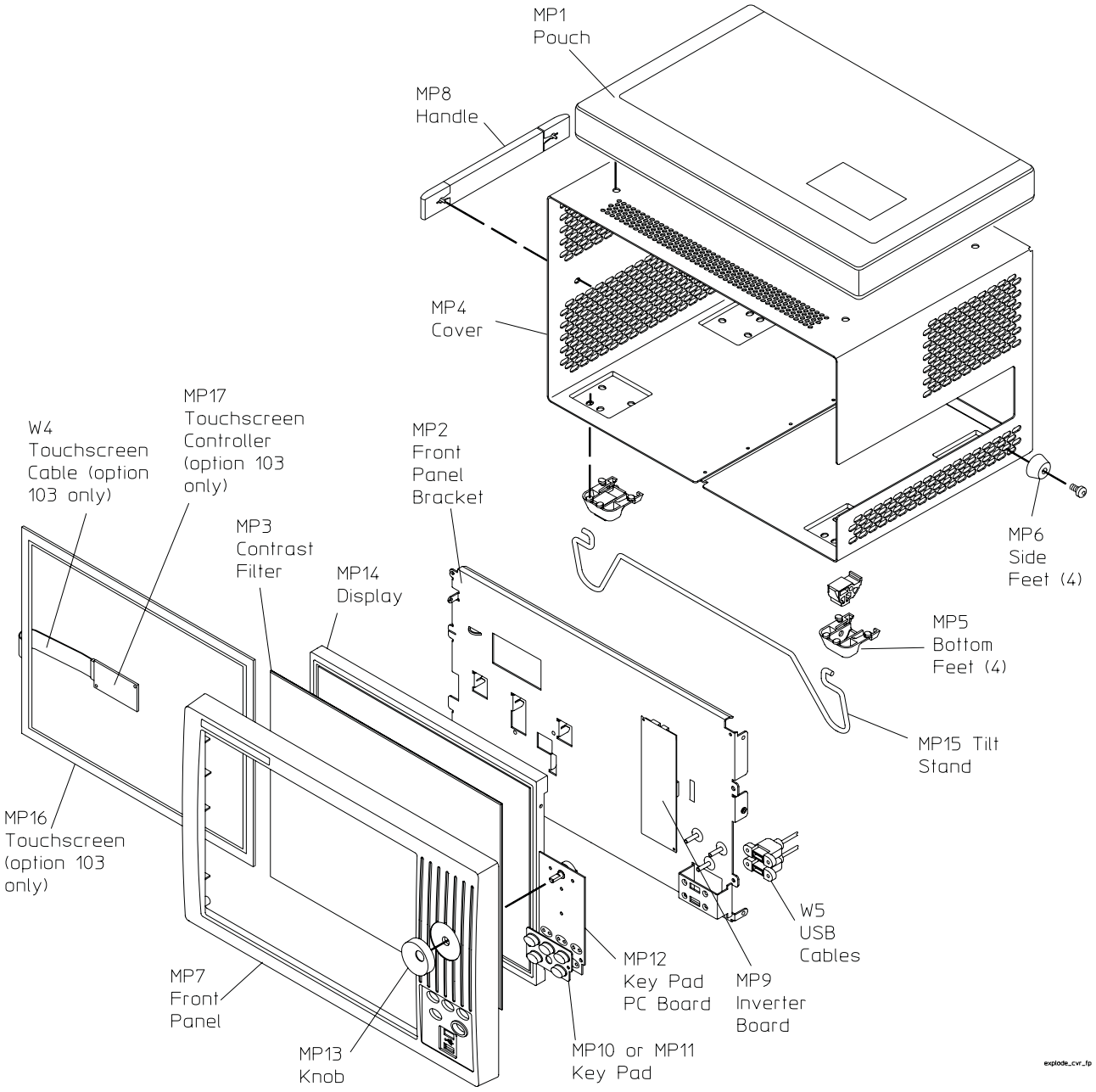


Table 17 Replaceable parts for the cover and front panel assembly

Ref. Des.	Keysight Technologies Part Number	Qty	Description
A1	16800-68700	1	Font panel with 15 inch display
A2	16800-68701	1	Font panel with 15 inch display and touchscreen (Option 103)
H1	0515-0374		Screw-machine M3 x 0.5 10mm long
H2	0515-2032		Screw-machine M3 x 0.5 8mm long 90-deg-flh-hd
H3	0515-0430		Screw-machine M3 x 0.5 6mm long
MP1	01680-68702	1	Accessory pouch
MP2	16800-01201	1	Bracket-front panel
MP3	16800-88001	1	Contrast filter
MP4	16800-04101	1	Cover
MP5	54810-61001	4	Foot-bottom
MP6	16800-40503	4	Foot-side
MP7	16800-40201	1	Front frame
MP8	16600-68707	1	Handle assembly (includes screws)
MP9	0950-4805	1	Inverter - DC-AC 8W dual output w/dimming function
M10	16800-47401	1	Keypad
MP11	16800-47402	1	Keypad - touchscreen (Option 103)
MP12	16800-66403	1	Keypad PC board assembly
MP13	16702-47402	1	Knob - cursor
MP14	2090-0939	1	LCD (Liquid Crystal Display) 15 inch TFT color
MP15	01680-04701	1	Tilt stand
M16	0960-2576	1	Touch screen (Option 103)
M17	0960-2535	1	Touch screen controller board (Option 103)
W1	16800-61613	1	Display cable (not shown)
W2	16800-61603	1	Front panel cable (not shown)
W3	16800-61614	1	Inverter cable (not shown)
W4	D8104-61604	1	Touch screen cable (Option 103)
W5	16800-61611	1	USB dual cable

Frame

There are two types of frames used in the 16800 Series logic analyzers, but their differences are minor:

- The 1-slot, low-power frame (for 16801A, 16802A, and 16803A logic analyzers) has:
  - A 1-slot module interface board (MIB).
  - A second, 15 W power supply.
- The 2-slot, high-power frame (for 16804A, 16806A, 16821A, 16822A, and 16823A logic analyzers) has:
  - A 2-slot module interface board (MIB).
  - A second, 175 W power supply.

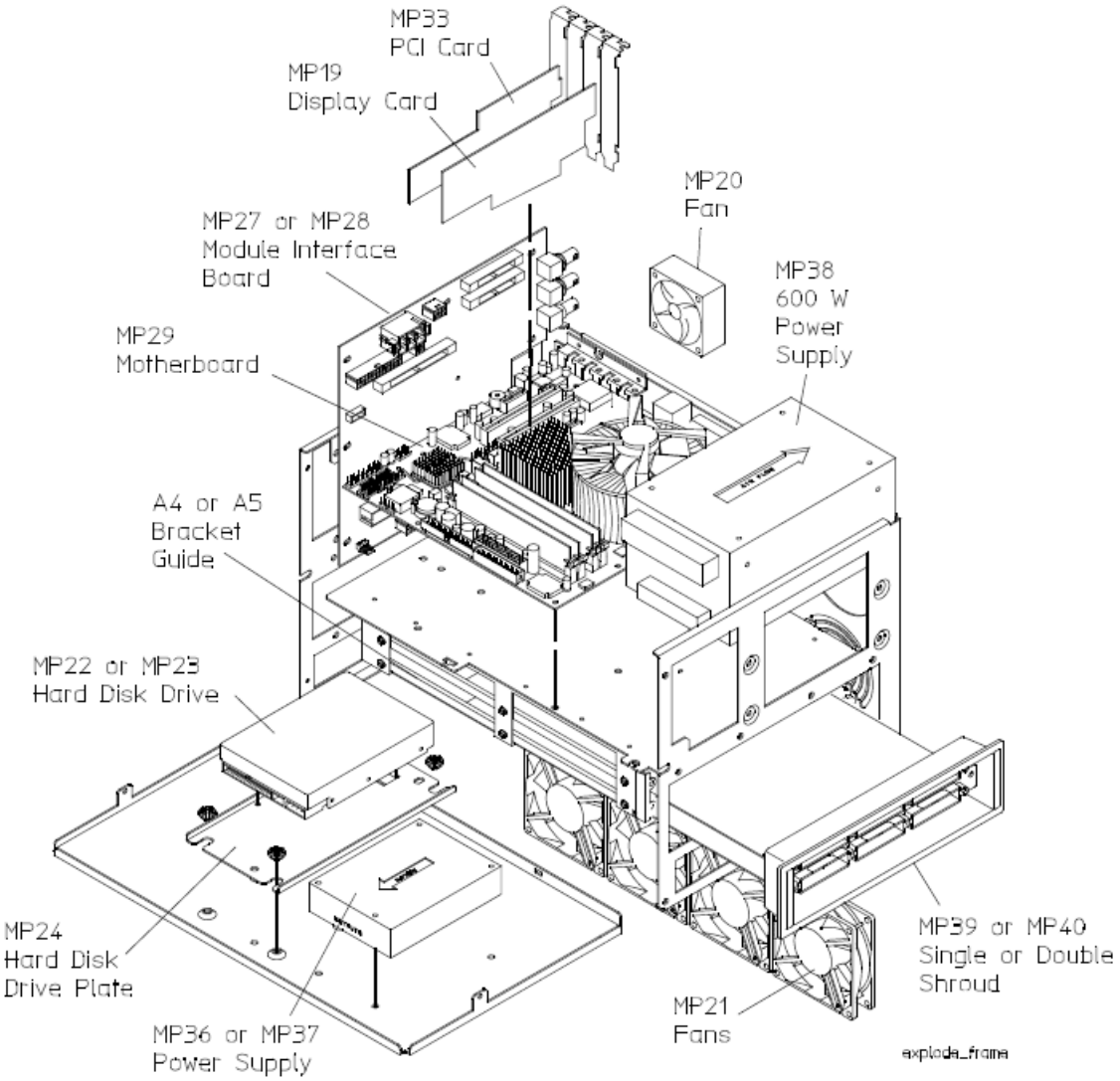


Table 18 Replaceable parts for the frame

Ref. Des.	Keysight Technologies Part Number	Qty	Description
	see page 139	1	Power cords
A3	16800-60002	1	Chassis - fan assembly (includes all fans)
A4	16801-68700	1	Chassis subassembly (low-power frame)
A5	16804-68700	1	Chassis subassembly (high-power frame)
MP18	16800-00201	1	CPU I/O panel (not shown)
MP19	0960-2530	1	Display card - advanced digital
MP20	16800-68502	1	Fan assembly 60mm
MP21	16800-68501	1	Fan assembly 92mm
MP24	16800-01203	1	Hard disk drive (HDD) plate
MP25	1150-7970	1	Keyboard (not shown)
MP26	16800-94301	1	Label AC power (not shown)
MP27	16800-66504	1	Module interface board (MIB) (high-power frame)
MP28	16800-66505	1	Module interface board (MIB) (low-power frame)
MP29	D81004-68809	1	Motherboard assembly (with CPU and SDRAM)
MP30	1150-7913	1	Mouse, optical wheel (not shown)
MP31	16903-66404	1	PCI card
MP32	16800-01205	1	PCI card bracket
MP33	16903-66504	1	PCI card w/bracket assembly
MP34	0950-4812	1	Power supply AC/DC 175W 5 outputs
MP35	16800-01204	1	Power supply plate for 15 W supply
MP36	16801-68701	1	Power supply subassembly - 15 W (low-power frame)
MP37	16804-68701	1	Power supply subassembly - 175 W (high-power frame)
MP38	16800-68702	1	Power supply subassembly - 600 W
MP39	16800-40502	1	Probe shroud (high-power frame)
MP40	16800-40501	1	Probe shroud (low-power frame)
MP41	16903-67101	1	RFI Gasket keyboard/mouse (not shown)
MP42	8160-0991	1	RFI strip-fingers (not shown)
MP43	1150-7997	4	Stylus (Option 103 - not shown)

Ref. Des.	Keysight Technologies Part Number	Qty	Description
W6	16800-61609	1	Cable - CPU power
W7	16800-61608	1	Cable - fan assembly
W8	16800-61601	1	Cable - front panel
W9	16800-61610	1	Cable - hard disk drive (HDD) power
W10	54855-61624	1	Cable - motherboard switch cable
W11	16800-61600	1	Cable - PCI/MIB
W12	16800-61605	1	Cable - power 175W (high-power frame)
W13	16800-61606	1	Cable - power supply 15W (low-power frame)
W14	16800-61607	1	Cable - power supply 175W (high-power frame)
W15	D8104-61603	1	Cable - serial-ATA hard drive

Replaceable parts for the frames with serial number MY50370000 or greater

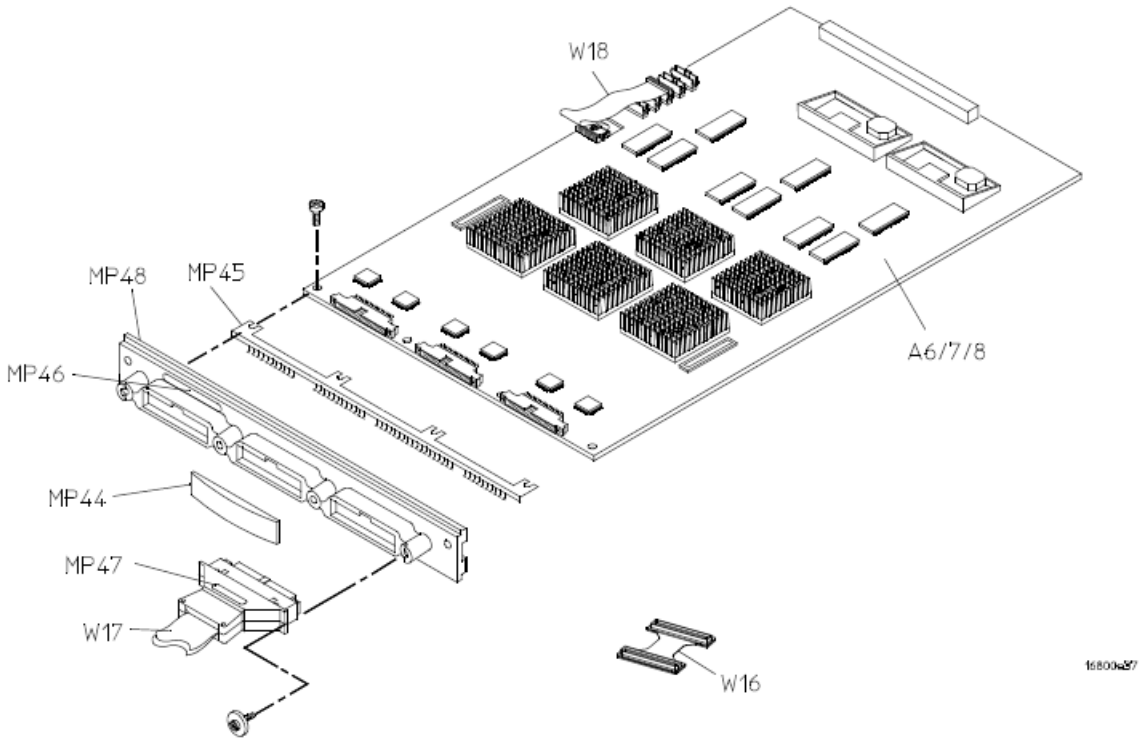
The following are the new part numbers for the replaceable parts of the 16800 Series logic analyzer frames with serial number MY50370000 or greater. For parts that are not listed in the following table, the old part numbers specified in Table 18 are applicable.

Table 19 Replaceable parts for the frame with serial number MY50370000 or greater

Ref. Des.	Keysight Technologies Part Number	Backward Compatible	Description
MP29	0960-2939	No	Motherboard
W10	16901-61607	No	Motherboard Switch Cable
W6	16800-61617	Yes	Cable - CPU power
MP18	16800-00202	No	CPU IO Panel
MP29	16901-68712	No	Motherboard Assembly
	16800-00107	No	Chassis
A3	16800-60007	No	Chassis - Fan Assembly
MP28	16800-66507	Yes	16800 Module Interface Board (MIB) - low-power frame
MP27	16800-66506	Yes	16800 Module Interface Board (MIB) - high-power frame
	54904-61617	No	Cable Assembly - Display and Inverter

Measurement Card Replaceable Parts List

Figure 10 Exploded view of the logic acquisition card



The replaceable parts list is organized by reference designation and shows exchange assemblies, electrical assemblies, then other parts.

Information included for each part on the list consists of the following:

- Reference designator (if applicable)
- Keysight Technologies part number
- Total quantity included with the module (Qty)
- Description of the part

Reference designators used in the parts list are as follows:

- A – Assembly
- MP – Mechanical Part
- W – Cable

Table 20 Measurement Card Replaceable Parts

Ref. Des.	Keysight Part Number	Qty	Description
A6	16912-68702	1	34-Channel Acquisition Board Assembly
A7	16911-68702	1	68-Channel Acquisition Board Assembly
A8	16910-68702	1	102-Channel Acquisition Board Assembly
MP44	16910-04101	1	Cover Plate
MP45	16715-29101	1	Ground spring
MP46	16802-94301 16804-94301 16806-94301 16821-94301	1 1 1 1	Label ID Label ID Label ID Label ID
MP47	01650-94312	1	Label pod and cable
MP48	16910-40201	1	Panel module
W16	16754-60002	1	2 x 50 Master/Expander Cable Kit (2 pieces)
W17	16715-61601	1	Cable probe
W18	16754-61602	1	Cable assembly 2x30

Pattern Generator Card Replaceable Parts

Figure 11 Exploded view of the pattern generator card

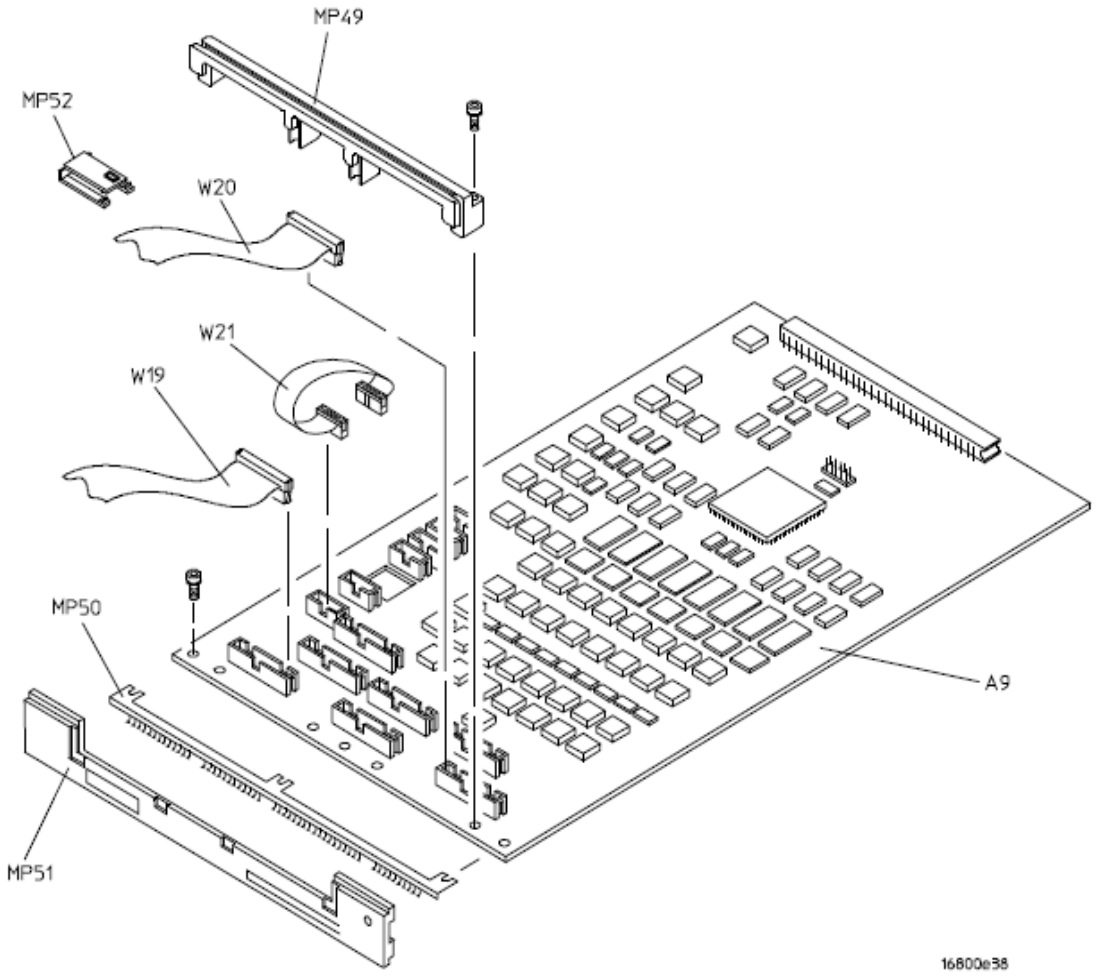


Table 21 Pattern Generator Card Replaceable Parts

Ref Des.	Part Number	Qty	Description
A9	16720-68702	1	Circuit board assembly for 16800
MP49	16510-40502	1	Cable clamp
MP50	16500-29101	1	Ground Spring
MP51	16510-40501	1	Rear panel
MP52	16500-41201	7	Ribbon cable ID clip
W19	16522-61602	1	Clock cable (J6)
W20	16522-61601	6	Data Cable (J1-J5)
W21	16522-61603	1	Interconnect cable

8 Theory of Operation

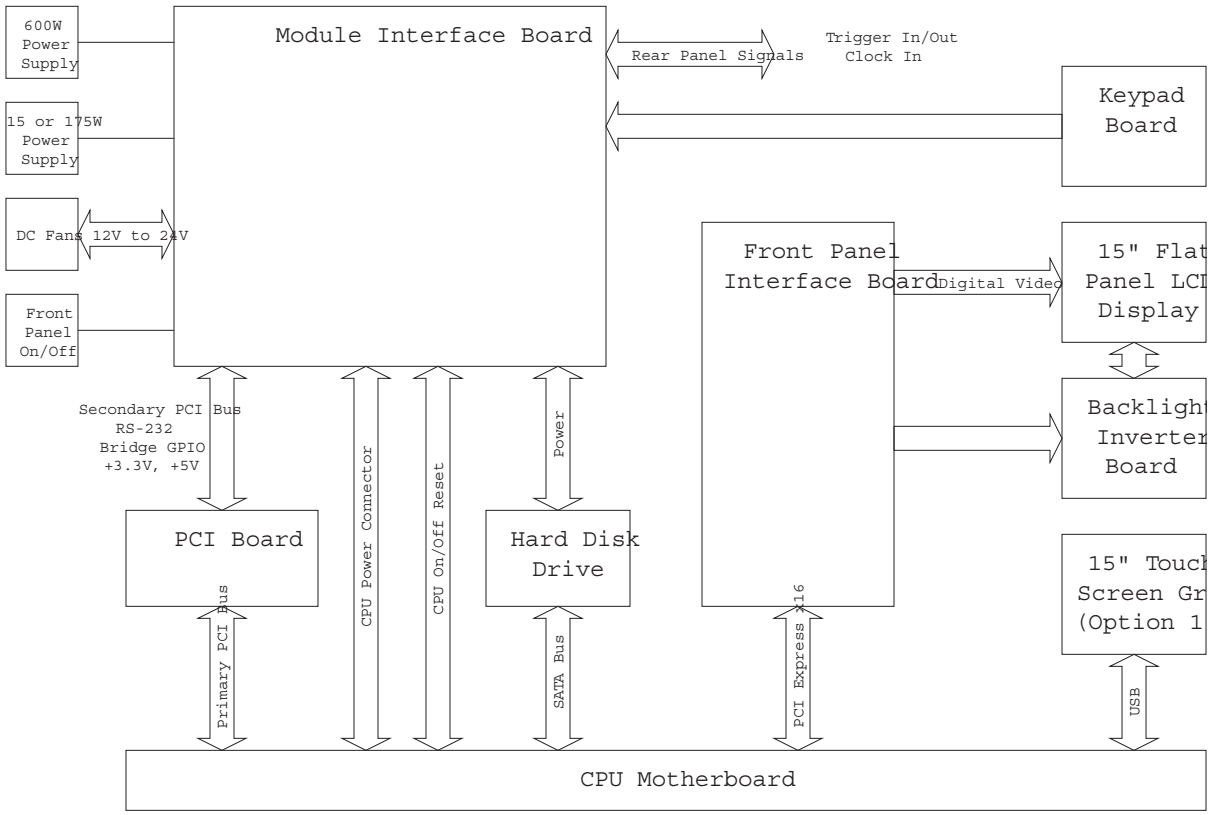
This chapter describes the theory of operation for the 16800 Series logic analyzers.

The information in this chapter is to help you understand how the logic analyzer and pattern generator (depending on the model) operate. This information is not intended for component-level repair.

System Block Level Theory

The block-level theory includes the theory of operation of the logic analyzer in terms of the major subsystems including:

- CPU subsystem.
- PCI board.
- MIB (module interface board).
- Front panel assembly.



CPU Subsystem

The CPU subsystem includes:

- CPU board (more on page 156).
- Disk drives (more on page 156).
- Power supply (more on page 156).

PCI Board

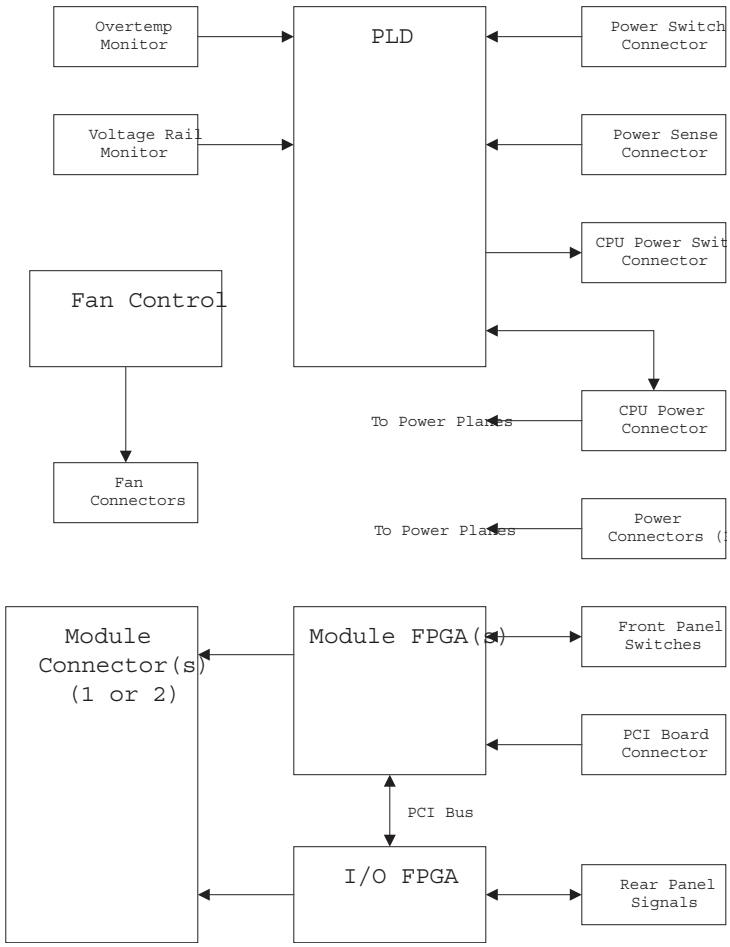
For more information on the PCI board go to page 156.

Module Interface Board (MIB)

The MIB subsystem block diagram shown here includes:

- Module bus FPGA(s) (more on page 157).

- I/O FPGA (more on page 157). Supported rear panel signals include:
  - Trigger IN/OUT (more on page 157).
  - Clock IN (more on page 157).
- PLD (more on page 158).
- Voltage rail monitor (more on page 158).
- Overtemp monitor (more on page 158).
- Fan control (more on page 158).

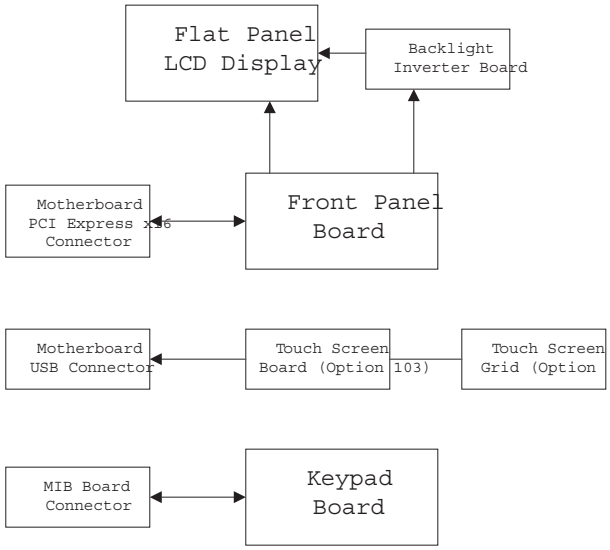


Front Panel Assembly

The front panel assembly block diagram shown here includes:

- LCD display.
- Touch screen board and grid (Option 103).
- Keypad board.

For more information on the front panel assembly to page 158.



CPU Subsystem

CPU Board

The CPU motherboard is a standard microATX configuration with 1 GB of system RAM. The exact CPU and speed grade will vary over the life of the product. Standard I/Os built into the ATX board are PS/2, serial port, parallel port, USB 2.0, 10/100 Mbit LAN, and VGA Video. One PCI slot and one PCI Express x1 slot are available for added I/O such as 1 Gbit LAN or video.

Disk Drive

The frame contains a SATA hard drive. It is logically controlled directly from the CPU motherboard.

Power supply

The frame uses two modular power supplies to provide the six DC voltage rails: -12 V, +12 V, -5 V, +5 V, -3.3 V, +3.3 V. These rails use remote sensing to maintain.01% load regulation. The module slots are limited to 100 W each and the instrument as a whole to 600 W.

The frame has a "soft" power on/off algorithm. Pressing the power switch notifies the CPU to either wake up or power down. The CPU then in turn drives the signal line which actually turns the supplies on or off. A PLD monitors this process and will force a power down after approximately two minutes if the CPU does not respond. The small portion of circuitry involved in this process is powered from an auxiliary +5 V which is always present as long as the instrument is plugged in. Additional logic monitors the voltage levels on the six rails and will also cause an immediate power down if any one drops below about 90% of regulation. Power down can also be caused by an over temperature sense circuit. In this case, the PLD notifies the CPU, the user receives a warning window, and a soft power down is started. Again, the PLD will force a power down if the CPU does not soft power down in about two minutes.

PCI board

The PCI Board plugs into a CPU motherboard PCI slot, providing the interface between the CPU motherboard and the logic analyzer. On the PCI board is a PCI bridge chip used to provide an electrical interface between the CPU PCI slot bus and the two PCI devices located on the Module

Interface Board. A TI2050A PCI bridge chip is used to connect to the primary PCI bus on the CPU motherboard connector and provides a secondary PCI bus, which is connected via an 80-pin high-density cable from this PCI board to the Module Interface Board.

MIB (Module Interface Board)

Top level function

The MIB contains all of the logic analyzer frame specific hardware. This includes all circuits necessary to interface with measurement modules, interface with the front panel knob and keys, monitor frame functions, and interface to the CPU motherboard via the PCI board. It also performs power distribution and numerous interconnects.

Two different MIBs are used in the 16800 Series logic analyzers:

- The MIB in the 2-slot, high-power frame (for 16804A, 16806A, 16821A, 16822A, and 16823A logic analyzers) has two module bus FPGAs.
- The MIB in the 1-slot, low-power frames (for 16801A, 16802A, and 16803A logic analyzers) has one module bus FPGA.

Module Bus FPGA(s)

The Xilinx XC3S500E FPGA is the primary bridge between the CPU and the measurement modules. It effectively performs a translation from PCI slot to the proprietary module interface bus.

In the 2-slot, high-power frame, a second module FPGA, Xilinx XC2VP20, performs the translation from PCI slot to a second, high-speed module interface bus.

I/O FPGA

The Xilinx XC2V250 FPGA is the center of the instrument I/O functions. The system interfaces directly to this part in the same way it talks to the measurement module slot(s), via a 16-bit multiplexed general purpose bus. The FPGA is loaded from an on board EPROM at power up. The EPROM contents can be changed (updated) through the system software via a JTAG port.

A major function of this FPGA component is system correlation; time alignment of the measurement modules and possible other modules connected through the Trigger In connector. This is done with eight 52-bit counters running at 1.6 GHz, allowing relative time alignment of eight separate events. A 100 MHz clock is also selected from two possible sources (internal, external) and a synchronizing signal is generated for time alignment.

A second major function of the FPGA is the logical combination and routing of the module arm and trigger lines: ARM, TRIG, FLAG. These signals are used by the modules to start and stop each other in addition to supplying the signals for real-time correlation.

The other FPGA functions include a system interface to control the Trigger In and Trigger Out ports, and a serial DAC programmer.

Trigger IN/OUT

These two BNCs function as an external trigger out and arm in signaling between frames or other test equipment. The TRIGGER OUT is a simple 3-state LVTTL 50 Ω line drive circuit. TRIGGER IN (ARM) is complicated by the need to handle variable threshold levels. The circuit consists of a programmable 12 bit DAC and comparator. This combined with a level shift and divide circuit allows for a ±5 V input range, 200 mV minimum swing, and 50 mV threshold steps.

Clock IN

This BNC input is specifically for a 10 MHz clock signal from an oscilloscope or other source. The signal is AC coupled and passed through a 10X multiplier part (low jitter) and then fed to the FPGA as one of the 100 MHz clock source choices. Using this input allows two measurement instruments to run on the same time base and maintain correct time alignment over long acquisitions.

PLD

The PLD is the low level system control element powered from the AUX +5 V rail and continuously ON. It logically controls the soft power ON/OFF through signal lines to the CPU and power switch monitoring. It physically turns power ON/OFF via power on/off signals on the power supply sense cables. In addition to the power switch starting a power down sequence, two additional monitoring circuits (overtemp and voltage rail) may cause the PLD to initiate power down. Both of these conditions are "latched" faults and require removing the power cord for 15 seconds to clear the condition.

Voltage Rail Monitor

All six voltage rails are continuously monitored for an under voltage fault condition. This could be caused by such things as a failed power supply or a short circuit within the instrument. When detected, both power supplies are immediately shut down. At power up, there is a one second time delay to allow the power to stabilize before the monitoring circuit is enabled.

Overtemp Monitor

A temperature monitoring circuit protects the instrument from thermal damage due to things such as failed fans or blocked frame vents. The circuit first notifies the CPU of a problem which then prompts the user with a warning message and initiates a soft power down. If the soft power down fails, a forced power down is initiated after about two minutes.

Fan Control

The instrument uses a pair of 24 V fans driven from a DC/DC boost converter circuit. This circuit creates a linear voltage ramp from 12 V to 24 V across the operating temperature range. The purpose of this circuit is to increase air flow as needed while maintaining the lowest possible fan noise.

Front Panel Assembly

The identical front panel assembly with LCD is used on all 16800 Series logic analyzers. The front panel assembly is composed of two PC boards comprising three independently operating sub-systems. The two PC boards are the front panel interface board and the keypad board. The three front panel sub-systems are:

- Front panel keypad board.
- Front panel interface board.
- Front panel touch screen (Option 103).

Front Panel Keypad Board

The front panel switches consist of five buttons and one digital encoder, the knob. When a button is pressed and released, or the knob turned, a series of codes are sent back to the module FPGA. When the module FPGA receives a front panel code, an interrupt is sent to the system CPU. The resulting ISR will read the code and act on it.

The module FPGA was used as a convenient place to put this logic. This logic operates independently of the module backplane logic also within the module FPGA.

Front Panel Interface Board

The front panel interface board plugs into the CPU motherboard's PCI Express x16 slot and provides a connection point for flat-panel display communication.

The connectors J2 and J3 are connected to a Mitsubishi 15" XGA AA150XN01 TFT-LCD 1024x768 display:

- Connector J2 provides the data path back to an Adlink video adapter.

- Connector J3 is used to provide the high-voltage needed to light the display backlight. This high-voltage is generated using a power inverter board, which is mounted on the front panel interface board. This power inverter board is a TDK CXA-0384 DC-AC Inverter Unit.

Front Panel Touch Screen (Option 103)

Attached to the front panel assembly (in models ordered with Option 103) is a Touch Screen Control module used to implement the touch screen. The touch screen controller board is a 3M SC801U. Mounted in front of the flat panel display is a touch screen grid connected directly to the touch screen controller. The controller interprets touch presses and communicates with the host CPU via USB.

Power Up Routine

The power up routing includes the following:

- Boot sequence (more on page 159).
- Product install (more on page 160).
- Software recovery methods (more on page 161).
- Self test (more on page 161).

Boot Sequence

The 16800 Series logic analyzers having the serial number prior to MY50370000 are shipped with the Windows XP Professional operating system. The 16800 Series logic analyzers having the serial number MY50370000 or higher are shipped with the Windows 7 operating system.

After power is applied to the frame, the basic input/output system (BIOS) is the first thing to run. Among other things, the BIOS is responsible for enumerating plug-and-play (PnP) devices in the system and doing a "power on self test" (POST). All of the CPU (motherboard) RAM is checked during POST--however, subtle memory problems may not be detected by this simple test. If any hardware that the BIOS detects is malfunctioning at a fundamental level, then the BIOS reports an error to the display (if available). If things are OK, control is turned over to the operating system.

On Windows XP, during startup, the Keysight logo is displayed by the system BIOS, then a few other messages, and finally the preliminary Windows XP startup screens.

On Windows 7, you are automatically logged on to the system using the Administrator account and the Windows 7 desktop is displayed.

During the first phase of the Windows startup, the kernel is loaded along with various system drivers. Prior to the video drivers loading, video is only displayed to the same video device as the BIOS startup screen. Once the video drivers load, the resolution will switch and eventually a logon screen will be presented. The logon screen will appear on whichever video adapter (LCD or external VGA) was displaying the Windows desktop when the system was last shut down. It is possible to get a blank screen. In this situation, you can press and hold the "Touch Off" button on the front panel to open Intel's configuration utility and switch the Windows desktop from one display adapter to the next. At any time, either the LCD panel or the external monitor will have the Windows desktop displayed to it. It is also possible, but not typical, for the Windows desktop to be stretched across both the LCD and external monitor. The "Touch Off" front panel button can be pressed and held to open Intel's configuration utility which can force the desktop to use either the LCD or external monitor exclusively.

By the time Windows has presented the Windows logon screen, two critical pieces of Keysight-specific software should already be running:

- Logic analyzer device drivers.
- Logic analyzer service.

The remaining critical piece of Keysight software (the GUI application itself) does not run until a user has logged onto the machine and started the application by clicking on the shortcut on the Windows desktop and/or the Windows start menu. The GUI application may auto-run when a user logs onto the machine.

The logic analyzer device drivers communicate directly with all of the hardware. This includes the frame hardware and all modules plugged into the frame. All other Keysight software in the system communicates with the drivers in order to access the hardware. Therefore, missing drivers look like missing hardware to the Keysight software. The frame power button LED will flash when the frame is first powered on and become steady once the frame drivers have loaded. A flashing power button LED should indicate:

1 The frame is in the middle of a power up or power down sequence.

2 The frame hardware was not recognized by the PnP system.

3 The frame drivers are missing.

Once the Windows kernel and the system drivers are loaded, a variety of Windows services (background processes) are started automatically by the system. These services are like UNIX/Linux daemons. They run silently in the background in order to provide system services. They run before any user has logged onto the system. If the logic analyzer product is installed on the system, a logic analyzer service called "Keysight Logic Analysis" should be running.

The logic analyzer service carries the following general responsibilities:

- System manager for the local frame.
- Communicates with local GUI application software.
- Listens for connection requests across the LAN (remote connect from other systems).
- Initialization of all local frame hardware including modules. This initialization includes loading of all FPGAs that are not loaded directly by boot-EEPROMs when power is first applied to the system.
- Hardware monitoring.
- Control over the "Touch Off" front panel button (if Option 103 is installed).

The logic analyzer service must be started and fully initialized before the application software will be allowed to run. The logic analyzer drivers are not required for the application software to run – however the software will not be able to go online with the local hardware until the drivers are installed/running. In addition, other machines will not be able to remote connect to the machine and use its hardware if the drivers are not installed and running.

Because the service should always be running regardless of whether any user is logged onto the system, the logic analyzer should always be responsive to remote connection requests from other machines. The Touch Off button should also always function (if Option 103 is installed).

When the GUI application is launched by a logged on user, the application (by default) will attempt to connect to local hardware and go "online". If the service is not started, the application should either wait for the service to start (newer software revisions) or generate a message box indicating the service needs to be started (older software revisions). If the drivers are not loaded, the GUI application will start in offline mode.

Once the GUI application is running, the user can go online with local hardware or the hardware in any other Keysight 168x/169x/168xx/1690x logic analyzer running the same version of the logic analyzer software. The remote machine must be available on the network.

Product install

The product install (SetupLAxxxx.exe) performs the following:

- Install the logic analyzer-specific files to the local hard drive.
- Register the application with the operating system (various registry settings are applied including COM registration).

- Create start menu/desktop shortcuts.
- Install device drivers.
- Install and start the service.
- Check frame boot-EEPROMs (non-volatile ROMs) and verify they are up-to-date. Reloads the boot-EEPROMs if necessary.

Software recovery methods

1 **Logic analyzer product re-installation**

Re-installing the logic analyzer product requires running the setup executable file – typically named SetupLAxxxx.exe. For example, the 03.50 software release file will be called SetupLA0350.exe.

During the installation of the product, older versions are automatically removed and replaced with the newer version. However, if you need to install an older version of the software over a newer version you must first uninstall the newer version. To uninstall the software, go to Windows **Start>Control Panel>Add or Remove Programs**. Select the logic analyzer software from the list of installed programs and select uninstall.

This recovery mechanism is used to fix problems with the logic analyzer software including application crash problems or problems with hardware recognition.

2 **Full hard drive (system-level) recovery:** This recovery mechanism is used to fix system-level problems – including damage done by viruses or previously-installed software, problems with operating system bugchecks (blue screen), etc.

On a Legacy 16800 Series Logic Analyzer with Windows XP Installation

This is done by placing the appropriate recovery CD into an external USB DVD-ROM drive and rebooting the analyzer. When the system begins booting after shutting down, the recovery sequence will begin. After addressing the introduction screens, the recovery CD will erase all data on the hard drive and image the disk back to the state it was in when the customer received it. After a full hard drive recovery, the logic analyzer software may or may not already be installed (depending on the version of the recovery CD used).

On a 16800 Series Logic Analyzer with Windows 7 Installation

These systems do not have any recovery CD or DVD in their shipment. To perform a system-level recovery, you run the recovery process on the hard drive of the system. This recovery process uses the hidden partition on the hard drive to restore the hard disk drive back to its original state in which it was shipped. Refer to "To restore the system software" on page 88 to know more about the recovery process.

Self Test

The logic analyzer does very little self test unless it is explicitly run by the user. As previously mentioned, the system BIOS does some hardware self test before turning control over to the operating system.

Once a user logs into the system and runs the logic analyzer GUI application software, self tests can be run by clicking on the "Help" menu within the application and then selecting "Self Test".

All self tests are consolidated into a single self test dialog.

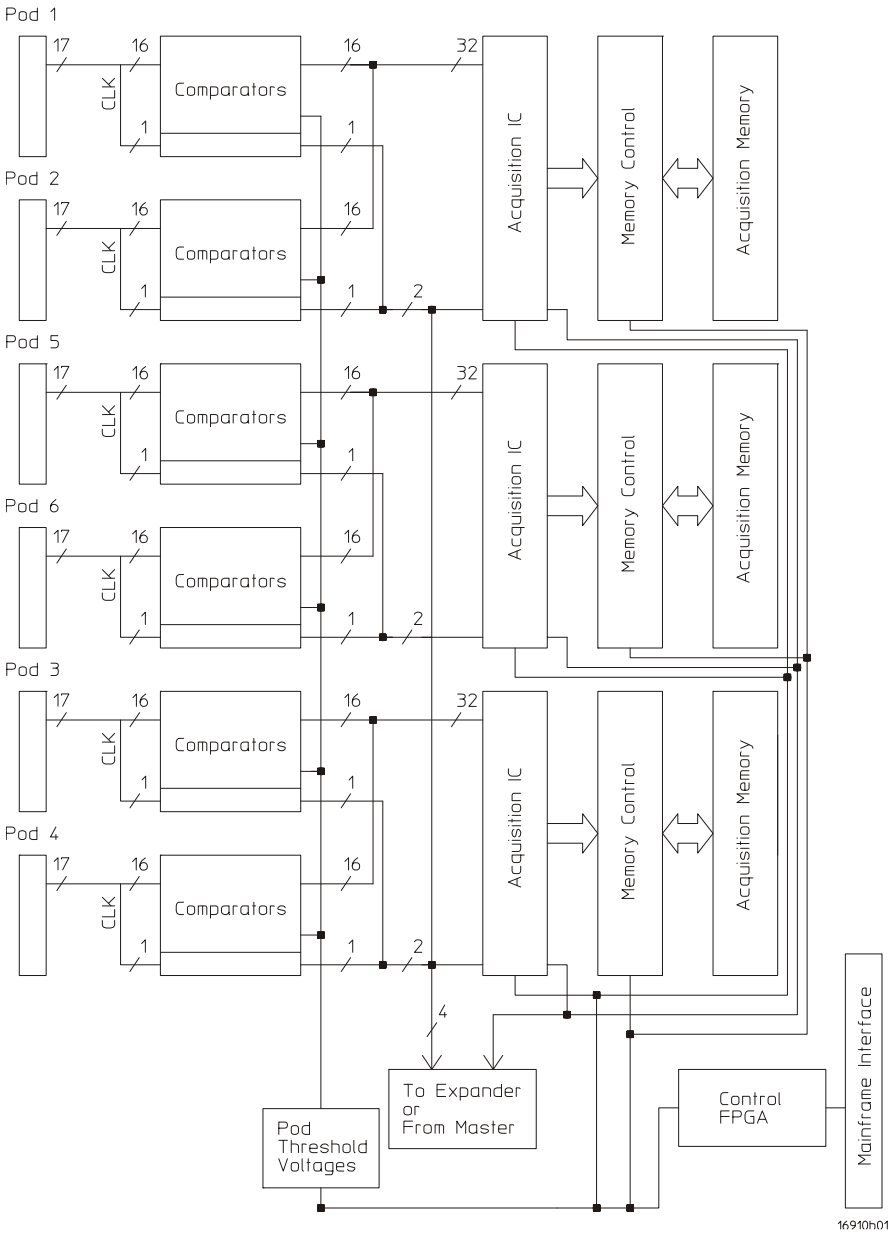
The self test dialog contains a pane which allows the user to select the "test suite" and a pane which allows the user to select a specific test within that suite – or all of the tests. The tests can be run once or repetitively. Each card will have its own suite of tests. The frame hardware itself has a suite called "System".

At the bottom of the self test dialog is a results pane. The reporting level (how verbose the tests are) can be controlled using a slider bar at the top of the dialog. At the very least, each test should report that it is running and what the final status of each test was (pass or fail). Increasing the reporting level and re-running certain tests may help isolate a specific hardware failure in the event that a test fails.

Logic Acquisition Block-Level Theory

The block diagram of the logic acquisition card is shown below.

Figure 12 Logic Acquisition Card Block Diagram



Probes

Two types of logic acquisition cards can be used: one that contains 6 probe pods, and one that contains 4 probe pods. One pod pair is ignored in the 34-channel 16801A and 16821A logic analyzer models.

Each pod is comprised of one cable and contains 16 single-ended data channels, a clock channel, two serial IIC (Inter-IC, also known as I2C) programming lines for configuring analysis probes, +5 V for powering analysis probes, and 22 ground signals. Each cable has a 40-pin probe cable connector.

The pods provide +5 Vdc ±5% auxiliary power to each 40-pin probe cable connector. Each connector can deliver up to 300 mA with a maximum of 1.0 A total from the analyzer card. A current limiting circuit protects the +5 V cable power from current overload. The VCC_Enable signal is used to control power to an analysis probe. Currently, the +5 Vdc is only disabled during the IIC self-test.

A variety of single-ended probes can be connected to the logic analyzer cables.

Comparators

The comparators are single-ended devices that interpret incoming data and clock signals as either high or low. A threshold voltage provided by a digital-to-analog-converter (DAC) is coupled to the reference input of the comparator through a precision resistor. Pod thresholds are individually adjustable; clock and data share the same threshold. The comparator outputs drive the acquisition ICs and clock divider circuitry.

Acquisition IC

Each Acquisition IC processes 32 channels of data and 2 channels of clock information. The Acquisition ICs perform data sampling, sequencing, store qualification, pattern recognition, and counting functions. State or Timing sample clocks are sent from the Master card to the Acquisition ICs in each of the Expander cards in a multi-card module. Sampled data is decelerated and passed to the Memory Controller for storage in the Acquisition Memory RAM array.

The Acquisition ICs also contain the 4 GHz sample Timing Zoom circuitry and memory.

Memory Controller and Acquisition Memory

The Memory Controllers store data from the Acquisition ICs into the Acquisition Memory array which is composed of 256 Mbit DDR DRAMs. They also unload data from the memory array after an acquisition is complete, and they deliver the data to the mainframe display system through the mainframe interface connector. In addition they control refresh of the RAM array and can perform a search of stored data.

Master/Expander Connectors

Connectors J9 through J13 and J15 route state and timing clocks, calibration signals, data search signals, and control from the Master card to all cards in the module.

Connectors J20 through J23 route pattern recognition signals between all cards in a card set as well as control clocks from the Master card to other cards in the set.

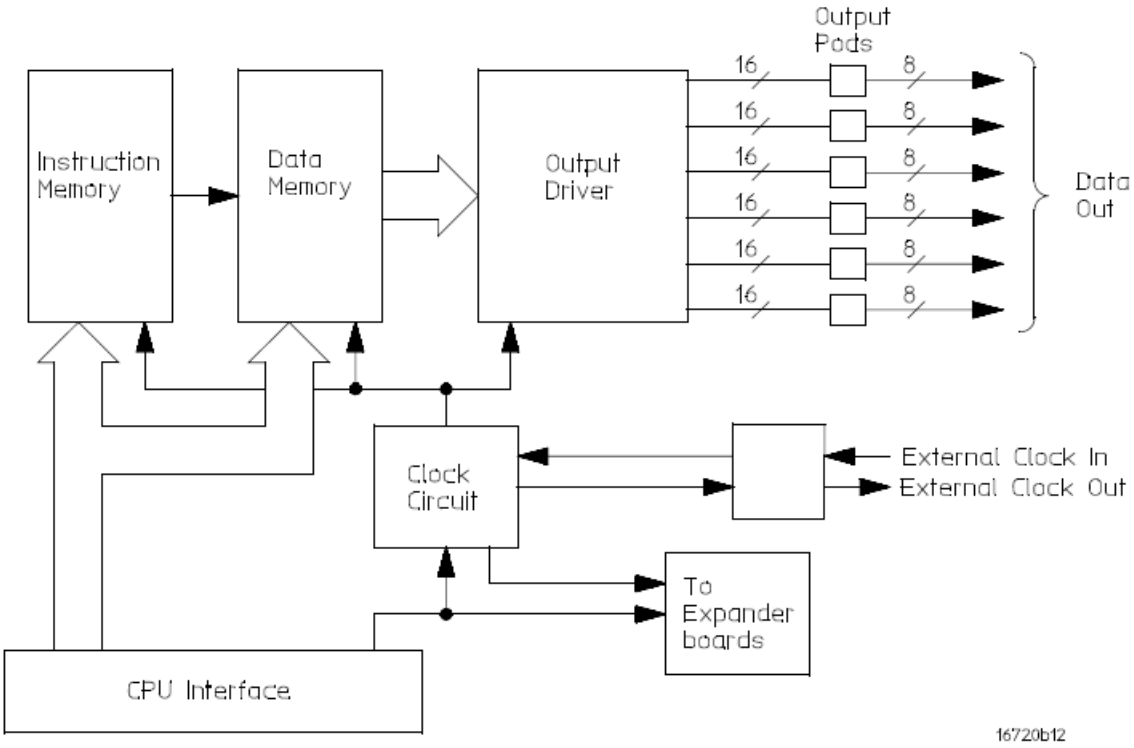
Mainframe Interface and Control FPGA

The Mainframe interface consists of an FPGA and the Mainframe Interface Connector. The connector brings power onto the card and provides for control of the card by the analyzer mainframe. It also provides a path for unloading acquired data to the analyzer display.

The FPGA converts bus signals generated by the mainframe processor into control signals for the logic analyzer card. It also provides centralized functions for the card such as I2C, Calibration signals, Flag routing, and Timing mode sample clock.

Pattern Generation Block-Level Theory

Figure 13 Pattern Generator Block Diagram



Instruction Memory

The instruction memory holds the programmable vector flow information and is paced in parallel with the data memory. User-programmable instructions are stored in instruction memory and control the pattern flow output.

Data Memory

Consisting of six 4Mx16 DRAM ICs and RAM addressing circuitry, the data memory stores the desired pattern that appears at the module output. The RAM addressing circuitry is merely a counter which addresses the pattern locations in data memory. When the end of the vector listing is reached, the addressing circuitry is loaded from the loop register with the address of the first vector of the listing to provide an uninterrupted vector loop. The RAM output is sent to the output driver circuit where the patterns are presented into a logic configuration usable by the output pods.

Output Driver

The output driver circuit is made up of a series of FIFO queues, latch/logic drivers, and multiplexers. The FIFO queue stabilizes and pipelines the pattern flow between data memory and the latch/logic drivers. The latch/logic drivers direct the pattern to multiplexers at ECL voltage levels.

The multiplexers, one per channel, direct the programmed data patterns to the output channels. The single-ended ECL-level signals are converted to differential signals, which are routed to the output cables and to the pods. Note that the differential ECL output signal of the pattern generator modules not suited to directly drive ECL circuitry.

Clock Circuit

The clock circuit paces the instruction memory, data memory, and the FIFO pattern queue and multiplexers in the output driver according to the desired data rate. Two phase-locked loops drive the clock circuit according to the user-selected data rate. The output of the multiplexer, which represents the user-selected clocking rate, is distributed to the above listed subcircuits on both the master board and all expander boards that are configured with the master board.

The output of the clock select multiplexer is also distributed to an external clock out circuit. The clock signal is routed to a bank of external clock delay select multiplexer. The output of this multiplexer, which represents the desired clock delay, is directed to the external clock out pin on the clock pod. Consequently either the internal clock or external clock is redirected to the clock out pin with a user-selected clock delay.

CPU Interface

The CPU interface is a single programmable logic device (PLD) which interprets the mainframe backplane logic and translates the logic into signals to drive and program the pattern generator module.

Pod

The Clock or Date Pod converts the differential output ECL signal to logic levels of interest. Because the output of the pattern generator module cannot directly drive ECL circuitry, the Clock and Data Pod is required to interface the pattern generator with the system under test.

Index

R

S

T

U

V

W

Sixth Edition, October 2014

16800-97014

www.keysight.com

KEYSIGHT
TECHNOLOGIES