KEITHLEY

Lab Notes

Model 82 C-V System

A Series of Experiments

Preface 2

Introduction 5

Experiment 1:
Basic Capacitance-Voltage Measurement 11

Experiment 2:
Use of Bias Temperature Stress for Determining
Mobile Charge in the Oxide 16

Experiment 3:
Use of the Triangular Voltage Sweep Method for
Determining Mobile Oxide Charges 18

Experiment 4:
Elimination of Series Resistance in
C-V Measurements 20

Experiment 5:
Measurement of Interface Trap Density by Combined
High and Low Frequency Capacitance Curves 22

Appendix 24

Preface

A Metal-Oxide-Semiconductor (MOS) capacitor is a simple structure. **Figure 1b** is an example of the construction of a capacitor. The metal provides one contact and its area defines the area of the capacitor. The semiconductor provides the other contact, while the oxide works as the dielectric. The most common materials used for this device include aluminum for the metal, silicon for the semiconductor, and silicon dioxide for the oxide.

A voltage applied across the device can change the capacitance of the MOS capacitor. The capacitance changes because the semiconductor depletes of charge in the region next to the oxide. This region becomes a dielectric, due to its inability to contain charge carriers, much less conduct them. The depletion region capacitance acts like a capacitor in series with the capacitor formed by the oxide, so the capacitance across the device drops as the depletion region becomes wider. This drop in capacitance, based on an applied voltage, is the most important property for this device, and performing capacitance-voltage (C-V) measurements to monitor this change describes the device very accurately.

The energy diagrams show how the semiconductor re-acts to differing voltages applied to the gate metal. The energy diagrams in **Figure 1** illustrate how a semiconductor doped n-type would react to applied voltages. Applying a positive voltage to the gate causes negative charges to collect at the semiconductor-oxide interface. **Figure 1a** shows this state of the semiconductor called accumulation. The build-up of charge at the silicon-oxide interface causes the bending of the conduction (upper) and valence (lower) bands. The straight, solid line in the middle is the Fermi level. The Fermi level represents where the probability of an electron existing in an open state is one-half. The dashed line is the mid-gap where an undoped and unbiased semiconductor would have its Fermi level. The valence and conduction bands represent energy levels where many electron states exist and conduct current. A state is an energy level where an electron can exist according to quantum physics and Schrodinger's equation. An open state is one of these quantum levels that has no electron in it. A free open state is a quantum state that has no electron in it and which has an equivalent state in the molecules surrounding thus allowing for the conduction of current. There are no free open states between the valence and conduction band of a semiconductor, only trap levels.

The energy diagram shown in **Figure 1c** shows the semiconductor in the state of depletion. A small, negative voltage applied on the gate repels the electrons in the conduction band away from the interface, creating an area where a positive charge develops due to the ions with missing electrons. This area of positive charge is the depletion region, because the applied voltage depleted the region of the majority carrier for this type of semiconductor, electrons. The depletion region contains no free charges because the voltage on the gate repels electrons, but not enough electrons to create current carrying holes in the valence band. Majority carriers are the type of current carriers, electrons or holes that exist in majority when the semiconductor has no applied voltage to change it. Minority carriers are the opposite type of current carrier. The minority carriers exist in fewer numbers in the silicon at equilibrium (no applied voltage), and disappear quickly upon forced entry into a type of semiconductor where they are a minority. As can be seen in **Figure 1d**, charges collect on the metal-oxide interface to counter the charges created in the semiconductor by the applied voltage.

The energy diagram of **Figure 1e** displays the start of inversion. Inversion occurs when the applied voltage has pushed the Fermi level at the semiconductor-oxide interface just past mid-gap. In this case, the voltage pushes the conduction band electrons away and starts repelling electrons in the valence band. This creates holes, open states where electrons can freely exist, in the valence band. Threshold occurs when the Fermi level reaches a point at the semiconductor-oxide interface that is as far on the other side of the mid-gap as the Fermi level was before application of a gate voltage. This

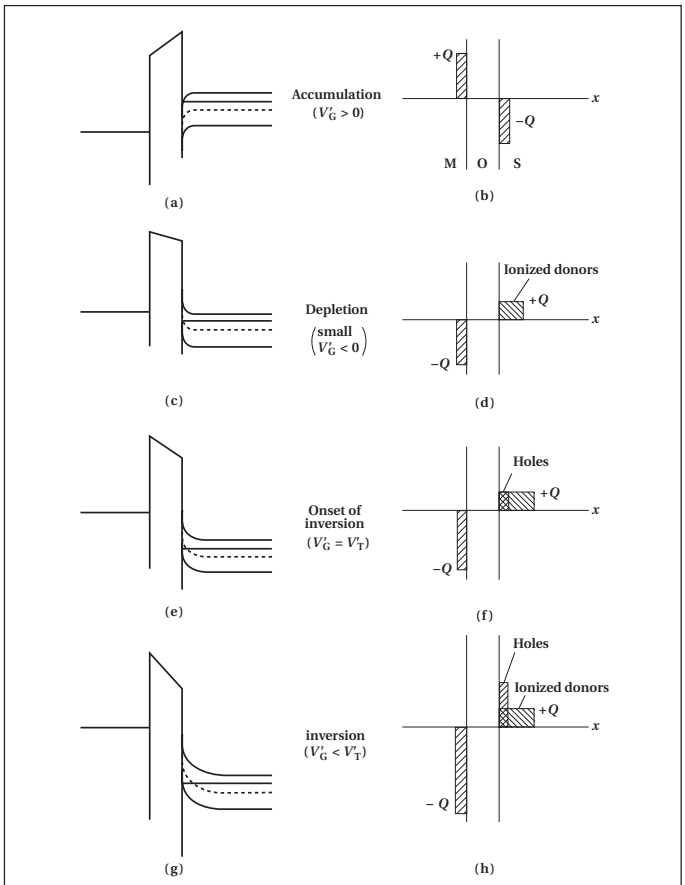


Figure 1. Energy band diagrams and corresponding block charges diagrams describing the station state in an equal **n**-type MOS-capacitor.

creates two areas where charge accumulates in the semiconductor. One area occurs at the semiconductor-oxide interface, where increased voltage creates more holes in the valence band. The other, temporary area, is the edge of the depletion region, where the voltage can push electrons in the conduction band away from their donor ions creating more positive ions. **Figures 1g and 1h** show what happens as a source applies more negative voltage and the device goes further into inversion.

The diagrams in **Figure 2** show the same regions for a p-type semiconductor. P-type semiconductors start off with holes in the valence band with no voltage applied. More holes appear in the valence band with the application of a negative gate voltage, causing the p-type version of accumulation. **Figure 2a** demonstrates this graphically. It is equivalent to **Figure 1a**, but for the opposite type of majority carrier.

Figure 2b shows depletion for a p-type MOS capacitor. It is very similar to the bending of the conduction and valence bands for a n-type semiconductor. The differences are that the bands bend the other way and the gate voltage is positive. **Figure 2c** shows what the p-type threshold looks like. The voltage is positive and the Fermi level is the same amount above the mid-gap as it originally appeared below the mid-gap. The figure shows an accumulation of electrons at the semiconductor-oxide interface.

The capacitance of the capacitor changes as an outside source applies a voltage. The equation for capacitance is the amount of charge that accumulates at the dielectric interfaces divided by the change in voltage used to accomplish the charge accumulation. Two different types of C-V measurements need investigation. The first involves a low frequency, or DC, voltage signal; while the second involves a high frequency AC voltage signal. These two methods produce two different curves upon reaching the inversion region. The low frequency measurement places a low frequency AC voltage, typically a DC voltage added to a DC voltage ramp, across the capacitor. The high frequency measurement adds a high frequency AC voltage signal to a similar DC voltage ramp. The voltage ramp provides a basis for determining what the voltage is across the device and causes the device to transfer through accumulation, depletion and inversion.

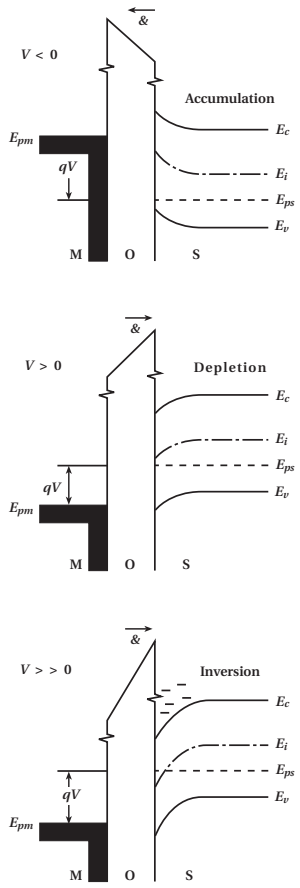


Figure 2. Effects of applied voltage on the ideal MOS capacitor:

(a) negative voltage causes hole accumulation in the p-type semiconductor,

(b) positive voltage depletes holes from the semiconductor surface,

(c) a large positive voltage causes inversion – a "n-type" layer at the semiconductor surface.

Both methods produce the same capacitance when an applied voltage places the device in accumulation. That value is the capacitance of the oxide, because the charges collect at the oxide interface in both frequency cases. Varying the voltage causes the amount of charge to change at the interface. **Figure 3a** shows the areas of charge change with a voltage change. As the device enters depletion, the charges start to accumulate as ions. When the source changes the voltage, the device responds by exposing more ions in the silicon further from the oxide. This leads to a series capacitance demonstrated in **Figure 3b**. The capacitance of the oxide is in series with the depletion region capacitance because the charge changes at the far end of the depletion region.

In inversion, the two methods separate. In both cases, the voltage ramp starts to accumulate charges at the oxide interface. The low frequency AC signal added to the voltage ramp gives the depletion region enough time to create carriers that collect at the oxide interface. This means, changing the voltage changes the charge at the oxide interface. The low frequency capacitance returns slowly to the higher capacitance value of the oxide. **Figure 3c** demonstrates the area of changing charge. The high frequency AC signal does not give the semiconductor enough time to create minority carriers, so a voltage change causes the depletion region to grow. The capacitance will remain equal to the oxide capacitance and the depletion region capacitance in series. This capacitance remains approximately constant through the inversion region, because the voltage ramp creates minority charges at the oxide interface and the depletion region does not grow. **Figure 3d** shows this type of charge accumulation.

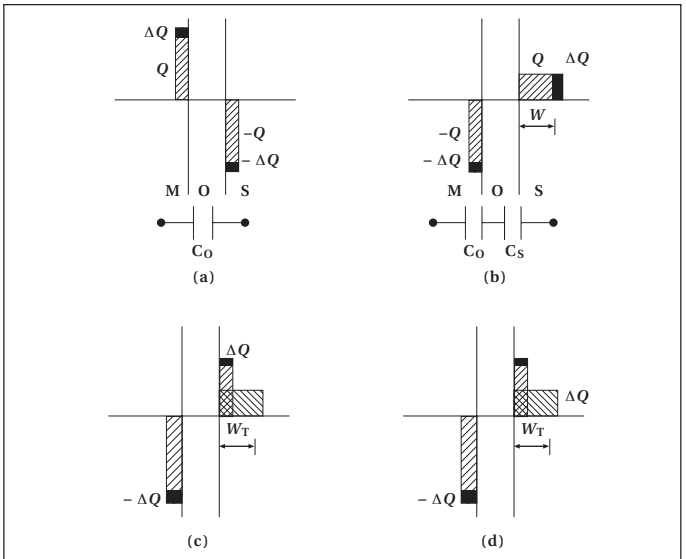


Figure 3. AC charge fluctuations inside a MOS-capacitor under DC biasing conditions corresponding to (a) accumulation, (b) depletion, (c) inversion when w – 0, and (d) inversion when W. Equivalent circuit models appropriate for accumulation and depletion biasing are also S beneath the block charge diagrams in parts (a) and (b) respectively.

Introduction

This Lab Note contains information on using the Model 5957 C-V software, and demonstrates the features of the Model 82-DOS Simultaneous C-V System. By using the Model 5957 C-V software, it is possible to test any type of two-terminal capacitor, including MOS capacitors and MOSFET gates.

The following are typical tests that the Model 82 system performs, and which later experiments demonstrate:

- Basic Simultaneous Capacitance-Voltage (C-V) measurements
- Bias-Temperature Stress (BTS) and Triangular Voltage Sweep (TVS) methods for determining oxide charges
- Series resistance measurements and compensation for effects
- Interface trap density plots for the band gap

Required Equipment

Hardware Requirements

Table 1 summarizes the equipment necessary to run the Model 5957 software.

Table 1. Required Equipment

Qty.	Equipment
1	Model 230-1 Voltage Source
1	Model 590 C-V Analyzer
1	Model 595 C-V Meter
1	Model 5951 Remote Input Coupler
1	Model 5909 Calibration Set
1	Faraday cage or large black box
1	Microscope for probe placement
2	Needle probes with wire connections
1	Hot chuck (for temperature-based measurements) or regular chuck
1	IBM-PC AT or compatible computer with EGA or CGA adapter and monitor
1	CEC PC-488, IOtech Personal488, or National Instruments PC-II or PC-IIA IEEE-488 interface
2	Model 7007-1 shielded IEEE-488 interface cables
1	Model 7007-2 shielded IEEE-488 interface cable
5	Model 4801 BNC low noise cables
3	Model 7051-2 BNC cables
1	Ribbon cable (supplied with Model 5951)

Notes:

1. The primary addresses of the Models 230-1, 590, and 595 are 13, 15, and 28 respectively. On the 595 and 590, use the front panel MENU buttons to set the addresses, if required. Set the 230-1 address using the dip switches on the rear panel.
2. The I/O address, DMA status, and interrupt level of the IEEE-488 interface card in the computer must be the same as those of the IEEE-488 driver software. See the driver software installation procedure for the card for details.
3. To obtain hard-copy plots, connect a supported plotter or printer. Refer to the manual for specific instructions on plotter and printer setup.

Software Requirements

In addition to the 5957 and driver software supplied, the Model 82 requires the following software:

- MS-DOS or IBM-PC DOS version 3.2 or higher

For those who wish to modify the supplied 5957 C-V program, the following software is necessary:

- Microsoft BASIC version 7.1 or higher

System Configuration

Figure 4 shows the overall system configuration for the Model 82. Connect all the cables as shown in the diagram.

Model 82 Connections

Figure 5 shows how to connect the Model 5951 Remote Input Coupler to the Model 590. Take one low noise Model 4801 cable and connect the 590 INPUT on the front of the 590 to the TO 590 INPUT on the back of the 5951. Use another Model 4801 cable and connect the 590 OUTPUT also on the front of the 590 to the TO 590 OUTPUT on the back of the 5951. Connect two more low noise cables to the front of the Model 5951, where the input and output to the device are. Connect the dark box to the cable grounds only. If this is not possible, connect a #18 AWG wire between the dark box and the white banana jack on the back of the 595.

Figure 4. System Block Diagram

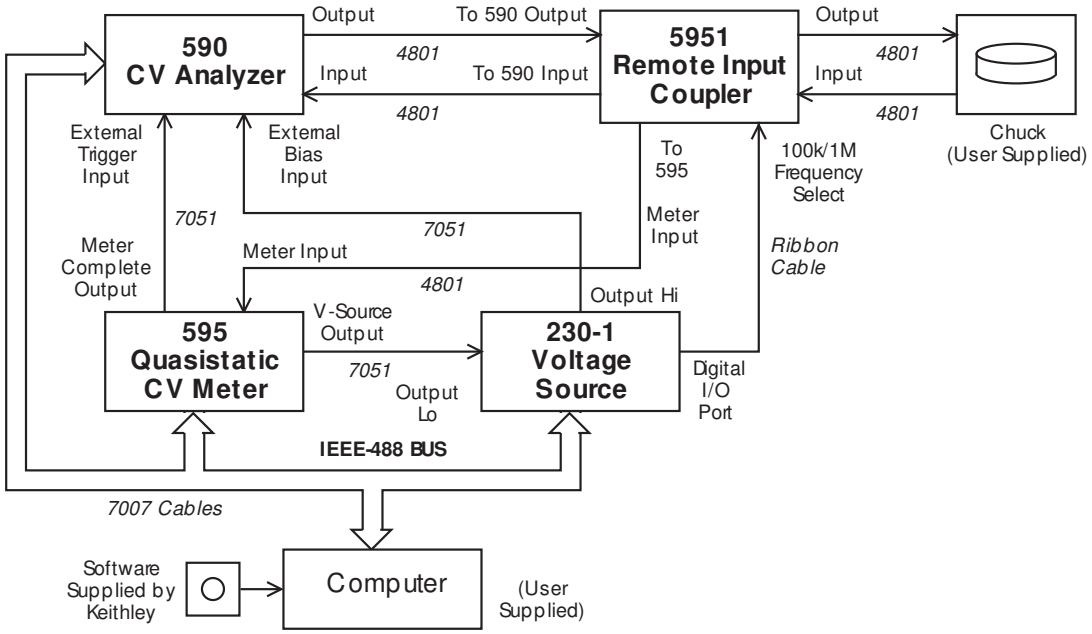


Figure 5. System Front Panel Connections

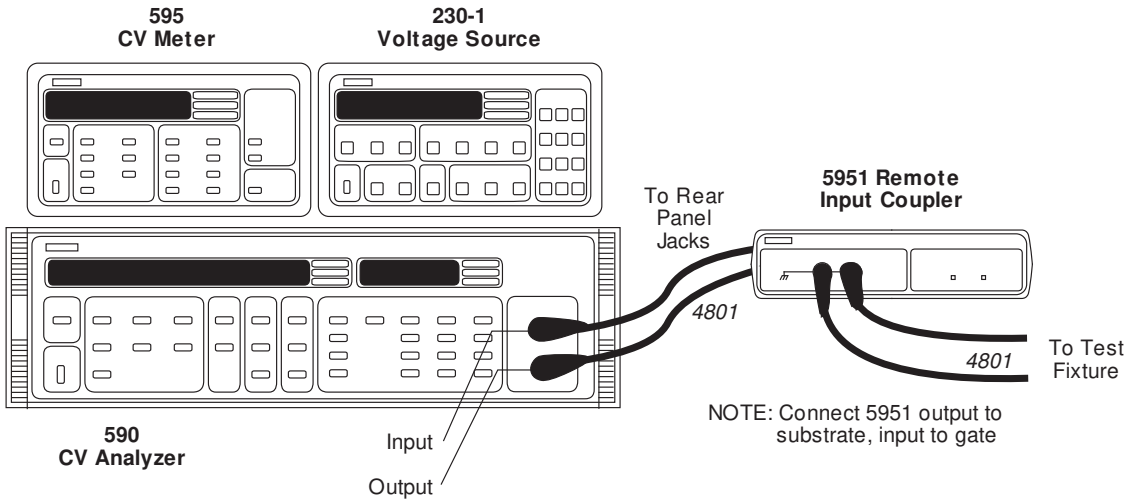


Figure 6 shows the rest of the main cabling configuration. Take the final Model 4801 cable and connect the METER INPUT on the back of the 595 to the TO 595 INPUT on the 5951. Take a Model 7051-2 BNC cable and connect the METER COMPLETE port on the back of the 595 to the TRIGGER INPUT on the back of the 590. Take another 7051-2 cable and connect the OUTPUT HI on the back of the 230-1 to the BIAS INPUT on the back of the 590. Use the remaining BNC cable to connect the OUTPUT LO on the back of the 230-1 to the VOLTAGE SOURCE OUTPUT on the back of the 595.

Next, attach the power cords to the devices. Take the ribbon cable and connect the DIGITAL I/O PORT on the back of the 230-1 to the TO 230-1 DIGITAL I/O on the back of the 5951. Take the power cables and plug in the units. **Figure 7** shows how to connect the IEEE-488 bus cables. Take the IEEE-488 bus cables and connect the 590, the 595, and the 230-1 to the IBM PC through the IEEE-488 card.

Figure 6. System Rear Panel Connections

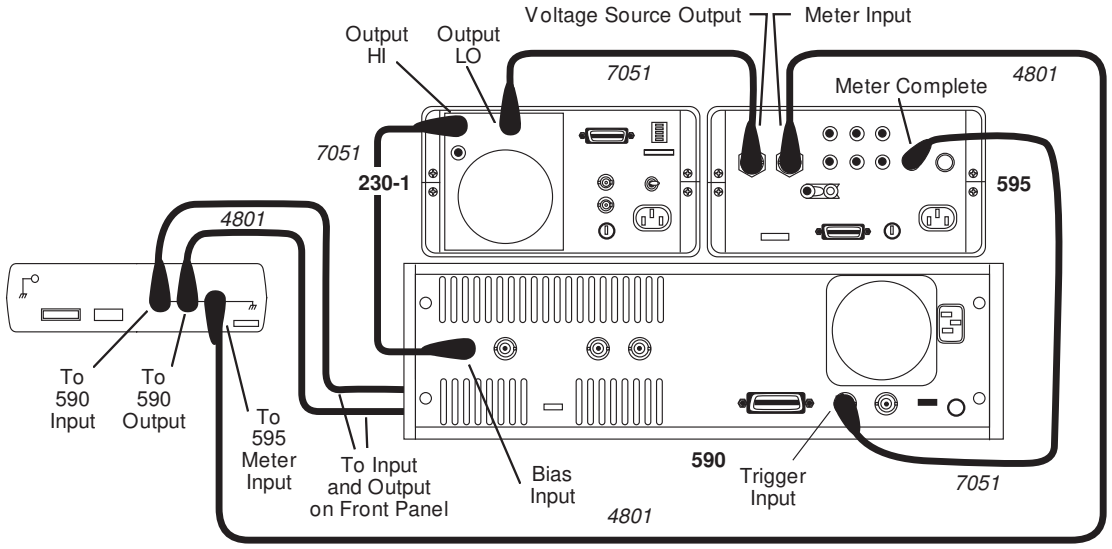
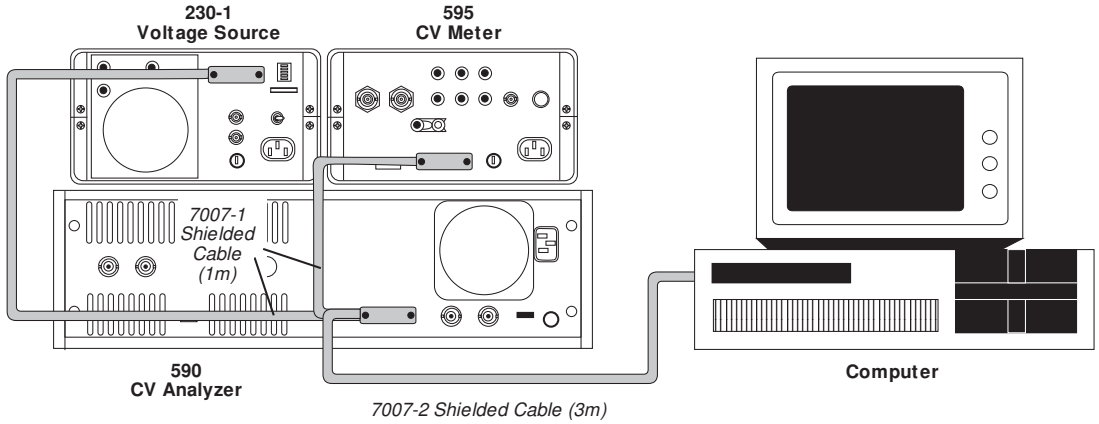


Figure 7. System IEEE-488 Connections



Software Installation

Software Backup

Before using the software for the first time, make a working copy to protect the integrity of your software. To do so, either use the DOS DISKCOPY command, or perform a Copy *.* procedure. Refer to the manual for more information.

IEEE-488 Board Parameters

Before installation, note the interface board settings in **Table 2** to enable proper configuration of the bus driver software during driver software installation.

Table 2. IEEE-488 Board Settings

Setting	Value
I/O port address	
DMA status	
Interrupts	
System Controller	

Proceed as follows:

1. Restart the computer.
2. Place the accompanying software in the appropriate drive of the computer.
3. Change the prompt to the appropriate drive by typing the drive name and : and Enter.
4. Type INSTALL and press Enter.
5. At the prompts, respond to the questions for directories, installation defaults, the graphics card, printer, and plotter.

Refer to **Table 2** for the installation defaults. **Table 3** lists the default directories. Refer to **Table 4** and the manual for the graphics cards supported. Usually, IBM EGA is compatible with all graphics cards. **Table 5** and the manual list the supported printers and plotters.

Table 4. Graphics Cards Supported by Model 82-DOS

Graphics Board	Mode	Resolution (pixels)
IBM color board	monochrome	640 × 200
Tseng EVA		640 × 480
Tecmar Graphics Master	monochrome	720 × 700
	16 color	640 × 400
Hercules Monochrome	monochrome	720 × 348
Enhanced Graphics	16 color	640 × 350
Adapter (EGA)	monochrome	
TeleVideo AT	monochrome	640 × 400
TeleVideo HRCGB	16 color	640 × 400
Sigma Color 400	16 color	640 × 400
AT & T 6300	native graphics	640 × 400
Corona PC	native graphics	640 × 325
Corona PC400	native graphics IBM	640 × 400
	emulation	640 × 200
Corona ATP	monochrome	640 × 400
H.P. Vectra	monochrome	640 × 400
T.I Professional	monochrome	720 × 300
Genoa SuperEGA HiRes	16 color	800 × 600
IBM VGA or compatible	16 color	640 × 480
	monochrome	640 × 480

Table 3. Default Directories

Sub-directory	Contents
C:\KTHLY_CV	
C:\KTHLY_CV\MODEL82	.EXE, configuration file, config.gpc .FNT or other files needed by .EXE cable calibration file, CABLECAL.EXE; file merge, FILEMRG.EXE
C:\KTHLY_CV\MODEL82\DAT	Data files, *.DAT
C:\KTHLY_CV\MODEL82\PAR	Test files, *.PAR
C:\KTHLY_CV\MODEL82\SRC	Source code, library, and utilities to re-build
C:\IEEE488	IOtech DRIVER488 GPIB board driver software.

Note: C:\IEEE488 is not created by Model 82-DOS installation program. Refer to bus driver installation instructions.

Table 5. Supported Printers and Plotters

Printer/Plotter
C. Itoh Prowriter; NEC 8023;8025
Epson FX,RX; Cannon BJ80
Okidata 92,93
IBM Graphic or Professional; Epson MX
Tektronix 4695 ink jet printer
Toshiba P321 and P351 (with unidirectional printing)
Corona Laser printer - REQUIRES AN EXTRA 128k OF MEMORY
Houston DMP-xx plotters
Hewlett-Packard HP-GL plotters
C. Itoh 24LQ
Watanabe Digi-Plot plotter
Epson LQI1500
Smith Corona D100
Epson HI-80 plotter
Hewlett Packard LaserJet+ (or compatible)
Micro Peripherals 150, 180
Okidata 192+ (eight bit graphics)
CALCOMP ColorMaster (BEING TESTED)
Toshiba 1340 (No unidirectional)
HP ThinkJet (SW5 up) (6.5x8.5 in.)
Roland DXY-800 Plotter
Toshiba P351C with color ribbon
NEC Pinwriter P series
Quadram QuadLaser (with vector software)
NEC Pinwriter P series with color ribbon

Calibrating the System

Follow the procedure below to calibrate the devices and compensate for cabling effects.

1. At the prompt, change to the hard drive by pressing C: and Enter. Also, change the directory to \KTHLY_CV\ MODEL82. Start the program by typing CABLECAL and press Enter.
2. Once loaded, press Alt-F to open the file menu. Use the arrow keys to find open file and open the PKG82CAL.CAL file. If this file doesn't exit, it will be created at the end of the procedure.
3. Press Alt-E to open the execute menu. Use the arrow keys to move the cursor down to Cable Cal Model 82. This starts calibrating the system for the cables.
4. Press in 1kHz, 100kHz, and 1MHz values for the capacitors where requested using the TAB to change selections. Use the Model 5909 calibration set supplied with the system. Alternate capacitors, in the same ranges as those in the Model 5909, need measurement at the different frequencies on a different calibrated device to obtain accurate capacitance measurements. Select OK when done to begin the calibration.
5. Choose CAL Model 82 to start the calibration. Follow the prompts and put the capacitors on as requested. If it asks for an open circuit or no capacitor, disconnect the capacitor from the end of the cables.
6. After calibration is complete, press Alt-F and select Save As. Use for the filename, when requested, PKG82CAL.CAL and then select Exit.

Running the 5957 C-V Software

Follow this general procedure to start the software and ensure the connections are correct.

1. In the \KTHLY_CV\MODEL82 directory, type KI82CV and return.
2. Press 2 at the Model 82 main menu to access the measure stray capacitance and leakage currents menu.
3. Press 1 to access the set measurement parameters menu. Fill in the parameters as follows:
   Range: 1
   Freq: 2
   Model: 1
   Start V: A normal starting voltage (10V)
   Stop V: A normal stopping voltage (-10V)
   Bias V: 0 V
   TDelay: 0.07 sec.
   Step V: 100 mV
   CCap: 1
   Filter: 2

   Then press E to exit and return to the measure stray capacitance and leakage current menu.
4. Press 2 to get to the measurement screen.
5. Press Z to zero the units.
6. Leave the probes off devices or connect a calibration capacitor while this measurement is being performed. Press S to sweep the voltages.
7. At the end of the sweep, press 4 to enter the graphing menu.
8. Press 2 to check the graph of Q/t current against time. If the curve has a slope or the curve is not less than 2pA (correct capacitance), then check the cables for correct connections. These two results indicate a leakage resistance and an offset current respectively. Press 8 to exit the Q/t graph and press 7 to view the C_q and C_h curves. Offset between curves should be less than 1%. Capacitance noise should be less than 2pF.

Recommended Devices

Table 6 lists the test devices necessary to perform the example tests below exactly as written. Substitute different, similar devices invoking minor changes to the test procedures as required.

Table 6. Recommended Devices for Test Examples

Example	Description	Recommended Devices
1	Basic MOS capacitance	1600 pF capacitor 20 pF capacitor 180 pF capacitor
2	BTS oxide charge	1600 pF contaminated oxide capacitor
3	TVS oxide charge	800 pF contaminated oxide capacitor 800 pF uncontaminated, high interface Trap density capacitor 800 pF uncontaminated, low interface Trap density capacitor
4	Series resistance	1600 pF capacitor 100 resistor 10 k resistor Pomona box
5	Interface traps	1600 pF high interface trap density capacitor 1600 pF low interface trap density capacitor

Experiment 1: Basic Capacitance-Voltage Measurement

Theory

C-V measurements are very useful in determining many of the characteristics of a particular MOS device. Capacitance measurements are useful in the modeling of the MOS structure for circuits. The Model 82 Simultaneous C-V system calculates specifications such as conductance and interface traps from the measurements.

The general method of measuring C-V curves involves performing a DC voltage sweep with a high frequency AC signal added to the DC voltage curve and later performing another measurement with a low frequency AC signal added. This causes problems in calculating specifications for the device if mobile charges in the oxide shifted the C-V curves and production of a low enough frequency source was difficult.

The Model 82 avoids these problems by performing high frequency and low-frequency measurements at the same time. It accomplishes the combined measurement using a quasistatic measurement in place of the low frequency measurement. For the high frequency measurement, the Model 590 places a 15mV rms signal of 100kHz or 1MHz on top of the DC voltage sweep. It steps the DC voltage and then measures the AC current through the MOS device. The Model 590 calculates the capacitance using the current and phase shift. It measures the current for the high frequency capacitance while the quasistatic meter is waiting to make its charge measurement.

The Model 82 accomplishes quasistatic measurement by using DC current. The Model 595 has an operational amplifier set up as an integrator with a switch to discharge the capacitor between measurements. Before the voltage step, the switch disconnects as an interior device measures the output voltage of the operational amplifier. The Model 595 steps the voltage and waits for the programmed delay time until it makes another measurement of the output voltage of the operational amplifier. It determines the capacitance by multiplying the capacitance of the integrator by the change in output voltage and dividing by the change in input voltage. This capacitance, is the capacitance mid-way between the voltages of the voltage step. The software adjusts the capacitance to the value expected at the voltage the Model 590 measured at. These methods enable the simultaneous measurement of the high frequency and quasistatic C-V curves.

Measurements performed by the Model 82 allow extraction of many of the MOS structure specifications. Primary among these is the threshold voltage. The calculations necessary for this require finding the flat band voltage. The Model 82 finds the flat band voltage by calculating the flat band capacitance using the C_{OX}, the area of the metal, and the doping of the bulk material to perform the calculation. C_{OX} is the capacitance of the oxide, so the unit uses the high frequency capacitance in deep accumulation. The device uses the same constants in the calculation of threshold voltage. These calculations are very useful in modeling the device for circuit calculations. (See ref. 1)

Record the gate areas or oxide thicknesses of the capacitors used for this lab in **Table 7**. If using different capacitance devices, substitute values.

Table 7. Recommended Devices and Information Required

Suggested Capacitor Values	Gate Area or Oxide Thickness
1600 pF	
20 pF	
180 pF	

Procedure

1. Place a 1600pF capacitor in a shielded dark box. The device is in a dark box to prevent light generation of extra carriers, which will affect the measurement. Isolating the device from electromagnetic disturbances prevents the Model 595, which is measuring very small currents, from jumping and producing huge errors due to noise produced when people walk by the test in progress.
2. Start the measurement program by moving to the \KTHLY_CV\MODEL82 directory and typing KI82CV. The Model 82 main menu should appear on the screen.
3. Access the measurement parameters menu.
   A. At the main screen press 3 (Compensate for Rseries and Determine Device Parameters) and Enter to access the device parameters screen.
   B. Next, press 1 (Set Measurement Parameters) and Enter to access the measurement parameters menu.
4. Set up the parameters to perform a voltage sweep to determine where accumulation and inversion occur and how wide the depletion region is. Select the following parameters:

   Range: 2 For an unknown device, use the highest range (2nF) to prevent out of range errors. If the device is less than 200pF, then use the 200pF range.

   Freq: 1 The user may select the frequency of the high frequency sweep for 1MHz or 100kHz, typically use 100kHz.

   Model: 1 The parallel model uses a constant conductance in correcting the capacitance values found by the device. The series model calculates the resistance at each measurement point, which changes with interface traps,

before correcting the capacitance. The parallel model gives much better data for the calculation of the effects found by the Model 82.

Start V: 1MV per cm of oxide thickness (or 10V). The starting voltage varies with the device. If it is a p-type and the threshold voltage is near 0, then this should be a positive value. If it is a n-type, this should be negative. This value should be fairly large to give a wide enough range for finding the inversion, accumulation and depletion regions.

Stop V: negative of Start V. The stop voltage is similar to the start voltage. Make sure it is less than 40V from start to stop voltage, but large enough to generate 50 measurement points with the following formula:

Points = |Start V - Stop V| / Step V - 7.

Bias V: 0V. Leave the bias voltage at 0V. Use a bias voltage only if the device being tested has very mobile carriers.

TDelay: 0.07 sec. The delay time is how long the Model 595 waits before stepping the voltage. Set the delay time at 0.07 for this experiment. This should be as low as possible to increase the speed of measurement.

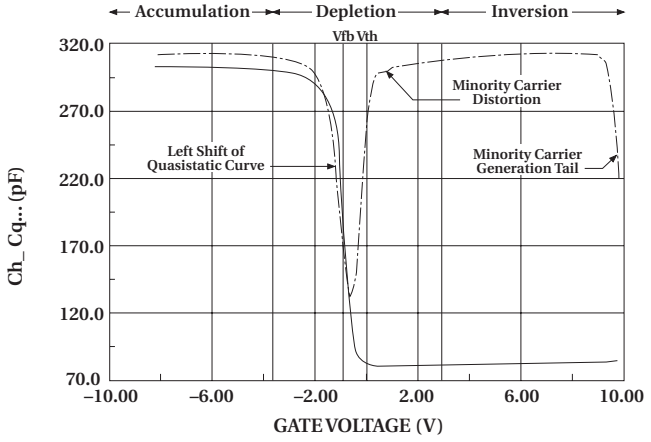
Step V: Choose the largest step voltage that gives at least 50 data points. The step voltage determines how much the Model 595 changes the voltage at each step.

CCap: 1 CCap stands for corrected capacitance. The Model 82 uses the corrected capacitance to correct the quasistatic capacitance for oxide leakage. Only use CCap on oxides with high leakage.

Filter: 2 The filter cuts down on the noise from the cables. Always leave enabled. Check the parameters to ensure correctness and press E and Enter twice to exit this part of the program.

5. Prepare the Model 82 for a measurement sweep.
   A. Press 2 (Run Diagnostic C-V Sweep) and Enter to get to the measurement screen.
   B. Lift the probes OFF the capacitor and press Z to zero the capacitance meters.
6. Run a voltage sweep and generate a C-V curve.
   A. Place the probes on the device. Pick a capacitor and locate the probe over it. Connect the input probe to the gate and the output probe to the substrate or chuck. Try to place the probe in the middle of the device pad. The probe will be on the device when the computer displays capacitance readings much larger than zero.
   B. Flash the capacitor with light and press S to perform the C-V sweep. Flashing the capacitor with light generates minority carriers in the silicon. Minority carriers at the silicon-silicon dioxide interface cause the quasistatic capacitance to rise back to C_{OX}. Setting the bias voltage into inversion and waiting for the minority carriers to build up takes too long and does not generate enough to raise the quasistatic capacitance back to C_{OX} before the delay time sweep. For this reason, use a light to generate minority carriers to give a good reading.
   C. Once the unit completes the sweep, press any key to return to the main menu.
7. Determine the range, start and stop voltages, and step voltage.
   A. Press 3 (Graph Diagnostic Sweep Data) and Enter to access the graph. The graph should appear like **Figure 8**.

Figure 8. Initial C-V Curve for Finding Voltage Limits



   B. Set C_{OX} equal to the maximum high frequency capacitance present. C_{OX} is the capacitance when the MOS device is in deep accumulation. Record this value on the line below.

$$C_{OX} = (\_\_\_\_\_) \text{ pF}$$

   C. Input the minimum high frequency capacitance as C_{MIN}.
   D. Input the area of the capacitor using the gate area from **Table 7**.
   E. Enter the doping concentration as suggested on the display. The value should read something similar to ±5E+15. It should equal approximately the doping concentration of the silicon beneath the oxide in the device. Note that parameters used for steps 7B through 7E give an initial analysis only and later steps adjust them.

F. The quasistatic curve may have distortions due to a voltage sweep that is too fast. Distortions that occur include: a negative shift of the quasistatic curve, a narrowing of the depletion region, a quasistatic generation tail, and an inability to return to C_{OX} during inversion. Step 9 corrects these problems by determining the equilibrium delay time. If unable to determine an accurate depletion region, return to step 4 by pressing Enter, 1, and Enter. Reverse the Start V and Stop V. Exit by pressing E and Enter twice. Repeat from step 5.

G. From the graph that appears, determine the range. Use the C_{OX} value the computer requested in the above step. If greater than 200pF, the range is 2nF: Range = 2. If less than 200pF, use Range = 1. Place the value for the range in **Table 8** below.

H. Determine the start and stop voltages. Look at the inversion region on **Figure 8**. Locate on your graph where the inversion region starts. Add 1V to the magnitude of that value and place it in **Table 8** for your start voltage. Now look at the accumulation region on **Figure 8**. Locate on your graph where the accumulation region starts. Add 1V to the magnitude of that value and place it in **Table 8** for your stop voltage.

I. Finally, determine the step voltage. Take the difference between the start and stop voltages and divide by 200. Round this number to 10, 20, 50, or 100mV, whichever is closest. Also, place this value in **Table 8**.

J. Exit to the device parameters menu by pressing Enter.

Table 8. Measurement Parameters

Measured Parameter	Value
Range	
Start Voltage	
Stop Voltage	
Step Voltage	
Series Resistance	
High Frequency Gain	
Delay Time	

8. Compensate for series resistance.
   A. Press 4 (ACCUMULATION) and Enter to access the accumulation series resistance section.
   B. Press M to access the measurement parameters menu.
   C. Change the parameters to the values found in **Table 8**.
   D. Change the bias voltage to the same value as the stop voltage. This is to prepare the Model 82 to calculate the series resistance.
   E. Press E and Enter twice to exit this menu.
   F. Lift the probes OFF the capacitor and press Z to zero the capacitance meters.
   G. Replace probes on the capacitor.
   H. Press C to change the series resistance. Input the series resistance calculated by the computer and press Enter. Press Enter three times, leaving the other constants alone.
   I. Calculate the gain difference between the high frequency and quasistatic corrected capacitance. Use the following formula to calculate the needed high frequency gain, using the compensated readings, and place the value in **Table 8**:

$$\text{Gain} = \frac{1 + C_q - C_h}{C_h}$$

   J. Press G to change the high frequency gain. Do not change the C_q gain or the Cq offset, by pressing Enter twice. Input the C_h gain calculated above and press Enter. Do not change the C_h offset by pressing Enter.
   K. Reset the constants. Input the series resistance calculated by the computer. Record this series resistance in **Table 8**, because it provides a better estimation of the true series resistance. Set C_{OX} equal to the maximum high frequency capacitance The gate area or oxide thickness has not changed so press Enter twice to return to the measurement screen.
   L. Press Q to exit to the Device Parameters menu.
9. Calculate delay time.
   A. Press 5 (INVERSION) and Enter to access the Delay Time menu.
   B. Press M to change the measurement parameters.
   C. Change the bias voltage to the same value as the start voltage. Press E and Enter twice to exit. This will bias the capacitor in inversion for delay time calculation.
   D. Leave the maximum delay time as it is. A maximum delay time of 10 seconds gives a reasonable measurement time for calculating the delay time, as well as covering expected delay times.
   E. Flash the capacitor with light for three seconds. Allow the device to settle after turning off the light. Press S to start the measurements. The light will generate minority carriers to make this measurement take less time. Otherwise, the Model 82 cannot make an accurate delay time measurement. The silicon draws carriers from the measurement device to reach the correct number of minority carriers for the bias voltage applied on it.
   F. Press Enter when finished and then press G to graph data points. This graph will show the best calculation for delay time. If the quasistatic capacitance curve has

not leveled off by the end of the graph, the maximum delay was too low. Exit, increase the maximum delay time, and run the measurement again.

G. Take the point on the graph where the quasistatic capacitance curve becomes fairly horizontal (the quasistatic curve should be leveling off also) and divide that time by three. Enter this value in **Table 8**. This technique works because the device is being measured from inversion to accumulation, so the capacitor will not need time to generate minority carriers for correct inversion measurements.

H. Exit the graph by pressing Enter and press Q, then 6 and Enter to exit to the main menu.

10. Make the C-V measurement.

A. Press 4 (Make C-V Measurements) and Enter to access the device measurement menu.

B. Press 1 and Enter to access the measurement parameters. Type in the measurement parameters from **Table 8**. Check the parameters to ensure correctness. Make sure the bias voltage is zero. Save the setup by pressing *, Enter, S, Enter, and typing in a file name for the device parameters (1600 for example). Press Enter after completing the file name entry. Press E and Enter twice to exit this part of the program.

C. Press 2 (Manual Start C-V Sweep) and Enter to get to the measurement screen.

D. Lift the probes OFF the capacitor and press Z to zero the capacitance meters.

E. To run the C-V sweep repeat step 6. Note that the screen displays the current value for V during the sweep. The screen will indicate when the computer has finished the sweep.

11. Analyze the data.

A. Press 4 (Analyze Sweep Data) and Enter to access the graphing and analysis section of the software. This should bring you to the sweep data analysis page.

B. To view the C-V curves press 7 (Graph both C_q and C_h vs. Gate Voltage) and Enter. The computer displays a quasistatic and a high frequency C-V curve. Plot this graph on a connected plotter or printer by pressing 3. The computer will ask for the length of the x-axis. Press 7 and Enter if using an 8½ × 11" sheet of paper. If the computer has no printer connected, see step 12 to save the data to disk. Exit the graph by pressing 8.

C. Press 4 and Enter to access the analysis constants menu.

D. Press 1 and Enter to change the constants.

a. Leave R the same as in **Table 8**.

b. Set C_{OX} equal to the maximum high frequency capacitance. Record C_{OX} in **Table 11**.

c. The gate area or oxide thickness has not changed so press Enter twice.

d. Enter the doping concentration as suggested on the display.

e. Input the minimum high frequency capacitance as C_{MIN}.

E. C_{FB} and V_{FB} are the capacitance and voltage at flat band respectively. V_{TH} is the threshold voltage. Find all three in the table on the screen and record them in **Table 9**.

F. Press 4 and Enter to return to the sweep data analysis menu.

Table 9. 1600pF Analysis Constants

Constant Names	Values
C_{OX}	
C_{FB}	
V_{FB}	
V_{TH} (V_{thresh})	

12. Save data if necessary and exit to main menu.

A. If the computer has no printer connected, save the data to a disk for transfer to another computer for printing by pressing 1 and Enter. This will ask for a file to save the data in, a header, and a data delimiter that allows you to pick a file format that other programs can use. Follow the menus for a header until exited to the sweep data analysis screen. Then, print the graph of the quasistatic and high frequency curves against voltage on another computer, if necessary.

B. Press 18, Enter, 5, and Enter to exit to the main menu.

13. Return to the main menu and repeat steps 3 through 12 for a 20pF capacitor. Use a different name for saving the measurement parameters than what was used for the 1600pF capacitor. (Try 20pF.) Use **Tables 10** and **11** in place of **Tables 8** and **9**.

Table 10. 20pF Measurement Parameters

Measured Parameter	Value
Range	
Start Voltage	
Stop Voltage	
Step Voltage	
Series Resistance	
High Frequency Gain	
Delay Time	

Table 11. 20pF Analysis Constants

Constant Names	Values
C_{OX}	
C_{FB}	
V_{FB}	
V_{TH}	

14. Return to the main menu and repeat steps 3 through 12 for a 180pF capacitor. Use a different name for saving the measurement parameters than what was used for the 1600pF or 20pF capacitors. (Try 180pF.) Use Tables 12 and 13 in place of Tables 8 and 9.

Table 12. 180pF Measurement Parameters

Measured Parameter	Value
Range	
Start Voltage	
Stop Voltage	
Step Voltage	
Series Resistance	
High Frequency Gain	
Delay Time	

Table 13. 180pF Analysis Constants

Constant Names	Values
C_{OX}	
C_{FB}	
V_{FB}	
V_{TH}	

Analysis

1. Compare the value for C_{FB} found in the graph with the value given by the following equations:

$$C_{FB} = \frac{C_{OX}\,\varepsilon_s\,A}{(1\times10^{-16})\,(C_{OX})\,(l)+\varepsilon_s\,A}$$

$$l = (1\times10^{4})\left[\frac{(\varepsilon_s\,kT)^{1/2}}{(q^2\,N_X)}\right]$$

where: C_{FB} = flat band capacitance(pF)
C_{OX} = oxide capacitance(pF)
ε_s = permittivity of substrate material = 1.04×10^{-12}(F/cm)
A = gate area (cm^2)
l = extrinsic Debye length (m)
kT = thermal energy at room temperature = 2.5248777×10^{-2} eV
q = electron charge = 1.60219×10^{-19}C
N_X = bulk doping of the silicon in the MOS device (cm^{-3})

2. Compare the value for V_{TH} found in the graph with the value given by:

$$V_{TH} = \frac{\pm\,(\,A\,(4\varepsilon_s\,q\,|N_{BULK}|\,|\phi_B|\,)^{1/2}}{(10^{12}\,C_{OX})} + 2\,|\phi_B|\,) + V_{FB}$$

where: V_{TH} = threshold voltage(V)
A = gate area(cm^2)
C_{OX} = oxide capacitance (pF)
ε_s = permittivity of substrate material = 1.04×10^{-12}F/cm
q = electron charge = 1.60219×10^{-19}C
N_{BULK} = bulk doping (cm^{-3})
V_{FB} = flat band voltage(V)
B = bulk potential (V) = (kT/q) ln(Nx/n_I)
kT = thermal energy at room temperature = 2.5248777×10^{-2} eV
Nx = bulk doping (cm^{-3})
nI = intrinsic carrier concentration of the material = $1.45\times10^{10}cm^{-3}$

3. Compare the curves of the three different capacitors. Comment on the differences in C_{OX} and C_{MIN}. Comment on the differences in the width of the depletion region.

Experiment 2: Use of Bias Temperature Stress for Determining Mobile Charge in the Oxide

Theory

The Bias Temperature Stress (BTS) technique is the most widely used method for determining the amount of mobile charge that exists in the oxide. In this method the flat band voltage of two high frequency curves is used to determine the amount of charge. Calculation of the mobile charge concentration uses the equation:

$$\Delta V_{FB} = \frac{N\ q\ A}{C_{OX}}$$

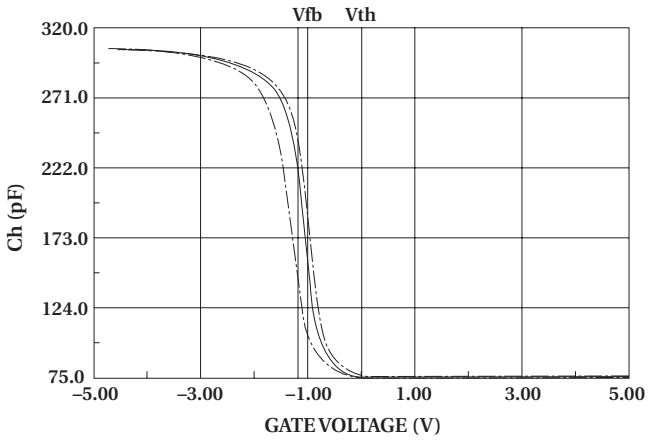
or:

$$N = Q_{eff} / q$$

where: ΔV_{FB} = the change in flat band voltage (V)
N = the mobile ion concentration per unit area (cm-2)
A = the gate area (cm2)
q = electron charge = 1.60219×10^{-19}C
C_{OX} = the oxide capacitance (pF)
Q_{eff} = the change in Q_{eff} between the negative and positive stresses (C/cm^2)
Q_{eff} = the sum of the charge in the oxide (C/cm^2)

This evaluation assumes the mobile charges are all packed up against one side or the other of the oxide during the two separate flat band measurements. The charges move to the ends of the oxide because of a bias voltage across the oxide while heating the oxide. Refer to **Figure 9** for an example of high frequency BTS curves.

Figure 9. Example of a BTS Curve



Procedure

1. Choose a wafer that has mobile charges in the oxide and find a 1600pF capacitor.
2. Place the device on a hot chuck that is able to reach a temperature of at least 300°C inside of an isolated dark box. Remove all wires and anything else that can melt at 300°C from the area of the hot chuck. The dark box prevents static noise problems that can affect the C-V measurements.
3. Turn on the computer and enter the Model 82 program to obtain the main menu.
4. Perform a room temperature C-V measurement to determine if the test device is good.
   A. Repeat steps 3 through 11 of Experiment 1, ignoring all references to **Table 9**.
   B. Re-enter the analysis constants menu by pressing 4 and Enter. Record the values for V_{FB}, Q_{eff}, and C_{OX} in **Table 14**. Press 4 and Enter when finished.
   C. Repeat step 12 of Experiment 1.

Table 14. V_{FB} Values after Different Stresses

C-V measurement after temperature stress	V_{FB} value	Q_{eff}	C_{OX}
No stress			
Positive voltage stress			
Negative voltage stress			

5. After the first C-V measurement is done, the measurement parameters need to be changed for the heating.
   A. Enter the manual C-V curve menu, from the main menu, by pressing 4, Enter, 2, and Enter.
   B. Press M to obtain the measurement parameters list. Change the following parameter:
      Start V: 10 V
   C. Exit the measurement parameter menu by pressing e and Enter twice.
6. Use the hot chuck to heat the device up to approximately 300°C with the probes contacting the device. Note: The high frequency capacitance should rise and equal the oxide capacitance. The high temperature generates minority carriers at a speed less than the period of the high frequency voltage change. This means that the charge changes at the oxide interface and the high frequency capacitance returns to C_{OX}.

A. Leave the device heated to 300°C for five minutes. As the chuck heats, the probes may lose contact with the device. If this happens, put the probe back on the device and wait an additional five minutes. Make sure the probes contact the device and measure capacitance. The voltage across the probes provides the bias that will move the mobile ions to the edge of the oxide.

B. Cool the device down to room temperature.

C. Return to the main menu by pressing Q, 5, and Enter.

D. Repeat steps 10 through 12 of Experiment 1, recording V_{FB}, Q_{eff}, and C_{OX} in **Table 14** under positive stress and ignoring all references to **Table 9**.

7. Repeat steps 5 and 6 using the following parameters:

   Start V: -10V

   Stop V: Change as necessary to obtain at least 50 samples.

   Record V_{FB}, Q_{eff}, and C_{OX} in **Table 14** under negative stress.

8. Graph the three high frequency curves from the saved data as in **Figure 9**. Repeatedly plotting the high frequency graphs on the same sheet of paper achieves this result or calling up the data in another graphing program also produces the graph.

Analysis

1. Take the V_{FB} values from the last two C-V measurements and subtract them. Solve for the mobile ion charge concentration per unit area using the equation in the explanation. Record the mobile ionic charge in the following area:

   Mobile Ionic Concentration = N = (_____) ions/cm2

2. Explain why the initial C-V curve lies between the positive and negative stress curves.

Conclusion

Mobile ions present a severe reliability issue in MOS structures. BTS will measure concentrations down to 1×10^{10} ions/cm^2. The Model 5958 C-V Software Utilities automates the task of controlling the hot chuck, acquiring the C-V curves, and calculating the mobile ionic concentration. A more sensitive measure of mobile ionic concentration involves the Triangular Voltage Sweep (TVS) technique, described in Experiment 3.

Experiment 3: Use of the Triangular Voltage Sweep Method for Determining Mobile Oxide Charges

Theory

The Triangular Voltage Sweep (TVS) method is very useful in determining the amount and type of mobile carriers that are in the oxide. This method uses a triangular voltage ramp applied to the gate of the device. The Model 595 applies a similar voltage ramp during its measurement. The Model 595 measures the ionic displacement current, while the device is at an elevated temperature. Elevating the temperature to approximately 300°C causes the high frequency curve to rise in inversion until it is similar to the quasistatic curve. If there are no mobile charges, the quasistatic curve remains approximately the same shape, except the depletion capacitance starts to approach the oxide capacitance. If mobile charges exist, a capacitance spike will appear on the quasistatic C-V curve when the mobile charges move from one side of the oxide to the other. The quasistatic curve will peak during the movement of the mobile charge. Calculation of the mobile charge involves taking the difference in the high frequency and quasistatic capacitance and multiplying by the change in V_{GS} as shown in the following:

$$N_m = \frac{+V_{GS}}{-V_{GS}} (C_q - C_h) V_{GS} / (q A)$$

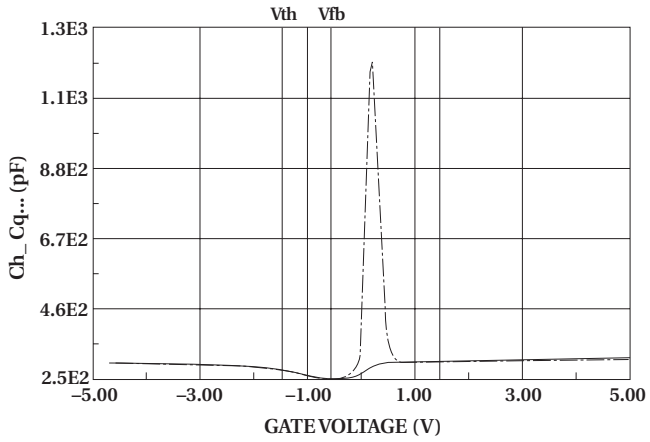
where: Nm = mobile ion concentration (cm^{-2})
$+V_{GS}$ = gate-substrate voltage (V)
$-V_{GS}$ = change in gate-substrate voltage (V)
C_q = quasistatic capacitance at given V_{GS} (pF)
C_h = high frequency capacitance at given V_{GS} (capacitance without mobile charges) (pF)
q = electron charge = 1.60219×10^{-19}C
A = area of gate capacitor (cm^2)

Figure 10 demonstrates what a contaminated oxide should produce for a TVS curve.

This method has four advantages over the BTS method:

1. It determines the mobile charges without interference from the interface trap charges.
2. It can determine the type of ion (sodium or potassium) that is contaminating the oxide, because the peak in gate current for different ions occurs at different gate biases.
3. It provides measurements an order of magnitude more sensitive than bias temperature stress BTS.
4. It is faster than the BTS method, since the device only needs heating once and the calculation needs only one curve. (See ref. 1)

Figure 10. Simultaneous TVS Plot on Highly Contaminated Wafer



Calculation of the mobile charge concentration could come from the measured V_{GS}, C_q, and C_h data. Alternatively, one can calculate the concentration graphically from the displayed simultaneous C-V curves. Contact Keithley for a modified version of the Model 5957 software, which will automatically calculate the mobile ion concentration.

Procedure

1. Choose a wafer that has mobile charges in the oxide and find a 800pF capacitor.
2. Turn on the computer and enter the Model 82 program to obtain the main menu.
3. Place the device on a hot chuck that is able to reach a temperature of at least 300°C inside of an isolated dark box. Remove all wires and anything that will melt at 300°C from the area of the hot chuck. The dark box prevents static noise problems that can affect the C-V measurements.
4. Perform a room temperature C-V measurement to determine if the test device is good. Repeat steps 3 through 9 of Experiment 1.
5. After obtaining the parameters for the first C-V measurement, the measurement parameters need to be changed for the heating.
   A. Enter the manual C-V curve menu, from the main menu, by pressing 4, Enter, 2, and Enter.
   B. Press M to obtain the measurement parameters list. Change the following parameters:

Range: As found in step 4
Start V: 5V
Stop V: -5V
Bias V: 0V
TDelay: Step V / 100mV/s
Step V: 10 or 20mV

Use these low step voltages for greatest accuracy in measurement.

C. Exit the measurement parameter menu by pressing E and Enter twice.

6. Prepare the device for the voltage sweep.
   A. Heat the device to 300°C and wait for three minutes. This allows time for the bias voltage to move all the mobile charges to one side of the oxide quickly. Make sure the probes contact the device and measure capacitance. The voltage across the probes provides the bias that will move the mobile ions to the edge of the oxide.
   B. Repeat step 6 of Experiment 1.
7. Data graphing and analysis.
   A. Press 4 and Enter to view the data graphs.
   B. Press 7 and Enter twice to view the simultaneous C-V graphs.
   C. Print the graph of the high frequency and quasistatic capacitances, or save the data to disk for later analysis. Plot this graph on a connected plotter or printer by pressing 3. The computer will ask for the length of the x-axis. Press 7 and Enter if using a 8½ × 11" sheet of paper. If the computer has no printer connected, see step 12 of Experiment 1 to save the data to disk. Exit the graph by pressing 8.
   D. Calculate the mobile ionic charge concentration from the graph or from the measured data. Write the number of mobile ions in **Table 15**. Note: View measured data by pressing 3, Enter, 1, and Enter while in the sweep data analysis menu. Calculation of mobile ion concentration involves this data and the use of the equation in the theory above. Use only data between $V_{GS} = \pm 1V$, because that will provide an accurate mobile ion concentration. When finished, press Q, Enter, 8, and Enter.
   E. Exit to the main menu by pressing 18, Enter, 5, and Enter.
8. Return to the main menu and repeat steps 3 through 7 with a device having an uncontaminated oxide and few interface traps. Record the mobile ion concentration in **Table 15**.
9. Return to the main menu and repeat steps 3 through 7 with a device having an uncontaminated oxide and high numbers of interface traps. Record the mobile ion concentration in **Table 15**.

Table 15. Mobile ion concentrations

Number of mobile ions for:	From Data	From Graph
Contaminated Oxide		
Uncontaminated Oxide with Low Numbers of Interface Traps		
Uncontaminated Oxide with High Numbers of Interface Traps		

Analysis

1. Compare the shapes of the curve from step 4 and the TVS curve. Note how the capacitance changes and the spike in capacitance in the contaminated oxide.
2. Compare the curves of the various TVS measurements. Notice the differences in the spikes and comment on any changes due to interface traps.
3. Compare the value for mobile ion charge density of the chip with contaminated oxide with the value found in Experiment 3. Compare the TVS and BTS techniques, commenting on the advantages and problems in both.

Experiment 4: Elimination of Series Resistance in C-V Measurements

Theory

Series resistance distorts the high frequency curve. As shown in **Figures 11** through **14**, increasing values of series resistance and frequency cause the high frequency capacitance to decrease and the change in capacitance between inversion and accumulation to become less. The resistor lowers the output current and causes the phase of the output to be incorrect. The phase is incorrect because the resistance adds a real component to the impedance not present in a circuit with only capacitance. The series resistance does not affect the quasistatic C-V measurement as much because it measures the capacitative charge transferred. The quasistatic C-V measurement also attempts to correct for any delay in the voltage change due to a resistance. It takes two final measurements and compares them to give the Q/t measurement.

The equation for corrected capacitance is:

$$C_C = \frac{(G_M^2 + \omega^2 G_M^2)\, C_M}{a^2 + \omega^2 C_M^2}$$

where: $a = G_M - (G_M^2 + \omega^2 C_M^2)\, R_{SERIES}$

C_C = series resistance compensated parallel model capacitance (F)

C_M = measured parallel model capacitance (F)

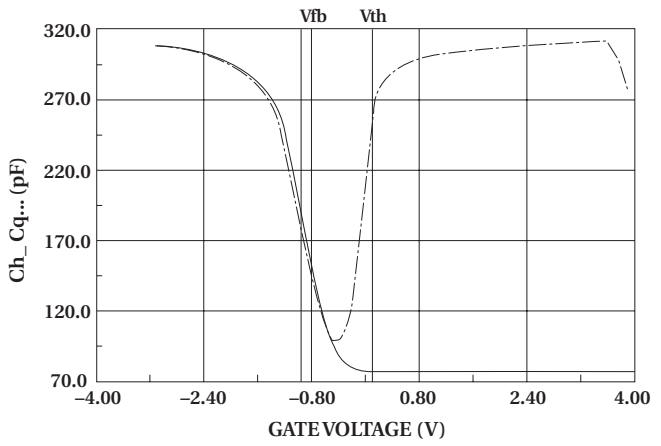
G_M = measured conductance (S) = 2f

R_{SERIES} = series resistance ()

Procedure

1. Place a 1600pF capacitor in a dark box isolated from disturbances.
2. Turn on the computer and enter the Model 82 program to obtain the main menu.
3. Perform a C-V measurement to determine the viability of the test device. Repeat steps 3 through 12 of Experiment 1, ignoring all references to **Table 9**.
4. Prepare for and take a series resistance measurement.
   A. Attach a 100Ω resistor in the measurement loop. The best place to attach the resistor uses a Pomona box (See appendix). If a Pomona box is unavailable, attempt to use the resistor as the probe for contacting the substrate, or place it between the substrate and the C-V instrument output.
   B. Leave the measurement parameters the same.
   C. Press 4 (Make C-V Measurements) and Enter to access the device measurement menu.
   D. Press 2 (Manual Start C-V Sweep) and Enter to get to the measurement screen.
   E. Lift the probes OFF the capacitor and press Z to zero the capacitance meters.
   F. Repeat steps 6, 11, and 12 of Experiment 1, ignoring all references to **Table 9**. Remember to save the data and print a graph of C_q and C_h against V_{GS}.
5. Analyze the data with the series resistance.
   A. Look at the effect of the series resistance on the high and low frequency curves on the printed graph. The graph of the high frequency capacitance, in this case, has little distortion, due to the small impedance change with a 100kHz signal on a 100Ω resistor. It should look like **Figure 11**.

Figure 11. 100Ω, 100kHz



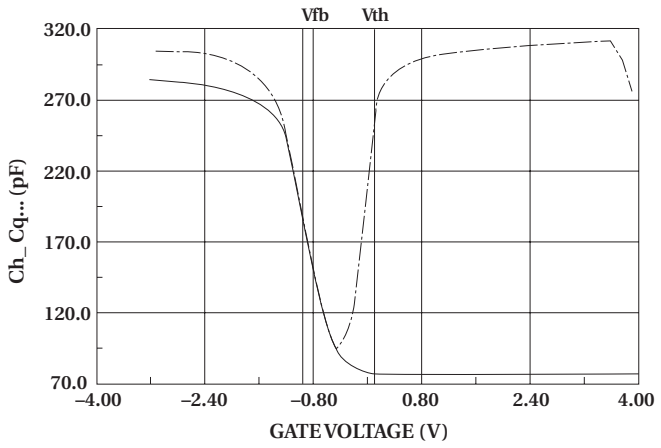
   B. Enter the Display Analysis Constants screen from the main menu by pressing 4, Enter, 4, Enter, 4, and Enter.
   C. Change the R_{SERIES} constant value by pressing 1 and Enter.
      a. Type in the computers value for R_{SERIES}.
      b. Set C_{OX} equal to the maximum high frequency capacitance. If the value presented is negative, type in 0.001 and press Enter.
      c. The gate area or oxide thickness has not changed, so press Enter twice.
      d. Enter the doping concentration as suggested on the display.
      e. Input the minimum high frequency capacitance as C_{MIN}. If this value is negative, type in 0.00001 and press Enter.
   D. Exit this menu by pressing 4 and Enter.
   E. To view the C-V curves press 7 and Enter. The computer displays a quasistatic and a high frequency C-V

curve. Plot this graph on a connected plotter or printer by pressing 3 and Enter. The computer will ask for the length of the x-axis. Press 7 and Enter if using a 8½ × 11" sheet of paper. If the computer has no printer connected, see step 12 to save the data to disk. Exit the graph by pressing 8.

F. Re-enter the measurement menu by pressing 18 and Enter.

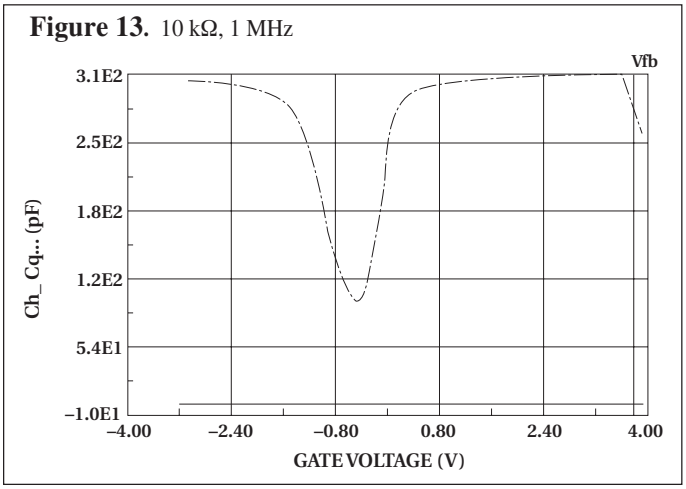
6. Perform the measurement at a higher frequency.
   A. Go to the measurement parameters menu by pressing 1 and Enter.
   B. Change the frequency in the parameters to 1MHz by typing f2 and pressing Enter.
   C. Exit the measurement parameters menu and enter the manual C-V measurement menu by pressing E, Enter twice, 2, and Enter.
   D. Repeat steps 4E and F and step 5. This high frequency curve should look like **Figure 12**.

Figure 12. 100Ω, 1 MHz



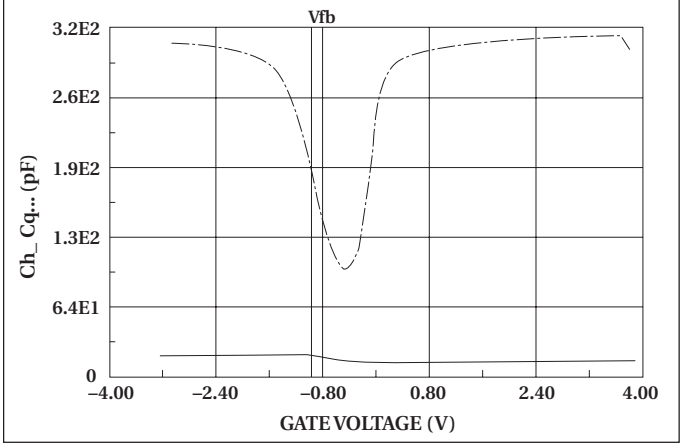
7. Change resistance.
   A. Attach a 10kΩ resistor in the measurement loop. Add the 10kΩ resistor the Pomona box as shown in the appendix.
   B. Repeat steps 4d through f. This high frequency curve should appear flat and at around 0pF. It should look similar to **Figure 13**.
   C. Enter the display analysis constants menu by following step 5b. Before correcting for series resistance, remove the high frequency gain.
      a. Begin the change by pressing 2 and Enter.
      b. Press Enter twice to skip the quasistatic gain and offset.
      c. Press 1 and Enter for the high frequency gain.
      d. Press Enter six times, until the computer asks for no more constants.
      e. Continue with the rest of step 5.

Figure 13. 10 kΩ, 1 MHz



8. Change frequencies again.
   A. Go to the measurement parameters menu by pressing 1 and Enter.
   B. Change the frequency in the parameters to 100kHz by pressing f1 and Enter.
   C. Exit the measurement parameters menu and enter the manual C-V measurement menu by pressing E, Enter twice, 2, and Enter.
   D. Repeat steps 4E and F and step 5. This high frequency curve should appear slightly higher than that for step 7. It should look like **Figure 14**.

Figure 14. 10kΩ, 100kHz



Analysis

1. Compare the initial curve taken without series resistance with the curves taken with series resistance.
2. Compare the curves obtained at the two different frequencies for the two different resistors.
3. Compare the curves obtained with the series resistance input as a constant with each other. Also compare them with the original curve that had no series resistance.

Experiment 5: Measurement of Interface Trap Density by Combined High and Low Frequency Capacitance Curves

Theory

Interface traps at the semiconductor-oxide boundary can cause profound shifts in the shape of the high and low frequency C-V curves. Interface traps come in two types, acceptor and donor. Acceptor traps are negative when filled and neutral when empty. Donor traps are neutral when filled and positive when empty. Both types of interface traps can exist at the interface, but one needs another method to determine the type of interface trap dominant in a small part of the band gap. The important fact is that both types of interface traps store charge at the interface and react to charge in the metal.

One effect of the interface traps is to spread out the C-V curve in the gate voltage axis. This is because as the gate voltage changes the energy bands at the semiconductor-oxide interface change. The bending of the bands exposes a certain amount of charge in the semiconductor at the interface, but also releases or stores charge in the interface traps. The charge at the surface of the metal must equal the charge at the surface of the semiconductor. When the charge at the metal surface changes, the additional change in charge from the interface traps causes the semiconductor charge to change less than would be the case if there were no interface traps. Because of the capacitative relation of the charge on the metal and the gate voltage, the effect of the charges from the interface traps causes the C-V curves to need more voltage to obtain the same amount of band bending and capacitance effects.

One finds the interface trap density from the interface trap capacitance. The following equation relates these two values:

(1) $$D_{IT} = (1 \times 10^{-12})\, C_{IT} / (A\, q)$$

where: C_{IT} = interface trap capacitance (pF)
D_{IT} = interface trap density at a certain energy in the semiconductor per unit area ($cm^{-2}\ eV^{-1}$)
A = gate area (cm^2)
q = electron charge (1.60219×10^{-19} C)

Using **Figure 15** and a quantitative treatment found in ref. 1, it is possible to find the interface trap capacitance through:

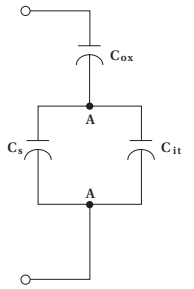
(2) $$C_{LF} = \frac{C_{LF} + (C_S + C_{IT})\, C_{OX}}{C_{OX} + C_S + C_{IT}}$$

where: C_{LF} = low frequency capacitance (pF)
C_S = semiconductor surface capacitance (pF)
C_{IT} = interface trap capacitance (pF)
C_{OX} = oxide capacitance (pF)

Solving this equation for the interface trap capacitance results in:

(3) $$C_{IT} = (1/C_{LF} - 1/C_{OX})^{-1} - C_S$$

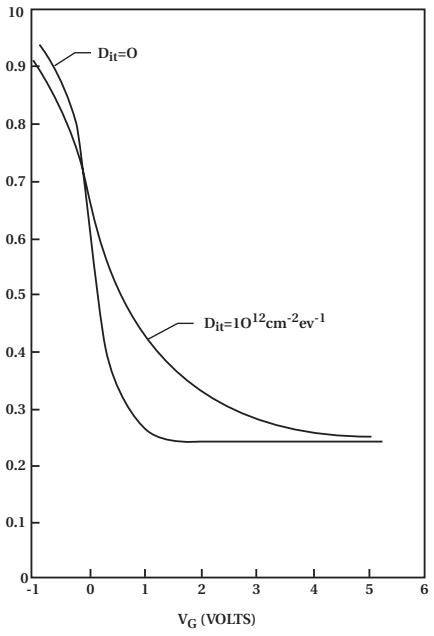
Figure 15. Low frequency equivalent circuit of the MOS capacitor.



This equation uses the same definitions of variables as the equation above.

Because a unit cannot measure the exact capacitance of the semiconductor, the Model 82 estimates it by another method. **Figure 16** shows that the high frequency capacitance has no interface trap capacitance term in it because the interface traps cannot respond to the change in voltage at the rate the high frequency capacitance changes. The equation for the high frequency semiconductor surface capacitance is:

Figure 16. Extraction of Interface Trap Properties from the Capaitance



(4) $C_S = (1/C_{HF} - 1/C_{OX})^{-1}$

where: C_S = semiconductor surface capacitance (pF)
C_{HF} = high frequency capacitance (pF)
C_{OX} = oxide capacitance (pF)

Combining equations (3) and (4) leads to the solution:

(5) $C_{IT} = (1/C_Q - 1/C_{OX})^{-1} - (1/C_H - 1/C_{OX})^{-1}$

where: C_{IT} = interface trap capacitance (pF)
$C_Q = C_{LF}$ = quasistatic capacitance (pF)
$C_H = C_{HF}$ = high-frequency capacitance (pF)
C_{OX} = oxide capacitance (pF)

The Model 82 first converts the C_{IT} (interface trap capacitance) to D_{IT} (interface trap density) by equation (1) above. Then the Model 82 calculates the interface trap energy using the band bending and the bulk potential. Finally, the Model 82 calculates the bulk potential by the equation:

(6) $B = [(kT) / q] \ln (N_X/n_I)$

where: B = bulk potential (eV)
k = Boltzmann's constant (1.38066×10^{-23} J/K)
T = test temperature (293 K)
n_I = intrinsic carrier concentration of material = $1.45 \times 10^{10} cm^{-3}$
N_X = doping at 90% W_{MAX}, or N_A or N_D if entered by the user (cm^{-3})

The band bending comes from the surface potential. The surface potential involves a summation over all the gate voltages. The equation is:

(7) $$(_{S-0}) = \sum_{V_{GS}1}^{V_{GS}\,Last} (1 - C_Q/C_{OX})\,(2V_{STEP})$$

where: $(_{S-0})$ = surface potential (V)
C_Q = quasistatic capacitance (pF)
C_{OX} = oxide capacitance (pF)
V_{STEP} = step voltage (V)
V_{GS} = gate-substrate voltage (V)

Once the measurement and summation finishes, the Model 82 uses the value of $(_{S-0})$ at flat band voltage as a reference. The program subtracts that value from the rest of the surface potential values in the column. This leaves the column with only values of $_S$ in the column. The Model 82 calculates the value of E_T by the equation:

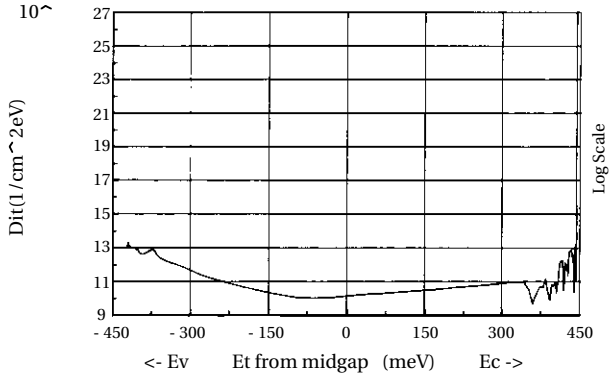
(8) $E_T = {}_{S-B}$

where: E_T = interface trap energy from mid-gap (eV)
$_S$ = band bending (V)
$_B$ = bulk potential (eV)

Procedure

1. Place a 1600pF capacitor in a dark box isolated from disturbances.
2. Turn on the computer and enter the Model 82 program to obtain the main menu.
3. Perform a C-V measurement. Repeat steps 3 through 12 of Experiment 1, ignoring all references to **Table 9**.
4. Return to the graph menu and print out the D_{IT} against E_T graph.
   A. Press 4, Enter, 4, and Enter to open the graphing menu.
   B. Press 14 and Enter to access the interface trap graph.
   C. Plot this graph on a connected plotter or printer by pressing 3 and Enter. The computer will ask for the length of the x-axis. Press 7 and Enter if using a 8½ × 11" sheet of paper. If the computer has no printer connected, see step H to save the data to disk. The graph should look like **Figure 17**. Exit the graph by pressing 8.
   D. Press 18, Enter, 5, and Enter to exit to the main menu.

Figure 17.



5. Repeat measurement with the high interface trap device.
   A. Place the new wafer on the chuck and locate a capacitor of similar size to that which was used before.
   B. Repeat steps 3 and 4 of this experiment.

Analysis

1. Compare the interface trap density curves of the two measurements. Comment on any peculiarities.
2. Compare the C-V curves obtained from the two chips Comment on the spread out of the C-V curves due to interface traps.

Appendix

Table 14 lists the parts necessary for constructing a shielded box for placing a series resistance in the measurement loop. To put these parts together, do the following:

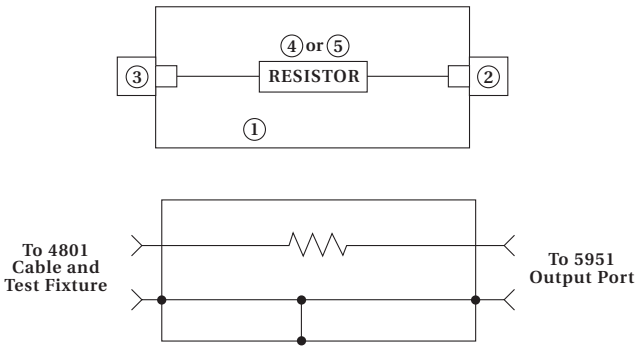
1. Open up all the parts.
2. Take the Pomona box and drill two 3/8-inch diameter holes in the ends of the box.
3. Take the BNC connectors and screw them into the drilled holes on the ends.
4. Solder the 100Ω resistor to the connectors on the inside.
5. Repeat steps 1 through 4 with the 10kΩ resistor.

Once finished the box should resemble **Figure 18**.

Table 14. Parts necessary for constructing series resistors into the measurement loop

Quantity	Part number	Part description
2	CN - 55	1. Pomona Shielded Box
2	CS - 564	2. Male BNC Connector
2	CS - 247	3. Female BNC Connector
1	R - 76 - 100	4. 100Ω Resistor
1	R - 76 - 10k	5. 10kΩ Resistor

Figure 18.



When Experiment 4 calls for a resistor attachment, proceed with the following:

1. Take the Model 4801 cable off the Output on the Model 5951. Attach this cable to the female BNC connector on the Pomona box.
2. Take the Pomona box and connect the male BNC connector to the Output of the Model 5951 Remote Input Coupler.
3. Make any measurements needed.
4. If the experiment requires a change of resistors, remove the Pomona box from the Model 5951 and the Model 4801 cable. Place the other Pomona box, with the different resistor, in the same place and continue the experiment.

Bibliography and References

1. Nicollian, E.H. and Brews, J.R. MOS Physics and Technology. Wiley, New York (1982).
2. Streetman, Ben G. Solid State Electronic Devices. Prentice Hall, Englewood Cliffs, New Jersey (1990).
3. Pierret, Robert F. Field Effect Devices. Vol. 4 of Modular Series on Solid State Devices. 5 vols. Addison-Wesley Publishing Co., Reading, Massachusetts (1983).
4. Keithley Instruments Inc. Instruction Manual Model 82-DOS Simultaneous C-V. Cleveland, Ohio (1988).

Acknowledgments

This series of C-V lab experiments was developed at the University of Notre Dame, Department of Electrical Engineering, by Christopher A. Martino, Stanley W. Polchlopek, Jay Millar, Robert J. Minniti, Jr., and Professor Gary H. Bernstein with assistance from the Keithley Instruments Applications Department.

KEITHLEY

Keithley Instruments, Inc. 28775 Aurora Road • Cleveland, Ohio 44139 • 440-248-0400 • Fax: 440-248-6168
1-888-KEITHLEY (534-8453) www.keithley.com

No. 1891
79410KAP