KEITHLEY

Package 82 Simultaneous CV Instruction Manual

Contains Operating Information

Publication Date: November 1988
Document Number: 5956-901-01 Rev. C

WARRANTY

Keithley Instruments, Inc. warrants this product to be free from defects in material and workmanship for a period of 1 year from date of shipment. During the warranty period, we will, at our option, either repair or replace any product that proves to be defective.

To exercise this warranty, write or call your local Keithley representative, or contact Keithley headquarters in Cleveland, Ohio. You will be given prompt assistance and return instructions. Send the instrument, transportation prepaid, to the indicated service facility. Repairs will be made and the instrument returned, transportation prepaid. Repaired products are warranted for the balance of the original warranty period, or at least 90 days.

LIMITATION OF WARRANTY

This warranty does not apply to defects resulting from unauthorized modification or misuse of any product or part. This warranty also does not apply to fuses, batteries, or damage from battery leakage.

This warranty is in lieu of all other warranties, expressed or implied, including any implied warranty of merchantability or fitness for a particular use. Keithley Instruments, Inc. shall not be liable for any indirect, special or consequential damages.

STATEMENT OF CALIBRATION

This instrument has been inspected and tested in accordance with specifications published by Keithley Instruments, Inc.

The accuracy and calibration of this instrument are traceable to the National Bureau of Standards through equipment which is calibrated at planned intervals by comparison to certified standards maintained in the Laboratories of Keithley Instruments, Inc.

KEITHLEY **Keithley Instruments Division / Keithley Instruments, Inc.**
28775 Aurora Road / Cleveland, Ohio 44139 / U. S. A. / (216) 248-0400 / Telex: 98-5469 / Fax: (216) 248-6168
WEST GERMANY: Keithley Instruments GmbH / Heiglhofstr. 5 / Munchen 70 / 089-71002-0 / Telex: 52-12160 / Telefax: 089-7100259
GREAT BRITAIN: Keithley Instruments, Ltd. / 1 Boulton Road / Reading, Berkshire RG 2 ONL / 0734-861287 / Telex: 847 047 / Telefax: 0734-863665
FRANCE: Keithley Instruments SARL / 3 Allee du 10 Rue Ambroise Croizat / B. P. 60 / 91121 Palaiseau/Cedex 1-6-0115 155 / Telex: 600 933 / Telefax: 1-6-0117726
NETHERLANDS: Keithley Instruments BV / Avelingen West 49 / 4202 MS Gorinchem / P.O. Box 559 / 4200 AN Gorinchem / 01830-35333 / Telex: 24 684 / Telfax: 01830-30821
SWITZERLAND: Keithley Instruments SA / Kriesbachstr. 4 / 8600 Dubendorf / 01-821-9444 / Telex: 828 472 / Telefax: 0222-315366
AUSTRIA Keithley Instruments GesmbH / Rosenhugelstrasse 12 / A-1120 Vienna / (0222) 84 65 48 / Telex: 131677 / Telefax: (0222) 84 35 97
ITALY: Keithley Instruments SRL / Viale S. Gimagno 4/A / 20146 Milano / 02-4120360 or 02-4156540 / Telefax: 02-4121249

Instruction Manual
Package 82
Simultaneous CV

Instruments Division
Cleveland, Ohio, U.S.A.
Document Number 5956-901-01

SPECIFICATIONS

ANALYSIS CAPABILITIES

CONSTANTS: Flatband C and V
Threshold Voltage
Bulk Doping
Effective Oxide Charge
Work Function
Doping Type
'Best Depth'

GRAPHICS:

Measured: Simultaneous C vs. Gate Voltage
High Frequency C vs. Gate Voltage
Quasistatic C vs. Gate Voltage
Conductance vs. Gate Voltage
Q/t Current vs. Gate Voltage
Quasistatic C and Q/t Current vs. Delay Time

Calculated: Interface Trap Density vs. Trap Energy
Doping vs. Depletion Depth
Depletion Depth vs. Gate Voltage
High Frequency $1/C^2$ vs. Gate Voltage
Band Bending vs. Gate Voltage
High Frequency C vs. Band Bending
Quasistatic C vs. Band Bending

VOLTAGE MEASUREMENT

ACCURACY (1 Year, 18°-28°C): ±(0.05% rdg + 50mV).

RESOLUTION: 10mV.

TEMPERATURE COEFFICIENT (0°-18° & 28°-40°C): ±(0.005% + 1mV)/°C.

VOLTAGE SOURCE

VOLTAGE	P-P NOISE[1] (0.1 Hz to 10 Hz)	RESOLUTION
≤ 20 V	150 μV	10 mV
> 20 V to 120 V	250 μV	100 mV

[1]Typically 3 mV up to 75 MHz.

MAXIMUM SWEEP SPAN, $|V_{START} - V_{STOP}|$: 40V.

MAXIMUM OUTPUT CURRENT: ±2mA (−0%, +20%).

SWEEP STEP VOLTAGE SELECTIONS: 10mV, 20mV, 50mV, 100mV.

DC OUTPUT RESISTANCE: <10Ω.

HIGH FREQUENCY CAPACITANCE*

100 kHz:

RANGE	RESOLUTION	ACCURACY (1 Year, 18°-28°C) ±(% rdg + pF)	TEMPERATURE COEFFICIENT (0°-18° & 28°-40°C) ±(% rdg)/°C	NOISE P-P
200 pF	10 fF	0.7 + 0.05	0.03	180 fF
2 nF	100 fF	0.9 + 0.5	0.08	1800 fF

1MHz:

RANGE	RESOLUTION	ACCURACY (1 Year, 18°-28°C) ±(% rdg + pF)	TEMPERATURE COEFFICIENT (0°-18° & 28°-40°C) ±(% rdg)/°C	NOISE P-P
200 pF	10 fF	0.9 + 0.05	0.03	200 fF
2 nF	100 fF	1.4 + 0.5	0.14	400 fF

SHUNT CAPACITANCE LOADING EFFECT: 0.1% of reading additional error per 100pF load with equal shunt load on input and output.

TEST VOLTAGE: 15mV rms ± 10%.

TEST FREQUENCY TOLERANCE: ±0.1%.

QUASISTATIC CAPACITANCE*

RANGE	RESOLUTION	ACCURACY (1 Year, 18°-28°C) ±(%rdg + pF)	NOISE P-P (typical)
200 pF	10 fF	1.0 + 0.1	(0.12% rdg + 0.13 pF) × (100 mV/STEP V) + 0.01 pF
2 nF	100 fF	0.8 + 0.2	(0.09% rdg + 0.13 pF) × (100 mV/STEP V) + 0.1 pF

TEMPERATURE COEFFICIENT (0°-18° & 28°-40°C): ±(0.02% rdg + 0.1 pF)/°C.

*NOTES

Specifications are based on parallel RC model and Quality Factor ≥ 20.

Assumes proper cable correction and open circuit suppression.

Quasistatic capacitance accuracy is exclusive of noise, for STEP V ≥ 0.05V and DELAY TIME ≤ 1 second. For other parameters, derate by (5mV/STEP V) × (DELAY TIME/1 second) in pF at 23°C. Double the derating for every 10°C rise in ambient temperature above 23°C.

Typical allowable non-equilibrium current plus leakage current: <20pA on 200pF range; <200pA on 2nF range during capacitance measurements.

GENERAL

READING RATES: 4½ readings per second to one reading every 400 seconds.

DATA BUFFER: 1000 points maximum.

GRAPHICAL OUTPUTS: Computer display or digital plotter supporting HPGL with IEEE-488 interface; also "screen copy" to compatible printer.

DIGITAL I/O: Consists of one output, four inputs, +5V (series limited with 33Ω), and COMMON referenced to IEEE-488 COMMON. Output will drive one TTL load. Inputs represent one TTL load.

MAXIMUM INPUT: 30V peak, dc to 60Hz sine wave.

MAXIMUM COMMON MODE VOLTAGE: 30V maximum, dc to 60Hz sine wave.

OPERATING ENVIRONMENT: 0° to 40°C, 70% non-condensing RH up to 35°C.

STORAGE ENVIRONMENT: −25° to +65°C.

WARMUP: 2 hours to rated accuracy.

SYSTEM CONFIGURATION: Models 230-1, 590, 595, and 5951 connected as shown in manual. Controller is HP Series 200 or 300 with BASIC 4.0. Requires 1 Mbyte of memory.

PACKAGE 82 COMPONENTS:

Model 230-1: Programmable Voltage Source
Model 595: Quasistatic CV Meter
Model 590: 100k/1M CV Analyzer
Model 5909: Calibration Sources
Model 5956: Package 82 CV Software and Manual
Model 5951: Remote Input Coupler—Includes Models:
4801: Low Noise BNC Cable, 1.2m (4 ft.) (5 supplied)
7007-1: Shielded IEEE-488 Cable, 1m (3.3 ft.) (2 supplied)
7007-2: Shielded IEEE-488 Cable, 2m (6.6 ft.) (1 supplied)
7051-2: RG-58C BNC to BNC Cable, 0.6m (2 ft.) (3 supplied)

Specifications subject to change without notice.

Contains information on Package 82 features, specifications, and supplied accessories.

SECTION 1
General Information

Gives information to aid in getting your simultaneous CV system up and running as quickly as possible, including hardware and software configuration.

SECTION 2
Getting Started

Covers detailed operation including system calibration, correction, and taking data.

SECTION 3
Measurement

Details analysis functions of the Package 82.

SECTION 4
Analysis

Discusses system block diagram, the remote input coupler, and quasistatic and high-frequency CV principles.

SECTION 5
Principles of Operation

Table of Contents

SECTION 1—GENERAL INFORMATION

SECTION 2—GETTING STARTED

SECTION 3—MEASUREMENT

SECTION 4—ANALYSIS

SECTION 5—PRINCIPLES OF OPERATION

SECTION 6—REPLACEABLE PARTS

APPENDICES

List of Illustrations

SECTION 2—GETTING STARTED

SECTION 3—MEASUREMENT

SECTION 4—ANALYSIS

SECTION 5—PRINCIPLES OF OPERATION

List of Tables

SECTION 1—GENERAL INFORMATION

SECTION 2—GETTING STARTED

SECTON 3—MEASUREMENT

SECTION 4—ANALYSIS

SECTION 1
General Information

1.1 INTRODUCTION

This section contains overview information for the Package 82 Simultaneous CV system and is arranged as follows:

1.2 FEATURES

The Package 82 is a computer-controlled system of instruments designed to make simultaneous quasistatic CV and high frequency (100kHz and 1MHz) CV measurements on semiconductors. The Package 82 includes a Model 590 CV Analyzer for high-frequency CV measurements, and a Model 595 Quasistatic CV Meter, along with the necessary input coupler, connecting and control cables, and cable calibration sources. A Model 230-1 Voltage Source and software for the HP 9000 Series 200 and 300 computers (or an IBM AT with an HP BASIC language processor card) running BASIC 4.0 are also included.

Key Package 82 features include:

- Remote input coupler to simplify connections to the device under test. Both the Model 595 and the Model 590 are connected to the device under test through the coupler, allowing simultaneous quasistatic and high frequency measurement of device parameters with negligible interaction between instruments.
- Supplied menu-driven software allows easy collection of C, G, V, and Q/t data with a minimum of effort. No computer programming knowledge is necessary to operate the system.
- Data can be stored on disk for later reference or analysis.
- Graphical analysis capabilities allow plotting of data on the computer display as well as hard copy graphs using an external digital plotter. Graphical analysis for such parameters as doping profile and interface trap density vs. trap energy is provided.
- Supplied external voltage source (Model 230-1) extends the DC bias capabilities to ±120V.
- Supplied calibration capacitors to allow compensation for cable effects that would otherwise reduce the accuracy of 100kHz and 1MHz measurements.
- All necessary cables are supplied for easy system hook up.

1.3 WARRANTY INFORMATION

Warranty information is located on the inside front cover of this instruction manual. Should you require warranty service, contact your Keithley representative or the factory for further information.

1.4 MANUAL ADDENDA

Any improvements or changes concerning the Package 82 or this instruction manual will be explained on a separate addendum supplied with the package. Please be sure to note these changes and incorporate them into the manual before operating or servicing the system.

Addenda concerning the Models 230-1, 590, 595, and 5909 will be packed separately with those instruments.

1.5 SAFETY SYMBOLS AND TERMS

The following safety symbols and terms may be found on one of the instruments or used in this manual:

The ⚠ symbol on an instrument indicates that you should consult the operating instructions in the associated manual.

The **WARNING** heading used in this and other manuals cautions against possible hazards that could lead to personal injury or death. Always read the associated information very carefully before performing the indicated procedure.

A **CAUTION** heading outlines dangers that could damage the instrument. Such damage may invalidate the warranty.

1.6 SPECIFICATIONS

Detailed specifications for the Package 82 system can be found at the front of this manual. Specifications for the individual instruments are located in their respective instruction manuals.

1.7 UNPACKING AND INSPECTION

1.7.1 Unpacking Procedure

Upon receiving the Package 82, carefully unpack all instruments and accessories from their respective shipping cartons, and inspect all items for any obvious physical damage. Report any such damage to the shipping agent at once. Save the original packing cartons for possible future reshipment.

1.7.2 Supplied Equipment

Table 1-1 summarizes the equipment supplied with the Package 82 system.

1.8 REPACKING FOR SHIPMENT

Should it become necessary to return any of the instruments for repair, carefully pack them in their original packing cartons (or the equivalent), and be sure to include the following information:

- Advise as to the warranty status of the equipment.
- Write ATTENTION REPAIR DEPARTMENT on the shipping label.
- Fill out and include the service form which is located at the back of this or one of the other instruction manuals.

1.9 COMPUTER CONFIGURATIONS

1.9.1 HP Series 200 and 300

The Package 82 is supplied with software intended for use with the Hewlett Packard HP 9000 Series 200 and 300 computers running under BASIC 4.0. Table 1-2 summarizes minimum requirements for the computer system. Table 1-3 summarizes necessary binary files.

1.9.2 IBM AT

The Package 82 can also be used with an IBM AT (or compatible) that is equipped with a BASIC-ROM configured HP-82321A Language Processor card. Paragraph 2.7 of this manual gives an overview of the procedure; see the HP documentation for detailed information.

1.10 SERVICE AND CALIBRATION

The Model 5951 Remote Input Coupler cannot be calibrated or repaired by the user, so it must be returned to the factory or authorized service center for repair or calibration. If the Model 5951 is to be returned, proceed as follows:

1. Complete the service form at the back of the manual and include it with the unit.
2. Carefully pack the unit in the original packing carton or its equivalent.
3. Write ATTENTION REPAIR DEPARTMENT on the shipping label.

Table 1-1. Supplied Equipment

Quantity	Description	Application
1	230-1 Voltage Source	Supply ±100V DC offset, control 5951 frequency
1	590 CV Analyzer	Measure 100kHz, 1MHz C and G
1	595 Quasistatic CV Meter	Measure C, Q/t; supply staircase bias waveform
1	5951 Remote Input Coupler	Connect 590 and 595 to DUT
1	5909 Capacitance Sources	System configuration/calibration
5	4801 Low noise BNC cables (4')	Connect 5951 to DUT and instruments
3	7051-2 BNC cables	Connect instrument control and voltage signals
2	7007-1 Shielded IEEE-488 cables (1m)	Connect instruments to bus
1	7007-2 Shielded IEEE-488 cable (2m)	Connect controller to instrument bus
1	5956 CV Software Package	Control Package 82 system.

Table 1-2. Minimum Computer Requirements

Computer	Hewlett-Packard HP9000 Series 200 or 300**
Minimum RAM	1M bytes*
Monitor	Monochrome
Disk Storage	HP82901m (5¼") or HP9122 (3½") floppy disk drive
IEEE-488 Interface	HP-IB
Programming language	BASIC 4.0

*Only 512K bytes required with ROM-based BASIC 4.0
**An IBM-AT equipped with the HP BASIC Language Processor Card can also be used. See paragraph 2.7.

Table 1-3. Necessary Binary Files

Filename	Comments
DISC or CS80*	Depends on disc drive type
HPIB*	
CRTA or CRTB*	Depends on display type
FHPIB*	
ERR**	
GRAPH**	
MAT**	
IO**	

*Driver
**Language extension

SECTION 2
Getting Started

2.1 INTRODUCTION

Section 2 contains introductory information to help you get your system up and running as quickly as possible. Section 3 contains more detailed information on using the Package 82 system.

Section 2 contains:

2.2 **Hardware Configuration:** Details system hardware configuration, cable connections, and remote input coupler mounting.

2.3 **System Power Up:** Covers the power up procedure for the system, environmental conditions, and warm up periods.

2.4 **Software Configuration:** Outlines methods for booting up the computer, making backup copies, and Package 82 software initialization.

2.5 **Software Overview:** Describes the purpose and overall configuration of the Package 82 software

2.6 **System Checkout:** Gives the procedure for checking out the system to ensure that everything is working properly.

2.2 HARDWARE CONFIGURATION

The system block diagram and connection procedure are covered in the following paragraphs.

2.2.1 System Block Diagram

An overall block diagram of the Package 82 system is shown in Figure 2-1. The function of each instrument is as follows:

Model 230-1 Voltage Source—Supplies a DC offset voltage of up to ±100V, and also controls operating frequency of the Model 5951 Remote Input Coupler.

Model 590 CV Analyzer—Supplies a 100kHz or 1MHz test signal and measures capacitance and conductance when making high-frequency CV measurements.

Model 595 CV Meter—Measures low-frequency (quasistatic) capacitance and Q/t, and also supplies the stepped bias waveform (±20V maximum) for simultaneous low- and high-frequency CV measurement sweeps.

Model 5951 Remote Input Coupler—Connects the Model 590 and 595 inputs to the device under test. The input coupler contains tuned circuits to minimize interaction between low- and high-frequency measurements.

Computer (HP 9000)—Provides the user interface to the system and controls all instruments over the IEEE-488 bus, processes data, and allows graphing of results.

Model 5909 Calibration Set—Provides capacitance reference sources for cable correcting the system to the test fixture.

2.2.2 Remote Input Coupler

The Model 5951 Remote Coupler is the link between the test fixture (which contains the wafer under test) and the measuring instruments, the Models 590 and 595. The unit not only simplifies system connections, but also contains the circuitry necessary to ensure minimal interaction between the low-frequency measurements made by the Model 595, and the high-frequency measurements made by the Model 590.

The front and rear panels of the Model 5951 are shown in Figures 2-2 and 2-3 respectively. The front panel includes input and output jacks for connections to the device under test, as well as indicators that show the selected test frequency (100kHz or 1MHz) for high-frequency measurements. The rear panel includes a binding post for chassis ground, BNC jacks for connections to the Models 590 and 595, a ribbon cable connector (which connects to the Model 230-1 digital I/O port), and a digital I/O port edge connector providing one TTL output, four TTL inputs, digital common, and +5V DC.

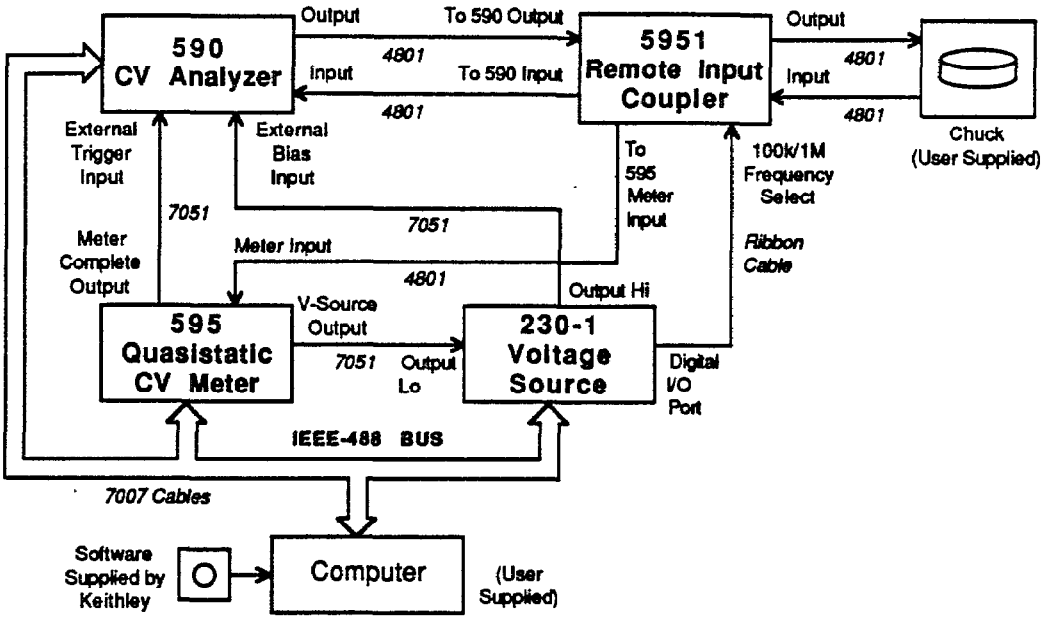
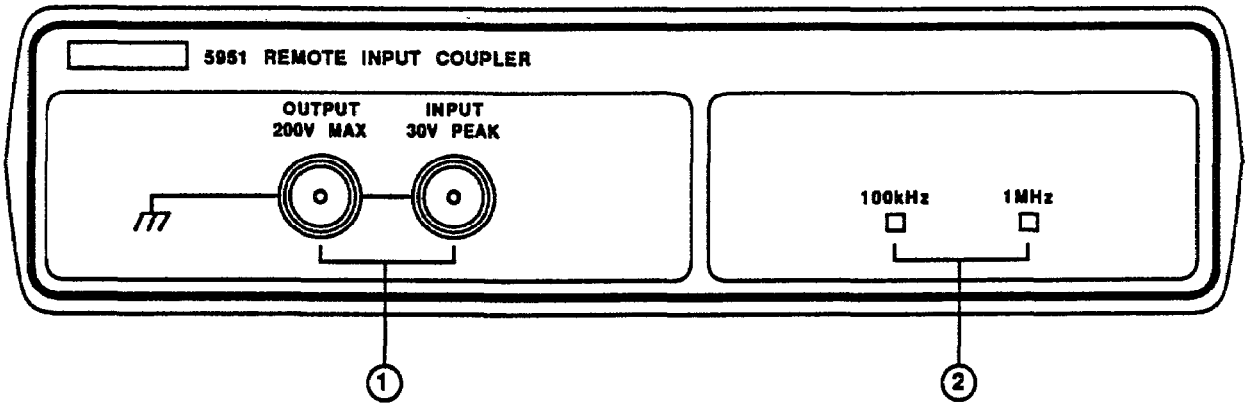


Figure 2-1. System Block Diagram

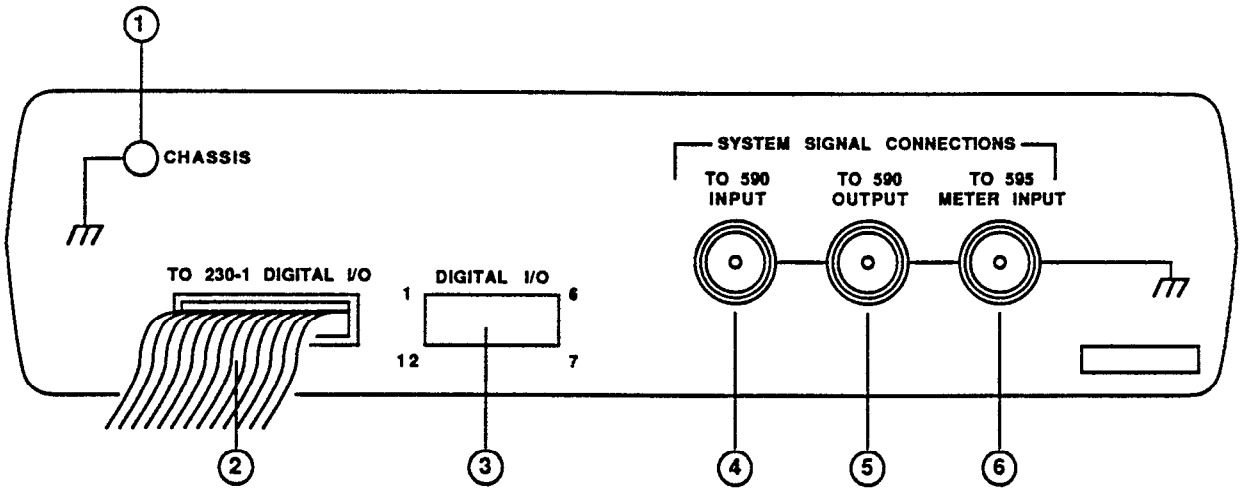


1 OUTPUT and INPUT—BNC jacks used to connect the Model 5951 to the test fixture containing the device under test.

2 Frequency indicators (100kHz and 1MHz)—Shows the selected test frequency for high-frequency measurements.

WARNING
Maximum voltage between the outer shell of the BNC jacks and earth ground is 30V RMS. Maximum OUTPUT voltage is 200V; maximum INPUT voltage is 30V peak. Exceeding these values may creat a shock hazard.

Figure 2-2. Model 5951 Front Panel



1 CHASSIS binding post—Provides a convenient connection to chassis ground of the Model 5951.

WARNING
Connect CHASSIS to earth ground to avoid a possible shock hazard. Use #16 AWG or larger wire.

2 Ribbon cable—Connects to the Model 230-1 digital I/O port for frequency switching of the remote coupler.

3 DIGITAL I/O—Passes through the Model 230-1 digital I/O port signals for control and sensing of other components (for example, light control and door closed status).

4 TO 590 INPUT—Connects to the Model 590 INPUT jack on the front panel of the instrument.

5 TO 590 OUTPUT—Connects to the Model 590 OUTPUT jack on the front panel.

6 TO 595 METER INPUT—Connects to the Model 595 METER INPUT jack on the rear of the instrument.

WARNING
Maximum voltage between the outer shell of the BNC jacks and earth ground is 30V RMS.

Figure 2-3. Model 5951 Rear Panel

Table 2-1. Supplied Cables

Qty	Model	Description	Application
5	4801	4' BNC Low Noise	590, 595, 5951
3	7051-2	2' BNC (RG-58)	230-1, 590, 595
2	7007-1	1m shielded IEEE-488	IEEE-488 instrument bus
1	7007-2	2m shielded IEEE-488	Computer to instruments
1	*	Ribbon cable	5951 to 230-1

*Supplied with Model 5951

2.2.3 System Connections

Supplied Cables

Table 2-1 summarizes the cables supplied with the Package 82 system along with the application for each cable. Note that low-noise cables are provided for making connections between the chuck and the CV measurement instruments. The Model 4801 cables are each four feet long. Be careful not to use the Model 7051 BNC cables in place of the low-noise cables (Model 4801), as doing so will have detrimental effects on your measurements.

Connection Procedure

Use Figures 2-4 and 2-5 as a guide and connect the equipment together as follows. Note that the stacked arrangement shown in the figures is recommended, but other setups can be used, if desired.

NOTE

All equipment should be turned off when making connections.

1. Connect a Model 4801 cable between the Model 590 INPUT jack and the TO 590 INPUT jack of the Model 5951 Remote Input Coupler. Connect a second Model 4801 between the Model 590 OUTPUT jack and the TO 590 OUT jack of the Model 5951.
2. Connect the Model 5951 INPUT and OUTPUT jacks to the chuck test fixture using Model 4801 cables.

NOTE

OUTPUT should be connected to the substrate contact, and INPUT should be connected to the gate metallization contact.

3. Connect the Model 5951 TO 595 METER INPUT jack to the Model 595 METER INPUT jack using a Model 4801 cable.
4. Connect the ribbon cable to the Model 5951, and then connect the opposite end of the cable to the digital I/O port of the Model 230-1. Both connectors are keyed so that they can be installed only in one direction.
5. Using a Model 7051 cable, connect the Model 595 METER COMPLETE OUTPUT to the EXTERNAL TRIGGER INPUT jack of the Model 590.
6. Using a second Model 7051 BNC cable, connect the Model 595 VOLTAGE SOURCE OUTPUT to the OUTPUT LO of the Model 230-1 Voltage Source. In a similar manner, use a Model 7051 BNC cable to connect the Model 230-1 OUTPUT HI to the EXTERNAL BIAS INPUT of the Model 590 CV Analyzer.
7. Connect the Model 5951 chassis ground post to earth ground using heavy copper wire.

WARNING

The Model 5951 must be connected to earth ground using #16 AWG or larger wire.

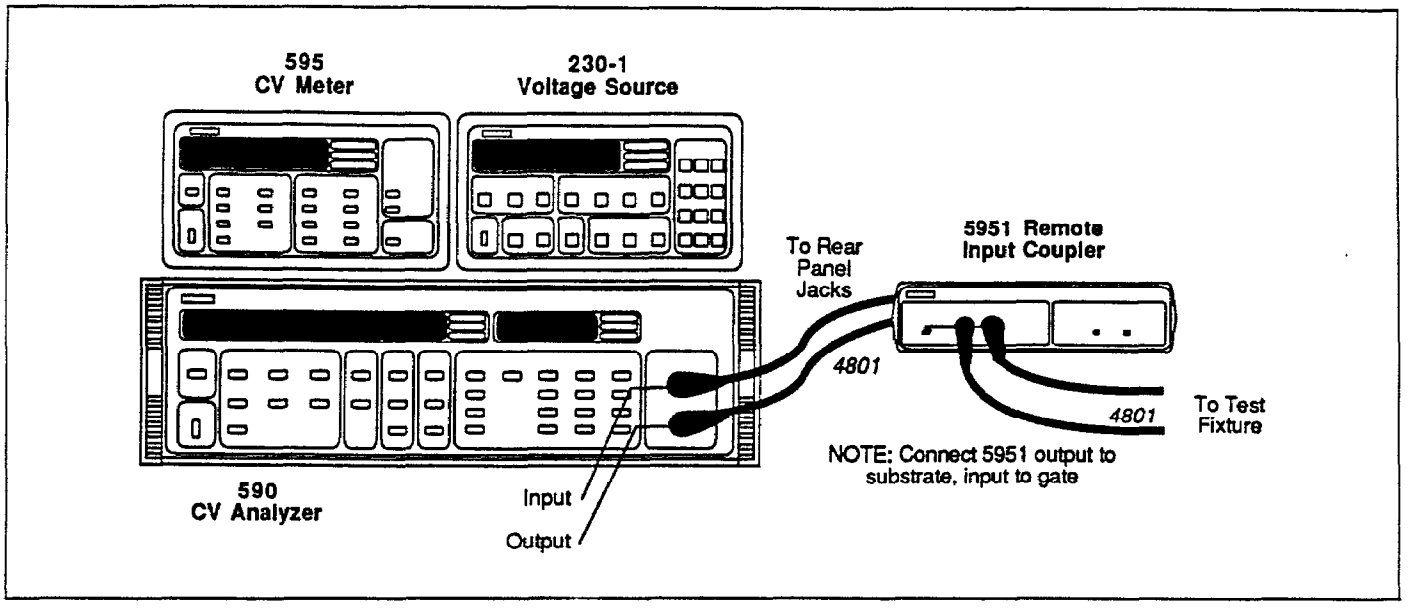


Figure 2-4. System Front Panel Connections

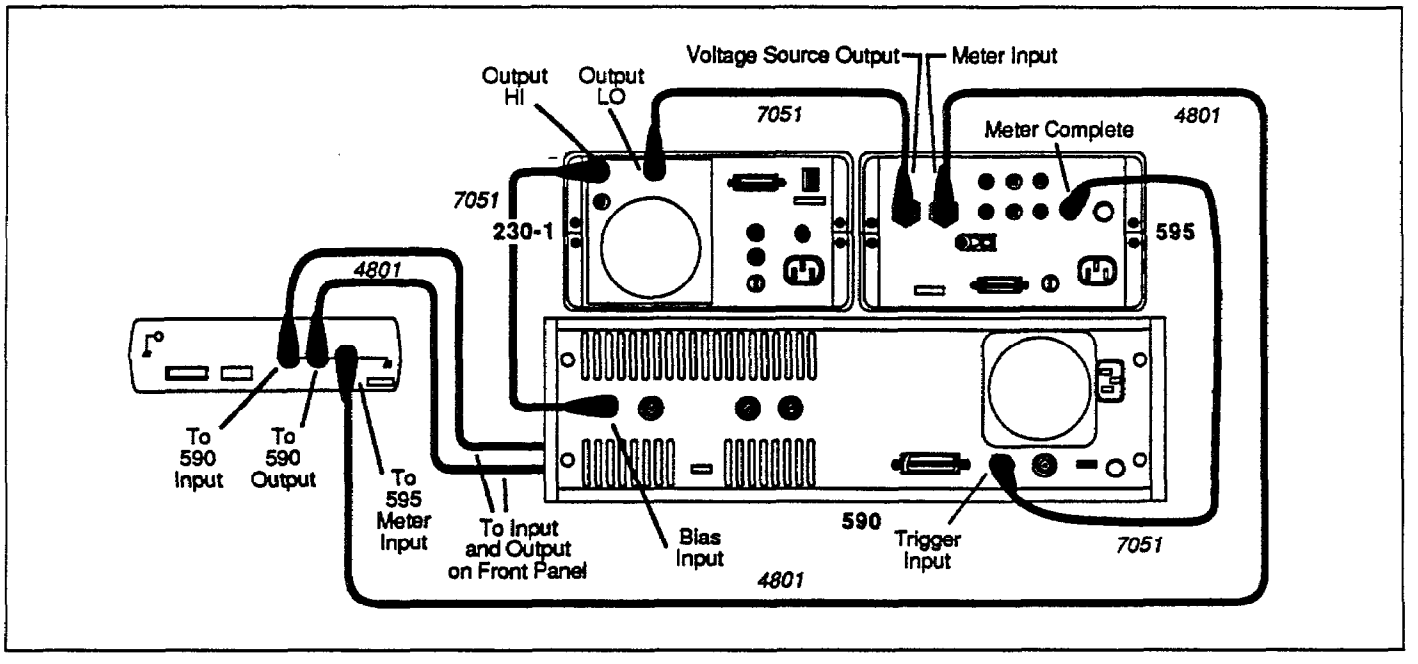


Figure 2-5. System Rear Panel Connections

2.2.4 IEEE-488 Bus Connections

In order to use the system, the instruments must be connected to one another and the computer using the supplied IEEE-488 cables. Typically the shorter cables will be used to connect the instruments together, while the longer cable connects the instrument group to the computer. Figure 2-6 shows a typical arrangement for IEEE-488 bus connections.

2.2.5 Remote Coupler Mounting

In many cases, the wafer prober will be located inside a faraday cage to minimize noise. In these situations, the remote coupler itself can also be placed inside the cage for convenience and to minimize cable lengths, assuming, of course, there is sufficient room.

The coupler can be permanently mounted to the sides or top of the faraday cage by removing the rubber feet and using the threaded holes in the bottom case for mounting. Appropriate mating holes can be drilled in the faraday cage, and the coupler should be secured to the cage with #6-32 screws of sufficient length.

CAUTION

Be sure that the mounting screws do not extend more than ¼" inside the Model 5951 case, or they may contact the circuit board inside.

Figure 2-7 shows a typical installation for coupler mounting, including suggested cable routing. Note that the Model 5951 chassis should be grounded to the faraday cage by connecting a grounding strap or wire between the cage and the coupler chassis ground binding post.

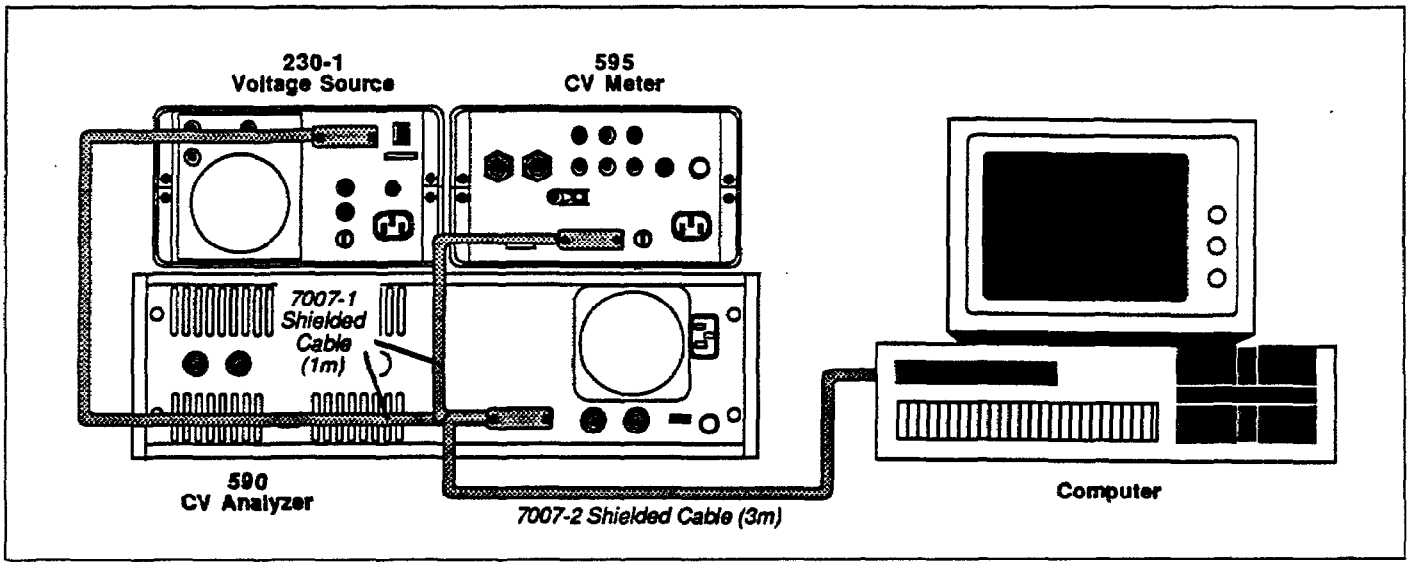


Figure 2-6. System IEEE-488 Connections

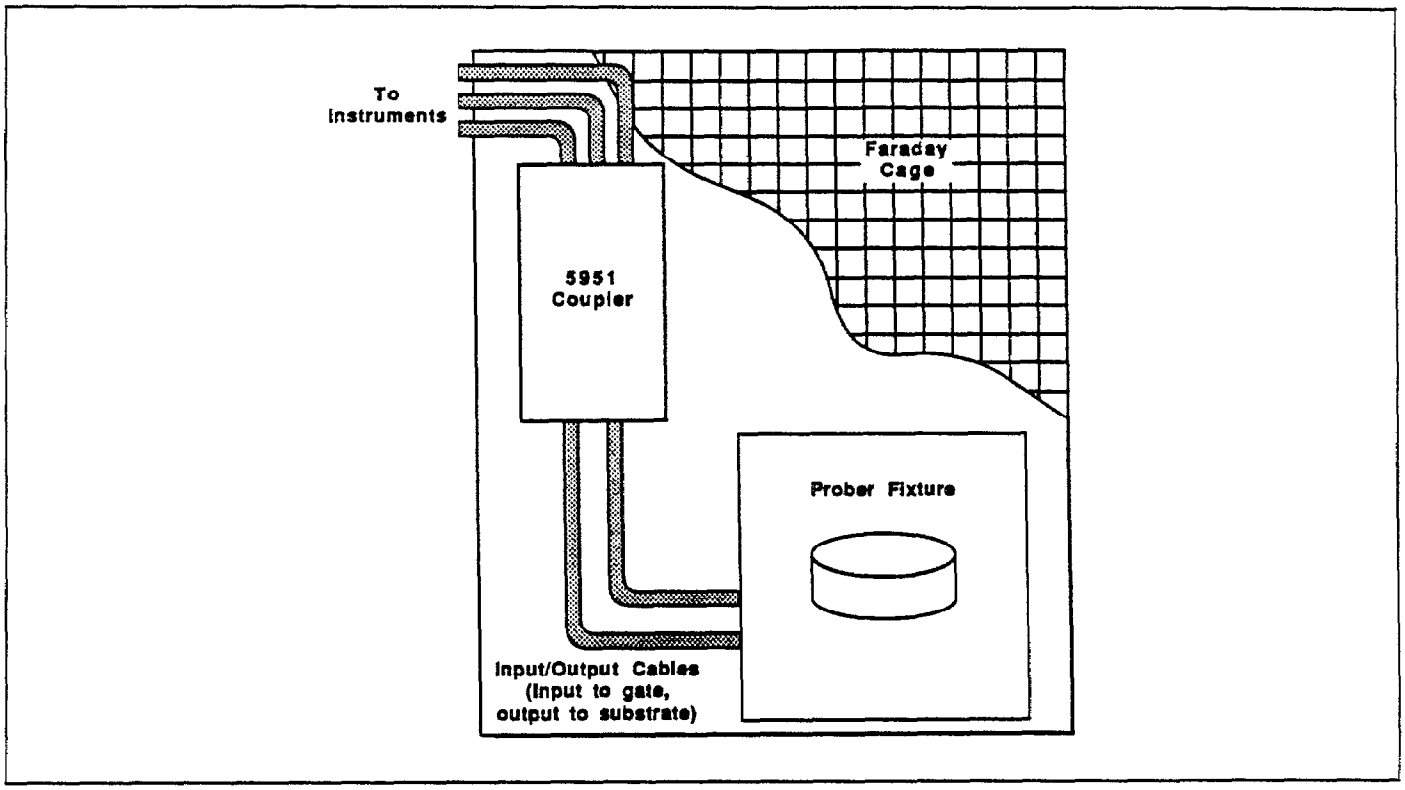


Figure 2-7. Remote Coupler Mounting

2.3 SYSTEM POWER UP

Line voltage selection, power connections, environmental conditions, and instrument warm-up periods are covered in the following paragraphs.

2.3.1 Instrument Power Requirements

The Models 230-1, 590, and 595 are designed to operate from 105-125V or 210-250V, 50 or 60Hz AC power sources (special transformers can be factory installed for 90-110V and 195-235V AC voltage ranges). The factory setting for each instrument is marked on the rear panel of that particular instrument. The operating voltage for each instrument is either internally or externally selectable; see the appropriate instruction manual for details.

CAUTION

Do not attempt to operate an instrument on a supply voltage outside the allowed range, or instrument damage may occur.

2.3.2 Power Connections

Each instrument should be connected to a grounded AC outlet using the supplied AC power cord or the equivalent.

WARNING

Each instrument must be connected to a grounded outlet using the supplied power cord in order to ensure continued protection from possible electric shock. Failure to use a grounded outlet and a 3-wire power cord may result in personal injury or death because of electric shock.

2.3.3 Environmental Conditions

For maximum measurement accuracy, all instruments and the remote coupler must be operated at an ambient temperature between 0 and 40°C at a relative humidity less than 70%, and within ±5°C of the cable correction temperature.

2.3.4 Warm Up Period

The system can be used immediately when all instruments are first turned on; however, to achieve rated system accuracy, all instruments should be turned on and allowed to warm up for at least two hours before use.

2.3.5 Power Up Procedure

Follow the general procedure below to power up the Package 82 system.

1. Connect the instruments together as outlined in paragraph 2.2.3.
2. Connect the instruments to the IEEE-488 bus of the host computer following the procedure given in paragraph 2.2.4.
3. Turn on the computer and boot up its operating system in the usual manner. Refer to the computer documentation for complete details for your particular system.
4. Turn on each instrument by pressing in on its front panel power switch. Verify that each instrument goes through its normal power up routine, as described below.

Model 230-1

1. The instrument first turns on all LEDs and segments.
2. The software revision level is then displayed as in this example:

   B13

3. The unit then displays the primary address:

   IE 13

   Verify the primary address is 13; set it to that value if not.

4. The unit begins normal display.

Model 590

1. The Model 590 first displays the software revision level as in this example:

   590 REV D13

2. The instrument then displays the programmed primary address:

   IEEE ADDRESS 15

   Verify the address is 15; program it for that value if not.
3. Finally, the unit begins displaying normal readings.

Model 595

1. The instrument first displays the ROM self-test message:

   r.o.

2. The unit then displays normal readings.
3. Press MENU and verify the primary address is 28; set it to that value if not.

2.3.6 Line Frequency

The Models 230-1 and 590 can be operated from either 50 or 60Hz power sources with no further adjustments. However, for the Model 595 to meet its stated noise specifications, the unit must be programmed for the line frequency being used. To set or check the Model 595 line frequency, proceed as follows:

1. Turn off the Model 595 if it is presently turned on.
2. Press and hold the MENU button and then turn on the power. Release the MENU button after the display blanks on power up.
3. Press the MENU button and note that the frequency selection prompt is displayed:

   Fr = 50

   or,

   Fr = 60

4. Use one of the ADJUST keys to toggle the unit to the desired frequency.
5. Press SHIFT EXIT to return to normal operation. Note that the frequency selection prompt will remain in the menu until power is removed.

2.4 SOFTWARE CONFIGURATION

The following paragraphs discuss booting up the computer, making backup copies of the Package 82 software, and loading and initializing the software.

2.4.1 Computer Boot Up

Before you can use the Package 82 software, the computer must be booted up with the proper operating system software. See paragraph 1.9 for further information on computer requirements.

Turn on the computer and boot up BASIC 4.0 (if the computer has ROM-based BASIC, no initialization is necessary).

2.4.2 Software Backup

Before using the software, it is strongly recommended that you make a working copy of the software supplied with the Package 82. Since the software is not copy protected, you can use the standard copy commands to duplicate each diskette. After duplication, put the master diskette away in a safe place and use only the working copy.

Use the COPY command to copy the software diskette. A typical example is:

```
COPY ":HP9895,700,0" TO ":HP9895,700,1"
```

Here, HP9895 represents the type of disk drive, 700 is the primary address, and 0 and 1 are the disk drive numbers. Note that the working diskette should be formatted with the INITIALIZE command before attempting copying.

2.4.3 Software Initialization

Software initialization is simply a matter of loading and running a program as you would any other BASIC program, as outlined below.

1. Boot up or enter BASIC 4.0 in the usual manner.
2. If necessary, assign a mass storage specifier to the drive you intend to use. A typical example is:

```
MASS STORAGE IS ":,700,0"
```

3. Place the Package 82 software working disk in the default drive.
4. Type in LOAD"PKG82CV" and press the EXEC key.
5. After the program loads, press the RUN key, or type in RUN and then press the EXEC key. The main menu shown in Figure 2-8 should appear on the computer display.

2.4.4 Software Files

Package 82 software files that are included with the distribution diskette are summarized in Table 2-2. Note that "pkg82cal" is created when cable correction is performed the first time.

2.5 SOFTWARE OVERVIEW

The main sections of the Package 82 software are discussed in the following paragraphs. These decriptions follow the order of the main menu shown in Figure 2-8. For detailed information on using the software to make measurements and analyze data, refer to Sections 3 and 4.

2.5.1 System Reset

By selecting option 1 on the main menu, you can easily reset the instruments and the software to default conditions. DCL (Device Clear) and IFC (Interface Clear) commands are sent over the bus to return the instruments to their power-on states and remove any talkers or listeners from the bus.

2.5.2 System Characterization

Option 2 on the main menu allows you to perform a "probes up" characterization of the complete system from the measuring instruments, through the connecting cables and remote coupler, down to the prober level. Characterization is necessary to null out (C_Q, C_H, or G), or remedy leakage currents, resistances, and stray capacitance present in the system that could affect measurement accuracy; the procedure also allows you to verify connection problems.

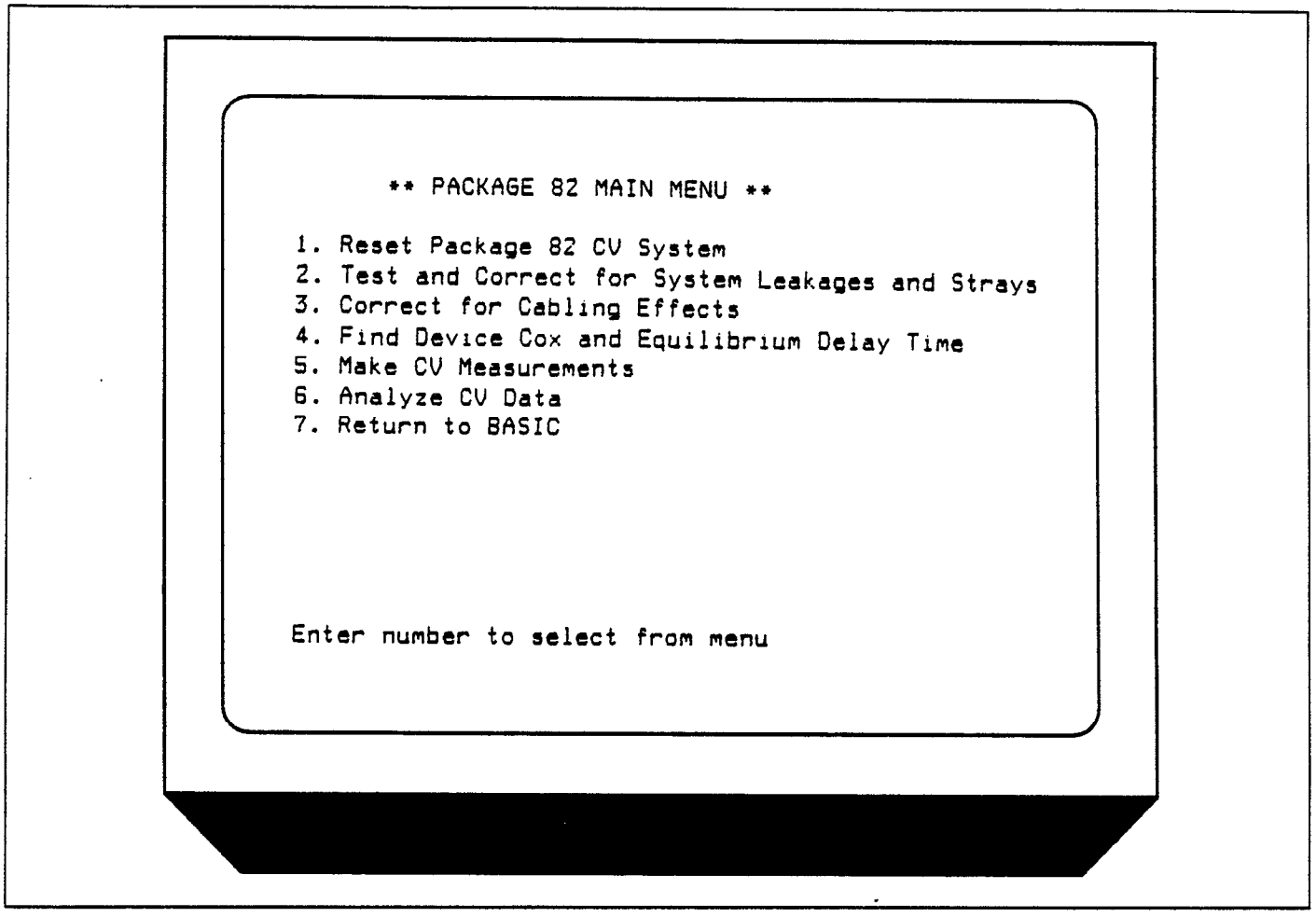


Figure 2-8. Main Menu

There are two important aspects to system characterization:

1. Quasistatic capacitance (C_Q), high-frequency capacitance (C_H), conductance (G), and Q/t (current) are measured at a specified bias voltage to determine system contribution of these factors. C_Q, C_H, and G can be suppressed in order to maximize accuracy. If abnormally large error terms are noted, the system should be checked for poor connections or other factors that could lead to large errors.
2. Q/t vs. V sweeps can be performed to determine the presence of leakage resistance and external leakage current sources. C vs. V sweeps can be done to test for the presence of voltage dependent capacitance in the system.

System checkout should be performed whenever the configuration, step V, or delay time is changed. Probes-up suppression should precede every measurement to achieve rated accuracy.

2.5.3 Cable Correction

Cable correction can be performed by selecting option 3 on the main menu. Cable correction is necessary to compensate for transmission line effects of the connecting cables and is essential for maintaining accuracy of high-frequency CV measurements. In order to cable correct the system, you must connect the Model 5909 Calibration Sources to the system. Refer to paragraph 3.5 Correcting for Cabling Effects.

Included in the cable correction procedure is a gain correction of the Model 595 CV Meter. Cable correction and gain correction parameters are automatically stored on disk during cable correction and are restored when the software is run initialized so that correction need not be performed each time the system is used. Note, however, that correction should be performed whenever the ambient temperature changes by more than 5°C, or if the system configuration is changed.

NOTE
The diskette for storing cable correction parameters must be in the default drive when correction is performed.

2.5.4 C_{ox} and Delay Time Determination

Option 4 allows you to determine optimum parameters for measuring the device under test. The key areas of this characterization process are:

1. A CV sweep of the device is used to find accumulation and inversion voltages.
2. The device is biased in the accumulation region in order to determine C_{ox}.
3. The device is biased in inversion to determine Model 595 step time. A test for equilibrium can be performed by monitoring the decay time of Q/t to the system leakage level following a step in DC bias voltage. The user can also control a light on the device to help achieve equilibrium.
4. A sweep of C and Q/t vs time delay is performed to determine optimum delay time.

2.5.5 Device Measurement

Option 5 on the main menu allows you to perform a simultaneous CV sweep on the device under test. As parameters are measured, the data are stored within an array for plotting or additional analysis, as required.

The two types of sweeps that can be performed include:

1. Accumulation to inversion: Initially, the device is biased in accumulation, and the bias voltage is held static until Q/t reaches the system leakage level. The sweep is then performed and the data are stored in the array.
2. Inversion to accumulation: In this case, the device is first biased in inversion, and the sweep is paused until equilibrium is reached (when Q/t equals the system leakage level). A submenu option allows you to control a light within the test fixture (using the Model 5951 digital I/O port) as an aid in attaining the equilibrium point. The sweep is then completed and the data are stored in an array for further analysis.

2.5.6 Data Analysis and Plotting

Option 6 on the main menu provides a window to a number of analysis and graphing tools. Key options here include printing out parameters, graphing array data on the CRT or plotter, graphical analysis, and loading or storing array data on disk. Note that this option can also be directly selected from menus providing sweep measurements without having to go through the main menu.

2.6 SYSTEM CHECKOUT

Use the basic procedure below to check out the Package 82 to determine if the system is operational. The procedure requires the use of the Model 5909 Calibration Sources, which are supplied with the package. Note that this procedure is not intended as an accuracy check, but is included to show that all instruments and the system are functioning normally.

2.6.1 Checkout Procedure

1. Connect the system together, as discussed in paragraph 2.2.
2. Power up the system using the procedure given in paragraph 2.3.
3. Boot up the computer and load the Package 82 software, as covered in paragraph 2.4.
4. Select option 2 on the main menu, and then option 2 on the subsequent menu. Connect the 1.8nF capacitor and verify that C_Q is within 1% of the 1kHz capacitor value, and that Q/t is <1pA. Correct any cabling problems before proceeding.
5. Select the cable correction option on the main menu.
6. Follow the prompts and connect the Model 5909 Calibration Sources to the Model 5951 INPUT and OUTPUT cables using the BNC adapters supplied with the Model 5909.
7. After correction, return to main menu selection 2, then select option 2 on the submenu. Connect the 1.8nF capacitor; verify that C_Q is within 1% of the 1kHz capacitance, and that C_R is within 1% of the 100kHz or 1MHz value (depending on the selected frequency).
8. Select option 3 on the leakage and strays menu.
9. Turn on the sweep and observe the Model 590 voltage display. Verify that the bias voltage readings step through the range of −2V to +2V in 10mV increments.

2.6.2 System Troubleshooting

Troubleshoot any system problems using the basic procedure shown in Table 2-3. For information on troubleshooting individual instruments, refer to the respective instruction manual(s).

Table 2-2. Diskette Files

Filename	File Type	Description
PKG82CV	Program	Main Package 82 program
M590CV*	Program	Model 590 program
M595CV*	Program	Model 595 program
pkg82cal**	Data	Cable correction constants

*See Appendix for details on these programs.

**This file is created/updated when cable correction is performed.

Table 2-3. System Troubleshooting Summary

Symptom	Possible Cause(s)
No instrument responds over bus.	Units not connected to controller, controller defective.*
One instrument fails to respond.	Unit not connected to bus, improper primary address, unit defective.
Improper low-frequency measurements.	595 not connected properly, 595 defective.
Improper high-frequency measurements.	590 not connected properly, ribbon cable not connected, 590 defective.
5951 does not change frequency.	Ribbon cable not connected, 5951 or 230-1 defective, loose ribbon cable connection.
No DC bias applied to device.	595 or 230-1 not connected properly, 595 or 230-1 defective.
Excessive leakage current.	Wrong cables used, dirty jacks, test fixture contamination.
Erratic readings.	EMI interference, poor connections.
590 readings not triggered.	595 to 590 trigger cable not connected.
Probes up Q/t vs V improper.	External leakage current present.
Probes up C vs V improper.	External voltage-dependent capacitance present.
Cable correction impossible.	Wrong cables used, 590 defective.
Reading dynamic range insufficient.	Connecting cables too long, excessive fixture capacitance.

*If using an IBM AT with the Language Processor Card, you can check to see if the card is functioning by using the procedure covered in paragraph 2.7.6.

2.7 USING THE PACKAGE 82 WITH THE IBM AT

The Package 82 can be used with IBM AT computers (and some compatibles such as the HP Vectra) that are equipped with the HP 82321A Language Processor Card. The HP BASIC 5.0 ROM must be installed on the processor card in order to support the Package 82 software. Note that an EGA monitor is recommended (a monochrome monitor will work, but displayed graphs will be somewhat small).

The following paragraphs give a brief overview of hardware and software installation, configuration file, and methods to change the print path to support a parallel or serial printer. Refer to the documentation supplied with the processor card, BASIC ROM, and programming language for detailed information.

2.7.1 Installation

Follow the overall procedure below to install the hardware and software.

1. Install the HP BASIC ROM on the processor card, as discussed in the HP BASIC ROM Installation Instructions. Be sure to place the ROM jumper in the ROM IN position.
2. Install the processor card in the IBM AT computer, as discussed in the Language Processor Instructions.
3. Connect the IEEE-488 bus of the Package 82 instruments to the HP-IB connector of the processor card. See paragraph 2.2.4 of this instruction manual for more information on IEEE-488 bus connections.
4. Boot up the IBM AT computer with MS-DOS.
5. Install the BASIC Language software, as discussed in the HP BASIC ROM Installation instructions.

2.7.2 Software Backup

Before using the Package 82 software, it is strongly recommended that you make working copies of the supplied disks, and use only the working disks on a day-to-day basis. To do so, perform an LIF-to-HPW copy using the HPWUTIL utility supplied with the HP BASIC package. Note that disks copied to the HPW format can only be used on MS-DOS drives along with the HP BASIC system; these copies cannot be used on HP Series 200 or 300 drives.

2.7.3 Configuration File Modification

The configuration file, HPW.CON, must be modified to redefine the display model type to combined alpha/graphics for use with the Package 82. To do so, run the CONF.EXE utility from MS-DOS, and change the machine type to "9816 combined". Save the new configuration before exiting the CONF.EXE utility. Remember that the HPW.CON file must be in the directory of the disk you use to BOOT the system.

2.7.4 Booting the System

Use the appropriate procedure below to boot BASIC and load the Package 82 software. These procedures assume that you have followed the software installation instructions given in the HP BASIC ROM Installation Instructions.

Hard Disk System Boot-up

The procedure below assumes that drive C is your hard disk, and that you have created a directory called HPW as part of the installation procedure. All pertinent HP files must exist under the HPW directory.

1. Type the following:

   C: <Enter>
   CD \HPW <Enter>
2. If you have not already done do, copy the Package 82 software into the HPW directory by using the HPWUTIL utility program supplied with HP BASIC. Select the LIF to HPW option for copying for master disks, or use HPW to HPW copy for working disks copied with HPUTIL utility.
3. After the disk has been copied, boot the system by typing the following:

   BOOT <Enter>
4. After the boot-up sequence has finished, type the following to enter BASIC:

   HPBASIC <Enter>
5. Load the Package 82 software as follows:

   LOAD "PKG82CV" <Enter>
   (Or use "M590CV" or "M595CV" filenames for those programs).

6. RUN the program in the usual manner. Refer to the remainder of Section 2, as well as Sections 3 and 4 for detailed operation information.

Flexible Disk System Boot-up

1. Place the HP BASIC working disk into the default drive, and type the following:

   BOOT <Enter>
2. After the boot-up procedure, enter the following:

   HPBASIC <Enter>
3. Place the Package 82 working disk in the default drive, and type the following:

   LOAD "PKG82CV" <Enter>

   (Or use "M590CV" or "M595CV" filenames for those programs.)
4. RUN the program in the usual manner. See Sections 2, 3, and 4 for detailed operation information.

2.7.5 Modifying the Print Path

As supplied, the Package 82 software supports a printer connected to the HP-IB bus with a primary address of 1. The program must be modified to support printers connected to the parallel or serial ports of the IBM AT, as outlined below. Note that such printers must emulate HP Think Jet bit-mapped graphics in order to properly display graphs generated by the Package 82.

1. Boot up HP BASIC and the "PKG82CV" (or "M590CV" or "M595CV") programs, as described above.
2. Type the following in order to locate the Printpath variable in the program:

   FIND "Printpath" <Enter>
3. When the computer displays the line in which Printpath is defined, modify the variable as follows (for the parallel port, LPT1):

   Printpath = 26

   For the serial port (COM1), modify the Printpath as follows:

   Printpath = 9

   (Note: It may also be necessary to modify the configuration file for proper serial port operation. See the HP BASIC Language Programmer's Reference Guide.)
4. Save the modified program under a convenient name. Use the modified program in order to support the parallel or serial printers.

2.7.6 Operational Check

After software and hardware installation, the procedure below can be used to determine if the language processor card is properly communicating with the instruments.

1. Connect the instruments to the IEEE-488 connector on the back of the IBM AT computer.
2. Turn on the computer, boot MS-DOS, then boot up HP BASIC, as described in paragraph 2.7.4.
3. Turn on the instruments; make sure they go through their normal power-up cycles, and that the primary addresses of the instruments are set to their default values (230-1, 13; 590, 15; 595, 28). If not, set or program the primary address(es) to the correct value(s).
4. From the HP BASIC direct mode, type in the following command, and verify that the Model 230-1 displays 10V:

   OUTPUT 713 ; "V10X" <Enter>
5. Type in the following, and note that the Model 590 goes into the autorange mode:

   OUTPUT 715 ; "R0X" <Enter>
6. Type in the following, and verify that the Model 595 changes to the current function:

   OUTPUT 728 ; "F1X" <Enter>

SECTION 3
Measurement

3.1 INTRODUCTION

This section gives detailed information on using the Package 82 Software to acquire CV data and is organized as follows:

3.2 **Measurement Sequence:** Outlines the basic measurement sequence that should be followed to ensure accurate measurements and analysis.

3.3 **System Reset:** Describes how to reset the instruments in the system.

3.4 **Testing and Correcting for System Leakages and Strays:** Describes the procedure to test the complete system for the presence of unwanted characteristics such as leakage resistance, current, and capacitance.

3.5 **Correcting for Cabling Effects:** Details cable correction that must be used in order to ensure accuracy of high-frequency CV measurements.

3.6 **Finding Device Oxide Capacitance and Equilibrium Delay Time:** Covers the procedures necessary to determine C_{ox} and optimum delay time to attain device equilibrium.

3.7 **Making CV Measurements:** Describes in detail the procedures necessary to measure the device under test and store the resulting data in arrays.

3.8 **Light Connections:** Discusses connection of a light to the system as an aid in attaining device equilibrium.

3.9 **Measurement Considerations:** Outlines numerous factors that should be taken into account in order to maximize measurement accuracy and minimize errors in analysis.

3.2 MEASUREMENT SEQUENCE

The measurements must be carried out in the proper sequence in order to ensure that the system is optimized and error terms are minimized. The basic sequence is outlined below; Figure 3-1 is a flowchart of the sequence.

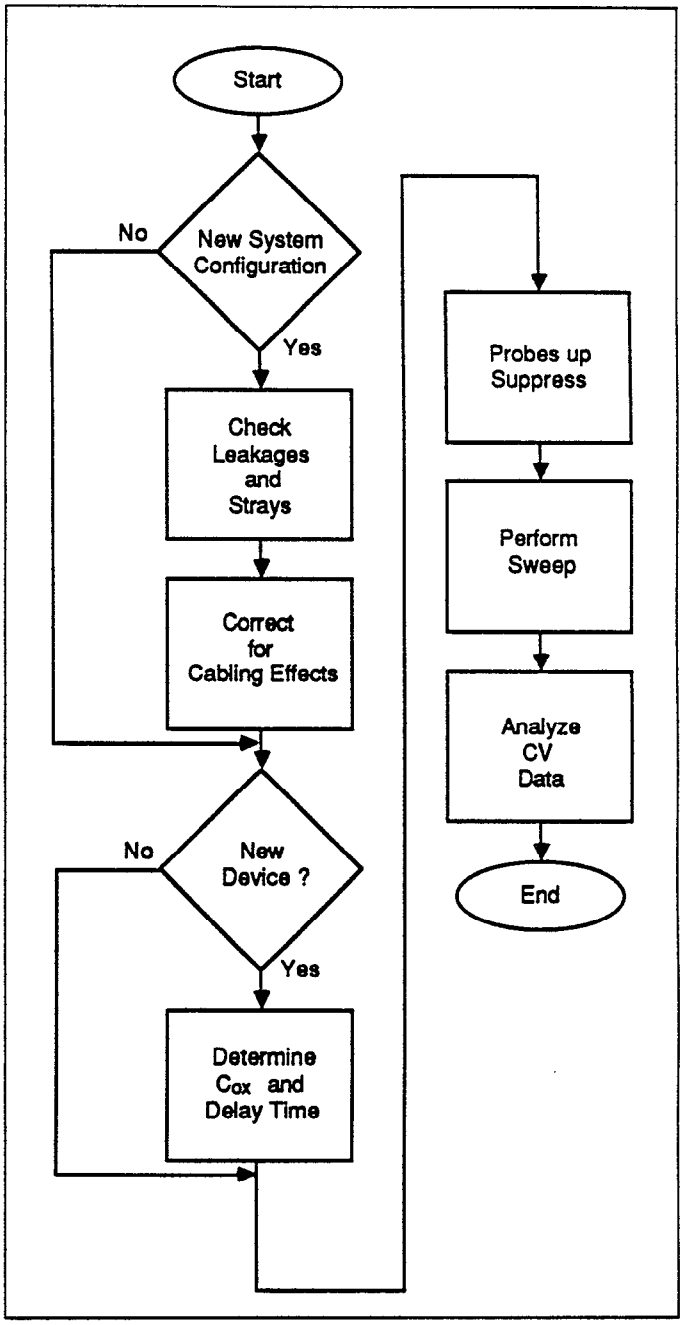


Figure 3-1. Measurement Sequence

Step 1: Test and Correct for System Leakage and Strays

Initially, you should test your system to determine if any problems such as excess leakage current or unwanted capacitance are present. You should correct any problems before continuing. Note that the system need be tested only when you change some aspect of its configuration (such as connecting cables or test fixture).

Suppression, which is also available under this menu option, should be performed before each measurement for optimum accuracy. Note that suppression can also be performed from a measurement menu by pressing "Z".

Step 2: Correct for Cabling Effects

Cable correction is necessary to compensate for transmission line effects through the connecting cables and remote input coupler. Failure to perform cable correction will result in substantially reduced accuracy of high-frequency CV measurements. In order to perform correction, it will be necessary for you to connect the Model 5909 calibration capacitors. Cable correction need be performed only if the system configuration is changed in some manner, or if the ambient temperature changes by more than 5°C.

Step 3: Determine Oxide Capacitance and Equilibrium Delay Time

The device must be tested to determine optimum delay time to maintain equilibrium as well as to determine C_{ox}. C_{ox} is determined with the device biased in accumulation. The device can then be biased in inversion to determine optimum delay time for equilibrium by plotting C and Q/t versus delay time. Note that these parameters must be determined for each device.

Step 4: Make CV Measurements

Now that all the "housekeeping", so to speak, is out of the way, a sweep can be performed to determine how such device parameters as capacitance change with applied DC bias voltage. First, of course, it will be necessary for you to select such parameters as range, frequency, and bias voltage values. As the sweep is performed, measured values are stored in arrays for later retrieval and analysis.

Step 5: Analyze CV Data

Once a sweep has been performed and the results are stored safely in computer arrays, you can apply any one of a number of different analysis techniques to the data. Raw data plotting (hard copy) or graphing (CRT) of such parameters as low and high frequency capacitance vs. V can be performed. Analysis features including doping profile, flatband calculations, and interface trap density are also provided. See Section 4 for analysis.

3.3 SYSTEM RESET

Option 1 on the main menu (Figure 3-2) allows you to reset your Package 82 System and return the instruments to their default conditions. When this option is executed, the IEEE-488 IFC (Interface Clear) and SDC (Selective Device Clear) commands are sent over the bus, and you will then be returned to the main menu after a two-second pause. During this period, the computer will display the following message:

Outputing IFC and SDC to reset system.

The IFC command removes any talkers and listeners from the bus, and the SDC command returns instruments to their default conditions. The Models 230-1 and 595 will always return the the same default state, but the default conditions for the Model 590 are determined by SAVE 0. See the appropriate instruction manuals for details. Note that the instruments are automatically reset when the program is first run, and that only the Models 230-1, 590, and 595 will be affected by the SDC Command; the disk drive, printer, or other peripherals will not be affected.

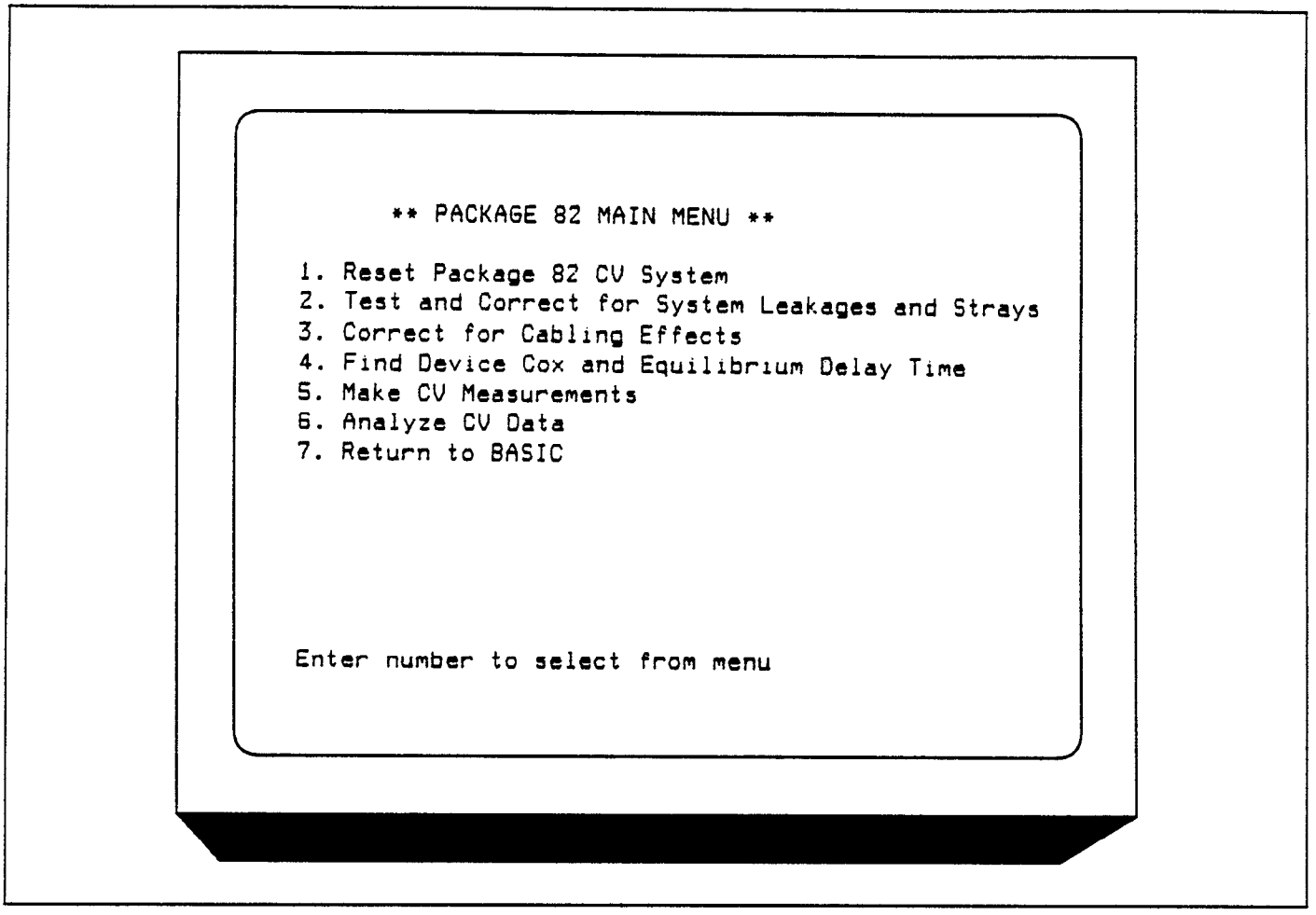


Figure 3-2. Package 82 Main Menu

3.4 TESTING AND CORRECTING FOR SYSTEM LEAKAGES AND STRAYS

The system should be tested with the probes up to determine if any sources of large errors such as defective cables are present. The following paragraphs give an overview of the process, discuss menus, and detail the procedure for testing your particular system.

Suppression should be performed prior to each measurement for optimum accuracy.

3.4.1 Test and Correction Menu

To test your system, select main menu option 2, Test and Correct for System Leakages and Strays.

Figure 3-3 shows the overall test and correction menu for the Package 82 software. Through this menu, you can select measurement parameters, monitor leakage levels, perform a probes-up sweep, analyze the results, and suppress offsets. These aspects are covered in the following paragraphs.

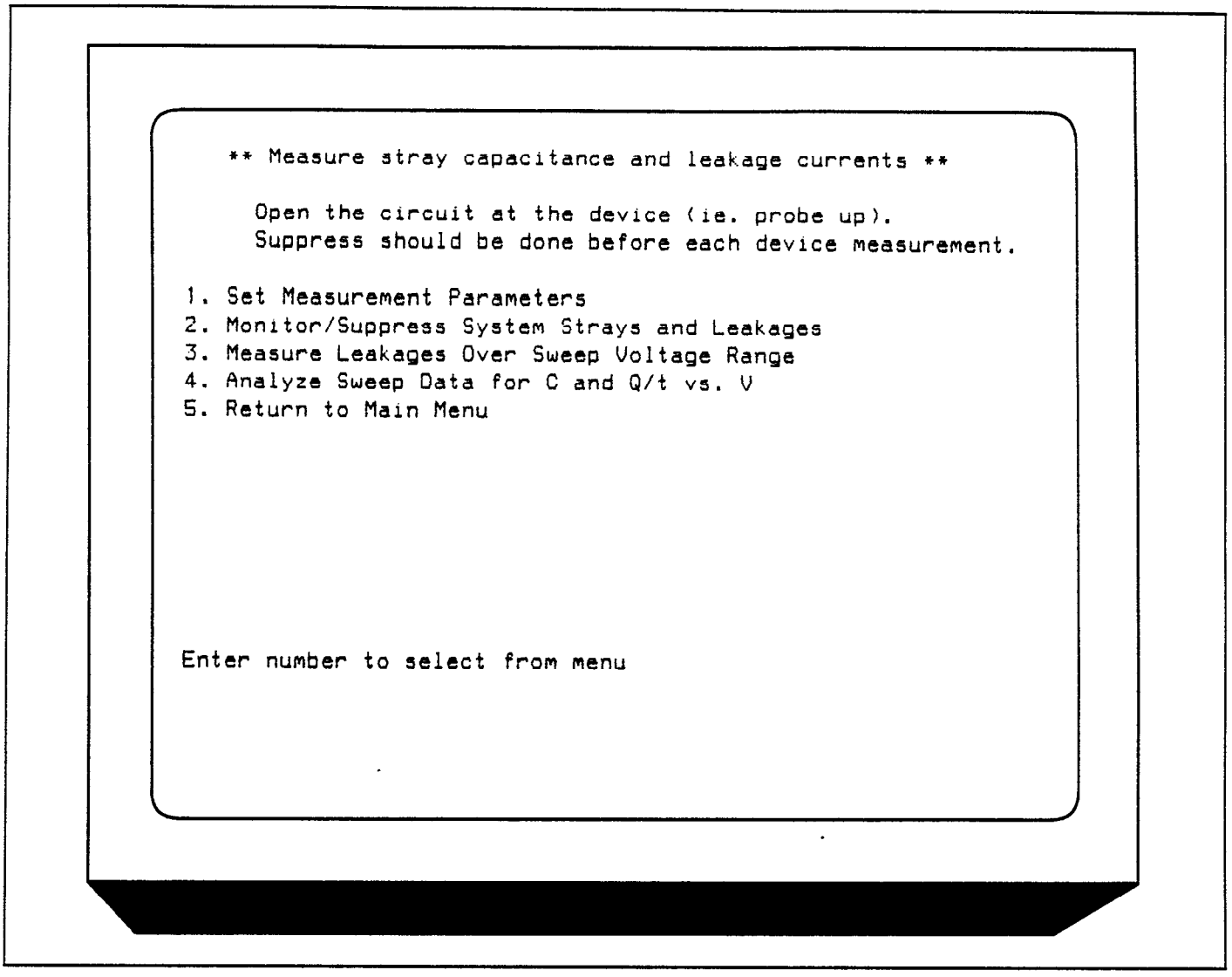


Figure 3-3. Stray Capacitance and Leakage Current

3.4.2 Parameter Selection

Menu Selections

By selecting option 1 on the system testing menu, you can access the parameter selection menu shown in Figure 3-4. You can also access this menu by pressing "M" from measurement menus. This menu allows you to program the following parameters:

1. Range for both quasistatic and high-frequency measurements (200pF or 2nF). The measurement ranges of both the Models 590 and 595 are set by this parameter.
2. Frequency for high-frequency measurements (100kHz or 1MHz). This parameter sets the operating frequency of the Models 590 and 5951.
3. Model (parallel or series). Model selects whether the device is modeled as a parallel capacitance and conductance, or a series capacitance and resistance.
4. Start V: ($-120 \leq V \leq 120$). Start V is the initial bias voltage setting of a CV sweep.
5. Stop V: ($-120 \leq V \leq 120$). Stop V is the final bias voltage setting of a CV sweep.
6. Bias V: Bias V is a static DC level used when static monitoring the system (for example, when testing for leakages and strays), and is the voltage level assumed when a sweep is completed.
7. T delay: ($0.07 \leq T \leq 199.99$sec). Note that the time delay must be properly set to attain device equilibrium.

8. Step V: (10mV, 20mV, 50mV, or 100mV): Step V is the incremental change of voltage of the bias staircase waveform sweep.
9. C-Cap: (Corrected capacitance). Uses the corrected capacitance program of the Model 595 when enabled. C-Cap should be used only when testing leaky devices.
10. Filter: Sets the Model 595 to Filter 2 when on, Filter 0 (off) when off.
    NOTE: Turning off the filter will increase the noise by 2.5 times.

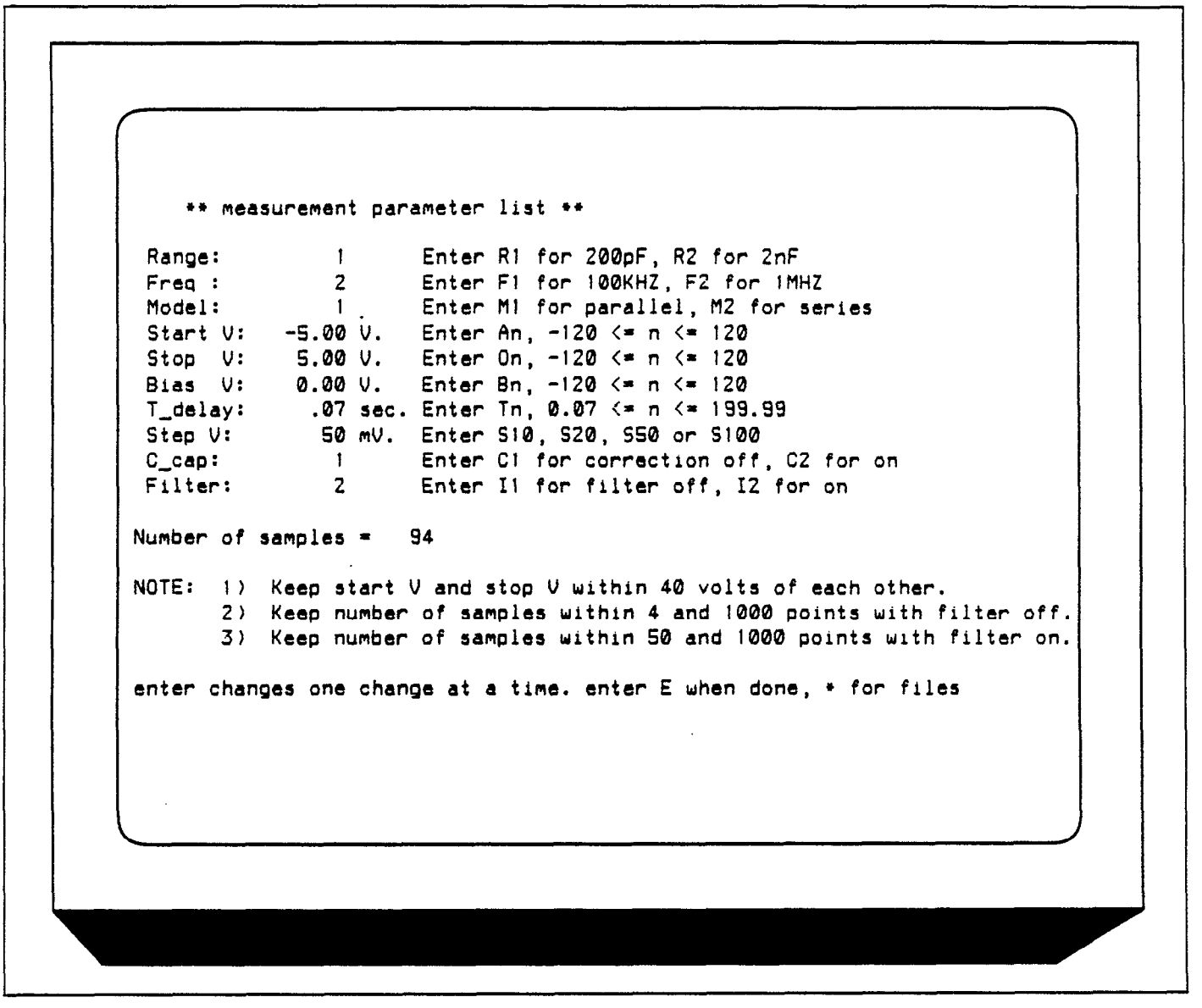


Figure 3-4. Parameter Selection Menu

Programming Parameters

To program a parameter, type in the indicated menu letter followed by the pertinent parameter. The examples below will help to demonstrate this process.

Example 1: Select 1MHz High-frequency Operation

To select high frequency operation, simply type in F2 at the command prompt and press the ENTER key.

Example 2: Program a +15V Bias V

Type in B15 and press the ENTER key.

Example 3: Select 0.1sec Delay Time

Type in T0.1 and press the ENTER key.

Example 4: Program a 20mV Step Voltage

Type in S20 and press the ENTER key.

Programming Considerations

When selecting parameters, there are a few points to keep in mind, including:

1. The maximum difference between the programmed Start V and Stop V is 40V. Exceeding this value will generate an error message.
2. The number of points must be between 4 and 1000 with the filter off, and between 50 and 1000 with the filter on to avoid curve distortion.
3. Bias voltage polarity is specified at the gate with respect to the substrate. For example, with a positive voltage, the gate will be biased positive relative to the substrate. Thus, an n-type material must be biased positive to be in the accumulation region.

NOTE

The voltage displayed on the front panel of the Model 590 is of the opposite polarity from the voltage displayed by the Package 82 software because of the gate-to-substrate voltage convention used. As described in Section 2, INPUT should be connected to the gate terminal, and OUTPUT should be connected to the substrate terminal.

Saving/Recalling Parameters

By pressing the " * " key, you can save or load parameters to or from diskette. The menu for these operations is shown in Figure 3-5. Press "S" (save) or "L" (load) to carry out the desired operation. You will then be prompted to type in the filename to be saved or loaded. An error message will be given if a file cannot be found or will be overwritten.

When the save option is selected, the parameter values currently in effect will be saved under the selected filename. Parameters loaded from an existing file will overwrite existing parameters.

Returning to Previous Menu

After all parameters have been programmed (or loaded from disk), press "E" to return to the system leakage testing menu.

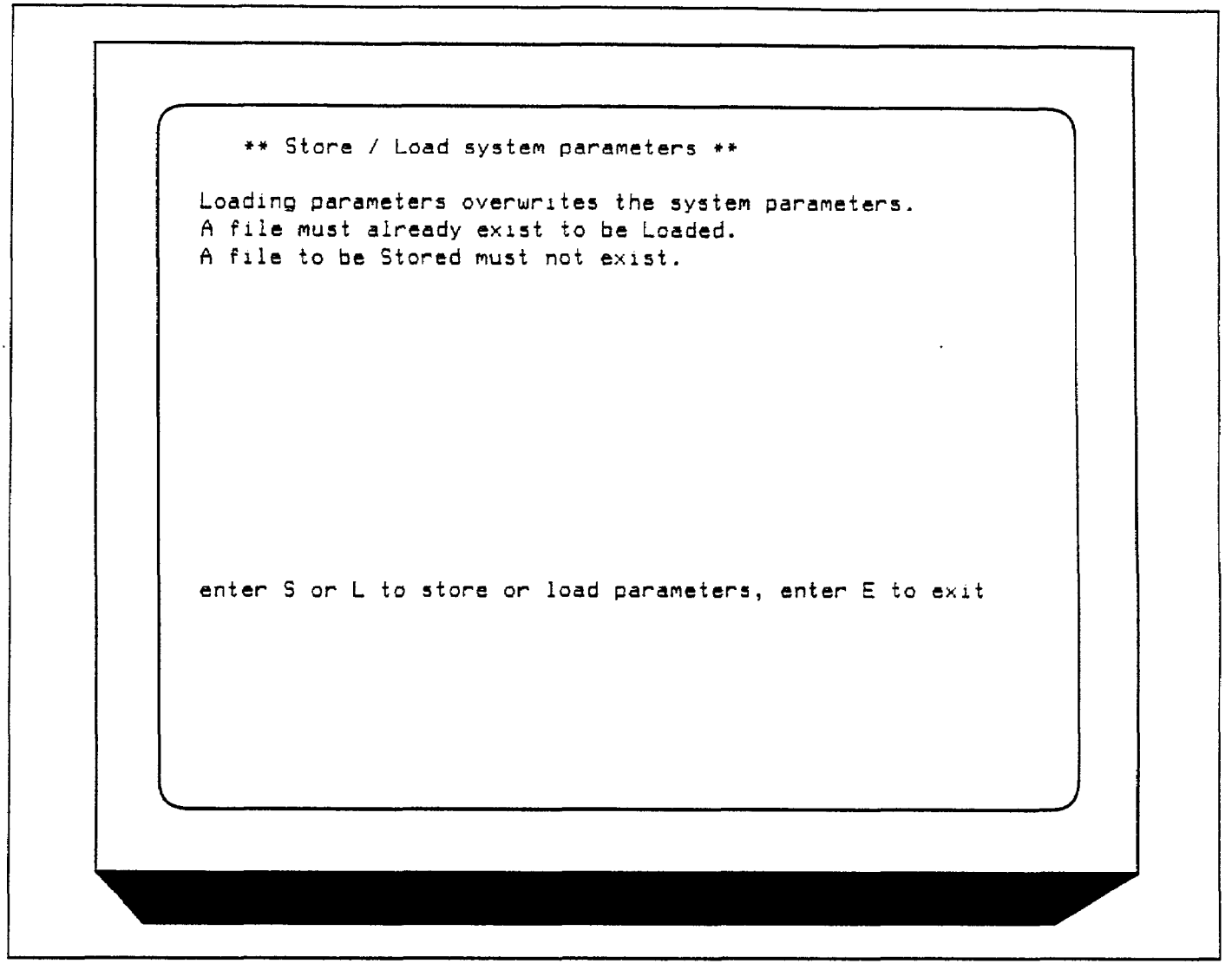


Figure 3-5. Save/Load Parameter Menu

3.4.3 Viewing Leakage Levels

Description

Before performing a test sweep, you should observe system leakage current and capacitance and fix any problems before continuing. Once system leakage levels have been reduced, proceed to paragraph 3.4.4 to perform a probes-up sweep of the system. Paragraph 3.9 discusses these factors in more detail.

Procedure

1. Select option 2 on the main menu followed by option 1 on the following menu. Program the following:

   Range: 200pF
   Frequency: 100kHz or 1MHz as required
   Model: Parallel
   Bias V: 0.00V
   T Delay: 0.07sec
   Step V: 50mV
   C-cap: Off
   Filter: On
   Press "E" then ENTER when parameters have been programmed, then select option 2, Monitor/Suppress System Strays and Leakages.
2. Disconnect the device from the system; in other words, place the probes in the up position. Close the shield on the test fixture.
3. If necessary, press "R" to turn off suppress and display "raw" readings.
4. You will then see a display similar to the one shown in Figure 3-6. The values shown are representative of what to expect in a typical system, but your values may be somewhat different.
5. Note the quasistatic and high-frequency capacitance and the leakage (Q/t) level. These values should be as small as possible. Ideally, stray capacitance should be less than 1% of the capacitance you expect to measure for optimum accuracy. Also, leakage current should be as low as possible.
6. If desired, press "Z" to suppress C_Q, C_H, and G.

Analyzing the Results

There are two key items to note when performing the above procedure: (1) excessive leakage current (Q/t), and (2) too much stray capacitance. If excessive leakage current is noted, you should check the following:

1. Make sure the proper cables are installed in the correct places. Be certain you have not interchanged Model 4801 (low-noise) cables with the Model 7051 (50Ω) cables.
2. Make sure all connecting jacks and connectors are free of contamination. Clean any dirty connectors with methanol and allow them to dry thoroughly before use.
3. Be certain that you are, in fact making a "probes-up" measurement.
4. Check to see that no leakage paths are present in the test fixture.
5. If necessary, tie down cables to avoid noise currents caused by cable flexing. Also, avoid vibration during testing.

Things to check for excessive stray capacitance include:

1. Verify that all cables are of the proper type and not of excessive length.
2. Verify the integrity of all cable shields and that the shield connections are carried through to the connectors.
3. Again, make sure the procedure is being performed in the "probes-up" configuration.
4. Use a test fixture of good, low-capacitance design.
5. Make certain the test fixture shield is in place when characterizing the system. The same precaution holds true when characterizing or measuring a device.

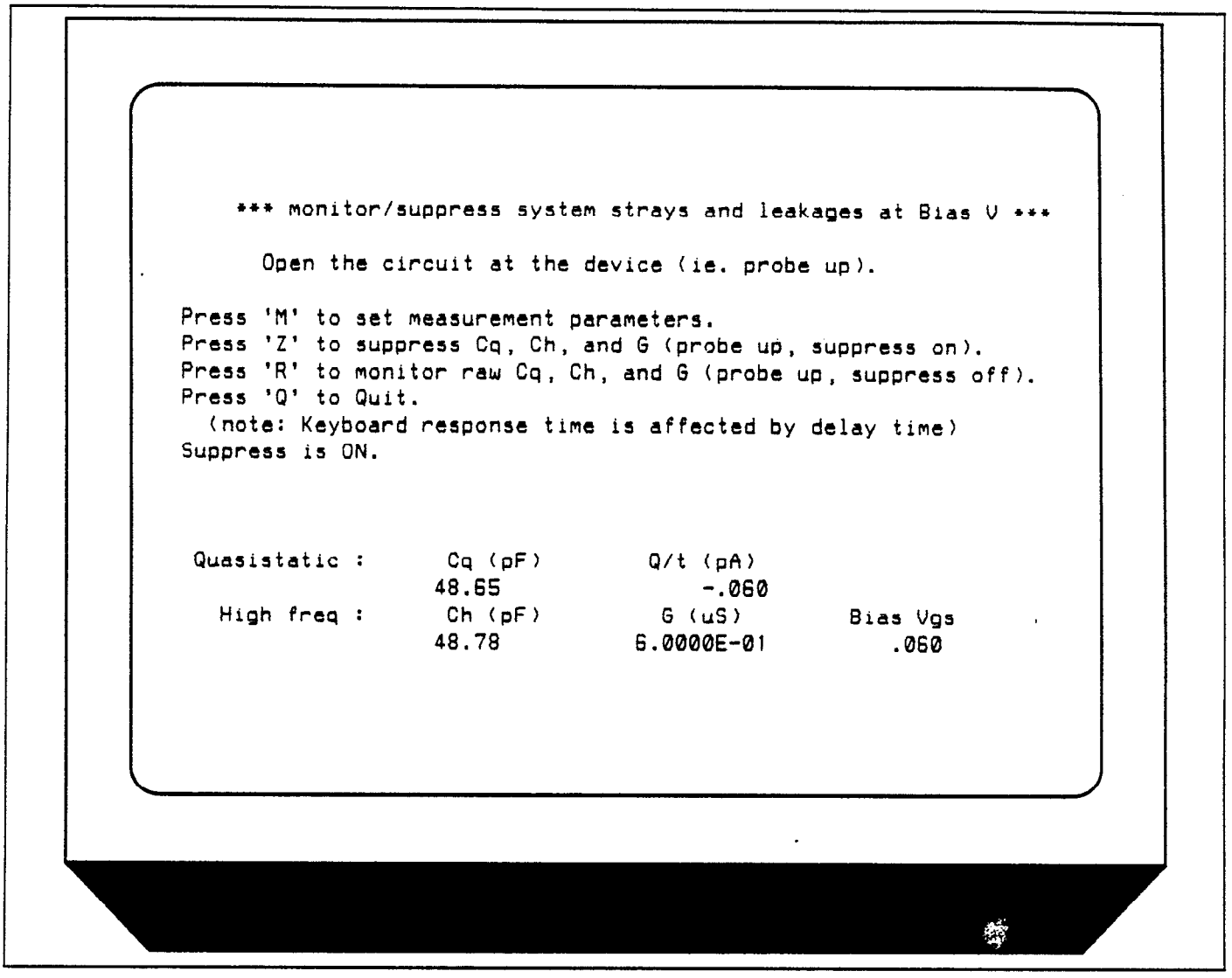


Figure 3-6. Monitor Leakage Menu

3.4.4 System Leakage Test Sweep

Description

This aspect of system leakage testing allows you to determine if there are any voltage-dependent leakages in the system. Basically there are two important points here: (1) how the leakage current varies as the bias voltage changes, and (2) apparent quasistatic capacitance variation with changes in voltage. These considerations are discussed more completely in paragraph 3.9.

Procedure

1. Select option 2 on the main menu, then option 1, set measurement parameters, and program the following parameters.

   Range: 200pF
   Frequency: 100kHz or 1MHz, as required
   Model: Parallel
   Start V: Most negative voltage generally used.
   Stop V: Most positive voltage usually used.

Bias V: 0.00V
T delay: 0.07sec
Step V: 100mV
C-Cap: Off
Press "E" then ENTER to exit. Select option 3, Measure Leakages over Sweep Voltage Range.

2. Place the probes in the up position to disconnect the device from the system.
3. Make sure the test fixture shield is in place before starting the procedure.
4. Press "R" to display "raw" readings. The computer display will show leakage levels, as shown in Figure 3-7.
5. Press "S" to initiate the sweep. During the sweep, the computer will display the following:

   Sweep in progress.

   Also, the sweep duration will be displayed.
6. At the end of the sweep, the PROBES UP DATA ANALYSIS MENU will be displayed:
   1. Graph both C_Q and C_H vs. Gate Voltage.
   2. Graph Q/t Current vs. Gate Voltage.
   3. Graph Conductance vs. Gate Voltage.
   4. Return to Previous Menu.
7. Select the desired sweep data option on the menu, to graph both quasistatic and high-frequency capacitance vs. gate voltage, and Q/t current vs. gate voltage.

Analyzing the Results

The leakage current you may observe during testing could be from two main sources: (1) constant leakage currents due to such sources as cables, and (2) voltage-dependent leakage currents caused by leakage resistances. A typical constant leakage current curve is shown in Figure 3-8, while a Q/t curve due to leakage resistance is shown in Figure 3-9. In the first case, note that the current is constant and does not depend on the applied voltage. For the case of curve dependent on leakage resistance, however, the current is directly proportional to the voltage, as is the case with any common resistor. The resistance, incidently, is simply the reciprocal of the slope of the line.

Since quasistatic capacitance is determined by integrating the current, the presence of unwanted leakage current will skew your quasistatic CV curves. Figure 3-10 shows the effects of constant leakage current. Here, the normal parasitic capacitance, C_P, is skewed upwards with an additional "phantom" capacitance added to the normal parasitic capacitance. The same type of curve skew will also occur with normal measurements, but its effects will usually be less noticable because of the larger capacitance levels involved.

A more serious situation is present in the case of the varying current, as shown in Figure 3-11. Now, the usually flat capacitance curve has been tilted, resulting in what is essentially a voltage-dependent capacitance. Again, the same curve-tilting effects can be expected for normal measurements, although usually to a lesser degree.

The high-frequency capacitance curves will not generally show any voltage-variability, and will show mainly parasitic capacitance at the frequency of interest. Such curves can also provide a good frame of reference for the quasistatic curves, as both quasistatic and high-frequency curves should be flat and very similar as long as leakage currents are sufficiently low.

The G vs. V curve shows AC loss at the selected measurement frequency (100kHz or 1MHz). The high frequency conductance value may represent a leakage resistance that is AC coupled into the test fixture.

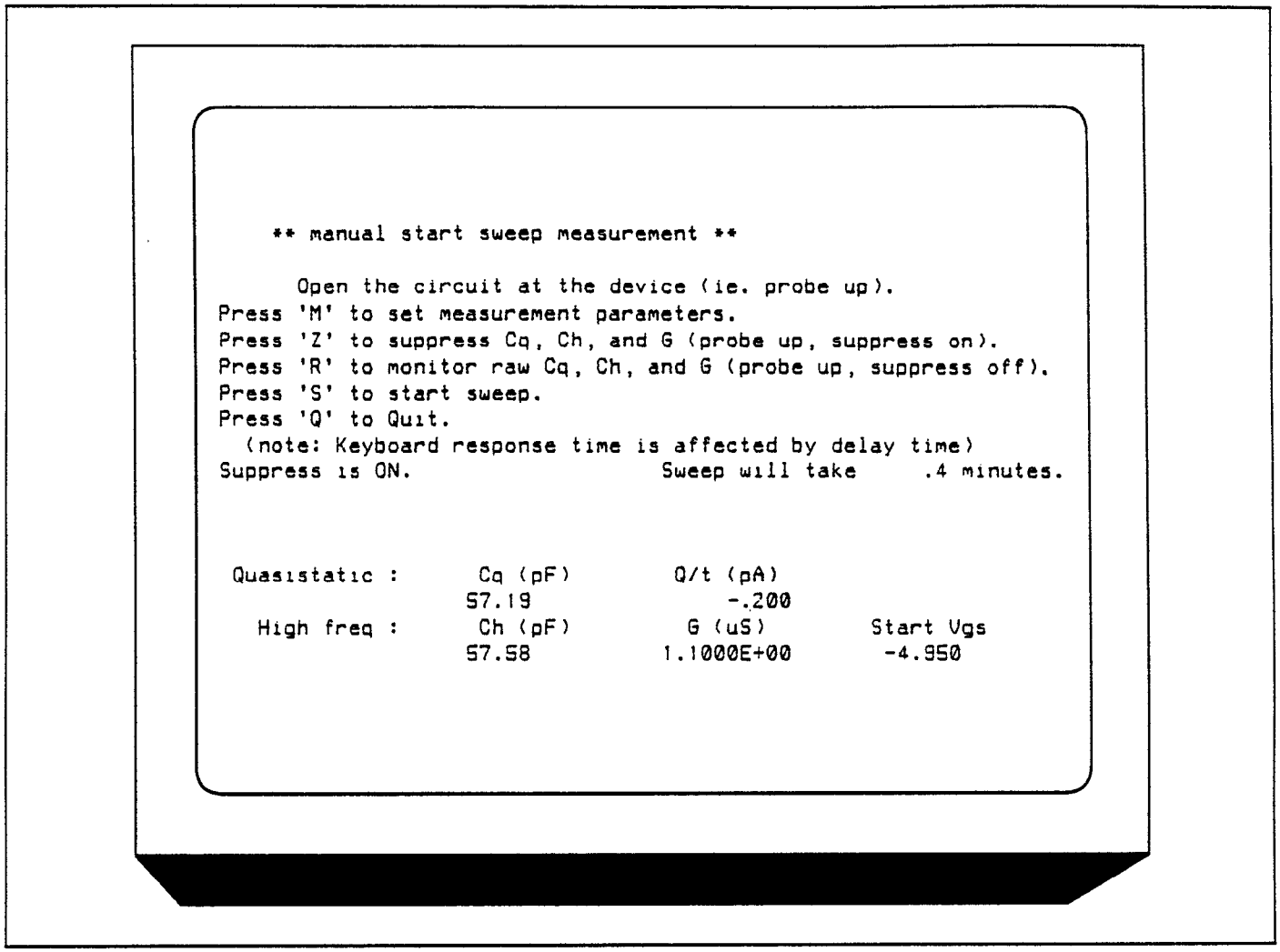


Figure 3-7. Diagnostic Sweep Menu

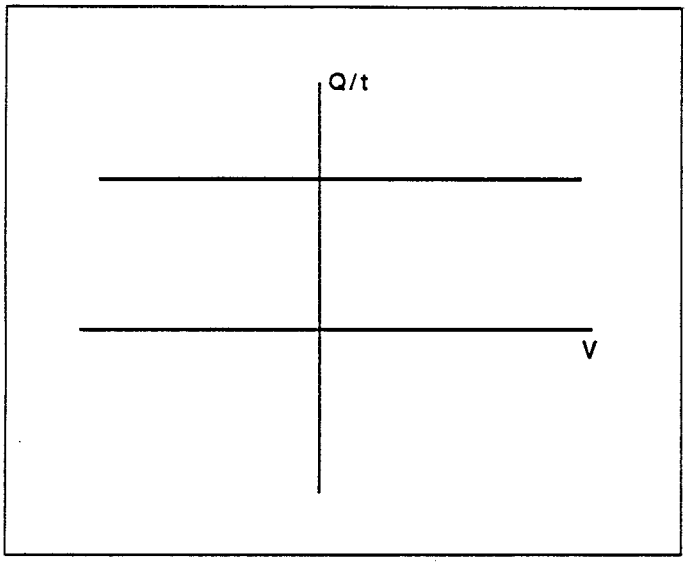


Figure 3-8. Leakage Due to Constant Current

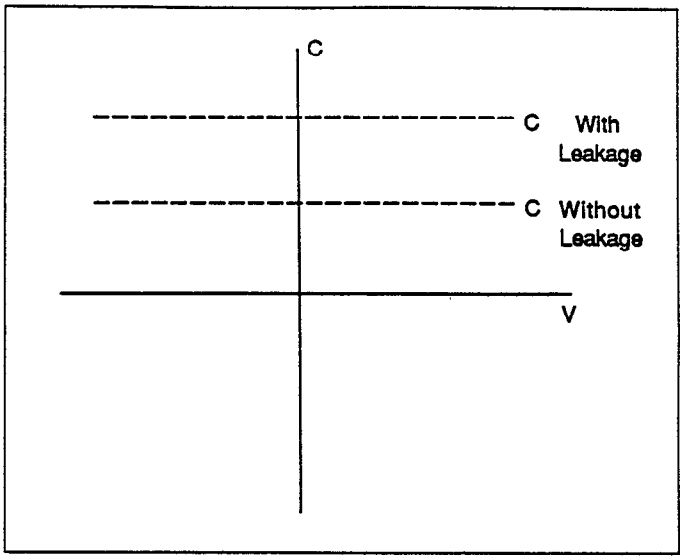


Figure 3-10. Constant Leakage Current Increases Quasistatic Capacitance

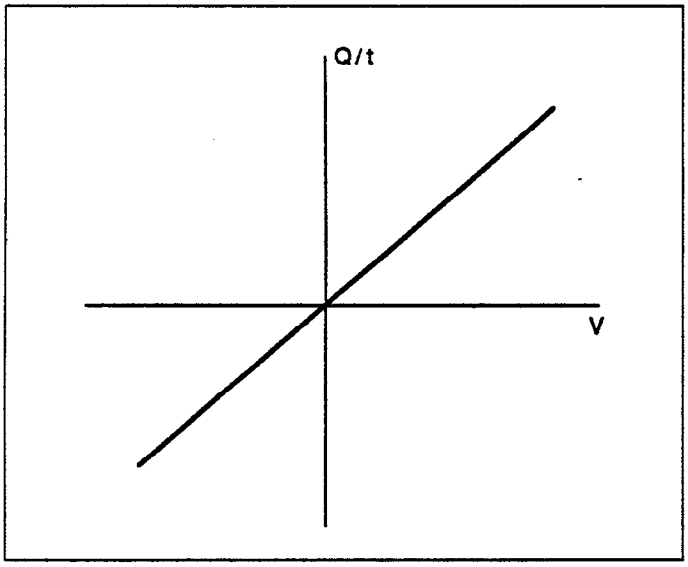


Figure 3-9. Q/t Curve with Leakage Resistance

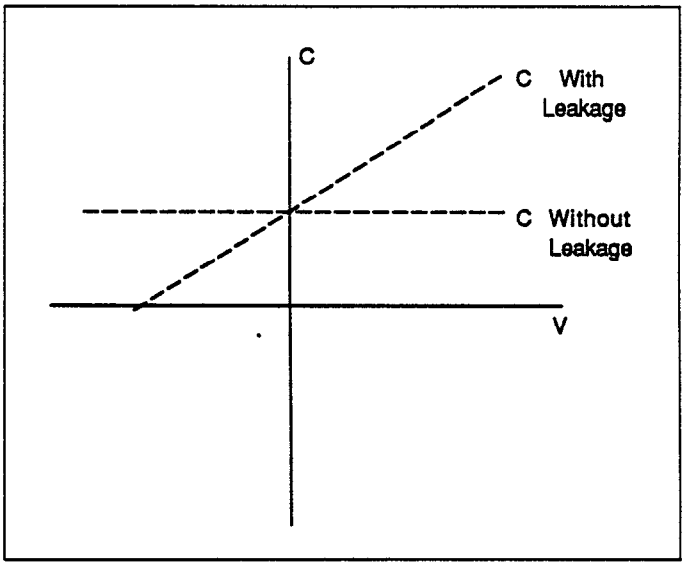


Figure 3-11. Quasistatic Capacitance with and without Leakage Current

3.4.5 Offset Suppression

Description

By selecting option 2 on the system leakage test menu, you can monitor the parameters listed below at a fixed bias voltage. This feature will give you an opportunity to suppress these leakage values to maximize accuracy. This suppression procedure should be carried out before each verified or performed measurement for optimum accuracy.

NOTE

Large leakage currents and stray capacitances should not be suppressed. Determine the source of the problem and correct it before using your system if large offsets are noted.

Monitored parameters include:

C_Q (quasistatic capacitance)
Q/t (leakage current)
C_H (high frequency capacitance)
G (conductance)
V_{GS} (gate voltage)

Suppressed parameters include C_Q, C_H, and G. Note that Q/t is not suppressed. Note that suppress on/off can be controlled from a measurement menu by pressing "Z" (suppress on) or "R" (suppress off).

Procedure

1. Disconnect the device from the system; in other words, place the probes in the up position. Close the shield on the probe fixture.
2. Select option 2, Monitor/Suppress System Strays and Leakages. You will then see a display similar to the one shown in Figure 3-6. The values shown here are representative of what to expect in a typical system, but yours could be somewhat different.
3. Press "Z" to suppress the leakage values. The Model 590 will be drift corrected, and its zero mode will be enabled to suppress C_H and G. Suppress on the Model 595 will also be enabled to suppress C_Q after a 15-second pause for settling. The status of suppress (on) will be displayed on the screen.
4. Press "Q" to return to the previous menu once suppression is complete.

Disabling Suppress

To disable suppress and display raw readings, simply press "R" at the command prompt.

3.5 CORRECTING FOR CABLING EFFECTS

Cable correction is necessary to optimize accuracy of high-frequency CV measurements, and to align C_Q and C_H for D_{IT} measurements. The process involves connecting calibration capacitors with precisely-known values to the connecting cables in place of the test fixture. Once correction is completed, correction constants are written to a disk file called "pkg82cal" and are recalled when the program is run.

The following paragraphs discuss required calibration sources as well as the overall cable correction procedure.

3.5.1 When to Perform Cable Correction

Cable correction must be performed the first time you use your system. Thereafter, for optimum accuracy, it is recommended that you cable correct your system whenever the ambient temperature changes by more than 5°C from the previous correction temperature. You can cable correct your system daily, if desired, but doing so is not absolutely essential.

NOTE

Cable correction parameters are stored on diskette in the "pkg82cal" file. These correction parameters are automatically retrieved during program initialization. The diskette containing correction parameters is in the default drive when running the program.

3.5.2 Recommended Sources

Table 3-1 summarizes the recommended calibration capacitors, which are part of the Model 5909 calibration set supplied with the Package 82. The values shown are nominal; you must use the 1kHz, 100kHz, and 1MHz values marked on the sources when correcting your system. Space has been provided in Table 3-1 for you to enter the actual values of your sources.

Table 3-1. Cable Correction Sources

Nominal Value*	1kHz Value**	100kHz Value**	1MHz Value**
47pF	_____	_____	_____
180pF	_____	_____	_____
470pF	_____	_____	_____
1.8nF	_____	_____	_____

*Nominal values inlcuded with Model 5909 Calibration Source

**Enter values from sources where indicated.

3.5.3 Source Connections

In order to correct your system, it will be necessary for you to disconnect your test fixture and connect each calibration capacitor in its place when prompted to do so, as shown in Figure 3-12. Use the supplied female-to-female BNC adapters to connect the sources to the cables.

When using the sources, be sure not to handle them excessively, as the resulting temperature rise will change the source values due to temperature coefficients. This temperature change will degrade the accuracy of the correction process.

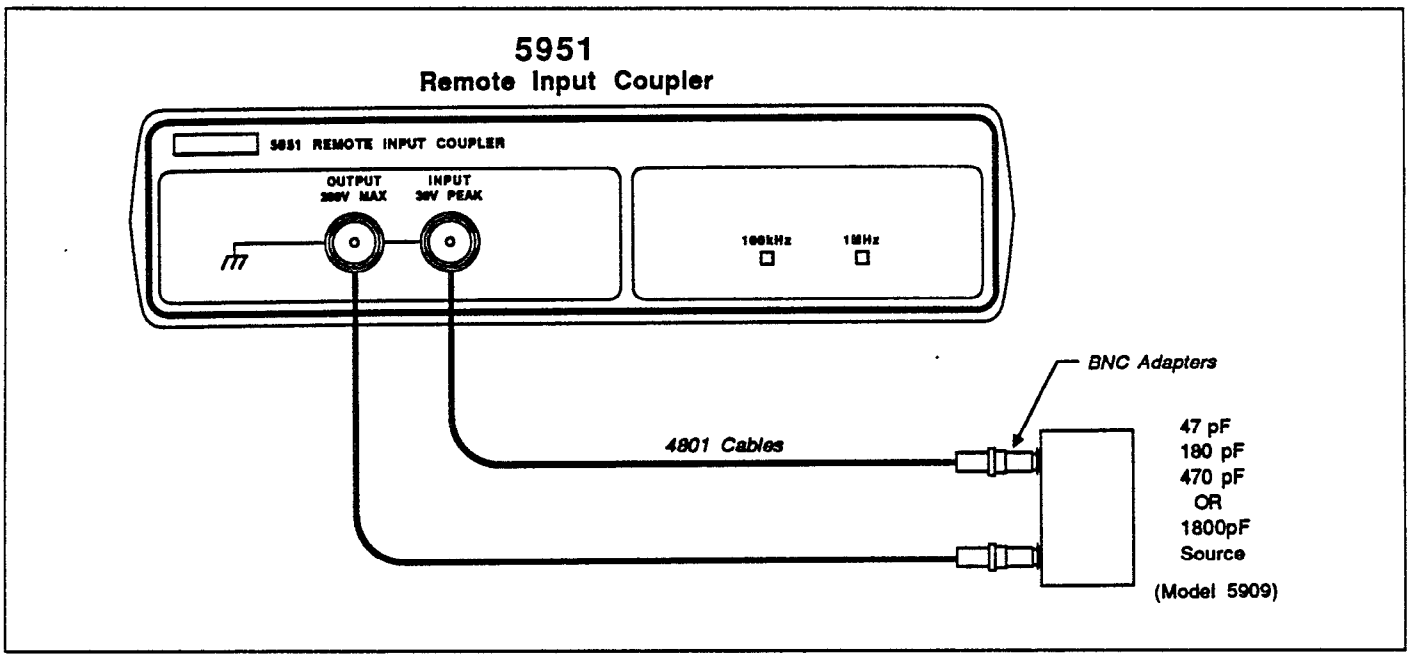


Figure 3-12. Cable Correction Connections

3.5.4 Software Modification

Before cable correcting your system the first time, it will be necessary for you to modify the software with the actual values of your particular calibration capacitors. This step is necessary because each set of sources has slightly different capacitance values. The software need not be modified again until you re-characterize your sources.

In order to modify your software, proceed as follows:

1. Load the Package 82 software in the usual manner, but do not RUN it.
2. LIST the first 30 to 40 lines of the program and locate the 12 string variables that contain the source values, as shown in Figure 3-13. The exact line numbers may vary depending on the software revision level.
3. Enter the EDIT mode and modify the variables with the actual 1kHz, 100kHz, and 1MHz values marked on your sources. In the string variables, "n" represents the nominal value (which should not be changed unless you are using different sources), "q" represents 1kHz, "k" is 100kHz, and "m" indicates 1MHz. For example, if your 1.8nF source has an actual 100kHz value of 1.802nF, modify the code as follows:

   680 Cs1800k$="1.802E-9"

NOTE

Nominal values can be changed, but the recommended source values are 25% (47,470) and 90% (180,1800) of full scale.

```
610   ! CALIBRATION SOURCE CONSTANTS
620   !
621   Cs47n$="4.7000E-11"                    ! 47pf NOMINAL
630   Cs47q$="4.7000E-11"                    ! 47pF at 1KHz
640   Cs47k$="4.7000E-11"                    ! 47pF at 100KHz
650   Cs47m$="4.7000E-11"                    ! 47pF at 1MHz
651   Cs180n$="1.8000E-10"                   ! 180pf NOMINAL
660   Cs180q$="1.8000E-10"                   ! 180pF at 1KHz
670   Cs180k$="1.8000E-10"                   ! 180pF at 100KHz
680   Cs180m$="1.8000E-10"                   ! 180pF at 1MHz
681   Cs470n$="4.7000E-10"                   ! 470pf NOMINAL
690   Cs470q$="4.7000E-10"                   ! 470pF at 1KHz
700   Cs470k$="4.7000E-10"                   ! 470pF at 100KHz
710   Cs470m$="4.7000E-10"                   ! 470pF at 1MHz
711   Cs1800n$="1.8000E-9"                   ! 1800pf NOMINAL
720   Cs1800q$="1.8000E-9"                   ! 1800pF at 1KHz
730   Cs1800k$="1.8000E-9"                   ! 1800pF at 100KHz
740   Cs1800m$="1.8000E-9"                   ! 1800pF at 1MHz
```

Figure 3-13. Partial Listing Showing Nominal Source Values

4. After modifying all 12 variables, save the program as a working file. Be sure that you use this modified program instead of the original from now on; otherwise, the cable correction procedure will yield erroneous calibration values, resulting in improper measurements.

3.5.5 Correction Procedure

As noted earlier, the following procedure must be performed the first time you use your system, and it should be done when the ambient temperature changes by more than 5°C from the previous correction point. Proceed as follows:

1. Load the modified Package 82 software (see paragraph 3.5.4) and RUN it in the usual manner.
2. Select option 2 and monitor the leakage current to assure proper hookup. Next, connect a calibration source to verify hookup, and return to the main menu.
3. Select option 3, Correct for Cabling Effects, on the main menu.
4. The program will then enter the cable correction portion of the program. Initially, you will be prompted to be sure that the calibration source values have been altered as described above. The actual source values will be displayed.
5. Disconnect the cables from the chuck when prompted to do so, and press ENTER to continue.
6. Follow the prompts to complete the correction process. For each range and frequency, you will be prompted when to disconnect the cables and connect the appropriate sources, as shown in Figure 3-12. After each correction, you will be given an opportunity to retry (press "R"). The Retry option will allow you to repeat the correction for the presently-selected range and frequency (for example 100kHz/2nF or 1MHz/200pF).

NOTE

Be sure to connect the right sources as no error messages will be given for improper correction.

7. When correction is completed, you will be returned to the main menu.
8. If you wish to verify correction accuracy, select option 2 on the main menu (Testing for Leakages and Strays) and then monitor system readings with calibration sources connected. Be sure to select the appropriate range and frequency for the sources being measured.

Note: If a mistake was made during correction, either repeat the correction or purge the "pkg82cal" file from your disk and rerun the "PKG82CV" program.

3.5.6 Optimizing Correction Accuracy to Probe Tips

To correct as close as possible to the probe tips, construct two BNC cables (50Ω, low noise if possible) equal in length to the distance from the last BNC connectors to the probe tips. Connect these substitute cables in place of the last cables with prober, and perform the correction procedure outlined in paragraph 3.5.5. After correction, replace the original cable.

3.6 DETERMINING OXIDE CAPACITANCE AND EQUILIBRIUM DELAY TIME

Before device measurement, it is necessary to determine optimum delay time, t_{DELAY}, to attain device equilibrium in the inversion region. It is often desirable to verify C_{ox}, thickness, and gate area. The following paragraphs discuss the procedures for determining C_{ox} and optimum delay time.

3.6.1 C_{ox} and Delay Time Menu

To determine C_{ox} and optimum delay time, select option 4, Find Device C_{ox} and Equilibrium Delay Time, on the Package 82 main menu. The computer will then display the menu shown in Figure 3-14. By selecting the appropriate option, you can perform the following:

1. Program measurement parameters as required.
2. Perform a diagnostic sweep CV sweep in order to check for proper accumulation and inversion voltages, as well as to verify device type.
3. Monitor oxide capacitance, Cox, and find oxide thickness, t_{ox}, and gate area, A.
4. Display Q/t and C vs. delay time to determine optimum delay time.

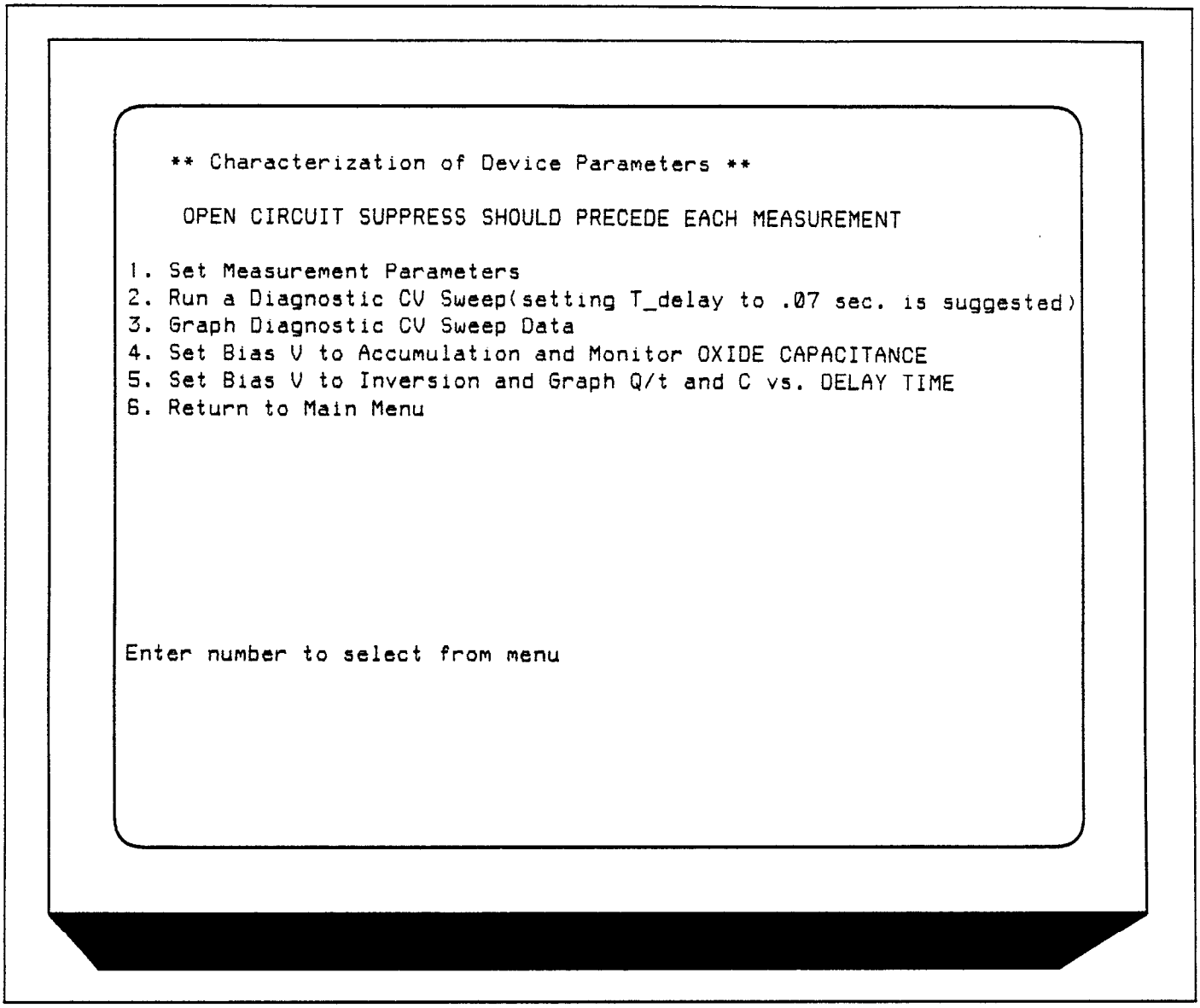


Figure 3-14. C_{ox} and Delay Time Menu

3.6.2 Running and Analyzing a Diagnostic CV Sweep

Before testing for C_{ox} and delay time, you should run a diagnostic sweep on the device to check to see that proper start and stop voltages have been programmed for the accumulation and inversion regions of the curve.

Procedure

1. Before running a sweep, verify connections and suppress if necessary, as outlined in paragraph 3.4.5.
2. Select menu option 1, Set Measurement Parameters, and program the following:

   Range: 200pF or 2nF depending on expected capacitance.
   Frequency: 100kHz or 1MHz, as required.
   Model: Parallel.
   Start V: As required to bias the device in accumulation.
   Stop V: As required to bias the device in inversion.
   T delay: 0.07sec
   Step V: 50mV
   C-Cap: Off
   Filter: On

   When programming voltage parameters, remember that the voltage polarity is at the gate with respect to the substrate. Thus, to begin the sweep in inversion on an n-type material, Start V would be negative and Stop V would be positive.
3. Return to the C_{ox} menu by pressing "E" then ENTER.
4. Select option 2, Run a Diagnostic CV Sweep, on the menu, then press "Z" to enable suppress if C_Q, C_H, or G offsets are >1% of anticipated measured values.
5. Place the probes down on the contact points for the device to be tested and close the fixture shield.
6. Press "S" to initiate the sweep after Q/t settles to the system leakage level. You can abort the sweep, by pressing any key, if desired.
7. After you are prompted that the sweep is completed, press ENTER to return to the characterization menu.
8. Select option 3, Graph CV Sweep Data. See the discussion below for interpretation of the CV graph and recommendations.

Analyzing the Results

The high-frequency curve should be analyzed to ensure that the sweep voltage range is sufficient to bias the device well into both accumulation and inversion. Typical high-frequency curves are shown in Figures 3-15 and 3-16. It may be necessary to re-program the Start V or the Stop V (or both) to bias the device properly. Re-run the sweep to verify that the new values are appropriate.

The curves can also be used to verify the type of material under test. As shown in Figure 3-15, an n-type material is biased in inversion when the gate voltage is substantially negative, while the device is in accumulation when the gate voltage is positive. Note that the high-frequency capacitance in inversion is much lower than the high-frequency capacitance in accumulation.

The same situation holds true for p-type curves (Figure 3-16) except the polarities are reversed. In this instance, inversion occurs for gate voltages much greater than zero, while the accumulation region occurs when the device is biased negative.

The oxide capacitance, C_{ox}, is simply the maximum high-frequency capacitance when the device is biased in accumulation. Its value can be taken directly from the CV plot, or a more accurate C_{ox} value can be determined using the procedure in the next paragraph.

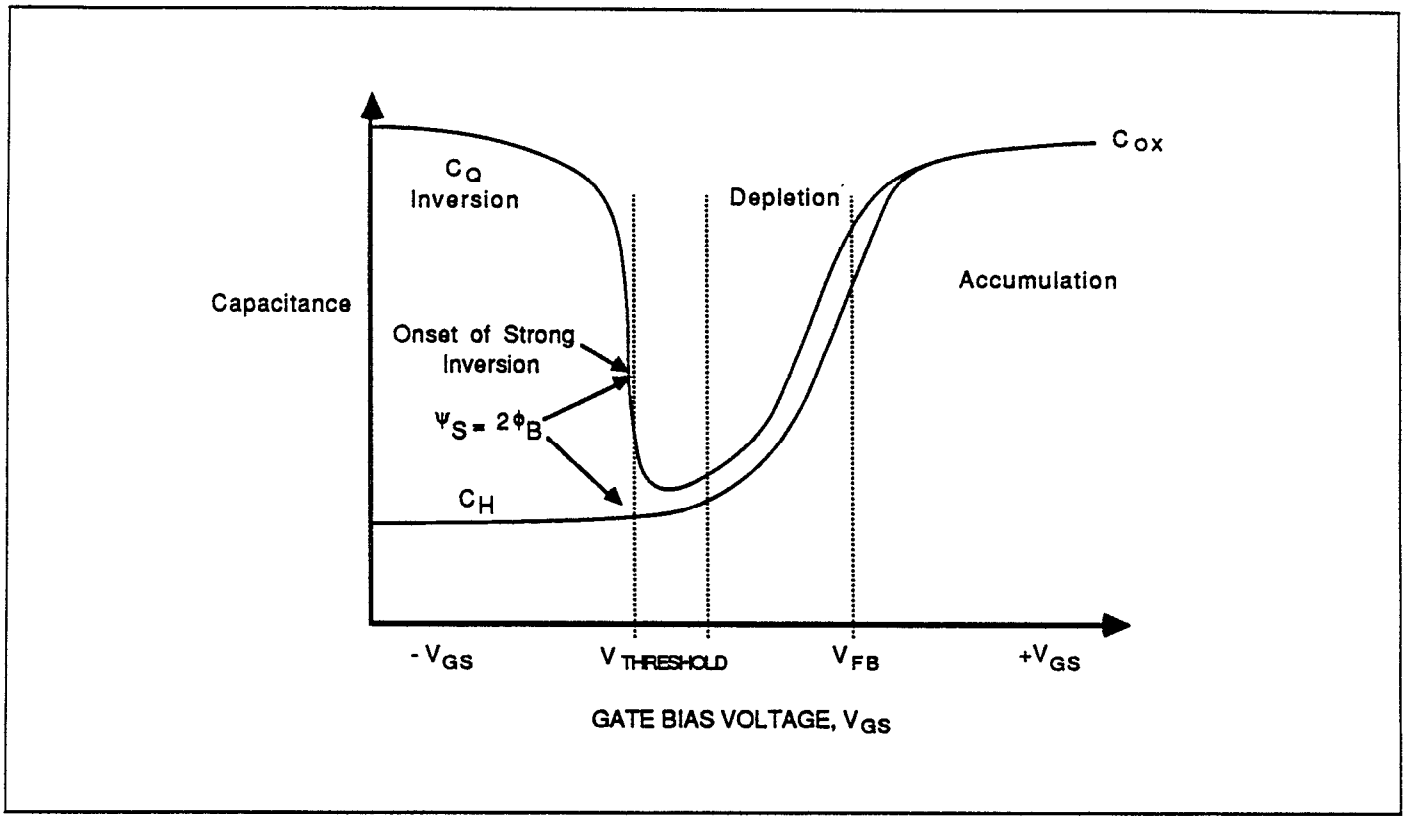


Figure 3-15. CV Characteristics of n-type Material

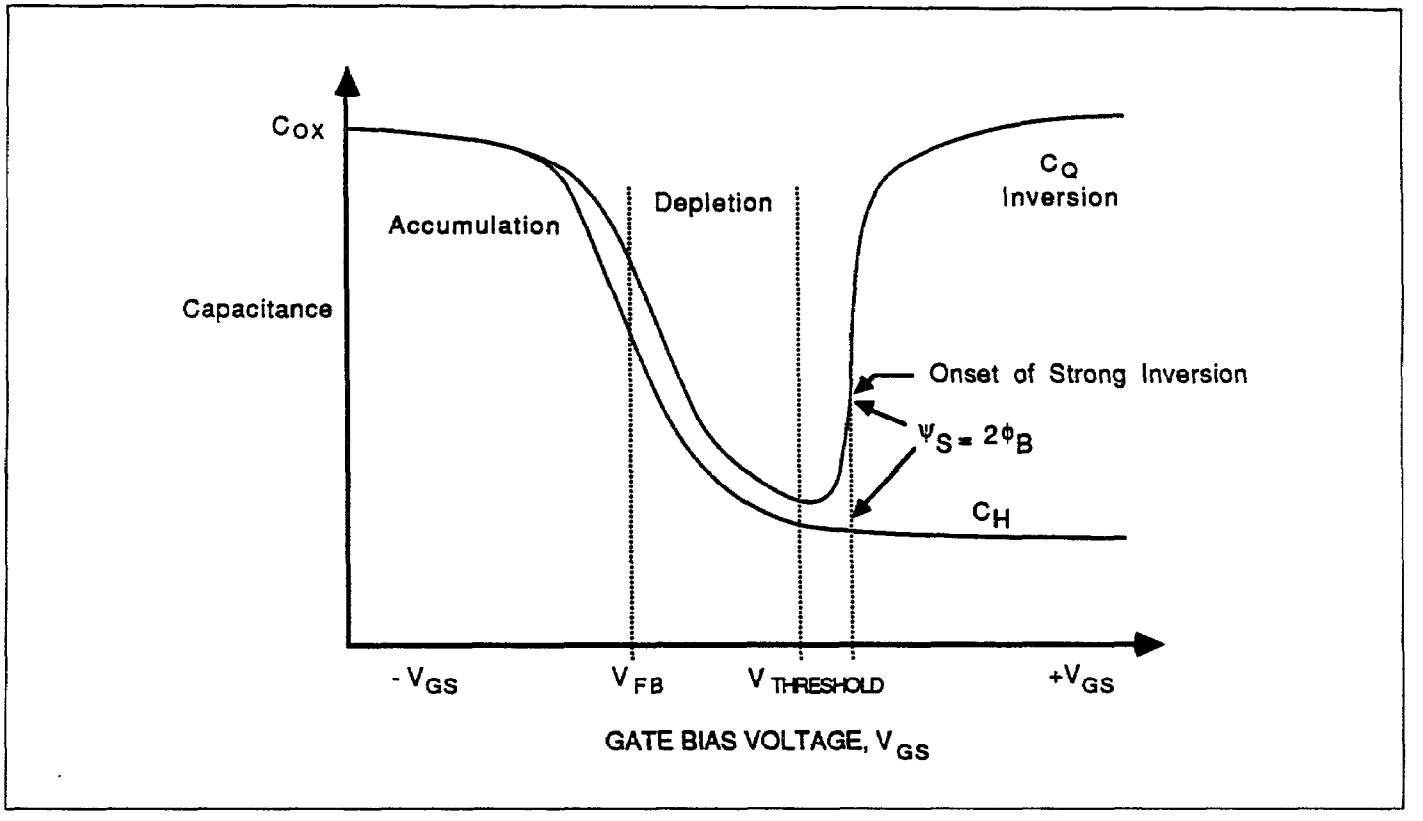


Figure 3-16. CV Characteristics of p-type Material

3.6.3 Determining Oxide Capacitance, Oxide Thickness, and Gate Area

The oxide capacitance can be determined by biasing the device in accumulation and noting the high-frequency capacitance, which is essentially C_{ox}. Once C_{ox} is known, the oxide thickness (t_{ox}) or gate area (A) can be calculated as discussed below. Note that these values are saved with the data array and are used for analysis, as discussed in Section 4.

NOTE

C_{ox}, t_{ox}, and area are offered here for quick device verification, and may be changed or added in the analysis section.

Procedure

1. Select the Monitor Oxide Capacitance option on the menu, then press "M" and program the Bias V parameter to bias the device in accumulation. Refer to the diagnostic curves made as outlined in paragraph 3.6.2 to determine optimum accumulation voltage. All other parameters should remain the same as those given in paragraph 3.6.2.
2. Verify that probes-up capacitance is zero, and suppress if necessary, by pressing "Z".
3. Place the probes down on the device contact points and close the test fixture shield.
4. Note the high frequency capacitance displayed on the computer CRT and verify that it is stable. A typical display, including option selections for C_{ox}, t_{ox}, and gate area, is shown in Figure 3-17.
5. To enter C_{ox}, press "C" and then type in the high frequency capacitance reading as C_{ox}. Press ENTER to complete the process. Entering C_{ox} will force a recalculation of t_{ox} or A with appropriate prompts.
6. If the oxide thickness (t_{ox}) is known, and you wish to find gate area, press T. Type in the oxide thickness in nm, and the computer will display the computed gate area in cm^2.
7. If, on the other hand, gate area is known, you can find t_{ox} by pressing "A" and then typing in the gate area, A in cm^2. The computer will then display oxide thickness in nm.
8. Press "Q" once data entry is complete to return to the previous menu.

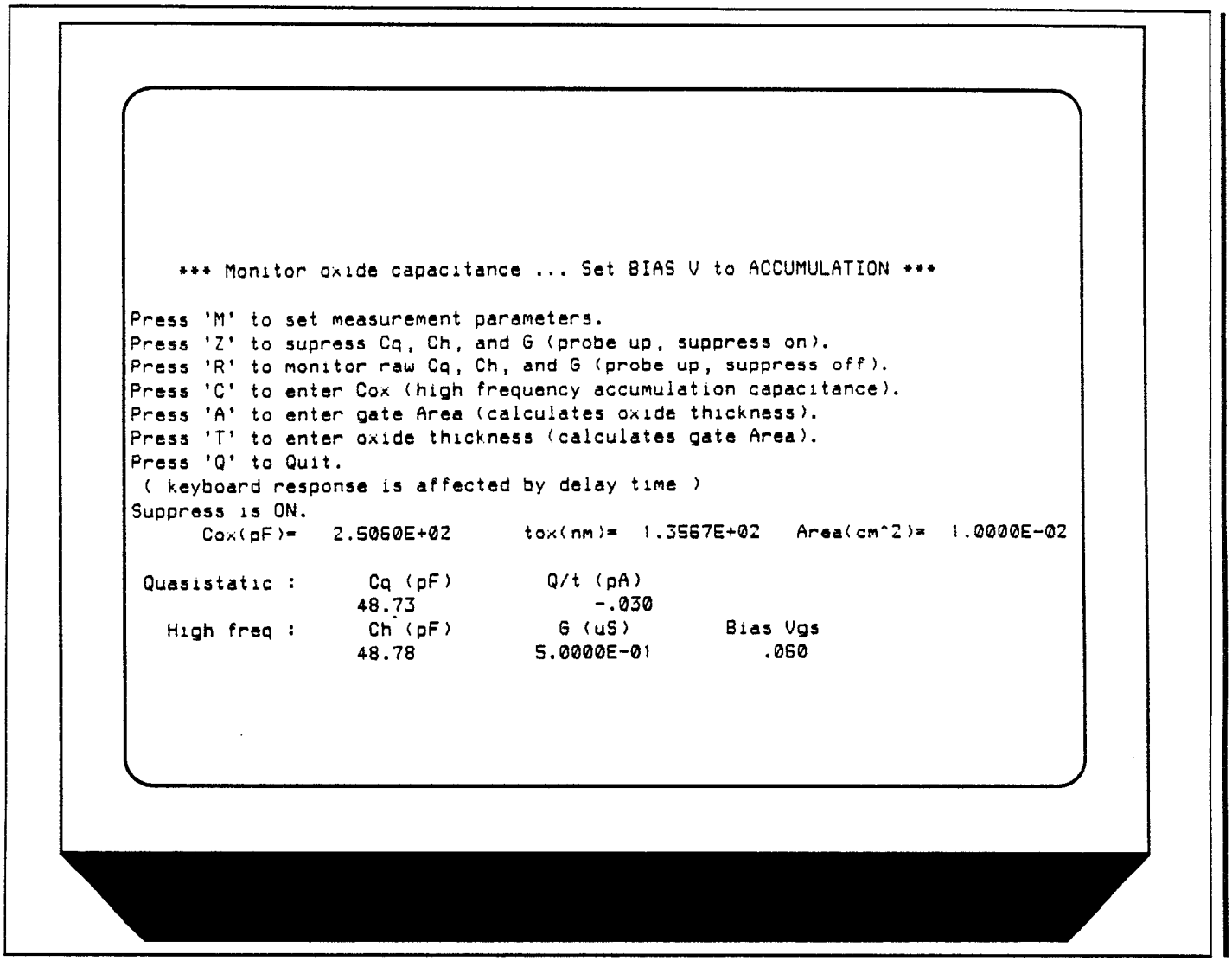


Figure 3-17. Oxide Capacitance Menu

Oxide Thickness and Gate Area Calculations

Oxide thickness is calculated from C_{ox} and the known gate area as follows:

$$t_{ox} = \frac{A\ \epsilon_{ox}}{(1 \times 10^{-19})\ C_{ox}}$$

Where: t_{ox} = oxide thickness (nm)
A = gate area (cm^2)
ϵ_{ox} = permittivity of SiO_2 (3.400×10^{-13} F/cm)
C_{ox} = oxide capacitance (pF)

Gate area is calculated simply by rearranging the above equation to solve for A:

$$A = \frac{(1 \times 10^{-19})\ C_{ox}\ t_{ox}}{\epsilon_{ox}}$$

Where: A = gate area (cm^2)
ϵ_{ox} = permittivity of SiO_2 (3.400×10^{-13} F/cm)
C_{ox} = oxide capacitance (pF)
t_{ox} = oxide thickness (nm)

Note that ϵ_{ox} and other constants are located at the top of the program listing and are defined for silicon and silicon dioxide; these constants can be changed for analysis of other types of materials if desired.

3.6.4 Determining Optimum Delay Time

Description

For accurate quasistatic measurements, the delay time must be carefully chosen in order to ensure that the device remains in equilibium in the inversion region during a voltage sweep. The procedure given in this section covers methods to find the optimum delay time from Q/t and C vs V curves. A test fixture light can be controlled to speed up device equilibium.

Delay Time Menu

Select option 5, Graph Q/t and C vs. DELAY TIME. The computer will then display the menu shown in Figure 3-18. Through this menu, you can choose the following options.

1. Set Measurement parameters (M).
2. Suppress strays and leakages (Z).
3. Display "raw" readings (R).
4. Toggle light on or off (L). If your test fixture is equipped with a light to shine on the device, you can turn it on to reach the equilibrium point more rapidly. See paragraph 3.8 for information on connecting a light to the Package 82 system.
5. Enter maximum delay time (D). Keep in mind that the plot will take 9.9 times the maximum delay time to complete. For example, if you program a maximum delay time of 10 seconds, the plot will take 99 seconds to complete.
6. Start measurement (S).
7. Graph data points (G) C_Q and Q/t vs. t_{DELAY} will be plotted by this option.
8. Print data points (P). After the measurement is completed, you can print out the data points on the printer by selecting this option.
9. View data points on CRT (V).
10. Quit (Q). Pressing "Q" returns you to the previous menu.

Procedure

1. Perform probes-up suppression, by pressing "Z".
2. Press "M", and program the following parameters.

   Range: 200pF or 2nF, depending on expected capacitance.

   Bias V: As required to bias device in inversion (Use value from diagnostic plot).

   Step V: Set amplitude to be used when actually testing device (polarity is derived from Start V and Stop V).

   C-Cap: Off except for leaky devices (see discussion below).

   Filter: On.
3. Place the probes down on the device contact points and close the test fixture shield.
4. Press "D" and enter the desired maximum delay time. Keep in mind that the plot will take 9.9 times the maximum delay time to complete.
5. If a light is connected to your system, press "L" to turn on the light to achieve equilibrium more rapidly. Note that the light status is indicated on the computer CRT.
6. Observe the Q/t readings on the computer CRT. Wait until the Q/t value is reduced to the system leakage level. At this point, the device has reached equilibrium.
7. If you are using a light, turn it off once equilibrium is reached before making the measurement by pressing "L". Again, the status of the light will be indicated on the computer CRT (it may take a few moments for the device to settle after the light is turned off).
8. Once equilibrium is reached, press "S" to begin the measurement. The computer will display the values of C_Q, Q/t, and t_{DELAY} on the CRT, up to a maximum of 11 points.
9. Once all points have been taken, press "G" to generate the Q/t and C_Q vs. t_{DELAY} graph, an example of which is shown in Figure 3-19. Note that both Q/t and C_Q will be automatically scaled along the Y axis of the graph. If desired, you can generate a hard-copy graph by using "DUMP GRAPHICS" to a compatible printer.
10. Once the graph is completed, note both the Q/t and capacitance curves. The optimum delay time occurs when both curves flatten out to a slope of zero. For maximum accuracy, choose the second point on the curves after the curve in question has flattened out (see discussion below for additional considerations).
11. After choosing the optimum delay time, exit the graph submenu. You can now print out or view your data points on the printer by pressing "P" or "V" if desired.
12. Press "Q" to return to the previous menu after optimum delay time has been determined.
13. Once the optimum delay time has been accurately determined, press "M", and program T Delay with the optimum delay time value determined by this procedure. Use this delay time when testing and measuring the device, as described in paragraph 3.7.

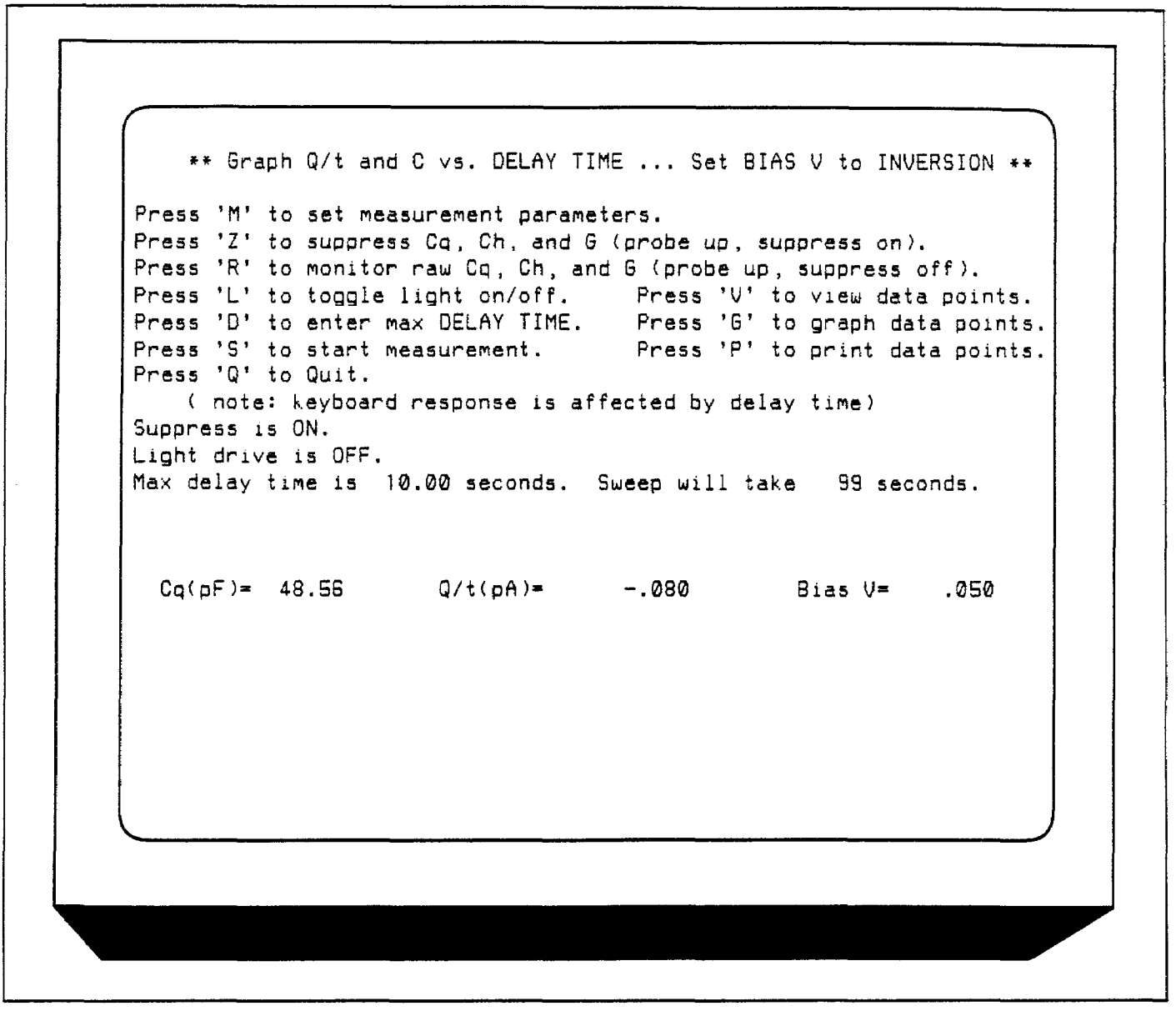


Figure 3-18. Delay Time Menu

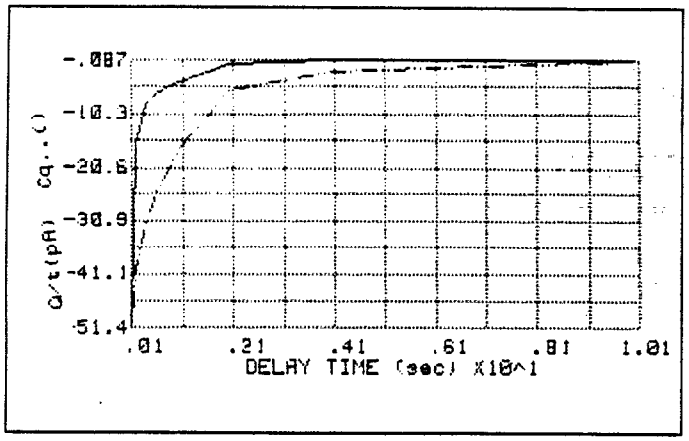


Figure 3-19. Q/t and C_Q vs. Delay Time Example

Analyzing the Results

For best accuracy, you should choose a delay time corresponding to the second point on the flat portion of both the capacitance and Q/t curves, as shown in Figure 3-20. Of course, for long delay times, the measurement process can become inordinately long with some devices. To speed up the test, you might be tempted to use a shorter delay time, one that results in a compromise between speed and accuracy. However, doing so is not recommended since it is difficult to quantify the amount of accuracy degradation in any given situation.

Determining Delay Time with Leaky Devices

When testing for delay time on devices with relatively large leakage currents, it is recommended that you use the corrected capacitance feature, which is designed to compensate for leakage currents. The reason for doing so is illustrated in Figure 3-21. When large leakage currents are present, the capacitance curve will not flatten out in equilibrium, but will instead either continue to rise (positive Q/t) or begin to decay (negative Q/t).

Using corrected capacitance results in the normal flat capacitance curve in equilibrium due to leakage compensation. Note, however, that the curve taken with corrected capacitance will be distorted in the nonequilibrium region, so data in that region should be considered to be invalid when using corrected capacitance.

NOTE

If it is necessary to use corrected capacitance when determining delay time, it is recommended that you make all measurements on that particular device using corrected capacitance (C-cap on).Return to the set parameters menu to turn on C-cap.

Testing Slow Devices

A decaying noise curve, such as the dotted line shown in Figure 3-20, will result if the maximum delay time is too short for the device being tested. This phenomenon, which is most prevalent with slow devices, occurs because the range signal is too small. To eliminate such erroneous curves, choose a longer maximum delay time. A good starting point for unknown devices is a 30-second maximum delay time, which would result in a five-minute test duration.

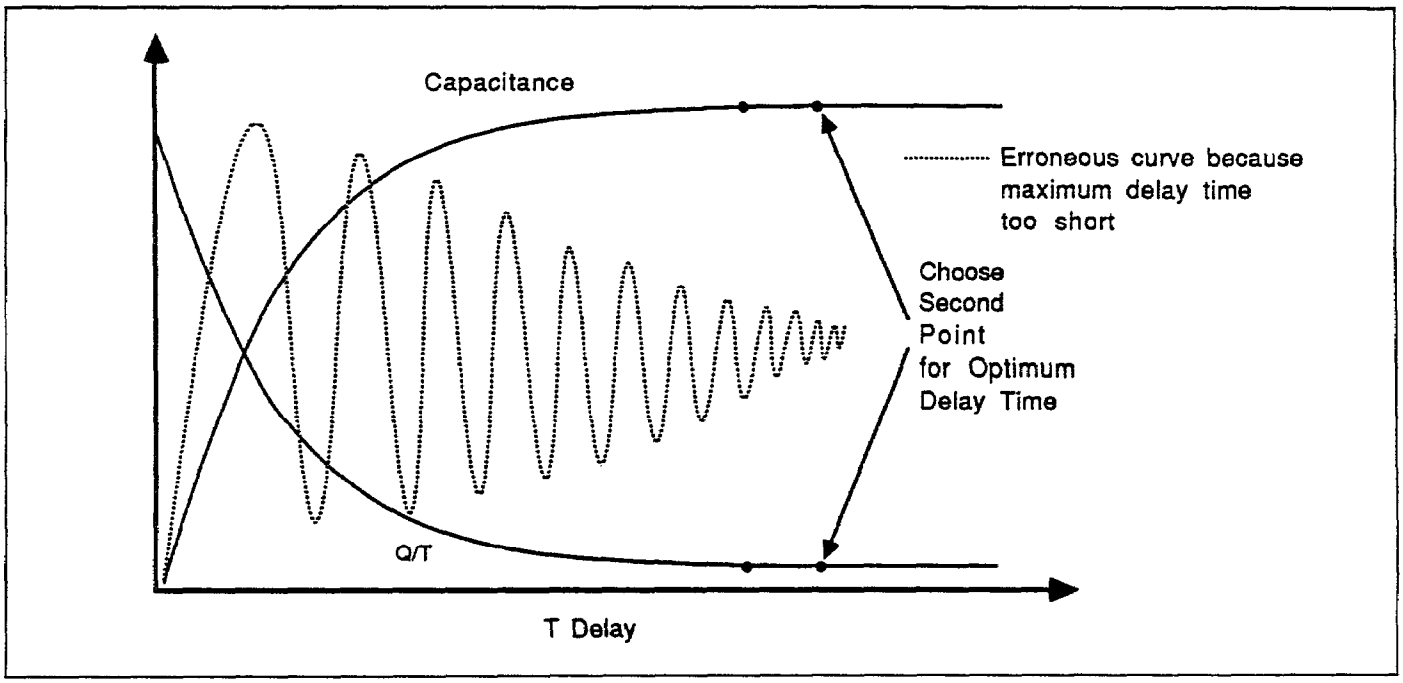


Figure 3-20. Choosing Optimum Delay Time

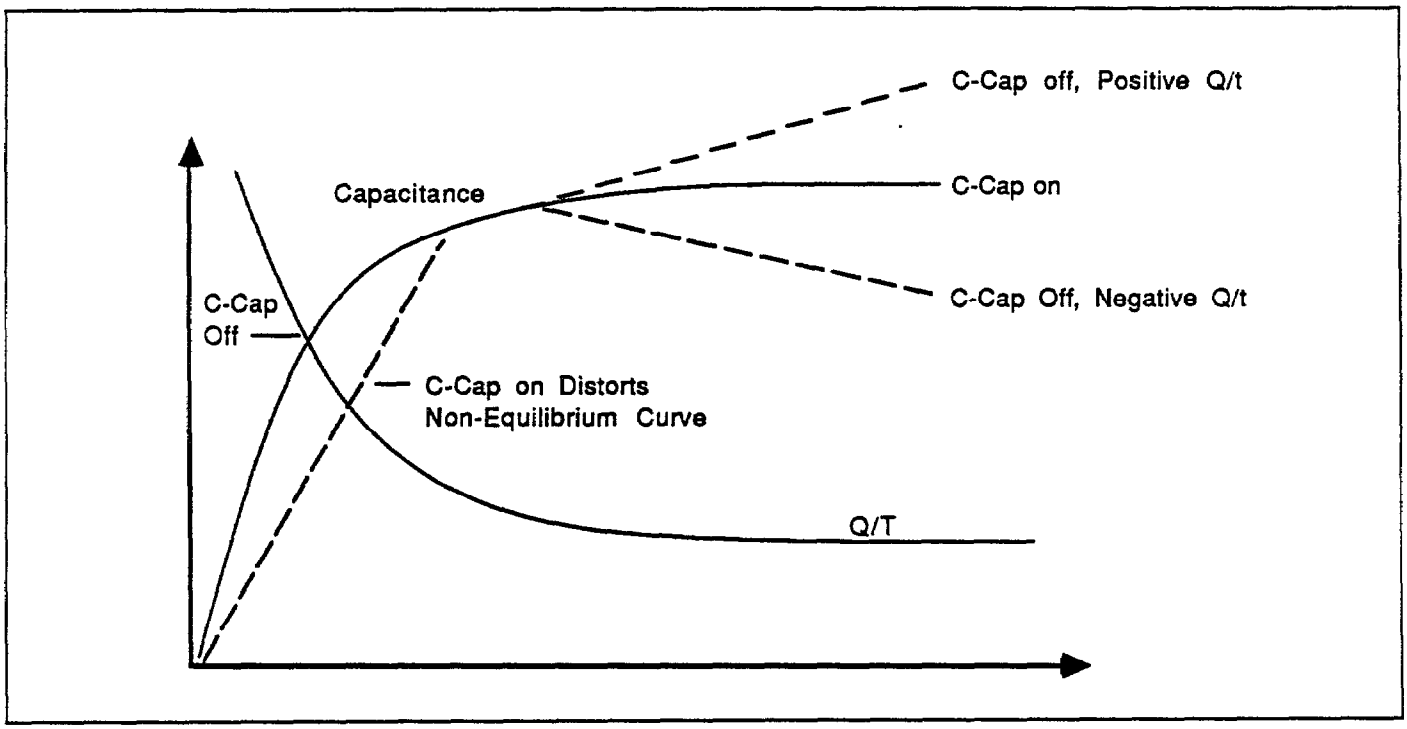


Figure 3-21. Capacitance and Leakage Current Using Corrected Capacitance

3.7 MAKING CV MEASUREMENTS

The following paragraphs describe procedures for making CV sweeps both manually, and automatically. During a sweep, the following parameters are stored within an array for later analysis:

1. C_Q (quasistatic capacitance). C_Q is measured by the Model 595.
2. Q/t (current), as measured by the Model 595.
3. C_H (high-frequency capacitance). High-frequency capacitance is measured at 100kHz or 1MHz (depending on the selected test frequency) by the Model 590.
4. G (high-frequency conductance). The Model 590 measures the conductance of the device at 100kHz or 1MHz, depending on the selected test frequency.

NOTE
When using series model, resistance will be stored and displayed instead of conductance.

5. V_{GS} (gate voltage). The gate voltage is measured by the Model 590. Note that the gate voltage as it is used by the computer is opposite in polarity from that displayed on the front panel of the Model 590 because of the gate-to-substrate voltage convention used (gate terminal connected to INPUT; substrate terminal connected to OUTPUT).

3.7.1 CV Measurement Menu

Figure 3-22 shows the menu for CV measurements. Various options on this menu allow you to program menu parameters, manually start a CV sweep, automatically initiate the sweep, and access the analysis functions. These options are discussed below.

3.7.2 Programming Measurement Parameters

Menu Selections

By selecting option 1 on the CV measurement menu, you can access the parameter selection menu shown in Figure 3-23. (Parameters can also be set from the sweep menu by pressing "M".) This menu allows you to program the following parameters:

1. Range for both quasistatic and high-frequency measurements (200pF or 2nF). The measurement ranges of both the Models 590 and 595 are set by this parameter.
2. Frequency for high-frequency measurements (100kHz or 1MHz). This parameter sets the operating frequency of the Models 590 and 5951.
3. Model (parallel or series). Model selects whether the device is modeled as a parallel capacitance and conductance, or a series capacitance and resistance. Model affects only high-frequency capacitance and conductance measurements. See the Model 590 Instruction Manual for more details on using parallel or series model.
4. Start V: ($-120 \leq V \leq 120$). Start V is the initial bias voltage setting of a CV sweep.
5. Stop V: ($-120 \leq V \leq 120$). Stop V is the final bias voltage setting of a CV sweep.
6. Bias V: Bias V is a static DC level applied to the device during certain static monitoring functions such as leakage level tests and determining device C_{ox} and delay time. Note that the voltage source value returns to the Bias V level after Stop V at the end of the sweep.
7. T delay: ($0.07 \leq T \leq 199.99$sec). Note that the time delay must be properly programmed to maintain device equilibrium during a sweep, as discussed in paragraph 3.6.
8. Step V: (10mV, 20mV, 50mV, or 100mV): Step V is the incremental change of voltage of the bias staircase waveform. The polarity of Step V is automatically set depending on the relative values of Start V and Stop V. If Stop V is more positive than Start V, Step V is positive; if Stop V is more negative than Start V, Step V is negative.
9. C-Cap: (Corrected capacitance). Uses the corrected capacitance program of the Model 595 when enabled. C-Cap should be used only when testing leaky devices. As discussed in paragraph 3.6, C-cap should be used for device measurement if you found it necessary to use C-cap when determining delay time.
10. Filter: Sets the Model 595 to Filter 2 when on, Filter 0 (off) when off.

NOTE
The filter may distort the quasistatic CV curve if there are less than 50 readings in the depletion region of the curve. Turning off the filter will increase reading noise by 2.5 times. See the Model 595 Instruction Manual for complete filter details.

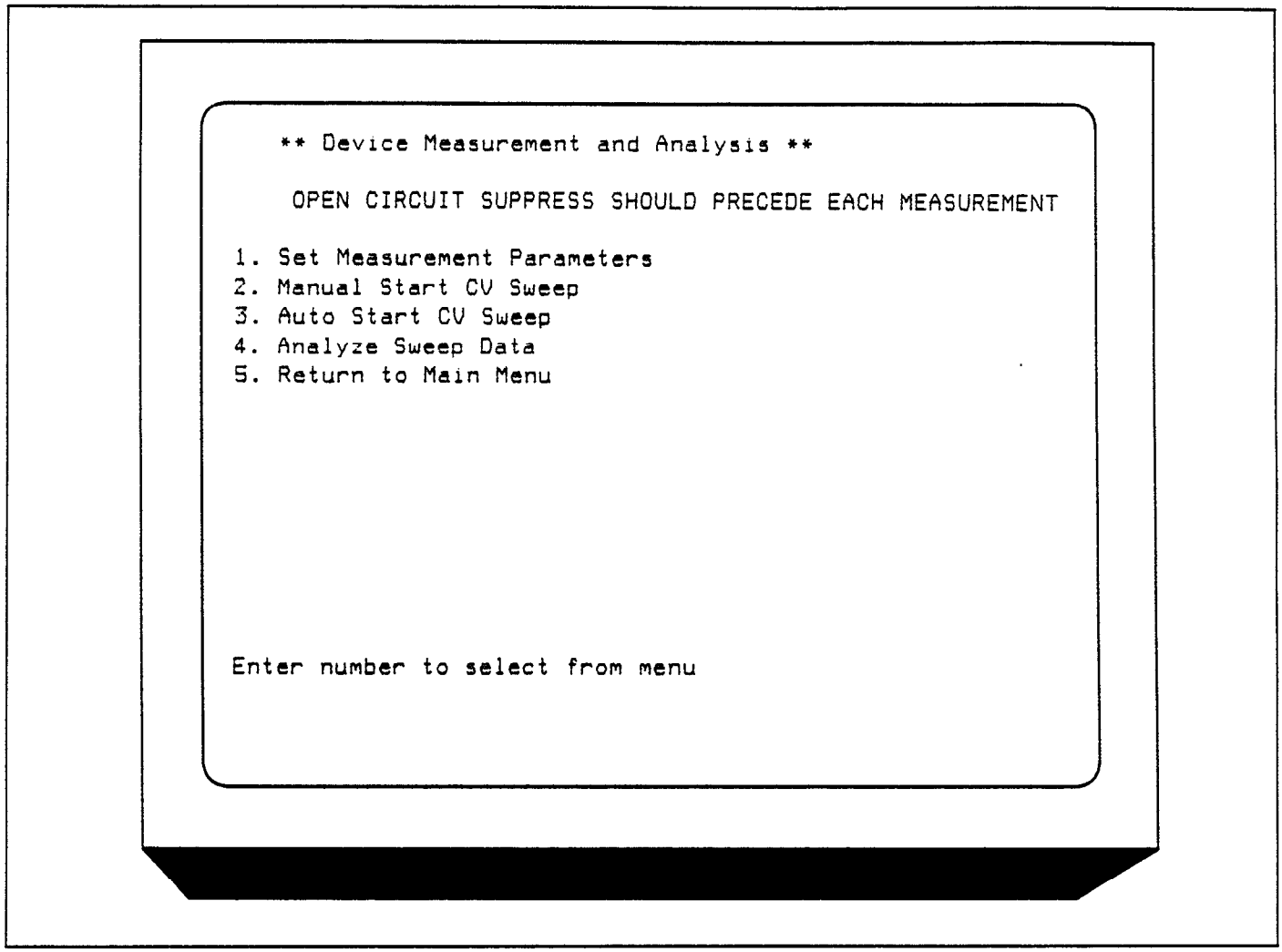


Figure 3-22. Device Measurement Menu

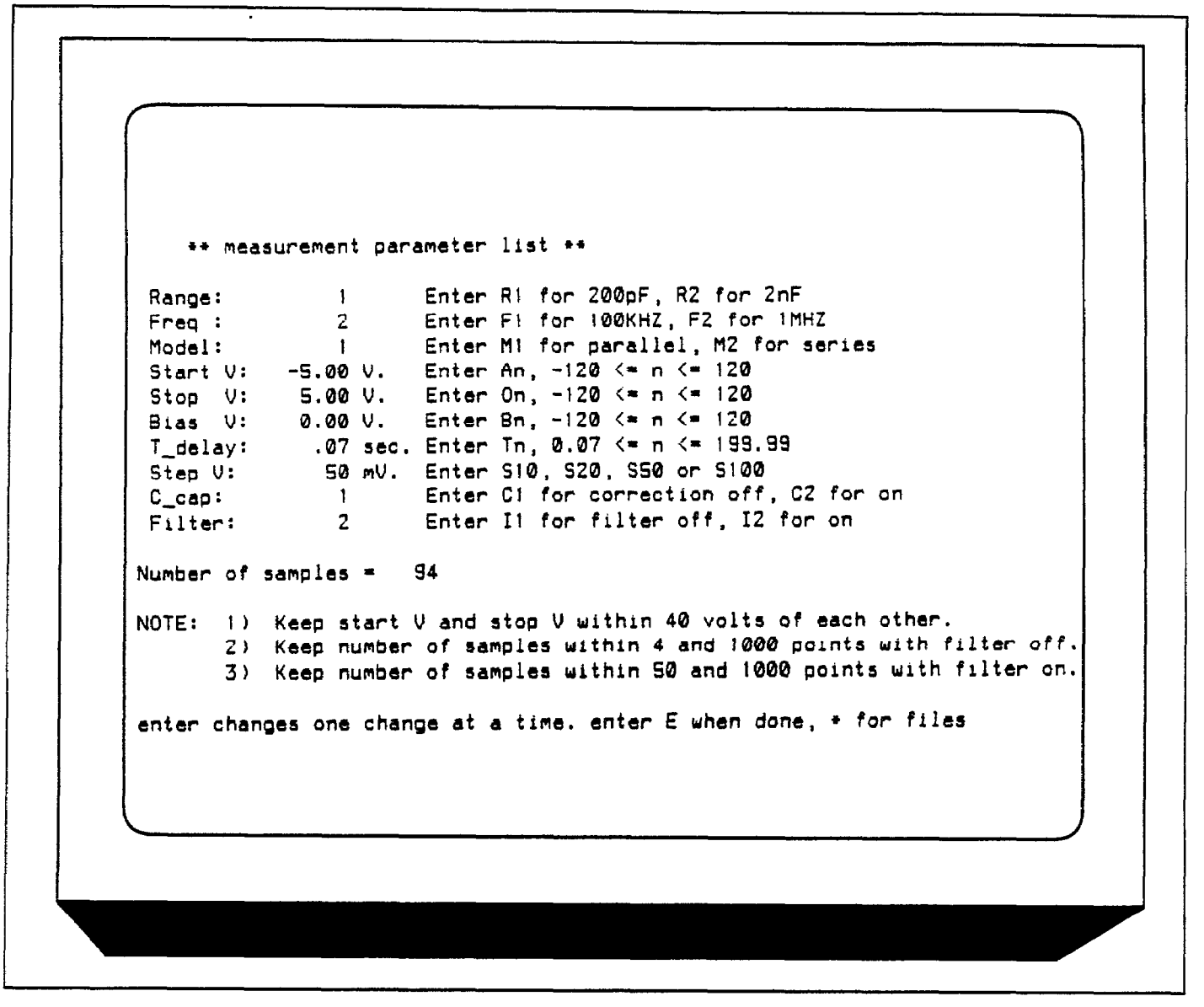


Figure 3-23. Parameter Selection Menu

Determining the Number of Readings in a Sweep

The number of readings (bias steps) in a given sweep is determined by Start V, Stop V, and Step V, as well as whether or not the filter is enabled. The number of readings is determined as follows:

$$R = INT\ [(ABS(V_{STOP} - V_{START}) / 2V_{STEP}) - F\ ]$$

Where: R = number of readings in the sweep
INT = take the integer of the expression
ABS = take the absolute value of the expression
V_{STOP} = programmed stop voltage
V_{START} = programmed start voltage
V_{STEP} = programmed step voltage
F = 2 if the filter is off
F = 6 if the filter is on

Example: Assume that Start V and Stop V are +10V and −10V respectively, and that Step V is 100mV. With the filter on, the number of readings is:

$$R = INT((ABS(-10-(10))/.2)-6$$
$$R = 94$$

Programming Parameters

To program a parameter, type in the indicated menu letter followed by the pertinent parameter. The examples below will help to demonstrate this process.

Example 1: Select 1MHz High-frequency Operation

To select high frequency operation, simply type in F2 at the command prompt and press the ENTER key.

Example 2: Program a +15V Bias V

Type in B15 and press the ENTER key.

Example 3: Select 0.1sec Delay Time

Type in T0.1 and press the ENTER key.

Example 4: Program a 20mV Step Voltage

Type in S20 and press the ENTER key.

Programming Considerations

When selecting parameters, there are a few points to keep in mind, including:

1. The maximum difference between the programmed Start V and Stop V is 40V. Exceeding this value will generate an error message.
2. Voltage source polarity is specified at the gate with respect to the substrate. For example, with a positive voltage, the gate will be biased positive relative to the substrate. Thus, an n-type material must be biased positive to be in the accumulation region.
3. Time delay must be carefully chosen so that the device remains in equilibrium throughout the sweep. The procedure to determine optimum delay time is covered in paragraph 3.6. Failure to properly program proper delay time will distort quasistatic and high-frequency CV curves. See paragraph 3.9 for additional measurement considerations.
4. The filter should be used only when more than 50 readings in the fundamental change area of the curve are taken; see the Model 595 Instruction Manual, paragraph 3.12 for more information. Note that the parameter menu includes a note to remind you of the 50-reading limitation because you will not be able to exit the parameter menu with the filter on and <50 points.

Saving/Recalling Parameters

By pressing the "*" key, you can save or load parameters to or from diskette. Press "S" (save) or "L" (load) to carry out the desired operation. You will then be prompted to type in the filename to be saved or loaded. An error message will be given if a file cannot be found or will be overwritten.

When the save option is selected, the parameter values currently in effect will be saved under the selected filename. Parameters loaded from an existing file will be updated to conform to the new values.

Returning to Previous Menu

After all parameters have been programmed (or loaded from disk), press "E" to return to the previous menu.

3.7.3 Manual CV Sweep

Description

A manual CV sweep requires that you observe device

leakage, and then manually trigger the sweep. When sweeping from inversion to accumulation, you must wait for the device to attain equilibrium. An optional light can be controlled to speed up the equilibrium process.

Procedure

1. Select the Manual Start CV Sweep option. The computer will display the options in Figure 3-24.
2. Verify a zero probes-up capacitance, and suppress if necessary (press "Z").
3. Press "M" and program the following parameters.

   Range: As required for the expected capacitance.
   Frequency: 100kHz or 1MHz as required.
   Model: Parallel or series as required.
   Start V: Accumulation or inversion voltage, as determined in paragraph 3.6.
   Stop V: Inversion or accumulation voltage, as determined in paragraph 3.6.
   T Delay: As required to maintain equilibrium (See paragraph 3.6)
   Step V: Same as used when testing device in paragraph 3.6.
   C-Cap: Off except for leaky devices (see paragraph 3.6).
   Filter: On
4. If sweeping from accumulation to inversion, monitor the current until it reaches the system leakage level, as discussed in paragraph 3.4. When the current reaches the system leakage level, press "S" to trigger the sweep.
5. If sweeping from inversion to accumulation, wait until the device reaches equilibrium (equilibrium occurs when Q/t decays to the system leakage level). If a light is connected to the system, press "L" to turn on the light to speed up equilibrium. Turn off the light once equilibrium is reached prior to initiating the sweep (it may take a few moments for the device to settle after turning off the light). Press "S" to initiate the sweep.
6. The computer will then display a message that the sweep is in progress. During the sweep, you can press any key to abort, if desired.
7. Following the sweep, press ENTER to return to the previous menu.
8. Select option 4 to view and analyze the data. Refer to Section 4 for complete details on data analysis. Note that C_{ox}, area, and N_{BULK} values, as previously used in analysis may not apply to this measurement, and may require changing before analysis.

3.7.4 Auto CV Sweep

Description

The auto sweep procedure is similar to that used for manual sweep, except that you can program the current trip point at which the sweep will automatically begin. Otherwise, the procedure is essentially the same, as outlined below.

Procedure

1. Select Auto Start CV Sweep. The computer will display the options in Figure 3-25.
2. Verify a zero probes-up capacitance and suppress if necessary, (press "Z").
3. Press "M" and program the following parameters.

   Range: As required for the expected capacitance.
   Frequency: 100kHz or 1MHz as required.
   Model: Parallel or series as required.
   Start V: Accumulation or inversion voltage, as determined in paragraph 3.6.
   Stop V: Inversion or accumulation voltage, as determined in paragraph 3.6.
   T Delay : As required to maintain equilibrium (See paragraph 3.6)
   Step V: Same as used when testing device in paragraph 3.6.
   C-Cap: Off except for leaky devices.
   Filter: On
4. Press "G" and the type in the desired leakage trip point when prompted to do so. Typically, this value will equal the system leakage level, as determined in paragraph 3.4.
5. Press "T" to select above or below trip threshold.
6. If sweeping from inversion to accumulation, you can turn on the light (if so equipped) to speed up equilibrium by pressing "L". Be sure to turn off the light once equilibium is reached before initiating the sweep (it may take a few moments for the device to settle after turning off the light).
7. Press "A" to arm the sweep. The computer will continue to monitor readings while waiting for the trip point.
8. Once the leakage current reaches the trip point, the sweep will be initiated. During the sweep, you can press any key to abort the process.
9. Once the sweep is completed, press the ENTER key to return to the previous menu.
10. Select option 4, Analyze CV Data, to view or graph the data. Section 4 covers analysis in detail.

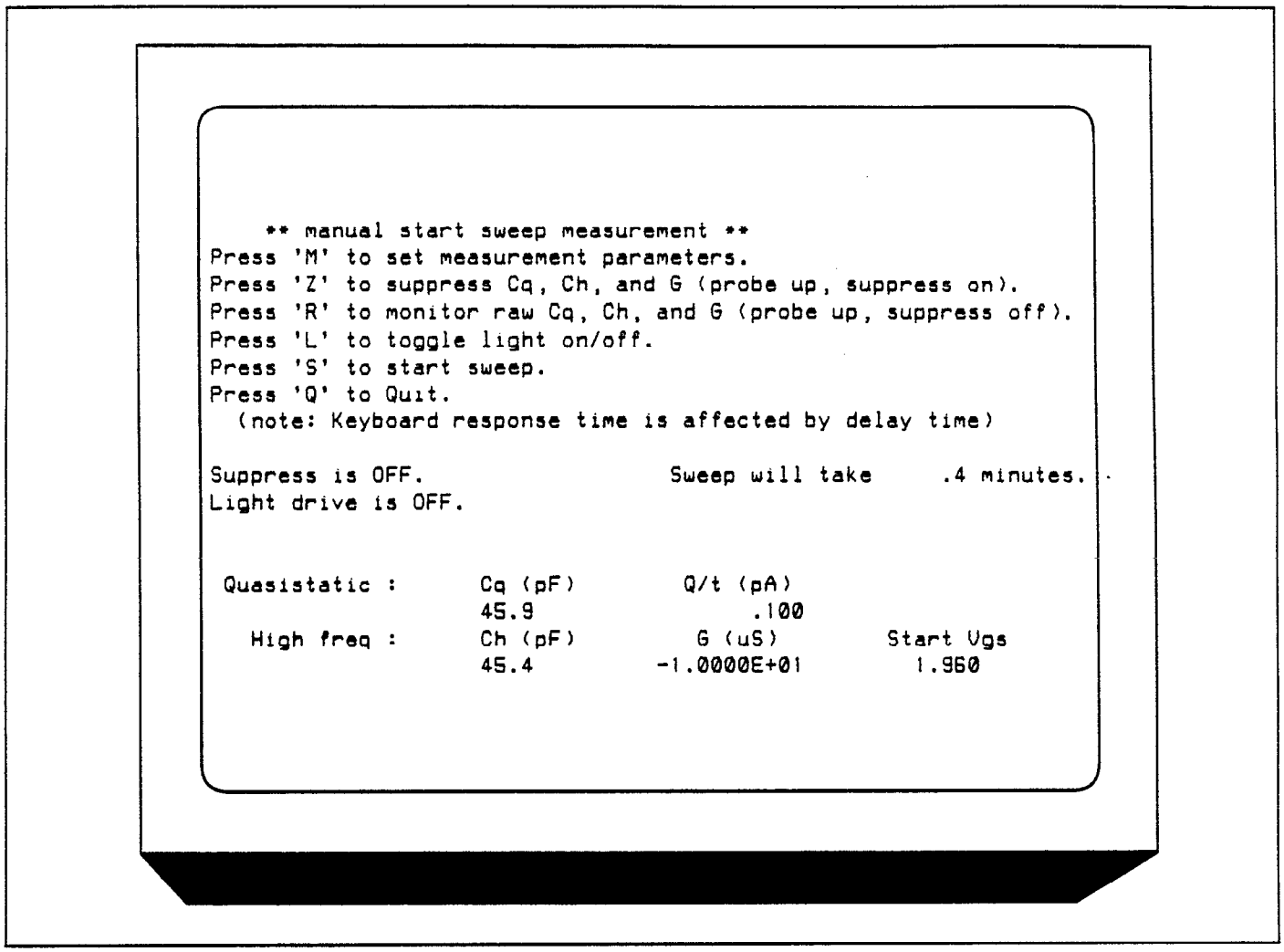


Figure 3-24. Manual Sweep Menu

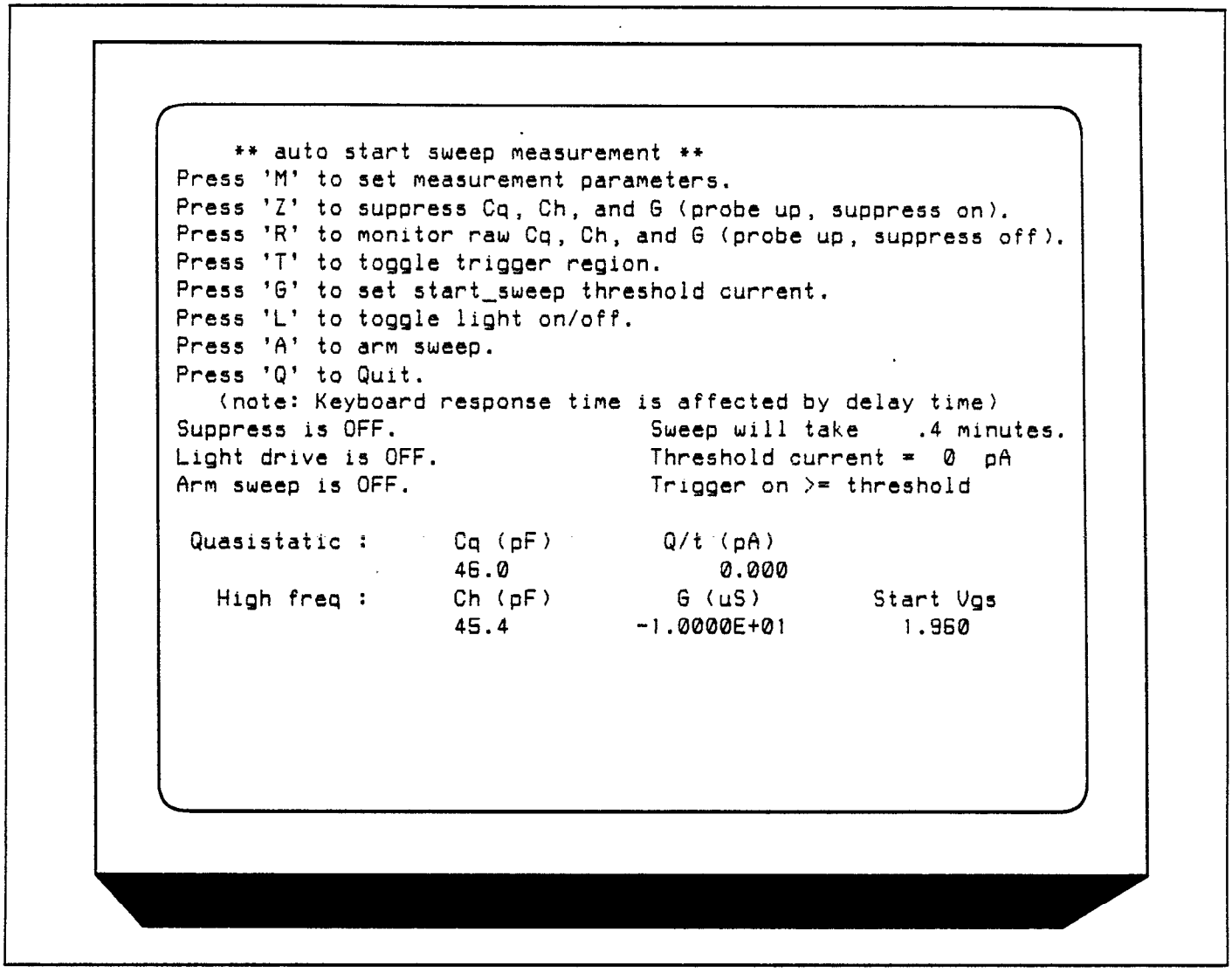


Figure 3-25. Auto Sweep Menu

3.7.5 Using Corrected Capacitance

When making quasistatic measurements on leaky devices, it is recommended that you use the corrected capacitance function to compensate for leakage. Otherwise, the resulting quasistatic CV curves will be tilted because of the leakage resistance of the device or test system. When using corrected capacitance, it is very important that the device remain in equilibrium throughout the sweep. Data taken in nonequilibrium with corrected capacitance enabled should be considered to be invalid, and the resulting curve will be distorted in the nonequilibrium region of the curve.

NOTE

If you found is was necessary to use corrected capacitance when determining delay time (paragraph 3.6), it is recommended that you also use corrected capacitance when measuring the device.

3.8 LIGHT CONNECTIONS

A user-supplied light can be connected to the system in order to help attain device equilibrium in inversion more rapidly. This light is controlled through appropriate terminals on the DIGITAL I/O port of the Model 5951 Remote Input Coupler. The following paragraphs discuss DIGITAL I/O port terminal assignments along with typical light connections.

3.8.1 Digital I/O Port Terminals

Table 3-2 summarizes the terminal assignments for the DIGITAL I/O port of the Model 5951. Figure 3-26 shows the pinouts for the supplied mating connector. Terminals include:

+5V Digital (pins 1 and 2): +5V digital is supplied through an internal 33Ω resistor for short-circuit protection. Current draw should be limited to 20mA to avoid supply loading.

Digital Inputs (pins 3-6): These terminals pass through the digital inputs to the Model 230-1. One possible use for these inputs would be to monitor a test fixture closure status switch. Note that the Package 82 software does not presently support reading the input terminals, but it could be modified to do so, if desired. The status of these inputs can be read with the U1 command, as described in the Model 230 Programming Manual.

OUTPUT: OUTPUT is intended for controlling an external light source. Logic convention is such that OUTPUT is LO when the software indicates that the light is ON. Note that OUTPUT is LS-TTL compatible with a guaranteed 8mA current sink capability.

Digital Common: Provides a common connection for external circuits.

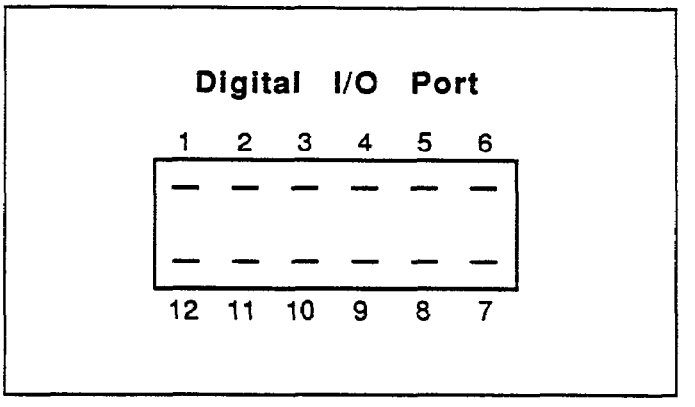


Figure 3-26. Digital I/O Port Terminal Arrangement

Table 3-2. Digital I/O Port Terminal Assignments

Terminal	Description
1	+5V Digital*
2	+5V Digital*
3	Digital Input 1**
4	Digital Input 2**
5	Digital Input 3**
6	Digital Input 4**
7	NC
8	NC
9	NC
10	Output†
11	Digital Common
12	Digital Common

*+5V sourced through internal 33Ω resistor.
**Digital inputs passed through to Model 230-1
†Output controls lights HI = OFF; LO = ON

3.8.2 LED Connections

The digital output has sufficient drive capability to directly drive LEDs up to 8mA using the connecting method shown in Figure 3-27. The anode of the LED should be connected to +5V, and the cathode should be connected to OUTPUT through a 330Ω current-limiting resistor. Use of LEDs that draw more than 8mA is not recommended.

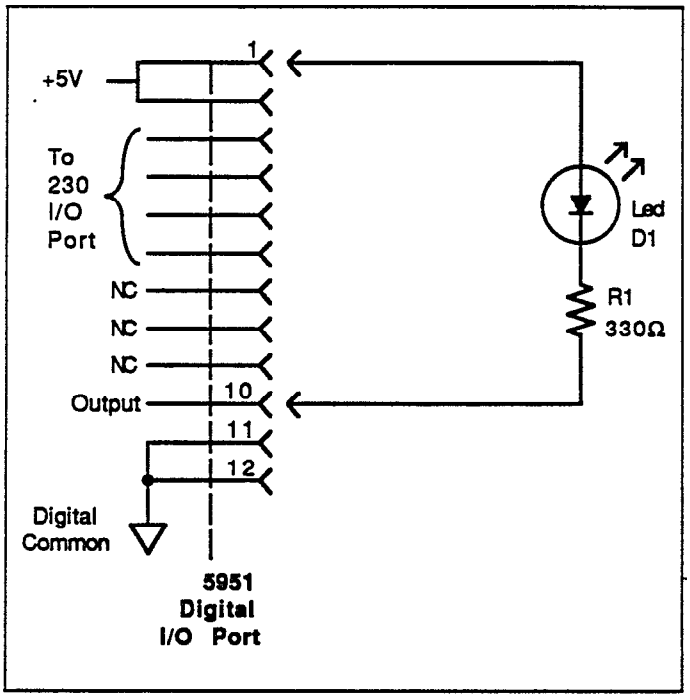


Figure 3-27. Direct LED Control

3.8.3 Relay Control

For larger LEDs, or for small incandescent lamps, an external relay control circuit can be used to switch the larger current. Figure 3-28 shows a typical circuit. With the configuration shown, a normally-closed relay contact will be necessary to ensure the light is on at the proper time. Note that an external power supply will be necessary to drive the external circuitry. The value of the base resistor will depend on the current gain of the transistor as well as the power supply voltage and relay coil resistance. For example, with a supply voltage of 5V, a coil resistance of 500Ω, and a current gain of 100, a base resistor value of 10kΩ should be adequate to drive the transistor into saturation.

Note that the diode across the relay coil should be included to protect the transistor from Ldi/dt voltages when the relay is de-energized.

3.9 MEASUREMENT CONSIDERATIONS

The importance of making careful CV curve measurements is often underestimated. However, errors in the CV data will propogate through calculations, resulting in errors in device parameters derived from the curves. These errors can be amplified during calculations by a factor of 10 or more.

With careful attention, the effects of many common error sources can be minimized. In the following paragraphs, we will discuss some common error sources and provide suggested methods for avoiding them.

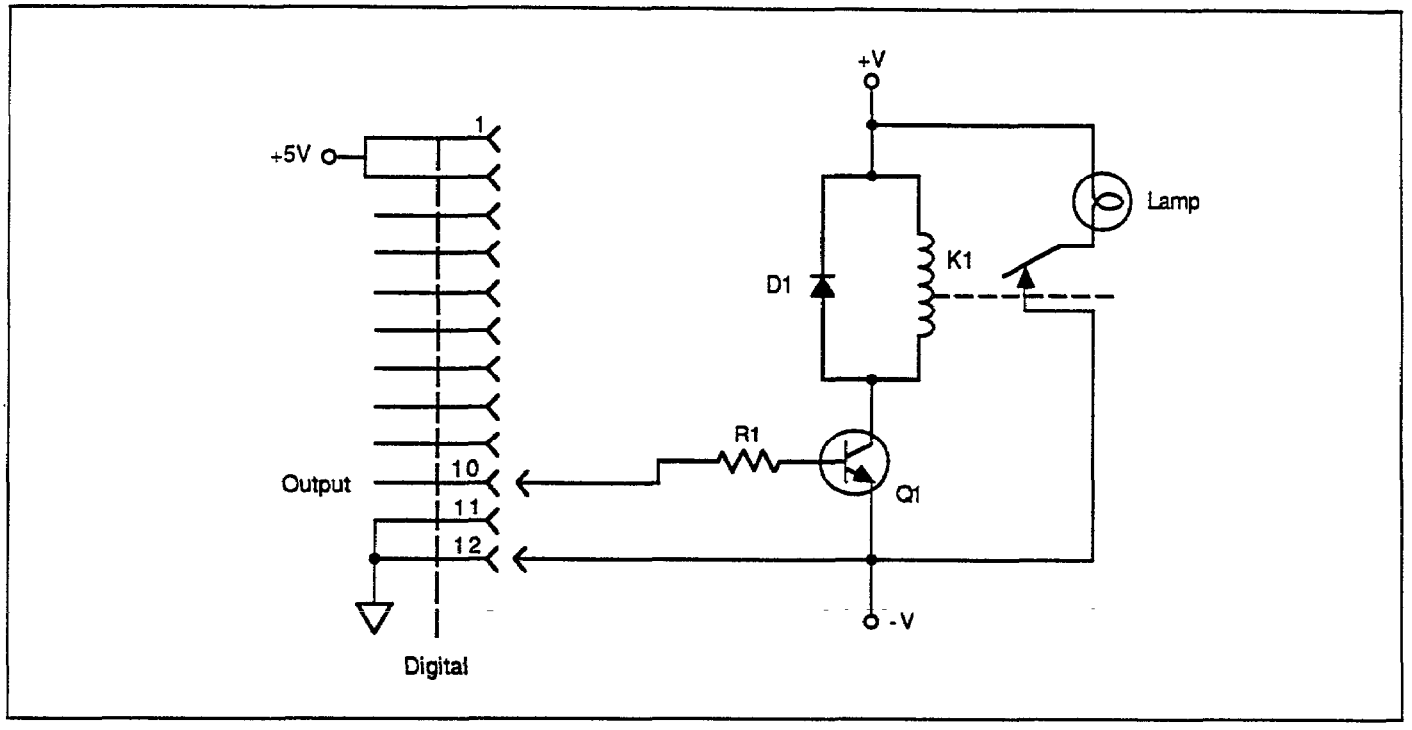


Figure 3-28. Relay Light Control

3.9.1 Potential Error Sources

Theoretically, a capacitance measurement using one of the common techniques would require only that two leads be used to connect the measuring instrument to the device under test (DUT)—the input and output. In practice, however, various parasitic or stray components complicate the measuring circuit.

Stray Capacitances

Regardless of the measurement frequency, stray capacitances present in the circuit are important to consider. Stray capacitances can cause offsets when they are in parallel with the device, can act as a shunt load on the input or output, or can cause coupling between the device and nearby AC signal sources.

When stray capacitance is in parallel with with the DUT, it causes a capacitance offset, adding to the capacitance of the device under test (C_{DUT}), as shown in Figure 3-29. Shunt capacitance, on the other hand, often increases the noise gain of the intrumentation amplifiers, increasing capacitance reading noise (Figure 3-30). Shunt capacitance also forms a capacitive divider with C_{DUT}, steering current away from the input to ground. This phenomenon results in capacitance gain error, with the CV curve results shown in Figure 3-31.

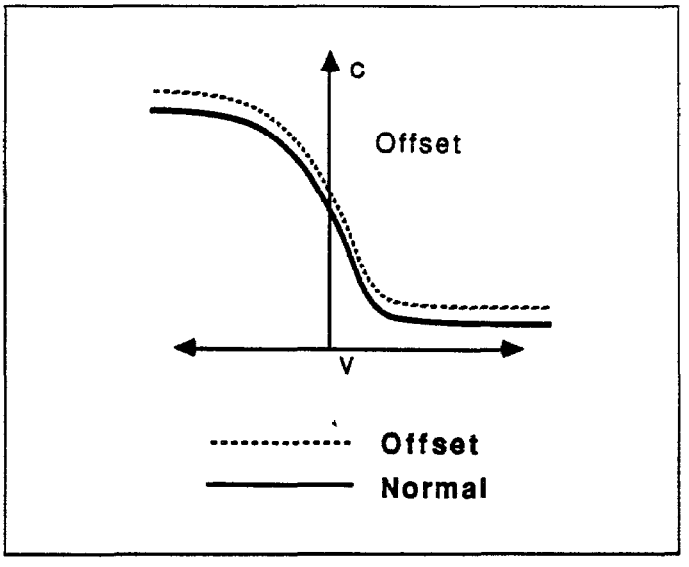


Figure 3-29. CV Curve with Capacitance Offset

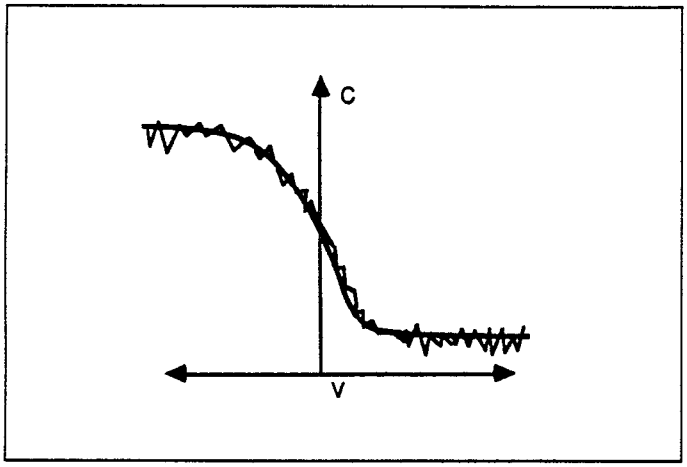


Figure 3-30. CV Curve with Added Noise

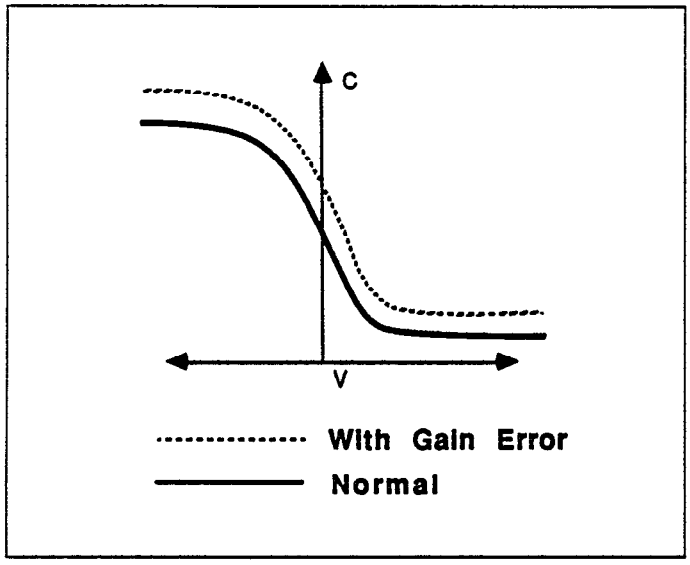


Figure 3-31. CV Curve Resulting from Gain Error

Stray capacitance may also couple current or charge from nearby AC signal sources into the input of the measuring instrument. This noise current adds to the device current and results in noisy, drifty, or unrepeatable measurements. For quasistatic measurements, power line frequency and electrostatic coupling are particularly troublesome, while digital and RF signals are the primary cause of noise induced in high-frequency measurements.

Leakage Resistances

Under quasistatic measurement conditions, the impedance of C_{DUT} is almost as large as the insulation resistances in the rest of the measurement circuit. Consequently, even leakage resistances of $10^{12}\Omega$ or more can contribute significant errors if not taken into consideration.

Resistance across the DUT will conduct an error current in addition to the device current. Since this resistive current is directly proportional to the applied bias voltage, and the capacitor current is not, the result is a capacitance offset that is proportional to the applied voltage. The end result shows up as a "tilt" in the quasistatic CV curve, as shown in Figure 3-32.

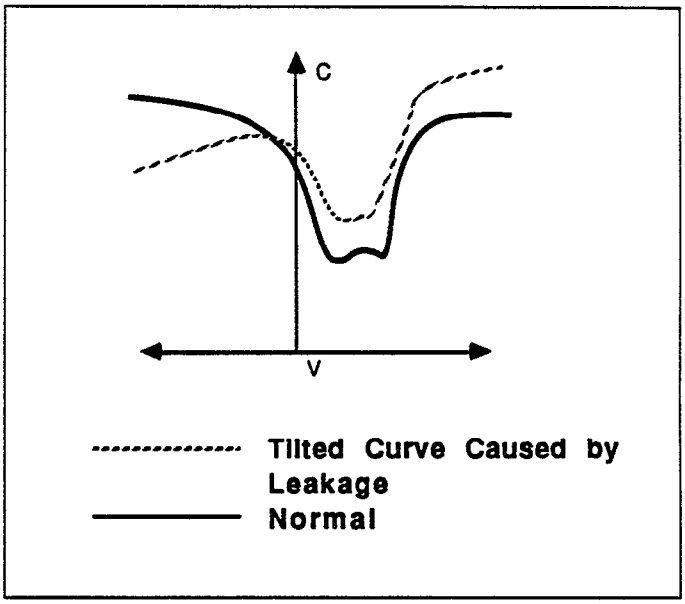


Figure 3-32. Curve Tilt Caused By Voltage-dependent Leakage

Stray resistance to nearby fixed voltage sources results in a constant (rather than a bias voltage-dependent) leakage current. Other sources of constant leakage currents include instrument input bias currents, and electrochemical currents caused by device or fixture contamination. Such constant leakage currents cause a voltage-independent capacitance offset.

Keep in mind that insulation resistance and leakage current are aggravated by high humidity as well as by contaminants. In order to minimize these effects, always keep devices and test fixtures in clean, dry conditions.

High-Frequency Effects

At measurement frequencies of approximately 100kHz and higher, the impedance of C_{DUT} may be so small than any series impedance in the rest of the circuit may cause errors. Whether such series impedance is caused by inductance (such as from leads or probes), or from resistance (as with a high-resistivity substrate), this series impedance causes non-linearity in the measured capacitance. The resulting CV curve is, of course, affected by such non-linearity, as shown in Figure 3-33.

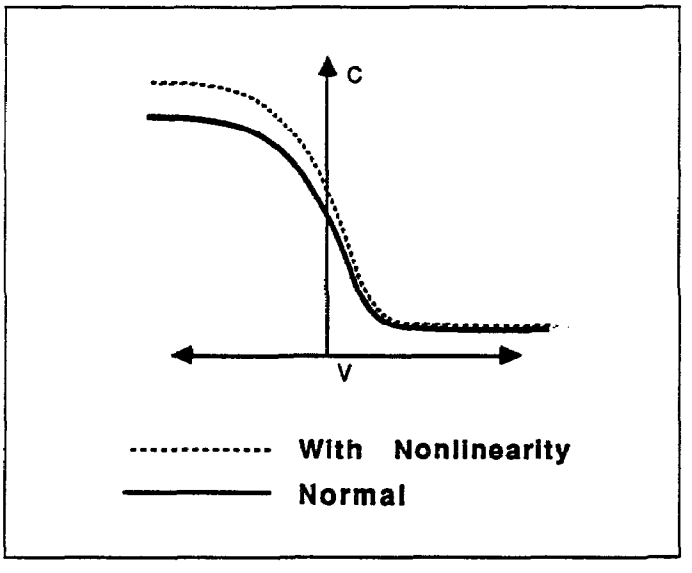


Figure 3-33. CV Curve Caused By Nonlinearity

Another high-frequency effect is caused by the AC network formed by the instrumentation, cables, switching circuits, and the test fixtures. Referred to as transmission line error sources, the network essentially transforms the impedance of C_{DUT} when it is referred to the input of the instrument, altering the measured value. Transmission line effects alter the gain and produce non-linearities.

3.9.2 Avoiding Capacitance Errors

The many possible error sources that can affect CV measurements may seem like a great deal to handle. However, careful attention to a few key details will reduce errors to an acceptable level. Once most of the error sources have been minimized, any residual errors can be further reduced by using the probes-up suppression and corrected capacitance features of the Package 82 software.

Key details that require attention include use of proper cabling and effective shielding. These important aspects are discussed below.

Cabling Considerations

Cables must be used to connect the instruments to the device under test. Ideally, these cables should supply the test voltage to the device unaltered in any way. The test voltage is converted into a current or charge in the DUT, and should be carried back to the instruments undisturbed. Along the way, potential error sources must be minimized.

Coaxial cable is usually used in order to eliminate stray capacitance between the measurement leads. The cable shield is connected to a low-impedance point (guard) that follows the meter input. This technique, known as a three-terminal capacitance measurement, is almost universally used in commercial instrumentation. The shield shunts current away from the input to the guard.

Coaxial cables also serve as smooth transmission lines to carry high-frequency signals without attenuation. For this reason, the cable's characteristic impedance should closely match that of the instrument input and output, which is usually 50Ω. Standard RG-58 cable is adequate for frequencies in the range of 1kHz to more than 10MHz. High-quality BNC connectors with gold-plated center conductors reduce errors from high series contact resistance.

Quasistatic CV measurements are susceptible to shunt resistance and leakage currents as well as to stray capacitances. Although coaxial cables are still appropriate for these measurements, the cables should be checked to ensure that the insulation resistance is sufficiently high ($>10^{12}\Omega$). Also, when such cables are flexed, the shield rubs against the insulation, generating small currents due to triboelectric effects. These currents can be minimized by using low-noise cable (such as the Model 4801) that is lubricated with graphite to reduce friction and to dissipate generated charges.

Flex-producing vibration should be eliminated at the source whenever possible. If vibration cannot be entirely eliminated, cables should be securely fastened to prevent flexing.

Once final point regarding cable precautions is in order: Cables can only degrade the measurement, not improve it. Thus, cable lengths should be minimized where possible, without straining cables or connections.

Device Connections

Care in properly protecting the signal path should not stop at the cable ends where the connection is made to the DUT fixture. In fact, the device connection is an extremely important aspect of the measurement. For the same reasons given for coaxial cables, it is best to continue the coaxial path as close to the DUT as possible by using coaxial probes. Also, it is important to minimize stray capacitance and maximize insulation resistance in the pathway from the end of the coaxial cable to the DUT.

Most devices have one terminal that is well insulated from other conductors, as in the gate of an MOS test dot. The input should be connected to the gate because it is more susceptible to stray signals than is the output. The output can better tolerate being connected to a terminal with high shunt capacitance, noise, or poor insulation resistance, although these characteristics should still be optimized for best results.

Test Fixture Shielding

At the point where the coaxial cable shielding ends, the sensitive input node is exposed, inviting error sources to interfere. Proper device shielding need not end with the cables or probes, however, if a shielded test fixture is used.

A shielded fixture, sometimes known as a Faraday cage, consists of a metal enclosure that completely surrounds the DUT and leads. In order to be effective, the shield must be electrically connected to the coaxial shield. Typically, bulkhead connectors are mounted to the side of the cage to bring in the signals. Coaxial cables should be continued inside, if possible, or individual input and output leads should be widely spaced in order to maintain input/output isolation.

3.9.3 Correcting Residual Errors

Controlling errors at the source is the best way to optimize CV measurements, but doing so is not always possible. Remaining residual errors include offset, gain, noise, and voltage-dependent errors. Ways to deal with these error sources are discussed in the following paragraphs.

Offsets

Offset capacitance and conductance caused by the test apparatus can be eliminated by performing a suppression with the probes in the up position. These offsets will then be nulled out when the measurement is made. Whenever the system configuration is changed, the suppression procedure should be repeated. In fact, for maximum accuracy, it is recommended that you perform a probes-up suppression or at least verify prior to every measurement.

Gain and Nonlinearity Errors

Gain errors are difficult to quantify. For that reason, gain correction is applied to every Package 82 measurement. Gain constants are determined by measuring accurate calibration sources during the cable correction process.

Nonlinearity is normally more difficult to correct for than are gain or offsets errors. The cable correction process that is part of the Package 82, however, provides nonlinearity compensation for high-frequency measurements, even for nonideal configurations such as switching matrices.

Voltage-Dependent Offset

Voltage-dependent offset (curve tilt) is the most difficult to correct error associated with quasistatic CV measurements. It can be eliminated by using the corrected capacitance function of the Package 82 software. In this technique, the current flowing in the device is measured as the capacitance value is measured. The current is known as Q/t because its value is derived from the slope of the charge integrator waveform. Q/t is used to correct capacitance readings for offsets caused by shunt resistance and leakage currents.

Care must be taken when using the corrected capacitance feature, however. When the device is in nonequilibrium, device current adds to any leakage current, with the result that the curve is distorted in the nonequilibrium region. The solution is to keep the device in equilibrium throughout the sweep by carefully choosing the delay time.

Curve Misalignment

At times, quasistatic and high frequency curves may be slightly misaligned due to gain errors or external factors. In such cases, curve gain and offset factors can be applied to the curves to properly align them. This feature is available under the analysis menu.

Noise

Residual noise on the CV curve can be minimized by using filtering when taking your data. Care must be taken, however, not to apply too much filtering, as doing do will distort the curve. Often, some experimentation may be necessary to optimize noise reduction and at the same time keep undesirable effects to a minimum. A good rule of thumb is to use the filter only when there are more than 50 points taken over the fundamental change in the data curve. The filter is selectable in the parameter menu.

Maintaining Equilibrium

The condition of the device when all internal capacitances are fully charged is referred to as equilibrium. Most quasistatic and high-frequency CV curve analysis is based on the simplifying assumption that the device is measured in equilibrium. Internal RC time constants limit the rate at which the device bias may be swept while maintaining equilibrium. They also determine the hold time required for device settling after setting the bias voltage to a new value before measuring C_{DUT}.

3.9.4 Interpreting CV Curves

Even when all the precautions outlined here are followed, there are still some possible obstacles to successfully using CV curves to analyze semiconductor devices. Semiconductor capacitors are far from ideal, so care must be taken to understand how the device operates. Also, the curves must be generated under well-controlled test conditions that ensure repeatable, analyzable results.

The two main parameters to be controlled, then, are the bias sweep rate and the hold time. When these parameters are set properly, the normal CV curves shown in Figure 3-34 result. Once the proper sweep rate and hold time have been determined, it is important that all curves compared with one another be measured under the same test conditions; otherwise, it may be the parameters, not the devices themselves, that cause the compared curves to differ.

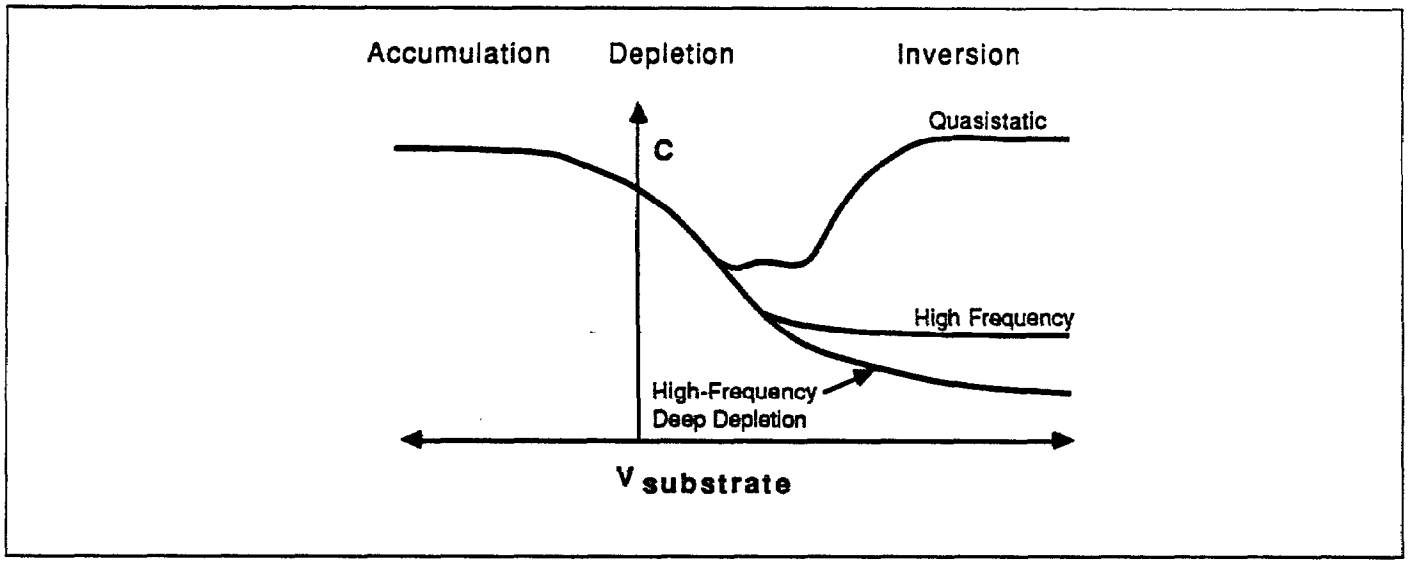


Figure 3-34. Normal CV Curve Results when Device is Kept in Equilibrium

Analyzing Curves for Equilibrium

There are three primary indicators that can be used to determine whether a device has remained in equilibrium during testing. First, as long as a device is in equilibrium, C_{DUT} is settled at all points in the sweep. As a result, it makes no difference whether the sweep goes from accumulation to inversion, or from inversion to accumulation, nor does it matter how rapidly the sweep is performed. Therefore, curves made in both directions will be the same, exhibiting no hysteresis, and any curve made at a slower rate will be the same. Figure 3-35 shows the type of hysteresis that will occur if the sweep rate is too fast, and the device does not remain in equilibrium.

The second equilibrium yardstick requires that the DC current through the device be essentially zero at each measurement point after device settling. This test can be performed by monitoring Q/t . Thirdly, the curves should exhibit the smooth equilibrium shape. Deviations from the ideal smooth shape indicate a nonequilibrium condition, as in the examples resulting from too short a hold time shown in Figure 3-36. Note that at least two of these indicators should be used together, if possible, because any of the three used alone can be misleading at times.

One final quick test to confirm equilibrium is to observe C_Q during a hold time at the end of the CV sweep from accumulation to inversion. During this final hold time, the capacitance should remain constant. If a curve has been swept too quickly, the capacitance will rise slightly during the final hold time.

Initial Equilibrium

Biasing the device to the starting voltage in the inversion region at the beginning of a CV measurement creates a nonequilibrium condition that must be allowed to subside before the CV sweep begins. This recovery to equilibrium can take seconds, minutes, or even tens of minutes to achieve. For that reason, it is generally advantageous to begin the sweep in the accumulation region of the curve whenever possible.

Still, it is often necessary to begin the sweep in the inversion region to check for curve hysteresis. In this case, a light pulse, shone on the device, can be used to quickly generate the minority carriers required by the forming inversion layer, thus speeding up equilibrium and shortening the hold time.

The best way to ensure equilibrium is initially achieved is to monitor the DC current in the device and wait for it to decay to the DC leakage level of the system. A second indication that equilibrium is reached is that the capacitance level at the initial bias voltage decays to its equilibrium level.

3.9.5 Dynamic Range Considerations

The dynamic range of a suppressed quasistatic or high-frequency measurement will be reduced by the amount suppressed. For example, if, on the 200pF range, you were to suppress a value of 10pF, the dynamic range would be reduced by that amount. Under these conditions, the maximum value the instrument could measure without overflowing would be 190pF.

A similar situation exists when using cable correction with the Model 590. For example, the maximum measurable value on the 2nF range may be reduced to 1.8nF when using cable correction. The degree of reduction will depend on the amount of correction necessary for the particular test setup.

The dynamic range of quasistatic capacitance measurements is reduced with high Q/t. The maximum Q/t value for a given capacitance value depends on both the delay time and the step voltage. See the Model 595 Instruction Manual Specifications for details.

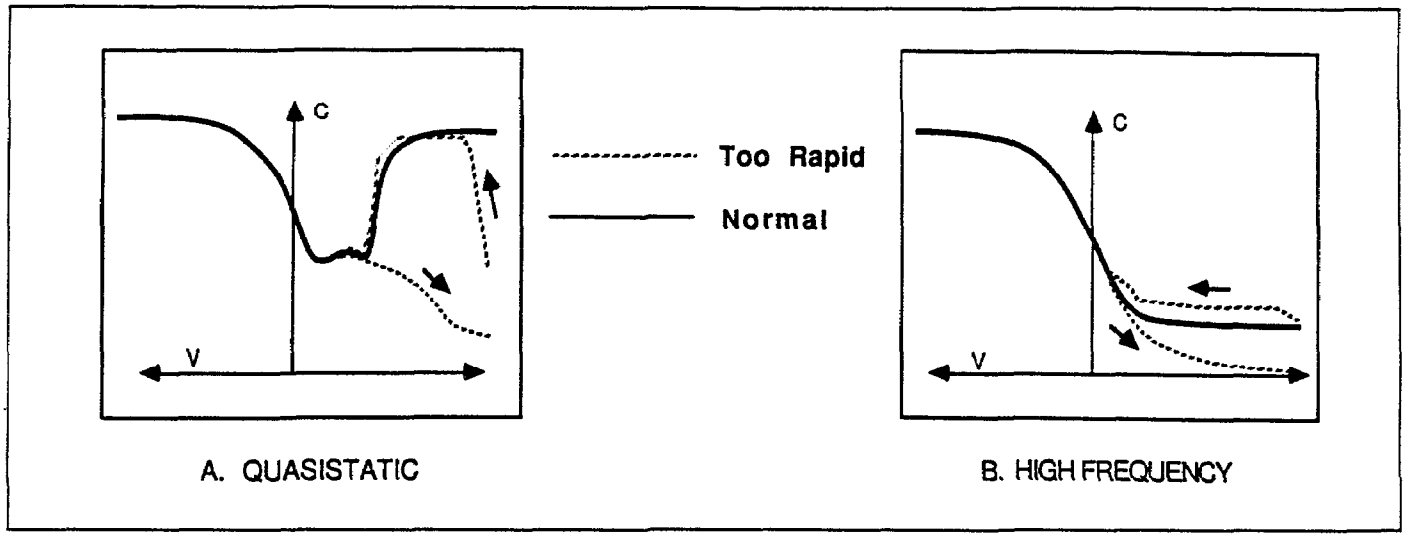


Figure 3-35. Curve Hysteresis Resulting When Sweep is Too Rapid

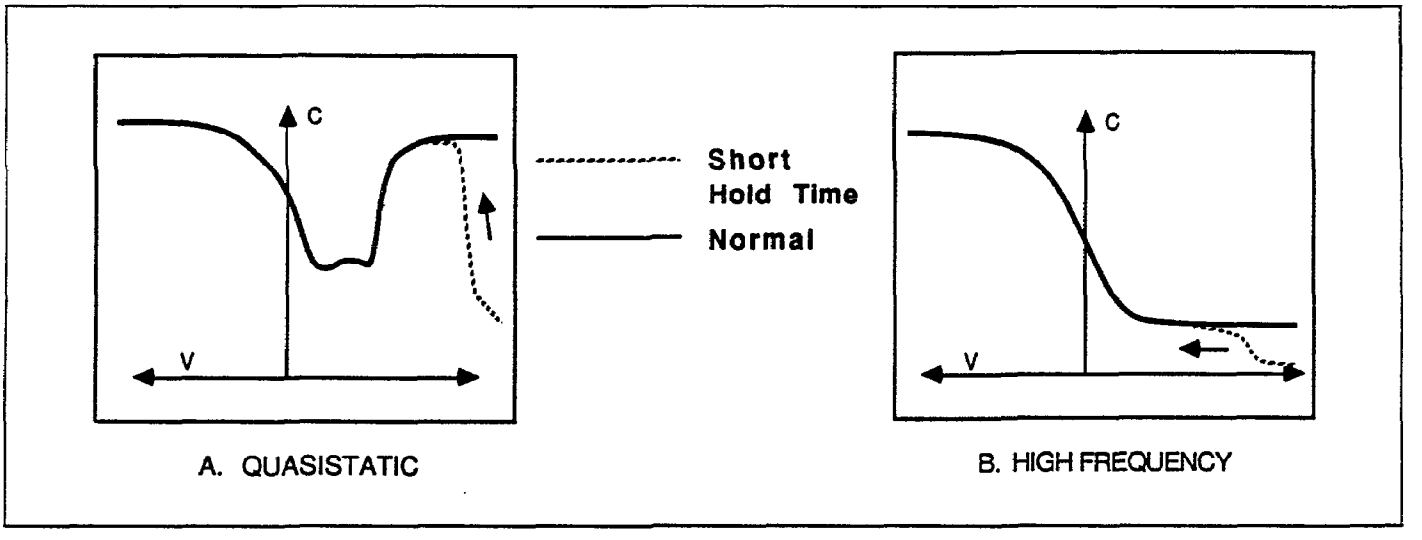


Figure 3-36. Distortion When Hold Time is Too Short

SECTION 4
Analysis

4.1 INTRODUCTION

This section covers the various analysis features of the Package 82 software. References and suggested reading are also included at the end of the section.

Information concerning equipment setup and measurement techniques may be found in Sections 2 and 3.

Section 4 information is arranged as follows:

4.2 Constants and Symbols Used for Analysis: Discusses the numerical constants and mathematical symbols used in this section and by the Package 82 software.

4.3 Obtaining Information from Basic CV Curves: Details how to obtain important information such as device type and C_{ox} from CV curves.

4.4 Analyzing CV Data: Discusses loading/saving reading data, graphing reading data, and graphical and mathematical analysis.

4.5 Mobile Ionic Charge Concentration Measurement: Discusses two methods to measure the mobile ionic charge concentration in the oxide of an MOS device.

4.6 References and Bibliography of CV Measurements and Related Topics: Lists references used in this section, along with additional texts and papers for suggested reading on CV measurement and analysis topics.

4.2 CONSTANTS AND SYMBOLS USED FOR ANALYSIS

4.2.1 Constants

Constants used by the Package 82 are summarized below. These constants are declared at the top of the program listing and are initialized for silicon and silicon dioxide. The constants can be re-defined for other material types, if desired.

$q = 1.60219 \times 10^{-19}$C. q is the fundamental unit of charge on an electron given in coulombs.

$kT = 4.046 \times 10^{-21}$J. kT represents thermal energy and is defined at room temperature (293°K).

$\epsilon_{ox} = 3.400 \times 10^{-13}$F/cm. ϵ_{ox} is the permittivity of silicon dioxide.

$\epsilon_s = 1.04 \times 10^{-12}$F/cm. ϵ_s is the permittivity of silicon.

$E_G = 1.12$eV. E_G is the energy gap of silicon from valence band to conduction band edge. Ideally no energy states are allowed in the gap.

$n_i = 1.45 \times 10^{10}$ cm^{-3}. n_i is the intrinsic carrier concentration per cm^3 in 25°C silicon.

4.2.2 Raw Data Symbols

The following symbols are used for data measured and sent by the Models 590 and 595. C'_Q is interpolated from C_Q so that C'_Q and C_H are values at the same bias voltage.

C_H	High-frequency capacitance, as measured by the Model 590 at either 100kHz or 1MHz.
C_Q	Quasistatic capacitance measured by the Model 595. C_Q' is interpolated from C_Q' so that C_Q' and C_H are values at the same bias voltage.
G	High-frequency conductance, as measured by the Model 590 at either 100kHz or 1MHz.
Q/t	Current measured by the Model 595 at the end of each capacitance measurement with the unit in the capacitance function.
V_H	Voltage reading sent by Model 590 with matching C_H and G_H.

4.2.3 Calculated Data Symbols

Calculated data used by the various analysis algorithms include:

A	Device gate area, usually a round aluminum dot.
C_{FB}	Flatband capacitance, corresponding to no band bending.
C_{QA}	The quasistatic capacitance that is adjusted according to gain and offset values. C_{QA} is the value that is actually plotted and printed.
C_Q'	Interpolated value of C_Q set to correspond to the quasistatic capacitance at V.
C_{HA}	The high-frequency capacitance that is adjusted according to gain and offset values. C_{HA} is the value that is actually plotted and printed.
C_{OX}	Oxide capacitance, usually set to the maximum C_H in accumulation.
D_{IT}	Density or concentration of interface states.
E_C	Energy of conduction band edge (valence band is E_V).
E_T	Interface trap energy.
L_B	Extrinsic Debye length.
N_A	Bulk doping for p-type (acceptors)
N_D	Bulk doping for n-type (donors)
N(90% W_{MAX})	Doping corresponding to 90% maximum w profile (approximates doping in the bulk).
N_M	Mobile ion concentration in the oxide.
t_{OX}	Oxide thickness.
V_{FB}	Flatband voltage, or the value of V_{GS} that results in C_{FB}.
V_{GS}	Gate voltage. More specifically, the voltage at the gate with respect to the substrate.
$V_{THRESHOLD}$	The point where the surface potential, ψ_S, is equal to twice the bulk potential, ϕ_B.
w	Depletion depth or thickness. Silicon under the gate is depleted of minority carriers in inversion and depletion.
Δ(i)	An intermediate value used in calculations.
ψ_S	Silicon surface potential as a function of V_{GS} . More precisely, this value represents band bending and is related to surface potential via the bulk potential.
ψ_0	Offset in ψ_S due to calculation method and V_O .
ϕ_B	Silicon bulk potential.

4.3 OBTAINING INFORMATION FROM BASIC CV CURVES

Much important information about the device under test can be obtained directly from a basic CV curve. Such information includes device type (p- or n-type material) and C_{OX} (oxide capacitance). These aspects are discussed in the following paragraphs.

4.3.1 Basic CV Curves

Figures 4-1 and 4-2 show fundamental CV curves for p-type and n-type materials respectively. Both high-frequency and quasistatic curves are shown in these figures. Note that the high-frequency curves are highly asymmetrical, while the quasistatic curves are almost symmetrical. Accumulation, depletion, and inversion regions are also shown on the curves. The gate biasing polarity and high-frequency curve shape can be used to determine device type, as discussed below.

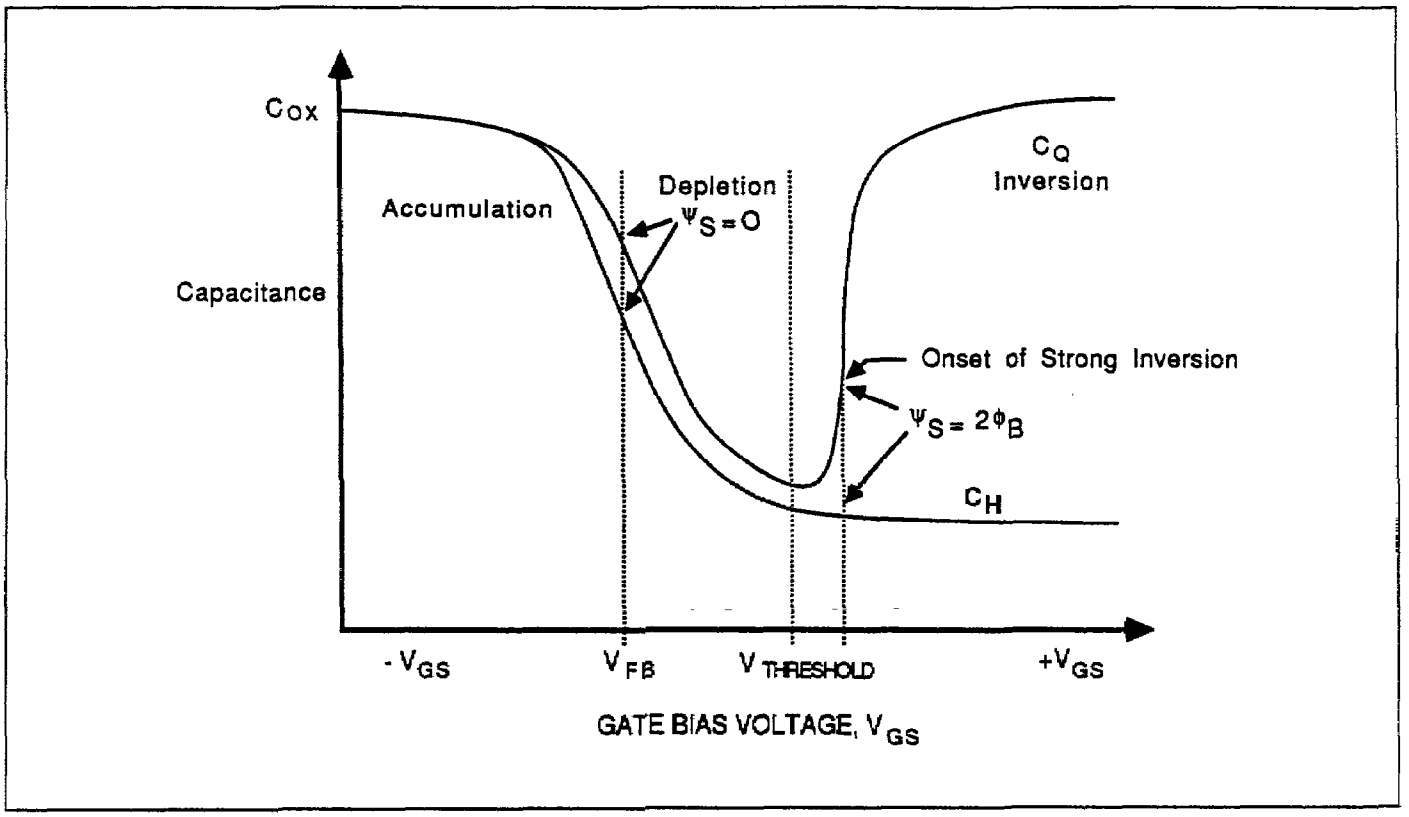


Figure 4-1. CV Characteristics of p-type Material

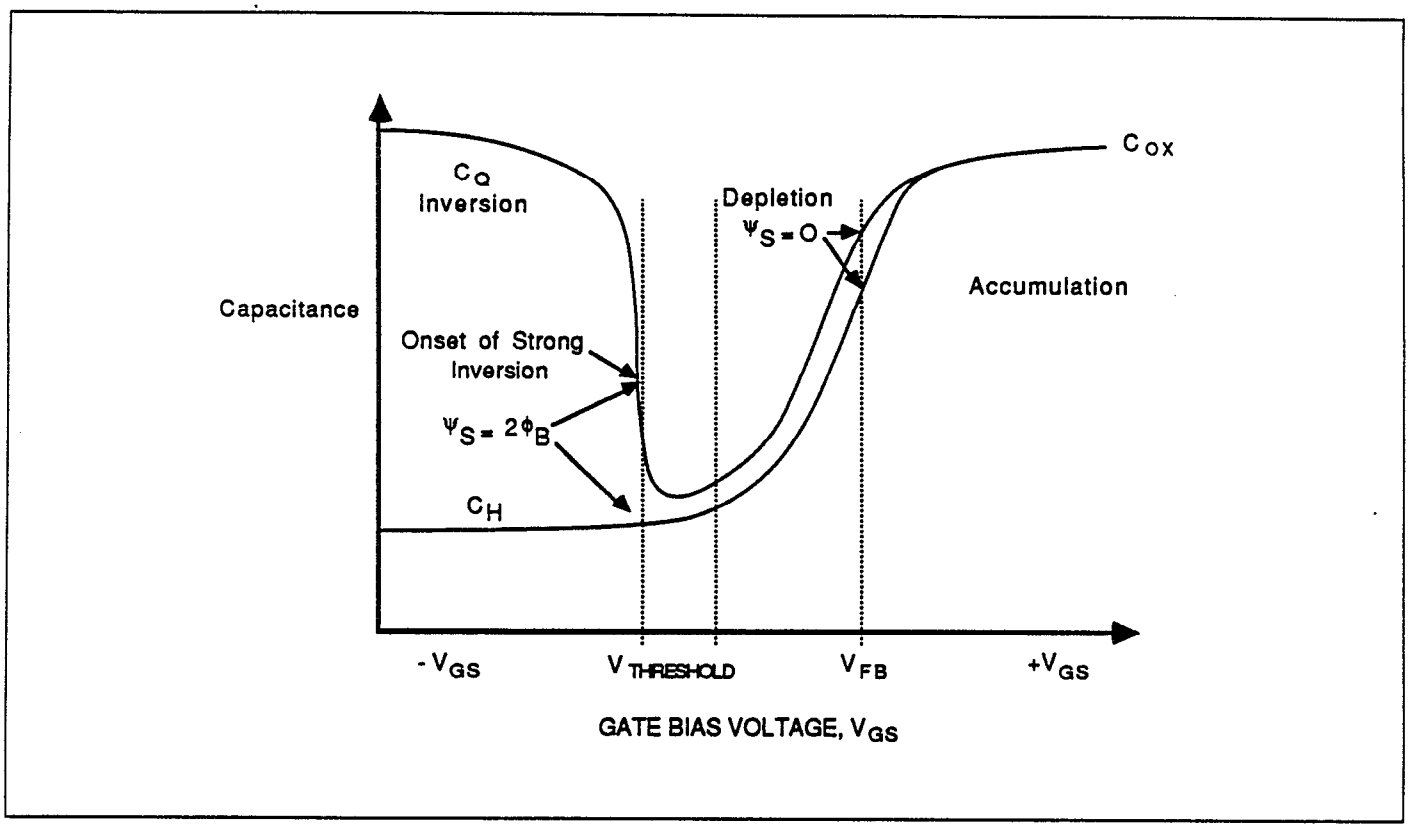


Figure 4-2. CV Characteristics of n-type Material

4.3.2 Determining Device Type

The semiconductor conductivity type (p or n dopant ions) can be determined from the relative shape of the CV curves. The high-frequency curve gives a better indication than the quasistatic curve because of its highly asymmetrical nature. Note that the CV curve moves from the accumulation to the inversion region as gate voltage, V_{GS}, becomes more positive for p-type materials, but the curve moves from accumulation to inversion as V_{GS} becomes more negative with n-type materials (Nicollian and Brews 372-374).

In order to determine the material type, use the following rules:

1. If C_H is greater when V_{GS} is negative than when V_{GS} is positive, the substrate material is p-type.
2. If, on the other hand, C_H is greater with positive V_{GS} than with negative V_{GS}, the substrate is n-type.
3. The end of the curve where C_H is greater is the accumulation region, while the opposite end of the curve is the inversion region. The transitional area between these two is the depletion region. These areas are marked on Figures 4-1 and 4-2.

4.4 ANALYZING CV DATA

A number of operations can be performed on sweep data stored in a reading array including: saving or loading reading data to or from disk, displaying or printing reading data, graphing or plotting reading data, as well as mathematical analysis of doping profile, flatband calculations, and interface traps. The following paragraphs discuss analysis operations available with the Package 82 software.

4.4.1 Plotter and Printer Requirements

Plotter

A plotter can be used to obtain hard copy graphs. The Package 82 software supports only plotters that use HP-GL graphics language. Only IEEE-488 plotters can be used.

The plotter must be set to the addressable mode with a primary address of 5. The plotter must, of course, be connected to the IEEE-488 bus of the computer using a suitable IEEE-488 cable. A shielded IEEE-488 cable should be used to avoid possible interference with other equipment.

Printer

A printer can be connected to the IEEE-488 bus to provide hardcopy printout of data. Note that the printer must be set to a primary address of 1. For the IBM AT, a printer can also be used with the parallel or serial port as long as the print path was changed (see paragraph 2.7.)

NOTE

Use the HP BASIC "DUMP GRAPHICS" or "DUMP ALPHA" statements to obtain a hard copy of any screen.

4.4.2 Analysis Menu

Figure 4-3 shows the analysis menu. You can access this menu either by selecting option 6, Analyze CV Data, on the main menu, or through most other submenus.

Key operations available on the menu include:

- Saving or loading array data to or from disk.
- Displaying (CRT) or printing (external printer) reading or graphics array data.
- Displaying or modifying numerical values such as C_{ox}, t_{ox}, and N (doping concentration).
- Graphing or plotting reading array data.
- Graphical and mathematical analysis of the data array.

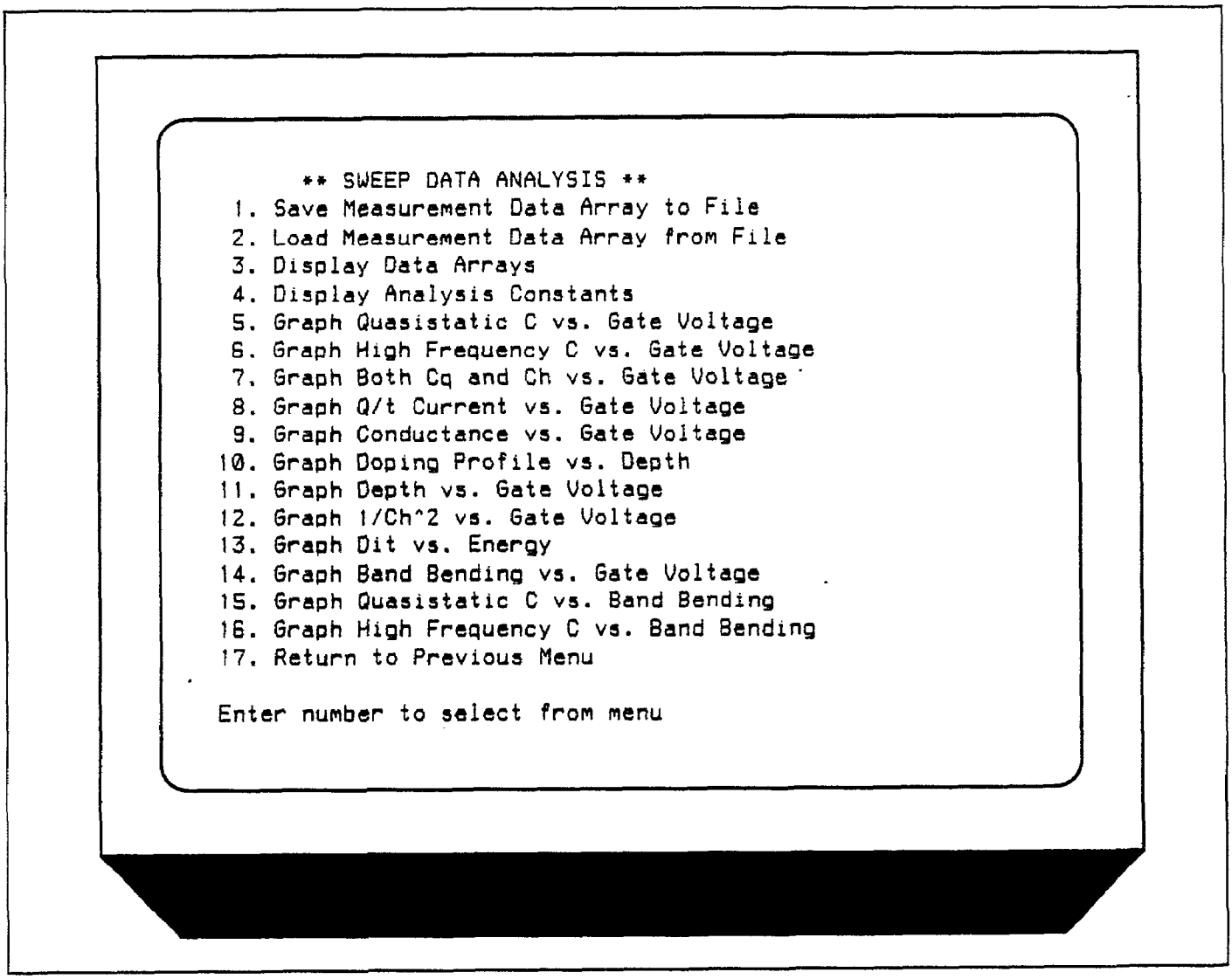


Figure 4-3. Data Analysis Menu

4.4.3 Saving and Recalling Data

By selecting option 1 or 2 you can save the current reading array to diskette, or load previously taken readings from diskette into the reading array. In addition to the array elements (C_Q, C_H, Q/t, G, and V_{GS}), the following numerical values are saved with the array: C_{ox}, A, t_{ox}, Step V, N, and graph offset and gain values.

NOTE

Loading reading from diskette will overwrite any data currently stored in the reading array. Data analysis and graphing is always carried out on data currently stored in the reading array.

Saving the Reading Array

Use the following procedure to save sweep data presently stored in the reading array.

1. Select option 1 on the analysis menu.
2. The computer will display the current disk directory.
3. You will then be prompted to type in the desired filename. Be sure to choose a name not on the present directory.
4. Next you will be prompted to enter header information, up to a maximum of 160 characters. This feature can be used to enter important information about the data you are saving. For example, you may wish to enter the type of device, the date, and the time the data was taken for future reference.
5. After entering header information, you will be given one last opportunity to change it.
6. If the header information is correct, respond affirmatively to store the reading array to disk. Once storage is complete, you will be returned to the analysis menu.

Loading the Reading Array

Use the procedure below to recall data from diskette and store it to the reading array. Remember that any data presently in the reading array will be overwritten by the data loaded from diskette.

1. Select option 2 on the analysis menu. The computer will then display the current disk directory.
2. At the prompt, type in the desired filename and press ENTER.
3. If the file exists, the reading array will be filled with the data from the file; however, an error message will be given if the file does not exist, or if it is of the wrong type.
4. The header information will be displayed after the file is loaded.
5. To return to the analysis menu, press ENTER.

4.4.4 Displaying and Printing the Reading and Graphics Arrays

By selecting option 3 on the analysis menu, you can display array data on the computer CRT or print out that array data for hardcopy. In order to print the data, you must, of course, have a printer connected to the IEEE-488 bus. When displaying array data, the screen will be cleared before arrays are displayed.

Note that you can display or print either reading or graphics array data by selecting the appropriate option on the submenu. The displayed and printed reading array data includes the reading number; quasistatic capacitance, current (Q/t); and high-frequency capacitance, conductance, and gate voltage. An example is shown in Figure 4-4.

NOTE

The quasistatic and high-frequency capacitance values that are plotted, printed, and used in calculations are first corrected for gain and offset (paragraph 4.4.6) to obtain C_{QA} and C_{HA} (adjusted capacitance).

Graphics array data includes depletion depth, doping concentration, band bending, interface trap energy, $1/C^2$, and interface trap density. An example is shown in Figure 4-5.

NOTE

Values of 10^{50} "flag" invalid data as explained in paragraph 4.4.8.

When displaying data on the CRT, you have the option of selecting the first reading number to display.

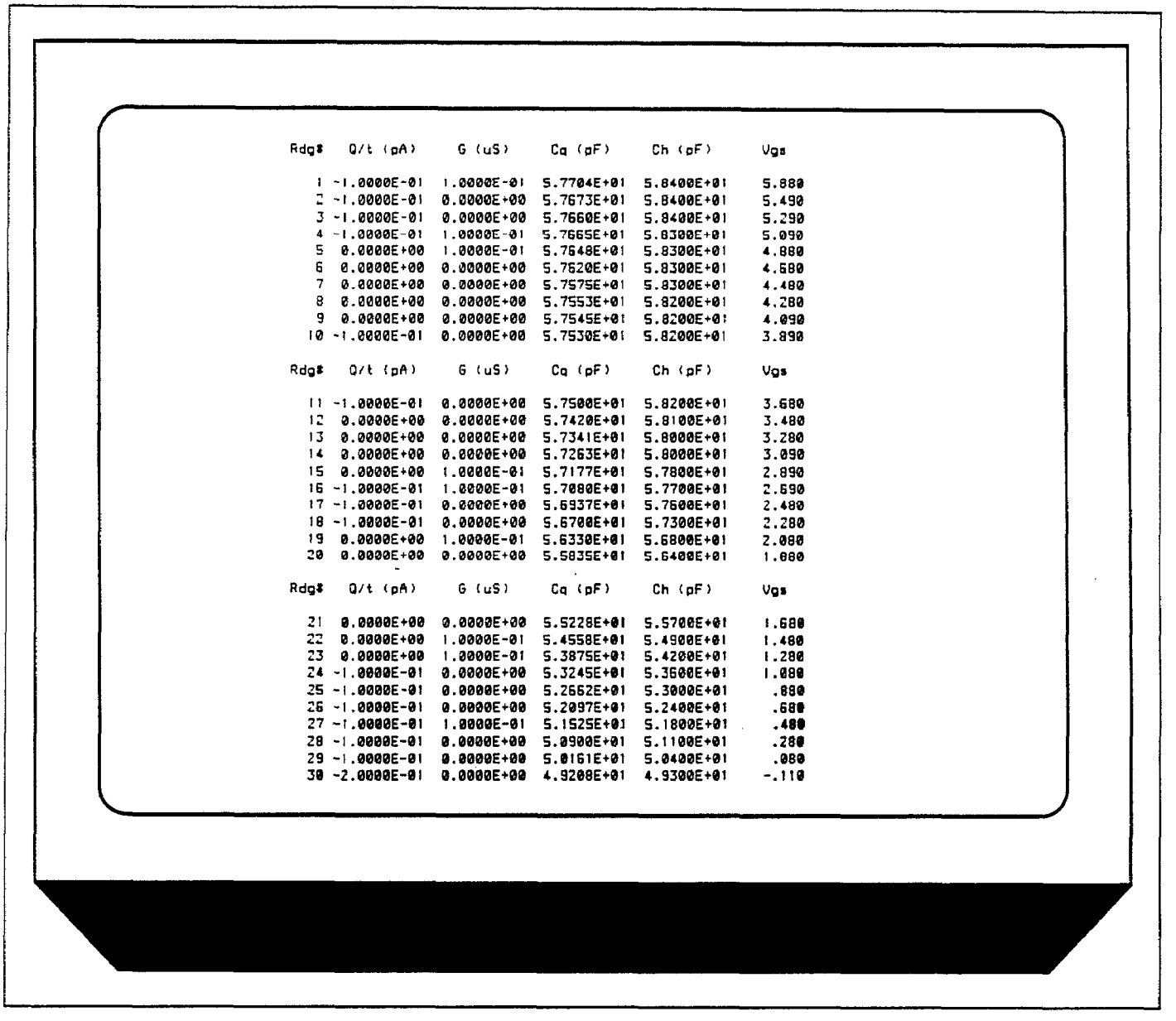
To print only a portion of the array, display that portion and then use the BASIC "DUMP ALPHA" statement.

Changing the Graphics Window

The graphics window defines the contiguous array area to be plotted. To change the graphics range (select graphics window), selection option 3 on the analysis menu, then option 5 on the subsequent menu. The present graphics

range along with best depth and total array size will be displayed. Key in the first and last readings in the window separated by commas.

One particularly good use for this feature is to select the window for best depth. The range over which N and D_{IT} are accurate within ±5% is equal to best depth. The graphics window can also be used to zoom in on interesting sections of other curves.

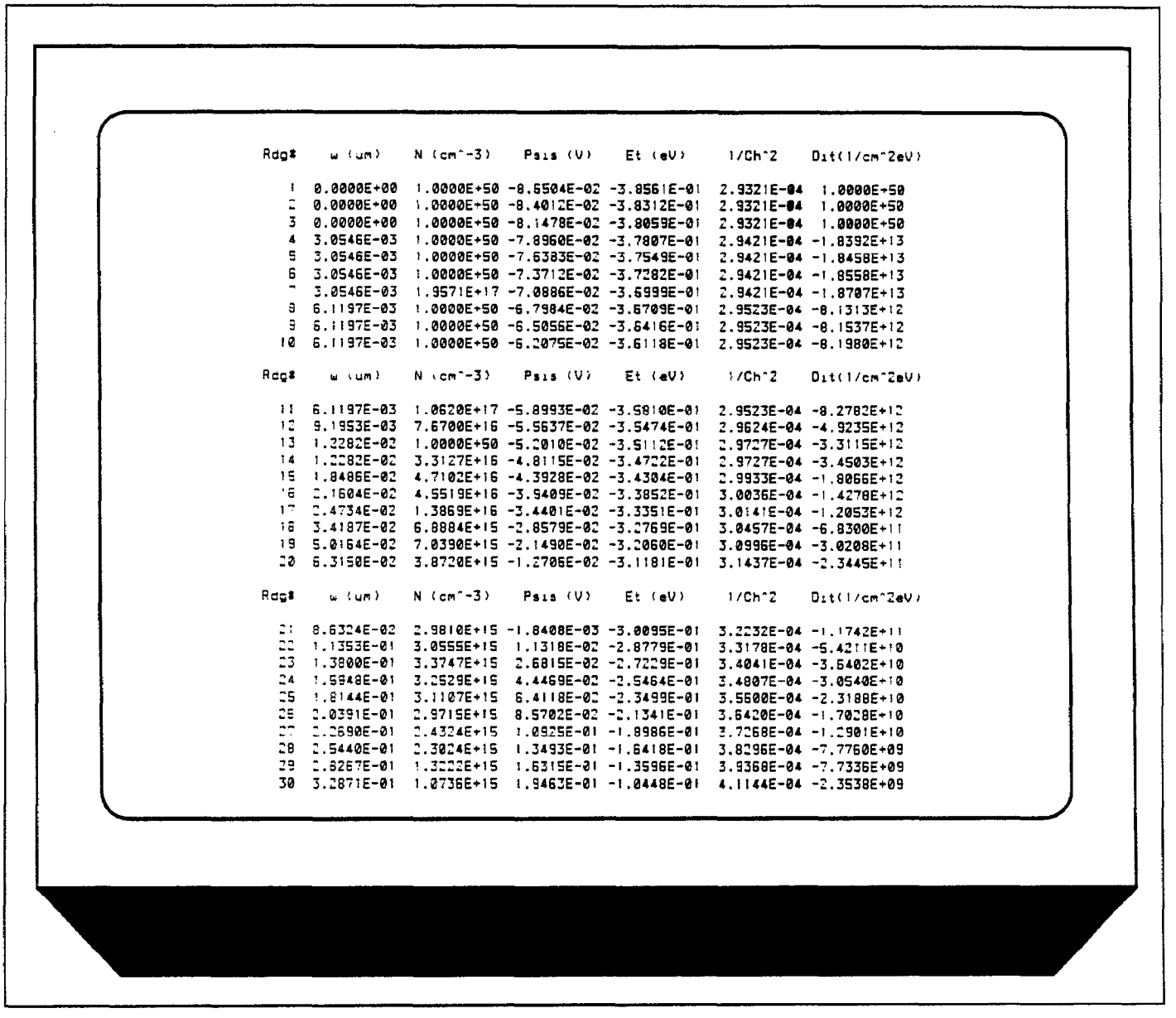


Rdg#	Q/t (pA)	G (uS)	Cq (pF)	Ch (pF)	Vgs
1	-1.0000E-01	1.0000E-01	5.7704E+01	5.8400E+01	5.880
2	-1.0000E-01	0.0000E+00	5.7673E+01	5.8400E+01	5.490
3	-1.0000E-01	0.0000E+00	5.7660E+01	5.8400E+01	5.290
4	-1.0000E-01	1.0000E-01	5.7665E+01	5.8300E+01	5.090
5	0.0000E+00	1.0000E-01	5.7648E+01	5.8300E+01	4.880
6	0.0000E+00	0.0000E+00	5.7620E+01	5.8300E+01	4.680
7	0.0000E+00	0.0000E+00	5.7575E+01	5.8300E+01	4.480
8	0.0000E+00	0.0000E+00	5.7553E+01	5.8200E+01	4.280
9	0.0000E+00	0.0000E+00	5.7545E+01	5.8200E+01	4.090
10	-1.0000E-01	0.0000E+00	5.7530E+01	5.8200E+01	3.890

Rdg#	Q/t (pA)	G (uS)	Cq (pF)	Ch (pF)	Vgs
11	-1.0000E-01	0.0000E+00	5.7500E+01	5.8200E+01	3.680
12	0.0000E+00	0.0000E+00	5.7420E+01	5.8100E+01	3.480
13	0.0000E+00	0.0000E+00	5.7341E+01	5.8000E+01	3.280
14	0.0000E+00	0.0000E+00	5.7263E+01	5.8000E+01	3.090
15	0.0000E+00	1.0000E-01	5.7177E+01	5.7800E+01	2.890
16	-1.0000E-01	1.0000E-01	5.7080E+01	5.7700E+01	2.690
17	-1.0000E-01	0.0000E+00	5.6937E+01	5.7600E+01	2.480
18	-1.0000E-01	0.0000E+00	5.6700E+01	5.7300E+01	2.280
19	0.0000E+00	1.0000E-01	5.6330E+01	5.6800E+01	2.080
20	0.0000E+00	0.0000E+00	5.5835E+01	5.6400E+01	1.880

Rdg#	Q/t (pA)	G (uS)	Cq (pF)	Ch (pF)	Vgs
21	0.0000E+00	0.0000E+00	5.5228E+01	5.5700E+01	1.680
22	0.0000E+00	1.0000E-01	5.4558E+01	5.4900E+01	1.480
23	0.0000E+00	1.0000E-01	5.3875E+01	5.4200E+01	1.280
24	-1.0000E-01	0.0000E+00	5.3245E+01	5.3600E+01	1.080
25	-1.0000E-01	0.0000E+00	5.2662E+01	5.3000E+01	.880
26	-1.0000E-01	0.0000E+00	5.2097E+01	5.2400E+01	.680
27	-1.0000E-01	1.0000E-01	5.1525E+01	5.1800E+01	.480
28	-1.0000E-01	0.0000E+00	5.0900E+01	5.1100E+01	.280
29	-1.0000E-01	0.0000E+00	5.0161E+01	5.0400E+01	.080
30	-2.0000E-01	0.0000E+00	4.9208E+01	4.9300E+01	-.110

Figure 4-4. Example of Reading Array Print Out



Rdg#	w (um)	N (cm^-3)	Psis (V)	Et (eV)	1/Ch^2	Dit(1/cm^2eV)
1	0.0000E+00	1.0000E+50	-8.5504E-02	-3.8561E-01	2.9321E-04	1.0000E+50
2	0.0000E+00	1.0000E+50	-8.4012E-02	-3.8312E-01	2.9321E-04	1.0000E+50
3	0.0000E+00	1.0000E+50	-8.1478E-02	-3.8059E-01	2.9321E-04	1.0000E+50
4	3.0546E-03	1.0000E+50	-7.8960E-02	-3.7807E-01	2.9421E-04	-1.8392E+13
5	3.0546E-03	1.0000E+50	-7.6383E-02	-3.7549E-01	2.9421E-04	-1.8458E+13
6	3.0546E-03	1.0000E+50	-7.3712E-02	-3.7282E-01	2.9421E-04	-1.8558E+13
7	3.0546E-03	1.9571E+17	-7.0886E-02	-3.6999E-01	2.9421E-04	-1.8707E+13
8	6.1197E-03	1.0000E+50	-6.7984E-02	-3.6709E-01	2.9523E-04	-8.1313E+12
9	6.1197E-03	1.0000E+50	-6.5056E-02	-3.6416E-01	2.9523E-04	-8.1537E+12
10	6.1197E-03	1.0000E+50	-6.2075E-02	-3.6118E-01	2.9523E-04	-8.1980E+12

Rdg#	w (um)	N (cm^-3)	Psis (V)	Et (eV)	1/Ch^2	Dit(1/cm^2eV)
11	6.1197E-03	1.0620E+17	-5.8993E-02	-3.5810E-01	2.9523E-04	-8.2782E+12
12	9.1953E-03	7.6700E+16	-5.5637E-02	-3.5474E-01	2.9624E-04	-4.9235E+12
13	1.2282E-02	1.0000E+50	-5.2010E-02	-3.5112E-01	2.9727E-04	-3.3115E+12
14	1.2282E-02	3.3127E+16	-4.8115E-02	-3.4722E-01	2.9727E-04	-3.4503E+12
15	1.8486E-02	4.7102E+16	-4.3928E-02	-3.4304E-01	2.9933E-04	-1.8066E+12
16	2.1604E-02	4.5519E+16	-3.9409E-02	-3.3852E-01	3.0036E-04	-1.4278E+12
17	2.4734E-02	1.3869E+16	-3.4401E-02	-3.3351E-01	3.0141E-04	-1.2053E+12
18	3.4187E-02	6.8884E+15	-2.8579E-02	-3.2769E-01	3.0457E-04	-6.8300E+11
19	5.0164E-02	7.0390E+15	-2.1490E-02	-3.2060E-01	3.0996E-04	-3.0208E+11
20	6.3150E-02	3.8720E+15	-1.2706E-02	-3.1181E-01	3.1437E-04	-2.3445E+11

Rdg#	w (um)	N (cm^-3)	Psis (V)	Et (eV)	1/Ch^2	Dit(1/cm^2eV)
21	8.6324E-02	2.9810E+15	-1.8408E-03	-3.0095E-01	3.2232E-04	-1.1742E+11
22	1.1353E-01	3.0555E+15	1.1318E-02	-2.8779E-01	3.3178E-04	-5.4211E+10
23	1.3800E-01	3.3747E+15	2.6815E-02	-2.7229E-01	3.4041E-04	-3.6402E+10
24	1.5948E-01	3.2529E+15	4.4469E-02	-2.5464E-01	3.4807E-04	-3.0540E+10
25	1.8144E-01	3.1107E+15	6.4118E-02	-2.3499E-01	3.5600E-04	-2.3188E+10
26	2.0391E-01	2.9715E+15	8.5702E-02	-2.1341E-01	3.6420E-04	-1.7028E+10
27	2.2690E-01	2.4324E+15	1.0925E-01	-1.8986E-01	3.7268E-04	-1.2901E+10
28	2.5440E-01	2.3024E+15	1.3493E-01	-1.6418E-01	3.8296E-04	-7.7760E+09
29	2.8267E-01	1.3222E+15	1.6315E-01	-1.3596E-01	3.9368E-04	-7.7336E+09
30	3.2871E-01	1.8736E+15	1.9463E-01	-1.0448E-01	4.1144E-04	-2.3538E+09

Figure 4-5. Example of Graphics Array Print Out

4.4.5 Graphing Data

Selecting a graphing option will cause a graph to be generated on the screen, along with the graphics control window.

NOTE

A particular graph retains its configuration until a new reading array is analyzed.

The graphics control menu is shown in Figure 4-6. Through this menu you can select the following:

1. Auto Scaling. When auto scaling is selected, the minimum and maximum values for the data will automatically be used as the limits for both X and Y axes.
2. Axes Limits. This option allows you to select the minimum and maximum limits for both X and Y axes, and it can be used to zoom in on a portion of the curve. At the prompt, type in Xmin, Xmax, Ymin, and Ymax separated by commas. To leave a parameter unchanged, simply type in a comma at that position. Note that the graph can be reversed top to bottom or right to left by interchanging maximum and minimum limit values. See also paragraph 4.4.5 for using the graphics window as an alternative.
3. Plot Graph. This option dumps the complete graph including the curve and axes to the plotter. Note, however, that the graphics control menu will not appear on the hard copy plot. "DUMP GRAPHICS" can be used to dump the graphics screen to a compatible printer. To do so, pause the program, "DUMP GRAPHICS", then continue the program.
4. Plot Curve. Use this option to generate the curve only on the external plotter. This feature is useful for drawing more than one curve on a graph.
5. Change Notes. You can type in two lines of notes that will appear at the top of the graph by using this option. The notes will also appear on any hard copy plot made of the graph. Each line is entered separately.
6. A. Normalize to C_{ox}. This option is available only when plotting C_Q or C_H vs. some other parameter such as gate voltage or band bending. When selected, the Y axis will show C/C_{ox}.
   B. Lin/Log Graph. This option is available only for plots other than C_Q or C_H. When log is selected, the Y axis is plotted logarithmically, but the X axis remains linear. Note that absolute values are being plotted using the log option.
7. Adjust Gain/Offset C_Q or C_H.
8. Exit.

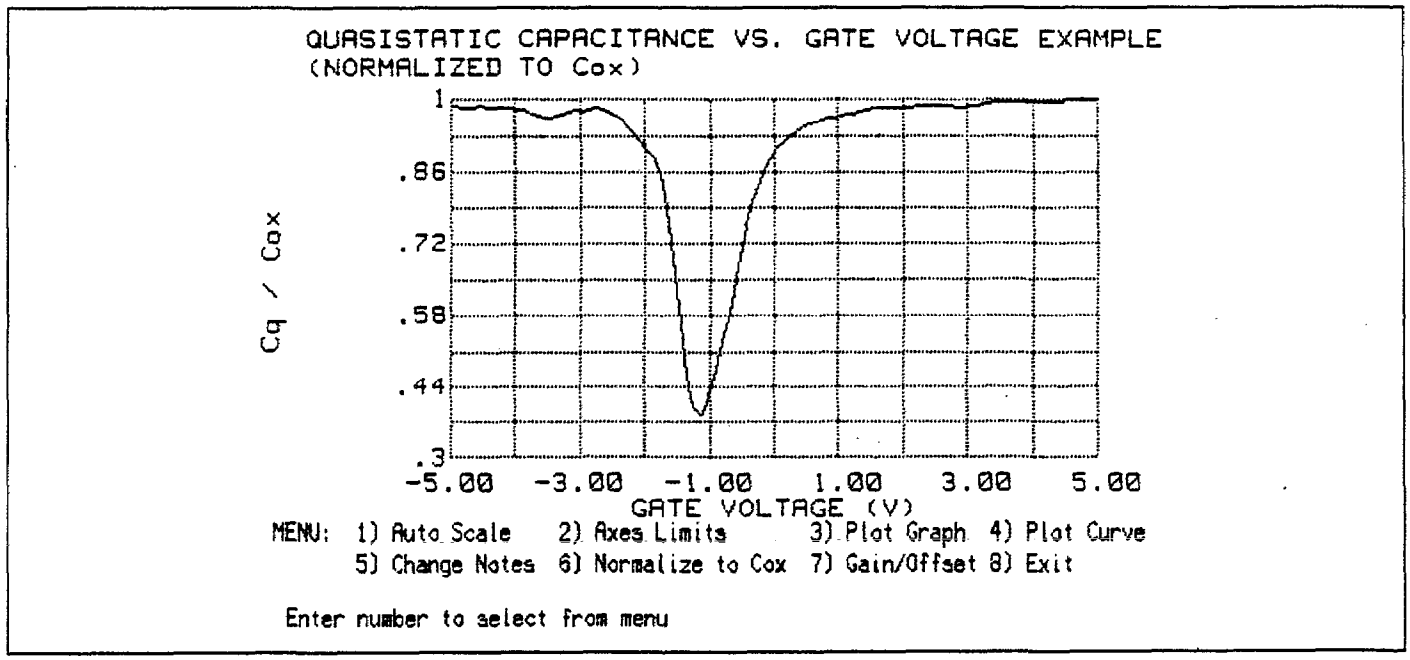


Figure 4-6. Graphics Control Menu

4.4.6 Analysis Tools

Graphical Analysis

Table 4-1 summarizes the graphical analysis tools included with the Package 82 software. To generate an analysis graph, simply select the desired option from the analysis menu and then tailor the graph using the graphics control menu. Reading data (C_{QA}, C_{HA}, G, Q/t, and V_{GS}) are plotted from reading array, while calculated data are plotted from the graphics array. See the following paragraphs for more detailed discussion of these arrays and plots.

Displaying Numerical Analysis Constants

Numerical analysis functions are summarized on Table 4-2. To use numerical analysis, select the option 4 on the analysis menu. Calculated data will then be displayed on the screen.

Table 4-2. Displayed Constants

Constant	Units
C_{OX}	pF
T_{OX}	nm
Area	cm^2
N_{BULK}	cm^{-3}
C_{FB}	pF
V_{FB}	V
$V_{THRESHOLD}$	V
ϕ_B	V
L_B	μm
Q_{EFF}	$Coul/cm^2$
Device type	p or n
Work function	V
Best depth	μm

Table 4-1. Graphical Analysis

Plot (Y vs X)	Description	Units	Comments
C_Q vs V_{GS}	Quasistatic capacitance vs gate voltage	pF vs V	C_Q/C_{OX} optional
C_H vs V_{GS}	High-frequency capacitance vs gate voltage	pF vs V	C_H/C_{OX} optional
$C_Q + C_H$ vs V_{GS}	Quasistatic & high frequency capacitance vs gate voltage	pF vs V	C_H/C_{OX}, C_Q/C_{OX} optional
Q/t vs V_{GS}	Current vs gate voltage	pA vs V	
G vs V_{GS}*	High frequency conductance vs gate voltage	μS vs V	
N vs w	Doping concentration vs depth	cm^{-3} vs μm	
$1/C_H^2$ vs V_{GS}	$1/C_H^2$ vs gate voltage	pF^{-2} vs V	$(C_{OX}/C_H)^2$ optional
w vs V_{GS}	Depth vs gate voltage	μm vs V	
D_{IT} vs E_T	Interface trap density vs trap energy	$cm^{-2}eV^{-1}$ vs eV	
ψ_S vs V_{GS}	Band bending vs gate voltage	V vs V	
C_Q vs ψ_S	Quasistatic capacitance vs band bending	pF vs V	C_Q/C_{OX} optional
C_H vs ψ_S	High-frequency capacitance vs band bending	pF vs V	C_H/C_{OX} optional

*R vs V_{GS} with R in ohms for series device model.

NOTE: Where indicated, plots can be normalized to C_{OX} by selecting C/C_{OX} option; remaining plots have semilog option.

Displayed values include:

C_{OX} (pF), oxide capacitance.
t_{OX} (nm), oxide thickness.
Area (cm^2), gate area.
N_{BULK} (cm^{-3}), bulk doping concentration.
C_{FB} (pF), flatband capacitance.
V_{FB} (V), flatband voltage.
$V_{THRESHOLD}$
ϕ_B (V), bulk doping.
L_B (μm), Debye length.
W_{MS} work function.
Q_{EFF}, effective oxide charge.

Best depth (μm), corresponds to the range of depth over which D_{IT} and N are accurate to within 5%.

C_Q gain and offset, C_H gain and offset, allow constant multipliers and offset values to be applied to C_Q and C_H data for curve alignment.

Changing C_{OX}, t_{OX}, and Area

Options 1 through 3 allow you to change C_{OX}, t_{OX}, or gate area. Changing any one of these values will cause the entire graphics array to be recalculated. Changing t_{OX} causes area to be recalculated; conversely, t_{OX} is recalculated if area is changed. If C_{OX} is selected, you will then be asked if t_{ox} or area is to be updated.

Changing N_{BULK}

Select option 4 on the analysis constants menu to enter a new value for N_{BULK}. Typically, N_A or N_D will be entered using this function. Note that the entire graphics array will be recalculated if N_{BULK} is changed.

Modifying Gain and Offet Values

Option 5 allows you to change the gain and offset values applied to C_Q and C_H data. Gain and offset can be entered to allow for curve alignment. A gain value is a multiplier that is applied to all elements of the array data (C_Q or C_H) before plotting or graphics array calculation. Offset is a constant value in pF added or subtracted to all C_Q or C_H data before plotting or array calculation. The adjusted capacitance values are called C_{QA} and C_{HA}.

For example, assume that you compare C_Q and C_H values at reading #3, and you find that C_Q is 2.3pF less than C_H. If you then add an offset of +2.3pF, the C_Q and C_H displayed readings will then be the same, and the two curves will be aligned at that point.

Gain and offset values do not affect raw C_Q and C_H values stored in the data file, but the gain and offset values will be stored with that data file so that compensated curves can easily be regenerated at a later date. To disable gain, program a value of unity (1); similarly, a value of 0 should be programmed to disable offset.

Threshold Voltage

The threshold voltage, $V_{THRESHOLD}$, is the point on the CV curve where the surface potential, ψ_S, equals twice the bulk potential, ϕ_B. This point on the curve corresponds to the onset of strong inversion (see Figures 4-1 and 4-2). For an enhancement mode MOSFET, $V_{THRESHOLD}$ corresponds to the point where the device begins to conduct.

$V_{THRESHOLD}$ is calculated as follows:

$$V_{THRESHOLD} = \left[\pm \frac{A}{10^{12} C_{OX}} \sqrt{4 \epsilon_S q |N_{BULK}| |\phi_B|} + 2 |\phi_B| \right] + V_{FB}$$

Where: $V_{THRESHOLD}$ = threshold voltage (V)
A = gate area (cm^2)
C_{OX} = oxide capacitance (pF)
10^{12} = units multiplier
ϵ_S = permittivity of silicon (1.04×10^{-12}F/cm)
q = electron charge (1.60219×10^{-12}/F/cm)
N_{BULK} = bulk doping (cm^{-3})
ϕ_B = bulk potential (V)
V_{FB} = flatband voltage (V)

Metal Semiconductor Work Function Difference

The metal semiconductor work function difference, W_{MS}, is commonly referred to as the work function. It contributes to the shift in V_{FB} from the ideal zero value, along with the effective oxide charge (Nicollian and Brews 462-477, Sze 395-402). The work function represents the difference in work necessary to remove an electron from the gate (assumed to be made of aluminum) and from the substrate assumed to be made of silicon), and it is derived as follows:

$$W_{MS} = W_M - \left[W_S + \frac{E_G}{2} - \phi_B \right]$$

$$W_{MS} = 4.1 - \left[4.15 + \frac{1.12}{2} - \phi_B \right]$$

Where: W_M = metal work function
W_S = silicon work function (electron affinity)
E_G = silicon bandgap
ϕ_B = bulk potential (defined in paragraph 4.3)

So that,

$$W_{MS} = -0.61 + \phi_B$$

$$W_{MS} = -0.61 - \left(\frac{kT}{q}\right) \ln\left(\frac{N_{BULK}}{n_i}\right) (\text{Dope Type})$$

Where, Dope Type is +1 for p-type materials, and −1 for n-type materials. For example, for an MOS capacitor with an aluminum gate and p-type silicon ($N_{BULK} = 10^{16}cm^{-3}$), $W_{MS} = -0.95V$. Also, for the same gate and n-type silicon ($N_{BULK} = 10^{16}cm^{-3}$), $W_{MS} = -0.27V$.

Effective Oxide Charge

The effective oxide charge, Q_{EFF}, represents the sum of oxide fixed charge, Q_F, mobile ionic charge, Q_M, and oxide trapped charge, Q_{OT}. Q_{EFF} is distinguished from interface trapped charge, Q_{IT}, in that Q_{IT} varies with gate bias and $Q_{EFF} = Q_F + Q_M + Q_{OT}$ does not (Nicollian and Brews 424-429, Sze 390-395). Simple measurements of oxide charge and CV measurements do not distinguish the three components of Q_{EFF}. These three components can be distinguished from one another by temperature cycling, as discussed in Nicollian and Brews, 429, Fig. 10.2. Also, since the charge profile in the oxide is not known, the quantity, Q_{EFF} should be used as a relative, not absolute measure of charge. It assumes that the charge is located in a sheet at the silicon-silicon dioxide interface. From Nicollian and Brews, Eq. 10.10, we have:

$$V_{FB} - W_{MS} = -\frac{Q_{EFF}}{C_{OX}}$$

Note that C_{OX} here is per unit of area. So that,

$$Q_{EFF} = \frac{C_{OX}(W_{MS} - V_{FB})}{A}$$

However, since C_{OX} is in F, we must convert to pF by multiplying by 10^{-12} as follows:

$$Q_{EFF} = 10^{-12}\,\frac{C_{OX}(W_{MS} - V_{FB})}{A}$$

Where: Q_{EFF} = effective charge (coul/cm²)
C_{OX} = oxide capacitance (pF)
W_{MS} = metal semiconductor work function (V)
A = gate area (cm²)

For example, assume a 0.01cm² 50pF capacitor with a flatband voltage of −5.95V, and a p-type $N_{BULK} = 10^{16}cm^{-3}$ (resulting in $W_{MS} = -0.95V$). Such a capacitor would have a $Q_{EFF} = 2.5 \times 10^{-8}$coul/cm².

4.4.7 Reading Array

During a voltage sweep, C_Q, C_H, G, Q/t, and V_{GS} are stored in the reading array where:

C_Q = Adjusted quasistatic capacitance
C_H = High-frequency capacitance
G = Conductance
Q/t = Current
V_{GS} = Gate voltage. Note that the substrate voltage is measured by the Model 590 and is changed to V_{GS} by negation.

General reading array structure is shown in Figure 4-7. Array readings are made at every other voltage step, but if the filter is on, the first four C_Q' and Q/t readings are invalid, so they are discarded.

Q/t, G, C_H, and V_H are all measured at the same point in the sweep, but C'_Q is measured one-half step V before V_H is measured. Since some calculations require that C_Q and C_H are measured at the same voltage, C_Q' must be interpolated to C_Q as follows:

$$C_Q(i) = C_Q'(i) + \frac{C_Q'(i+1) - C_Q'(i)}{V_H(i+1) - V_H(i)}\,\frac{V_{STEP}}{2}$$

After interpolation, the C_Q and C_H values are adjusted according to programmed gain and offset values to determine C_{QA} and C_{HA} (adjusted C_Q and C_H). C_{QA} and C_{QH} are the values actually plotted, printed, and used in calculations.

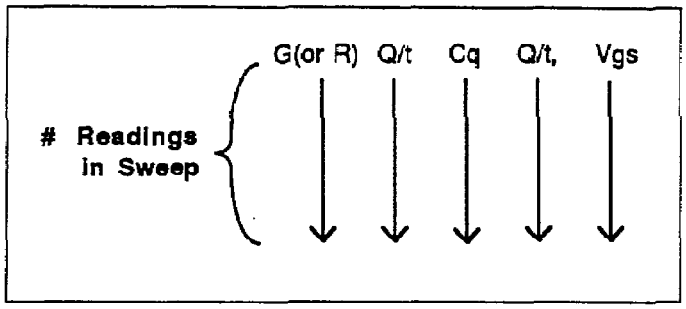


Figure 4-7. Reading Array

4.4.8 Calculated Data Array (Graphics Array)

In order to support the analysis functions, a calculated data (graphics) array must be built to include w, N, ψ_S, E_T, and D_{IT}, where:

w = Depletion depth or thickness
N = Doping concentration
ψ_S = Band bending
E_T = Interface trap energy
D_{IT} = Density of interface traps
$1/C^2$ = High-frequency capacitance

Graphics Array Structure

The graphics array is constructed by solving for these parameters at each value of V_{GS} using C_{QA}, C_{HA}, C_{OX}, and gate area, resulting in the general structure shown in Figure 4-8. The graphics array is recalculated each time analysis is selected on the menu, if new data has been taken, or if a reading data file is loaded from diskette. If C_{OX}, t_{OX}, and gate area are not defined, the array is not calculated, and the user is notified.

Changing Device Constants

Changing C_{OX}, gate area, or t_{OX} will cause the entire graphics array to be recalculated. Changing N_{BULK} will cause C_{FB}, ψ_S, and E_T to be recalculated.

Invalid Array Values

Most of the equations used for analysis can have a situation where a divide by zero error could occur in certain circumstances (for example, if $C_H = C_{OX}$, or $C_H(i) = C_H(i+1)$). In order to avoid problems, a very high value (10^{50}) is placed in any array element where such a divide by zero error occurred. During plotting, a test for 10^{50} is done and the pen is lifted for invalid values. As a result, the curve will be generated only over areas of valid data.

Discontinuous areas of a curve are normal with some curves because trap tests are intended only for depletion; also curves might not be properly aligned, resulting in invalid areas when plotting D_{IT}.

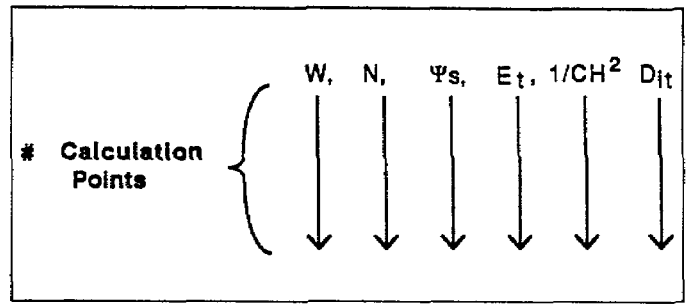


Figure 4-8. Graphics Array

4.4.9 Constants Used for Analysis

Table 4-3 summarizes constants used for analysis. These constants are defined at the top of the program listing. Note that the constants assume silicon devices, and they can be changed (where applicable) for analysis of other type of semiconductor material, if desired.

4.4.10 Graphing the Reading Array

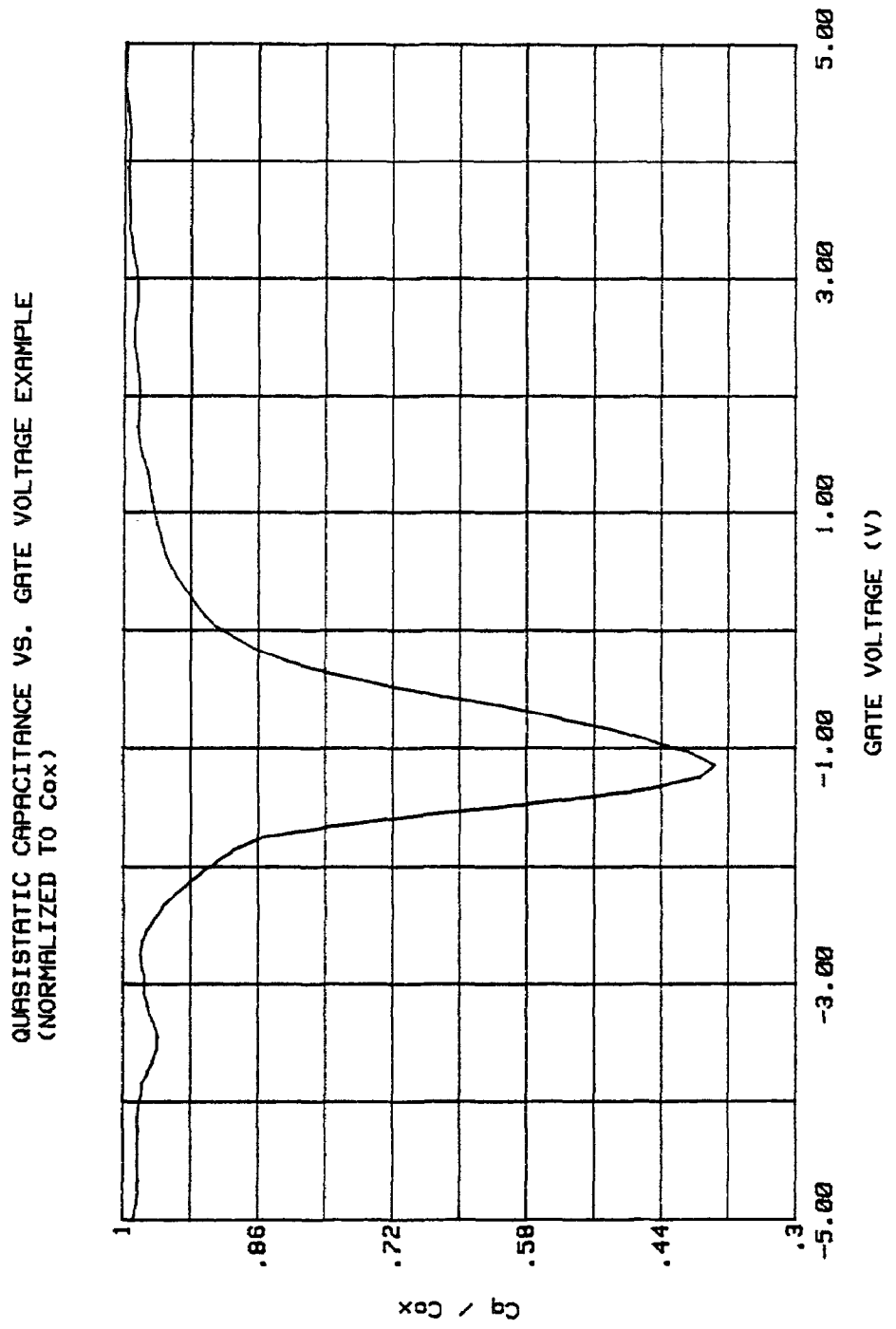
Data from the reading array can be graphed by selecting the appropriate option(s) on the analysis menu. Data that can be plotted includes:

C_{QA} vs. V_{GS}
C_{HA} vs. V_{GS}

Both C_{QA} and C_{HA} vs. V_{GS} on the same graph
Q/t vs. V_{GS}
G vs. V_{GS} (R vs V_{GS} for series device model)

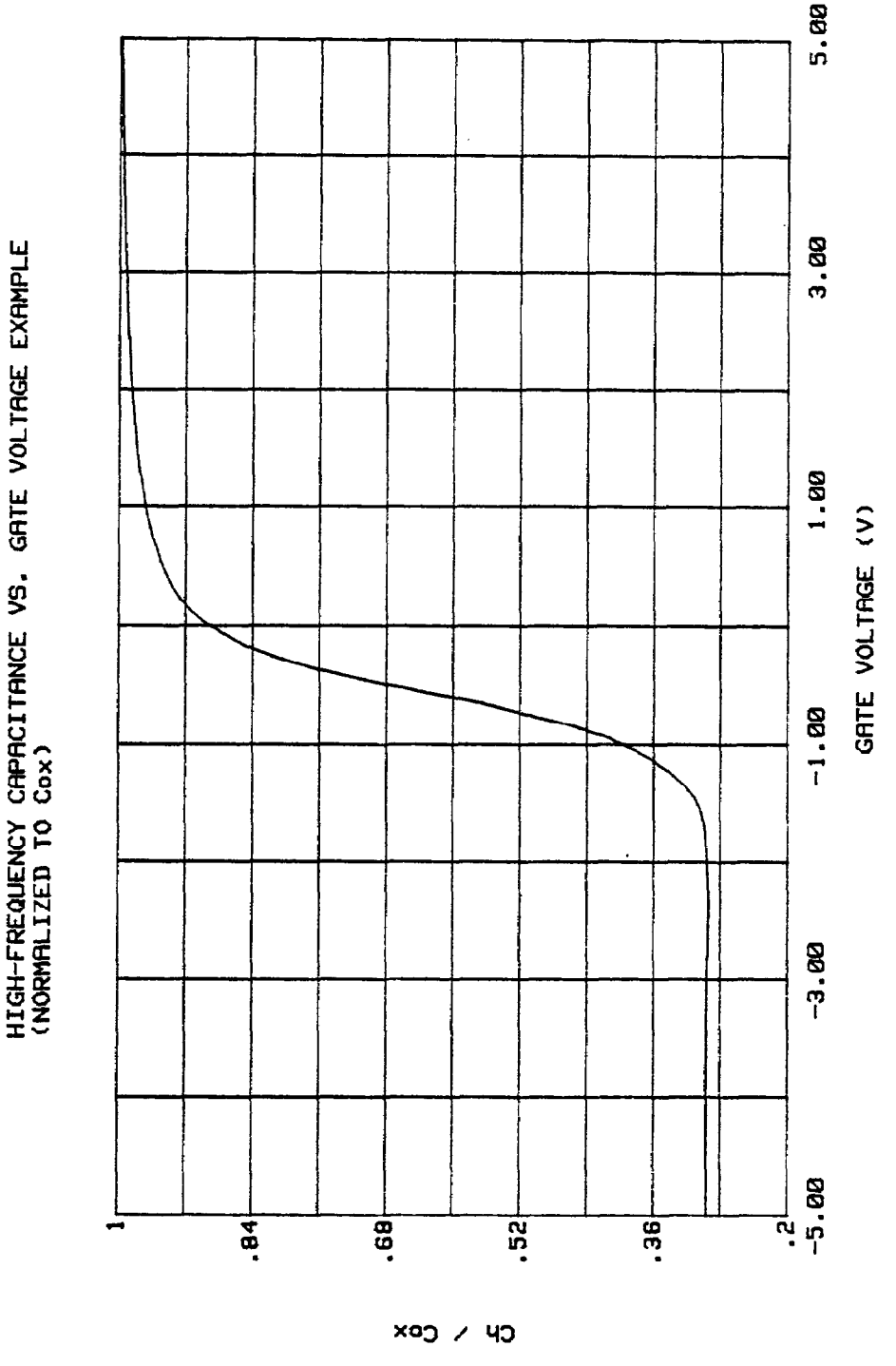
Note that adjusted C_Q and C_H are the values plotted.

Examples of these graphs are shown in Figures 4-9 through 4-13.



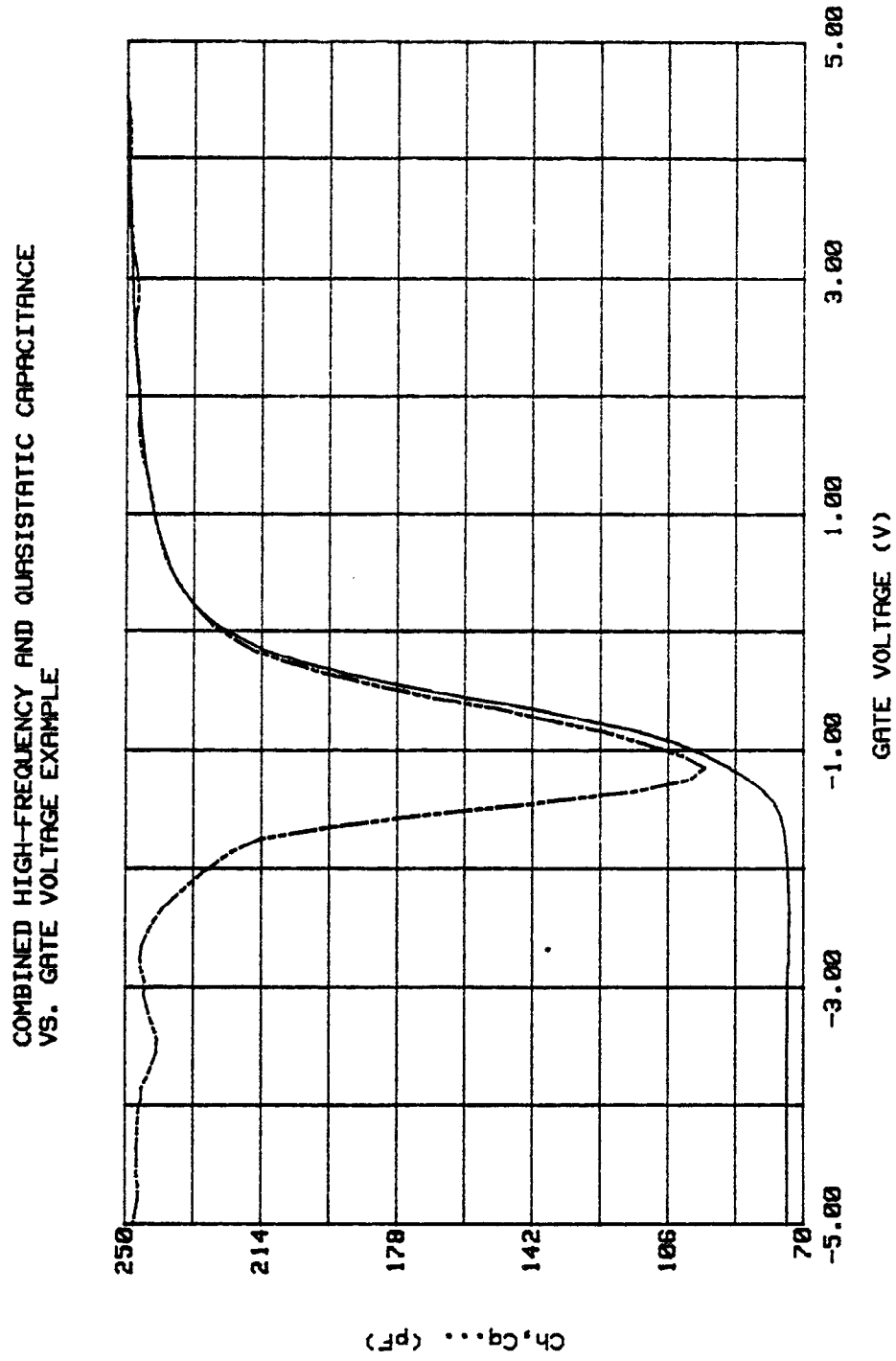
The curve data represents the low-frequency capacitance of the device under test including interface trap and inversion layer capacitance

Figure 4-9. Quasistatic Capacitance vs. Gate Voltage Example (Normalized to C_{ox})



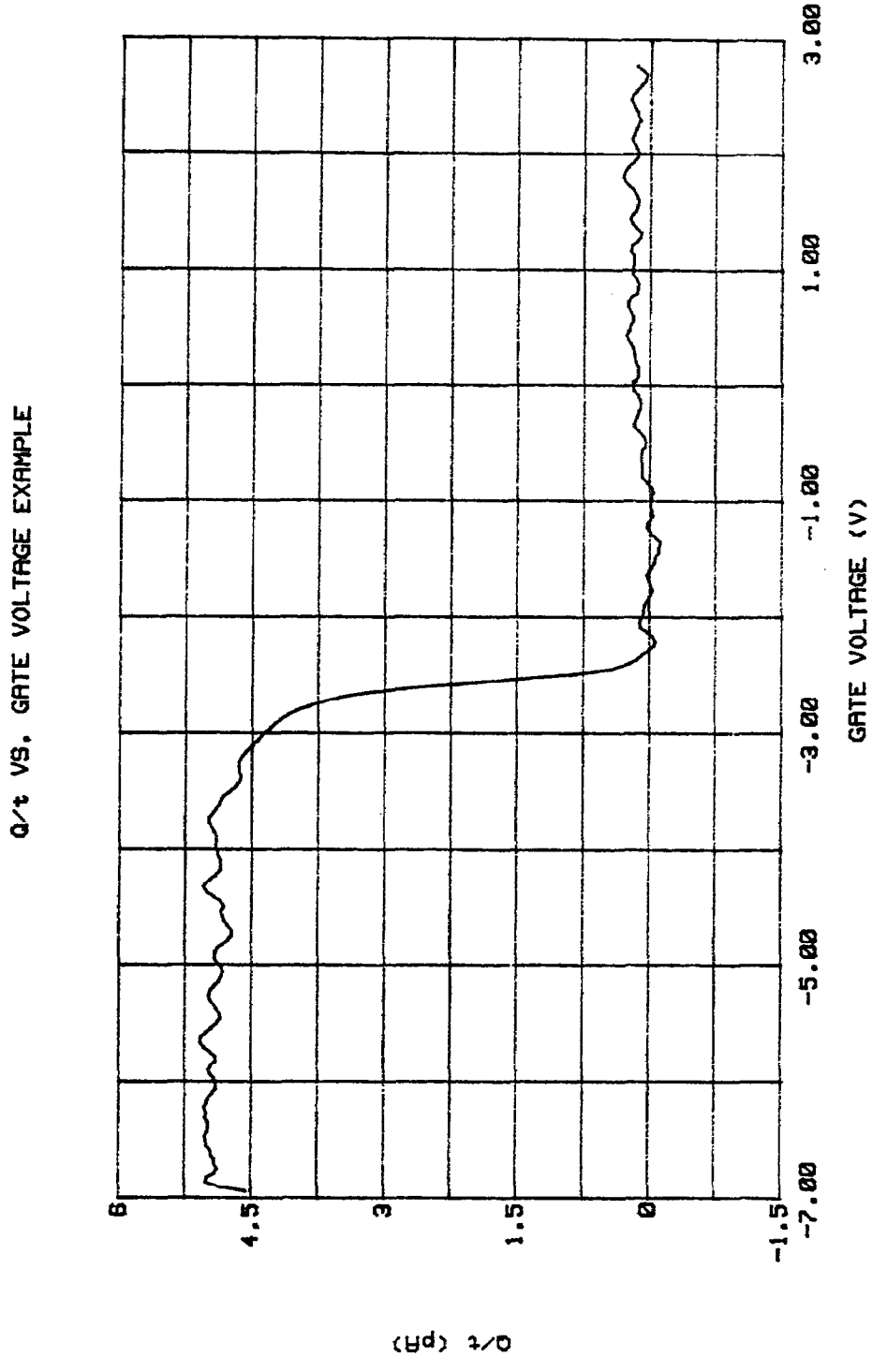
The curve data shows the high-frequency capacitance of the device under test. Interface traps and the inversion layer respond to the DC bias voltage, but do not follow the high-frequency AC test signal, resulting in reduced capacitance in inversion.

Figure 4-10. High-Frequency vs. Gate Voltage Example (Normalized to C_{ox})



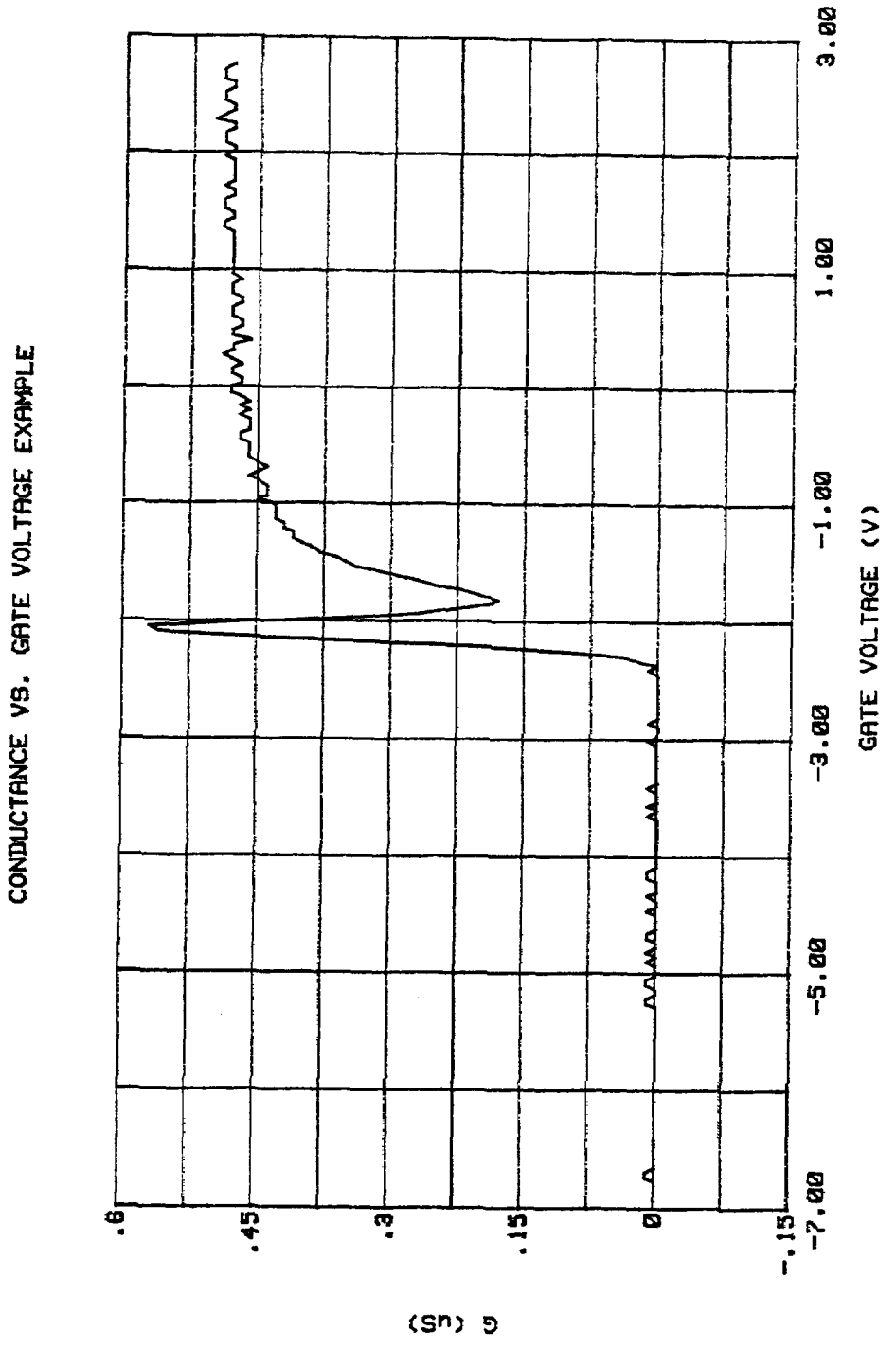
Curve differences result from such phenomena as interface charge trapping or inversion layer formation. Curve alignment errors caused by voltage stress, mobile ionic charge, and interface trap stretchout are minimized by simultaneous CV measurement.

Figure 4-11. High-Frequency and Quasistatic vs. Gate Voltage Example



Q/t vs. V_{GS} data provides an important method of ensuring that the device remains in equilibrium throughout the sweep. The curve shown demonstrates how the current flowing through the DUT rises sharply in inversion (V_T = −2.2V), a sign of nonequilibrium.

Figure 4-12. Q/t vs. Gate Voltage Example



A plot of 100kHz or 1MHz conductance vs. V_{ox} shows the conductance peak in the depletion region caused by lossy interface traps. Curve asymmetry results from high series resistance of the device under test.

Figure 4-13. Conductance vs. Gate Voltage Example

Table 4-3. Analysis Constants

Symbol	Description	Value
q	Charge on an electron	1.60219×10^{-19} Coul.
kT	Thermal energy at room temperature	4.046×10^{-21}J
ϵ_{ox}	Permittivity of SiO_2	3.4×10^{-13}F/cm
ϵ_S	Permittivity of silicon	1.04×10^{-12} F/cm
E_G	Energy gap of silicon	1.12eV
n_I	Intrinsic carrier concentration	1.45×10^{10} cm^{-3}

4.4.11. Doping Profile

Doping profile analysis includes graphing of depletion depth vs. gate voltage, doping concentration vs. depth, and $1/C^2$ vs. gate voltage, as discussed below.

Depletion Depth vs. Gate Voltage (w vs. V_{GS})

The Package 82 computes the depletion depth, w, from the high-frequency capacitance and oxide capacitance at each measured value of V_{GS} (Nicollian and Brews 386).

Depletion depth vs. gate voltage can be graphed by selecting the corresponding option on the analysis menu. In order to graph this function, the program computes each element of the w column of the calculated data array as shown below.

$$w = A\epsilon_S \frac{1}{C_H} - \frac{1}{C_{ox}}$$

Where: w = depth (μm)
ϵ_S = permittivity of silicon (1.04×10^{-12}F/cm)
C_H = high-frequency capacitance (pF)
C_{ox} = oxide capacitance (pF)
A = gate area (cm^2)

Figure 4-14 shows a typical example of a w vs. V_{GS} plot. The CV curves for the device are shown in Figure 4-11.

Doping Concentration vs. Depth (N vs. w)

The doping profile of the device is derived from the CV curve based on the definition of the differential capacitance (measured by the Models 590 and 595) as the differential change in depletion region charge produced by a differential change in gate voltage (Nicollian and Brews 380-389).

In order to correct for errors caused by interface traps, the error term $(1-C_Q/C_{ox})/(1-C_H/C_{ox})$ is included in the calculations as follows:

$$N = \frac{(-2\times10^{-24})\ [(1-C_Q/C_{ox})/(1-C_H/C_{ox})]}{A^2 q \epsilon_S \Delta(i)}$$

Where: N = doping concentration (cm^{-3})
C_Q = quasistatic capacitance (pF)
C_{ox} = oxide capacitance (pF)
C_H = high-frequency capacitance (pF)
A = gate area (cm^2)
q = electron charge (1.60219×10^{-19}C)
ϵ_S = permittivity of silicon (1.04×10^{-12}F/cm)
1×10^{-24} = units conversion factor

And:

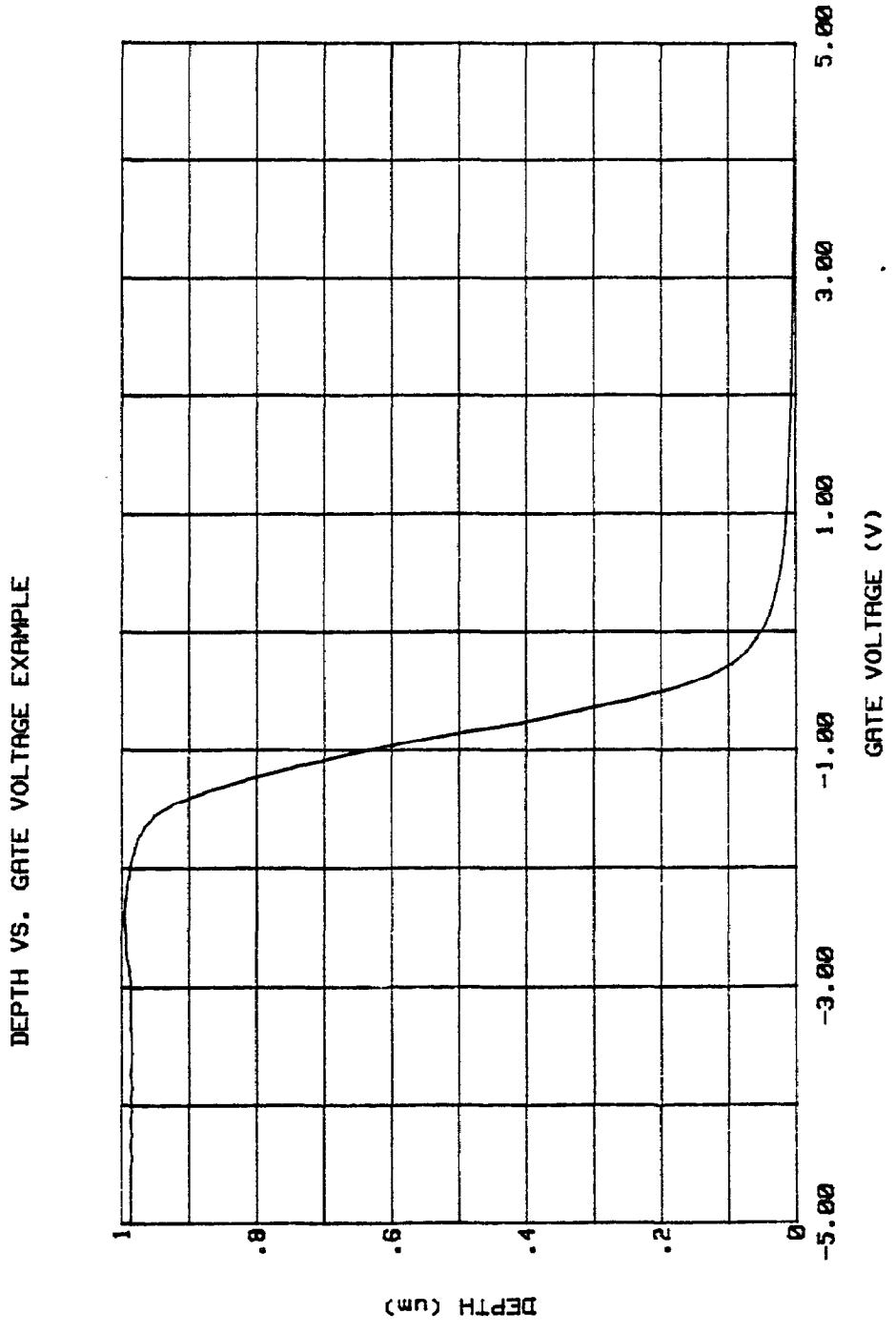
$$\Delta(i) = \frac{1/C_H^2(i+1) - 1/C_H^2(i)}{V_{GS}(i+1) - V_{GS}(i)} = \frac{\Delta(1/C_H^2)}{\Delta V_{GS}}$$

Figure 4-15 shows an example of a N vs. w graph. Figure 4-11 shows the CV curves of the DUT.

$1/C^2$ vs V_{GS}

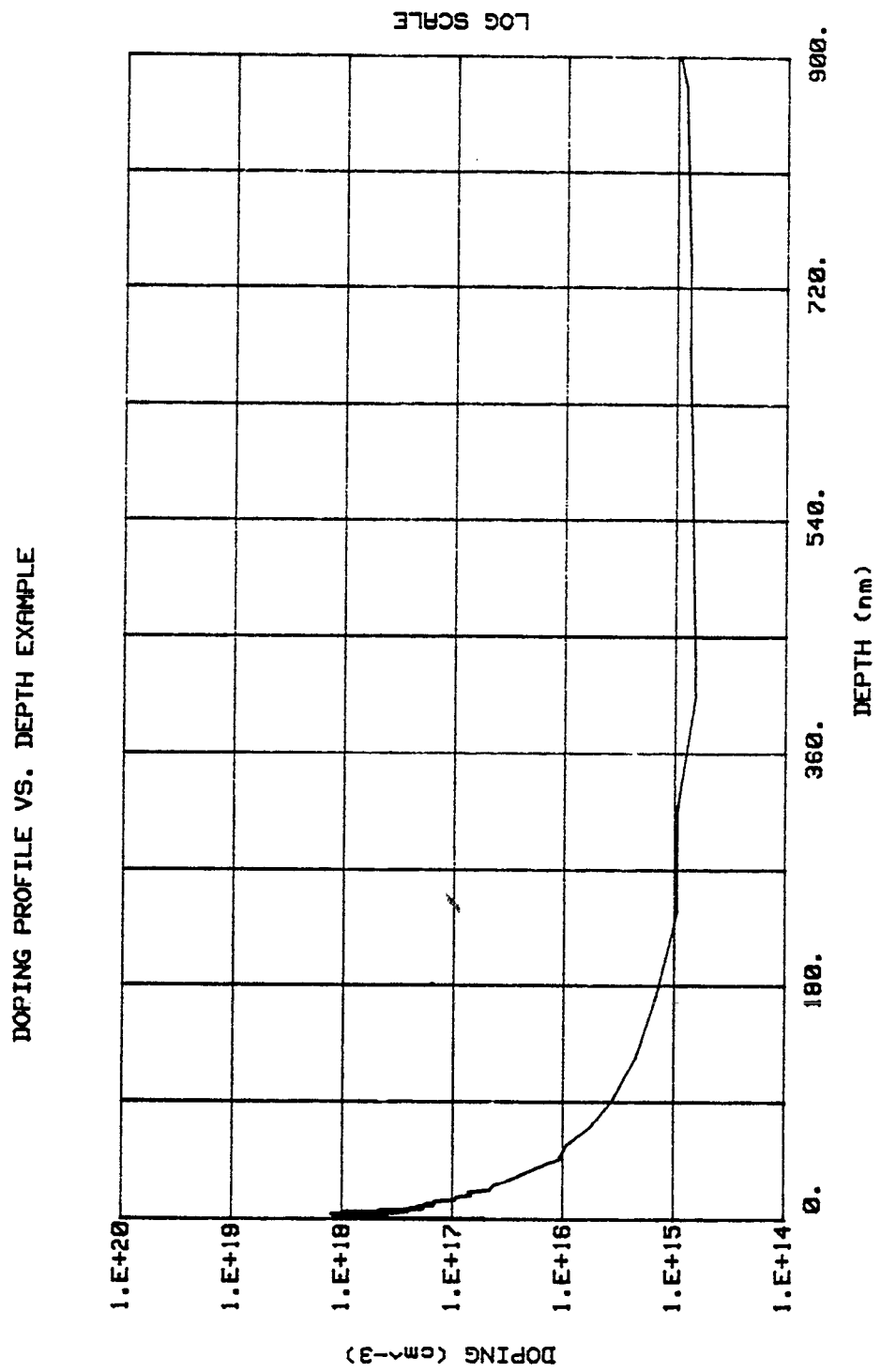
A $1/C^2$ graph can yield important information about doping profile. N is related to the reciprocal of the slope of the $1/C^2$ vs. V_{GS} curve, and the V intercept point is equal to the flatband voltage caused by surface charge and metal-semiconductor work function (Nicollian and Brews 385).

Figure 4-16 shows a typical $1/C^2$ vs. V_{GS} plot. Data for the plot is shown in Figure 4-11.



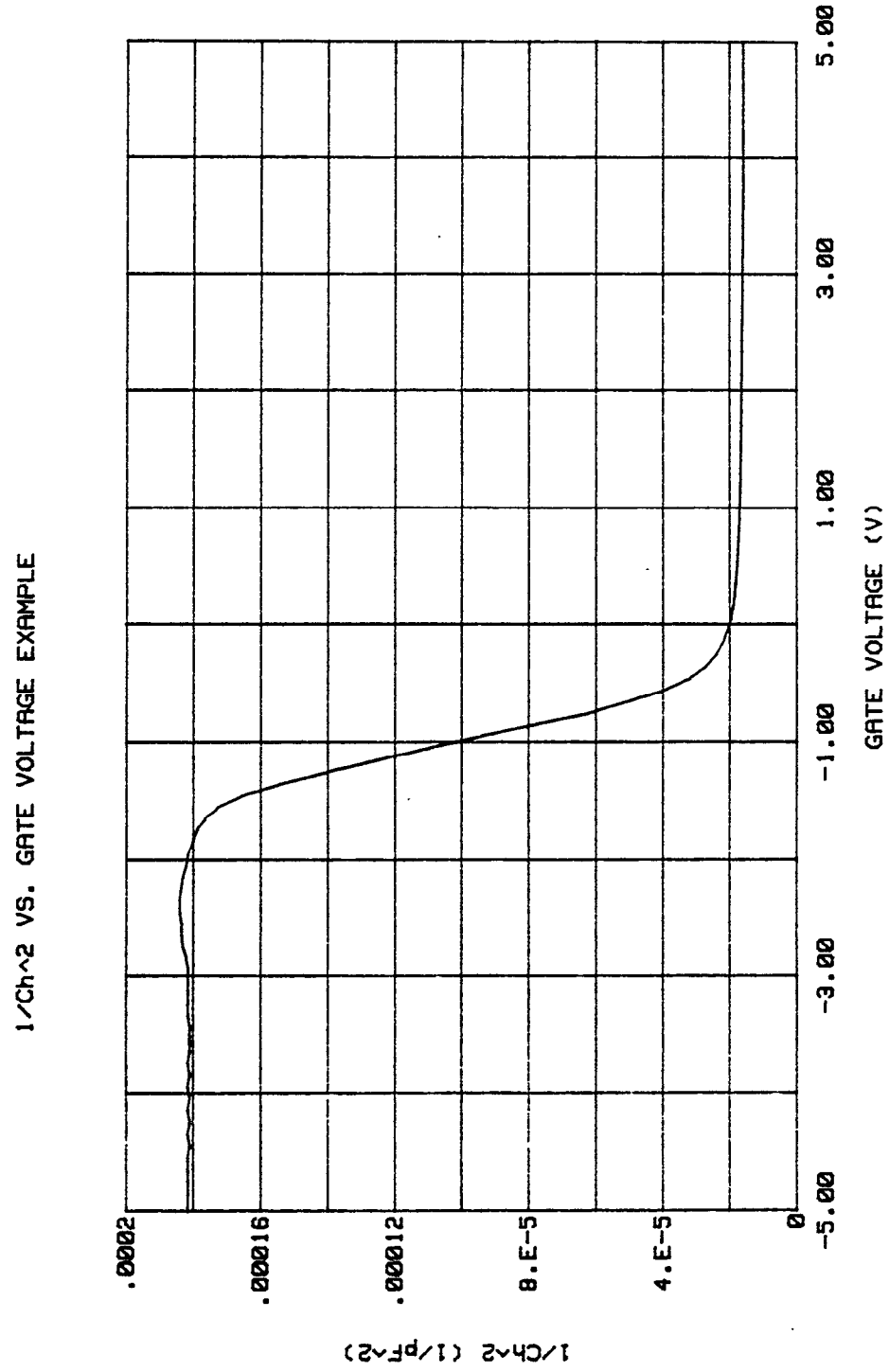
This curve demonstrates the formation of the depletion region at the onset of depletion, as well as its saturation at maximum depth at the point where the inversion layer forms.

Figure 4-14. Depth vs. Gate Voltage Example



The doping profile curve shows how the ionized purity density varies as a function of the depletion depth. Doping profile is calculated from both quasistatic and high-frequency capacitance in order to minimize errors caused by interface states.

Figure 4-15. Doping Profile vs. Depth Example



The shape of the curve is related to the doping profile in an MOS capacitor. The reciprocal of the slope of the curve at any point is proportional to the doping profile.

Figure 4-16. 1/Ch² vs. Gate Voltage Example

4.4.12 Flatband Capacitance

The Package 82 uses the flatband capacitance method of finding flatband voltage, V_{FB}. The Debye length is used to calculate the ideal value of flatband capacitance, C_{FB}. Once the value of C_{FB} is known, the value of V_{FB} is interpolated from the closest V_{GS} values (Nicollian and Brews 487-488).

The method used is invalid when interface trap density becomes very large ($10^{12}-10^{13}$ and greater). However, this algorithm should give satisfactory results for most users. Those who are dealing with high values of D_{IT} should consult the appropriate literature for a more appropriate method and modify the Package 82 software accordingly.

Based on doping, the calculation of C_{FB} uses N at 90% w_{MAX} or user-supplied N_A (bulk doping for p-type, acceptors) or N_D (bulk doping for n-type, donors).

C_{FB} is calculated as follows:

$$C_{FB} = \frac{C_{OX}\,\epsilon_S\,A/(1\times10^{-4})(L_B)}{(1\times10^{-12})(C_{OX})+\epsilon_S\,A/(1\times10^{-4})(L_B)}$$

Where: C_{FB} = flatband capacitance (pF)
C_{OX} = oxide capacitance (pF)
ϵ_S = permittivity of silicon (1.04×10^{-12}F/cm)
A = gate area (cm^2)
1×10^{-4} = units conversion for L_B
1×10^{-12} = units conversion for C_{OX}

And: L_B = extrinsic Debye length =

$$(1 \times 10^4)\sqrt{\frac{\epsilon_S kT}{q^2 N_X}}$$

Where: kT = thermal energy at room temperature (4.046×10^{-21}J)
q = electron charge (1.60219×10^{-19}C)
N_X = N at 90% w_{MAX} or N_A or N_D when input by the user.

N at 90% w_{MAX} is chosen to represent bulk doping.

To change the value of N to N_A or N_D, select "Display Analysis Constants" in the menu. Note that changing N forces a recalculation of ψ, E_T, and C_{FB}.

4.4.13 Interface Trap Density Analysis

Interface trap density graphical analysis tools include interface trap density vs. energy, band bending vs. voltage, as well both quasistatic and high-frequency capacitance vs. band bending. In addition, flatband voltage, which is necessary to determine band bending, is also calculated as part of the analysis operation.

The CV curve is transformed into a D_{IT} vs. E_T curve (Nicollian and Brews 319-325; Sze 379-390). This transformation is performed using the model shown in Sze (381) or Nicollian and Brews (Figure 8.1 and 8.3). The interface capacitance, C_{IT}, is the only element not in common between Figures 8.1 and 8.3 (Nicollian and Brews). However, by measuring both quasistatic and high-frequency capacitance, we can calculate its value, as discussed below.

Band Bending vs. Gate Voltage (ψ_S vs. V_{GS})

As a preliminary step, surface potential ($\psi_S - \psi_O$) vs. V_{GS} is calculated with the results placed in the ψ_S column of the array. Surface potential is calculated as follows:

$$(\psi_S-\psi_O) = \sum_{V_{GS}\#1}^{V_{GS}\text{Last}} (1-C_Q/C_{OX})(2V_{STEP})$$

Where: $(\psi_S-\psi_O)$ = surface potential (V)
C_Q = quasistatic capacitance (pF)
C_{OX} = oxide capacitance (pF)
V_{STEP} = step voltage (V)
V_{GS} = gate-substrate voltage (V)

Note that the $(\psi_S-\psi_O)$ value is accumulated as the column is built, from the first row of the array (V_{GS} #1) to the last array row (V_{GS} last). The number of rows will, of course, depend on the number of readings in the sweep, which is determined by the Start, Stop and Step voltages.

Once $(\psi_S-\psi_O)$ values are stored in the array, the value of $(\psi_S-\psi_O)$ at the flatband voltage is used as a reference point and is set zero by subtracting that value from each entry in the $(\psi_S-\psi_O)$ column, changing each element in the column to ψ_S. The value of ψ_O is interpolated as discussed below.

Once band bending voltage is known, graphs of ψ_S vs. V_{GS}, C_Q vs. ψ_S, and C_H vs ψ_S can be generated. Examples are shown in Figures 4-17 through 4-19. Again, CV curves for the device are shown in Figure 4-11.

V_{FB} and ϕ_0 Interpolation

The program determines flatband voltage, V_{FB}, by locating the V_{GS} point where C_H approximately equals C_{FB}. V_{FB} is then interpolated from the closest V_{GS} values.

A straight line interpolation from the previous or following data points is used, and the interpolated V_{FB} and ϕ_0 points are computed.

Interface Trap Density vs. Energy from Midgap (D_{IT} vs E_T)

Interface trap density is calculated from C_{IT} as shown below (Nicollian and Brews 322).

$$C_{IT} = \frac{1}{(1/C_Q - 1/C_{OX}) - (1/C_H - 1/C_{OX})}$$

And:

$$D_{IT} = \frac{(1 \times 10^{-12})\, C_{IT}}{Aq}$$

Where: C_{IT} = interface trap capacitance (pF)
D_{IT} = interface trap density ($cm^{-2}\ eV^{-1}$)
C_Q = quasistatic capacitance (pF)
C_H = high-frequency capacitance (pF)
C_{OX} = oxide capacitance (pF)
A = gate area (cm^2)
q = electron charge (1.60219×10^{-19}C)
1×10^{-12} = units conversion for C_{IT}

The results are stored in the D_{IT} column of the array as calculated.

Interface trap energy from midgap, E_T, is computed from ψ_S offset by bulk potential, ϕ_B as follows:

$$\psi_S - \phi_B - E_T$$

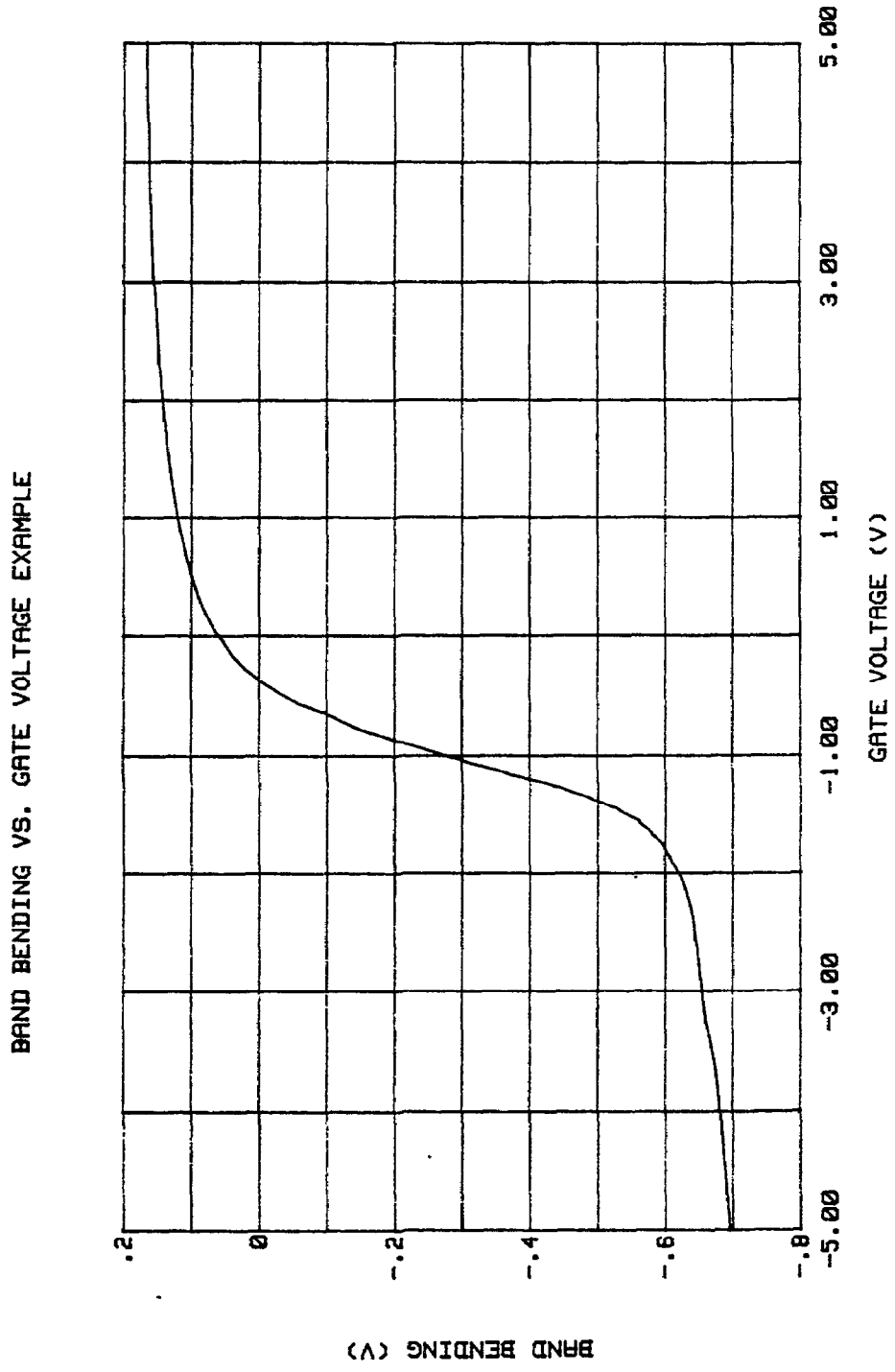
Where: ψ_S = band bending (V)
E_T = interface trap energy from midgap (eV)

And:

$$\phi_B = \frac{kT}{q} \ln\left(\frac{N_X}{n_I}\right)$$

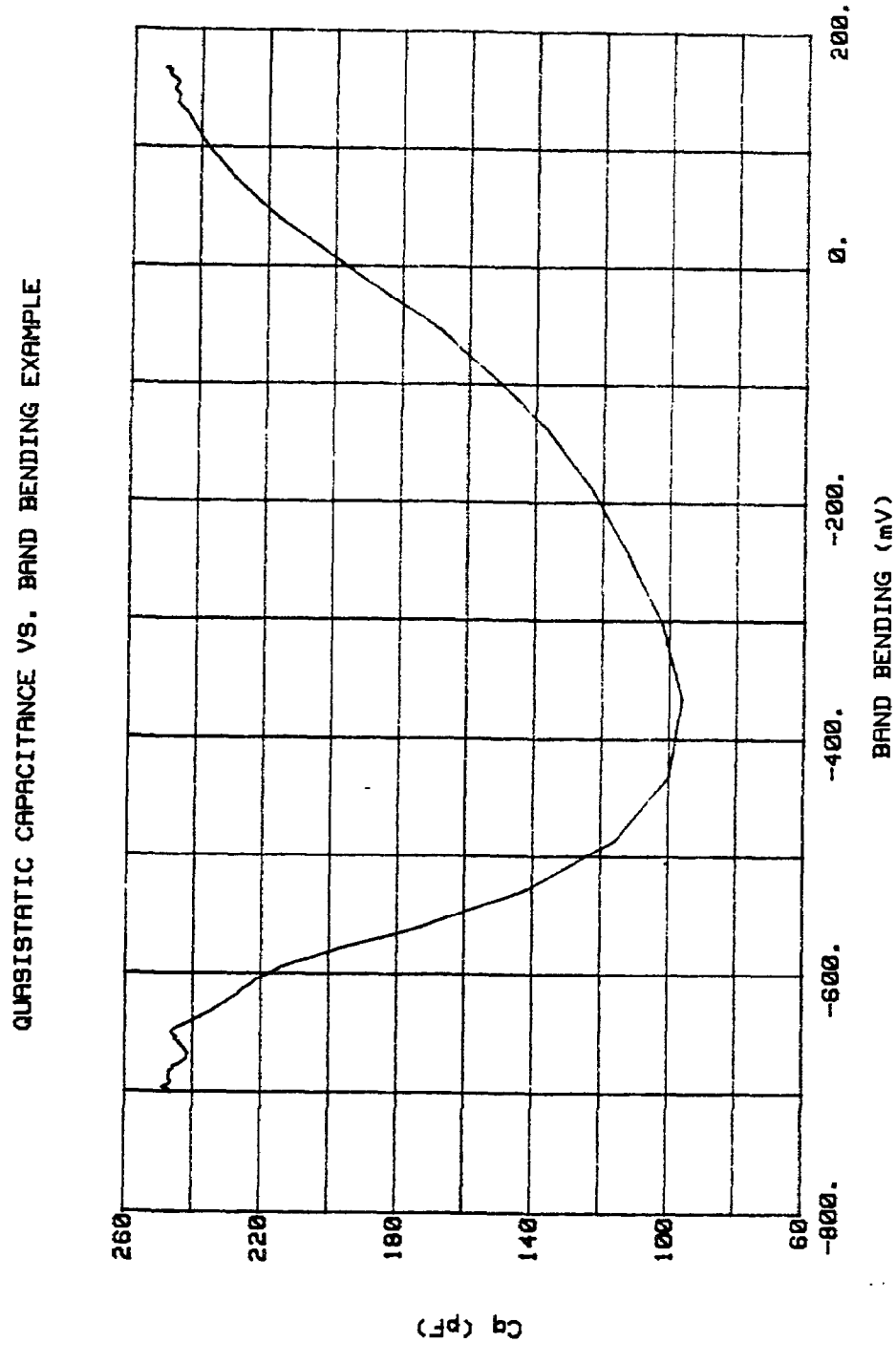
Where: ϕ_B = bulk potential (eV)
kT = thermal energy at room temperature (4.046×10^{-21}J)
n_I = intrinsic carrier concentration in silicon ($1.45 \times 10^{10} cm^{-3}$)
N_X = N at 90% w_{MAX}, or N_A or N_D if entered by the user

A typical example of a D_{IT} vs. E_T plot is shown in Figure 4-20.



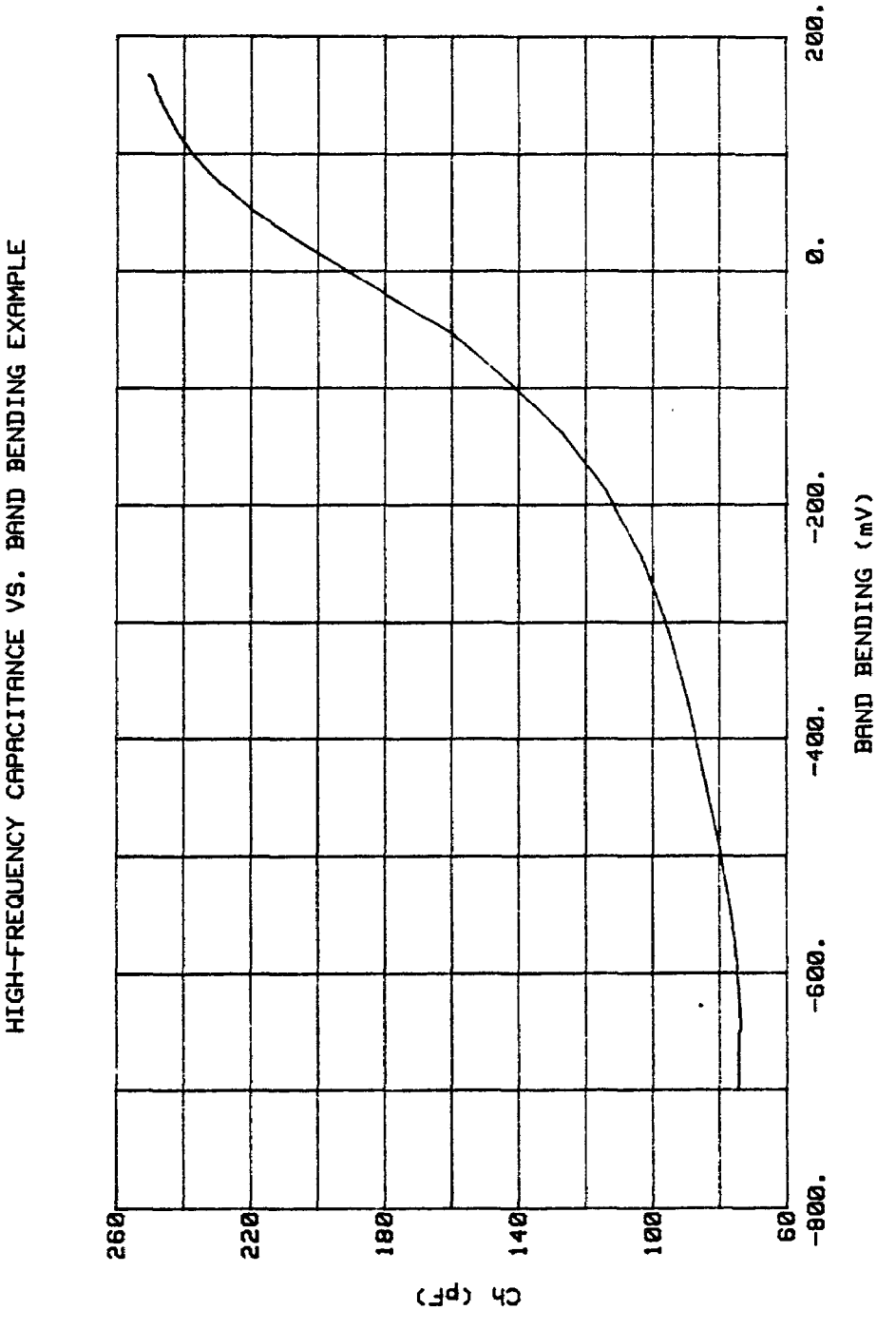
The ψ_s vs. V_{GS} curve aids in understanding how changes in bias voltage affect the device under test. The accumulation, depletion, and inversion regions of a CV curve are defined by three specific values of band bending voltage: zero (flatbands), equal to the bulk potential, and twice the bulk potential ($V_{THRESHOLD}$).

Figure 4-17. Band Bending vs. Gate Voltage Example



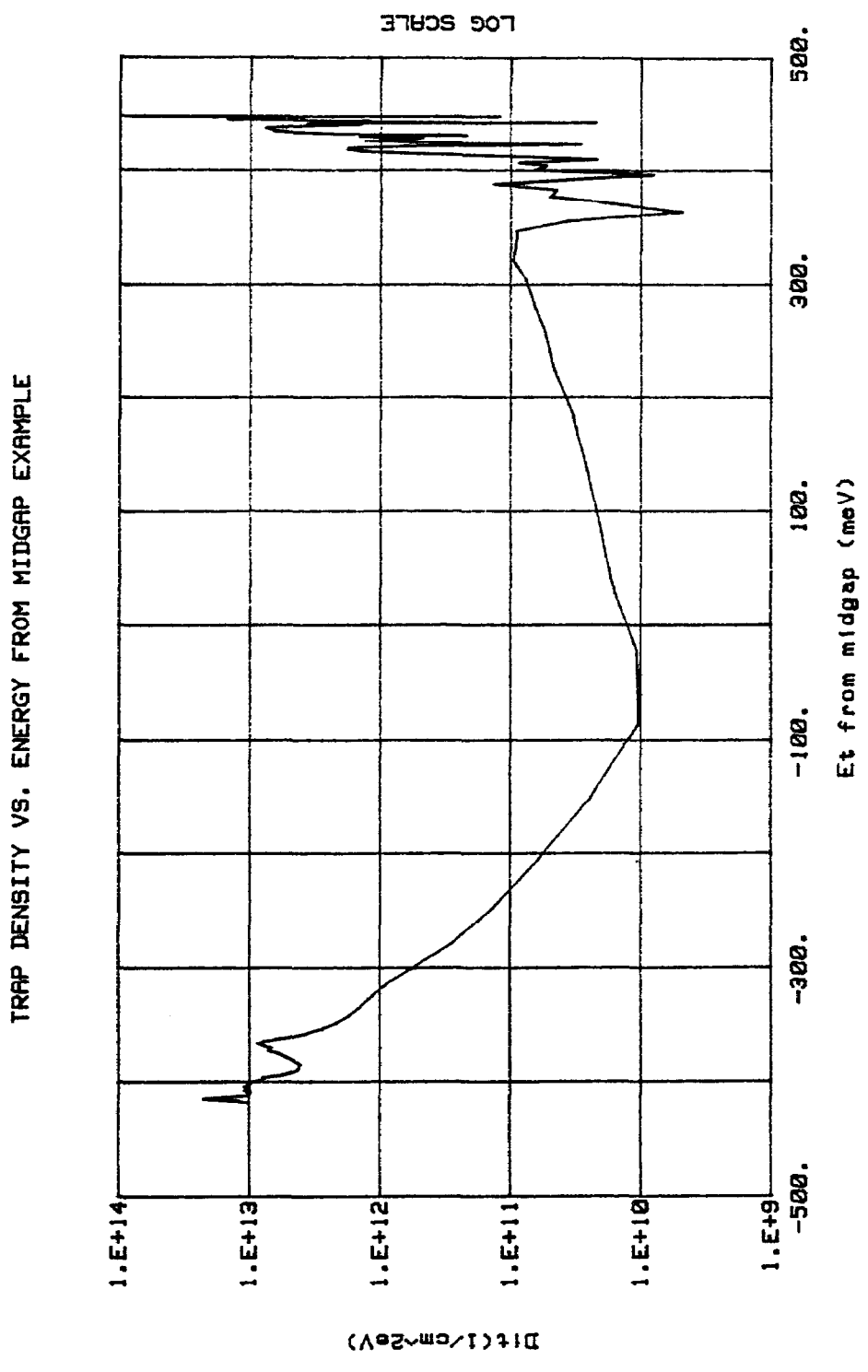
The C_Q vs. ψ_s curve aids in comparing Package 82 curves with previously-taken, manually-aligned curves.

Figure 4-18. Quasistatic Capacitance vs. Band Bending Example



The C_H vs. ψ_s curve also aids in comparing to previously taken data.

Figure 4-19. High-Frequency Capacitance vs. Band Bending Example



The D_{IT} vs. E_T curve indicates the quality of the $Si-SiO_2$ interface.

Figure 4-20. Interface Trap Density vs. Energy from Midgap Example

4.4.14 Calculated Accuracy of N and D_{IT}

The calculated values of N and D_{IT} have a nominal error of $<\pm 5\%$ when the depletion depth, w , falls within the following limits:

$$3L_D \leq w \leq 2L_D \sqrt{\ln (N_X/n_i)}$$

Where: L_D = extrinsic Debye length (see above)
w = depletion depth (μm)
N_X = N at 90% w_{MAX} , N_A , or N_D
n_i = intrinsic carrier concentration ($1.45 \times 10^{10} cm^{-3}$)

This accuracy range is displayed as best depth under option 4, Display Analysis Constants under the analysis menu.

NOTE

In order to set the graphics window to the range of best depth, select option 3 on the analysis menu followed by option 5 on the subsequent menu. Type in window limits equal to displayed best depth. Reading numbers for best depth are shown in the graphics range selection menu.

4.5 MOBILE IONIC CHARGE CONCENTRATION MEASUREMENT

Mobile ionic charge concentration in the oxide of an MOS device must be carefully controlled during the manufacturing process. Sodium ion concentrations are particularly important because of their abundance in the environment and the fact that they move rapidly through the oxide.

The following paragraphs discuss two methods for measuring mobile ionic charges in the oxide: the flatband voltage shift method, and the triangular voltage sweep (TVS) method.

4.5.1 Flatband Voltage Shift Method

The primary method for measuring oxide charge density is the flatband voltage shift or temperature-bias stress method (Snow et al). In this case, two high-frequency CV curves are measured, both at room temperature. Between the two curves, the device is biased with a voltage at 200-300°C to drift mobile ions across the oxide. The flatband voltage differential between the two curves is then calculated, from which charge density can be determined.

Procedure

1. Using the Package 82 or the separate Model 590 program, measure a high-frequency CV curve of the device at room temperature.
2. Note the flatband voltage, V_{FB} , as calculated and displayed by the program (select Display Analysis Constants on the analysis menu).
3. Raise the temperature of the DUT to 200-300°C, and apply a bias voltage of 10-20V for 3-10 minutes.
4. Return the device to room temperature and remove the bias voltage.
5. Measure a second CV curve of the device at room temperature.
6. Display the flatband voltage by selecting the Display Analysis Constants on the analysis menu.
7. Subtract value of V_{FB} obtained in step 6 from the value in step 2 to determine ΔV_{FB} .

Calculation

From Nicollian and Brews (426, Eq. 10.9 and 10.10), we have:

$$V_{FB} - W_{MS} = \frac{\overline{x}Q_0}{\epsilon_{ox}} = \frac{\overline{x}Q_0}{x_0 C_{ox}}$$

Where: $\overline{x}Q_0$ = the first moment of the charge distribution
$\overline{x}$ = charge centroid
W_{MS} = metal semiconductor work function (constant)
ϵ_{ox} = oxide dielectric constant
x_0 = oxide thickness
C_{ox} = oxide capacitance

So that:

$$\Delta V_{FB} = \Delta(V_{FB} - W_{MS})$$
$$= \Delta\left(\frac{\overline{x}Q_0}{\epsilon_{ox}}\right)$$
$$= \frac{Q_0}{C_{ox}} \Delta \left(\frac{\overline{x}}{x_0}\right)$$

For the common case of thermally-grown oxide, $\overline{x}$(before)= x_0 and $\overline{x}$(after)=0, so that

$$\Delta V_{FB} = \frac{-Q_0}{C_{ox}}$$

where Q_0 is the effective charge. Divide Q_0 by the gate area to obtain mobile ion charge density per unit area.

4.5.2 Triangular Voltage Sweep Method

A second but less familiar way to measure oxide charge density is the triangular voltage sweep (TVS) method (Nicollian and Brews 435-440). There are four key advantages of the TVS method over the CV method including:

1. Mobile ion density measurements are accurate even in cases where interface trap density levels vary substantially.
2. Different mobile ion species such as sodium and potassium can be distinguished from one another.
3. Greater sensitivity allowing low ion densities to be detected.
4. Greater speed because only one curve is required, in addition to the fact that the device can remain heated for several measurements.

Procedure

1. Load the "M595CV" program into the computer.
2. Connect the Model 595 to the test fixture containing the device under test.
3. Raise the temperature of the device to a temperature of 300°C and maintain the DUT at that temperature throughout the test.
4. Perform a quasistatic measurement by sweeping from $-V_{GS}$ to $+V_{GS}$ at the required amplitudes. Keep in mind that Step V must be low enough and T delay must be long enough so that $C_Q \cong C_{OX}$ in the absence of mobile ions.
5. Display or print out the reading array to obtain the C_Q and V_{GS} values. Calculations can be performed as outlined below.

Calculations

Although the method presented here was originally developed for the ramp technique of quasistatic measurement, the Model 595 is used to make the necessary measurement. The end result is the same: the area between the measured capacitance curve and C_{OX} indicates the charge density as shown.

$$\sum_{-V_{GS}}^{+V_{GS}} (C_{MEAS} - C_{OX})\Delta V_{GS} = qN_M \left[\frac{\overline{x}(V_{GS})}{X_0} - \frac{\overline{x}(-V_{GS})}{X_0} \right]$$

Where: V_{GS} = gate-substrate voltage
ΔV_{GS} = change in gate substrate voltage (V step)
C_{MEAS} = quasistatic capacitance measured by 595
C_{OX} = oxide capacitance
q = electron charge
N_M = mobile ion density
$\overline{x}$ = charge centroid
x_0 = oxide thickness
Q_0 = mobile ion charge

or, for the case of thermally-grown oxide, the above reduces to:

$$\sum_{-V_{GS}}^{+V_{GS}} (C_{MEAS} - C_{OX})\,\Delta V_{GS} = -Q_0$$

Proof of Measurement Method

An adaptation of the proof by Nicollian and Brews (437) follows. This proof describes the validity of the feedback charge technique as applied to the TVS method for measuring oxide charge density.

Objective:

To demonstrate that mobile ion density drift at a given temperature is proportional to the area under the peak in a quasistatic CV curve caused by ionic motion as shown below.

Assumptions:

1. Temperature is high enough (≅300°C) and the staircase is slow enough (≤100mV/sec) so that $C_Q \cong C_{OX}$ in the absence of mobile ions.
2. ΔV_{GS} is in the small signal range.

Model:

The model for the derivation of proof is shown in Figure 4-21.

Derivation:

The gate charge, Q_G, is made up of the following:

$$Q_G = -Q_M + Q_{OT} - Q_F - Q_{IT} - Q_S \quad (1)$$

Where: Q_G = gate charge
Q_{OT} = oxide trapped charge
Q_M = mobile ionic charge
Q_F = fixed oxide charge
Q_{IT} = interface trapped charge
Q_S = space charge

The amounts of Q_M, Q_{OT}, and Q_F are fixed, although the distribution may change, so that,

$$\Delta Q_G = -\Delta Q_{IT} - \Delta Q_S \quad (2)$$

In equilibrium,

$$-\Delta Q_{IT} = C_{IT}(\psi_S)\,\Delta\psi_S \quad (3)$$

and,

$$-\Delta Q_S = C_S(\psi_S)\,\Delta\psi_S \quad (4)$$

Thus, from (2), (3), and (4), we have,

$$\Delta Q_G = (C_{IT} + C_S)\,\Delta\psi_S \quad (5)$$

From Gauss's law on the Model in Figure 4-21,

$$\begin{aligned}(C_{IT} + C_S)\,\Delta\psi_S &= C_{OX}\,[\Delta(V_{GS} - V_{FB}) - \Delta\psi_S] \\ &= C_{OX}\,\Delta(V_{GS} - V_{FB}) - C_{OX}\,\Delta\psi_S \end{aligned} \quad (6)$$

Rearranging (6) gives,

$$\Delta\psi_S = \Delta(V_{GS} - V_{FB})\,\frac{C_{OX}}{C_{OX} + C_{IT} + C_S} \quad (7)$$

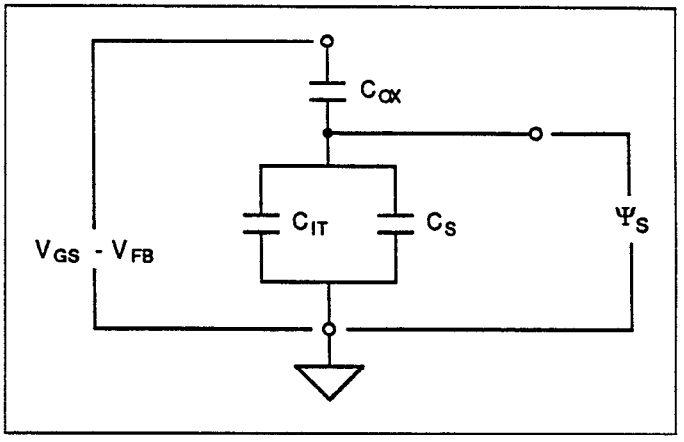


Figure 4-21. Model for TVS Measurement of Oxide Charge Density

In equilibrium for the model, C_Q is

$$C_Q = C_{ox}\,\frac{C_S + C_{IT}}{C_{ox} + C_S + C_{IT}} \quad (8)$$

Combining (7) and (8) we have,

$$\Delta\psi_S = \Delta(V_{GS} - V_{FB})\,\left(\frac{C_Q}{C_S + C_{IT}}\right) \quad (9)$$

From assumption (1), $C_Q \cong C_{OX}$, so that

$$\Delta\psi_S \cong \Delta(V_{GS} - V_{FB})\,\left(\frac{C_{OX}}{C_S + C_{IT}}\right) \quad (10)$$

Rearranging (10) results in:

$$(C_{IT} + C_S)\,\Delta\psi_S = C_{OX}\,\Delta(V_{GS} - V_{FB}) \quad (11)$$

Using (5) and (11), and,

$$C_{MEAS} = \frac{\Delta Q_G}{\Delta V_{GS}}$$

we derive,

$$C_{MEAS}\,\Delta V_{GS} = \Delta Q_G = C_{OX}\,\Delta(V_{GS} - V_{FB}) \quad (12)$$

Rearranging (12) yields:

$$(C_{MEAS} - C_{OX})\,\Delta V_{GS} = -\,C_{OX}\,\Delta V_{FB} \quad (13)$$

From assumption 2, ΔV_{GS} is in the small signal range. If we staircase the bias voltage from $-V_{GS}$ to $+V_{GS}$, we have from (13):

$$\sum_{-V_{GS}}^{V_{GS}} (C_{MEAS} - C_{OX})\,\Delta V_{GS} = -\,C_{OX} \sum_{-V_{GS}}^{V_{GS}} \Delta V_{FB}$$

(C_{OX} is a constant) (14)

The lefthand side of (14) represents the area under the curve caused by ionic motion:

$$\sum_{-V_{GS}}^{V_{GS}} (C_{MEAS} - C_{OX})\,\Delta V_{GS} = \sum_{-V_{GS}}^{V_{GS}} C_{MEAS}\,\Delta V_{GS} - \sum_{-V_{GS}}^{V_{GS}} C_{OX}\,\Delta V_{GS} \quad (15)$$

Area under CV curve peak caused by ionic motion

Area under curve with ionic motion

Area under curve without ionic motion

Now consider the right hand side of (14):

$$-C_{OX} \sum_{-V_{GS}}^{V_{GS}} \Delta V_{FB}$$

From Nicollian and Brews (426, Eq. 10.9):

$$V_{FB} - W_{MS} = \frac{\overline{x}Q_o}{\epsilon_{ox}} \quad (16)$$

Where:

W_{MS} = work function ($\Delta W_{MS} = 0$)
$\overline{x}Q_0$ = first moment of charge distrubution
$\overline{x}$ = charge centroid
ϵ_{ox} = dielectric constant of oxide

Thus, we have,

$$\Delta(V_{FB} - W_{MS}) = \Delta\left(\frac{\overline{x}Q_o}{\epsilon_{ox}}\right) \quad (17)$$

but W_{MS}, Q_o, and ϵ_{ox} are constants, so:

$$\Delta V_{FB} = \frac{Q_o}{\epsilon_{ox}}\,\Delta\overline{x} \quad (18)$$

Since,

$$Q_o = qN_{M'}$$

$$\Delta V_{FB} = \frac{qN_M}{\epsilon_{ox}}\,\Delta\overline{x} \quad (19)$$

Where:

N_M = mobile ionic charge density.

Combining (19) with (14), we have:

$$\sum_{-V_{GS}}^{V_{GS}} (C_{MEAS} - C_{OX})\,\Delta V_{GS} = -\,C_{OX}\,\frac{qN_M}{\epsilon_{ox}} \sum_{-V_{GS}}^{V_{GS}} \Delta\overline{x}$$

(C_{OX} is a constant) (20)

From Nicollian and Brews (426, Eq. 10.10),

$$C_{OX} = \frac{\epsilon_{ox}}{x_o}$$

and defining $\overline{x}(-V_{GS})$ and $\overline{x}(V_{GS})$ as $\overline{x}$ at $-V_{GS}$ and $+V_{GS}$ respectively, we conclude:

$$\sum_{-V_{GS}}^{V_{GS}} (C_{MEAS} - C_{OX})\,\Delta V_{GS} = -qN_M \left[\frac{\overline{x}(V_{GS})}{x_o} - \frac{\overline{x}(-V_{GS})}{x_o}\right] \quad (21)$$

Area under CV curve peak caused by ionic motion

Mobile ion density drifted at given temperature

Conclusion: Equation 21 demonstrates the validity of the $C_{MEAS} = \Delta Q_G/\Delta V_{GS}$ method for the TVS measurement of mobile ion drift.

4.5.3 Using Effective Charge to Determine Mobile Ion Drift

The flatband voltage method of determining mobile ion drift discussed in paragraph 4.5.1 can be simplified by using Q_{EFF} to determine the ion charge. The basic procedure is as follows:

1. Using the Package 82 or separate Model 590 program, measure a high-frequency CV curve of the device at room temperature.
2. Note the effective charge, Q_{EFF}, as calculated and displayed by the program (select Display Analysis Constants on the analysis menu).
3. Raise the temperature of the DUT to 200 - 300°C, and apply a bias voltage of 10-20V for 2-10 minutes.
4. Return the device to room temperature and remove the bias voltage.
5. Measure a second CV curve of the device at room temperature.
6. Display the effective oxide charge by selecting Display Analysis Constants on the analysis menu.
7. Subtract the value of Q_{EFF} obtained in step 6 from that obtained in step 2 to determine the effective mobile ion charge density. Note that this procedure assumes the simple case of mobile ions drifting completely across the oxide in a thin sheet. See paragraph 4.5.1 for a description of the general case.

4.6 REFERENCES AND BIBLIOGRAPHY OF CV MEASUREMENTS AND RELATED TOPICS

4.6.1 References

The references below are cited in Section 4.

1. Nicollian, E.H. and Brews, J.R., MOS Physics and Technology. Wiley, New York (1982).
2. Sze, S.M., Physics of Semiconductor Devices, 2nd edition. Wiley, New York (1985)
3. Snow, E.H, Grove, A.S, Deal, B.E., and Sah, C.T. J., "Ionic Transport Phenomena in Insulating Films", Appl. Phys., 36, 1664 (1965)

4.6.2 Bibliography of CV Measurements and Related Topics

I. Texts:

A. Grove, A.S., Physics and Technology of Semiconductor Devices. Wiley, New York (1967).

B. Sze, S.M., Semiconductor Devices, Physics and Technology. Wiley, New York (1985).

II. Articles and Papers:

A. Feedback Charge Method

1. Mego, T.J. "Improved Feedback Charge Method for Quasistatic CV Measurements in Semiconductors". Rev. Sci. Instr. 57, 11 (1986).
2. Mego, T.J. "Improved Quasistatic CV Measurement Method for MOS". Solid State Technology, 29, 11, S19-21 (1986).
3. Markgraf, W., Baumann, M., Beyer, A., Arst, P., Rennau, M., "Nutzung der statischen CU-Methode im Rahmen eines mikrorechnergesteuerten MOS-Messplatzes", Phys. d. Halbleiteroberflaeche. 15, 73 (1984).

B. Q-V/Static Method

1. Ziegler, K. and Klausmann, E., "Static Technique for Precise Measurements of Surface Potential and Interface State Density in MOS Structures", Appl.Phys. Lett. 26, 400 (1975).

2. Kirov, K., Alexsandrova, S. and Minchev, G., "Error in Surface State Determination Caused by Numerical Differentiation of Q-V Data", Solid State Electronics. **18**, 341 (1978).

C. Q-C Method and Simultaneous High-Low Frequency CV

1. Nicollian, E.H. and Brews, J.R., "Instrumentation and Analog Implementation of the Q-C Method for MOS Measurements", Solid State Electronics. **27**, 953 (1984).
2. Boulin, D.M., Brews, J.R. and Nicollian, E.H., "Digital Implementation of the Q-C Method for MOS Measurements", Solid State Electronics. **27**, 977 (1984).
3. Derbenwick, G.F., "Automated C-V and |Y|-w Curves for MOS Device Analysis", Sandia Report SAND80-1308 (1982).
4. Lubzens, D., Kolodny, A., and Shacham-Diamond, Y.J., "Automated Measurement and Analysis of MIS INterfaces in Narrow-Bandgap Semiconductors,", IEEE transactions on Electron Devices, ED-28, 5 (1981).

D. Ramp Method

1. Kuhn, M., "A Quasistatic Technique for MOS C-V and Surface State Measurements", Solid State Electronics. **13**, 873 (1970).
2. Castagne, R., "De'termination de la densite' d'e'tats lents d'une capacite' me'tak-isolant semiconducteur par l'e'tude de la charge sous une tension croissant line 'airement", C.R.Acad. Sci. **267**, 866 (1968).
3. Kerr, D.R., "MIS Measurement Technique Utilizing Slow Voltage Ramps", Int.Conf.Properties and Use of MIS Structures, Grenoble, France, 303 (1969).
4. Castagne, R. and Vapaille, A., "Description of the SiO_2-Si Interface Properties by Means of Very Low Frequency MOS Capacitance Measurements", Surface Science, **28**, 157 (1971).
5. Kuhn, M. and Nicollian, E.H., "Nonequilibrium Effects in Quasi-static MOS Measurements", J.Electrochem.Soc., **118**, 373 (1971).
6. Lopez, A.D., "Using the Quasistatic Method for MOS Measurements", Rev.Sci.Instr. **44**, 200 (1973).

E. Interface States/Doping Profiles

1. Berglund, C.N., "Surface States at Steam-Grown Silicon-Silicon Dioxide Interfaces", IEEE Trans.Electron.Dev., **13**, 701 (1966).
2. DeClerck, G., "Characterization of Surface States at the Si-SiO_2 Interface", Nondestructive Evaluation of Semiconductor Materials and Devices (J.N. Zemel, ed.) Plenum Press, New York, p. 105 (1979).
3. Brews, J.R., "Correcting Interface-State Errors in MOS Doping Profile Determinations", J.Appl.Phys. **44**, 3228 (1973).
4. Gordon, B.J., "On-Line Capacitance-Voltage Doping Profile Measurement of Low-Dose Ion Implants", IEEE Trans. Elec. Dev., ED-27, 12 (1980).
5. VanGelder, W., and Nicollian, E.H., "Silicon Impurity Distribution as Revealed by Pulsed MOS C-V Measurements, "J. Electrochem. Soc. Solid State Science, 118, 1 (1971).

F. MOS Process Characterization

1. Zaininger, K.H. and Heiman, F.P., "The C-V Technique as an Analytical Tool", Solid State Technology. **13**:5-6 (1970).
2. McMillan, L., "MOS C-V Techniques for IC Process Control", Solid State Technology. **15**, 47 (1972).
3. Zerbst, M., "Relaxationseffekte an Halbeiter-Isolator-Grenzflaechen", Z.Angew.Phys. **22**, 30 (1966).

SECTION 5
Principles of Operation

5.1 INTRODUCTION

This section discusses fundamental operating principles for the Package 82 system and is arranged as follows:

5.2 **System Block Diagram:** Presents an overview of the system from a block diagram perspective.

5.3 **Remote Input Coupler:** Covers operation of the Model 5951 Remote Input Coupler.

5.4 **Quasistatic CV:** Outlines fundamental principles for low-frequency measurements using the Model 595 Quasistatic CV Meter.

5.5 **High-frequency CV:** Shows fundamental operation of the system when making 100kHz and 1MHz CV measurements.

5.6 **Simultaneous CV:** Discusses the basic simultaneous CV cycle.

5.2 SYSTEM BLOCK DIAGRAM

Figure 5-1 shows a block diagram of the Package 82 system. The various components in the system perform the following functions.

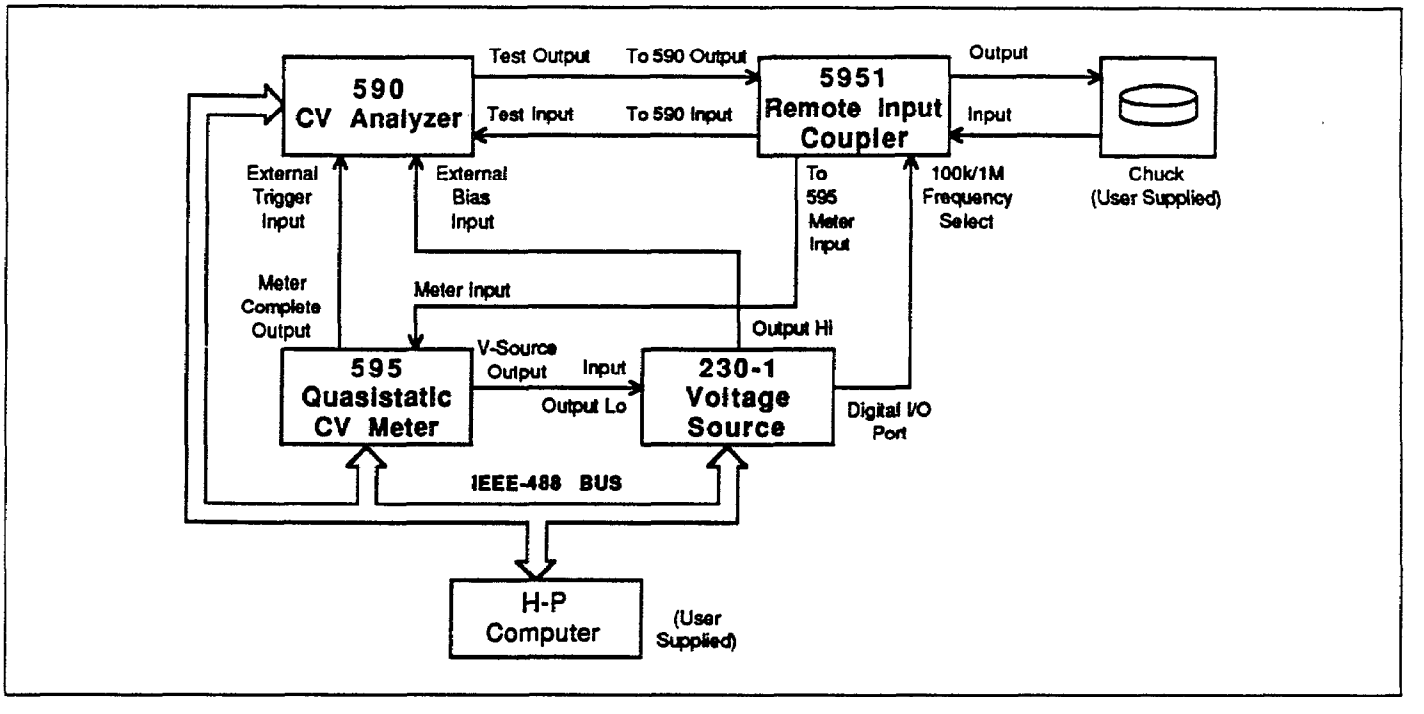


Figure 5-1. System Block Diagram

Model 230-1 Programmable Voltage Source: Provides a DC offset bias voltage of up to ±100V, and also controls 100kHz/1MHz frequency selection of the input coupler.

Model 590 CV Analyzer: Supplies a 100kHz or 1MHz, 15mV RMS test signal to the device under test, and measures high frequency capacitance and conductance.

Model 595 Quasistatic CV Meter: Sources the sweep voltage to the device under test, measures low frequency capacitance and device currents, and also triggers Model 590 readings.

Model 5951 Remote Input Coupler: Connects the device under test to the Models 590 and 595. Internal circuitry ensures minimal interaction between instruments when making both low- and high-frequency measurements.

Computer (HP 9000, Series 200 and 300 running BASIC 4.0): Controls the Models 230-1, 590, 595, and (indirectly through Model 230-1) 5951.

5.3 REMOTE INPUT COUPLER

A simplified schematic of the Model 5951 is shown in Figure 5-2.

5.3.1 Tuned Circuits

Two sets of tuned circuits are used to pass or trap out the 100kHz and 1MHz test signals. L1 and C1, and L2 and C2 on the AC blocking board form two parallel resonant circuits to block the 100kHz and 1MHz test signals from, and provides a DC path to the Model 595 input.

Meanwhile, two series resonant circuits allow passage of the 100kHz and 1MHz test signals to the Model 590 input while blocking DC. The series resonant circuit made up of L4, C2, C3, and C6 is tuned to 100kHz, while the series resonant circuit made up of L5, C4, C5, and C7 is tuned to 1MHz.

5.3.2 Frequency Control

A digital control signal, supplied by the Model 230-1, controls 100kHz or 1MHz operation of the Model 5951. This signal is applied to J8, buffered by elements of U2, and then coupled through opto-isolator U1 in order to maintain isolation between analog and digital circuits. The frequency select signal controls Q1, which switches relay K1 to select 100kHz or 1MHz operation.

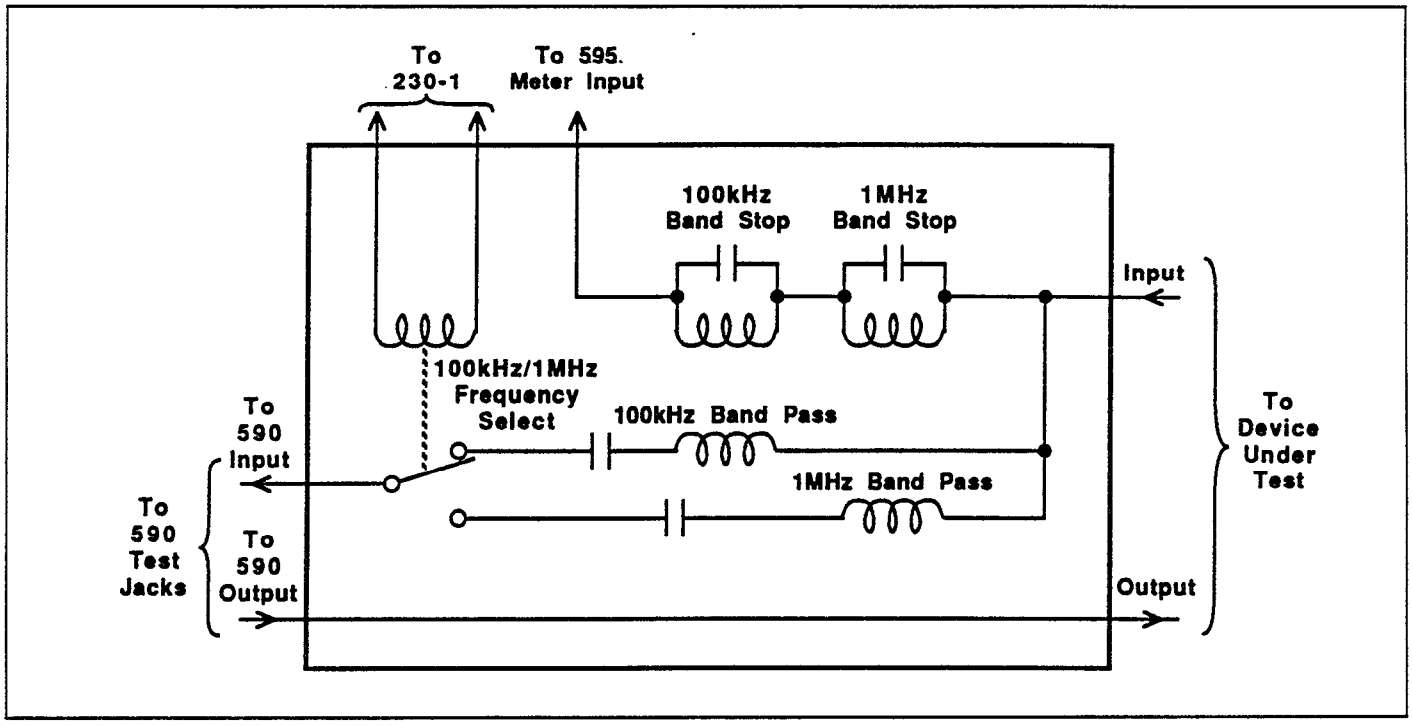


Figure 5-2. Simplified Schematic of Remote Input Coupler

5.4 QUASISTATIC CV

5.4.1 Quasistatic CV Configuration

A simplified block diagram of the Package 82 system when making low-frequency (quasistatic) CV measurements is shown in Figure 5-3. The Model 595 bias voltage is applied through the Models 590 and 5951 to the device under test. When a step voltage is applied, the unit measures the change in charge and then computes the capacitance, as discussed below.

Additional bias offset voltage of up to ±100V DC can be applied by the Model 230-1 Voltage Source. Note that this voltage is placed in series with the Model 595 voltage source, and the source voltage is routed through the Model 590 (even though that instrument is not used for low-frequency CV measurements) to superimpose the 15mV, 100kHz or 1MHz test signal on the DC bias, so that both signals can be simultaneously applied to the DUT.

5.4.2 Measurement Method

The Model 595 uses the feedback charge method for making capacitance measurements. As shown in Figure 5-4, one terminal of the unknown capacitance, C_x, is connected to the voltage source, while the other terminal is connected to the inverting input of the feedback charge amplifier, A, which is an integrator.

Initially, the feedback capacitor, C_F, is discharged by closing switch, S, which is in parallel with C_F. When the measurement begins, the switch is opened, and any charge transferred from the capacitor to the integrator input will now cause a change in integrator output as follows:

$$\Delta V_{OUT} = -Q/C_F$$

The voltage source is then changed by a small amount ΔV, which causes a charge to be transferred to C_x. The charge on C_x is proportional to the voltage change: $dQ = C_x dV$, and that charge is then applied to the integrator input, resulting in a change at its output. The charge on the feedback capacitor is determined by measuring the integrator output both before and after the voltage step and making the following calculation:

$$\Delta Q = -C_F \Delta V_{OUT}$$

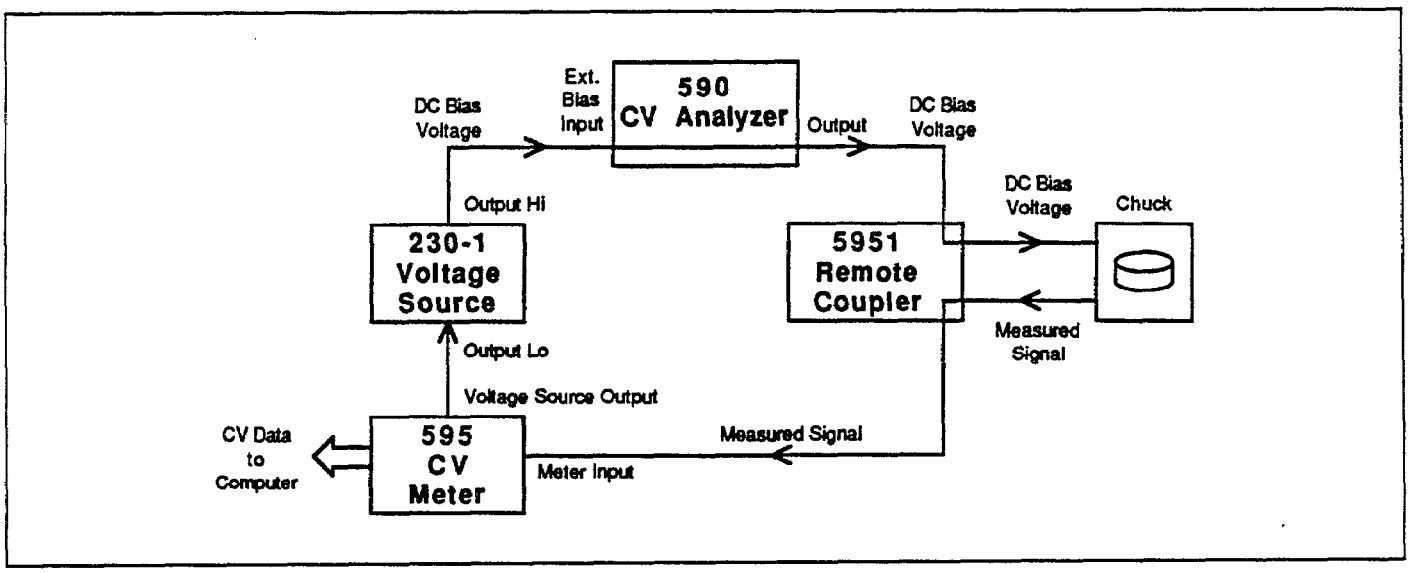


Figure 5-3. System Configuration for Quasistatic CV Measurements

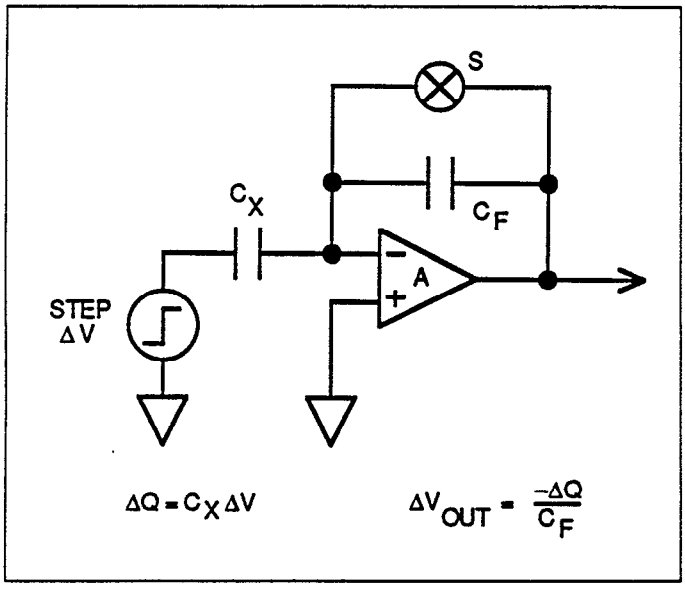


Figure 5-4. Feedback Charge Method of Capacitance Measurements

The unknown capacitance, C_x, is then calculated as follows:

$$C_x = \Delta Q/\Delta V = -C_F \Delta V_{OUT}/\Delta V$$

Figure 5-5 shows how the charge waveform is actually measured. Q1, Q2, and Q3 represent charge measurements made at three specific times. Q1 is the baseline charge made immediately before the voltage step occurs. Q3 is measured after a specified delay time (tDELAY) and is an indication of the final charge transferred through C_x. Q2 is measured before Q3 (preceding it by t_o) and is used to determine the slope of the charge waveform. This slope represents the amount of current (Q/t) flowing in C_x during the final portion of the delay time, t_o. Q/t represents the leakage current in C_x or the system. The corrected capacitance (cCAP) feature of the instrument can be used to compensate for substantial leakage currents; cCAP calculations are shown in Figure 5-5.

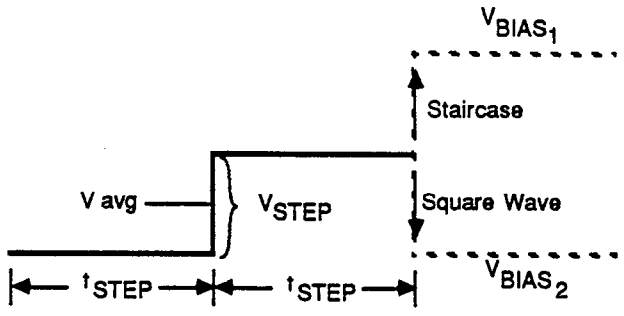


Figure 5a: Voltage Output Waveform

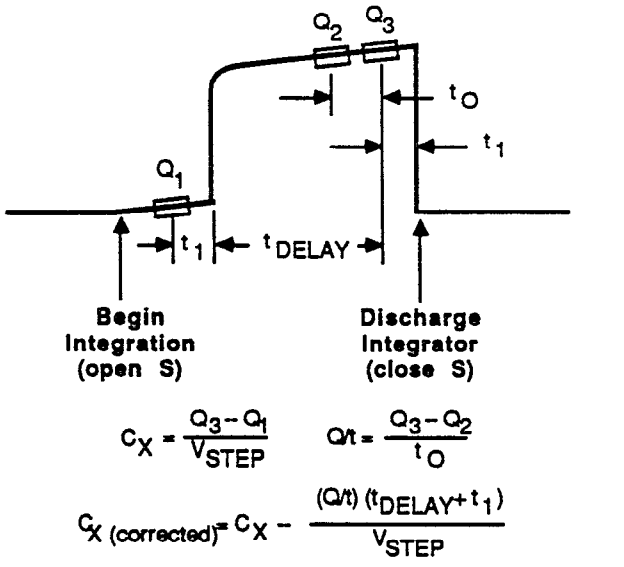


Figure 5b: Measured Charge Waveform

Figure 5-5. Voltage and Charge Waveforms for Quasistatic Capacitance Measurement

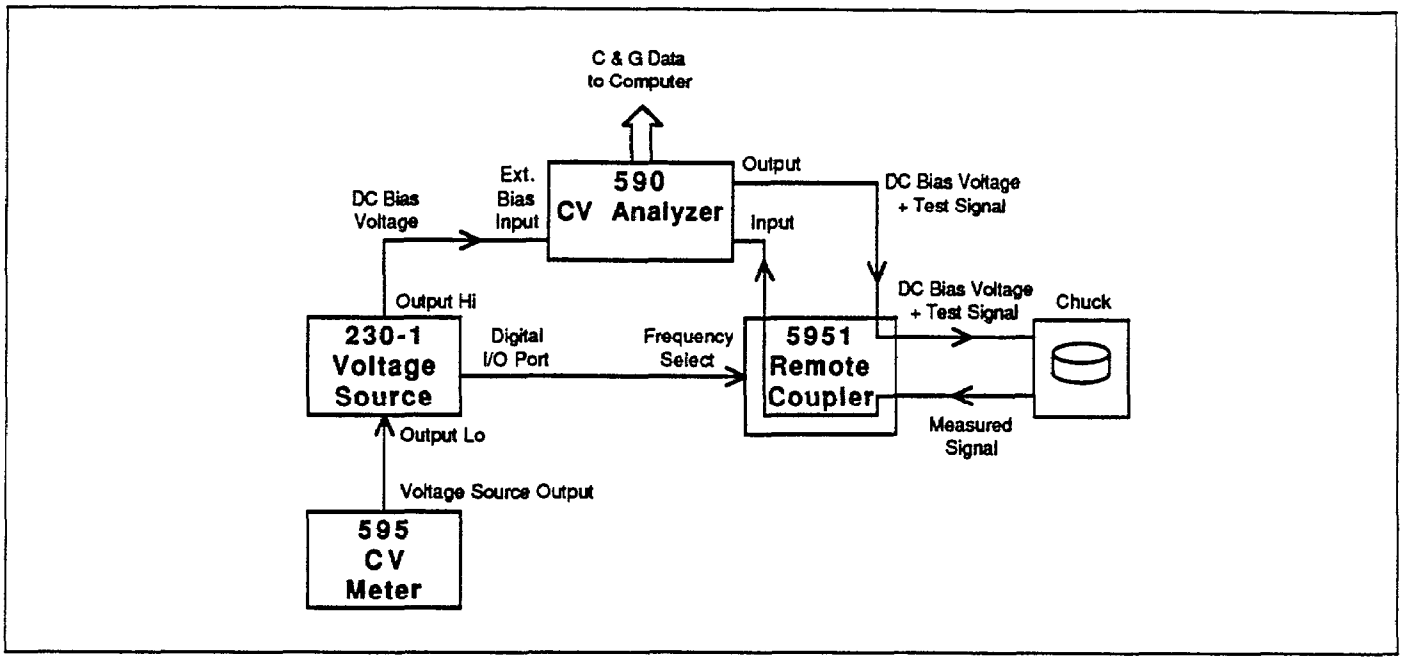


Figure 5-6. System Configuration for High Frequency CV Measurements

5.5 HIGH FREQUENCY CV

5.5.1 High Frequency System Configuration

A block diagram showing system configuration during high-frequency measurements is shown in Figure 5-6. The system is somewhat similar to the configuration for low-frequency measurements discussed above. Now, however, the Model 590 supplies a 100kHz or 1MHz test signal to the device under test and measures resulting gain and phase variations to determine capacitance and conductance values, a described below.

Even though the Model 590 has its own internal DC voltage source, that source is not used for the Package 82 system. Instead, a DC bias voltage, supplied by the Models 230-1 and 595, is routed through the Model 590, and is then applied as a composite AC and DC test signal to the device under test.

One additional aspect of the high-frequency system is the 100kHz/1MHz frequency control of the Model 5951 remote input coupler. This function is performed by the Model 230-1 through its digital I/O port.

5.5.2 High-Frequency Measurements

A simplified block diagram of the high-frequency CV modules located in the Model 590 is shown in Figure 5-7. The 100kHz and 1MHz modules do differ somewhat in detail, but their operation can be represented as outlined here.

A 100kHz or 1MHz reference signal is first generated by the waveform synthesizer, and then amplified and shaped into a sine wave by the output amplifier. The output coupling section isolates the signal and attenuates it to approximately 15mV RMS at 100kHz or 1MHz, depending on the selected test frequency. The DC bias voltage, which is supplied by the Models 230-1 and 595, is also applied at this point.

The test signal is then routed through the OUTPUT jack to the device under test, and then fed back through the test INPUT jack of the Model 590. The signal undergoes a phase and magnitude transformation, both of which depend on the complex impedance of the device under test. The test signal then undergoes current-to-voltage transformation, is further amplified, and is finally applied to the synchronous detector, which extracts phase and magnitude information. The detector provides output

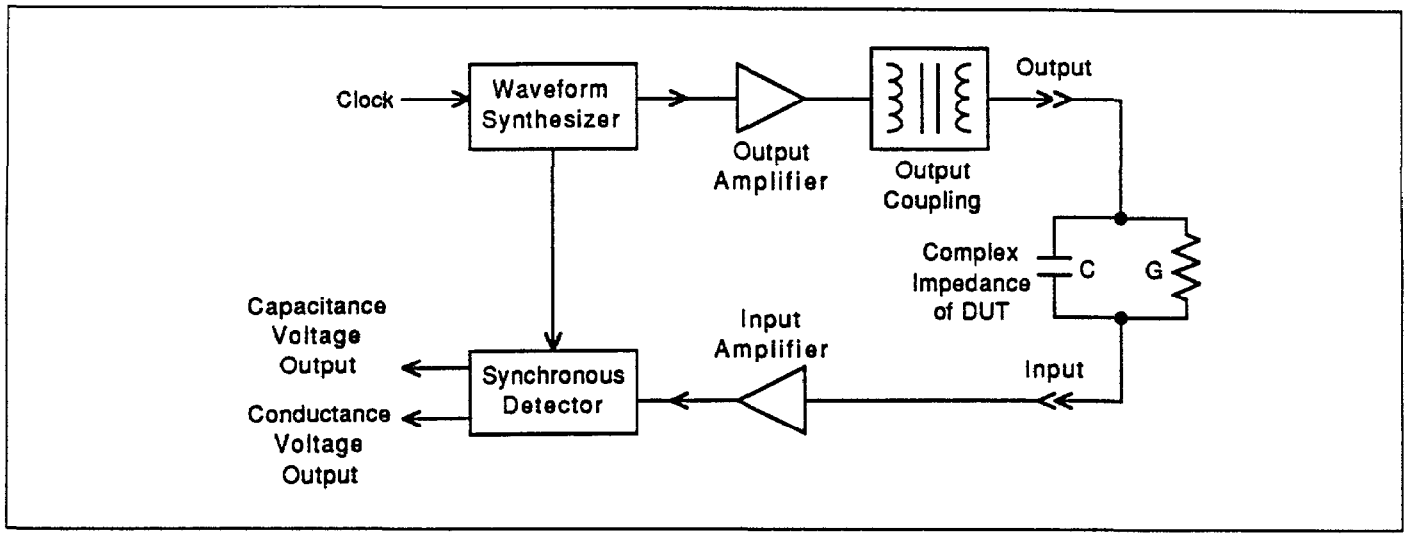


Figure 5-7. High Frequency Capacitance Measurement

voltages analogous to the capacitance and conductance of the device under test.

5.6 SIMULTANEOUS CV

In order to eliminate drift errors due to voltage stress, the Models 590 and 595 both measure capacitance during the same voltage sweep. The readings from the two instruments are synchronized using external triggering and are taken alternately during the sweep. After the sweep, C_Q is interpolated to the voltage at which C_H was measured.

Figure 5-8 shows a simplified representation of the stepped bias voltage supplied by the Model 595 during a measurement sweep. Each vertical voltage step size depends on the programmed Model 595 bias step, while each horizontal time step is determined by the programmed delay time.

As discussed above, a quasistatic measurement is a two-step process requiring at least two charge measurements. Initially, at the end of step S_1, the first charge measurement Q_1 is made, after which the voltage goes to the next step. Following the programmed delay period, the Q_3 charge measurement is made, and the capacitance is then calculated from these values and the step size; note that the voltage at this capacitance is assumed to be midway between the step increment values, or V_{AVG} in this case. Here we see that two voltage steps are necessary for every low-frequency capacitance measurement.

The Model 590 is triggered one delay time after the completion of each Model 595 reading. As a result, high-frequency measurements are made only on every other step (as represented by small rectangles in Figure 5-8). Furthermore, notice that the high-frequency measurements are not made at exactly the same voltage as the low-frequency measurements. In our present example, C_{H1} is measured at V_2. While C_1 is averaged between V_1 and V_2, and C_2 is between V_3 and V_4.

To compensate for this voltage skew, an adjusted low-frequency capacitance value, C'_1, is interpolated to a value at V_2, where C_{H1} was taken, as follows:

$$C'_1 \text{ at } V_2 = C_1 + \frac{C_2 - C_1}{V_4 - V_2} \bullet \frac{V_{STEP}}{2}$$

All C_Q readings in the array are replaced by C'_Q values upon completion of the voltage sweep.

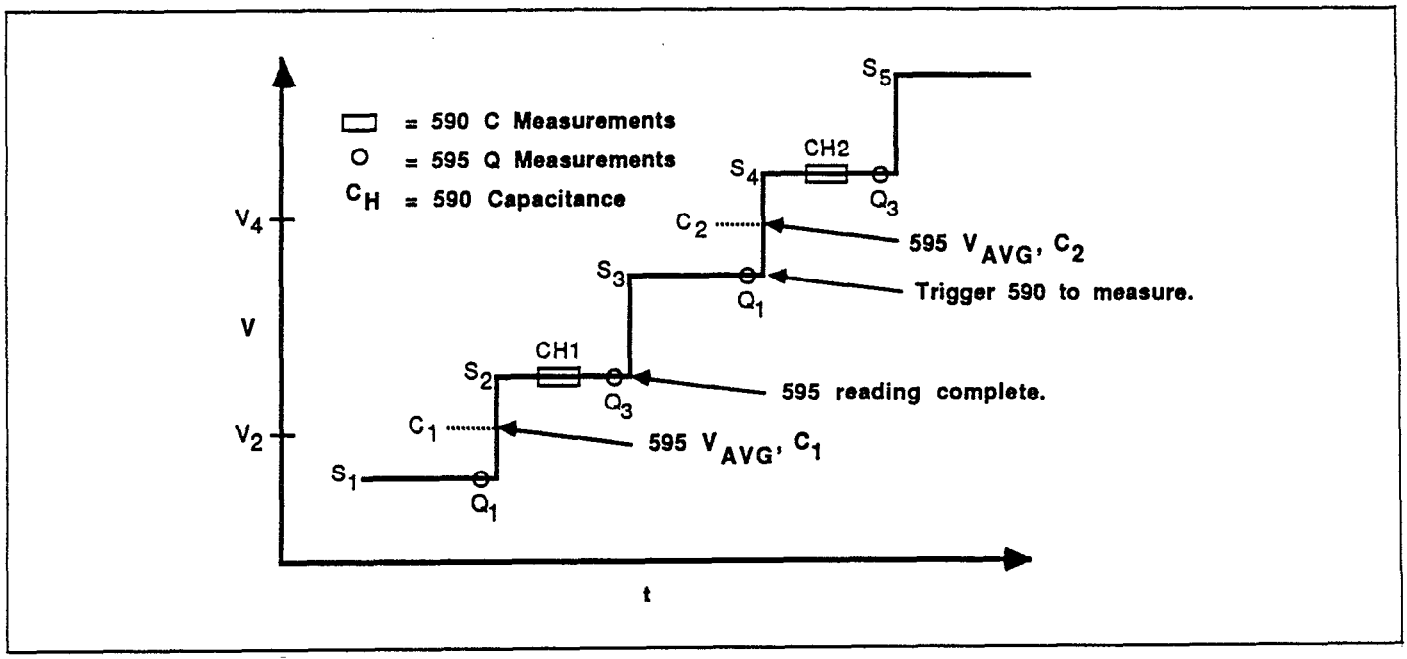


Figure 5-8. Simultaneous CV Waveform

SECTION 6
Replaceable Parts

6.1 INTRODUCTION

This section contains a list of replaceable parts for the Model 5951 Remote Input Coupler, as well as additional parts for the Model 230-1 Programmable Voltage Source (parts common to the Models 230 and 230-1 are listed in the Model 230 Instruction Manual). Component layouts and schematic diagrams for these instruments are also included.

6.2 PARTS LIST

Electrical parts for the Model 5951 are listed in order of circuit designation in Tables 6-1 and 6-2. Table 6-3 lists Model 5951 mechanical parts. Table 6-4 summarizes parts specific to the Model 230-1 only.

6.3 ORDERING INFORMATION

To place a parts order, or to obtain information concerning replacement parts, contact your Keithley representative or the factory (see the inside front cover for addresses). When ordering parts, be sure to include the following information:

1. Unit model number (230-1 or 5951)
2. Unit serial number
3. Part description
4. Circuit description, if applicable
5. Keithley part number

6.4 FACTORY SERVICE

If the unit is to be returned to Keithley Instruments for repair or service, perform the following:

1. Complete the service form at the back of this manual, and include it with the unit.
2. Carefully pack the card in the original packing carton.
3. Write ATTENTION REPAIR DEPARTMENT on the shipping label.

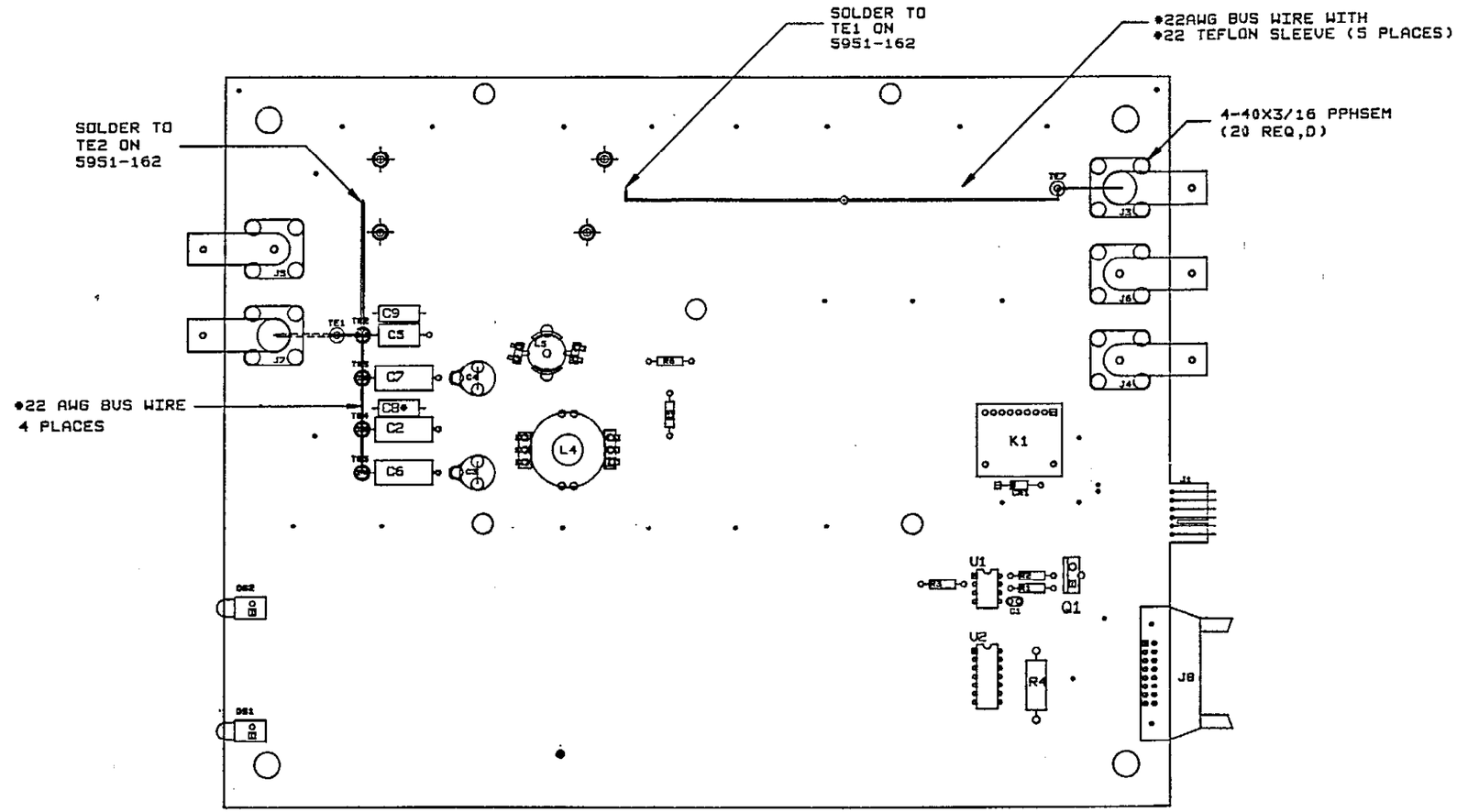
6.5 COMPONENT LAYOUTS AND SCHEMATIC DIAGRAMS

Component layout drawings and schematic diagrams for the Models 230-1 and 5951 are included on the following pages.

TABLE 6-1. HIGH FREQUENCY AND CONTROL BOARD, PARTS LIST

CIRCUIT DESIG.	DESCRIPTION	KEITHLEY PART NO.
	LABEL, WARNING	MC-233
	POLARIZING KEY	CS-491
	#22 TEFLON SLEEVING	
	2-56 NUT	2-56NUT
	2-56x7/16 PHIL PAN HD SCREW	2-56x7/16PPH
	4-40x3/16 PHIL PAN HD SCREW	4-40x3/16PPHSEM
C1	CAP,.1uF,20%,50V,CERAMIC	C-237-.1
C2	CAP,680pF,5%,500V,POLYSTYRENE	C-138-680P
C3,C4	CAP,7-70pF,500V,VARIABLE	C-345
C5	CAP,220pF,5%,500V,POLYSTYRENE	C-138-220P
C6,C7	CAP,2200pF,5%,500V,POLYSTYRENE	C-138-2200P
C8	SELECTED,100kHZ RESONANT CIRCUIT	5951-600
C9	CAP,150pF,5%,500V,POLYSTYRENE	C-138-150P
CR1	DIODE,SILICON,1N4148 (DO-35)	RF-28
DS1,DS2	PILOT LIGHT,RED,LED	PL-77
J3..J7	CONNECTOR,RIGHT ANGLE,BNC	CS-504
J8	CONN,FEMALE,16-PIN	CS-487-16
K1	RELAY,(SPDT)	RL-91
L4	CHOKE,3.3mH	CH-44
L5	CHOKE,60.1uH	CH-43
	LENGTH TO SUIT #22 AWG BUS WIRE	
Q1	TRANS,PNP SILICON,MPSU56 (CASE 152-02)	TG-148
R1	RES,560,5%,1/4W,COMPOSITION OR FILM	R-76-560
R2	RES,10K,5%,1/4W,COMPOSITION OR FILM	R-76-10K
R3	RES,1.2K,5%,1/4W,COMPOSITION OR FILM	R-76-1.2K
R4	RES,33,10%,1W,COMPOSITION	R-2-33
R5,R6	RES,100K,1%,1/8W,METAL FILM	R-88-100K
TE1,TE7	TERMINAL,INSULATED	TE-91
TE2..TE5,TE8	TERMINAL (TEFLON)	TE-97-1
U1	IC,LOW INPUT CURRENT OPTO,HCPL-2200	IC-411
U2	IC,HEX INVERTER,74HC04	IC-354

LTR.	ECO NO.	REVISION	ENG.	DATE
B	12144	RELEASED		5/15/87
B1	12451	REVISED	S.Z.	11-10-87
C	12839	REVISED		6-7-88



NOTE:

FOR COMPONENT INFORMATION, REFER TO BILL OF MATERIAL (5951-000-01).

MODEL	NEXT ASSEMBLY USED ON	QTY
5951		

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 5-20-88	SCALE 1:1	TITLE COMPONENT LAYOUT, HIGH FREQUENCY & CONTROL BOARD
KEITHLEY INSTRUMENTS INC. CLEVELAND, OHIO 44139	XX=±.015 ANG.=±1°	DRN. CB	ENG. APPR.	
	XXX=±.005 FRAC.=±1/64	MATERIAL SEE PAGE 1	C	NO. 5951-100
	SURFACE MAX. 63	FINISH SEE PAGE 1		

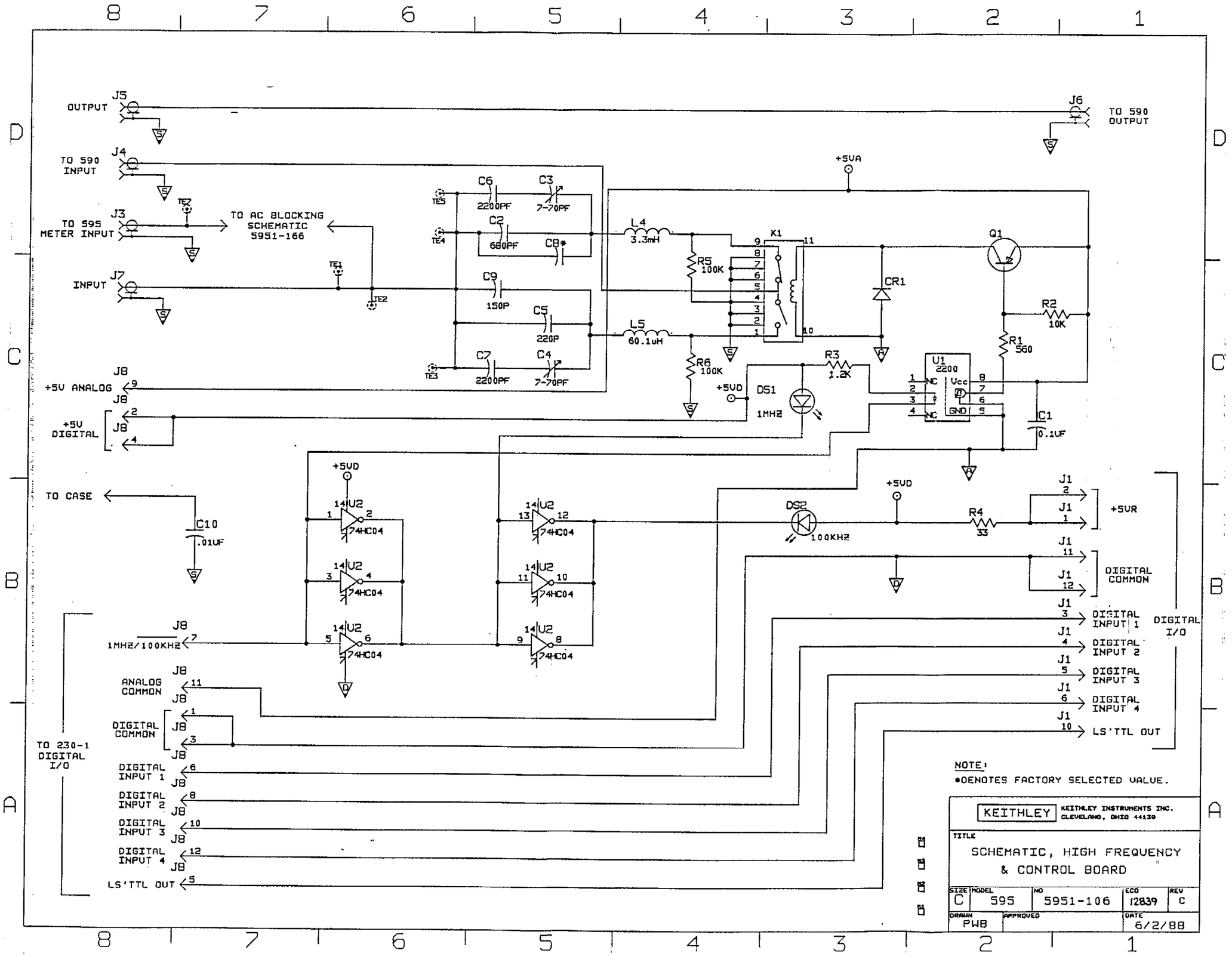
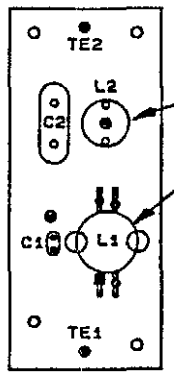


TABLE 6-2. AC BLOCKING BOARD, PARTS LIST

CIRCUIT DESIG.	DESCRIPTION	KEITHLEY PART NO.
C1	CAP,1000pF,1%,100V,CERAMIC	C-372-1000P
C2	CAP,1800pF,1%,500V,MICA	C-209-1800P
L1	CHOKE,VARIABLE	CH-23
L2	CHOKE,15uH	CH-26-15
TE1,TE2	TERMINAL	TE-92

NO. 5951-160

LTR.	ECO NO.	REVISION	ENG.	DATE
A	12144	RELEASED	WS	5-15-87



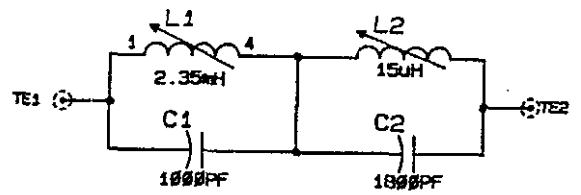
APPLY GLYPTOL TO ADJUSTMENT SCREWS AFTER FINAL CAL

NOTE:

FOR COMPONENT INFORMATION, REFER TO BILL OF MATERIAL (5951-000-03).

MODEL	NEXT ASSEMBLY USED ON	QTY.

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 3-9-87	SCALE 1:1	TITLE COMPONENT LAYOUT, AC BLOCKING BOARD
KEITHLEY INSTRUMENTS INC. CLEVELAND, OHIO 44139	XX=±.015 ANG.=±2°	DRN. CB	ENG. APPR.	
	XXX=±.005 FRAC.=±1/64	MATERIAL	C	NO. 5951-160
	SURFACE MAX. 63	FINISH		



KEITHLEY	KEITHLEY INSTRUMENTS INC. CLEVELAND, OHIO 44139				
TITLE: SCHEMATIC, AC BLOCKING BOARD					
SIZE: C	MODEL: 595	NO: 5951-166	ECO: 12144	REV: A	
DRAWN: PWB	APPROVED: [illegible]	DATE: 2/18/87			

TABLE 6-3. MODEL 5951 MECHANICAL, PARTS LIST

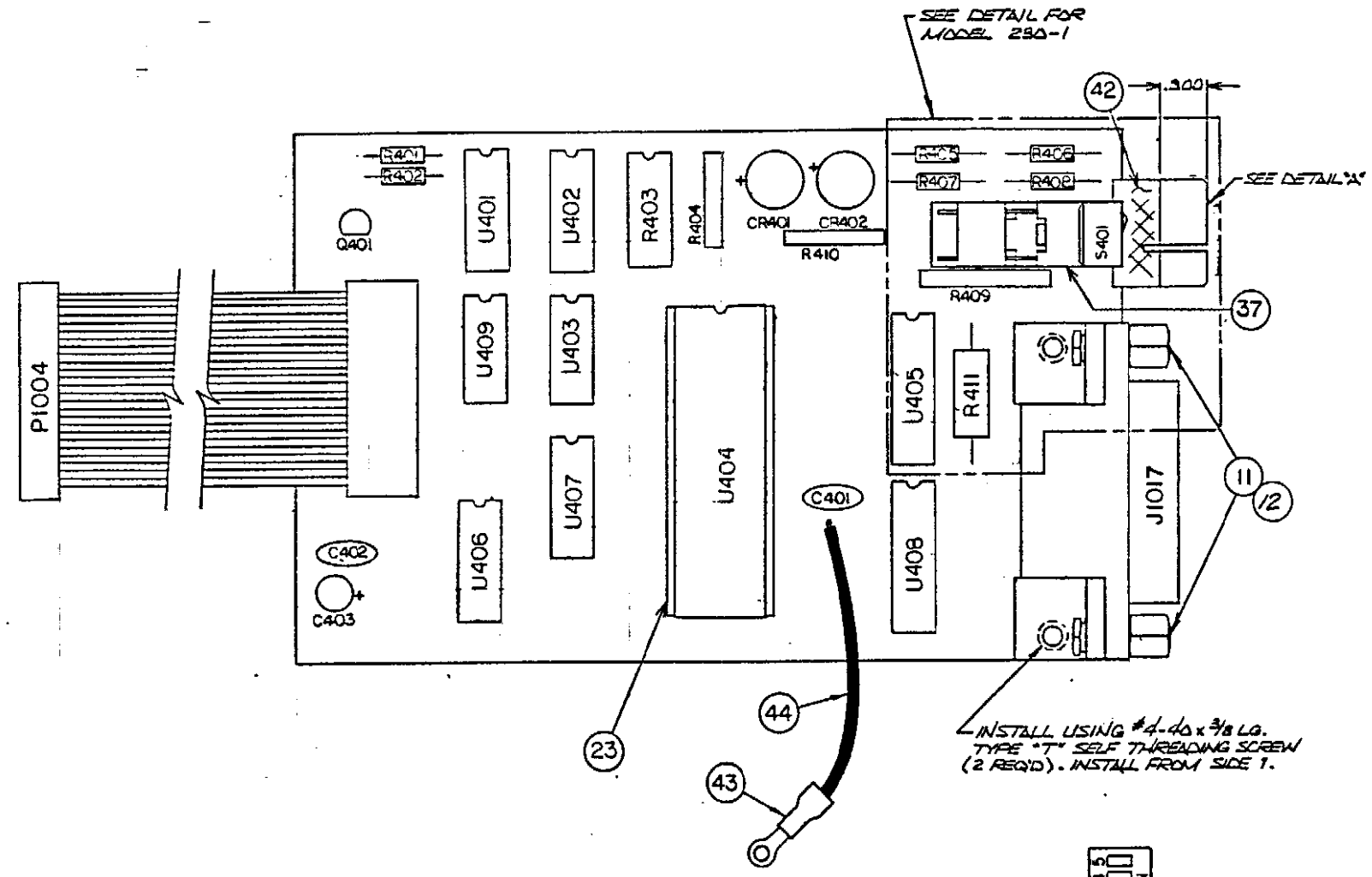
CIRCUIT DESIG.	DESCRIPTION	KEITHLEY PART NO.
	1/8"DIA.x1/4" SEMI-TUBULAR RIVET	1/8"x1/4" RIVET
	4-40 KEP NUT	4-40KEPNUT
	ARTWORK, REAR PANEL SILKSCREEN	5951-309
	ASSEMBLY	5951-300
	ASSEMBLY,CABLE	A5951-313
	BOX	BOX 711
	BRACKET, SIDE	5951-311
	BRACKET,MTG	5951-307
	CABLE,BNC	MODEL 7051-2
	CASE, BOTTOM	5951-303
	CASE, TOP	5951-302
	CONNECTOR	CS-297-16
	CONNECTOR	CS-613-16
	FEET	FE-17-1
	GROMMET	GR-44-1
	GROMMET	GR-44-1
	IEEE CABLE,SHIELDED	MODEL 7007-2
	IEEE CABLES,SHIELDED	MODEL 7007-1
	LABEL, SERIAL NO	MC-285
	LOW NOISE BNC CABLES	MODEL 4801
	LUG	LU-7
	OVERLAY, FRONT PANEL	5951-305
	PANEL, FRONT	5951-304
	PANEL, REAR	5951-308
	PEM NUT	FA-40
	PEM STUD	FA-82
	PEM, STUD	FA-82
	PEMNUT	FA-18
	POLARIZING KEY	CS-474
	SHIELD, BOTTOM	5951-312
	SHIELD, TOP	5951-310
	ARTWORK, FRONT PANEL OVERLAY	5951-306

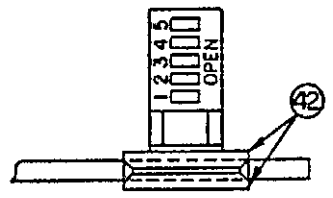
TABLE 6-3. MODEL 5951 MECHANICAL, PARTS LIST

CIRCUIT DESIG.	DESCRIPTION	KEITHLEY PART NO.
	1/8"DIA.x1/4" SEMI-TUBULAR RIVET	1/8"x1/4" RIVET
	4-40 KEP NUT	4-40KEPNUT
	ARTWORK, REAR PANEL SILKSCREEN	5951-309
	ASSEMBLY	5951-300
	ASSEMBLY,CABLE	A5951-313
	BOX	BOX 711
	BRACKET, SIDE	5951-311
	BRACKET,MTG	5951-307
	CABLE,BNC	MODEL 7051-2
	CASE, BOTTOM	5951-303
	CASE, TOP	5951-302
	CONNECTOR	CS-297-16
	CONNECTOR	CS-613-16
	FEET	FE-17-1
	GROMMET	GR-44-1
	GROMMET	GR-44-1
	IEEE CABLE,SHIELDED	MODEL 7007-2
	IEEE CABLES,SHIELDED	MODEL 7007-1
	LABEL, SERIAL NO	MC-285
	LOW NOISE BNC CABLES	MODEL 4801
	LUG	LU-7
	OVERLAY, FRONT PANEL	5951-305
	PANEL, FRONT	5951-304
	PANEL, REAR	5951-308
	PEM NUT	FA-40
	PEM STUD	FA-82
	PEM, STUD	FA-82
	PEMNUT	FA-18
	POLARIZING KEY	CS-474
	SHIELD, BOTTOM	5951-312
	SHIELD, TOP	5951-310
	ARTWORK, FRONT PANEL OVERLAY	5951-306

	BINDING POST	BP-25
	BOT SHIELD TO MB6-32x1/4 PHIL PAN HEAD SEM	6-32x1/4PPHSEM
	FOR CLOSING CASE6-32x1/4" PPHSEM BLACK ZINC FINISH	6-32x1/4PPHSEMBLKZIN
FOR FA-82	4-40 KEP NUT	4-40KEPNUT
FOR MTG BP-25	6-32x1/4 PHIL PAN HEAD SEM	6-32x1/4PPHSEM
FOR MTG FE-17-1	6-32x1/4" PHIL PAN HEAD	6-32x1/4PPH
	LENGTH 5 FEET CABLE,FLAT RIBBON	SC-63-4
	MB. TO CASE BOT 6-32x5/8 PHIL PAN HEAD SEM	6-32x5/8PPHSEM
	MTG F.P. TO M.B.BRACKET,MTG	5951-307
	SEE 5951-000-01 COMP L/O, M.B.	5951-100
	SHIELD TO CASE CAPACITOR C10	C-22-.01
	SHIELD TO SHIELD4-40x1/4 PHIL PAN HEAD SEM	4-40x1/4PPHSEM
	SOS-8632-20 STANDOFF	ST-186-1
	SWAGED IN SHIELDSTANDOFF	ST-139-4

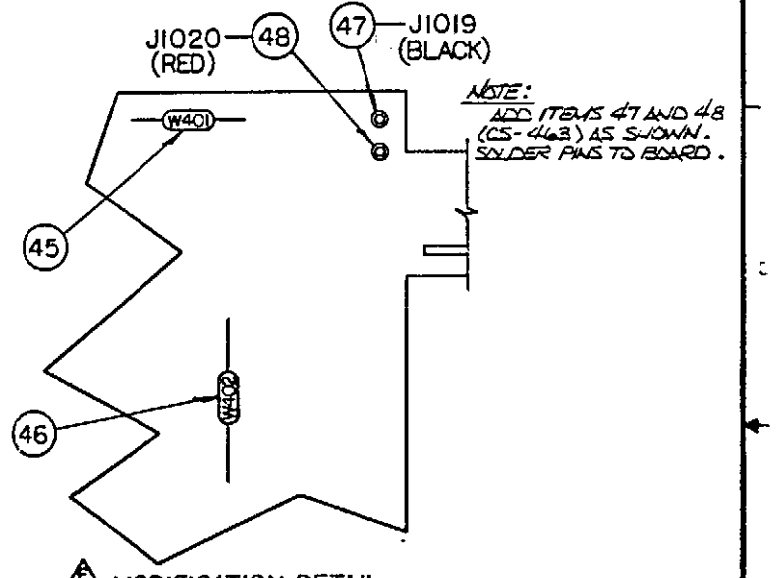
ZONE	LTR	ECO NO	REVISION	DATE
	A	[illegible]	RELEASED	[illegible]
	B	B310	RENUMBERED, WAS 220-130	3-11-82
			ADDED ITEMS 22 AND 23	
	C	B399	R 17 WAS TF-102-10K	4-26-82
	D	B456	ADDED ITEMS 24, 25, 44	6-25-82
			ARTWORK WAS 19-0	
	E	B572	ITEM 38 WAS SW-453	11-4-82
	F	V215	ADDED MOD. DETAIL FOR 230-1, ADDED ITEMS 45 THRU 48	4-28-87
	G	V2848	ADDED ITEM 12	8-28-87
	H	V2523	ADDED DESIG. W401, W402	1-8-88
	J	V3112	CHG'D CS-380 TO CS-378	2-17-89





DETAIL "A"

⚠ NOTE:
REMOVE R405, 406, 408 AND 411. ADD W401 AND W402 JUMPERS TO R405 AND 411 LOCATIONS.



NOTE:
ADD ITEMS 47 AND 48 (CS-463) AS SHOWN. SOLDER PINS TO BOARD.

⚠ MODIFICATION DETAIL MODEL 230-1

*DELETE FOR MODEL 230-1

ITEM	PART NO.	SCHEM. DESIG.	ZONE
1	220-132	MAKE ITEM	
2			
3			
4	C-22-0.01	C401	E2
5	C22-0.01	C402	C3
6	C314-10	C403	C3
7	RF46	CR401	E1
8	RF46	CR402	E1
9	CA-10-2	P1004	C2
10	CS-443	J1017	F2
⚠ 11	CS-378	——	F2
⚠ 12	4-40 HEXNUT	2-220-0	F3
13			
14	IC-251	U401	D2
15	IC-130	U402	D2
16	IC-186	U403	D2
17	LSI-49	U404	D2
18	IC-298	U405	E2
19	IC-182	U406	D3
20	IC-161	U407	D3
21	IC-299	U408	E3
⚠ 22	IC-163	U409	D2

ITEM	PART NO.	SCHEM. DESIG.	ZONE
23	SO-84		D3
24			
25			
26	R76-4.7K	R401	C1
27	R76-4.7K	R402	C1
⚠ 28	TF-102-2	R403	D1
29	TF-103-2	R404	D1
30	R1-100	R405	E1 *
31	R1-100	R406	E1 *
32	R1-100	R407	E1
33	R1-100	R408	E1 *
34	TF-100	R409	E2
⚠ 35	TF-103-1	R410	E2
⚠ 36	R-2-33	R411	E2 *
37	SO-86	——	E1
⚠ 38	SW-450-5	S401	E2
39			
40			
41	TG-47	Q401	C2
42	219338-25	——	F1
⚠ 43	LU-77-1	——	E4
⚠ 44	SC-55	LENGTH 3"	E3

+MODEL 230-1 ONLY

ITEM	PART NO.	SCHEM. DESIG.	ZONE	
⚠ 45	J-3	W401	G3	+
⚠ 46	J-3	W402	G3	+
⚠ 47	CS-463	J1019	H3	+
⚠ 48	CS-463	J1020	H3	+
49				
50				
51				
52				
53				
54				

MODEL	NEXT ASSEMBLY	QTY
	USED ON	

DO NOT SCALE THIS DRAWING
DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED
XX ± .015 ANG ± 1°
XXX ± .005 FRAC ± 1/64
SURFACE MAX 63

KEITHLEY Keithley Instruments Inc. Cleveland, Ohio 44139

DATE 12/4/81 | SCALE 2-1
DRN R.S. | ENG APPR JT.
MATERIAL
FINISH

TITLE COMPONENT LAYOUT IEEE

SIZE D | NO 220-130

REV A

MATES WITH MAINFRAME CONNECTOR J1004
SEE SCHEMATIC D220-106

MODIFICATION DETAIL
MODEL 230-1

DIGITAL CONTROL OUTPUT
J1018
DIGITAL COMMON
MSB
DATA OUTPUT
LSB
FROM 230-126 ANALOG
+5VA
W401
W402
R404 2.2K
R407 100
R405 100
R408 100
R406 100
R410 4.7K
CR402
CR401
R411 33
R403 10K
R401 4.7K
R402 4.7K
Q401
U401 4094
U402 4021
U403
U404 TMS9914
U405 75160
U406 LS138
U407 LS367
U408 75161
U409
P1004
PB2 (LATCH)
PB0 (CLOCK)
PB1 (DATA)
DIGITAL COMMON
+5V DIGITAL
C402 10
C403 0.01
C401 0.01
S401
TO IEEE BUS
DIGITAL COMMON
(8004)

NOTES:

1) ALL RESISTOR VALUES ARE IN OHMS UNLESS MARKED OTHERWISE. (K-KILOHMS, M MEGOHMS)
2) ALL CAPACITOR VALUES ARE IN MICOFARADS UNLESS MARKED OTHERWISE. (pF-PICOFARADS)
3) ⏚ DENOTES DIGITAL COMMON.
4) ● DENOTES REAR PANEL ACCESS.
5) (8004) DENOTES MEMORY MAPPED ADDRESS (HEXIDECIMAL).
6) ⏥ DENOTES CHASSIS CONNECTION.
7) ▼ DENOTES ANALOG COMMON.

HIGHEST SCHEMATIC DESIGNATIONS USED		
P1004	R411	U409
J1018	C403	S401
	CR402	Q401

SCHEMATIC DESIGNATIONS NOT USED			

ZONE	LTR	ECO NO	REVISION	DATE
	A		RELEASED	2-12-82
	B	8310	MODEL U405 & U406 IC, PIN 1 P 2345 TO MOD. CHG PIN 9 TO PIN 16 ON U402. CHG'D U406 MODEL PINS 4,5,11. DELETED PIN 7 ON U402. SWITCHED PIN 1 & 2 ON U406.	3-12-82
	C	8468	ADDED C411, 33; CHGD C401 FROM +5V TO CHASSIS	6-25-82
	D	12525	ADDED MODIFICATION DETAIL FOR MODEL 230-1.	4-4-83

DO NOT SCALE THIS DRAWING	UNLESS OTHERWISE SPECIFIED	DATE 12-27-81	SCALE NONE	TITLE SCHEMATIC IEEE BOARD
KEITHLEY Keithley Instruments Inc. Cleveland, Ohio 44139	XX = ± .010 ANG ± 1°	DWN		
	XXX = ± .005 FRAC = 1/64	MATERIAL		SIZE D NO 220-136
	SURFACE MAX 63	FINISH		

MODEL NEXT ASSEMBLY

FORM 285118 rev C

230-120 ON

ZONE	LTR	ECO NO.	REVISION	DATE
		2270	[illegible]	[illegible]
	C	2654	DELETED VR-32, R-33, R-34, R-35, R-36, R-37, R-38, R-39, R-40, R-41, R-42, R-43, R-44, R-45, R-46, R-47, R-48, R-49, R-50, R-51, R-52, R-53, R-54, R-55, R-56, R-57, R-58, R-59, R-60, R-61, R-62, R-63, R-64, R-65, R-66, R-67, R-68, R-69, R-70, R-71, R-72, R-73, R-74, R-75, R-76, R-77, R-78, R-79, R-80, R-81, R-82, R-83, R-84, R-85, R-86, R-87, R-88, R-89, R-90, R-91, R-92, R-93, R-94, R-95, R-96, R-97, R-98, R-99, R-100, R-101, R-102, R-103, R-104, R-105, R-106, R-107, R-108, R-109, R-110, R-111, R-112, R-113, R-114, R-115, R-116, R-117, R-118, R-119, R-120, R-121, R-122, R-123, R-124, R-125, R-126, R-127, R-128, R-129, R-130, R-131, R-132, R-133, R-134, R-135, R-136, R-137, R-138, R-139, R-140, R-141, R-142, R-143, R-144, R-145, R-146, R-147, R-148, R-149, R-150, R-151, R-152, R-153, R-154, R-155, R-156, R-157, R-158, R-159, R-160, R-161, R-162, R-163, R-164, R-165, R-166, R-167, R-168, R-169, R-170, R-171, R-172, R-173, R-174, R-175, R-176, R-177, R-178, R-179, R-180, R-181, R-182, R-183, R-184, R-185, R-186, R-187, R-188, R-189, R-190, R-191, R-192, R-193, R-194, R-195, R-196, R-197, R-198, R-199, R-200, R-201, R-202, R-203, R-204, R-205, R-206, R-207, R-208, R-209, R-210, R-211, R-212, R-213, R-214, R-215, R-216, R-217, R-218, R-219, R-220, R-221, R-222, R-223, R-224, R-225, R-226, R-227, R-228, R-229, R-230, R-231, R-232, R-233, R-234, R-235, R-236, R-237, R-238, R-239, R-240, R-241, R-242, R-243, R-244, R-245, R-246, R-247, R-248, R-249, R-250, R-251, R-252, R-253, R-254, R-255, R-256, R-257, R-258, R-259, R-260, R-261, R-262, R-263, R-264, R-265, R-266, R-267, R-268, R-269, R-270, R-271, R-272, R-273, R-274, R-275, R-276, R-277, R-278, R-279, R-280, R-281, R-282, R-283, R-284, R-285, R-286, R-287, R-288, R-289, R-290, R-291, R-292, R-293, R-294, R-295, R-296, R-297, R-298, R-299, R-300, R-301, R-302, R-303, R-304, R-305, R-306, R-307, R-308, R-309, R-310, R-311, R-312, R-313, R-314, R-315, R-316, R-317, R-318, R-319, R-320, R-321, R-322, R-323, R-324, R-325, R-326, R-327, R-328, R-329, R-330, R-331, R-332, R-333, R-334, R-335, R-336, R-337, R-338, R-339, R-340, R-341, R-342, R-343, R-344, R-345, R-346, R-347, R-348, R-349, R-350, R-351, R-352, R-353, R-354, R-355, R-356, R-357, R-358, R-359, R-360, R-361, R-362, R-363, R-364, R-365, R-366, R-367, R-368, R-369, R-370, R-371, R-372, R-373, R-374, R-375, R-376, C-301, C-302, C-303, C-304, C-305, C-306, C-307, C-308, C-309, C-310, C-311, C-312, C-313, C-314, C-315, C-316, C-317, C-318, C-319, C-320, C-321, C-322, C-323, C-324, C-325, C-326, C-327 THRU C-330, CR-301, CR-302, CR-303, CR-304, CR-305, CR-306, CR-307, CR-308, CR-309, CR-310, CR-311, CR-312, CR-313, CR-314, CR-315, Q-301, Q-302, Q-303, Q-304, Q-305, Q-306, Q-307, Q-308, Q-309, Q-310, Q-311, Q-312, Q-313, U-301, U-302, U-303, U-304, U-305, U-306, U-307, U-308, U-309, U-310, U-311, U-312, U-313, U-314, U-315, U-316, VR-301, K-301, K-302, K-303, J-1001, J-1002, J-1003, J-1004, J-1005, J-1006, J-1007, J-1008, J-1009, CHANGED J1002 TO J1003, CHANGED J1003 TO J1009.	9752
	D	8840	SEE PAGE 2.	12-4-86
	F	10026	SEE PAGE 2.	2-24-87
	G	10478	DELETED C327 THRU C330.	10-27-86
	J	10765	SEE PAGE 2.	2-24-87
	K	10879	SEE PAGE 2.	4-3-87
	L	12115	SEE PAGE 2.	11-25-87

#4-40 x 3/16 LG PHIL PAN HD.

R301 R302 U301 U302 U303 R303 R304 R305 C301 C302 CR301 R306 R307 R308 U304 R309 R310 R311 C304 U305 C303 R312 U307 U306 C305 U308 R313 R314 R315 U309 R316 R322 R320 U310 R317 R318 R319 R321 R324 U311 R325 R326 R327 R328 U312 U313 U314 R376 R330 R331 R332 R333 Q301 Q302 Q303 R375 R334 Q304 Q305 Q306 Q307 R340 R335 R336 R337 R338 R339 R341 R342 R343 R344 C315 U315 Q308 C316 R346 R351 C317 R347 R348 R349 R352 R353 R354 CR304 CR307 R356 CR305 CR308 CR309 CR310 K301 K302 R357 C319 R358 R359 R360 R361 R362 R363 R364 C320 C329 CR311 CR313 CR314 CR315 K303 C322 J1009 R366 R368 R369 R370 R371 R372 R373 U316 C324 J1003

#4-40 x 3/16 LG. PHIL PAN HD. (4 PLACES TYP.)

#4-40 x 1/2 LG. PHIL PAN HD. (4 PLACES TYP.)

8 REQ'D USE WITH R353, R354, R359, R360

SEE DETAIL FOR MODEL 230-1

VR301 C309 C310 C311 R329 CR302 R355 C330 C307 C308 C312 Q314 C313 R374 CR303 R345 R360 C318 CR306 Q309 Q310 Q311 Q312 R365 C321 CR312 R367 Q313 Q315 C325 C326

189 192 191 195

224 P1020 223 222 225 P1019 226 223 221 ADD HEATSINK (HS-34) TO VR301 AS SHOWN. RED BLACK 227 POSITION INSULATOR ON BOARD AS SHOWN.

⚠ MODIFICATION DETAIL MODEL 230-1

MODEL	NEXT ASSEMBLY
SERIAL NO.	

DO NOT SCALE THIS DRAWING — UNLESS OTHERWISE SPECIFIED: DIMENSIONAL TOLERANCES — XX ± 0.015, ANG ± 1°, XXX ± 0.005, FRAC ± 1/64, SURFACE MAX 63 — DATE 11-4-74 — DRN — CHK ADM FAM — SCALE 2-1 — MATERIAL — FINISH

KEITHLEY Keithley Instruments Inc. Cleveland, Ohio 44139

TITLE COMPONENT LAYOUT, ANALOG BOARD

SIZE D NO 230-120

FORM 285116 REV. A

230-120 ON

ZONE	LTR	ECO NO	REVISION	DATE
	B	8270	RELEASED	4-Feb
	C	8694	SEE PAGE 1	14-7-82
	D	[illegible]	ITEM [illegible]	12-[illegible]
	E	[illegible]	ITEM [illegible]	[illegible]
	F	9472	DELETED ITEM 50,51 ADDED C327 & C328	10-27-83
	G	9936	R312 WAS 2.2K, U305 WAS 2304-400	4-26-84
	H	10546	R344 WAS 1K, R355 WAS [illegible]	11-[illegible]-84
	—	10765	[illegible]	2-5-86
	K	12058	CHGD ITEM 16 FROM C-314-250 TO C-314-220	4-3-87
	L	12115	ADDED ITEMS 221 THRU 227. ITEMS 164 & 168 MADE EC-71. ADDED 27A, 28A, 29A	4-28-87

ITEM	PART NO.	SCHEM. DESIG.	ZONE
1	D230-122	HOLE SIZE	
2			
3			
4	C-22-0.01	C301	C2
5	C-237-.47	C302	D2
6	C-238-.1	C303	C2
7	"	C304	B2
8	C-22-.01	C305	D2
9			
10	C-178-.1	C307	E3
11	C-22-0.01	C308	F3
12	C-314-10	C309	D3
13	"	C310	D3
14	"	C311	E3
15	C-240-4.7	C312	F3
16	C-314-220	C313	E4
17			
18	C-22-.001	C315	C4
19	C-238-.1	C316	C4
20	"	C317	D4
21	"	C318	F4
22	C-88-470p	C319	C5
23	C-22-220p	C320	C5
24	C-238-.1	C321	F5
25	C-22-.01	C322	E5
26			
27	C-238-.1	C324	D5
28	C-240-4.7	C325	F5
29	C-22-0.01	C326	F5
30			
31			
32	C-22-0.01	C329	E4
33	C-314-15	C330	E3
34			
35	RF-28	CR301	D2
36	"	CR302	E3
37	RF-38	CR303	E4
38	RF-43	CR304	C4
39	RF-43	CR305	D4
40	RF-28	CR306	F4

ITEM	PART NO.	SCHEM. DESIG.	ZONE
41	RF-43	CR307	C4
42	RF-43	CR308	D4
43	RF-42	CR309	D4
44	"	CR310	D5
45	"	CR311	D5
46	RF-28	CR312	F5
47	RF-43	CR313	D5
48	RF-43	CR314	D5
49	"	CR315	D5
50			
51			
52	:		
53	.		
54			
55	CS-389-3	J1003	E5
56	CS-288-4	J1009	E5
57			
58			
59	EL-60	K301	D4
60	EL-60	K302	E4
61	EL-71	K303	E5
62			
63			
64	76-128	Q301	C3
65	"	Q302	D3
66	"	Q303	D3
67	"	Q304	C3
68	"	Q305	C3
69	"	Q306	D3
70	"	Q307	D3
71	76-130	Q308	C4
72	76-84	Q309	F4
73	"	Q310	G4
74	76-140	Q311	F4
75	76-47	Q312	G5
76	"	Q313	G5
77	230-600	Q314	F4
78	230-601	Q315	F5
79			
80			

ITEM	PART NO.	SCHEM. DESIG.	ZONE
81	RP-97-100K	R301	C1
82	RP-97-100K	R302	C2
83	TF-103-4	R303	C2
84	TF-103-3	R304	D2
85	"	R305	D2
86	R-76-10K	R306	D2
87	"	R307	D2
88	"	R308	D2
89	R-88-301K	R309	B2
90	"	R310	C2
91	R-88-6.04K	R311	C2
92	R-76-1K	R312	D2
93	R-88-10K	R313	B2
94	R-88-1M	R314	B2
95	R-88-49.9K	R315	C2
96	R-263-22.2K	R316	C2
97	R-76-10K	R317	D2
98	R-76-4.7K	R318	D2
99	"	R319	D2
100	RP-97-200	R320	C3
101	RP-97-10K	R321	B3
102	R-263-22.2K	R322	C3
103	R-76-10K	R323	D3
104	R-88-11K	R324	C3
105	R-76-15K	R325	C3
106	R-76-24K	R326	C3
107	R-76-100K	R327	C3
108	R-76-24K	R328	C3
109	R-76-10K	R329	D3
110	R-76-3.3K	R330	C3
111	R-76-10K	R331	C3
112	TF-103-2	R332	D3
113	RP-97-5K	R333	C3
114	R-263-10K	R334	D3
115	R-76-2.2M	R335	E4
116	R-88-2.49K	R336	B4
117	"	R337	B4
118	R-88-7.5K	R338	C4
119	R-76-100K	R339	D4
120	R-263-88.7K	R340	D4

ITEM	PART NO.	SCHEM. DESIG.	ZONE
121	R-76-10K	R341	C4
122	RP-97-100	R342	C4
123	RP-97-10K	R343	D4
124	RP-97-1K	R344	D4
125	R1-22	R345	F4
126	R-263-19.96K	R346	C4
127	R-88-12.1	R347	D4
128	R-88-294	R348	E4
129	R-76-430	R349	E4
130	R-176-2.5K	R350	F4
131	R-263-101K	R351	C4
132	R-88-13	R352	D4
133	R-88-26.1	R353	E4
134	R-76-6Ω2	R354	E4
135	R-76-4.7K	R355	F4
136	R-264-99.6K	R356	C4
137	R-264-204.8K	R357	C4
138	R-88-13	R358	D5
139	R-88-26.1	R359	E5
140	R-76-6Ω2	R360	E5
141	R-76-1K	R361	C5
142	R-88-12.1	R362	D5
143	R-88-294	R363	E5
144	R-76-430	R364	E5
145	R-176-2.5K	R365	F5
146	R-176-100K	R366	C5
147	R-1-22	R367	F5
148	R-176-100K	R368	C5
149	"	R369	C5
150	"	R370	C5
151	"	R371	C5
152	"	R372	C6
153	R-176-2.5K	R373	C5
154	R-76-3.9K	R374	E4
155	R-76-10M	R375	D3
156	R-76-10M	R376	D3
157			
158			
159			
160			

ITEM	PART NO.	SCHEM. DESIG.	ZONE
161	IC-251	U301	C1
162	"	U302	D1
163	"	U303	D1
164	IC-158	U304	E2
165	IC-323	U305	C2
166	IC-248	U306	D2
167	IC-320	U307	D2
168	IC-102	U308	E2
169	IC-248	U309	C3
170	IC-312	U310	D3
171	IC-106	U311	E3
172	IC-219	U312	C3
173	"	U313	D3
174	IC-206	U314	D3
175	IC-274	U315	C4
176	IC-176	U316	C5
177			
178			
179	IC-93	VR301	E3
180			
181			
182			
183			
184			
185			
186			
187			
188			
189	MS-22	2 REQ'D	F3, F6
190			
191	MK-16	2 REQ'D	F3, F6
192	MK-20	2 REQ'D	F3, F6
193			
194			
195	30-83-1	8 REQ'D	D4, E4
196			
197			
198			
199			
200			

ITEM	PART NO.	SCHEM. DESIG.	ZONE

MANEL 220-1 ONLY

221	HS-34	—	
222	SC-68	RED	
223	TX-17X3/8	—	
224	LU-90	PINK	
225	LU-90	PINK	
226	SC-68	BLACK	
227	27493-20	—	

MODEL NEXT ASSEMBLY
USED ON

DO NOT SCALE THIS DRAWING

DIMENSIONAL CLEARANCES UNLESS OTHERWISE SPECIFIED
XX ± ± .015 ANG ± ±1°
XXX ± ± .005 FRAC XX1/64
SURFACE MAX 63

KEITHLEY Keithley Instruments Inc. Cleveland, Ohio 44139

DATE 11 4 82 SCALE
DRN
CHK APPR RAM
MATERIAL
FINISH

TITLE COMPONENT LAYOUT, ANALOG BOARD

SIZE D NO 230-120

APPENDIX A

Constants Used for Analysis

Symbol	Description	Value
q	Charge on electron	1.60219×10^{-19}C
kT	Thermal energy (room temperature)	4.046×10^{-21}J
ϵ_{ox}	Permittivity of SiO2	3.4×10^{-13}F/cm
ϵ_s	Permittivity of silicon	1.04×10^{-12}F/cm
E_G	Energy gap of silicon	1.12eV
n_i	Intrinsic carrier concentration	1.4×10^{-11}cm^{-3}

APPENDIX B

Analysis Variables

Symbol	Description	Unit
A	Gate area	cm^2
C_{FB}	Flatband capacitance	pF
C_H	High-frequency capacitance	pF
C_{OX}	Oxide capacitance	pF
C_Q	Quasistatic capacitance	pF
D_{IT}	Interface trap density	$cm^{-2}eV^{-1}$
E_T	Interface trap energy	eV
G	High-frequency conductance	μS
N	Doping concentration	cm^{-3}
Q/t	Current	pA
t_{OX}	Oxide thickness	nm
V_{FB}	Flatband voltage	V
V_{GS}	Gate-substrate voltage	V
W	Depletion depth	μm
ϕ_B	Bulk potential	V
ψ_S	Band bending	V

APPENDIX C

Summary of Analysis Equations

Analysis Function	Computation	Comments
Doping Profile	$W = A\epsilon_S\left(\frac{1}{C_H} - \frac{1}{C_{OX}}\right)$	Computed for each V_{GS} value.
	$N = \frac{(-2\times10^{-14})(1-C_Q/C_{OX})/(1-C_H/C_{OX})}{A^2q\,\epsilon_S\,\Delta(i)}$	Computed for each V_{GS} value.
	where: $\Delta(i) = \frac{\frac{1}{C_H^2(i)} - \frac{1}{C_H^2(i+1)}}{V_{GS}(i+1) - V_{GS}(i)}$	
Flatbands	$C_{FB} = \frac{C_{OX}\,A\epsilon_S/L_B\,(1\times10^{-4})}{(1\times10^{-12})\,C_{OX} + A\epsilon_S/L_B\,(1\times10^{-4})}$	
	where: $L_B = (1\times10^4)\sqrt{\frac{\epsilon_S\,kT}{q^2N_X}}$	N_A, or N_D
	where: N_X = N at 90% W_{MAX}, N_A or N_D	
Interface Trap Density	$(\psi_S - \psi_0) = \sum_{V_{GS1}}^{V_{GS}\,last}\left(1-\frac{C_Q}{C_{OX}}\right)2V_{STEP}$	ψ_S determined by finding $(\psi_S - \psi_O)$ at V_{FB} and subtracting from all $\psi_S - \psi_0$ values
	$\psi_S - \phi_B - E_T$	
	where: $\phi_B = (kT/q)\ln(N_X/ni)$	
	where: N_X = N at 90% W_{MAX}, N_A or N_B	
	$C_{IT} = (1/C_Q - 1/C_{OX})^{-1} - (1/C_H - 1/C_{OX})^{-1}$	
	$D_{IT} = \frac{(1\times10^{-12})\,C_{IT}}{Aq}$	

APPENDIX D

Prefixes of Unit Values

Exponent	Prefix	Symbol	Exponent	Prefix	Symbol
10^{18}	exa	E	10^{-1}	deci	d
10^{15}	peta	P	10^{-2}	centi	c
10^{12}	tera	T	10^{-3}	milli	m
10^{9}	giga	G	10^{-6}	micro	μ
10^{6}	mega	M	10^{-9}	nano	n
10^{3}	kilo	k	10^{-12}	pico	p
10^{2}	hecto	h	10^{-15}	femto	f
10	deka	da	10^{-18}	atto	a

APPENDIX E

Using the Model 590 and 595 Programs

INTRODUCTION

Two programs included on the Package 82 distribution diskette allow you to run the Model 590 or Model 595 separately, if desired. Of course, the measurement and analysis capabilities of each individual program are somewhat less than for the simultaneous CV software. Table E-1 below summarizes important differences among the three programs.

USING THE MODEL 590 PROGRAM

Follow the procedure below when using the Model 590 program. Refer to Sections 2 and 3 of this manual for details on using the software, which is very similar to the applicable sections of the Package 82 software.

1. With the power off, connect the Model 590 to the IEEE-488 bus of the computer.
2. Turn on the instrument power and allow the unit to warm up for one hour for rated accuracy. During the power-up cycle, verify that the primary address is set to 15. If not, program it for that value.
3. Using the Model 7051 50Ω cables, connect the DUT test fixture directly to the Model 590 INPUT and OUTPUT jacks (do NOT use the Model 5951 Remote Input Coupler). Refer to the Model 590 Instruction Manual for connection information.
4. Boot up the computer in the usual manner and load the program file called "M590CV." Run the program after loading it.
5. Check out system leakages, and perform a probes up suppression, as discussed in paragraph 3.4.
6. Perform cable correction as discussed in paragraph 3.5.
7. Determine C_{ox} using the general procedure covered in paragraph 3.6.
8. Set up your measurement parameters and perform a high-frequency CV sweep on the device. The general procedure is given in paragraph 3.7.
9. Select the analysis option on the main menu, and perform the required analysis operations; see Section 4 and Table E-1 for details.

USING THE MODEL 595 PROGRAM

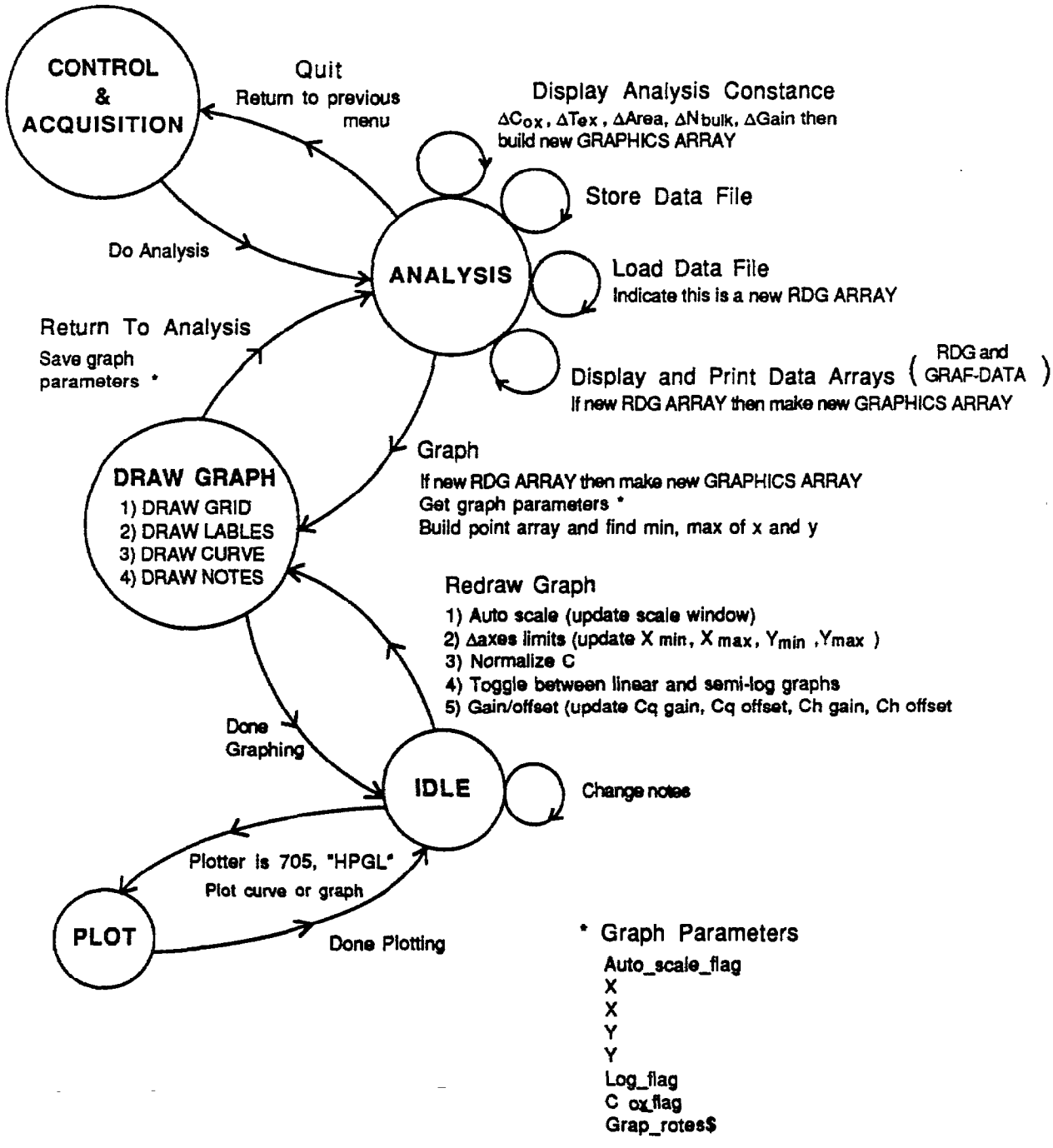
Follow the procedure below to use the Model 595 program. Refer to Sections 2 and 3 of this manual for details on using the Model 595 software. Applicable sections of the Model 595 software are very similar to the corresponding sections of the Package 82 software.

1. With the power off, connect the Model 595 to the IEEE-488 bus of the computer.
2. Turn on the instrument power and allow the unit to warm up for two hours for rated accuracy. Use the MENU button to verify that the primary address is set to 28. If not, program it for that value.
3. Using the Model 4801 low-noise cables, connect the DUT test fixture directly to the Model 595 METER INPUT and VOLTAGE OUTPUT jacks (do NOT use the Model 5951 Remote Input Coupler). Refer to the Model 595 Instruction Manual for connection information, if required.
4. Boot up the computer in the usual manner and load the program file called "M595CV." Run the program after loading it.
5. Check out system leakages, and perform a probes up suppression, as discussed in paragraph 3.4.
6. Determine optimum delay time, as discussed in paragraph 3.6.
7. Set up your measurement parameters, and perform a quasistatic CV sweep on the device. The general procedure is given in paragraph 3.7.
8. Select the analysis option on the main menu and perform the required analysis operation. See Table E-1 and Section 4 for details.

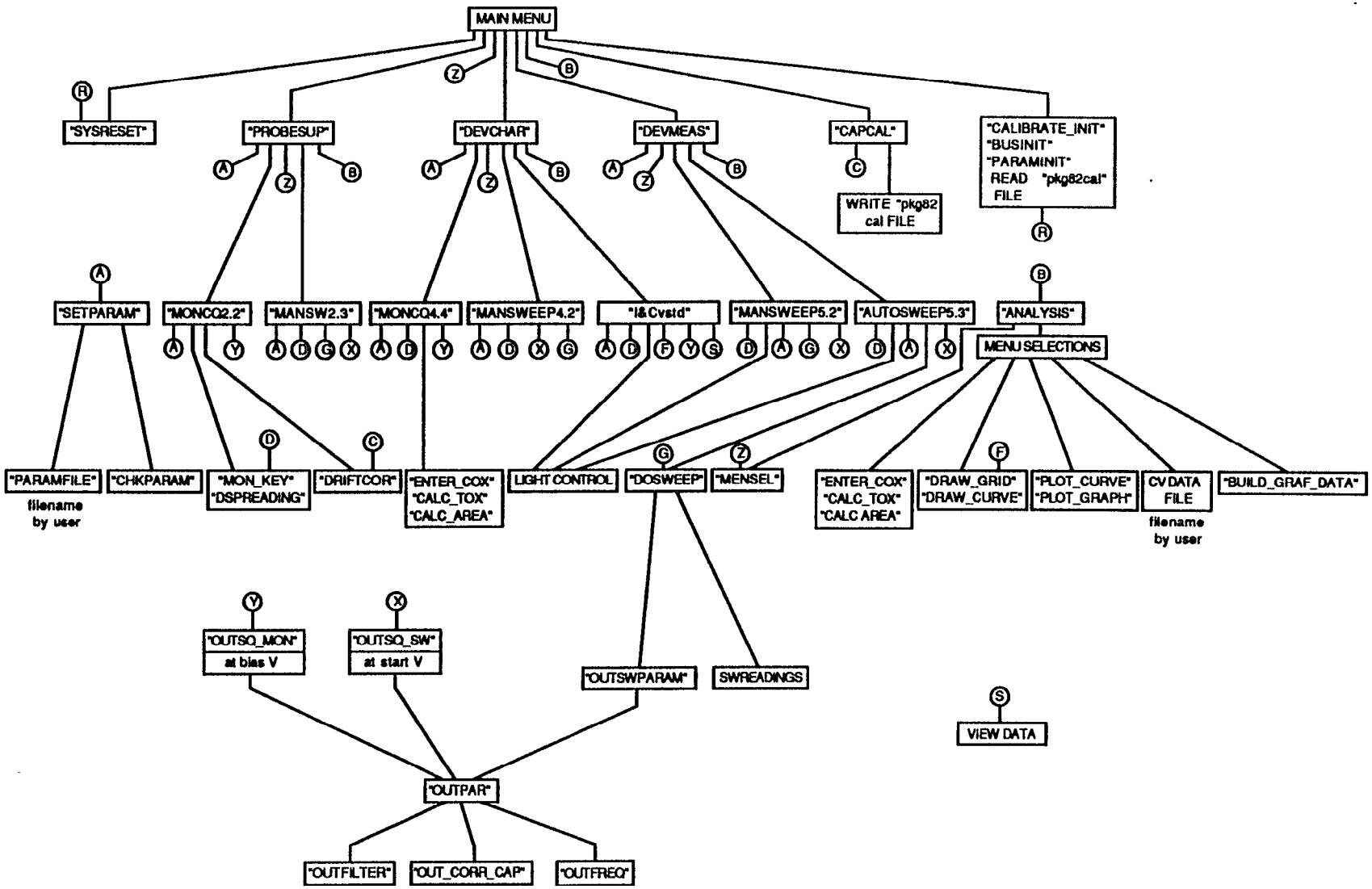
Table E-1. Comparison of Simultaneous CV and Individual Programs

Package 82 Software	Model 590 Software	Model 595 Software
C_Q vs. V_{GS}		C_Q vs. V_{GS}
C_H vs. V_{GS}	C_H vs. V_{GS}	
C_Q & C_H vs. V_{GS}		
Q/t vs. V_{GS}		Q/t vs. V_{GS}
G vs. V_{GS}	G vs. V_{GS}	
w vs. V_{GS}	w vs. V_{GS}	
N vs. w	N vs. w	
$1/C_H^2$ vs. V_{GS}	$1/C_H^2$ vs. V_{GS}	
D_{IT} vs. E_T		
ψ_S vs. V_{GS}		
C_Q vs. ψ_S		
C_H vs. ψ_S		
C_{OX}	C_{OX}	C_{OX}
t_{OX}	t_{OX}	t_{OX}
Area	Area	Area
N_{BULK}	N_{BULK}	
C_{FB}	C_{FB}	
V_{FB}	V_{FB}	
ϕ_{BULK}	ϕ_{BULK}	
L_B	L_B	
Q_{EFF}	Q_{EFF}	
W_{MS}	W_{MS}	
Threshold Voltage	Threshold Voltage	

Package 82 State Transition Diagram



PACKAGE 82 STRUCTURE CHART



KEITHLEY

SERVICE FORM

Model No. _____ Serial No. _____ Date _____

Name and Telephone No. _____

Company _____

List all control settings, describe problem and check boxes that apply to problem. _____

_____

_____

☐ Intermittent
☐ IEEE failure
☐ Front panel operational
☐ Analog output follows display
☐ Obvious problem on power-up
☐ All ranges or functions are bad
☐ Particular range or function bad; specify _____
☐ Batteries and fuses are OK
☐ Checked all cables

Display or output (circle one)

☐ Drifts
☐ Unstable
☐ Overload
☐ Unable to zero
☐ Will not read applied input

☐ Calibration only
☐ Data required
☐ C of C required

(attach any additional sheets as necessary.)

Show a block diagram of your measurement system including all instruments connected (whether power is turned on or not). Also, describe signal source.

Where is the measurement being performed? (factory, controlled laboratory, out-of-doors, etc.)

_____

_____

What power line voltage is used? _____ Ambient Temperature? _____ °F

Relative humidity? _____ Other? _____

Any additional information. (If special modifications have been made by the user, please describe.) _____

_____

Be sure to include your name and phone number on this service form.

KEITHLEY

Keithley Instruments Division / Keithley Instruments, Inc.
28775 Aurora Road / Cleveland, Ohio 44139 / U. S. A. / (216) 248-0400 / Telex: 98-5469 / Fax: (216) 248-6168

WEST GERMANY:	Keithley Instruments GmbH / Heiglhofstr. 5 / Munchen 70 / 089-71002-0 / Telex: 52-12160 / Telefax: 089-7100259
GREAT BRITAIN:	Keithley Instruments, Ltd. / 1 Boulton Road / Reading, Berkshire RG 2 ONL / 0734-861287 / Telex: 847 047 / Telefax: 0734-863665
FRANCE:	Keithley Instruments SARL / 3 Allee du 10 Rue Ambroise Croizat / B. P. 60 / 91121 Palaiseau/Cedex 1-6-0115 155 / Telex: 600 933 / Telefax: 1-6-0117726
NETHERLANDS:	Keithley Instruments BV / Avelingen West 49 / 4202 MS Gorinchem / P.O. Box 559 / 4200 AN Gorinchem / 01830-35333 / Telex: 24 684 / Telfax: 01830-30821
SWITZERLAND:	Keithley Instruments SA / Kriesbachstr. 4 / 8600 Dubendorf / 01-821-9444 / Telex: 828 472 / Telefax: 0222-315366
AUSTRIA	Keithley Instruments GesmbH / Rosenhugelstrasse 12 / A-1120 Vienna / (0222) 84 65 48 / Telex: 131677 / Telefax: (0222) 84 35 97
ITALY:	Keithley Instruments SRL / Viale S. Gimagno 4/A / 20146 Milano / 02-4120360 or 02-4156540 / Telefax: 02-4121249