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Service Guide

HP 8133A 3 GHz Pulse Generator

HEWLETT PACKARD

HE Part No. 08133-91021
Printed in Germany March 1994

Edition 1.1
E0394

Warranty
The information contained in this document is subject to change without notice.
Hewlett-Packard makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties or merchantibility and fitness for a particular purpose.
Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this material.

Complete product warranty information is given in the User Guide.

Safety
This is a Safety Class 1 instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under **Safety** Symbols.

Warning
Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective earth conductor of the (mains) power cord. The mains plug must only be inserted in a socket outlet with a protective earth contact. Do not negate the protective action by using an extension power cord without a protective grounding conductor. Grounding one conductor of a two-conductor outlet is not sufficient protection.

Service instructions are for trained service :personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

If you energize this instrument using an auto-transformer (for voltage reduction) make sure that the common terminal is connected to the earth terminal of the power source.

Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

Do not install substitute parts or perform any unauthorized modification to the instrument.

Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

Safety Symbols

Instruction Manual symbol: The instrument is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the instrument.

Hazardous voltage symbol.

Earth terminal symbol: used to indicate a circuit common connected to grounded chassis.

Protected conductor symbol

WARNING
The Warning symbol calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury or loss of life. Do not proceed beyond a Warning symbol until the indicated conditions are fully understood and met.

CAUTION
The Caution symbol calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the equipment. Do not proceed beyond a Caution symbol until the indicated conditions are fully understood and met.

Notice

Warranty

This Hewlett-Packard product has a warranty against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Hewlett-Packard. The Buyer shall pay Hewlett-Packard's round-trip travel expenses.

For products returned to Hewlett-Packard for warranty service, the Buyer shall prepay shipping charges to Hewlett-Packard and Hewlett-Packard shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties and taxes for products returned to Hewlett-Packard from another country.

Hewlett-Packard warrants that its software and firmware designated by Hewlett-Packard for use with an instrument will execute its programming instructions when properly installed on that instrument. Hewlett-Packard does not warrant that the operation of the instrument software, or firmware, will be uninterrupted or error free.

Limitation of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by the Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

No other warranty is expressed or implied. Hewlett-Packard specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

Exclusive Remedies

The remedies supplied are the Buyer's sole and exclusive remedies. Hewlett-Packard shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract, tort or any other legal theory.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products. For any assistance, contact your nearest Hewlett-Packard Sales Office.

Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States Institute of Standards and Technology, to the extent allowed by the Institute's calibrating facility, and to the calibration facilities of other International Standards Organization members.

About this edition

HP Part Number
08133-91021

Printed in Germany

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About this book

This book is a guide to testing, troubleshooting and servicing the HP 8133A 3 GHz Pulse Generator.

Introducing the HP 8133A Pulse Generator

A summary of the instrument options, frontpanel, interchannel timing relationships, and using the frontpanel Vernier Keys, plus Installation instructions, with details of setting the line voltage.

HP 8133A Pulse Generator Specifications

The HP 8133A Pulse Generator's warranted specifications and other characteristics.

Testing the HP 8133A Pulse Generator

Performance and Verification tests for testing the instrument.

Troubleshooting A series of flowcharts to assist troubleshooting in the Power Supplies down to component level, plus general tests to establish the general area of a fault.

Replacing Assemblies A guide to removing and replacing the main assemblies of the HP 8133A Pulse Generator.

Replaceable Parts Lists of parts that can be replaced in the HP 8133A Pulse Generator.

Theory of Operation Functional description of the HP 8133A Pulse Generator PC boards.

Making Adjustments Information on adjustments and recalibration of the HP 8133A Pulse Generator.

CLIP Component level information package.

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Introducing the HP 8133A Pulse Generator

This chapter contains the following information:

- A summary HP 8133A Pulse Generator models currently available
- An overview of the front panel
- Interchannel Timing relationships
- How to use the Vernier keys
- Installing the HP 8133A Pulse Generator

Summary of HP 8133A Models

HP 81338 Single-channel 3 GHz Pulse Generator.
Selectable variable delay OR pulse-width.

HP 81338 Option 001 Single-channel 3 GHz Pulse Generator.
Simultaneously variable delay AND pulse-width.

HP 81338 Option 002 Dual-channel 3 GHz Pulse Generator.
Channel 1 same as HP 8133A Option 001
Channel 2 PULSE/DATA Channel:

Selectable: Divided Squarewave
OR 32-Bit programmable data
OR PRBS $2^{23}-1$

HP 81338 Option 003 Dual-Channel 3 GHz Pulse Generator.
Channel 1 same as HP 8133A Option 001
Channel 2 same as HP 8133A

Frontpanel Overview

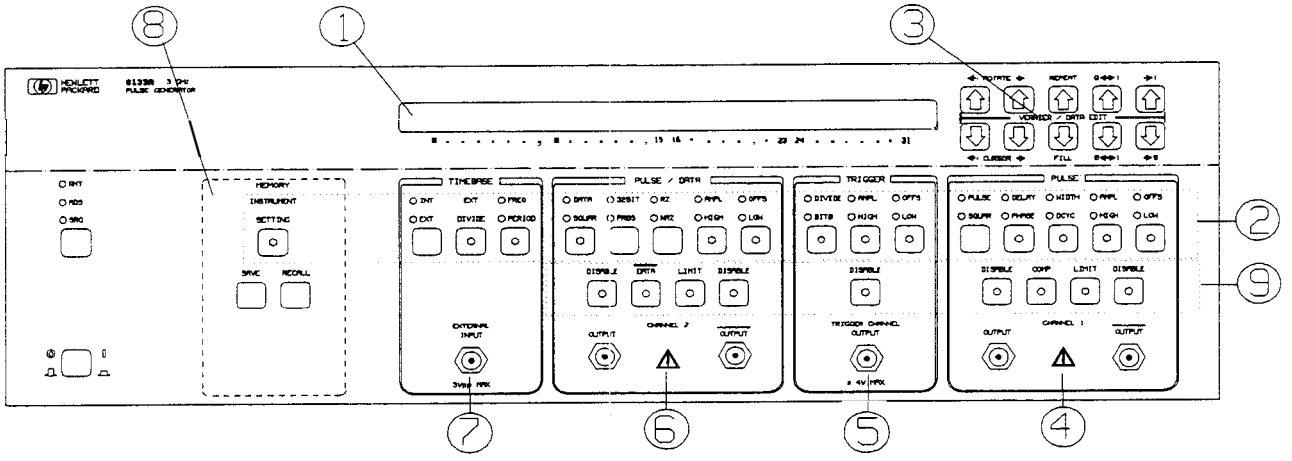


Figure 1-1. HP 8133A Frontpanel overview

① The *Display* shows the **active parameter** and one other parameter.

② Choose the **active parameter** using the **Mode/Parameter Keys**

③ Edit the **active parameter** using the VERNIER Keys. The **32** BIT **DATA** editing functions are indicated **in blue** (Option 002 only).

④ PULSE Channel **1** controls and output connectors.

⑤ TRIGGER Channel controls and output connector.

⑥ Optional Channel 2 controls and output connectors. (Option 002 PULSE/DATA , Option 003 PULSE)

⑦ Use the TIMEBASE keys to control the instrument frequency.

⑧ Use the MEMORY keys to save and recall instrument settings.

⑨ Use the **Control keys** to control the output modes.

Active Parameter The active parameter is the parameter which can be adjusted using the VERNIER keys. It is the *bright* parameter on the display, and the LED in the **parameter key** is lit.

Mode keys Mode keys toggle between different operating modes. They are located in the upper row of keys, see Figure 1-1. The LEDs above the key indicate which mode is selected.

Parameter keys Parameter keys activate a parameter on the display. They are located in the upper row of keys, see Figure 1-1. Press once to activate the selected parameter indicated by the LEDs above the key. Press again to select and activate the alternative parameter. The LED in the key indicates that the parameter is active in the display.

Control keys Control keys toggle an output mode on or off. They are located in the lower row of keys, see Figure 1-1. The LED in the key is lit when the mode is on.

Interchannel Timing relationships

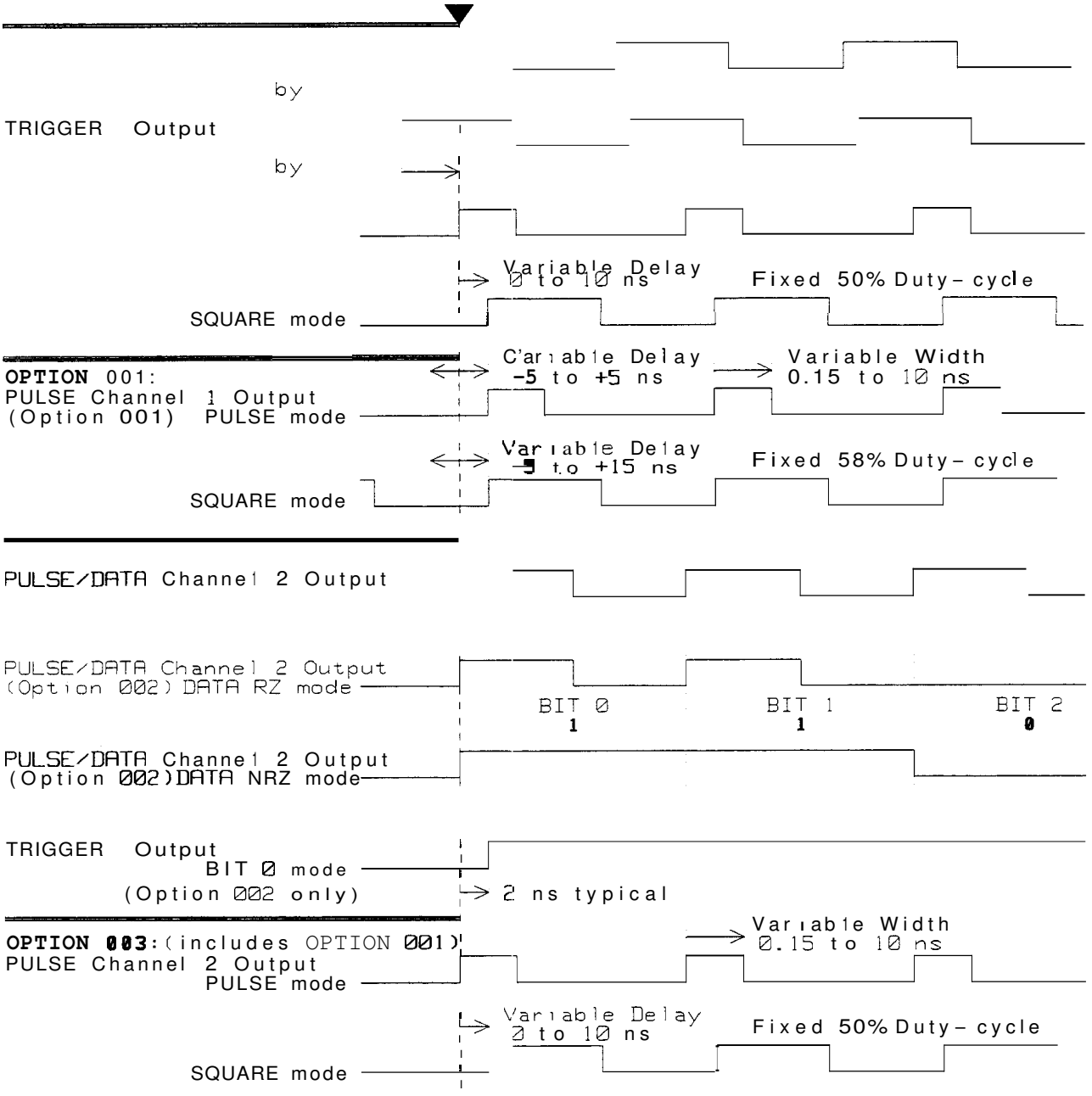
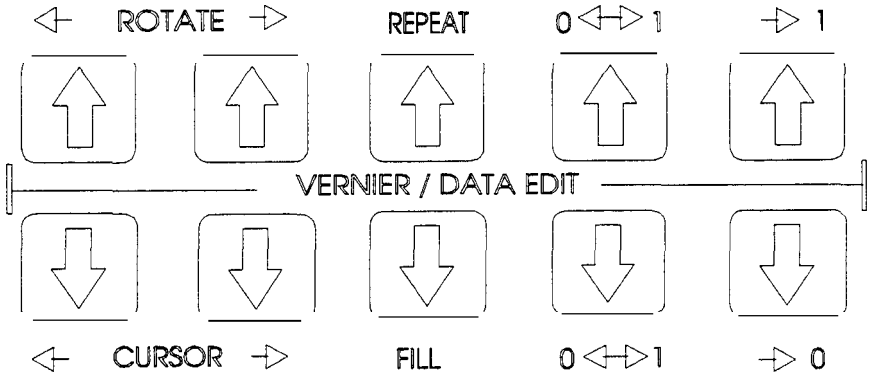


Figure 1-2. HP 8133A Interchannel Timing Diagram

Using the VERNIER keys



Summary

Use the **VERNIER** keys to adjust the value of the active parameter. Only one parameter can be active at a time, although two may be visible on the display. The active parameter is

- the *bright* parameter on the display.
- indicated by LEDs in and above a **mode/parameter key** (See Figure 1-1).

Each pair of keys controls the corresponding digit of the parameter:

Press once to increment digit by 1

Press once to decrement digit by 1

Hold a key down to auto-repeat and smoothly change a parameter. If you hold two neighbouring keys down, the auto-increment (or decrement) steps at a rate of three times the lower digit.

A decimal-carry operates when you change a digit from 9 to 0 or from 0 to 9. Leading zeroes are not displayed, but the vernier keys can still be used to increase/decrease the "digit". If you try to adjust a parameter outside its valid range, you will see an error message telling you the parameter limit.

Example - Adjusting the Frequency

After recalling the Standard settings, the display shows the standard Period and Channel 1 Width settings. The Period is the active parameter and appears brighter:

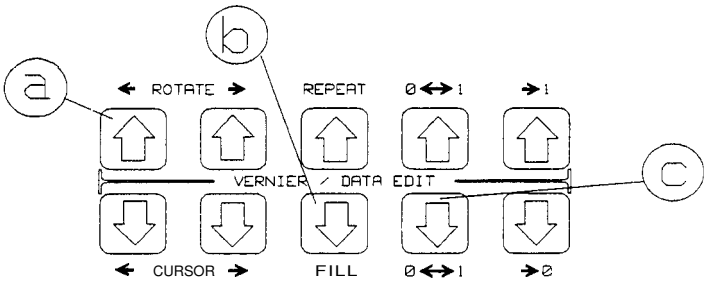
```
Per  30.303 ns 1:Wid  150 ps
```

1. Press **TIMEBASE** (FREQ/PERIOD) to activate the Frequency parameter.

   The PERIOD LED switches off and the FREQ LED switches on. The LED in the key remains on, indicating that this is still the active parameter. The display now shows the timebase Frequency:

   ```
   Freq  33.0 MHz 1:Wid  150 ps
   ```

2. Use the VERNIER keys to increase the timebase Frequency to 1.0000 GHz:



a. Press the ↑ ↑↑↑↑ key once:
   Freq 1.0330 GHz
b. Press the ↓↓ ↓ ↓↓ key three times:
   Freq 1.0030 GHz
c. Press the ↓↓↓ ↓ ↓ key three times:
   Freq 1.0000 GHz

Installing the HP 8133A Pulse Generator

Initial Inspection

Inspect the shipping container for damage. If the container or cushioning material is damaged, keep it until the contents of the shipment have been checked for completeness and the instrument has been verified both mechanically and electrically.

Warning

To avoid hazardous electric shock, do not perform electrical tests when there are signs of shipping damage to any part of the instrument's outer covers or panels.

If the contents are incomplete, or there is mechanical damage, or if the instrument does not pass the Performance Tests in Chapter 3, notify the nearest Hewlett-Packard office. Keep the shipping materials for inspection by the carrier. The HP office will arrange for repair or replacement without awaiting settlement.

Power Requirements and Line Voltage Selection

Power Requirements

Caution

BEFORE APPLYING AC LINE POWER TO THE HP 81338 Pulse Generator, ensure that the instrument is set to the local line voltage and the correct line fuse is installed in the fuse holder.

The HP 8133A Pulse Generator can operate from any single-phase AC power source supplying 100 V, 120 V, 220 V or 240 V in the frequency range from 50 to 60 Hz (see Table 1-1). The maximum power consumption is 250 VA with all options installed.

Table 1-1. Line Voltage Ranges

Selector Voltage	AC Voltage Range
100	90 - 110 V
120	108 - 132 V
220	198 - 242 V
240	216 - 264 V

The line voltage selector is set at the factory to correspond to the most commonly used line voltage of the country of destination. The switch is combined with the power line voltage receptacle on the rear panel. Refer to Table 1-1 for the line voltage ranges and Table 1-2 to set the line voltage and select the appropriate fuse.

Table 1-2. Line Voltage and Fuse Selection

Line Voltage	Fuse Type	*HP* Part Number
100 V / 120 V	T 3A, 250 V	2110-0029
220 V / 240 V	T 1.5A, 250 V	2110-0304

Selecting the Line Voltage and Replacing the Fuse

1. Remove the power cord.
2. Insert a screwdriver into the recess at the side of the assembly.
3. To change the voltage setting, the selector must be removed and then replaced with the new setting value displayed.
4. If necessary, change the fuse in accordance with the new voltage setting.

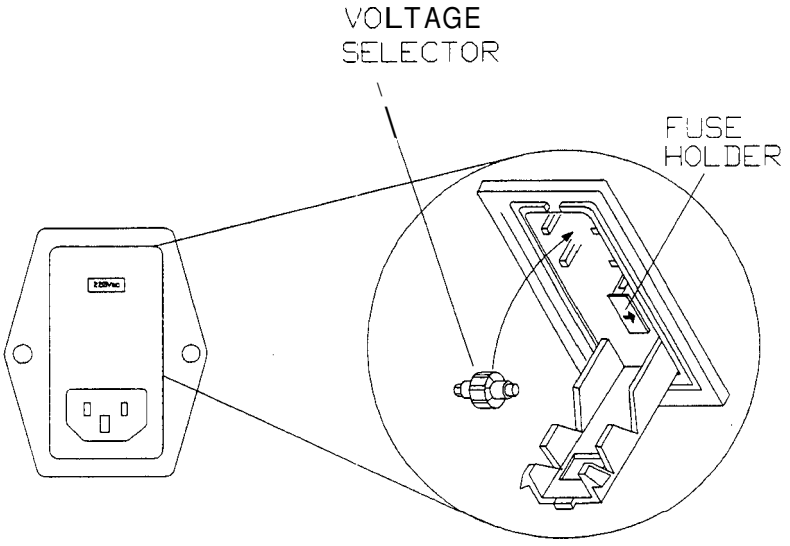


Figure 1-3. Line Voltage Switch Assembly

Power Cable

In accordance with international safety standards, this instrument is equipped with a three-wire power cable. When connected to an appropriate AC power receptacle, this cable grounds the instrument cabinet. The type of power cable shipped with each instrument depends on the country of destination. Refer to Figure **1-4** for the part numbers of the power cables available.

Warning

To avoid the possibility of injury or death, the precautionary Warnings given on the inside front-cover of the manual must be followed before the instrument is switched on.

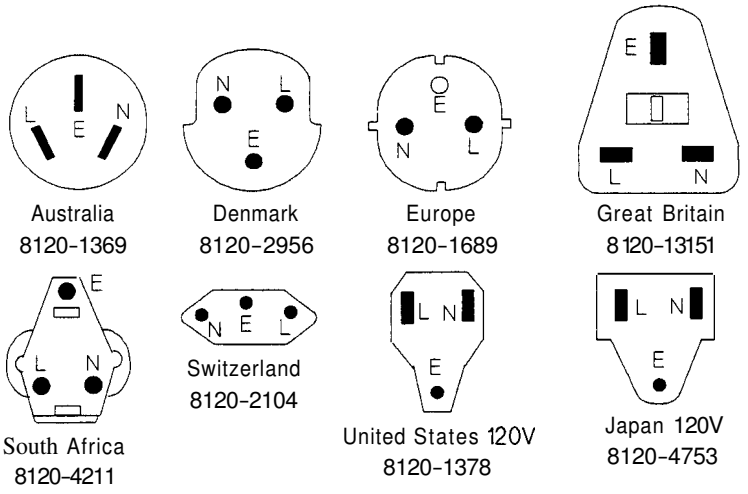


Figure 1-4. Power Cables - Plug Identification

The following work should be carried out by a qualified electrician - all local electrical codes being strictly observed. If the plug on the

cable does not fit the power outlet, or the cable is to be attached to a terminal block, cut the cable at the plug end and re-wire it.

The color coding used in the cable will depend on the cable supplied. If a new plug is to be connected, it must meet local safety requirements and include the following features:

- Adequate load-carrying capacity (see table of specifications).
- Ground connection.
- Cable clamp.

Ventilation Requirements

The HP 8133A Pulse Generator is fitted with two cooling fans. Make sure that there is adequate clearance of 3 inches (75 mm) at the rear and 1 inch (25 mm) at the sides to ensure adequate airflow. If the airflow is restricted the internal operating temperature will be higher, reducing the instrument's reliability.

Mounting Hardware

Table 1-3. Mounting Accessories

Mounting Accessors	HP Part Number
Front Handle Kit	5062-3989
Rack Mount Flange Kit	5062-3987
Front Handle and Flange Kit	5062-3983

2

HP 8133A Pulse Generator Specifications

Specifications describe the instruments warranted performance after a 30 minute warm-up period, with ambient temperature in the range 0 to 55°C, and 50 Ω load resistance at all outputs.

Non-warranted characteristics are described as 'typical' or 'nominal'.

All timing parameters are measured at 50% of amplitude.

Internal Clock

You can set the internal clock in terms of frequency or period:

	FREQUENCY	PERIOD
Range:	33.0 MHz to 3.0000 GHz	333 ps to 30.303 ns
Resolution:	3.5 digits, best case 100 kHz	3.5 digits, best case 1 ps
Accuracy:	±0.5% (±0.1% typical)	
Repeatability:	4 times better than accuracy	

External Clock

External Input

You can apply an external clock signal to the External Input:

Frequency Range:	33 MHz to 3 GHz
Input Coupling:	ac-coupled
Impedance:	50 Ω nominal
Minimum Swing:	300 mV, rise-time < 3 ns 0 dBm sinewave
Maximum Amplitude:	$3V_{pp}$, ±20 V_{dc}

External Frequency Counter

You can measure and display the frequency of the external clock signal:

	FREQUENCY	
	33 MHz to 3.00 GHz (2 MHz to 3.50 GHz typical)	333 ps to 30.3 ns (286 ps to 500 ns typical)
Resolution:	10 kHz	1 ps
Accuracy:	±0.1%	

External Divide

You can divide the external clock signal by:
(1), 2, 4, 8, 16, 32, 64
as long as the internally available (divided) signal frequency > *33* MHz. (The instrument will continue to function down to *3* MHz, except for Option 002 PULSE/DATA Channel 2.)

TRIGGER

All specification:; apply for Trigger Output frequency > 33 MHz.

Timing

	DIVIDEd mode	BIT *0* mode (Option *002* only)
Signal Format:	fixed Duty-cycle **50%** nominal	
Transition Times (20% – 80%):	< **100** ps (typically < 60 ps)	
RMS Jitter:	< **5** ps (< 2 ps typical)	
Frequency:	Timebase Frequency divided by : (1), 2, **4,** 8, 16, 32 or **64** (**Minimum:3** MHz typical)	Timebase Frequency divided by 32
Propagation Delay:	**6** ns typical, External Input to Trigger Channel Output, with Trigger and External Dividers = 1	-2.0 ns typical, Start of Bit 0 on Channel 2 to Trigger Channel Output

Output Levels

You can set the Trigger Output levels in terms of either Amplitude/Offset or High-Low-level. Levels apply for a 50 Ω load, offset level doubles into open circuits:

Voltage Window:	-4.00 V to +4.00 V
Amplitude Range:	**0.50** V to 1.80 V
Resolution:	10 mV
Maximum External Voltage:	±4 V

PULSE and PULSE/DATA

PULSE Timing (Channel 1 and Option 003 Channel 2)

		CHANNEL 1 or CHANNEL 2 (OPT 003)		CHANNEL 1 with OPT 001,002 or 003	
		PULSE mode	SQUARe mode	PULSE mode	SQUARe mode
Delay[1]	Range:	Not Applicable	0.000 ns to 10.000 ns	-5.000 ns to +5.000 ns	-5.000 ns to +15.000 ns
	Resolution:	Not Applicable	1 ps		
	Accuracy:	Not Applicable	±50 ps[2]		
Phase[1]	Range:	Not Applicable	0° to 3600°	-3600° to +3600°	
	Resolution:	Not Applicable	0.1°		
Width[3]	Range:	150 ps to Period−150 ps (Max. 10.000 ns)	Not Applicable	150 ps to Period−150 ps (Max. 10.000 ns)	Not Applicable
	Resolution:	1 ps	Not Applicable	1 ps	Not Applicable
	Accuracy:	±100 ps (±30 ps typical)	Not Applicable	±100 ps (±30 ps typical)	Not Applicable
Duty-cycle[3]	Range:	0% to 100%	Not Applicable	0% to 100%	Not Applicable
	Resolution:	0.1%, best case 1 ps	Not Applicable	0.1%, best case 1 ps	Not Applicable
Skew[4]	Max.Range:	Not Applicable	-5.000 ns to +5.000 ns		
Transition Times	10% - 90%:	< 100 ps (< 60 ps typical)			
	20% - 80%:	< 60 ps (< 40 ps typical)			
RMS Jitter:		< 5 ps (< 1 ps typical)			
Propagation Delay:		18.8 ns typical, Trigger Output to Channel Output, Trigger ÷ 1			

1 The Delay and Phase parameters are mutually exclusive. Phase settings are also subject to Delay, Skew and Period specifications and settings.

2 Delay variation only, if other parameters vary ±150 ps (±30 ps typical).

3 Width and Duty-cycle parameters are mutually exclusive. The Duty-cycle setting is also subject to the Width specification and setting.

4 Skew + Delay (or Phase) must be within the limits given under Delay above. The Delay specifications assume Skew = 0.

PULSE Frequency (Option 003 Channel 2)

The output frequency of Option 003 Channel 2 can be divided in both PULSE and SQUARe modes:

	CHANNEL 2	
	PULSE mode	SQUARe mode
Frequency:	Timebase frequency divided by:[1] (1); 2, 4, 8, 16, 32, 64 (Minimum: 3 MHz typical)	

1 The TRIGGER frequency must also be divided by the same (or higher) divisor

PULSE/DATA Timing (Option 002 Channel 2)

	CHANNEL 2 (OPT 002)		
	SQUARe mode	DATA mode	
		32 BIT	PRBS
Propagation Delay:	18.8 ns typical, Trigger Output to Channel Output, Trigger ÷ 1 or -2.0ns typical, Trigger Output to Channel Output, Trigger on Bit 0		
Frequency:'	Timebase Frequency divided by: (1), 2, 4, 8, 16, 32	Timebase Frequency	
Signal Format:	fixed Duty-cycle 50% nominal	32 bits programmable data RZ/NRZ selectable	PRBS $2^{23}-1$, CCITT 0.151 Norm
RMS Jitter:	< 5 ps (< 2 ps typical)		< 10 ps typical'
Transition Times (10%- 90%)	< 100 ps (< 60 ps typical)		
Transition Times (20%- 80%)	< 60 ps (< 40 ps typical)		

Output Levels

Each channel has **50 Ω** (nominal) differential outputs (OUTPUT and $\overline{\text{OUTPUT}}$) at SMA connectors on the frontpanel. You can set the Output levels in terms of either Amplitude/Offset or High-Low-level (Levels double when driving into open circuits):

Voltage Window:	-2.00 V to +4.00 V
Amplitude Range:	0.30 V to 3.00 V
Settling Time:	1 ns
Resolution:	10 mV
Level Accuracy:	±2% f2% of Amplitude ±20 mV
Overshoot, Ringing:	< 15% of Amplitude f20 mV
Maximum External Voltage:	f 3 V
Inter-output Skew:	< 20 ps typical (OUTPUT/$\overline{\text{OUTPUT}}$)
Short-circuit Current:	-80 mA < I_{sc} < 160 mA typical

Output Modes

LIMIT — You can limit the maximum High- and Low-levels (into 50 Ω) to protect the device-under-test. When you first switch on LIMIT mode, the current levels are declared as level-limits which cannot be exceeded until you switch off LIMIT mode.

COMPlement — On a PULSE channel, you can complement the output signal by switching on COMPlement mode.

DISABLE — You can disable the output signal by switching on DISABLE mode. The signal is disconnected from the output connectors using internal relays.

$\overline{\text{DATA}}$ — On a PULSE\DATA channel (Option 002 only), you can logically complement the data by switching on $\overline{\text{DATA}}$ mode.

HP-IB Capabilities

- All modes and parameters are programmable.
- Operates according to IEEE 488.1 and 488.2, 1987.
- Conforms, where appropriate, to the Standard Commands for Programmable Instruments (SCPI) 1991.0.

Additional Features

Non-volatile Memory

- Current settings are saved on power-down.
- Additionally, 20 complete settings can be saved and recalled.

Rearpanel Connectors

Channel 1 Input & Output

For normal operation the Input and Output have to be connected using the rigid coaxial link supplied.

For multi-channel timing applications delay-lines from the HP 15436A multi-channel delay-line set are substituted for the standard links.

Output Amplitude:	**2 V_{pp}, ac-coupled**
Input Amplitude:	**Max. 2.5 V_{pp}, ac-coupled** **Min. 1.0 V_{pp}, ac-coupled**

Channel 2 Input & Output

These are only fitted to an Option 002 or 003 instrument. The specifications are the same **as** for Channel 1.

Start/Stop Input

The Start/Stop Input is part of the PULSE/DATA Channel 2 (Option 002). It can be used to stop the data-stream in order to set up a data pattern and start data generation from Bit 7.

Interface:	**dc-coupled**
Impedance:	**50 Ω nominal**
Transitions:[1]	< 1 ns
Start Level:	**0 V (default)**
Stop Level:	**-0.4 V**
Max.Levels:	**-0.8 - +0.4 V**

1 You should use a clean signal, for example from a pulse generator. Noisy transitions, for example switch bounce, can confuse the Data circuits.

General Information

Operating Environment

Storage Temperature:	-40°C to +70°C
Operating Temperature:	0°C to 55°C
Humidity:	95% R.H. (0°C to 40°C)

Warning

- The **HP 8133A** Pulse Generator is not designed for outdoor use. Do not expose the **HP 8133A** Pulse Generator to rain or other excessive moisture. Protect the **HP 8133A** Pulse Generator from humidity and temperature changes which could cause condensation within the instrument.
- Do not operate the **HP 8133A** Pulse Generator in the presence of flammable gases, fumes or powders. Operation of any electrical instrument in such **an** environment constitutes a definite safety hazard.

Power Requirements

110-120/220-240 V_{rms} ±10%
250 **VA** max.
47-63 Hz

Weight

Net: 21.5 kg (48 lb)
Shipping: 29 kg (65 lb)

Dimensions (H×W×D)

145 mm x 426 mm x 525 mm
(5.7 in x 16.75 in x 20.65 in)

Ventilation Requirements

The HP 8133A Pulse Generator is fitted with two cooling fans. Make sure that there is adequate clearance of 3 inches (75 mm) at the rear and 1 inch (25 mm) at the sides to ensure adequate airflow. **If** the airflow is restricted the internal operating temperature will be higher, reducing the instrument's reliability.

Acoustic Noise Emission

For ambient temperature up to 30°C, under normal operation and at the typical operator position:

LpA = 41 dB

Measured in accordance with ISO 6081.

Recalibration Period 1 year recommended

Declaration of Conformity

Manufacturer: Hewlett-Packard GmbH
Boboblingen Instruments Division
Herrenberger Str. 130
D-7030 Boboblingen Germany

We declare that the product ***HP* 8133A 3 GHz Pulse Generator** conforms to the following standards:

Safety: IEC 1010-1 (1990)

EMC: EN 55011 (1991) / CISPR 11 Group 1, Class B

EN 50082-1 (1991)

IEC 801-2 ESD: 4kV cd, 8kV ad
IEC 801-3 Radiated Immunity: 3V/m
IEC 801-4 Fast Transients: 0.5kV, 1kV

Supplementary Information

During the measurements against EN 55011, the I/O ports were terminated with their normal impedance, the HP-IB connector was terminated with the cable HP 10833B. When the product is connected to other devices, the user must ensure that the connecting cables and the other devices are adequately shielded to prevent radiation.

Böboblingen, 29th January 1992

Robert Hofgärtner
Quality Assurance Manager

3

Testing the HP 8133A Pulse Generator

Use the tests in this chapter if you want to check that the HP 8133A Pulse Generator is working correctly. Before starting any testing:

- Recall the HP 8133A Pulse Generator Standard Settings from Memory 0.
- Let the HP 8133A Pulse Generator and all other test equipment warm up for at least 30 minutes.

The tests are divided into the following sections:

TIMEBASE	Applies to all instruments.
TRIGGER	Applies to all instruments
Outputs	Applies to each Output Channel. The tests in this section need to be repeated for both channels in a dual channel instrument. Not all the tests apply to both PULSE and PULSE/DATA Channels, see Table 3-3.

Within each section carry out the tests in the order given.

All tests which test the instrument against its warranted specifications are called **Performance** tests, and the results can be recorded on the Performance Test Record at the end of the chapter.

The **Verification** tests verify the instrument's non-warranted characteristics.

Recommended Test Equipment and Accessories

The following tables list the recommended test equipment you need to carry out all the tests in this chapter. You can use alternative instruments as long as they meet the critical specifications given. The test set-ups and procedures assume you are using the recommended equipment.

Table 3-1. Recommended Test Equipment

Type	Model	Critical Specifications
Oscilloscope	HP 54120 Series with 2.5 GHz Trigger Recommended: HP 54121T or HP 54124T	Timing Accuracy: ≤10 ps ±0.1% of readiq Bandwidth: ≥20 GHz Risetime: 517.5 ps DC Accuracy: ±0.4% of fullscale f.2 mV Jitter: ≤2.5 ps + 5%10^{-5}× delay setting Input Impedance: 500 nominal
Counter	HP 5334B Opt 030 HP 8133A	Range:% 1300 MHz, 9 digit mantissa Range:To 3.33 GHz (333 ps to 30.3 ns) Accuracy: ±0.1%
Pulse Generator	HP 8133A	3 GHz pulses (333 ps period) 33 MHz pulses (30.303 ns period) Accuracy: ±0.5%

Table 3-2. Recommended Accessories

Type	Model	Critical Specifications
Attenuator	33340C #020	20 dB, dc-26.5 GHz, APC -3.5
Cables	8120-4948	50Ω SMA (m-m)
Adapters	1250-1200	SMA (m) to BNC (f)
	1250-2015	SMA (f) to BNC (m)
	1260-1700	SMA (f) to BNC (m)
	1260-1169	SMA (m-m)
Power Splitter	11667B	50Ω, dc-26.5 GHz, APC -3.5
Torque Wrench	8710-1682	5/16 in, 5 lb-in (56 Ncm)

TIMEBASE

Tests

Carry out the following tests in order:

1. Internal Clock— Low Frequency Performance
2. TRIGGER Divider Verification
3. External Frequency Counter Performance
4. External Divider Verification
5. Internal Clock—High Frequency Performance

Equipment

- Low Frequency Counter to 100 MHz (HP 5334B)
- High Frequency Counter to 3.33 GHz (HP 8133A)
- 2 x Cable (SMA m-m)
- Adapter (SMA (f) to BNC (m))

Internal Clock—Low Frequency Performance

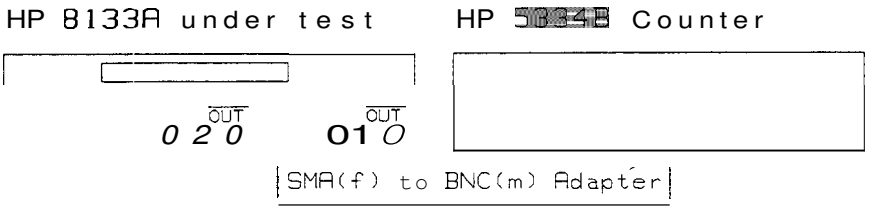


Figure 3-1. Internal Clock Low Frequency Test Set-up

1. Connect the HP 8133A Pulse Generator **TRIGGER** Output to the HP 5334B Counter Input A **as** shown in Figure 3-1
2. Set up the Counter as follows:

   PER A
   AUTO TRIG OFF
   LEVEL 0.0 V
   GATE TIME 1 ms
   100 Gate Averages

3. Set up ithe HP 8133A Pulse Generator under test as follows:

TIMEBASE	INT/EXT	INTernal
	FREQ/PERIOD	PERIOD 30.000 ns
TRIGGER	AMPL/HIGH	HIGH +0.5 V
	OFFS/LOW	LOW -0.6 V
	DIVIDE/BIT0	DIVIDE ÷1
	DISABLE	Off (Output enabled

4. Check that the measured period is 30.00 ns ±0.15 ns, and record the measured period on the Test Record.
5. Adjust ithe HP 8133A Pulse Generator period to 10.000 ns.
6. Check that the measured period is 10.00 ns ±0.05 ns, and record the measured period on the Test Record.

TRIGGER Divider Verification

7. Disable the Counter's 100 Gate Averages mode.
8. Adjust the HP 8133A Pulse Generator under test period until the *measured* period is 10.00xx ns (that is, to an accuracy of 2 decimal places).

9. Adjust the TRIGGER Divider through its possible values and verify that the measured period varies accordingly:

Divider	Measured Perio
÷2	20.00xx ns
	40.00xx ns
	80.00xx ns
÷16	160.0xx ns
÷32	320.0xx ns
÷64	640.0xx ns

10. Adjust the TRIGGER Divider back to 1.

External Frequency Counter Performance

Low Frequency

11. Set up a *second* HP 8133A Pulse Generator as an External Clock source. Recall the Standard Setting, and then set up the following:

TIMEBASE	INT/EXT	INTernal
	FREQ/PERIOD	PERIOD 10.000 ns
TRIGGER	AMPL/HIGH	HIGH +0.5 V
	OFFS/LOW	LOW -0.5 V
	DIVIDE/BIT0	DIVIDE ÷1
	DISABLE	Off (Output enabled)

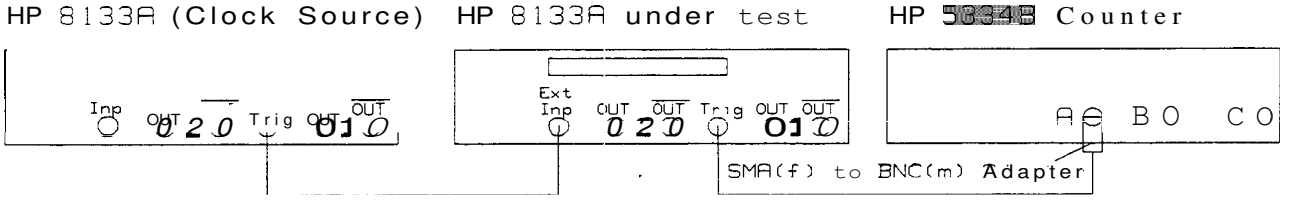


Figure 3-2. External Frequency Counter Low Frequency Test Set-up

12. Connect the ***second*** HP 8133A Pulse Generator Trigger Channel Output to the External Input of the HP 8133A Pulse Generator under test.

13. Set up the HP 8133A Pulse Generator under test as follows:

TIMEBASE	INT/EXT	EXTernal
	FREQ/PERIOD	PERIOD
	EXT DIVIDE	÷1

14. Adjust the ***second*** HP 8133A Pulse Generator period (clock source) until the *measured* period on the Counter is 10.00xx ns.

15. Check that the measured period on the HP 8133A Pulse Generator under test is 10.00 ns ±0.01 ns, and record the result on the Test Record.

External Divider Verification

16. Adjust the TIMEBASE External Divider on the HP 8133A Pulse Generator under test through its possible values and verify that the measured period on the Counter varies accordingly:

Ext Divider	Measured Perio
	20.00xx ns
	40.00xx ns
	80.00xx ns
f16	160.0xx ns
f32	320.0xx ns
÷64	640.0xx ns

17. Adjust the TIMEBASE External Divider back to 1.

External Frequency Counter Performance

High Frequency

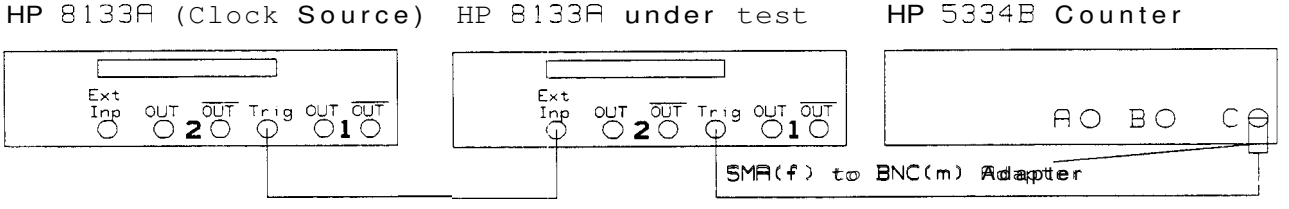


Figure 3-3. External Frequency Counter High Frequency Test Set-up

18. Reconnect the HP 8133A Pulse Generator TRIGGER output to the high frequency Input C of the HP 5334B Counter.
19. Set the Counter to measure the frequency of Input C.
20. Set up the HP 8133A Pulse Generator under test as follows:

TIMEBASE	INT/EXT	EXTernal
	FREQ/PERIOD	FREQ
	EXT DIVIDE	& divl;

21. Adjust the frequency of the *second* HP 8133A Pulse Generator until the *measured* frequency on the Counter is 1.000X GHz ± 0.0002 GHz.

22. Set up the ***second*** (Clock Source) HP 8133A Pulse Generator **as** follws:

TIMEBASE	EXT/INT	INTernal
	FREQ/PERIOD	FREQ 1.0000GHz

23. Check that the measured frequency on the HP 8133A Pulse Generator under test is 1.000 GHz ±0.001 GHz, and record the result on the Test Record.

Internal Clock—High Frequency Perfoirmance

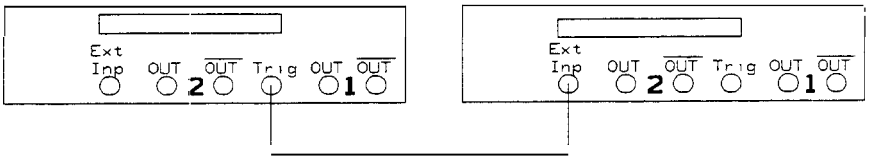


Figure 3-4. Internal Clock High Frequency Test Set-up

TIMEBASE	INT/EXT	INTernal
	FREQ/PERIOD	FREQUENCY 3.0000 GHz

27. Set up the ***second*** HP 8133A Pulse Generator to be used **as** a High Frequency Counter:

TIMEBASE	INT/EXT	EXTernal
	FREQ/PERIOD	FREQ

28. Check that the measured frequency is 3.000 GHz ±0.015 GHz, and record the measured frequency on the Test Record.
29. Disconnect the Trigger Channel Output from the ***second*** HP 8133A Pulse Generator.

TRIGGER

Tests Carry out the following tests in order:

1. Transition Time Performance
2. Dutycycle Verification
3. Level Verification

Set-up

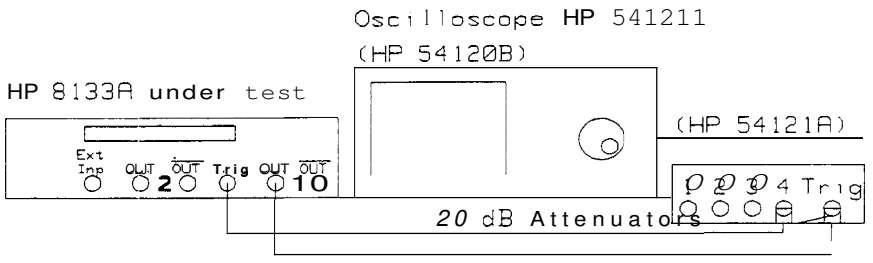


Figure 3-5. TRIGGER Transition Time Test Set-up

Equipment

- Oscilloscope (HP 54121T)
- 2 x Cable (SMA m-m)
- 2 x 20 dB Attenuator (33340C)

Transition Time Performance

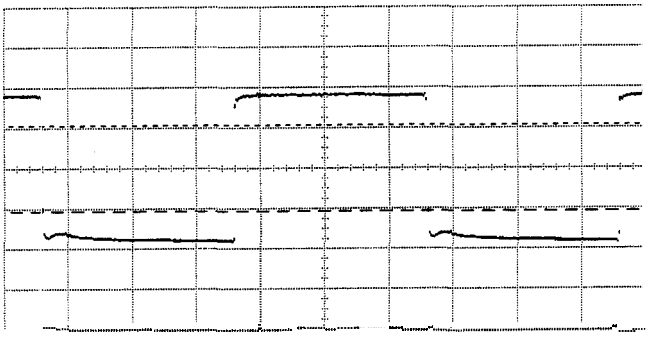
1. Connect the HP 8133A Pulse Generator to the oscilloscope as shown in Figure 3-5.
   a. Connect the TRIGGER Output to the Channel 4 input on the 'scope.
   b. Connect the PULSE Output under test to the Trigger Input on the 'scope.
2. Set up the HP 8133A Pulse Generator as follows:

TIMEBASE	INT/EXT	INTernal
	FREQ/PERIOD	PERIOD 30.000 ns
TRIGGER	AMPL/HIGH	HIGH +1.8 V
	OFFS/LOW	LOW 0.0 V
	DIVIDE/BIT0	DIVIDE ÷1
	DISABLE	Off (Output enabled)
PULSE 1	PULSE/SQUAR	SQUAR
	AMPL/HIGH	HIGH +0.5 V
	OFFS/LOW	LOW -0.5 V
	DISABLE	Off (OUTPUT enabled

Risetime

3. On the oscilloscope:

   a. Press AUTOSCALE.
   b. Select the Timebase menu and adjust the TIME/DIV and DELAY until one pulse is centered on the display.
   c. Select the Display menu and set the Display Mode to Averaged and the NUMBER OF AVERAGES to 64.
   d. Set the Bandwidth to 20 GHz
   e. Select the Channel menu and set the Attenuation Factor for Channel 4 to 10 to account for the 20 dB attenuator.
   f. Select the Delta V menu and turn the V Markers on.
   g. Set the Preset Levels to 20–80% and press Auto Level Set:



   h. Select the Timebase menu and adjust the Time/Div to 100 ps/div.
   i. Adjust the Delay until the positive edge of the pulse is centered.
   j. Select the Delta t menu and turn the T Markers on.
   k. Set the START ON POS EDGE 1 and STOP ON POS EDGE 1 and press the Precise Edge Find key:

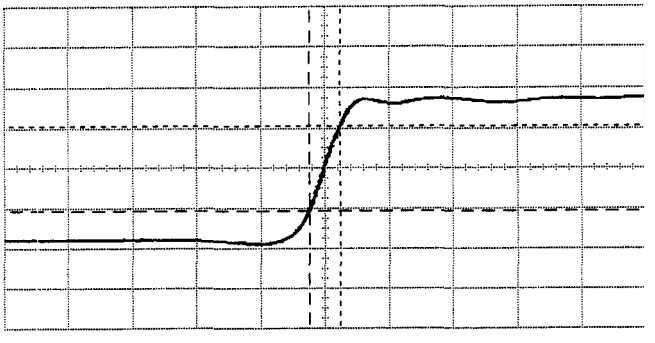


Figure 3-6. TRIGGER Risetime – 100 ps/div

4. Check that the measured risetime (At) <100 ps, and record the measured risetime on the Test Record.

Falltime

5. On the oscilloscope:
   a. Select the Timebase menu and adjust the DELAY until the negative edge of the pulse is centered.
   b. Select the Delta t menu.
   c. Set the START ON NEG EDGE 1 and STOP ON NEG EDGE 1 and press the Precise Edge Find key.
6. Check that the measured falltime (At) <100 ps, and record the measured falltime on the Test Record.

Dutycycle Verification

7. On the oscilloscope:
   a. Select the Timebase menu and adjust the Time/Div to 5 ns/div.
   b. Set the Delay to 16 ns.
   c. Press More on the bottom row of keys, and select the Measure menu.
   d. Press More on the right-hand row of keys and select Duty Cycle to measure the Duty Cycle.
   e. Check that the Dutycycle is 50% nominal.

Level Verification

8. On the oscilloscope:
   a. Press More on the bottom row of keys.
   b. Select the Delta V menu and set the Preset Levels to 0–100%.
   c. Press Auto Level Set.
   d. Check. that the Low Level V(1) is 0 V nominal.
   e. Check that the High Level V(2) is 1.8 V nominal.

Tests

Depending on the options fitted, carry out the indicated tests in order for Channel 1.

If you have a dual channel instrument, then carry out the indicated tests for Channel 2.

Table 3-3. Output Test Summary

	Channel 1			Channel 2	
	Single Channel		Dual Channel		
	Standard	Option 001	Option 002/003	Option 003 PULSE	Option 002 PULSE/DATA
1 Delay Performance	√	J	J	√	x
2 Extended Delay Performance	x	√	√	x	x
3 Inter-Channel Delay Performance	x	x	J	x[1]	x[1]
4 Width Performance	J	√	J	√	x
6 Dutycycle Verification	J	J	J	J	x
6 Level Performance	√	J	J	J	√
7 Level Window Performance	√	J	√	√	√
8 Overshoot & Ringing Performance	√	J	√	√	J
9 Transition Time Performance	√	√	√	√	√
10 Jitter Performance	J	J	J	√	√
11 Data Performance	x	x	x	x	J

1 Test carried out as part of Channel 1 tests

Equipment

- Oscilloscope (HP 54121T)
- 3 x Cable (SMA m-m)
- 3 x 20 dB Attenuator (33340C)
- Adapter (SMA m-m)
- Power Splitter (11667B)

Delay Performance

The Delay F'erformance test applies only to **PULSE** channels.

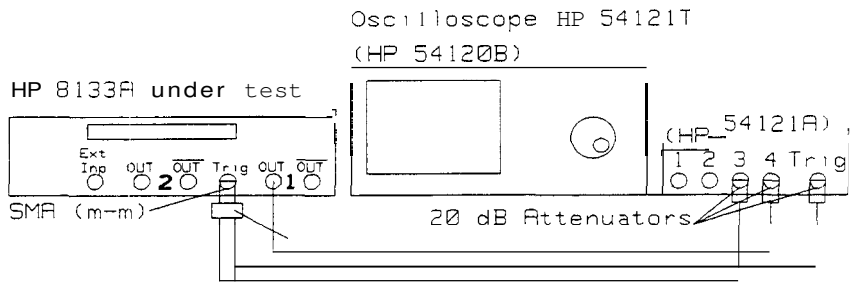
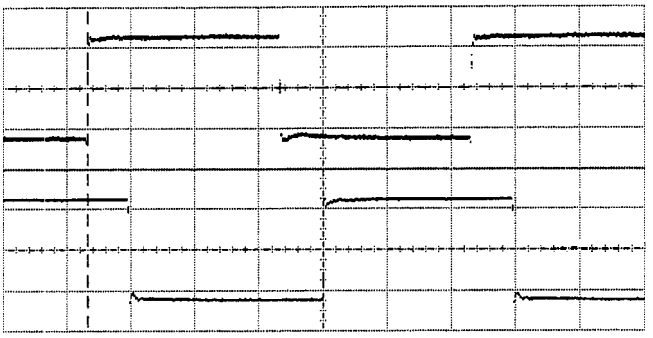


Figure 3-7. PULSE Channel Delay Test Set-up (Channel 1)

1. Connect the HP 8133A Pulse Generator to the oscilloscope as shown in Figure **3-7.**
   a. Connect the Output of the Channel under test to the Channel **4** Input on the 'scope.
   b. Connect the **TRIGGER** Output via the Power Splitter to the Trigger Input and Channel **3** Input on the 'scope.
2. Set up the HP 8133A Pulse Generator as follows:

TIMEBASE	(INT/EXT)	INTernal
	(FREQ/PERIOD)	PERIOD 30.000 ns
TRIGGER	(AMPL/HIGH)	HIGH +0.5 V
	(OFFS/LOW)	LOW -0.5 V
	(DIVIDE/BIT0)	DIVIDE ÷1
	(DISABLE)	Off (Output enabled)
PULSE 1	(PULSE/SQUAR)	SQUAR
	(AMPL/HIGH)	HIGH +0.5 V
	(OFFS/LOW)	LOW -0.5 V
	(DELAY/PHASE)	DELAY 0 ps
	(DELAYPHASE)	SKEW 0 ps
	(DISABLE)	Off (OUTPUT enabled]

3. On the oscilloscope:
   a. Press (AUTOSCALE).
   b. Select the Timebase menu and adjust the Time/Div to 5 ns/div.
   c. Adjust the Delay to **25** ns.
   d. Select the Display menu and set the number of averages to 16.
   e. Select the Delta V menu and switch the Voltage Markers on.
   f. Assign Marker 1 to Channel 3 and Marker 2 to Channel **4.**
   g. Set the Preset Levels to 50-50% and press Auto Level Set.
   h. Select the Delta t menu and switch the T Markers on.
   i. Assign START ON POS EDGE 1 and STOP ON POS EDGE 1.
   j. Press the Precise Edge Find key.



Figuire 3-8. Δt_0 : 5.00 ns/div, DELAY = 25.0000 ns

4. Record the measured At on the Test Record as the Fixed Delay Δt_0 for the Channel under test.
5. Set the HP 8133A Pulse Generator Channel Delay to +5 ns.
6. On the oscilloscope press (Clear Display) and then the Precise Edge Find key.

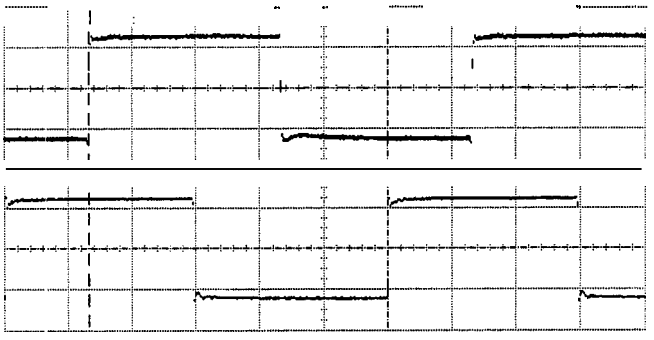


Figure 3-9. Δt_{+5} : 5.00 ns/div, DELAY = 25.0000 ns

7. Subtract the Fixed Delay Δt_0 from the measured At and record the result on the Test Record as Δt_{+5} for the Channel under test. The result should be 5 ns ±0.05 ns.
8. Set the HP 8133A Pulse Generator Channel Delay to +10 ns.
9. On the oscilloscope:
   a. Assign STOP ON POS EDGE 2
   b. Press (Clear Display) and then the Precise Edge Find key.
10. Subtract the Fixed Delay Δt_0 from the measured At and record the result on the Test Record as Δt_{+10} for the Channel under test. The result should be 10 ns f0.05 ns.
11. ***Thefollowing Extended Delay test applies only to Channel 1, with Option 001, 002 or 003 instruments. If you are testing a Standard HP 8133A Pulse Generator without Options, go straight to Figure 7-4.***

12. Set the HP 8133A Pulse Generator Channel 1 Delay to +15 ns.
13. On the oscilloscope press (Clear Display) and then the Precise Edge Find key,
14. Subtract the Fixed Delay Δt_0 from the measured At and record the result on the Test Record as Δt_{+15} for Channel 1. The result should be 15 ns ±0.05 ns.
15. Set the HP 8133A Pulse Generator Channel 1 Delay to -5 ns.
16. On the oscilloscope:
    a. Assign STOP ON POS EDGE 1
    b. Press (Clear Display) and then the Precise Edge Find key:

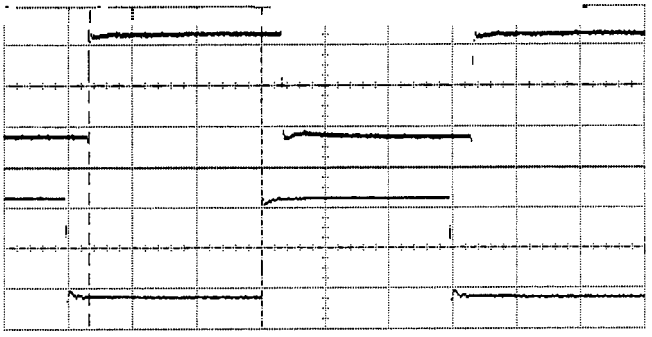


Figure 3-10. At-5 : *5.00* ns/div, DELAY = *25.0000* ns

17. Subtract the Fixed Delay Δt_0 from the measured At and record the result on the Test Record as Δt_{-5} for Channel 1. The result should be -5 ns ±0.05 ns.
18. Set up the HP 8133A Pulse Generator as follows:

PULSE 1	PULSE/SQUAR	PULSE
	WIDTH/DCYC	WIDTH 5 ns
	DELAY/PHASE	DELAY 0 ps

19. On the oscilloscope press (Clear Display) and then the Precise Edge Find key.
20. Record the measured At on the Test Record as the PULSE mode Fixed Delay Δtp_0 for Channel 1.
21. Set the HP 8133A Pulse Generator Channel 1 Delay to -5 ns.
22. On the oscilloscope press (Clear Display) and then the Precise Edge Find key.
23. Subtract the PULSE mode Fixed Delay Δtp_0 from the measured At and record the result on the Test Record as Δtp_{-5} for Channel 1. The result should be -5 ns ±0.05 ns.
24. Set the HP 8133A Pulse Generator Channel 1 Delay to +5 ns.

25. On the oscilloscope press (Clear Display) and then the Precise Edge Find key.
26. Subtract the PULSE mode Fixed Delay Δtp_0 from the measured At and record the result as Δtp_{+5} on the Test Record. The result should be +5 ns ±0.05 ns.
27. *The Inter-Channel Delay test only applies to dual channel instruments. If you are testing a single-channel HP 8133A Puke Generator, or have already carried out the Inter-Channel Delay test while testing Channel 1, go straight to Figure 7-4.*

Inter-Channel Delay Performance (Options 002 & 003 only)

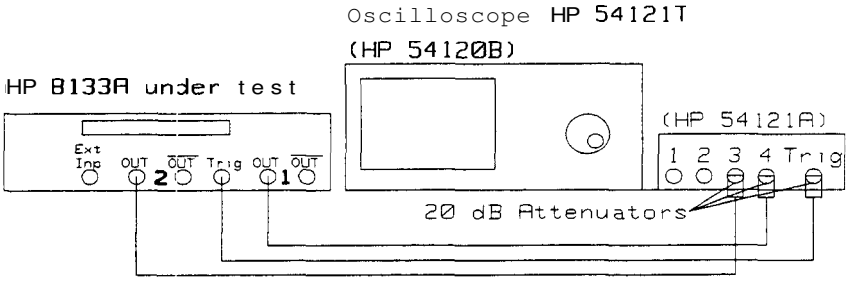


Figure 3-11. Inter-Channel Delay Test Set-up

28. Connect the HP 8133A Pulse Generator to the 'scope as shown in Figure 3-11.
29. Set up the HP 8133A Pulse Generator as follows:

PULSE 1	DELAY/PHASE	DELAY 0 ps
	WIDTH/DCYC	WIDTH 1 ns
PULSE/DATA 2[1]	DATA/SQUAR	SQUAR
PULSE 2[2]	PULSE/SQUAR	SQUAR
	DELAY/PHASE[2]	DELAY 0 ps
	AMPL/HIGH	HIGH +0.5 V
	OFFS/LOW	LOW -0.5V
	DISABLE	Off (OUTPUT enabled:

1 Option 002 only

2 Option 003 only

30. On the oscilloscope:
    a. Select the Channels menu and set the Attenuation Factor for Channel **3** to 10.
    b. Set the VOLTS/DIV for Channel 3 to 400 mV/div.
    c. Select the Timebase menu and adjust the TIME/DIV to 1 ns/div and the DELAY to 16 ns.
    d. Select the Delta t menu and press the Precise Edge Find key.

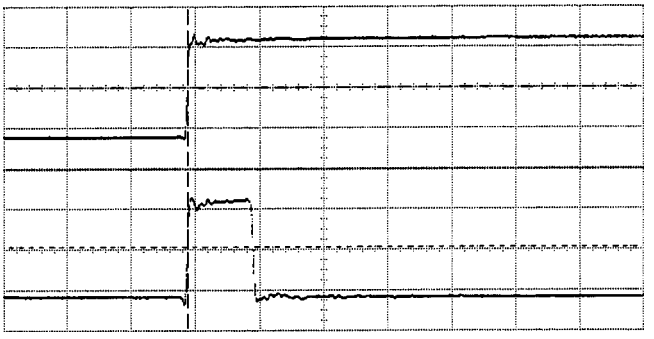


Figure 3-12. Δt_{ic} : 1.00 ns/div DELAY = 16.0000 ns

31. Record the measured At **as** At;,. The result should be 0 ns ±0.15 ns.
32. Set the HP 8133A Pulse Generator Channel 1 Delay to -3 ns.
33. On the oscilloscope press Clear Display
34. If necessary, select the Timebase menu and adjust the DELAY to get both pulses on the display. Then reselect the Delta t menu.

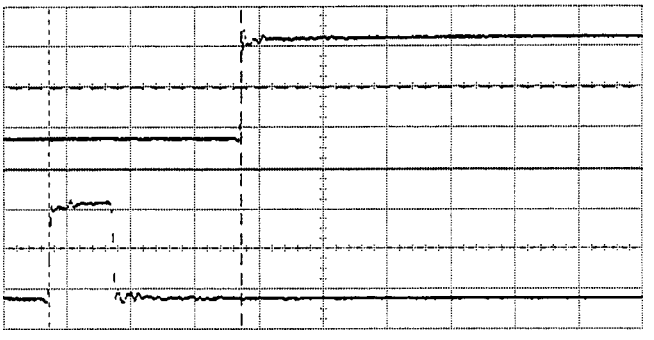


Figure 3-13. $\Delta t_{ic\text{-}3}$: 1.00 ns/div Delay = 16.0000 ns

35. Press the Precise Edge Find key.
36. Subtract the fixed delay Δt_{ic} from the measured At and record the result as $\Delta t_{ic\text{-}3}$. The result should be -3 ns ±0.05 ns.
37. Set the HP 8133A Pulse Generator Channel 1 Delay to +5 ns.
38. On the oscilloscope press Clear Display.

39. If necessary, select the Timebase menu and adjust the DELAY to get both pulses on the display. Then reselect the Delta t menu:

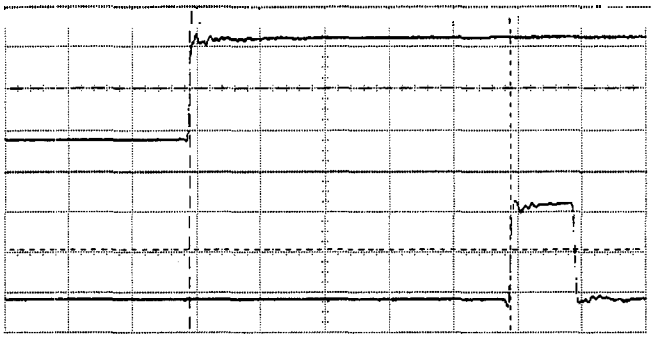


Figure 3-14. Δt_{ic+5} : 1.00 ns/div

40. Press the Precise Edge Find key.
41. Subtract the fixed delay Δt_{ic} from the measured At and record the result as Δt_{ic+5}. The result should be +5 ns ±0.05 ns.

Width Performance

3idx|Testing:PULSE Width|

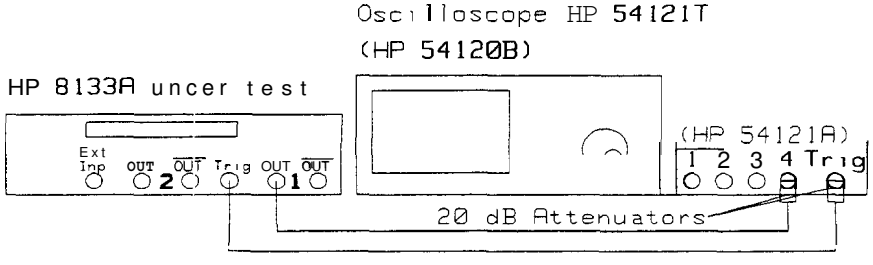


Figure 3-15. PULSE Channel Width Test Set-up

42. Connect the HP 8133A Pulse Generator to the oscilloscope as shown in Figure 3-15.

43. Set up the HP 8133A Pulse Generator as follows:

TIMEBASE	INT/EXT	INTernal
	FREQ/PERIOD	PERIOD 30.000 ns
TRIGGER	AMPL/HIGH	HIGH +0.5 V
	OFFS/LOW	LOW -0.6 V
	DIVIDE/BIT0	DIVIDE ÷1
	DISABLE	Off (Output enabled)
PULSE	PULSE/SQUAR	SQUAR
	AMPL/HIGH	HIGH +0.5 V
	OFFS/LOW	LOW -0.5 V
	DELAY/PHASE	DELAY 0 ps
	DELAY/PHASE	SKEW 0 ps
	DISABLE	Off (OUTPUT enabled)

44. On the oscilloscope:

a. Press AUTOSCALE.
b. Select the Display menu and set the number of averages to 16.
c. Select the Timebase menu and set the Time/Div to 5 ns/div.
d. Select the Delta V menu and switch the V Markers on.
e. Set the Preset Levels to 50-50% and press Auto Level Set.

45. Set up the HP 8133A Pulse Generator as follows:

PULSE	PULSE/SQUAR	PULSE
	WIDTH/DCYCLE	WIDTH 10 ns

46. On the oscilloscope:

a. Press Clear Display.
b. Select the Timebase menu and set the Time/Div to 2 ns/div.
c. Adjust the Delay until one pulse is centered in the display
d. Select the Delta t menu and switch the T Markers on.
e. Assign START ON POS EDGE 1 and STOP ON NEG EDGE 1.
f. Press the Precise Edge Find key.

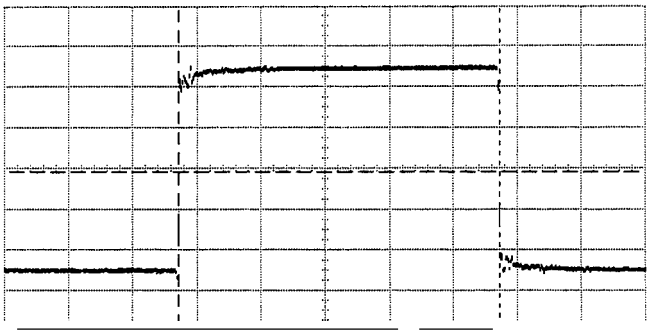


Figure 3-16. Width,, : 2.00 ns/div

47. Record the measured pulse-width (At) for the Channel under test on the Test Record as $Width_{min}$, it should be 10 ns ±0.1 ns.

48. Set up the HP 8133A Pulse Generator as follows:

PULSE	(WIDTH/DCYCLE)	WIDTH 160 ps

49. On the oscilloscope:
    a. Select the Timebase menu and set the Time/Div to 100 ps/div.
    b. Adjust the Delay until one pulse is centered in the display
    c. Select the Delta t menu and press Precise Edge Find.

50. Record the measured pulse-width (At) for the Channel under test on the Test Record as $Width_{min}$, it should be 150 ps ±100 ps.

Dutycycle Verification

51. Set up the HP 8133A Pulse Generator as follows:

TIMEBASE	(FREQ/PERIOD)	PERIOD 20.000 ns
PULSE	(WIDTH/DCYCLE)	DCYCLE 50.0%

52. On the oscilloscope:
    a. Press (AUTOSCALE)
    b. Select the Display menu and set the number of averages to 16.
    c. Select More on the bottom row of keys and select the Measure menu.
    d. Select More on the right-hand row of keys and measure the Duty Cycle.

53. Check that the measured Duty Cycle is 50% nominal.

54. Set the Duty Cycle to 10%.

Level Performance

55. Disable the HP 8133A Pulse Generator outputs.
56. Keep the equipment as shown in Figure 3-15, but remove the 20 dB attenuator on Channel 4 of the oscilloscope.

Minimum Amplitude

57. Set up the HP 8133A Pulse Generator as follows:

TIMEBASE	INT/EXT	INTernal
	FREQ/PERIOD	PERIOD 30.000 ns
TRIGGER	AMPL/HIGH	HIGH +0.5 V
	OFFS/LOW	LOW -0.5 V
	DIVIDE/BIT0	DIVIDE ÷1
	(DISABLE)	Off (Output enabled)
PULSE	PULSE/SQUAR	SQUAR
	AMPL/HIGH	HIGH +0.15 V
	OFFS/LOW	LOW -0.15 V
	DELAY/PHASE	DELAY 0 ps
	DELAY/PHASE	SKEW 0 ps
	DISABLE	Off (OUTPUT enabled

58. On the oscilloscope:
    a. Press AUTOSCALE
    b. Select the Display menu and set the number of averages to 64.
    c. Select Channels and set the attenuation factor for Channel 4 to 1.
    d. Select the Delta V menu and switch on the V Markers.
    e. Set the Preset Levels to 0–100% and press Auto Level Set.
59. Check the Low-level voltage V(1) is −150 mV ±29 mV and record the measured value on the Test Record for the Channel under test.
60. Check the High-level voltage V(2) is 150 mV ±29 mV and record the measured value on the Test Record for the Channel under test.

Maximum Amplitude

61. Disable the HP 8133A Pulse Generator outputs.
62. Add a 20 dB Attenuator to the Channel 4 input of the oscilloscope.
63. Re-enable the HP 8133A Pulse Generator outputs.
64. Set up the HP 8133A Pulse Generator as follows:

PULSE	AMPL/HIGH	AMPL 3.0 V
	OFFS/LOW	OFFS 0.0 V

65. On the oscilloscope:
    a. Press (AUTOSCALE)
    b. Select Channels and set the attenuation factor for Channel 4 to 10.
    c. Select the Delta V menu and switch on the V Markers.
    d. Set Preset Levels to 0–100% and press Auto Level Set.

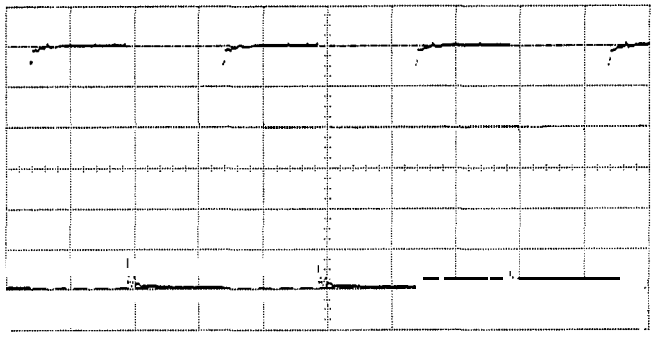


Figure 3-17. Maximum Amplitude : 500 mV/div

66. Check the Low-level voltage V(1)is −1.5 V ±0. 11 V and record the measured value on the Test Record for the Channel under test.
67. Check the High-level voltage **V(2)** is 1.5 V ±0.11 V and record the measured value on the Test Record **for** the Channel under test.

Level Window Performance

Maximum High-level

68. Set up the HP 8133A Pulse Generator as follows:

PULSE	AMPL/HIGH	HIGH 4.00 V
	OFFS/LOW	LOW 3.70 V

69. On the oscilloscope:
    a. Select the Channels menu and set the OFFSET for Channel **4** to +3.8 V and the VOLTS/DIV to 100 mV/div.
    b. Select the Delta V menu and press Auto Level Set.
70. Check the High-level voltage V(2) **is 4** V rt0.106 V and record the measured value on the Test Record for the Channel under test.

Minimum Low-level

71. Set up the HP 8133A Pulse Generator as follows:

PULSE	AMPL/HIGH	HIGH -1.70 V
	OFFS/LOW	LOW -2.00 V

72. On the oscilloscope:
    a. Select the Channels menu and set the OFFSET for Channel **4** to -1.85 V.
    b. Select the Delta V menu and press Auto Level Set.
73. Check the Low-level voltage V(1)is -2.00 V ±0.066 V and record the measured value on the Test Record for the Channel under test.

Overshoot and Ringing Performance

74. Set up the HP 8133A Pulse Generator **as** follows:

PULSE	PULSE/SQUAR	SQUAR
	AMPL/HIGH	HIGH +1.5 V
	OFFS/LOW	LOW -1.5 V
	DELAY/PHASE	DELAY 0 ps
	DELAY/PHASE	SKEW 0 ps
	DISABLE	Off (OUTPUT enabled)

75. On the oscilloscope:
    a. Press AUTOSCALE
    b. Select the Display menu and set the Number of Averages to 64.
    c. Select the Timebase menu and set the Sweep Time to 5 ns/div.
    d. Select the Delta V menu and switch on the V Markers.
    e. Set the Preset Levels to Variable Levels and set the Variable Levels to 85%and 115%.
    f. Press Auto Level Set.
    g. Select the Timebase menu and set the Sweep Time to 500 ps/div.
    h. Adjust the Delay to center the positive edge.
    i. Select the Channels menu and set the Channel 4 Offset to 1.45 V.
    j. Set the VOLTS/DIV to 200 mV/div.
76. Check that the Overshoot of the Positive edge is within the 115% of amplitude limits, **and** record the result on the Test Record for the Channel under test.

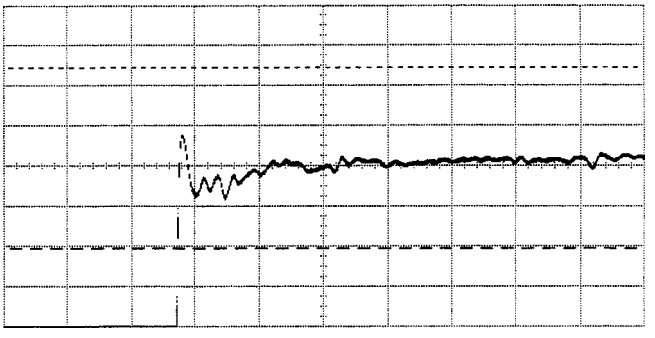


Figure 3-18. Positive Edge Overshoot and Ringing

77. On the oscilloscope:
    a. Select the Channels menu and set the Channel 4 Offset to 0 V and Sensitivity to 500 mv/div.
    b. Select the Timebase menu and set the Sweep Time to 5 ns/div.
    c. Select the Delta V menu and set the Variable Levels to -15% and +15%.
    d. Press Auto Level Set.
    e. Select the Timebase menu and set the Sweep Time to 500 ps/div.
    f. Adjust the Delay to center the negative edge.
    g. Select the Channels menu and set the Channel 4 Offset to -1.45 V.
    h. Set the VOLTS/DIV to 200 mV/div.
78. Check that the Overshoot of the Negative edge is within the ±15% of amplitude limits, and record the result on the Test Record for the Channel under test.

Note

The maximum specified Overshoot is actually ±15% ± 20 mV which is ±470 mV for an amplitude of **3** V.

If the Overshoot is not within the ±15% of amplitude limits, make a precise measurement against the specification of ±470 mV.

Transition Time Performance

Risetime 10–90%

79. On the oscilloscope:
    a. Press AUTOSCALE
    b. Select the Display menu and set the Bandwidth to 20 GHz.
    c. Select the Delta V menu and switch on the V Markers.
    d. Set the Preset Levels to 10–90%and press Auto Level Set.
    e. Select the Timebase menu and set the TIME/DIV to 20 ps/div.
    f. Adjust the Delay until a positive edge is centered.
    g. Select the Delta t menu and switch on the T Markers.
    h. Select START ON POS EDGE 1 and STOP ON POS EDGE 1.

i. Press Precise Edge Find.

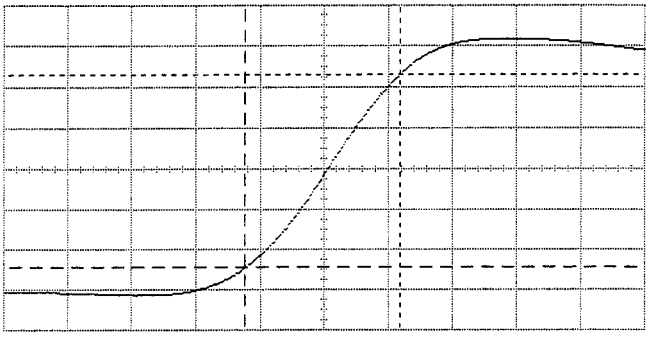


Figure 3-19. Risetime 10–90%

80. Check that the measured rise-time (At) is < 100 ps, and record the measured value on the Test Record for the Channel under test.

Risetime 20–80%

81. On the oscilloscope:
    a. Select the Timebase menu and set TIME/DIV to 5 ns/div.
    b. Select the Delta V menu and set the Preset Levels to 20–80%.
    c. Press Auto Level Set.
    d. Select the Timebase menu and set TIME/DIV to 20 ps/div.
    e. Select the Delta t menu and press Precise Edge Find.
82. Check that the measured rise-time (At) is < 60 ps, and record the measured value on the Test Record for the Channel under test.

Falltime 20–80%

83. On the (oscilloscope:
    a. Select the Timebase menu and adjust the Delay until a negative edge is centered on the display.
    b. Select the Delta t menu and set START ON NEG EDGE 1 and STOP ON NEG EDGE 1.
    c. Press Precise Edge Find.
84. Check that the measured fall-time (At) is < 60 ps, and record the measured value on the Test Record for the Channel under test.

Falltime 10–90%

85. On the oscilloscope:
    a. Select the Timebase menu and set the TIME/DIV to 5 ns/div.
    b. Select the Delta V menu and change the Preset Levels to 10–90%.
    c. Press Auto Level Set.
    d. Select the Timebase and set the Sweep Time to 20 ps/div.
    e. Select the Delta t menu and press Precise Edge Find.
86. Check that the measured fall-time (At) is < 100 ps, and record the measured value on the Test Record for the Channel under test.

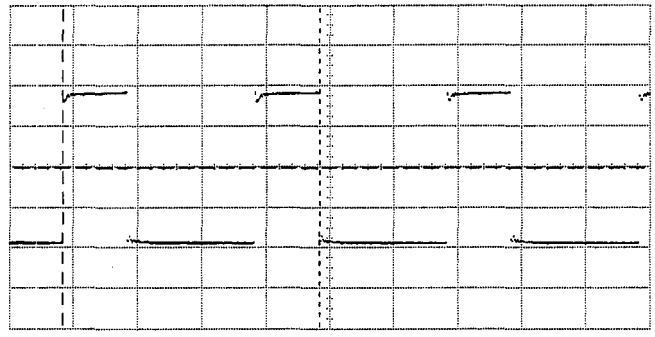
Jitter Performance

87. Set up the HP 8133A Pulse Generator as follows:

	STD			
PULSE/SQUAR	PULSE	PULSE	SQUARE	PULSE
AMPL/HIGH	HIGH +1.5V	HIGH +1.5V	HIGH +1.5V	HIGH +1.5V
OFFS/LOW	LOW -1.5V	LOW -1.5V	LOW -1.5V	LOW -1.5V
WIDTH/DCYCLE	WIDTH 10ns	WIDTH 10ns		WIDTH 10ns
DELAY/PHASE		DELAY +5ns	DELAY +5ns	
DELAY/PHASE		SKEW 0 ps	SKEW 0ps	
DISABLE	OFF	OFF	OFF	OFF
STD	Ch.1			
#001		Ch.1		
#002		Ch.1	Ch.2	
#003		Ch.1		Ch.2

88. On the oscilloscope:

a. Press (AUTOSCALE).
b. Select the display menu and set Average mode with Number of Averages **64.**
c. Set the Bandwidth to 20 GHz.
d. Select the Trigger menu and switch HF Sens on.
e. Select the Delta V menu and switch on the V Markers.
f. Set the Preset Levels to 50–50%and press Auto Level Set.
g. Select the Delta t menu and switch on the T Markers.
h. Set STAFCT ON POS EDGE 1 and STOP ON NEG EDGE 2.
i. Press Precise Edge Find:



j. Select the Timebase menu and set the TIME/DIV to 20 ps/div.
k. Adjust the Delay until the 2nd negative edge is centered (approximately 60 ns).
l. Select the Channels menu and set the Channel **4** VOLTS/DIV to 20 mV/div.
m. Set the OFFSET to 0 V.
n. Select More and then the Histogram menu.
o. Select Time Histogram.
p. Select Source is Chan **4.**
q. Set the Window Marker **1** to + 15 mV.

r. Set the Window Marker 2 to -15 mV. The window is now 1 % of the signal amplitude around 0 V.
s. Select Acquire and set the Number of Samples to 1000
t. Press Start Acquiring.
u. After 1000 samples are completed, select Results and press Sigma:

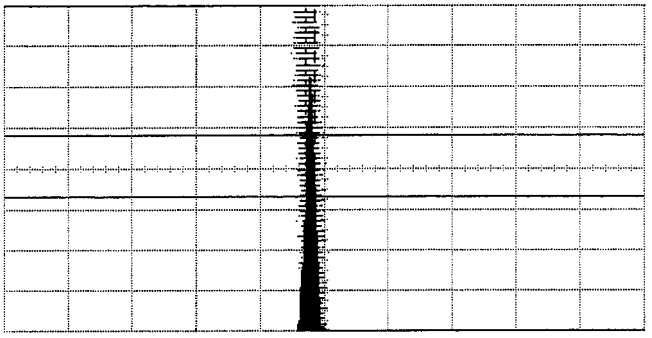


Figure 3-20. Jitter Histogram

89. Record the Sigma value on Test Record as the RMS Jitter for the Channel under test, which should be < 5 ps.

Note

Sigma is not. actually the true RMS Jitter value.

The Sigma value includes the effect of the falltime of the f1 5 mV window, and the oscilloscope's trigger/timebase jitter.

If the Sigma, value is not within specification, make a precise calculation of the true RMS Jitter:

a. Measure and eliminate the falltime error:

$$X = \frac{(6 \times Sigma) - (WindowFalltime)}{6}$$

b. Eliminate the oscilloscope's Jitter:

$$RMSJitter = \sqrt{X^2 - TimebaseJitter^2 - TriggerJitter^2}$$

Refer to Product Note 54120-2 for information on how to measure the Timebase **and** Trigger Jitter of the oscilloscope.

c. Indicate on the Test Record that you have corrected the measured Sigma to the true RMS Jitter value.

Data Performance

The Data Performance test applies only to PULSE/DATA Channel 2 (Option 002).

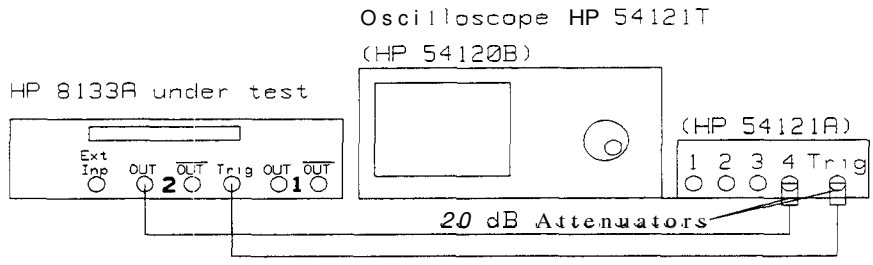


Figure 3-21. PULSE/DATA Channel Data Test Set-up

32 BIT RZ

1. Set up the HP 8133A Pulse Generator as follows:

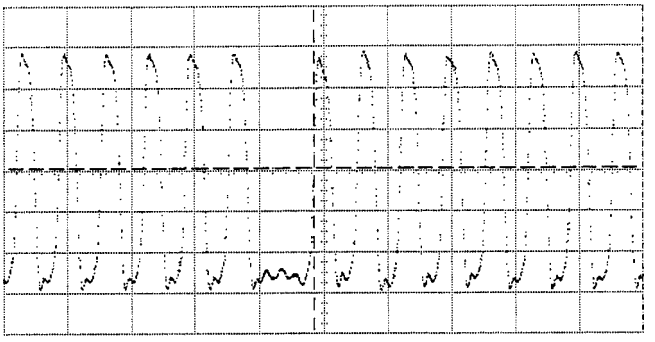
PULSE	PULSE/SQUAR	SQUAR
TIMEBASE	INT/EXT	INTernal
	FREQ/PERIOD	FREQ 3.000 GHz
TRIGGER	AMPL/HIGH	HIGH +0.5 V
	OFFS/LOW	LOW -0.5 V
	DIVIDE/BIT0	BIT 0
	DISABLE	Off (Output enabled)
PULSE/DATA	DATA/SQUAR	DATA
	AMPL/HIGH	HIGH +0.5 V
	OFFS/LOW	LOW -0.5V
	RZ/NRZ	RZ
	32 BIT/PRBS	32 BIT
	DISABLE	Off (OUTPUT enabled:

2. Set Bits 0 to **30** of the **32** Bit data to '1' and Bit **31** to 0:

3. On the oscilloscope:

   a. Press AUTOSCALE.
   b. Select the Timebase menu and set the TIME/DIV to 500 ps/div and the DELAY to **16** ns.
   c. Select the Delta V menu and switch on the V Markers.
   d. Set the Preset Levels to **50-50%** and press Auto Level Set.
   e. Select the Delta t menu and switch on the T Markers.

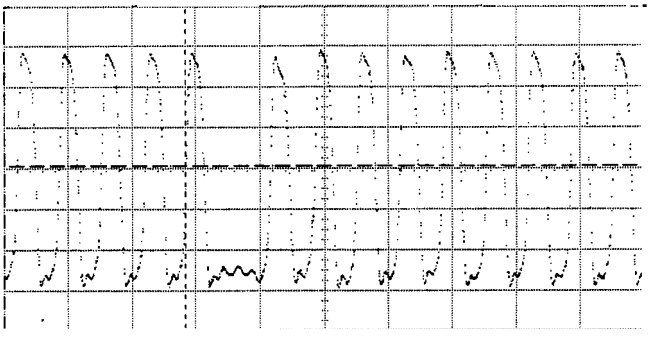
f. Adjust the START ON POS EDGE number until the start marker is on the first positive edge after the 0 in the bitstream (Bit 0):



Bit *0*

g. Select the Timebase menu and set the TIME/DIV to 2 ns.
h. Select the Delta t menu ans set the STOP ON POS EDGE number to (START number + 30).
i. Select the Timebase menu and set the TIME/DIV to 500 ps/div and the DELAY to **27** ns.
j. Select the Delta t menu

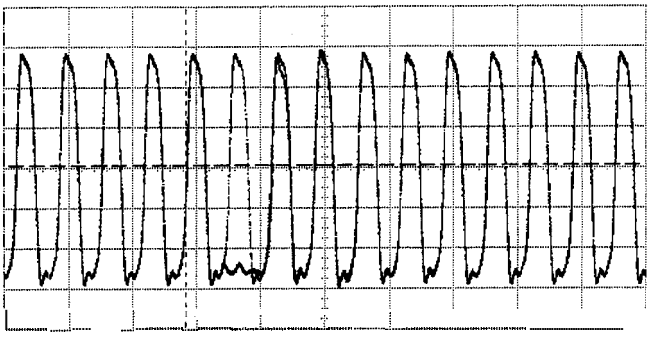
4. Check that the STOP marker is on the rising edge of the last pulse before the 0 in the bitstream (Bit 30), and record the result on the Test Record:



Bit 30

5. Change Bit **31** of the data to **'1'.**

6. Press Clear Display on the 'scope and check that the '1' pulse appears in the bitstream on the 'scope, and record the result on the Test Record:



Bit 31

32 BIT NRZ

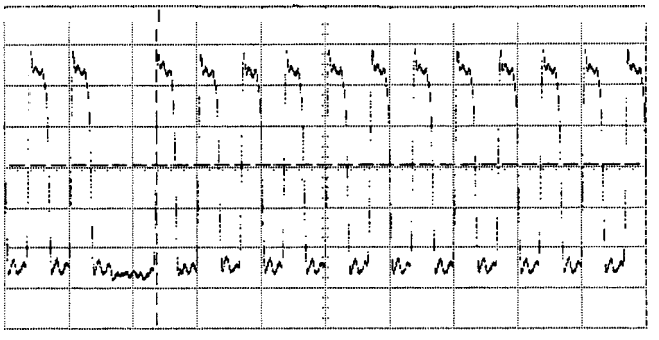
7. Switch the Data format to NRZ, and set the data to '10101010101010101010101010101000':

   ⊓_⊓_⊓_⊓_⊓_⊓_⊓_⊓_⊓_⊓_⊓_⊓_⊓_⊓_⊓_⊓___

8. On the oscilloscope:

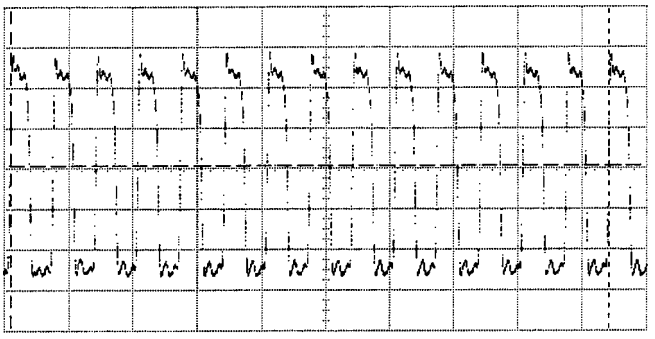
   a. Select the Timebase menu and set the TIME/DIV to 1 ns/div and the DELAY to 17.2 ns.

   b. Select the Delta t menu and adjust the START ON POS EDGE number until the start marker is on the first positive edge after the gap in the bitstream (Bit 0):



Bit 0

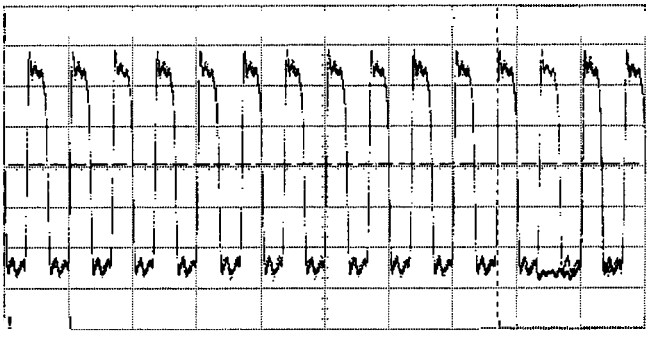
c. Select the Timebase menu and adjust the DELAY until this edge is the *first* edge on the screen:



Bit 0 to Bit 28

d. Select the Delta t menu and select START ON POS EDGE 1 and STOP ON POS EDGE **15** (Bit 28).
e. Select the Timebase menu and adjust the DELAY until the gap following the stop marker is shown (Bits 29,30,31).

9. On the HP 8133A Pulse Generator under test move the DATA EDIT cursor to Bit 30 and toggle Bit **30** from '0' to '1':



Bit 30

10. Check on the 'scope that a **'1'** pulse appears in the gap between the Bit 28 '1' and the Bit 0 '1'. Record the result on the Test Record.

HP 8133A Performance Test Record

Test Facility:

_____	Report No. _____
_____	Date _____
_____	Customer _____
_____	Tested By _____

Model HP 8133A 3 GHz Pulse Generator

Serial No.	_____	Ambient temperature	_____ °C
Options	_____	Relative humidity	_____ %
Firmware Rev.	_____	Line frequency	_____ **Hz**

Special Notes:

_____

_____

_____

_____

_____

_____

_____

Test Equipment **Used:**

	Description	Model No.	Trace No.	Cal. Due Date
1.	Oscilloscope	HP 54121T		
2.	Counter	HP 5334B		
3.	Pulse Generator	HP 8133A		
4.				
5.				
6.				
7.				
8.				
9.				
10.				
11.				
12.				
13.				
14.				
15.				
16.				
17.				
18.				

HP 8133.A Performance Test Record

IP 8133A 3 GHz Pulse Generator No. _____ Date _____

Tesi Sectior	rest Description	Minimum Spec.	Result	Maximum Spec.	Measurement Uncertainty
TIMEBASE	Internal Clock—Low Frequency		ns		
	neasured at PERIOD 30 ns				
	Output Period	29.85 ns		30.15 ns	
	neasured at PERIOD 10 ns				
	Output Period	9.95 ns		10.05 ns	
	External Frequency Counter		GHz		
	neasured at External PERIOD 10.00 ns				
	Displayed Period	9.99 ns		10.01 ns	
	measured at External FREQUENCY 1.000 GHz				
	Displayed Frequency	0.999 GHz		1.001 GHz	
	Internal Clock—High Frequency		GHz		
	measured at FREQUENCY 3.0000 GHz				
	Output Frequency	2.985 GHz		3.015 GHz	
TRIGGER	Transition Time		ps		
	Risetime	-		100 ps	
	Falltime	-		100 ps	

HP 8133A Performance Test Record

HP 8133A 3 GHz Pulse Generator No. _____ Date _____

Tes Sectio	Test Description	Minimum Spec.	Result Channel 1	Result Channel 2	Maximum Spec.	Measurement Uncertainty
output	**Delay**		ns	ns		
	Δt_0		_____	_____ [1]		_____
	Δt_{+5}	1.95 ns	_____	_____ [1]	5.05 ns	_____
	Δt_{+10}	9.95 ns	_____	_____ [1]	10.05 ns	_____
	Extended Delay (Option 001)		ns	ns		
	Δt_{+15}	14.95 ns	_____	-	15.05 ns	_____
	Δt_{-5}	5.05 ns	_____	-	4.95 ns	_____
	Δtp_0		_____	_____ [1]		_____
	Δtp_{+5}	1.95 ns	_____	_____ [1]	5.05 ns	_____
	Δtp_{+10}	9.95 ns	_____	_____ [1]	10.05 ns	_____
	nter-channel Delay (Option 002/003)		ns			
	Δt_{ic}	0.15 ns	_____		± 0.15 ns	_____
	Δt_{ic-3}	3.05 ns	_____		2.95 ns	_____
	Δt_{ic+5}	1.95 ns	_____		5.05 ns	_____
	Width		ns	ns		
	$Width_{max}$	9.9 ns	_____	_____ [1]	10.1 ns	_____
			ps	ps		
	$Width_{min}$	50 ps	_____	_____ [1]	150 ps	_____
	Level					
	measured at Minimum Amplitude:		mV	mV		
	Low-level V(1)	179 mV	_____	_____	121 mV	_____
	High-level V(2	121 mV	_____	_____	179 mV	_____
	measured at Maximum Amplitude:		V	V		
	Low-level V(1	-1.61 V	_____	_____	-1.39 V	_____
	High-level V(2	1.39 V	_____	_____	1.61 V	_____

1 Option 003 PULSE only

HP 8133.A Performance Test Record

HP 8133A 3 GHz Pulse Generat · No. _____ Date _____

Tes Sectio	Test Description	Minimum Spec.	Result Channel 1	Result Channel 2	Maximum Spec.	Measurement Uncertainty
Output:	**Level** Window					
	Measured at Maximum High-level:		V	V		
	High-level V(2)	3.894 V			4.106 V	
	Measured at **Minimum** Low-level:		V	V		
	Low-level V(1)	-2.066 V			-1.944 V	
	Overshoot and Ringing					
	Positive Edge	–	PASSIFAIL	PASSIFAIL	–	–
	Measured Overshoot[1]	-470 mV			470 mV	
	Negative Edge	–	PASSIFAIL	PASSIFAIL	–	–
	Measured Overshoot[1]	-470 mV			470 mV	
	Transition Time[2]		ps	ps		
	Risetime 10–90%	–			100 ps	
	Risetime 20–80%	–			60 ps	
	Falltime 20–80%	–			60 ps	
	Falltime 10–90%	–			100 ps	
	Jitter[2]		ps	ps		
	RMS Jitter (Sigma)	–			5 ps	
	Corrected true RMS Jitter:	–	YESINO	YESINO	–	–
	Data[2]					
	2 BIT RZ					
	Bit 30	–	–	PASSIFAIL	–	–
	Bit 31 '1'	–	–	PASSIFAIL	–	–
	2 BIT NRZ					
	Bit 30 '1'	–	–	PASSIFAIL	–	–

1 An overshoot measurement is **only** necessary if the PASSIFAIL test fails.

2 Measured **using** HP 54120 Series oscilloscope.

4

Troubleshooting

This chapter contains the following information:

- How to use the flow-charts to locate a fault in the HP 8133A Power Supplies
- The Power Supply flow-charts
- How to use the Self-Test facility
- Troubleshooting faulty assemblies

Troubleshooting the Power Supplies

This section contains flowcharts enabling you to locate faults in the Power Supplies down to individual component level.

Using the Flowcharts

Enter each flow-chart at its highest point and perform the recommended tests until the fault is found and corrected.

The first chart assumes that the HP 8133A is showing no signs of life at all, and the other charts progress from there, covering the various possible causes of failure.

The following two **block** diagrams show the relationships between the various parts of the Power Supply, and the voltages available:

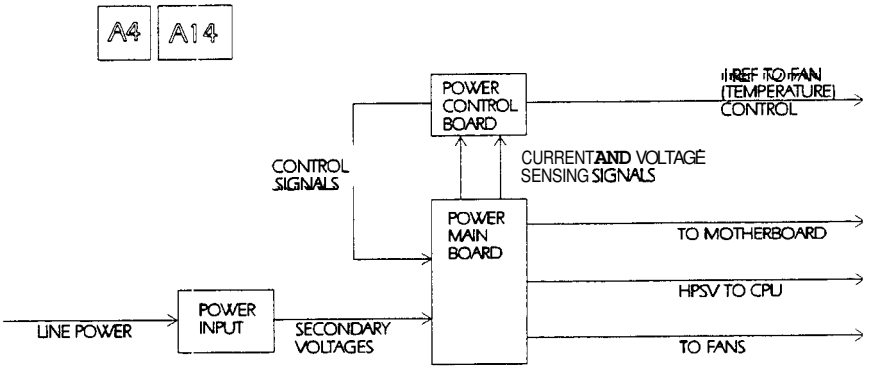


Figure 4-1.
Functional Block Diagram of the HP 8133A Pulse Generator Power Supplies

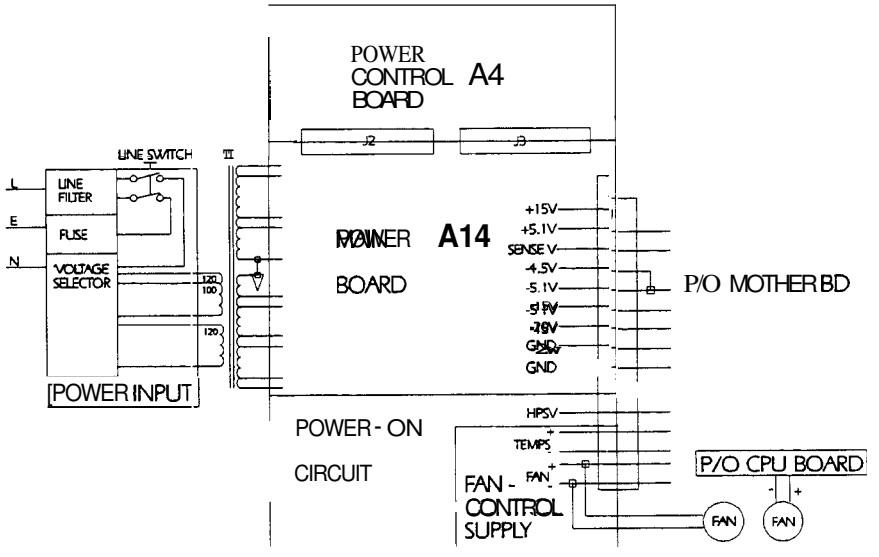


Figure 4-2.
Block Diagram of the Power Supplies Showing Power Connections

Unit not Operating

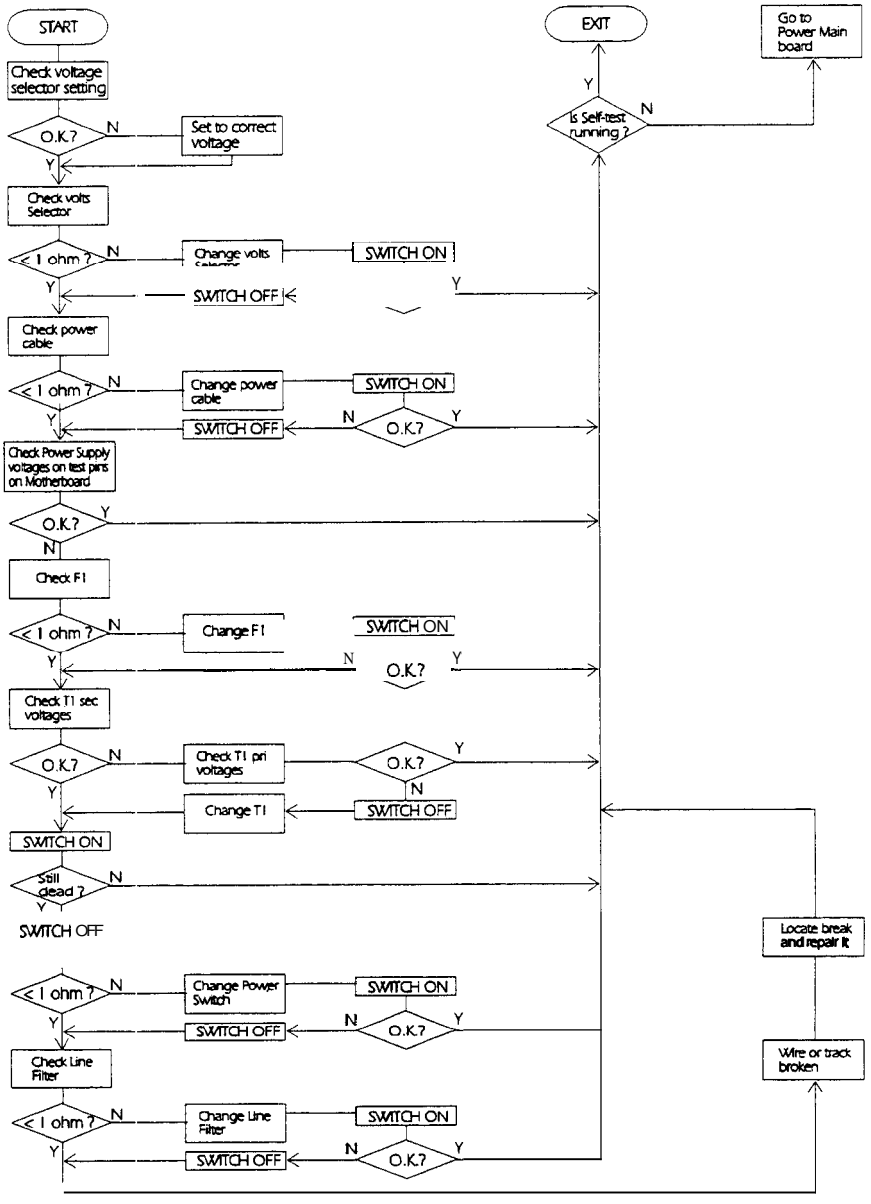


Figure 4-3. Unit Shows No Signs of Operating

Power Main board

This board contains the following Circuits:

- Power-on Reset
- Fan Control

And the following regulator drivers:

- -20V 1.0A
- +15V 1.8A
- -15V 1.1A
- +5.1V 2.7A
- -5.1V 2.5A
- -4.5V 3.5A

The flow-charts on the following pages enable faultfinding down to individual component level.

Power-on Reset Circuit Faulty

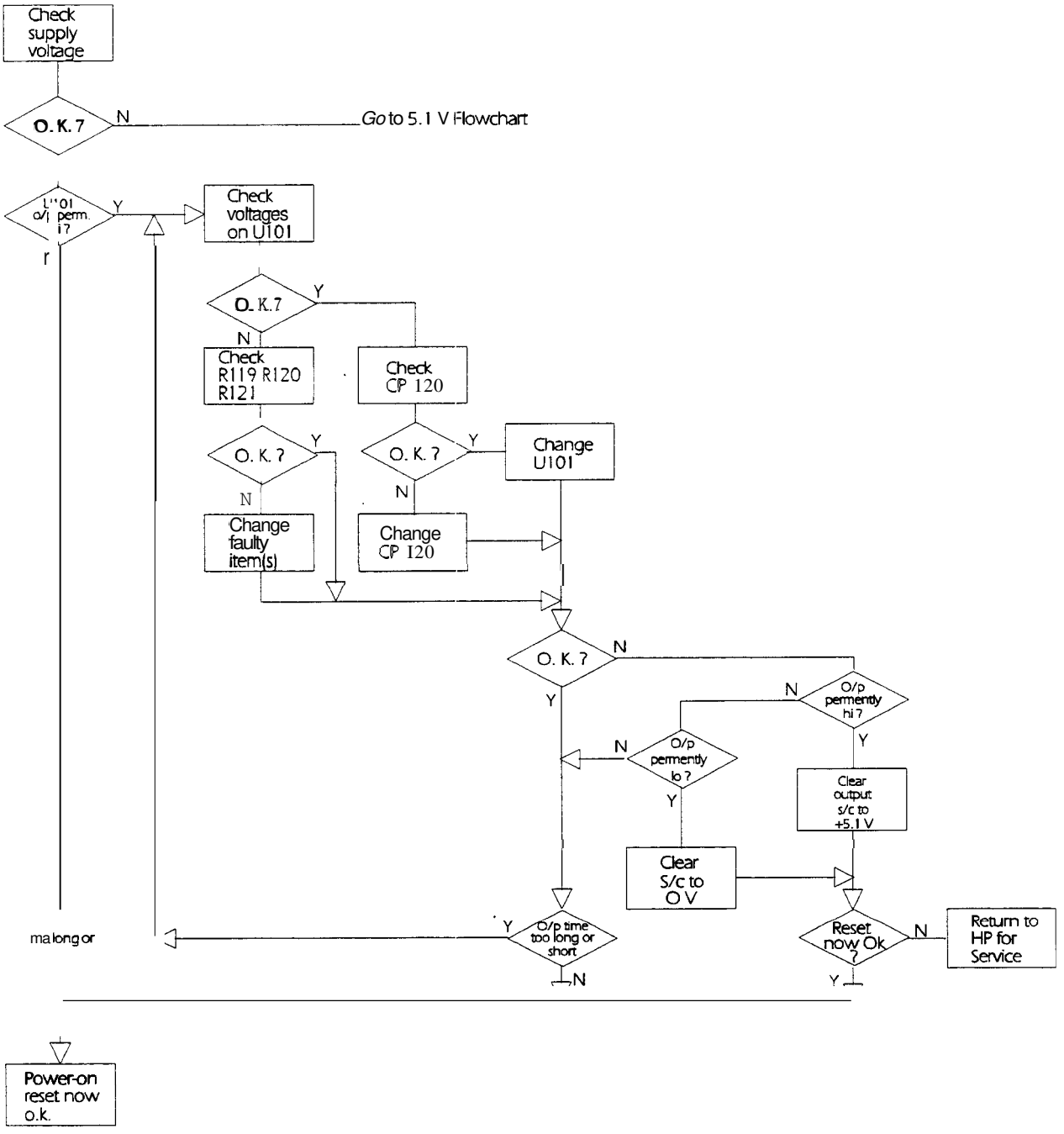


Figure 4-4. Power-on Reset Not Working, or Period Too Long or Too Short

Fan Control Circuit Faulty

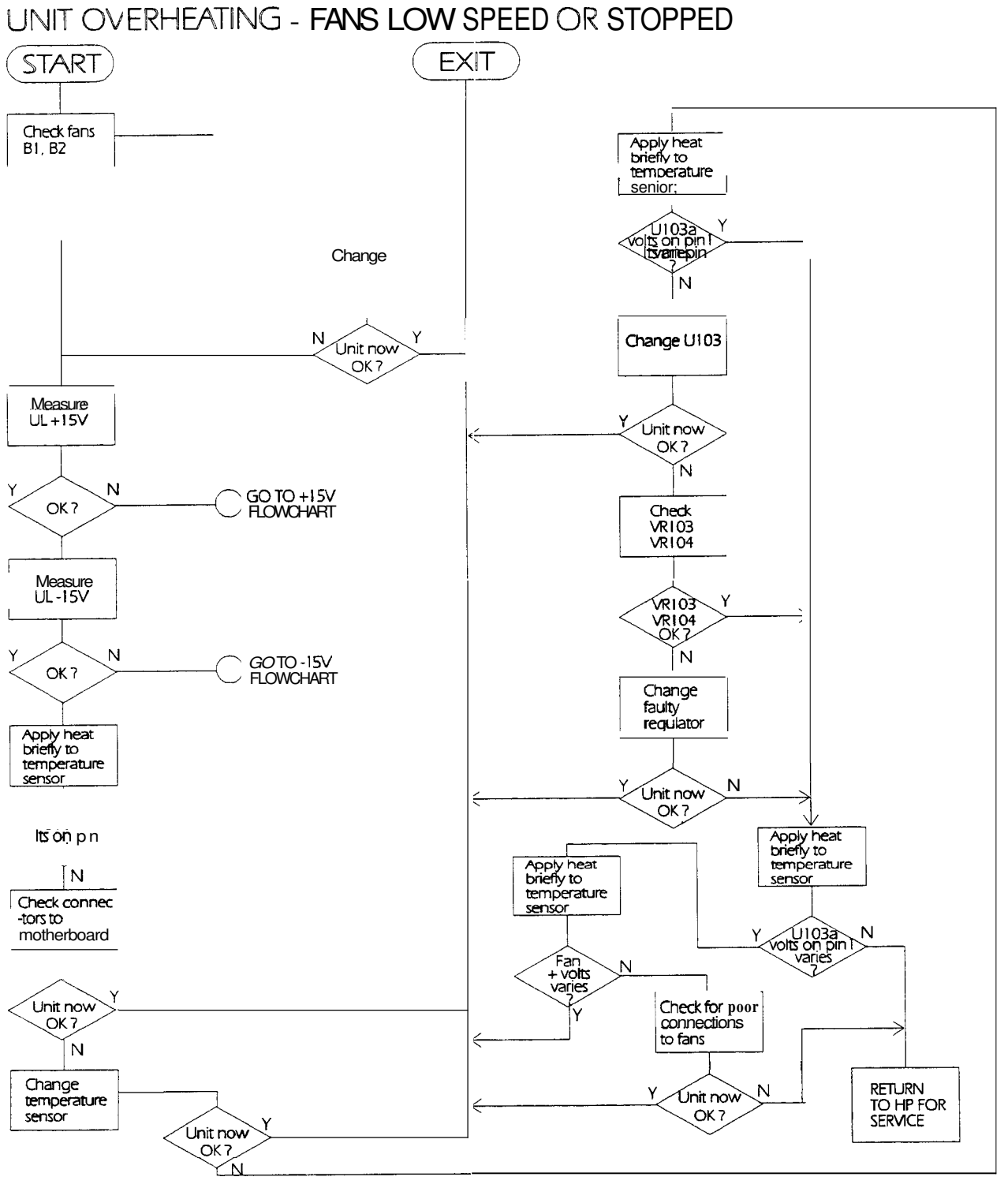


Figure 4-5. Flowchart for Tracing Common Faults in Fan Control Circuit

-20V / 1.0A No Output or Wrong Voltage

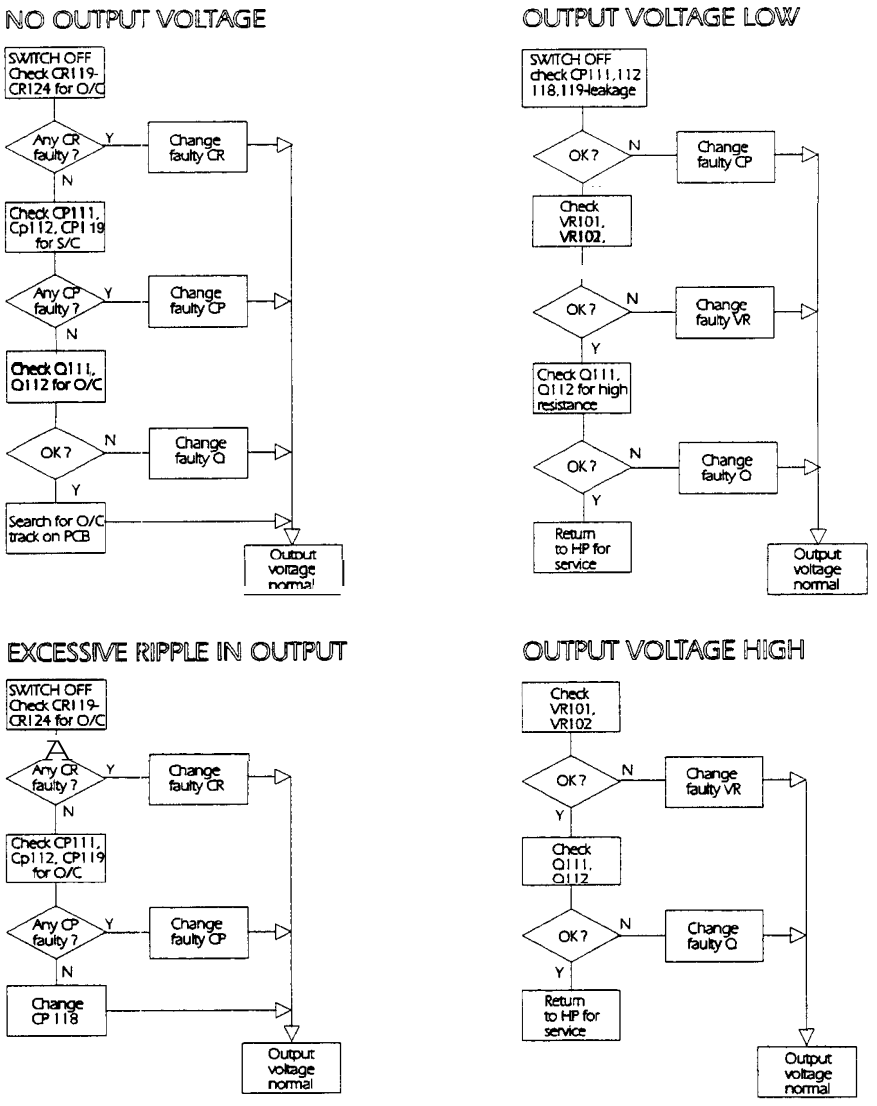


Figure 4-6. Flowcharts for Tracing Common Faults in -2OV Regulator

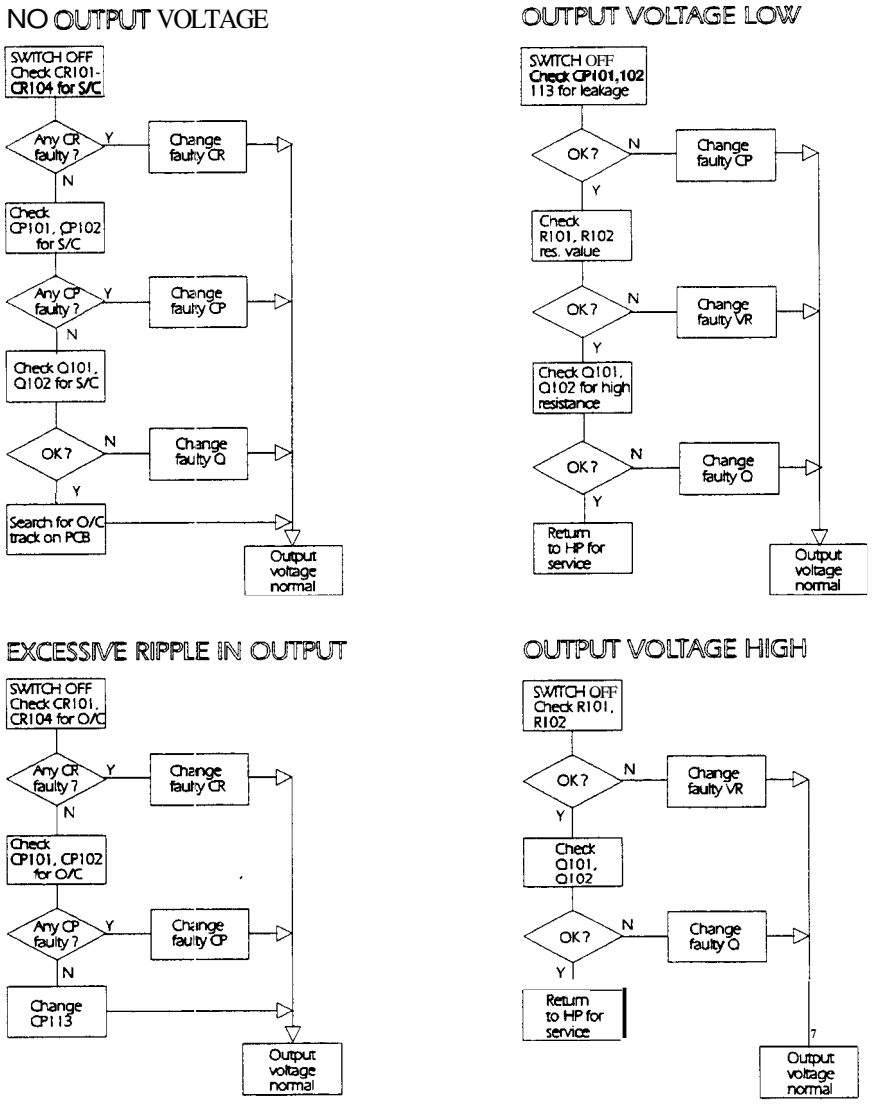


Figure 4-7.
Flowcharts for Tracing Common Faults in +15V Regulator

-15V / 1.1A No Output or Wrong Voltage

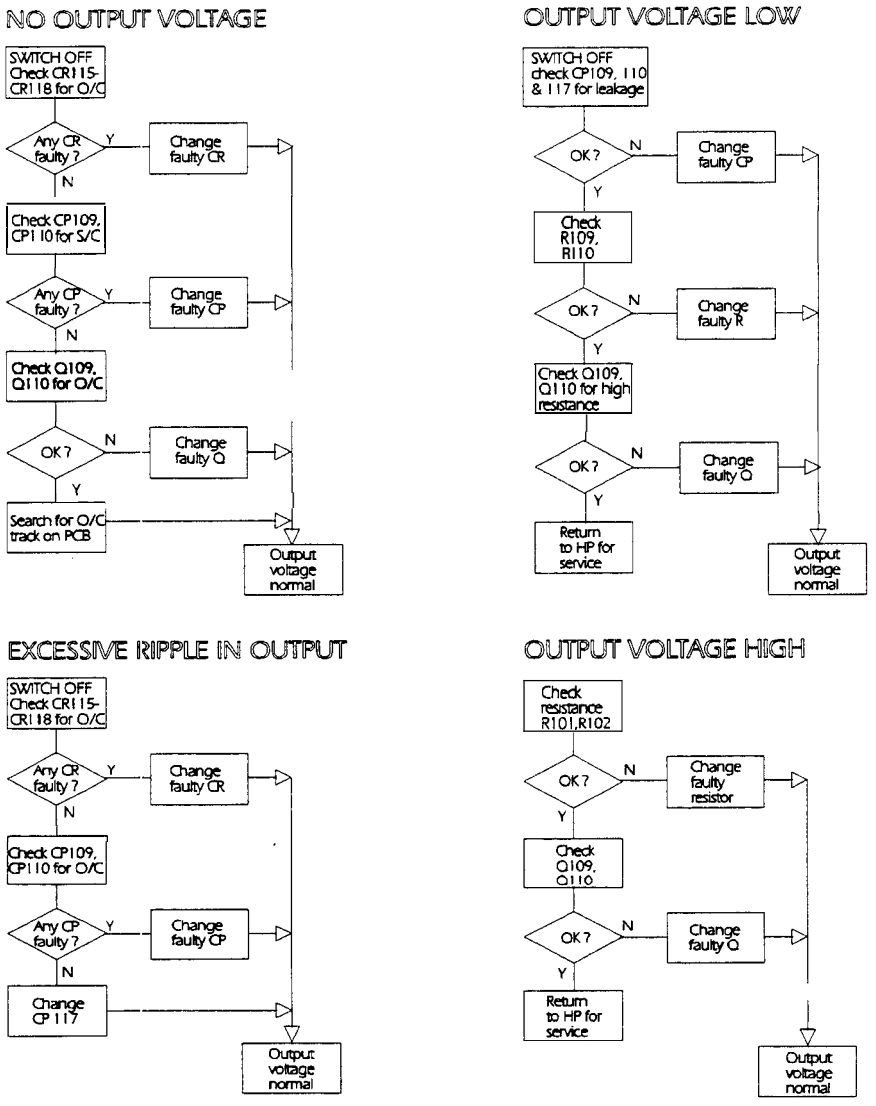


Figure 4-8.
Flowcharts for Tracing Common Faults in -15V Regulator

+5.1V / 2.7A No Output or Wrong Voltage

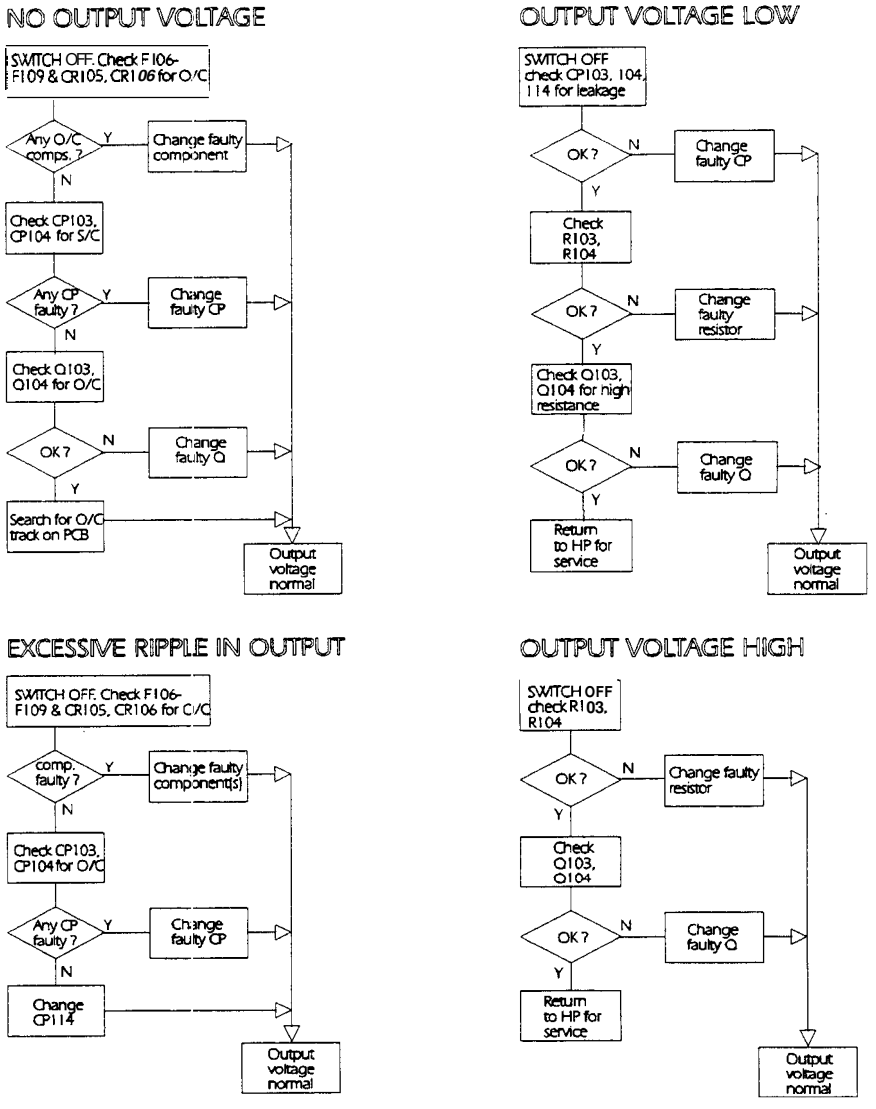


Figure 4-9.
Flowcharts for Tracing Common Faults in +5.1V Regulator

-5.1V / 2.5A No Output or Wrong Voltage

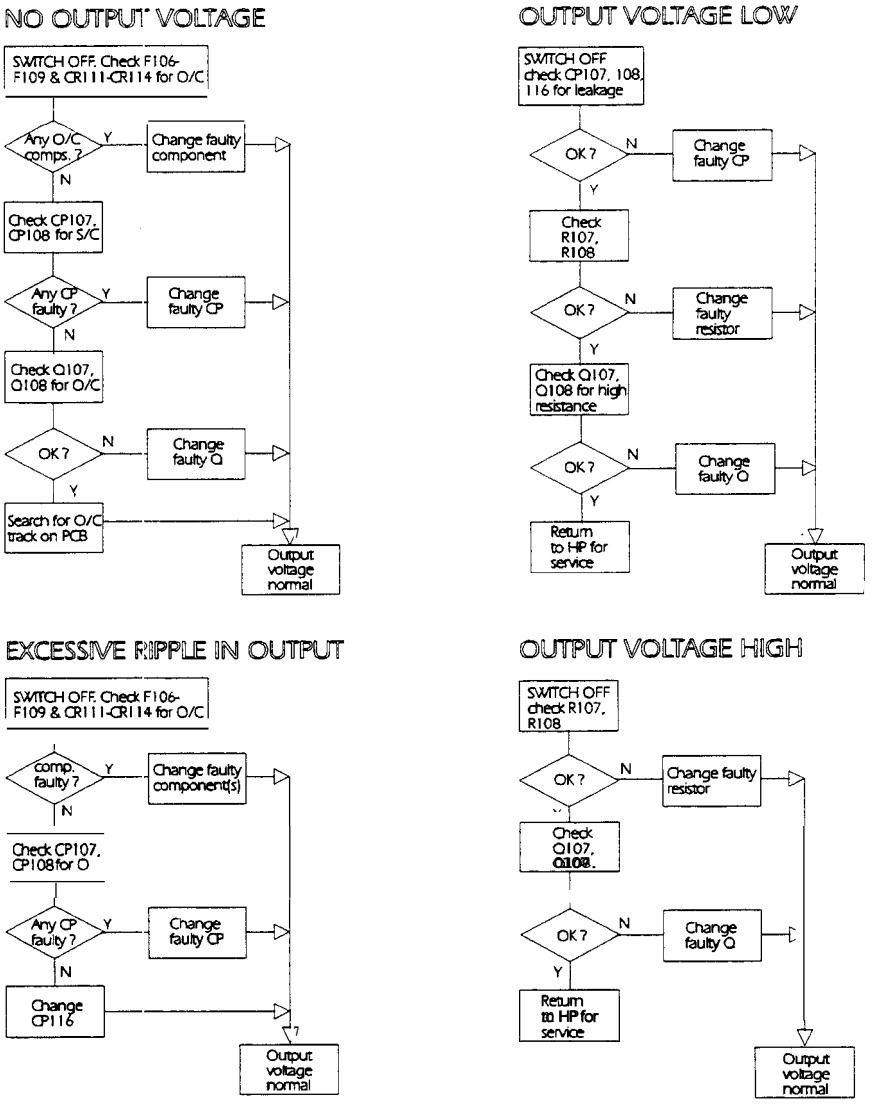


Figure 4-10.
Flowcharts for Tracing Common Faults in -5.1V Regulator

-4.5V / 3.5A No Output or Wrong Voltage

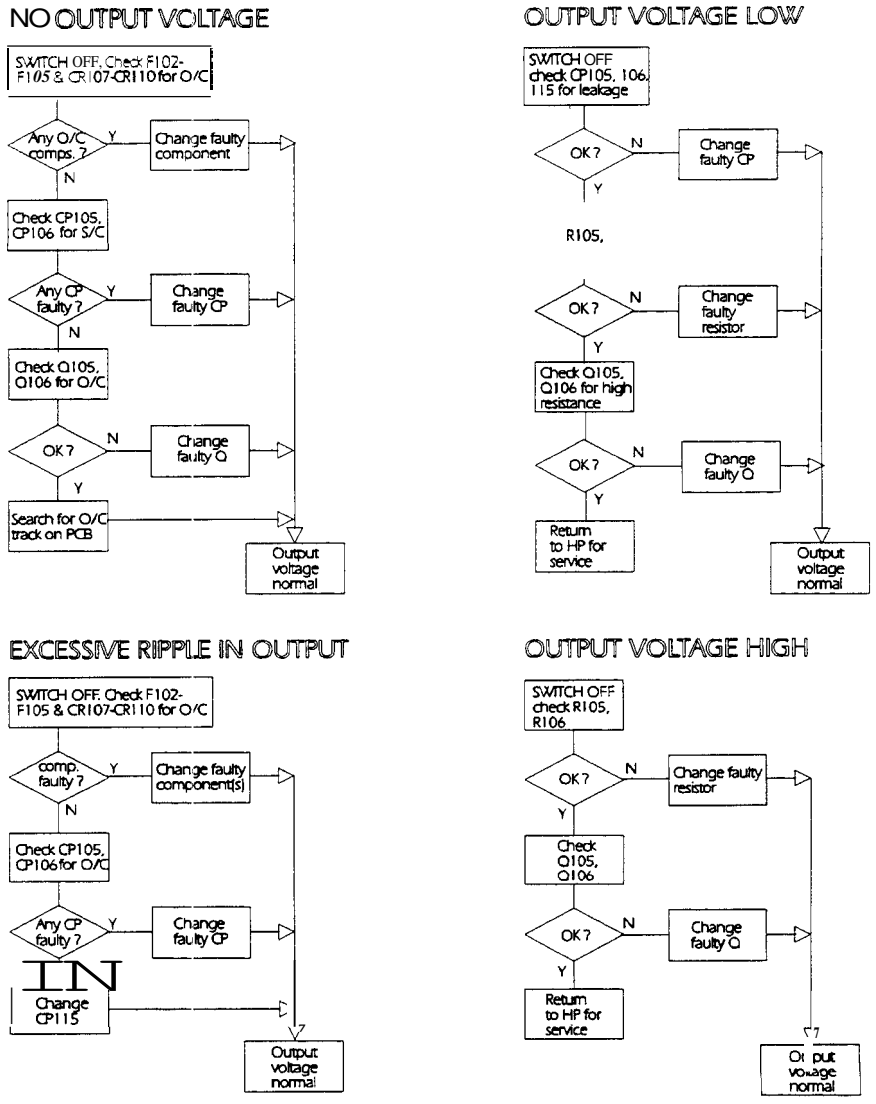


Figure 4-11.
Flowcharts for Tracing Common Faults in -4.5V Regulator

Power Control board

This board provides the following Services:

- Reference voltages
- -20V 1.0A Regulator Output
- +15V 1.8.4 Regulator Output
- -15V 1.1A Regulator Output
- +5.1V 2.7A Regulator Output
- -5.1V 2.511 Regulator Output
- -4.5V 3.511 Regulator Output

The flow-charts on the following pages enable faultfinding down to individual component level.

Reference Voltages Faulty

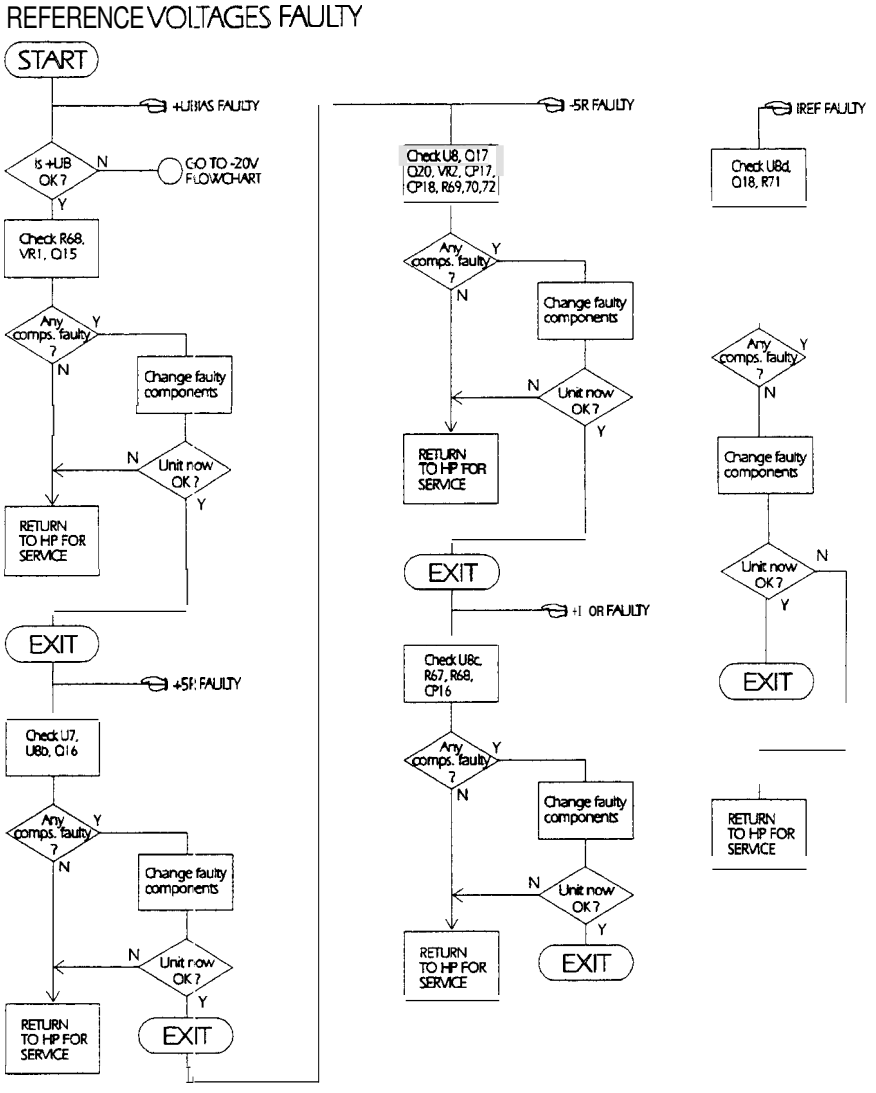


Figure 4-12. Flowchart for Tracing Reference Voltage Faults

-20V / 1.0A No Output or Wrong Voltage

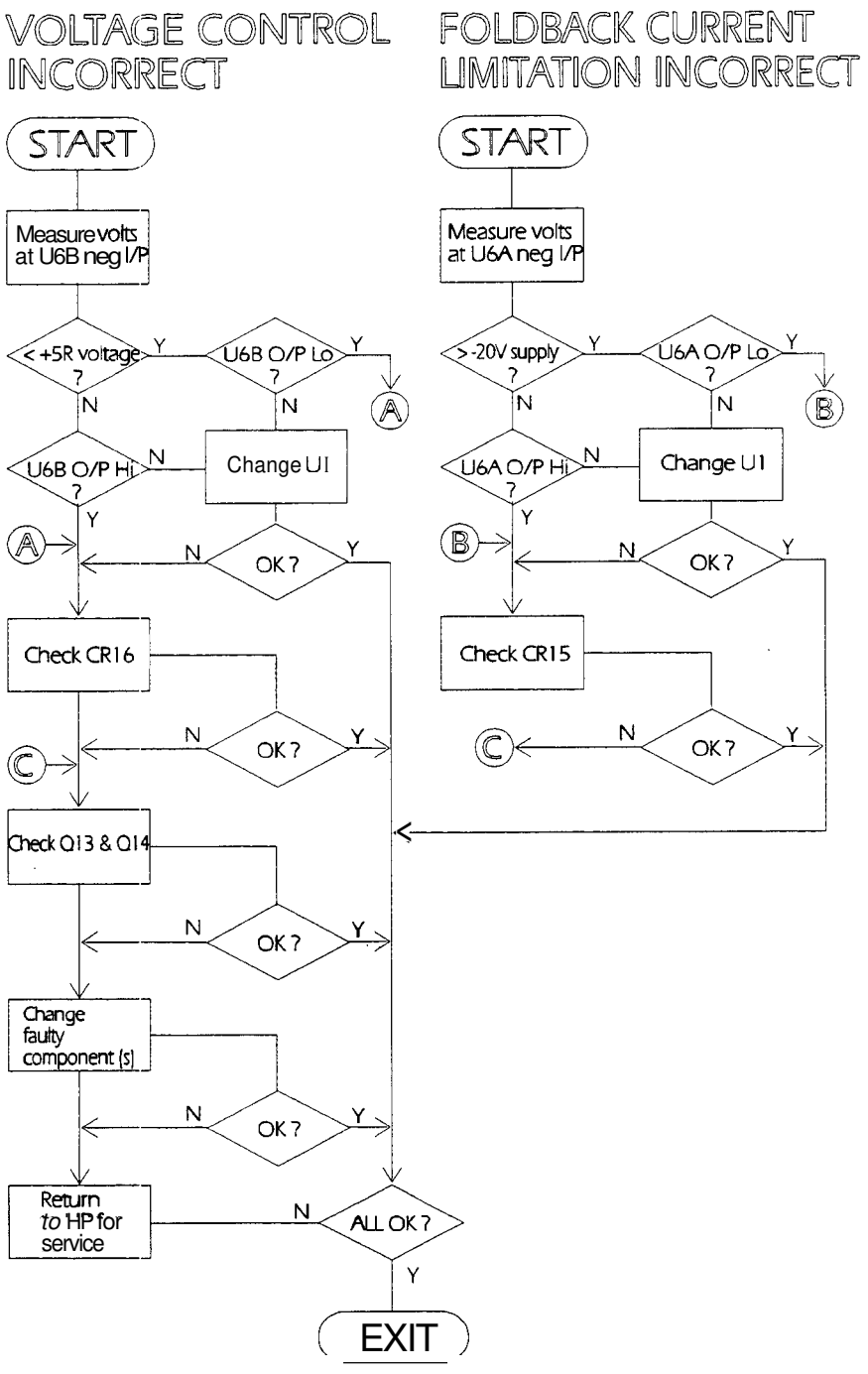


Figure 4-13.
Flowchart for Tracing Common Faults in -20V Regulator

+15V / 1.8A No Output or Wrong Voltage

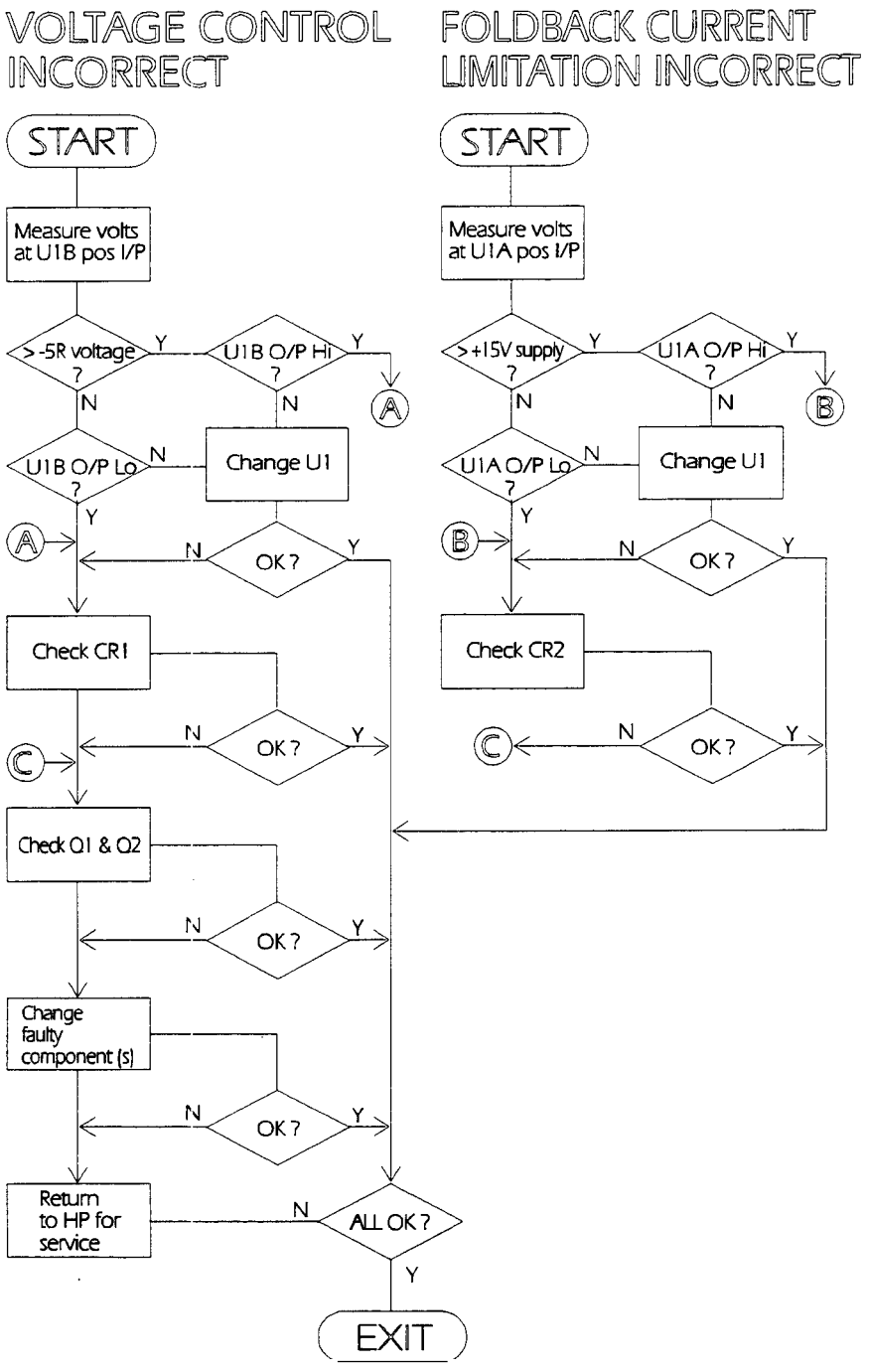


Figure 4-14.
Flowchart for Tracing Common Faults in +15V Regulator

-15V / 1.1A No Output or Wrong Voltage

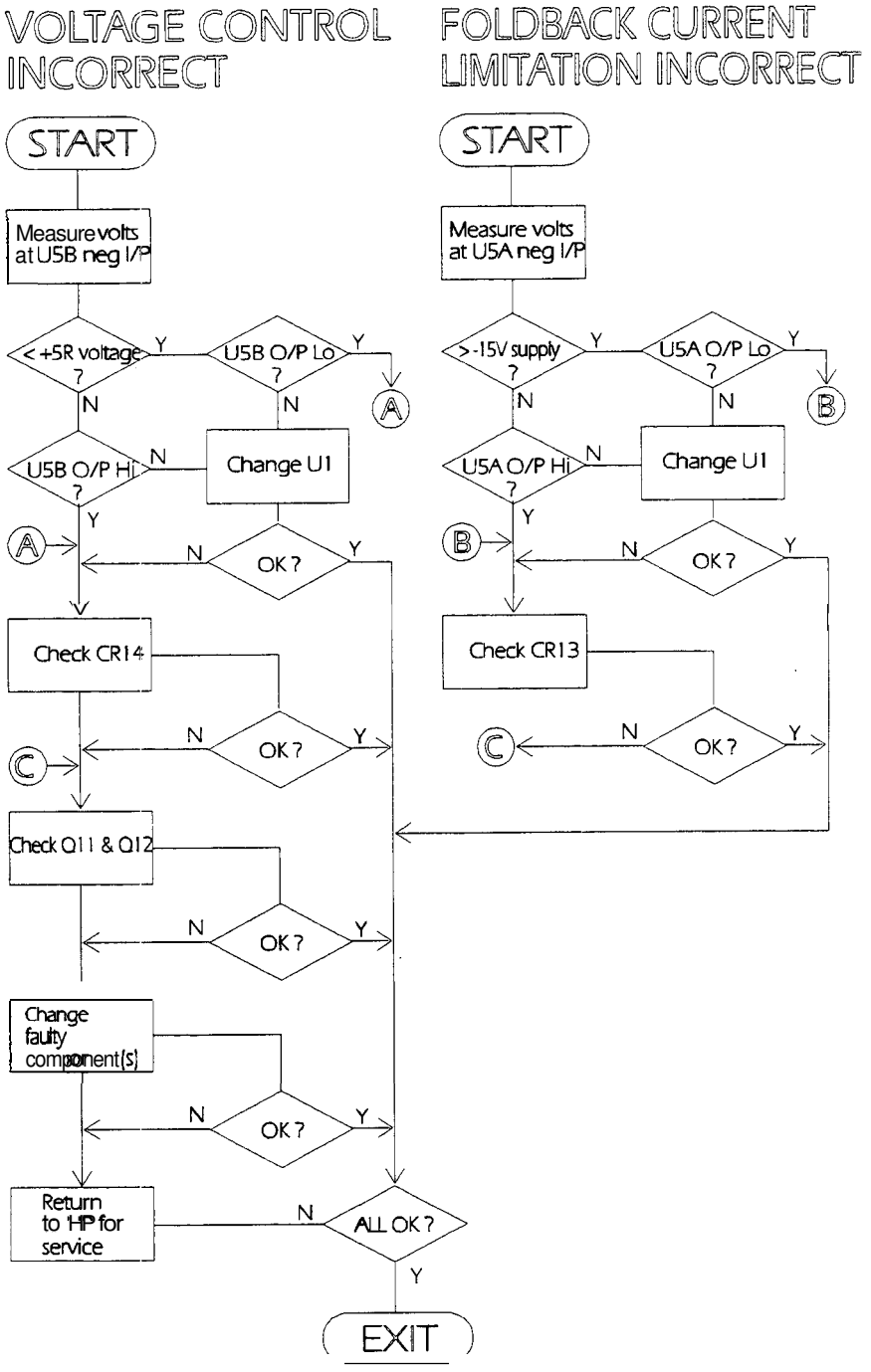


Figure 4-15.
Flowchart for Tracing Common Faults in -15V Regulator

+5.1V / 2.7A No Output or Wrong Voltage

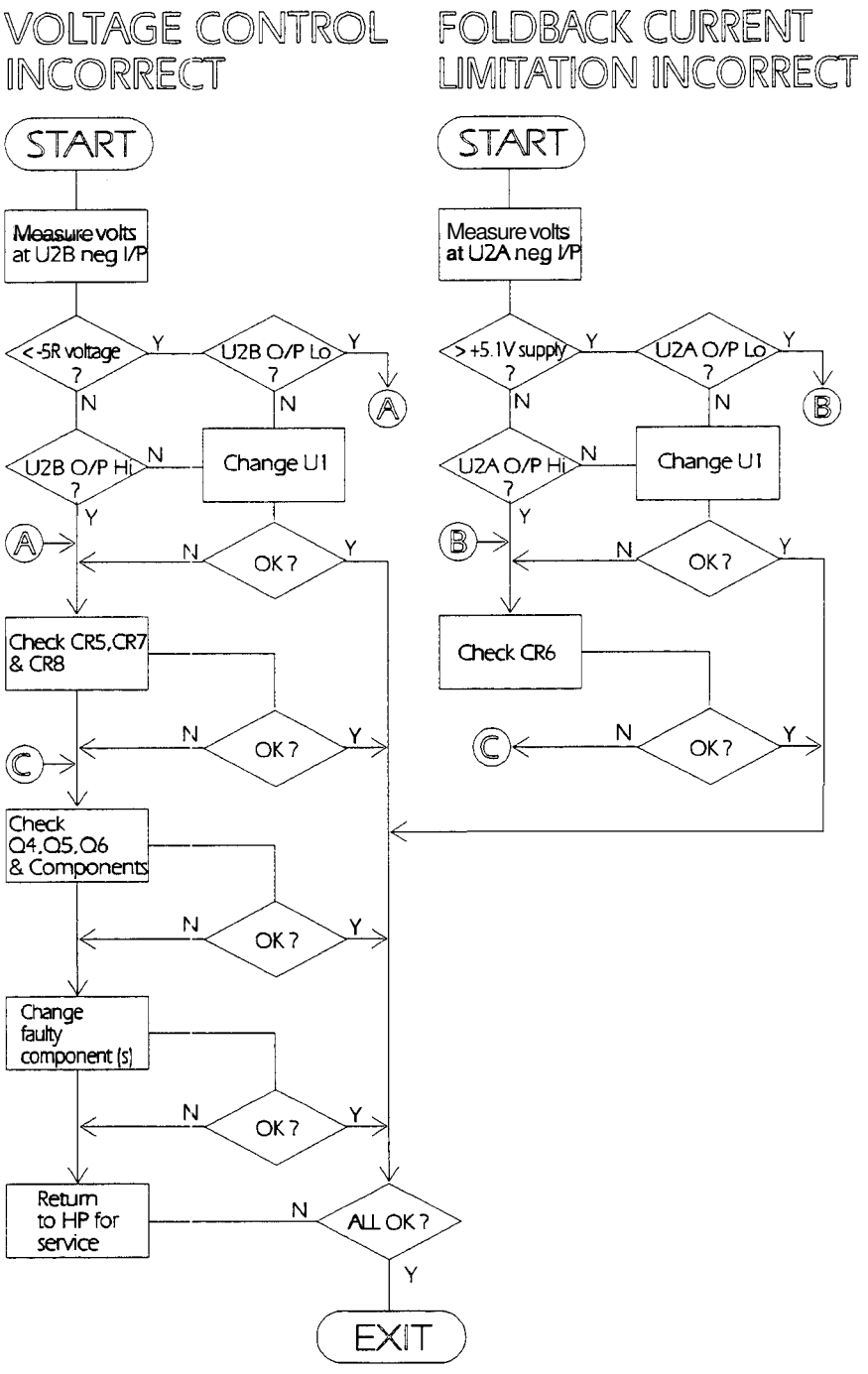


Figure 4-16.
Flowchart :for Tracing Common Faults in +5.1V Regulator

-5.1V / 2.5A No Output or Wrong Voltage

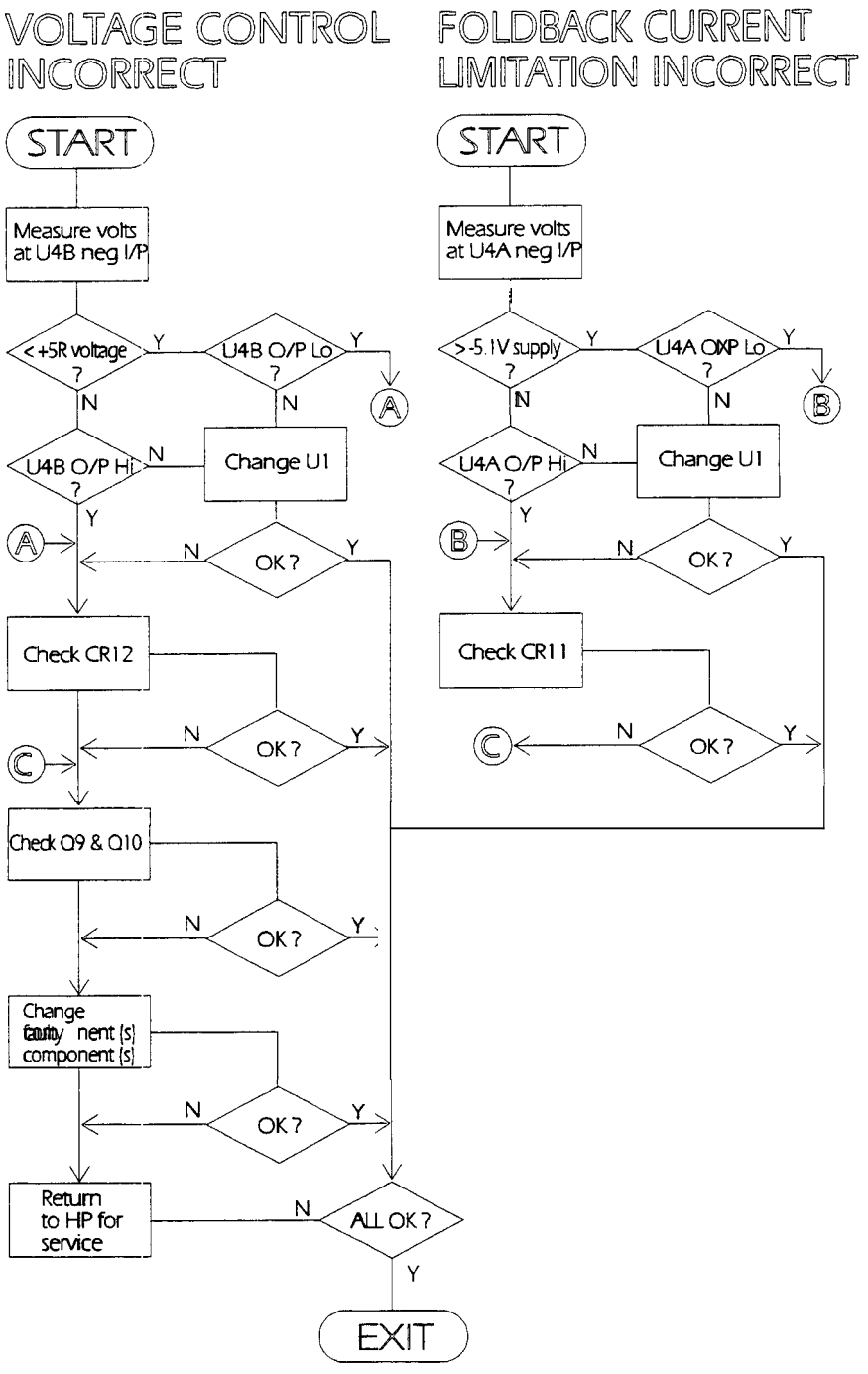


Figure 4-17.
Flowchart for Tracing Common Faults in -5.1V Regulator

-4.5V / 3.5A No Output or Wrong Voltage

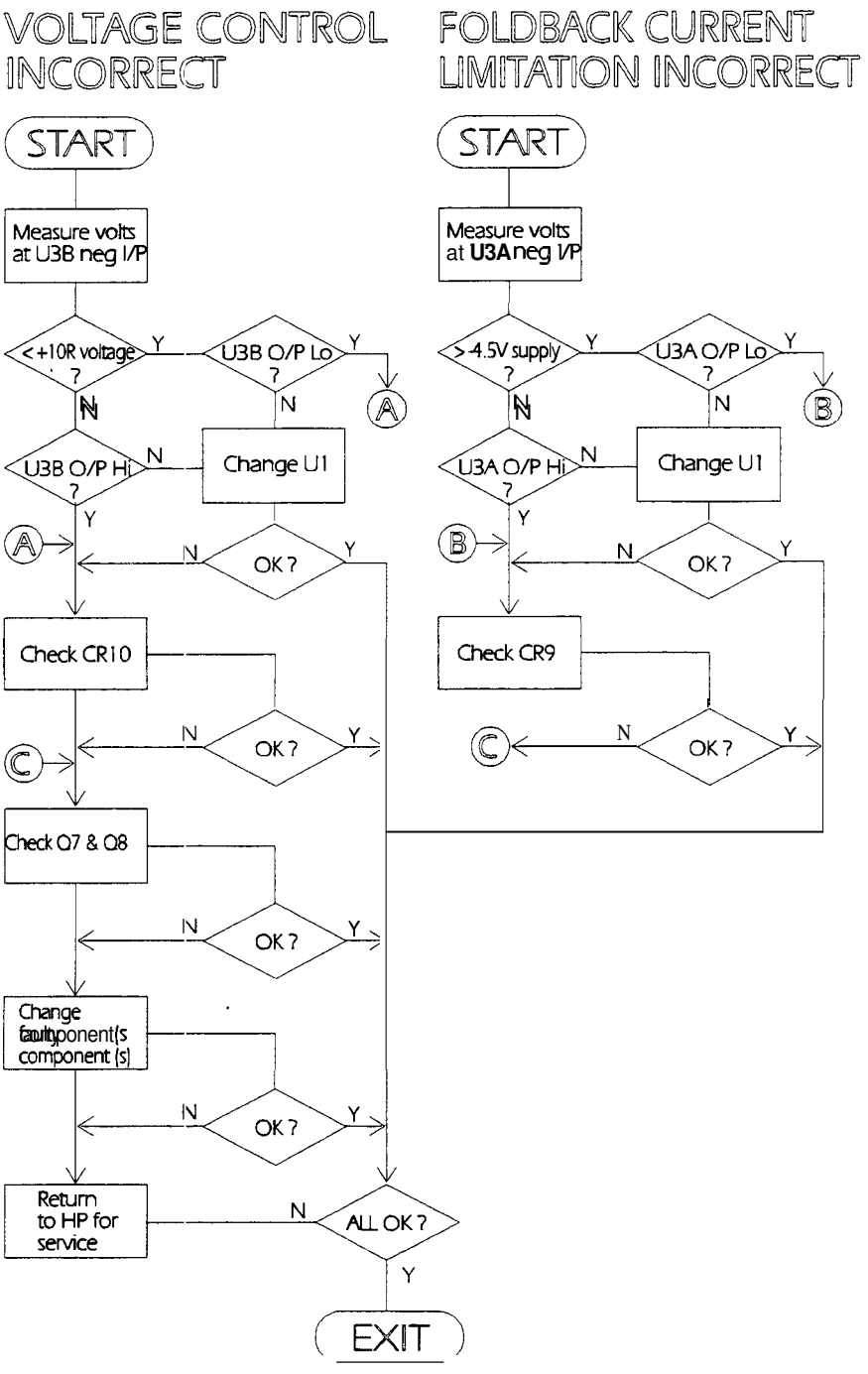


Figure 4-18.
Flowchart for Tracing Common Faults in -4.5V Regulator

Understanding the Self-Test Facility

The Self-Test function operates when the HP 8133A Pulse Generator is first switched on, providing there are no faults preventing its operation.

The self-test messages **and** their meanings are listed below:

Table 4-1. Self-Test Messages and Their Meanings

Message ID	Displayed Text	Meaning
E000	NO ERROR	Self-test was run successfully and no errors were found
E001	KEY JAMMED	A key on the front-panel keyboard is being continuously
	pressed, or is jammed	
E002	UNKNOWN INSTRUMENT OPTION	An option has been implemented that is not acceptable
E003	NO TIMING BOARD	Self-test cannot find a timing board (unlikely to be seen)
E004	NO WIDTH1 BOARD	Self-test cannot find a width1 board (unlikely to be seen)
E006	NO TIMING+WIDTH BOARD	Self-test can find neither width nor timing boards (unlikely to be seen)
E006	WRONG TIMING BOARD	Self-test finds the wrong timing board in the instrument (unlikely to be seen)
E007	CAN NOT LOCK PLL	The PLL is out of range (faulty) and cannot be locked
E008	FREQUENCY COUNTER ERROR	The frequency counter is giving an incorrect reading
E009	NO CALDATA ON TIMING BOARD	There is incorrect output or no output from the timing board
E010	NO CALDATA ON WIDTH1 BOARD	There is incorrect output or no output from the width1 board
E011	NO CALDATA ON WIDTH2 BOARD	There is incorrect output or no output from the width2 board
E012	NO CALDATA ON DATA BOARD	There is incorrect output or no output from the data board

The following faults are "fatal" and are unlikely to be encountered during normal operation, as they usually cause complete failure of the instrument, preventing the self-test facility from operating:

Table 4-2.
Fatal Self-Test Messages and Their Meanings

Message ID	Displayed Text	Meaning
	RAM error (U10 and/or U11)	RAM faulty (Either U10 and/or U11)
	RAM error (U10)	U10 faulty
	RAM error (U11)	U11 faulty
E110	EPROM checksum error	Incorrect checksum (faulty RAM or ROM)
E120	MFF error	Multi Functional Peripheral U21 faulty
E130	Keyboard controller error	Keyboard giving incorrect output or no output

Troubleshooting Faulty Assemblies

This section contains general tests to isolate a faulty board in the HP 8133A Pulse Generator, without dismantling the instrument.

The following diagram shows the relationships between the boards in the instrument. It shows two channels fitted. Refer only to the part that is relevant to your instrument.

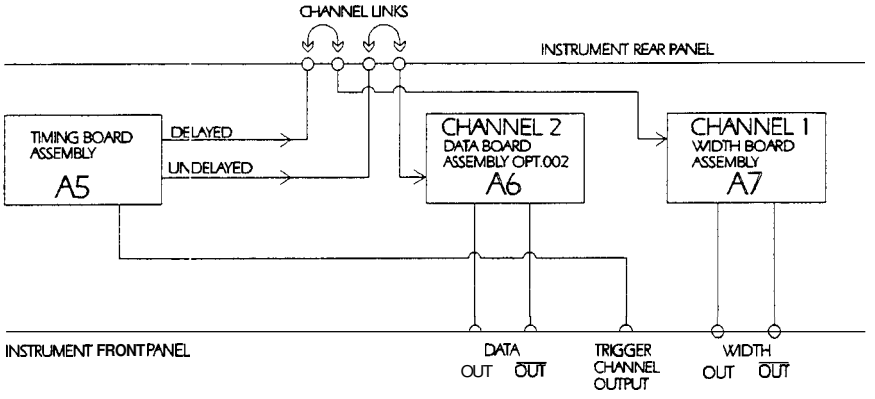


Figure 4-19. Channel Links and Outputs

Trigger Output Check

Detecting a signal at the Trigger Output proves that the Timing Board is working.

Connecting the Test Equipment

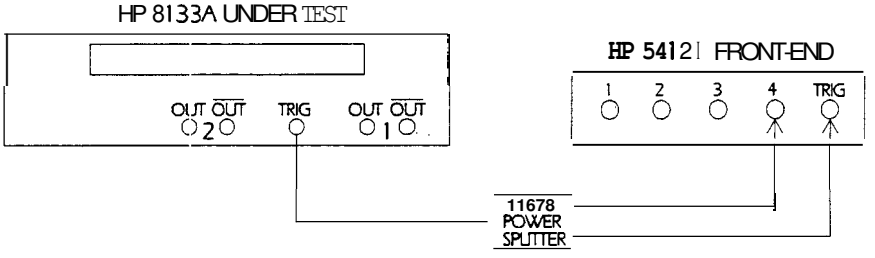


Figure 4-20. Setup for Testing the Trigger Output

Performing the Test

On the HP 8133A Pulse Generator:

1. Set the interrial frequency of the HP 8133A Pulse Generator under test to **500MHz**
2. **Set Trigger Output Hi** to **+0.5V**
3. Set **Trigger Output Lo** to **-0.5V**
4. Press **Enable**

On the Scope:

1. Select [Auto Scale]
2. Set [Volts/Div] to **200mV/Div**

3. Set [Time/Div] 10ns/Div
4. Center two pulses on the screen
5. Select [Delta V] and set [V Markers] to On
6. Set [Preset Levels] to 0 - 100%
7. Press [More], [Frequency]

The waveform displayed should look similar to this:

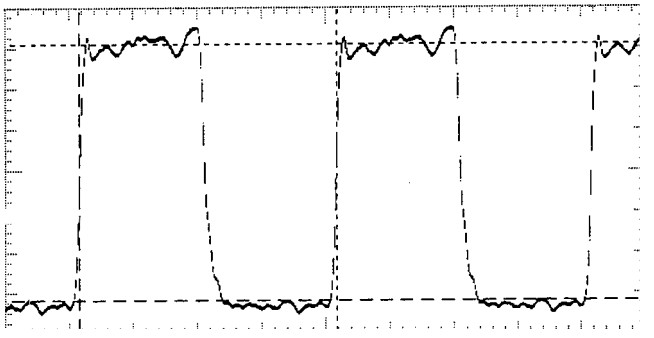


Figure 4-21. HP 8133A Pulse Generator Trigger Output Waveform

Checking the Channel Link

Before testing the Width Board output, the channel link should be tested, as loss of output could be due to a faulty Channel Link preventing the signal from the Timing Board from being passed to the Width Board.

Preparing for the Test

Locate the block holding the input and output channel links on the rear panel of the instrument. There are different configurations for these connections on the various options of the HP 8133A Pulse Generator, as follows:

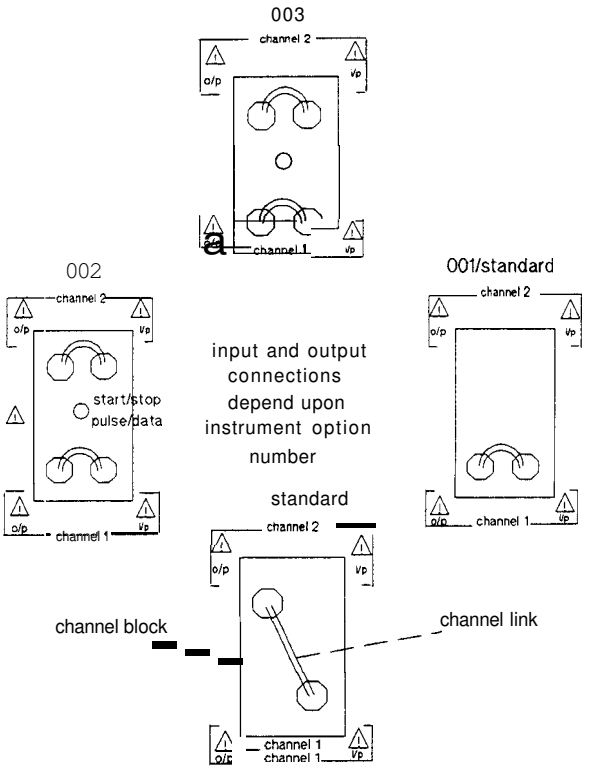


Figure **4-22.** Channel **Block Link** Configurations

Identify the link: you want to check, **and** remove it from the block.

Caution

Alternately loosen each nut on a single link about half a turn at a time. This avoids one side of the link being freed at a greater rate than the other and thereby locking or distorting the channel links.

Loosen the SMA link nuts with a type A 7.9mm torque wrench.

On a dual channel instrument replace the links in the same location when boards are NOT being returned for service. This ensures that an instrument which is calibrated continues to give accurate signals.

Testing the Channel Link

Using a resistance meter:

1. Check for continuity of <1Ω from each end on the inner cable
2. Check for continuity of <1Ω from each end on the outer shield
3. Check that there is no continuity between the inner and the outer shield

If the link **is** faulty, replace it. If it is OK, retain it for replacement after the next test.

Timing Board Output Check

Detecting a waveform at the output of the Timing Board proves that a signal is available to drive the Width Board.

Connecting the Test Equipment

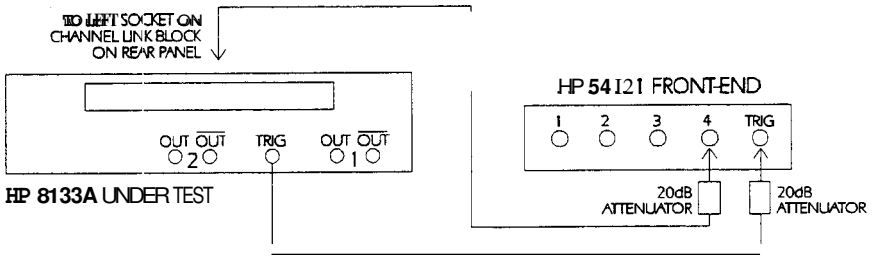


Figure 4-23. Setup for Testing the Width Board Output

On the Scope:

1. Select (Auto Scale)
2. Set (Volts/Div) to **200mV/Div**
3. Set (Time/Div) **500ps/Div**
4. Select (Delta) and set (———) to **On**
5. Set (Preset Levels) to **0 - 100%**
6. Select (Delta T)
7. Press (More), (Frequency)

The waveform displayed should look similar to this:

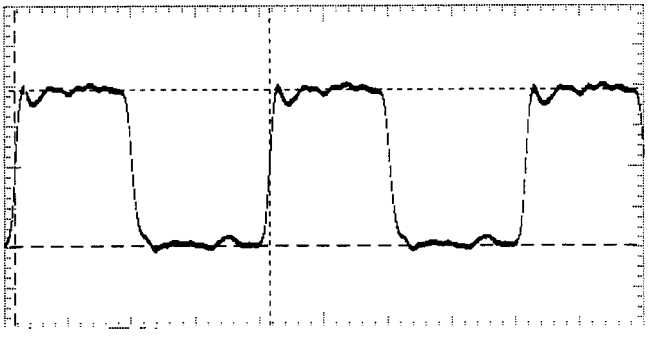


Figure 4-24. Width Board Output Path Waveform

Replace the Channel Link on the rear panel of the instrument, taking care to use the correct method as described in **Caution** above.

Option 1 Fitted

If your instrument has been fitted with Option 1, perform the following tests to check the Width Board Output path:

Width Board Output Path

On the Scope:

1. Select (Auto Scale)
2. Set (Volts/Div) to **200mV/Div**
3. Set (Time/Div) **200ps/Div**
4. Select (Delta V) and set (V Markers) to **On**
5. Set (Preset Levels) to ***50%***
6. Select (Delta)
7. Set **Precise Edge Find**
8. On the HP 8133A Pulse Generator front panel, vary the delay on Channel 1

The displayed waveform should move to the right and left of center, indicating that the delayed output is functioning.

Replace the Channel Link on the rear panel of the instrument, taking care to use the correct method as described in **Caution** above.

Option 2 Fitted

If your instrument has been fitted with Option 2, perform the following tests to check the Data Board Output path:

Remove the Channel 2 link from the rear of the HP 8133A Pulse Generator, taking care to observe the correct method of removal as described in **Caution** above.

Testing the Channel 2 Link

Using a resistance meter:

1. Check for continuity of **<10** from each end on the **inner** cable
2. Check for continuity of **<1Ω** from each end on the **outer** shield
3. Check that there is **no continuity** between the **inner** and the **outer** shield

If the link is faulty, replace it. If it is OK, retain it for replacement after the next test.

Data Board Output Path

On the Scope:

1. Select (Auto Scale)
2. Set (Volts/Div) to **200mV/Div**
3. Set (Time/Div) **500ps/Div**
4. Select (Delta V) **and** set (V Markers) to **On**
5. Set (Preset Levels) to **0 - 100%**
6. Set -500mV to +500mV on the waveform

The waveform displayed should look similar to this:

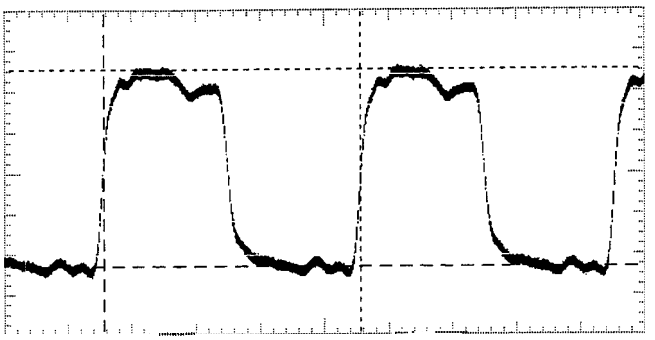


Figure 4-25. Data Board Output Path Waveform

Replace the Channel Link on the rear panel of the instrument, taking care to use the correct method as described in **Caution** above.

If any of the above tests reveal a faulty board, send the complete instrument to your HP Service Center.

5

Replacing Assemblies

This chapter will enable you to remove and replace the main assemblies of the HP 8133A 3GHz Pulse Generator. There are two sub-units contained within the instrument's chassis:

1. The card cage and its assemblies, which produce and control the pulse generator functions.
2. The power supply cage, which contains the power supply assemblies and the microprocessor.
3. First decide which set of assemblies you need to access, card cage or power supply, then follow the appropriate set of the two sets of steps detailed below.

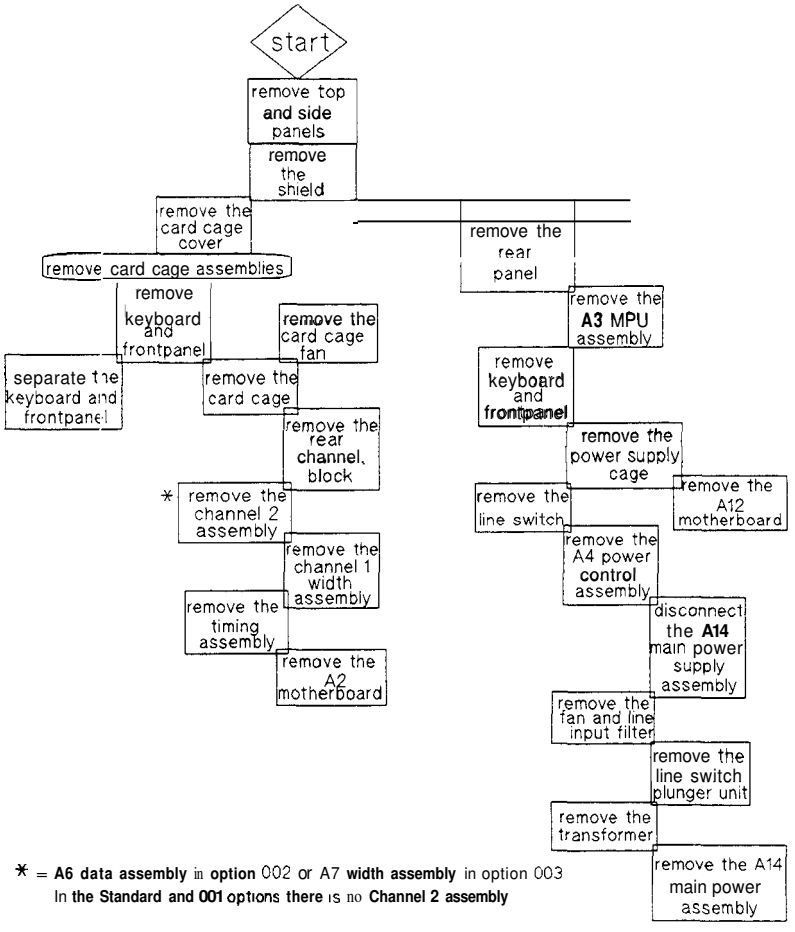


Figure 5-1. Sequence of operations

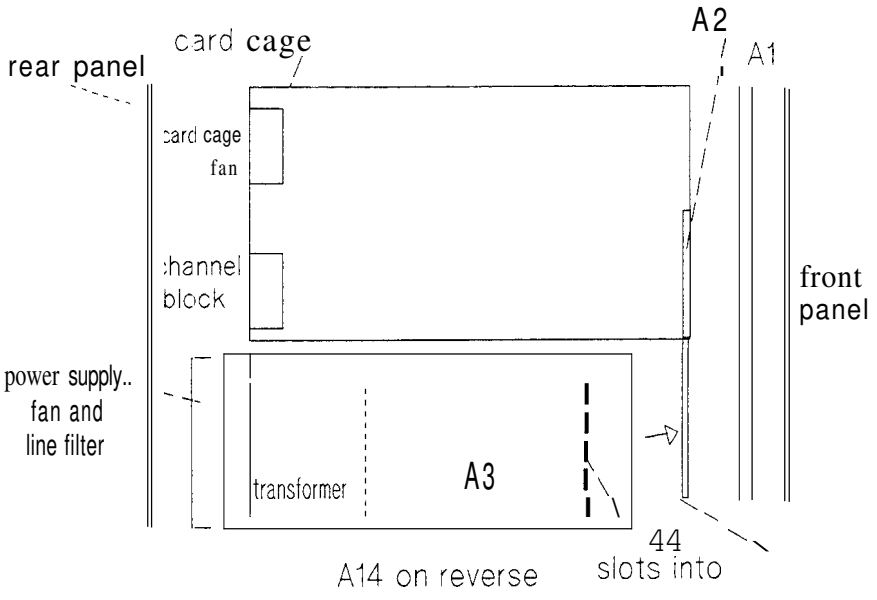


Figure 5-2. Plan view of instrument

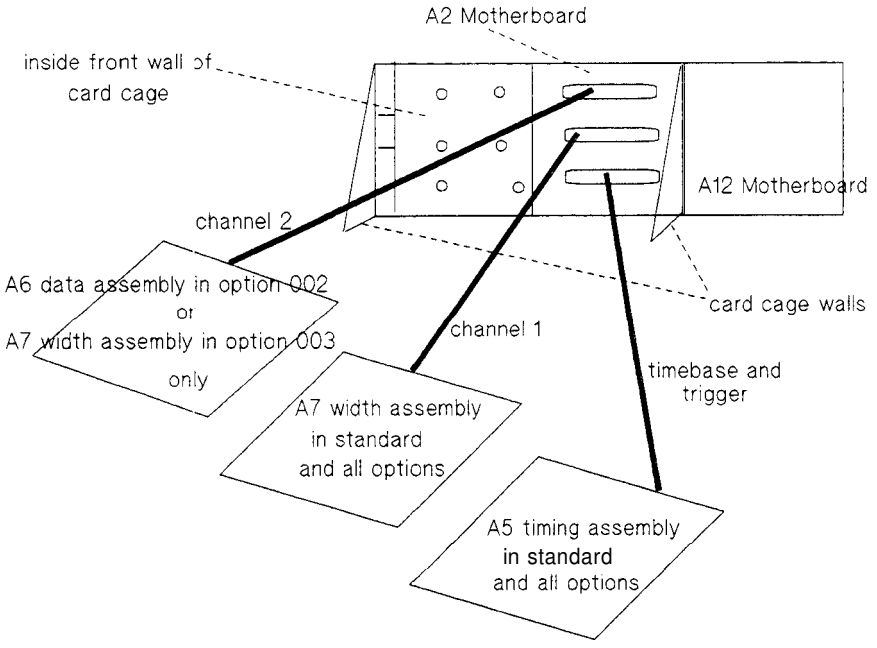


Figure 5-3. Card cage assembly locations

Table 5-1. Assemblies Indentification Table

Assembly	Description
A1	Keyboard
A2	Motherboard (Cardcage)
A3	Microprocessor Board
A4	Power Control Board
A5	Timing Board
A6[1]	Data Board
A7[2]	Width Board
A12	Motherboard (Power and MPU)
A14	Main Power Board

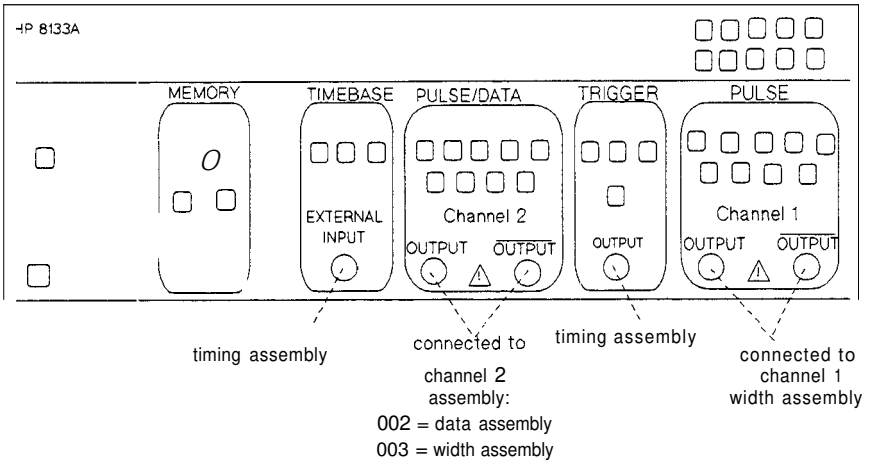


Figure 5-4. Frontpanel internal connections

Removing the top and side panels

1. Remove the four plastic feet on the rear of the instrument.
2. Loosen the screw found in the middle of the rear flange of the top cover and slide the panel to the rear to remove it.
3. Remove the carrying handle (on left panel as front of instrument faces you) by unscrewing its two securing nuts and removing the retainers at each end of the handle. Slide the left panel backwards to remove it.
4. Remove right side panel by loosening the screw in the middle of its rear flange arid sliding the panel backwards.

Removing the shield

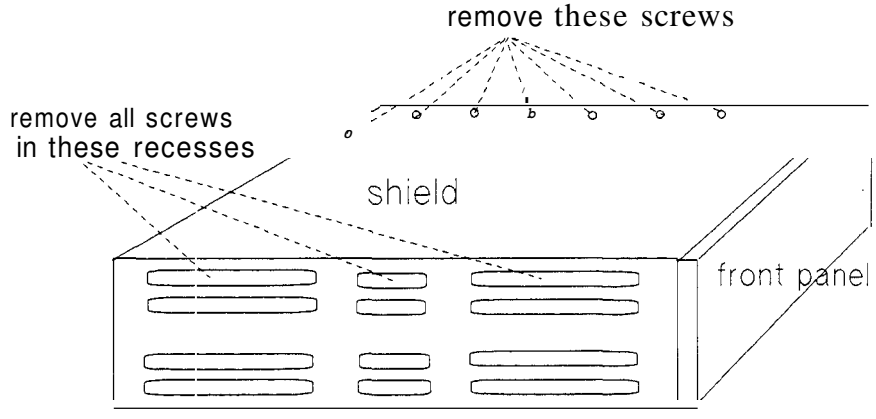


Figure 5-5. Shield securing screws

1. With the front of the instrument facing you, remove the six screws along the right edge of the shield and one on the rear edge.
2. Removing the seven screws located in the upper channel of the upper left frame strut, see Figure *5-5.*

Caution

Do not lift the shield at too great an angle. Do not force the shield or the assembly under it may be damaged.

3. Turn the right side of the pulse generator towards you and lift the shield's right edge at a slight angle. With your thumbs along the top of the shield apply pressure to it with the heels of your palms. If the shield is held at the correct angle it should then pull out towards you.

Removing the card cage and its assemblies

Removing the card cage cover

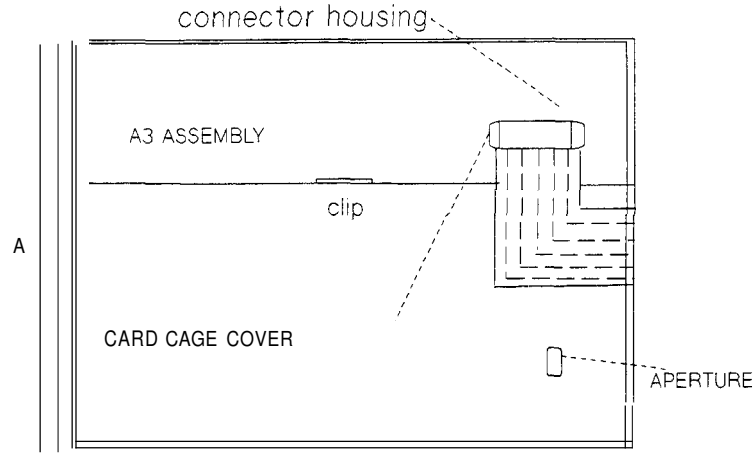


Figure 5-6. Connector ribbon location

1. Free the connector ribbon, which lays over the rear left corner of the card cage, from its housing on the **A3** assembly by opening the clips on each side of the connector housing and easing it free. Fold the ribbon over the rear frame.
2. Remove the sixteen **screws** around the front, right and rear edges of the card cage cover.
3. Free the securing clip located at the middle of the left edge of the card cage cover and lift the cover out to the left.

Removing the frontpanel and A1 keyboard

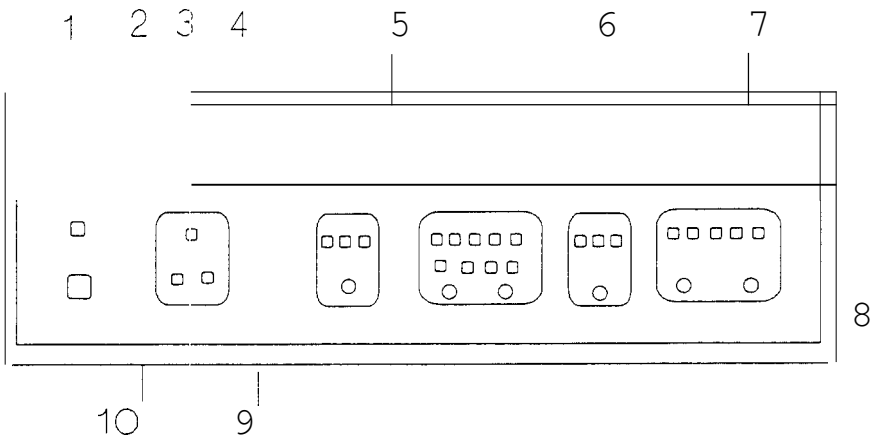


Figure 5-7. A1 Keyboard assembly securing screws

1. Remove the top and side trims on the front frame of the chassis in order to access and remove the screws securing the A1 keyboard assembly.
2. Remove the ten screws shown in Figure 5-7 if the A1 keyboard and frontpanel assembly *and* the card cage are to be removed.
3. Screws 2 and 3 secure the card cage to the chassis front frame, and may be left in position if only the A1 keyboard and frontpanel assembly is to be removed.
4. When its securing screws have been removed ease the top of the A1 keyboard and frontpanel assembly out of the chassis and locate the W100 connector ribbon, found at the top left of the keyboard assembly.
5. Pull back the clips on each side of the connector housing to release the connector.
6. Remove the W100 connector ribbon from its housing.
7. Remove the A1 assembly and frontpanel completely and if necessary separate the frontpanel from the A1 assembly, as described in the next section, in order to access the assembly components.

Separating the A1 keyboard assemlbly from the frontpanel

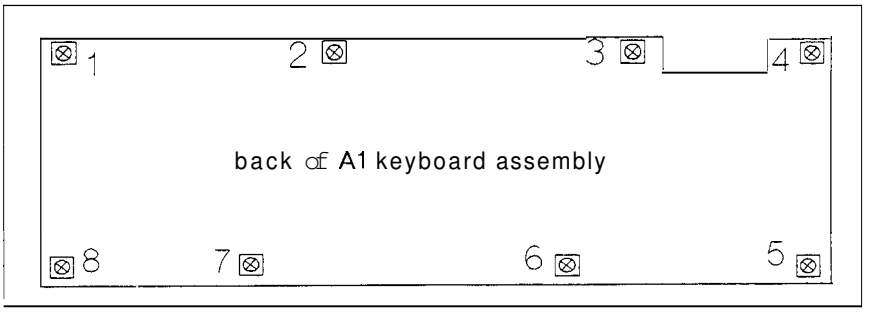


Figure 5-8. A1 keyboard and frontpanel separation

1. **Remove the eight screws detailed in Figure *5-8* and separate the A1 assembly and the front panel to gain access to the A1 keyboard assembly components.**

Removing the card cage

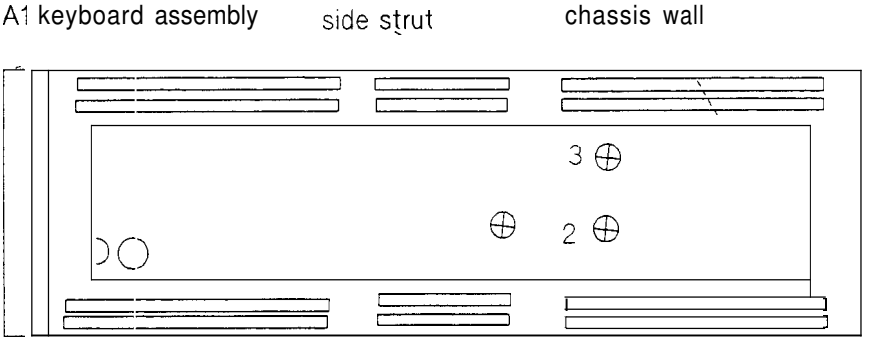


Figure 5-9. Screws securing card cage to right hand chassis wall

1. **Remove the three screws located in the right side of the chassis. Refer to Figure 5-9**

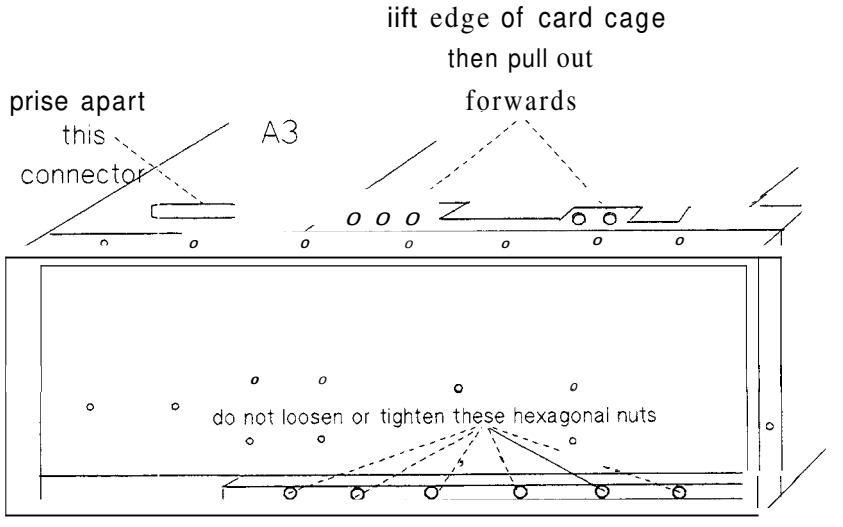


Figure 5-10. Remove the card *cage* from the chassis

2. Place your thumbs on the front top strut of the front frame and your right hand fingers over the front edge of the card cage, lift and pull forwards. The front of the card cage will move forward over the edge of the front frame and can then be removed completely. The fingers of the left hand may be needed to ease open the pin connector housing between the A1 assembly and the **A3** assembly.

Removing the card cage fan

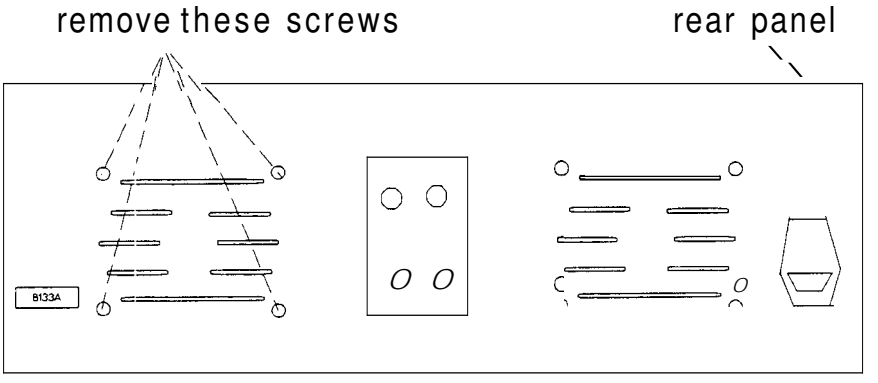


Figure 5-11. Card cage fan

1. Uncouple the fan power supply cable at location 521 on the **A3** MPU assembly.
2. Remove the four screws which secure the card cage fan to the rear panel.
3. Remove the fan.

Removing the channel link block

1. Turn the card cage so that its rear is facing you.
2. Locate the block which holds the input and output channel links, there are different configurations for these connections on the various options of the HP 8133A. These configurations are shown in Figure 5-12:

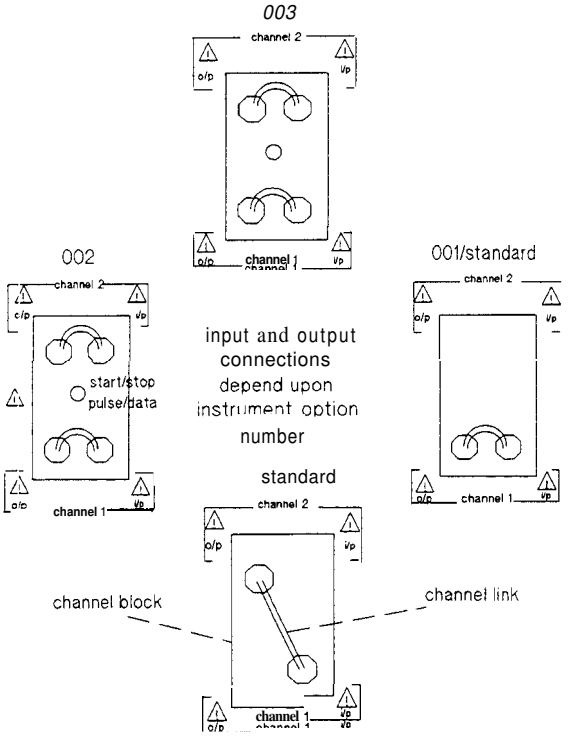


Figure 5-12. Channel block link configurations

Caution

Alternately loosen each nut on a single link about half a turn at a time. This avoids one side of the link being freed at a greater rate than the other and thereby locking or distorting the channel links.

Loosen the **SMA link** nuts with a type **A** 7.9mm torque wrench.

On a dual channel instrument replace the links in the same location when boards art?NOT being returned for service. This ensures that an instrument which is calibrated continues to give accurate signals.

3. Remove the links, on a dual channel instrument you can tape one link to identify which set of studs it must return to.
4. On option 002 only there is a brown co-axial cable running from the center stud of the block to location 5112 on the A6 assembly; disconnect this cable at 5112. The connector is a push/pull type.

5. Remove the flat hexagonal nuts and washers that secure the threaded SMA assembly connectors to the block, see Figure **5-13.** Use a 7.9mm socket for this.

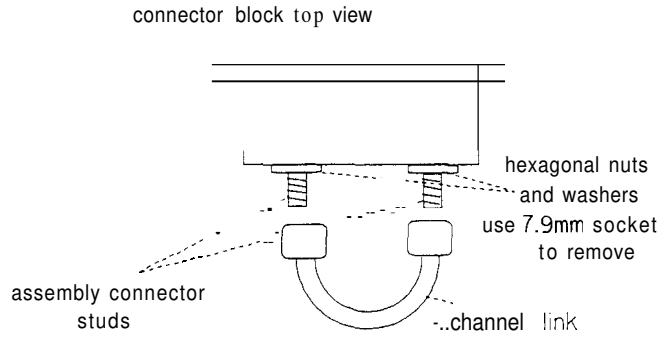


Figure 5-13. Location of hexagonal securing nuts

6. Remove the ten screws which secure the block to the card cage and remove the block, see Figure **5-14.**

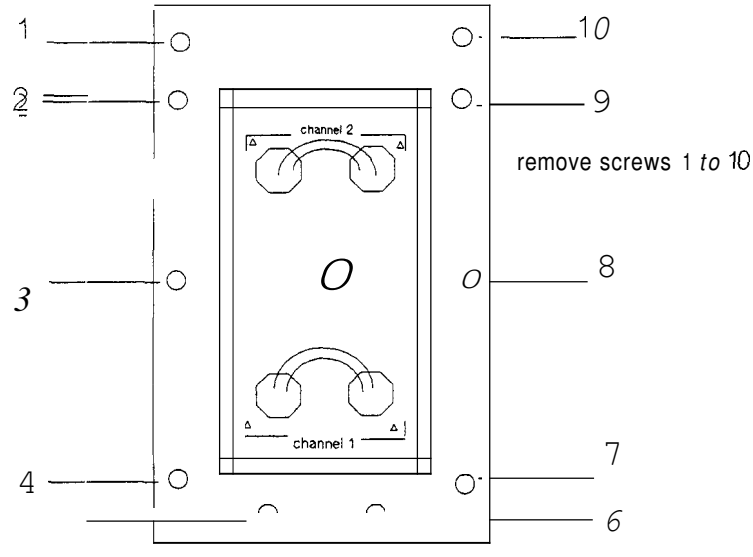


Figure 5-14. Channel block securing screws

Removing the board keepers

1. The two board keepers are located in the card cage, between the rear of the card cage and the assemblies in the card cage. Their function is to hold the assemblies secure.
2. Twist the board keepers in a clockwise direction, until they are free of the assemblies, and lift them out.
3. Notice that the keepers have locator feet at top and bottom. The smaller feet always relocate in the holes in the bottom of the card cage.

Removing the channel 2 assembly, channel 1 assembly, and timing assembly

1. Refer to Figure 5-3 to identify which assemblies are fitted to your instrument.
2. Turn the card cage so its front is facing you.

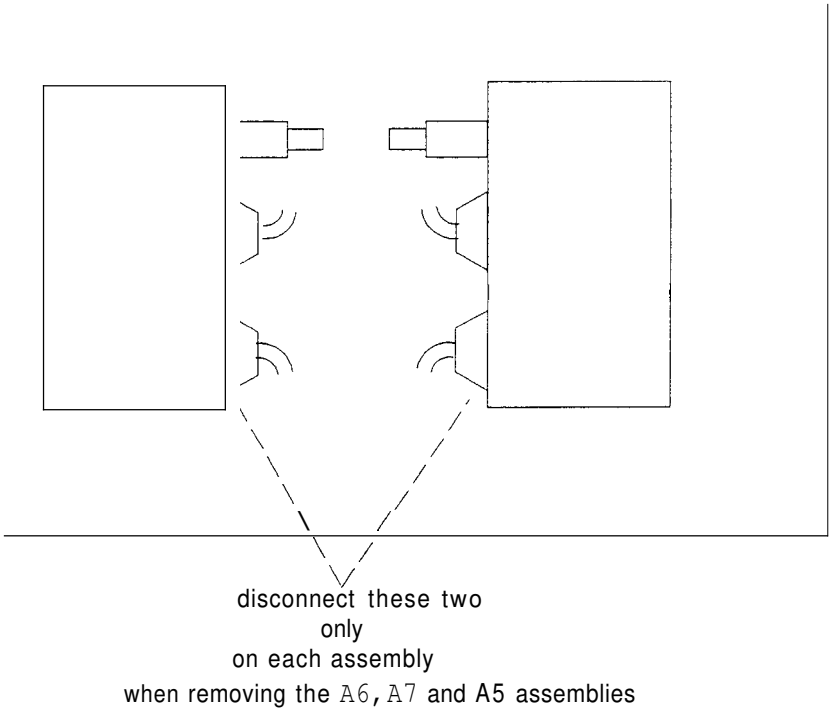


Figure 5-15. Relay box connectors

Caution 

Note carefully the routing of the cable mentioned in the next step and ensure that the cable is replaced in ***exactly*** the same position when replacing this board.

3. On option 002 only, locate and free the brown co-axial cable which connects the A6 (channel 2) assembly to the A5 timing assembly. The cable joint to be separated is on the **A6** assembly at location J104.
4. On options 002 and 003 only locate the two relay boxes at the front right of the channel 2 assembly. Each of these relays is connected to two semi-rigid cables by **SMA** connectors.
5. Locate the two **SMA** connector nuts which are nearest to the front edge of the card cage, one connects to the left relay box and one to the right relay box. See Figure 5-15.
6. Use the type C 7.9mm torque wrench with a removable head to disconnect these two **SMA** nuts from the relay box.
7. Slide the channel 2 assembly towards the rear of the card cage and lift it out to the left.
8. Repeat steps **3** to 6 to remove each assembly **in** the card cage.

Removing the A2 Motherboard assembly

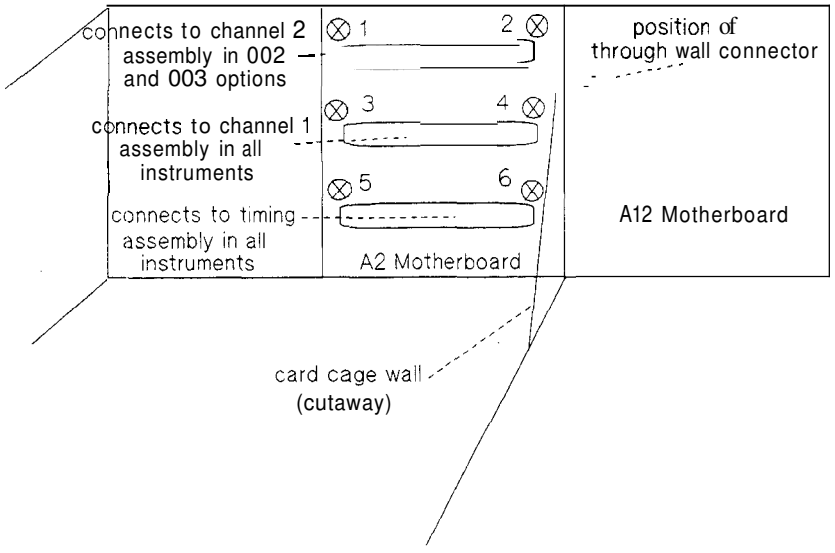


Figure 5-16. A2 motherboard removal

1. The **A2** assembly is the motherboard for the card cage assemblies. All of the card cage assemblies must be removed to access the **A2** motherboard.
2. Remove screws 1 to 6, shown in Figure 5-16.
3. The **A2** motherboard can then be freed of the through wall connector, Figure 5-16, to the **A12** motherboard and lifted out.

Reassembling the card cage and its assemblies

Reassembly is basically the reverse of disassembly, but there are some details to be careful of.

Assembly replacement

1. Replace the **A5** timing assembly first. Replace it from the left of the card cage into its original position at the bottom, being careful not to catch the front and rear semi-rigid cables on anything.
2. Locate the guide pin on the left edge of the A5 timing assembly into its locator groove on the inside left wall of the card cage.
3. When the assembly is located correctly, slide it forward until the front right corner of the assembly locates into the board holder brackets in the front right corner of the card cage.
4. Make sure that the assembly connector pins locate fully into the **A2** motherboard housing when replacing assemblies.
5. Carefully tighten the two **SMA** connector nuts onto the relay **box** studs by hand, then with the type *C* 7.9mm torque wrench. ***Do*** ***not overtighten these nuts.***

6. Repeat steps 1 to **4** to replace the channel one and two assemblies. The channel 2 (top) assembly does not have a guide pin.

Replacing the channel block

1. Replacing the block is the reverse procedure to removing it, but extra care is needed when replacing the links.
2. Reconnect the brown co-axial cable, running from the timing assembly, at location 5112 on the **A6** data assembly (OPTION 002 ONLY).
3. Replace the card cage into the chassis. Refer to Figure 5-9 and Figure 5-10.
4. Replace the hexagonal nuts and washers on the threaded studs. Refer to Figure 5-13.
5. Read the following caution ***before*** replacing the channel links.

Caution

Replace the each channel link to the same input/output connection from which it was removed. If they are mixed the waveforms generated by the instrument will be out of calibration. The SMA nuts should be tightened alternately by about half a turn each, using the type A 7.9mm torque wrench.

Replacing the A1 keyboard assembly

Caution

The hexagonal nuts which secure the threaded SMA studs at the ***front*** of the card cage DO NOT require loosening or tightening at any time. Refer to Figure 5-10 for the location of these nuts

1. Before replacing the A1 keyboard assembly replace and tighten the three screws on the right side of the chassis which secure the card cage to the chassis.
2. Secure the frontpanel to the A1 keyboard assembly, if it has been removed.
3. Replace the keyboard assembly in the frontframe, and reconnect the W100 connector ribbon to its position at the top left of the assembly.
4. Replace and tighten the A1 assembly securing screws. See figure 5-8.
5. Replace the top and side trims. It is important that the top trim is replaced as shown in Figure 5-17.

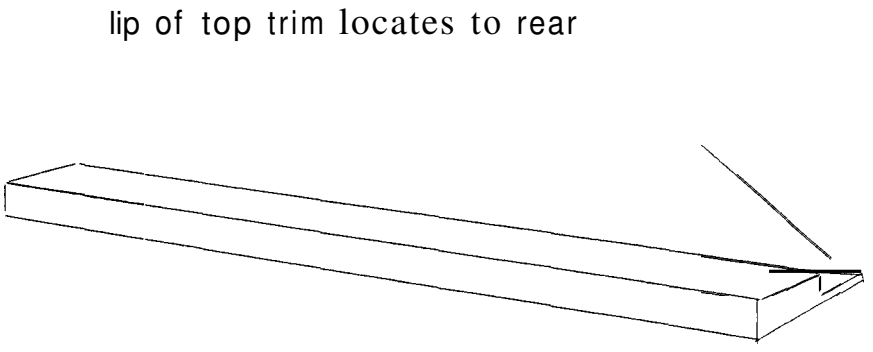


Figure 5-17. Top trim replacement

Replacing the card cage cover, shield and panels

1. Fit the assembly keepers into the card cage. The smaller feet locate into the holes in the bottom of the card cage.
2. Slide the card cage cover into position from the left side of the instrument. See Figure 5-6.
3. Make sure that the right edge locates under the flanges on the chassis.
4. Position the top feet of the assembly keepers into the apertures in the rear of the card cage cover.
5. Place the clip on the left side of the cover over the left wall of the card cage.
6. Replace the sixteen cover securing screws.
7. Fold the connector ribbon over the card cage cover and reconnect to its housing on the **A3** MPU assembly. See Figure 5-6.
8. Replace and secure the shield.
9. Replace and secure the side panels, handle, and top panel.
10. Replace and secure the four plastic feet.

Removing the power supply and MPU assemblies

This section will enable you to remove and replace the HP 8133A power supply assemblies, and to remove and replace the **A3** MPU assembly.

Removing the rear panel

1. Remove the top and left panels and the shield, if not already done, as described on page **1-4.**
2. Remove the rear panel securing screws and remove the rear panel.

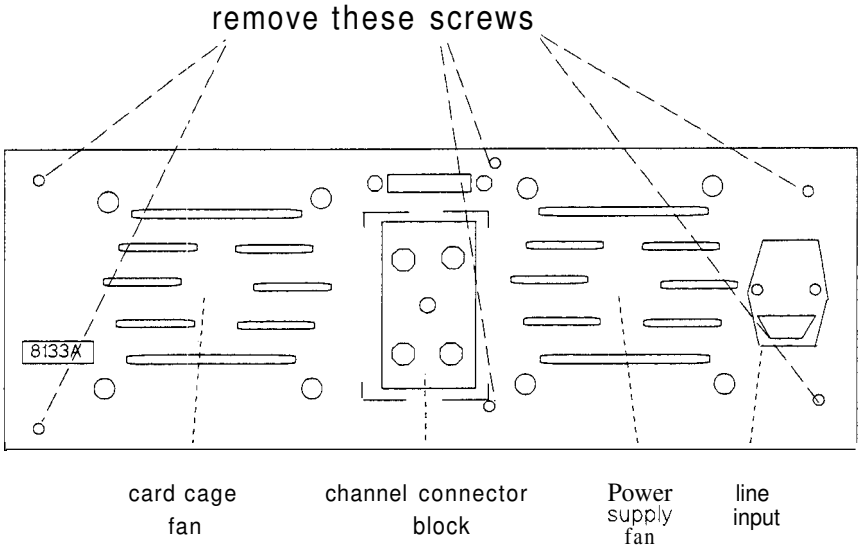


Figure **5-18.** Rear panel removal

1. If necessary, disconnect from the **A3** assembly the ribbon which lays across the left rear edge of the card cage cover.
2. If necessary uncouple the connector located at 521 on the **A3** assembly.

Removing the A3 MPU assembly and the A4 power control assembly

1. Free the **A3** from the power supply unit by removing the six screws located in the **six** metal pillars on the **A3** assembly and uncoupling the connection at location 521 on the **A3** assembly then pull the assembly back and lift it clear.
2. Turn the whole power supply unit upside down in order to access the **A4** and **A14** power supply assemblies. The **A4** assembly is the small assembly which stands vertically and slots into the large **A14** assembly.
3. Lift the **A4** assembly from the **A14** assembly. There are pin connectors between these two assemblies, located at each side of the bottom edge of the **A4** assembly, which need easing apart.

Note

There is a black plastic slot on the cage wall which the edge of the **A4** card must fit into when being relocated.

Removing the power supply cage and line switch

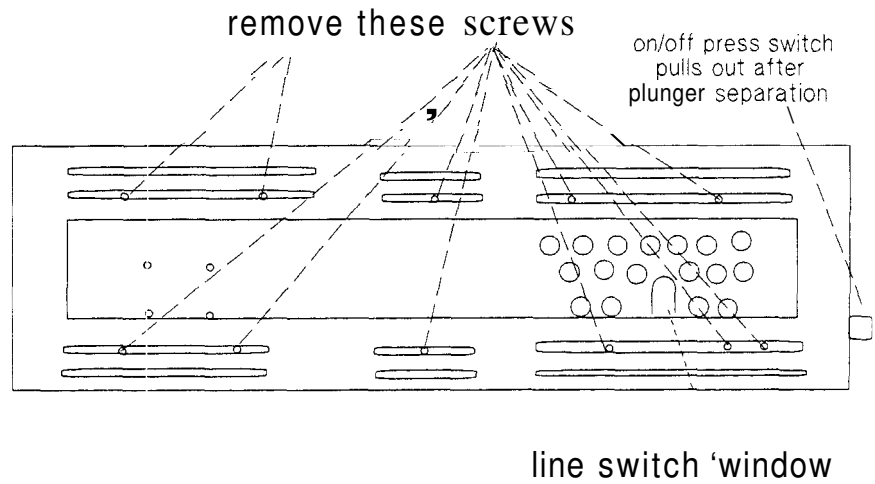


Figure 5-19. Line switch and power supply *cage* removal

1. Remove the screws detailed in figure 5-18.
2. Remove the line switch by first ensuring that the switch is in the OFF position and then prising the switch shaft free from the switch plunger. Do this with a flat bladed screwdriver inserted into the window in the left chassis wall.
3. This separates the on-off press switch from the plunger unit inside the cage. The switch can be pulled out at the frontpanel.
4. The line switch plunger unit can be removed after it has been disconnected from the line input filter, see "Disconnecting the line filter" and "Removing the line switch plunger unit" in this chapter.
5. If necessary, remove the A1 keyboard assembly and frontpanel, see Figure 1-7.
6. Remove the power supply unit from the chassis by holding the top edge of the fan window at the rear of the unit, and lifting the rear of the unit slightly and pulling it to the rear in order to free the pin connector between the power supply assemblies and the A12 motherboard.
7. The front of the power supply cage can then be lifted up at an angle and taken out of the chassis ***over the top*** of the front frame, *not* through the frontframe.

Removing the A12 motherboard

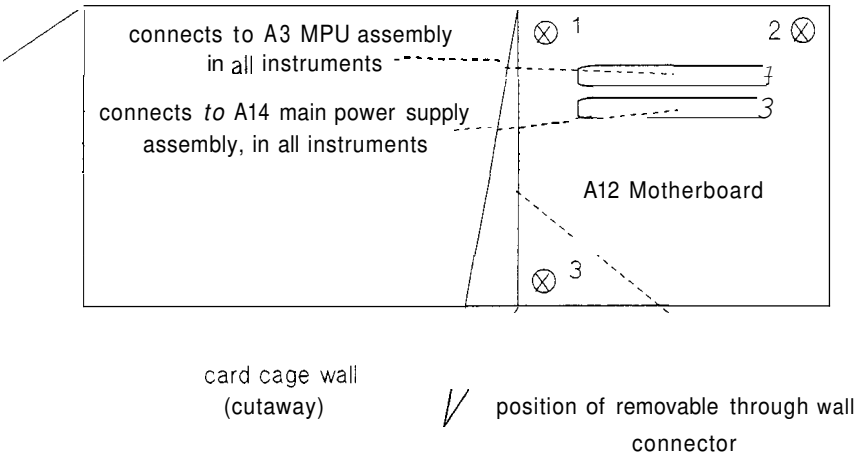


Figure 5-20. A12 Motherboard removal

1. The **A2** and **A12** assemblies together form the Motherboard, the assemblies are connected through the card cage wall by a pin connector. This connector is removable.
2. Remove screws 1 to **4,** shown in Figure **5-20.** The **A12** motherboard can then be freed of its through wall connector and lifted out.
3. Remove the **A2** and **A12** pin connector by unscrewing its four securing screws and lifting it out.

Disconnecting the A14 main power assembly

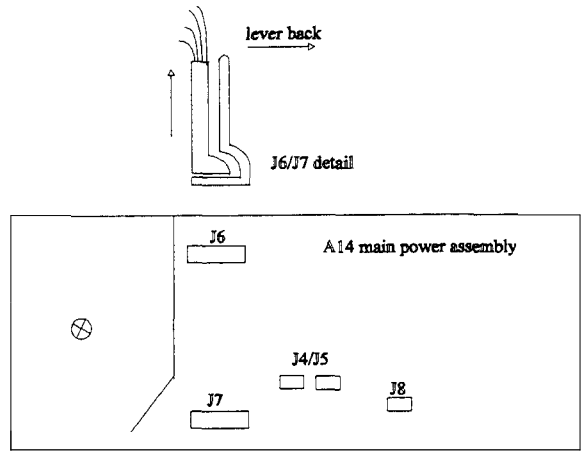


Figure 5-21. J6 and J7 location and removal

1. Make sure that the location of each connector is noted and that each connector is reconnected to the *same* location on reassembly.
2. Uncouple the connections at locations J4 and J5; J6 and 57; J8 on the **A14** assembly BEFORE removing any other assemblies.
3. If the connector block at location J6 cannot be removed leave it until the transformer has been removed, allowing easier access.

Caution 

Carefully lever back the retaining walls of the 56/57 housings with a flat-bladed screwdriver. Do not lever the retainers back too **far.**

Removing the fan and line filter assembly

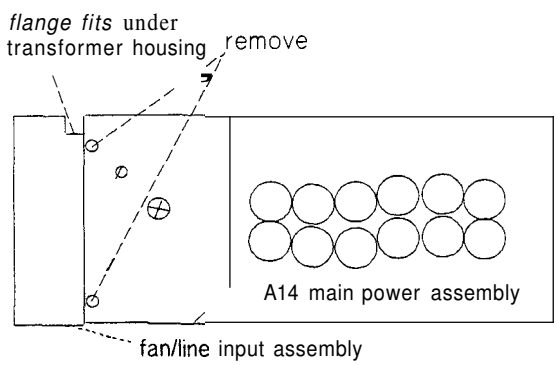


Figure 5-22. Fan assembly securing screws A14 side

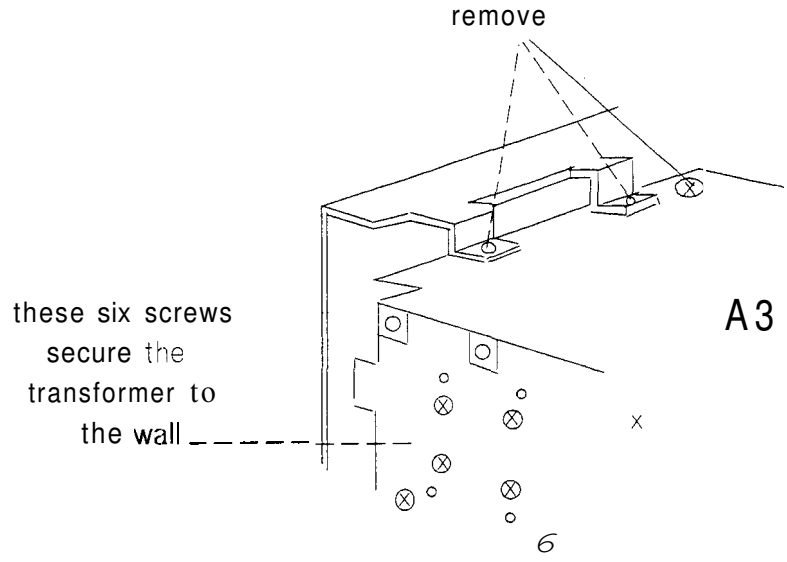


Figure 5-23. Fan assembly securing screws A3 side

1. First separate the unit from the transformer housing (**A14** assembly uppermost) by removing the two screws at the rear of the transformer housing. Notice that the flange of the fan housing locates under the edge of the transformer housing and must be replaced in this position.
2. Next turn the cage so that the **A3** side is uppermost and remove the two screws which secure the fan housing to the cage. Notice that the flanges on this side of the fan housing locate over the cage floor and must be refitted in this position.
3. Remove the larger screw located next one of the fan housing flanges. This frees the foot **of** the transformer housing from the cage floor.
4. Ease the fan unit back about two inches.
5. The fan itself can now be removed by unscrewing its four securing screws on the rear of the housing and sliding the fan out sideways. Note the route of its black and red cable.

Disconnecting the line filter

1. A number of wires which run from the line input filter to the transformer and the line switch are now exposed. Uncouple these connections before separating the line input filter and the transformer assembly.
2. Notice that a yellow and green wire earths the transformer to the assembly housing, but does not connect on the line input filter.
3. Figure **5-24** shows the face of the line input filter, which is only directly accessible after disconnection has taken place. After separating the **fan** housing **from** the transformer housing **look** at the line input filter from the left side, when looking from the rear of the instrument. locate the white wire from c to d in order to orientate yourself to the position of the other wires.

Table 5-2. Line Filter Connections

connection	color	connects to	soldered
a	white/dark grey	line switch	no
b	yellow/green	housing	yes
c	white	d	yes
d	white	line switch	yes
e	grey	line switch	no
f	red/black	transformer	no
g	green/black	transformer	no
h	brown/grey/white	line switch	no
i	red/white/grey	line switch	no
j	yellow/black	transformer	no
k	black	transformer	no
l	orange	transformer	no

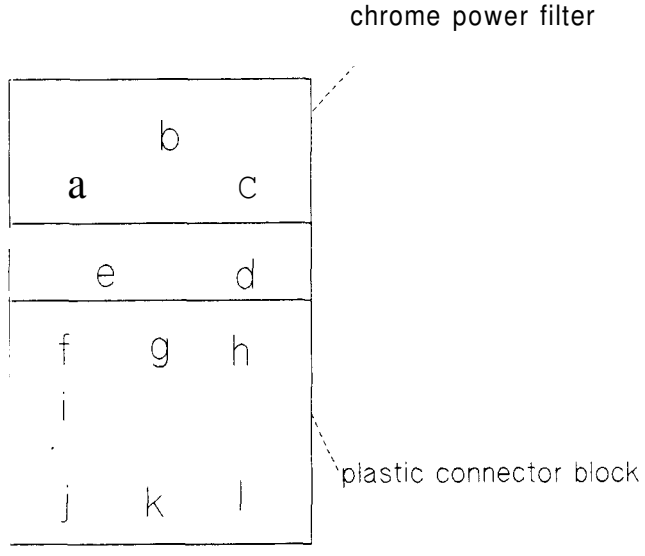


Figure 5-24. Line input filter and transformer connections.

Warning

These connections must be made to the *same* locations on reassembly.

4. If the holder for the line filter needs to be separated entirely from the unit housing its two retaining rivets must be drilled out.

Removing the line switch plunger unit

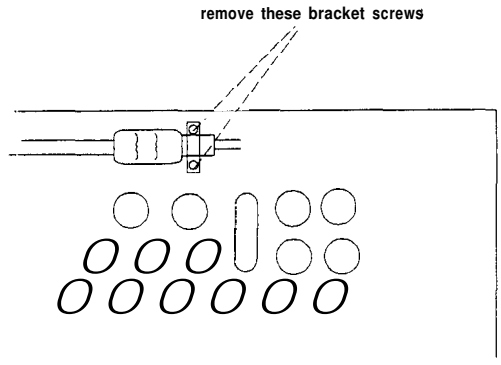


Figure 5-25. Line switch plunger unit securing bracket

1. Ensure that all line switch plunger unit connections have been disconnected from the line input filter.
2. Notice that the black plastic plunger unit *must* be replaced with the same face against the power supply cage wall.
3. Remove the line switch securing bracket in order to completely remove the line switch assembly, see Figure **5-25.**

Removing the transformer assembly

1. Unsolder the green transformer earth wire on the fan assembly housing.
2. Ensure that the transformer to line filter and **A14** main power assembly connections are uncoupled.
3. Remove the six screws which secure the transformer unit to the cage wall. If the large screw which secures the transformer housing on the **A3** assembly side **is** still in position, remove it. See Figure **5-23.**

Caution

Hold or otherwise support the transformer unit during removal to avoid its weight damaging components on the **A14** assembly.

4. Remove the transformer from its cover by unscrewing the largest screw on top of the cover and lifting the transformer out.
5. On reassembly ensure that the transformer locating pin Figure **5-26** fits into its correct location.

Removing the A14 main power assembly

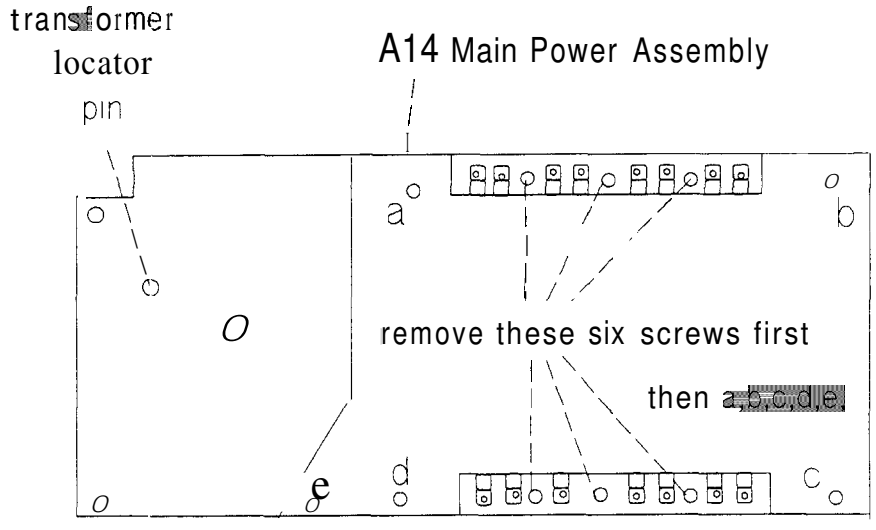


Figure 5-26. A14 securing screws

1. Free the **A14** assembly by removing the screws shown in Figure Figure 5-26 The assembly then lifts out to the left.

Reassembly

Reassembly of the power supply is the reverse of disassembly.

6

Replaceable Parts

The following lists detail replaceable parts for the HP 8133A and options 001, 002 and *003*.

HP 8133A Replaceable Parts List

Table 6-1. Standard Replaceable Parts List

Ref	HP Part #	CD	Qty	Description	Man'f	Part #
A1	08133-66501	6	1	BD AY KEY STD	28480	38133-66501
A2	08133-66502	7	1	BD AY MOTHC	28480	08133-66502
A3	08133-66503	8	1	BD AY UPCR	28480	08133-66503
A4	08133-66504	9	1	BD AY PWR CTL	28480	08133-66504
A7	08133-66507	2	1	BD AY WIDTH CHAN	28480	08133-66507
A14	08133-66514	1	1	BD AY PWR MAIN	28480	08133-66514
A15	08133-66545	8	1	BD AY TIMBID STD	28480	08133-66545
B1	08131-68502	9	0	FAN ASSY	28480	08131-68502
B2	08131-68502	9	0	FAN ASSY	28480	18131-68502
F1	2110-0029	0	1	FUSE 3A 250V	04703	313 003
F2	2110-0304	4	1	FUSE 1.5A 250V	02805	MDX-1-1/2A
MP1	5021-5837	2	1	STRUT CRNR 497.8	28480	5021-5837
MP2	5021-5837	2	1	STRUT CRNR 497.8	28480	5021-5837
MP3	5021-5837	2	1	STRUT CRNR 497.8	28480	5021-5837
MP4	5021-5837	2	1	STRUT CRNR 497.8	28480	5021-5837
MP5	5021-5804	3	1	FRAME REAR 132.6	28480	5021-5804
MP6	5021-8403	4	1	FRAME FRNT 132.2	28480	5021-8403
MP7	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP8	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP9	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP10	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP11	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP12	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP13	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP14	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP15	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP16	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP17	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP18	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP19	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP20	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP21	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP22	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP23	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP24	0515-1331	5	1	SCR-MTRC SPCLY	01125	

Table 6-1.
Standard Replaceable Parts List (continued)

Ref	HP Part #	CD	Qty	Description	Man'f	Part #
MP25	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP26	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP27	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP28	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP29	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP30	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP31	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP32	0515-1331	5	1	SCR-MTRC SPCLY	01125	
MP33	0515-1114	2	1	SCR-MACH M4X0.7	01125	
MP34	0515-1114	2	1	SCR-MACH M4X0.7	01125	
MP40	5001-0539	9	1	SIDE TRIM	28480	5001-0539
MP41	5001-0539	9	1	SIDE TRIM	28480	5001-0539
MP42	5041-8802	9	1	TRIM STRIP TOP	28480	5041-8802
MP49	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP50	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP51	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP52	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP53	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP54	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP55	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP56	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP57	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP58	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP59	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP60	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP61	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP62	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP63	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP64	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP65	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP66	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP67	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP68	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP69	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP70	0515-0898	7	1	SCR-MACH M4X0.7	09908	

Table 6-1. Standard Replaceable Parts List (continued)

Ref	HP Part #	CD	Qty	Description	Man'f	Part #
MP71	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP72	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP73	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP74	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP75	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP76	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP77	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP78	0515-0898	7	1	SCR-MACH M4X0.7	09908	
MP85	08131-60110	9	1	CAGE AY PWR	28480	38131-60110
MP88	0400-0018	0	1	GROM-CHAN	01963	G-51H-A
T1	9100-4949	7	1	XFMR-PWR	12949	
MP98	0460-0616	0	1	TAPE-INDL .5IN	04726	3568
MP99	08131-05402	6	1	INSULATOR,BOTTOM	28480	38131-05402
MP100	08131-01212	8	1	BRKT FAN	28480	08131-01212
MP101	0515-0890	9	1	SCR-MACH M3X0.5	09908	
MP102	0515-0890	9	1	SCR-MACH M3X0.5	09908	
MP103	0515-0890	9	1	SCR-MACH M3X0.5	09908	
MP104	0515-0890	9	1	SCR-MACH M3X0.5	09908	
MP105	0515-1173	3	1	SCR-MACH M6X1.0	09908	
MP112	0624-0267	5	1	SCR-TPG 6-20	05115	
MP113	0624-0267	5	1	SCR-TPG 6-20	05115	
MP114	0624-0267	5	1	SCR-TPG 6-20	05115	
MP115	0624-0267	5	1	SCR-TPG 6-20	05115	
MP116	0624-0267	5	1	SCR-TPG 6-20	05115	
MP117	0624-0267	5	1	SCR-TPG 6-20	05115	
MP118	0624-0267	5	1	SCR-TPG 6-20	05115	
MP119	0624-0267	5	1	SCR-TPG 6-20	05115	
MP120	1535-5036	8	1	3EM	28480	1535-5036
MP121	1535-5036	8	1	3EM	28480	.535-5036
MP122	1535-5036	8	1	OEM	28480	.535-5036
MP123	1535-5036	8	1	3EM	28480	.535-5036
MP124	1535-5036	8	1	OEM	28480	.535-5036
MP125	1535-5036	8	1	3EM	28480	.535-5036
MP126	1535-5036	8	1	OEM	28480	.535-5036
MP127	1535-5036	8	1	3EM	28480	.535-5036

Table 6-1. Standard Replaceable Parts List (continued)

Ref	HP Part #	CD	Qty	Description	Man'f	Part #
MP128	5001-1235	4	1	SPACER	28480	5001-1235
MP129	5001-1235	4	1	SPACER	28480	5001-1235
MP130	5001-1235	4	1	SPACER	28480	5001-1235
MP131	5001-1235	4	1	SPACER	28480	5001-1235
MP132	5001-1235	4	1	SPACER	28480	5001-1235
MP133	5001-1235	4	1	SPACER	28480	5001-1235
MP134	5001-1235	4	1	SPACER	28480	5001-1235
MP135	5001-1235	4	1	SPACER	28480	5001-1235
MP136	0400-0002	2	1	GROM-RND	04604	1656
MP137	0400-0002	2	1	GROM-RND	04604	1656
MP138	0400-0002	2	1	GROM-RND	04604	1656
MP139	0400-0002	2	1	GROM-RND	04604	1656
MP140	0400-0002	2	1	GROM-RND	04604	1656
MP141	0400-0002	2	1	GROM-RND	04604	1656
MP142	0400-0002	2	1	GROM-RND	04604	1656
MP143	0400-0002	2	1	GROM-RND	04604	1656
MP144	0515-1110	8	1	SCR-MACH M3X0.5	01125	
MP145	0515-1110	8	1	SCR-MACH M3X0.5	01125	
MP146	0515-1110	8	1	SCR-MACH M3X0.5	01125	
MP147	0515-1110	8	1	SCR-MACH M3X0.5	01125	
MP148	0515-1110	8	1	SCR-MACH M3X0.5	01125	
MP149	0515-1110	8	1	SCR-MACH M3X0.5	01125	
MP150	0515-1110	8	1	SCR-MACH M3X0.5	01125	
MP151	0515-1110	8	1	SCR-MACH M3X0.5	01125	
MP154	08131-00111	4	1	ANGLE PWR	28480	38131-00111
MP155	08131-44301	6	1	LBL CAUTION	28480	38131-44301
MP156	0515-1110	8	1	SCR-MACH M3X0.5	01125	
MP157	0515-1110	8	1	SCR-MACH M3X0.5	01125	
MP158	0515.1110	8	1	SCR-MACH M3X0.5	01125	
MP159	0515.1110	8	1	SCR-MACH M3X0.5	01125	
MP160	0515-1110	8	1	SCR-MACH M3X0.5	01125	
MP161	0515-1110	8	1	SCR-MACH M3X0.5	01125	
MP162	0515-1112	0	1	SCR-MACH M3X0.5	01125	
MP163	0515-1112	0	1	SCR-MACH M3X0.5	01125	
MP164	0515-1112	0	1	SCR-MACH M3X0.5	01125	

Table 6-1. Standard Replaceable Parts List (continued)

Ref	HP Part #	CD	Qty	Description	Man'f	Part #
MP165	0515-1112	0	1	SCR-MACH M3X0.5	01125	
MP166	0515-1112	0	1	SCR-MACH M3X0.5	01125	
MP167	0515-1112	0	1	SCR-MACH M3X0.5	01125	
MP175	0403-0374	7	1	BMPR FT-ADH MTG	28480	0403-0374
MP176	0403-0374	7	1	BMPR FT-ADH MTG	28480	0403-0374
MP177	0403-0374	7	1	BMPR FT-ADH MTG	28480	0403-0374
MP178	0403-0374	7	1	BMPR FT-ADH MTG	28480	0403-0374
MP179	3101-2992	2	1	SW-PB DPDT NO	04486	
MP180	0890-0196	2	1	TBG-HS .75 IN-D	02145	PVC
MP181	0890-0346	4	1	TUBING-FLEX	04726	3003-CLR
MP182	5040-9319	3	1	SHAFT PWR SWITCH	28480	5040-9319
MP183	08180-47401	2	1	KEY CAP	28480	08180-47401
MP184	3050-0066	8	1	WSHR-FL MTLC	04604	1451
MP185	3050-0066	8	1	WSHR-FL MTLC	04604	1451
MP186	3050-0066	8	1	WSHR-FL MTLC	04604	1451
MP187	3050-0066	8	1	WSHR-FL MTLC	04604	1451
MP188	3050-0066	8	1	WSHR-FL MTLC	04604	1451
MP189	3050-0066	8	1	WSHR-FL MTLC	04604	1451
MP190	3050-0066	8	1	WSHR-FL MTLC	04604	1451
MP191	3050-0066	8	1	WSHR-FL MTLC	04604	1451
MP192	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP193	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP194	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP195	0515-0886	3	1	SCR-MACH M3XO.5	09908	
MP196	0515-0886	3	1	SCR-MACH M3XO.5	09908	
MP197	0515-0886	3	1	SCR-MACH M3XO.5	09908	
MP198	0515-0886	3	1	SCR-MACH M3XO.5	09908	
MP199	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP200	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP201	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP202	0515-0886	3	1	SCR-MACH M3XO.5	09908	
MP203	0515-0886	3	1	SCR-MACH M3XO.5	09908	
MP204	0515-0886	3	1	SCR-MACH M3XO.5	09908	
MP205	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP206	0515-0886	3	1	SCR-MACH M3X0.5	09908	

Table 6-1.
Standard Replaceable Parts List (continued)

Ref	HP Part #	CD	Qty	Description	Man'f	Part #
MP207	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP208	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP209	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP210	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP211	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP212	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP213	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP214	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP215	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP216	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP217	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP218	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP219	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP220	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP221	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP222	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP223	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP224	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP225	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP226	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP227	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP228	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP229	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP230	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP231	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP232	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP233	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP234	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP235	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP236	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP237	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP238	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP239	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP240	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP241	0515-0886	3	1	SCR-MACH M3X0.5	09908	

Table 6-1.
Standard Replaceable Parts List (continued)

Ref	HP Part #	CD	Qty	Description	Man'f	Part #
MP242	0515-1232	5	1	SCR-MACH	01125	
MP243	0515-1232	5	1	SCR-MACH	01125	
MP244	0515-1232	5	1	SCR-MACH	01125	
MP245	0515-1232	5	1	SCR-MACH	01125	
MP246	0515-1232	5	1	SCR-MACH	01125	
MP247	0515-1232	5	1	SCR-MACH	01125	
MP248	0515-1232	5	1	SCR-MACH	01125	
MP249	0515-1232	5	1	SCR-MACH	01125	
MP250	0515-1232	5	1	SCR-MACH	01125	
MP251	0515-1232	5	1	SCR-MACH	01125	
MP252	0515-1232	5	1	SCR-MACH	01125	
MP253	0515-1232	5	1	SCR-MACH	01125	
MP254	0515-1232	5	1	SCR-MACH	01125	
MP255	0515-1232	5	1	SCR-MACH	01125	
MP256	0515-1232	5	1	SCR-MACH	01125	
MP257	0515-1508	8	1	SCR-MACH M3XO.5	01125	
MP258	0515-1508	8	1	SCR-MACH M3X0.5	01125	
MP259	0515-1508	8	1	SCR-MACH M3X0.5	01125	
MP260	0515-1508	8	1	SCR-MACH M3X0.5	01125	
MP261	0515-1508	8	1	SCR-MACH M3X0.5	01125	
MP262	0515-1508	8	1	SCR-MACH M3X0.5	01125	
MP263	0515-1508	8	1	SCR-MACH M3X0.5	01125	
MP264	0515-1508	8	1	SCR-MACH M3X0.5	01125	
MP265	0515-1508	8	1	SCR-MACH M3X0.5	01125	
MP266	0515-1508	8	1	SCR-MACH M3X0.5	01125	
MP267	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP268	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP269	0515-0886	3	1	SCR-MACH M3X0.5	09908	
MP275	3050-0891	7	1	WASHER-FL MTLC	06691	
MP276	3050-0891	7	1	WASHER-FL MTLC	06691	
MP277	3050-0891	7	1	WASHER-FL MTLC	06691	
MP278	3050-0891	7	1	WASHER-FL MTLC	06691	
MP279	3050-0891	7	1	WASHER-FL MTLC	06691	
MP280	3050-0891	7	1	WASHER-FL MTLC	06691	
MP298	2190-0073	2	1	WSHR-LK HLCL	04939	

Table 6-1. Standard Replaceable Parts List (continued)

Ref	HP Part #	CD	Qty	Description	Man'f	Part #
MP299	2190-0073	2	1	WSHR-LK HLCL	04939	
MP310	9320-5334	2	1	LBL-LNE-PTR	12236	
MP410	08131-04102	1	1	CVR TOP CABINET	28480	38131-04102
MP430	08131-04103	2	1	COVER TOP	28480	38131-04103
MP431	0403-0285	9	1	BMPR FT-ADH MTG	04726	SJ-5018 GRAY
MP432	0403-0285	9	1	BMPR FT-ADH MTG	04726	SJ-5018 GRAY
MP433	0403-0285	9	1	BMPR FT-ADH MTG	04726	SJ-5018 GRAY
MP451	0515-0897	6	1	SCR-MACH M3X0.5	09908	
MP452	0515-0897	6	1	SCR-MACH M3X0.5	09908	
MP453	0515-0897	6	1	SCR-MACH M3X0.5	09908	
MP454	0515-0897	6	1	SCR-MACH M3X0.5	09908	
MP455	0515-0897	6	1	SCR-MACH M3X0.5	09908	
MP456	0515-0897	6	1	SCR-MACH M3X0.5	09908	
MP457	0515-0897	6	1	SCR-MACH M3X0.5	09908	
MP458	0515-0897	6	1	SCR-MACH M3X0.5	09908	
MP459	0515-0897	6	1	SCR-MACH M3X0.5	09908	
MP460	0515-0897	6	1	SCR-MACH M3X0.5	09908	
MP490	5062-3747	5	1	CVR BOTTOM 497.8	28480	5062-3747
MP491	5041-8801	8	1	FOOT	28480	5041-8801
MP492	5041-8801	8	1	FOOT	28480	5041-8801
MP493	5041-8801	8	1	FOOT	28480	5041-8801
MP494	5041-8801	8	1	FOOT	28480	5041-8801
MP495	1460-1345	5	1	TILT STAND	00359	
MP496	1460-1345	5	1	TILT STAND	00359	
MP510	5062-3812	5	1	COVER SIDE PERF	28480	5062-3812
MP530	5062-3837	4	1	COVER SIDE PERF	28480	5062-3837
MP531	0515-1132	4	1	SCR-MACH M5X0.8	09908	
MP532	0515-1132	4	1	SCR-MACH M5X0.8	09908	
MP533	5041-8819	8	1	STP HNDL FRNT	28480	5041-8819
MP534	5041-8820	1	1	STP HNDL REAR	28480	5041-8820
MP535	5062-3704	4	1	STRAP HNDL 497.8	28480	5062-3704
MP550	5180-2471	0	1	HP-IB-ASSY	28480	5 8012471
MP551	0380-0643	3	1	STDF-HEX .255-IN	02685	
MP552	0380-0643	3	1	STDF-HEX .255-IN	02685	
MP555	8120-1689	7	3.5000	CA-ASSY	08674	

Table 6-1. Standard Replaceable Parts List (continued)

Ref	HP Part #	CD	Qty	Description	Man'f	Part #
MP606	0363-0125	0	1	RFI STRP-FINGERS	03647	97-555
MP607	0363-0125	0	1	RFI STRP-FINGERS	03647	97-555
MP608	0363-0125	0	1	RFI STRP-FINGERS	03647	97-555
MP609	0363-0170	5	1	RFI STRP-FINGERS	03647	0097-0520-02
MP610	08133-04107	8	1	BOARD-KEEPER	28480	08133-04107
MP611	08133-04107	8	1	BOARD-KEEPER	28480	08133-04107
MP612	08133-62701	0	1	FILTER ASSY 34P	28480	08133-62701
MP614	1401-0202	7	1	CAP-PROT STR	11040	.234-5
MP615	1401-0202	7	1	CAP-PROT STR	11040	.234-5
MP616	1401-0202	7	1	CAP-PROT STR	11040	.234-5
MP617	1401-0202	7	1	CAP-PROT STR	11040	.234-5
MP620	5040-0478	7	1	SLEEVE-BLUE	28480	5040-0478
MP621	5040-0478	7	1	SLEEVE-BLUE	28480	5040-0478
MP622	5041-8821	2	1	FOOT REAR	28480	5041-8821
MP623	5041-8821	2	1	FOOT REAR	28480	5041-8821
MP624	5041-8821	2	1	FOOT REAR	28480	5041-8821
MP625	5041-8821	2	1	FOOT REAR	28480	5041-8821
MP630	6960-0006	8	5	PLUG-HOLE	04213	D-2587-LCS
MP631	6960-0006	8	1	PLUG-HOLE	04213	D-2587-LCS
MP632	6960-0006	8	1	PLUG-HOLE	04213	D-2587-LCS
MP633	0515-1124	4	1	SCR-MACH M3X0.5	01125	
MP634	0515-1124	4	1	SCR-MACH M3XO.5	01125	
MP635	0515-1124	4	1	SCR-MACH M3XO.5	01125	
MP636	0515-1124	4	1	SCR-MACH M3XO.5	01125	
MP637	0515-1124	4	1	SCR-MACH M3X0.5	01125	
MP638	0515-1124	4	1	SCR-MACH M3X0.5	01125	
MP640	08133-23701	8	1	SEAL CC-SPOILER	28480	08133-23701
MP641	08133-23702	9	1	SEAL II CARD-CAG	28480	08133-23702
MP642	08133-00101	4	1	CHASSIS-MAIN	28480	08133-00101
MP643	E2900-00610	4	1	SHIELD CRT	28480	E2900-00610
MP644	08133-00202	6	1	SUB-PANEL	28480	08133-00202
MP645	08133-00203	7	1	REAR-PANEL	28480	08133-00203
MP646	08133-24702	1	1	REAR_SUPPORT	28480	08133-24702
MP647	08133-40204	2	1	PNL F'RNT STD	28480	08133-40204
MP648	08133-64101	8	1	COVER-TOP CARD-C	28480	08133-64101

Table 6-1. Standard Replaceable Parts List (continued)

Ref	HP Part #	CD	Qty	Description	Man'f	Part#
MP649	08133-64501	2	1	CARD-CAGE	28480	08133-64501
MP650	9211-6119	2	1	CTN-CORR RSC	06137	
MP651	9220-4582	8	1	PAD-FOAM	12506	
MP652	9220-4582	8	1	PAD-FOAM	12506	
MP653	9220-4583	9	1	PAD-FOAM	12506	
MP654	9220-45133	9	1	PAD-FOAM	12506	
MP655	7250-0042	8	1	HARDWOOD	12256	
MP656	5040-9383	1	1	PAD CORRUGATED	28480	5040-9383
MP657	9220-0556	8	1	PAD-FOAM	06292	PWL
MP658	9223-0514	4	4	TAPE-INDL 80MM	07036	OPTIMAL S
MP659	9230-0028	0	1	ENVELOPE-PKG-LST	05250	
MP660	5021-2840	1	1	KEY-LOCK-FOOT	28480	5021-2840
MP661	5021-2840	1	1	KEY-LOCK-FOOT	28480	5021-2840
W107	08133-61607	3	1	CBL AY CHA1-FRP	28480	08133-61607
W108	08133-61608	4	1	CBL AY CHA1-FRP	28480	08133-61608
W114	08133-61614	2	1	CBL AY TIM-TRIG0	28480	08133-61614
W117	08133-61617	2	1	CBL AY JUM_STD	28480	0813361617
W119	08133-61619	7	1	CBL AY EXTIN-TIM	28480	08133-61619

HP 8133A Option 001 Replaceable Parts List

Ref	HP Part #	CD	Qty	Description	Man'f	Part #
A15	08133-66555	0	1	BD AY TIMBID 001	28480	08133-66555
W118	08133-61618	6	1	CBL AY JUM-OPT	28480	08133-61618

HP 8133A Option 002 Replaceable Parts List

Table 6-3. Replaceable Parts List, Option 002

Ref	HP Part #	CD	Qty	Description	Man'f	Part #
A1	08133-66521	0	1	BD AY KEY 2CH	28480	08133-66521
A6	08133-66506	1	1	BD AY DATA	28480	08133-66506
A15	08133-66535	6	1	BD AY TIMBID 002	28480	08133-66535
MP700	08133-40201	9	1	FRNT PNL #002	28480	08133-40201
MP705	1401-0202	7	3	CAP-PROT STR	11040	.234-5
W103	08133-61603	9	1	CBL AY STSTP	28480	08133-61603
W106	08133-61606	2	1	CBL AY CHA2-FR	28480	08133-61606
W109	08133-61609	5	1	CBL AY CHA2-FRP	28480	08133-61609
W118	08133-61618	6	2	CBL AY JUM-OPT	28480	08133-61618

HP 8133A Option 003 Replaceable Parts List

Ref	HP Part #	CD	Qty	Description	Man'f	Part #
A1	08133-66521	0	1	BD AY KEY 2CH	28480	08133-66521
A7	08133-66507	2	1	BD AY WIDTH CHAN	28480	08133-66507
A15	08133-66535	6	1	BD AY TIMBID 002	28480	08133-66535
MP700	08133-40202	0	1	PNL FRNT #003	28480	08133-40202
MP705	1401-0202	7	2	CAP-PROTSTR	11040	.234-5
W106	08133-61606	2	1	CBL AY CHA2-FR	28480	08133-61606
W109	08133-61609	5	1	CBL AY CHA2-FRP	28480	08133-61609
W118	08133-61618	6	2	CBL AY JUM-OPT	28480	08133-61618

HP 8133A Exchange Parts List

Ref	HP Part #	Description	Used
A6	08133-69506	Data Board (**BD** AY DATA)	Option 002
A7	08133-69507	Width Board (BD AY WIDTH)	All (2 in Option 003)
A15	08133-69535	Timing Board (BD AY TIMING)	Options 002, 003
	08133-69545	Timing Board (**BD** AY TIMING)	Standard
	08133-69555	Timing Board (**BD AY** TIMING)	Option 001

7

Theory of Operation

This chapter contains the following information:

- Overview of the HP 8133A Pulse Generator
- Description of each of the blocks that comprise the HP 8133A Pulse Generator:
  - The Microprocessor (CPU) Board
  - The Tinning Board
  - The Width Board
  - The Data Board & PLL
  - The Power Supply Unit

Overview

The following diagram shows the main functional blocks of the HP 8133A Pulse Generator:

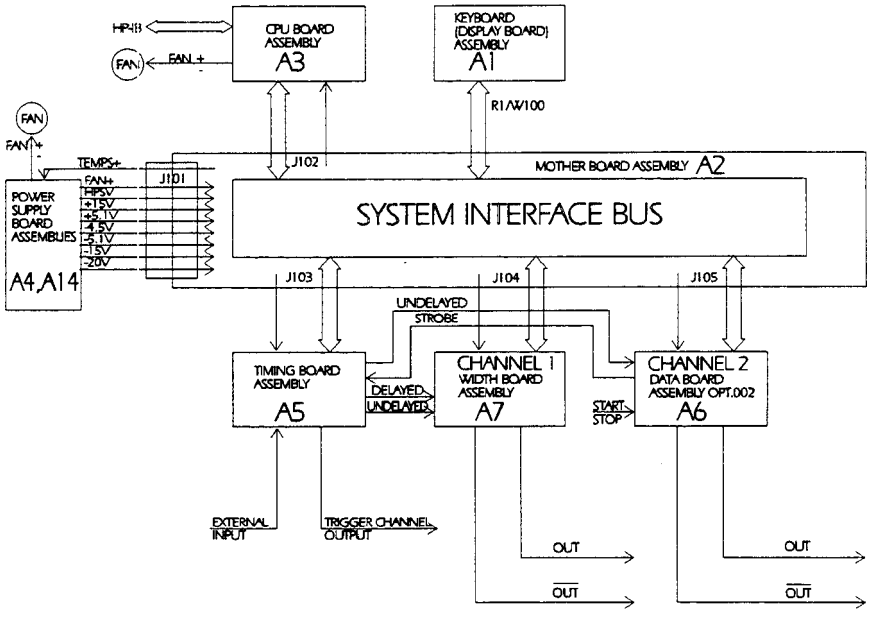


Figure 7-1. Block Diagram of the HP 8133A Pulse Generator

The functional blocks of the HP 8133A Pulse Generator communicate internally through a System Interface bus, and externally through

the HP-IB interface. Commands are input through the keyboard, and status is viewed on the displays. The blocks comprising the HP 81338 Pulse Generator are described briefly in the following paragraphs, and then in greater detail in the next section.

The functional blocks in the HP 8133A Pulse Generator have been given identifying numbers. These numbers appear on the overall block diagram, and again on the block diagram on each block when it is illustrated in the detailed description, making identification easier.

Microprocessor (CPU) - A3

The Microprocessor controls timing and sequencing within the system, sending commands on the System interface bus and the HP - IB interface, and receiving information from the front panel controls. It provides visual status information on the display unit mounted on the front panel. The Keyboard and the Display Board might be considered functional blocks in their own right, but as they are closely associated with the Microprocessor Board, they are described in that section, and not in this overview. See "Keyboard Controller - 3C" and "Display Control - 3C".

The Microprocessor also provides power to the units cooling fan when the temperature inside the instrument becomes excessive.

Timing Board - A5

The Timing Board can be considered as the heart of the instrument, generating waveforms at various frequencies, both direct and, and delayed, for processing by the Width Board (A7), before being made available at the output of the HP 8133A Pulse Generator as Channel 1.

The waveforms are generated by a stable YIG oscillator, but an external source can be connected and used if required.

An output can also be provided as Channel 2 by the inclusion of the optional Data Board (A6), or by using option 003.

The timing circuitry also provides a trigger channel output for synchronizing external equipment.

Width Board - A7

The Width Board gets its input from the Timing Board and varies the width of the output signal by two means:

- By a variable width circuit
- By a switched width circuit

Together, these width controllers provide the total range of widths that can be applied to the output waveform. A pulse formatter and output amplifier condition the signal before it is passed to the HP 8133A Pulse Generator output.

The Width Board provides switchable inverted and non-inverted outputs.

Data Board - A6 (Optional)

This board, when fitted, provides an output in data form. A multiplexer converts the signal from the Timing Board to data and provides a signal for synchronizing the data. This signal represents the pulse output signal, divided by 4.

The data gate array provides the 32:4 Multiplexed Data as well as the PRBS Data, RZ (Return to Zero) and NRZ (Non-Return to Zero) formatting is done by the Multiplexer. A wide range PLL (Phase-locked Loop) keeps the data gate array and the multiplexer synchronized.

The Data function is started and stopped by controlling the data gate array.

The Data Board provides switchable inverted and non-inverted outputs.

Power Supply Unit - A4, A14

The HP 8133A Pulse Generator power supply is an analog series regulator. Its main features are:

- Primary 4-voltage tapping transformer
- Additional secondary tapping transformer
- Schottky power rectifiers
- Power MOSFETs with low resistance when on.

The Power Supply Unit consists of three functional blocks:

- Power input that includes a 50/60 Hz transformer
- Power main board
- Power control board.

Power Input

This block is responsible for:

- Filtering the line voltage
- Fusing
- Selection
- On/off switching
- Transforming the primary voltages to secondary voltage levels.

Power Main Board

This block provides:

- Rectification
- Filtering
- Series regulation of all secondary voltages and their transmission to the motherboard
- Generation of the voltage and current sensing signals
- Generation of the control power +UB and its transmission to the control board
- The fan control circuit
- The power. on reset circuit which generates the HPSV signal to reset the MPU.

Power Control Board

This board contains the regulators. The power main board supplies this board with:

- The control power +UB
- The voltage and current sensing signals.

It is responsible for :

- Generating the required reference voltages and gate control signals. This enables the power main board to carry out voltage regulation (with foldback current limiting) and selection of secondary winding taps.
- Supplying the reference current for the fan control circuit on the power main board.

Power Outputs

The power supply provides the following outputs:

- -4.5 V, 3.5 A
- -5.1 V, 2.5 A
- +5.1 V, 2.7 **A**
- -15 V, 1.1 A
- +15 V, 1.8 A
- -20 V, 1.0 **A**
- fan(+) & (-)voltages
- HPSV (High Power Supply Valid): This is a signal for the Microprocessor indicating that the Power Supply is stable (Power Fail Detection)
  - >4.35 V, 1.16mA at +5.1 V > 4.85 V
  - <0.40 V, 0.05 mA at +5.1 V < 4.85 V

Microprocessor Board (CPU)

The following figure shows a block diagram of the microprocessor board:

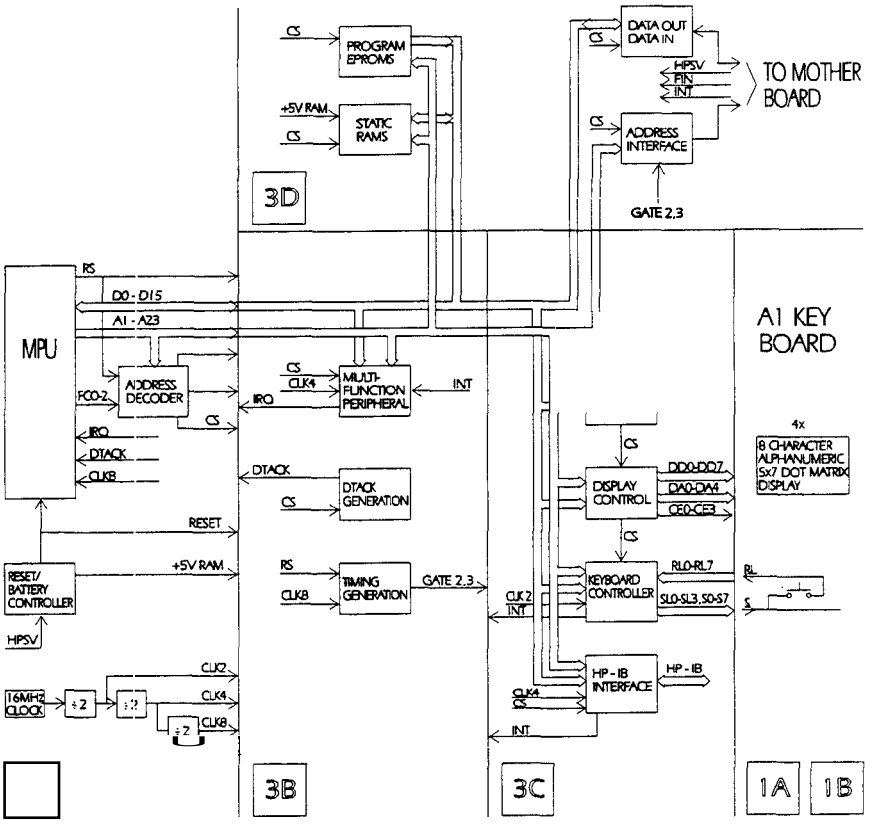


Figure 7-2.
Functional Block Diagram of the CPU and the Keyboard and Display Board

The HP 8133A Microprocessor board is built around a 68000 microprocessor running at 8 MHz. An MFP (multi-functional peripheral) is used for interrupt control, generation of a 20 ms clock interrupt, and for serial I/O (called **LAB-10).** The firmware is stored in two **64** KByte (128 KByte) EPROMs. The RAM consists of two 32 KByte **(64** KByte) battery buffered static CMOS RAMs. Other circuits on the Microprocessor board include a keyboard/display controller, an HP-IB controller and a gate array which is used as a frequency counter. The device bus is a secondary bus system which controls the hardware on the signal boards.

Microprocessor Interface

The microprocessor interface is uncomplicated. There is no buffering of the address, data and control bus, because there are only a few devices connected to it. All address and data lines have a 10 kohms pull up resistor to keep them at a defined level when the bus is in high impedance state.

The RST and HLT signals are driven by the Microprocessor control circuit, as described in "Reset **and** Battery Backup - 3A.

The DTACK generation is described in "DTACK Generation - 3B".

The interrupt line IPLI is driven by the MFP as described in "Multi-Functional Peripheral - 3B". The microprocessor lines BR, BG, BGACK, IPLO, E, VPA and VMA are unused and are tied to +5.1V, or left open.

Clock Generation - 3A

The master clock is generated by an integrated quartz oscillator running at 16 MHz. The 16 MHz signal is divided by three D-type flip flops to 8,4 and 2 MHz, which are used to clock the various circuits, as follows:

- The 8 MHz signal (CLK8,NCLK8) is used to clock the microprocessor (U1) and the device bus timing generation circuit. It is also used as the frequency reference for the frequency counter gate array (U37)
- The 4 MHz signal (CLK4) is used to clock the MFP (U21) and the HP-IB controller (U19)
- The 2 MHz signal (CLK2) is used to clock the keyboard/display controller (U24)

Address Decoding - 3A

Address Range	Chip Select line	Valid Data bits	Wait States
0x000000 ... 0x03ffff	LCSEPROM	D0 ... D15	0 or 1
0x040000 ... 0x07ffff	LCSMFP	D0 ... D7	4 - 10
0x080000 ... 0x0bffff	LCSKEYB	D0 ... D7	4
0x0c0000 ... 0x0fffff	LCSHPIB	D0 ... D7	1
0x100000 ... 0x13ffff	LCSFC	D0 ... D7	0
0x140000 ... 0x17ffff	LCSDB	D0 ... D7	9
Ox180000 ... Oxlbffff	LCSDISP	D0 ... D7	0
0x1c0000 ... Oxlfffff	LCSRAM	D0 ... D15	0

In conjunction with RD/WR, UDS and LDS a number of additional signals are generated. These are described in table 7-2:

Table 7-2. Other address decode signals

signal name	derived from
LCSEPROML	LCSEPROM+LDS
LCSEPROMU	LCSEPROM+UDS
LCSRAML	LCSRAM+LDS
LCSRAMU	LCSRAM+UDS
LLDWRITE	RD/WR+LDS
LUDWRITE	RD/WR+UDS
LLDREAD	(not RD/WR)+LDS
LUDREAD	(notDR/WR)+UDS
HLDREAD	(not(notRD/WR)+LDS)
LIACK	AS+(not(FOC.FC1.Fc2))

Device Bus Timing and Wait State Generation - 3B

The wait state signals and the signals GATE2 and GATE3 are generated by two D-type flip flops (U35) and the 8 bit shift register (U5).

The outputs of the shift register are also used to generate wait states (to delay the DTACK generation by a number of clock cycles when OR'ed with the appropriate chip select lines). Table 3 shows the number of wait states that can be achieved by the various signals. Table 1 shows how many wait states are generated for the various address ranges. One wait cycle equals one clock period (125 ns). A μP read or write cycle without any wait states takes four clock cycles (500ns).

Signal	number of wait states
not 2Q of U36	1
not QA of U5	2
not QB of US	3
not QC of US	4
not QD of US	5
not QE of US	6
not QF of US	7
not QG of U5	8
not QH of U5	9

DTACK Generation - 3B

The DTACK generation is not complex. U6A, U6B and U33B are connected together as an AND gate with eight inputs. The chip select signals (listed in table 1) are fed into this AND gate either directly (i.e. with zero wait states), or OR'ed with one of the wait state signals (listed in tables 3 and 1). For the MFP, the DTACK signal (U21, pin 46) is used instead of the chip select line.

RAM - 3D The RAM circuits U10 (data bits DO-D7) and U11 (data bits D8-D15) are battery-backed to be non-volatile. When the supply voltage drops below 4.65 V the RAM circuits are supplied by a lithium battery, and the CE lines of the RAMs are pulled high.

Currently, 32 KByte RAMs are fitted.

ROM - 3D The firmware is stored in two EPROMs (U12 for data bits DO-D7 and U13 for data bits D8-D15). The IC sockets are suitable for 32 KByte and 128 KByte ROMs.

Currently, 128 KByte ROMs are fitted. The wait states for U12 and U13 can be selected with jumper J8 to be either zero or one.

Multi-Functional Peripheral - 3B

For a detailed description of the MFP refer to *M6800 Family Reference Motorola Inc. 1989.*

In the HP8133A the MFP is clocked with a 4 MHz signal. It is used as interrupt controller, timing generator and for serial I/O (LAB-10). These three functions are explained in the following subsections:

- Interrupt Control and LAB/DIAG Jumpers
- Timing Generation
- LAB.IO

Interrupt control and LAB/DIAG jumpers

All interrupt sources (HPIB, keyboard controller, device bus request) and the DIAG and LAB jumpers are connected to the I/O lines of the MFP. The IRQ line of the MFP is used tp drive the processor's IPL1 line. All I/O lines of the MFP are configured as input lines. Table 7-4 shows the assignment. Note that the interrupt line from the keyboard controller (HKBDIRQ) is active-high.

MFP Pin	signal name	0	1
17	LPF	power fail	
16	LHPIBIRQ	HPIB interrupt	
16	LBDBRQ	device bus request	
14	-unused-		
13	-unused-		
12	HKBDIRQ		keyboard interrupt
11	DUG jumper	DUG	NORM
LO	LAB jumper	LAB	NORM

Timing generation

Two of the MFP timers (D and B) are used to generate a periodic interrupt every 20 ms. This is necessary for the operating system pSOS, on which the firmware is based. Timer B is internally connected to the MFP clock (4 MHz). Its prescaler is programmed to a value of 100; its counter to a value of 20. This results in a frequency of 1 kHz on the output timer D (TDO). TDO is connected to the output timer B (TDI) which operates in event count mode. As the counter

value of timer B is 20, there is a timeout every 20 ms. Every time timer B times out, it generates an interrupt.

LAB_IO

Timer C is internally connected to the MFP clock (4 MHz). Its output TCO is connected to RC and TC and serves as a clock source for the serial interface. Timer C prescaler is programmed to a value of 4. Its counter is programmed to a value of 52. This results in an output frequency of 9615.4 kHz on the output of timer C (TCO). The serial interface is configured to operate at this frequency. This is sufficiently close to 9600 baud, at which rate the terminal is configured.

The SI and SO signals of the MFP axe level-shifted by an RS232 transceiver (U26), and connected to jumper J3. U26 and the capacitors CP4-CP7 are fitted in prototype boards only.

Device Bus Interface - 3D

The device bus interface is a bi-directional parallel interface with long (> 125 ns) setup and hold times. The cycle time for a device bus access is 13μP clock cycles (1.625 μs) Figures 2 and 3 show a read and write cycle on the device bus. The output buffers for device bus Address and Data are ACT gates, Which can sink or source up to 70 mA. This is necessary to drive the filter capacitors on the motherboard.

A latch (U32) is used to latch the μP address bus and generate the device bus addresses and card selects. U27, U28 and U33 are used to connect the device data bus to the μP data bus.

HP-IB Interface - 3C

The HP-IB controller provides the HP-IB interface. Interface lines are buffered by two drivers. For a detailed description refer to the *TMS 9914 Data Sheet.*

Keyboard Controller - 3C

The front panel keys and LEDs are connected by the integrated keyboard/display controller. This is operated at a clock frequency of 2 MHz. The internal prescaler is programmed to a value of 20, resulting in a scan rate close to 1 kHz. The scan lines SLO-SL3 are buffered with an HCT gate (U20A). The signal lines AO-A3 and BO-B3 are buffered with an ALS gate (U25) because they drive the LEDs on the front panel directly.

Display Control - 3C

The HPSP display modules on the keyboard are connected to the μP bus on the motherboard via two latches (U38 and U39). These are used to buffer the address and data bus. A demultiplexer (U29A) generates the chip select and write signals for the display Modules.

Frequency Counter - 3C

The gate array FACE is used as the frequency counter. The frequency signal from the timing board is fed directly into the FVFC pin of the gate array. The reference clock is 8 MHZ.

Serial I/O See **LAB-10.**

Reset and Battery Backup - 3A

The reset generation and battery backup is controlled by the μP control circuit U15. When the +5.1V supply voltage is lower than 4.65V (see *MAX691 Data Sheet)* the RESET line (U15, Pin 15) is low and keeps the microprocessor and the other circuits in a define state. The two RAM ICs and the OR-gate U7 (which drives the chip select lines of the RAMs) are supplied from Vout (U15, Pin 2) which in turn is supplied from the backup battery. When the supply voltage exceeds 4.65V the BATT_ON signal (U15, Pin 5) goes low and turns on transistor Q1 which connects the +5.1V supply to the +5VRAM. After approximately 50 ms the RESET line goes high and releases the microprocessor from the reset state.

Signal Description

The following table lists **and** describes the microprocessor signals:

Signal description

signal name	active	description
+5.1VIN		+5.1V supply from mother board. This is before the filter network
+5.1V		+5.1V supply after the filter network. This is used as supply for all circuits on the IP board except the RAMs (U10 & U11) and U7.
+5VRAM		Battery buffered supply voltage for the RAM ICs (U10 & U11) and U7.
A1 ... A23	high	Microprocessor address bus
D0 ... D15	high	Microprocessor data bus
AS	low	Microprocessor AS (address strobe) line. A low signal indicates valid address.
BERR	low	Microprocessor BERR (bus error) line.
CLK16	high	16MHz clock signal, generated by the master oscillator.
CLK8	high	8 MHz clock signal, derived from CLK16.
NCLK8	high	8 MHz clock signal, inverted CLK8.
CLK4	high	4 MHz clock signal, derived from CLK8.
CLK2	high	2 MHz clock signal, derived from CLK4.
DCOM, GND		Common ground
DTACK	low	DTACK of the microprocessor. A low signal indicates, that the current read/write cycle is complete.
HLDREAD	high	Low Data Read. A high signal indicates, that the lower half of the data bus is valid.
HLT	low	HLT of the microprocessor. A low signal halts the microprocessor.
HPSV	high	Power fail. With a high signal the power supply indicates, that power is about to go down.
HRSET	high	Inverted RESET line. Reset signal for the keyboard controller.
IRQ	low	Interrupt line. Pulled low by MFP when an interrupt condition occurs.
LCSDB	low	Chip select device bus

Signal description (continued)

signal name	active	description
LCSDISP	low	Chip select display modules
LCSEPROM	low	Chip select EPROM
LCSEPROML	low	Chip select EPROM low. A low signal indicates, that the lower EPROM (U12) is selected
LCSEPROMH	low	Chip select EPROM high. A low signal indicates, that the upper EPROM (U13) is selected
LCSFC	low	Chip select frequency counter
LCSHPIB	low	Chip select HP-IB controller
LCSKEYB	low	Chip select keyboard control
LCSMFP	low	Chip select MFP
LCSRAM	low	Chip select RAM
LCSRAML	low	Chip select RAM low. A low signal indicates, that the lower RAM (U10) is selected
LCSRAMH	low	Chip select RAM high. A low signal indicates, that the upper RAM (U11) is selected
LDS	low	Microprocessor LDS (low data strobe) line. A low signal indicates, that the lower half of the data bus is valid.
LIACK	low	Low interrupt acknowledge. A low signal indicate: an interrupt acknowledge cycle
LLDREAS	low	Lower data read. A low signal indicated a read cycle on the lower half of the data bus
LLDWRITE	low	Lower data write. A low signal indicated a write cycle on the lower half of the data bus
LPF	low	Power fail. This line is pulled low by the reset controller, U15, to indicate power failure
LUDREAD	low	Upper data read. A low signal indicates a read cycle on the upper half of the data bus
LUDWRITE	low	Upper data write. A low signal indicates a write cycle on the upper half of the data bus
LWHR	both	Microprocessor RD/WR /read/write) line. A low signal indicates a writing cycle
UDS	low	Microprocessor UDS (upper data strobe) line. A low signal'indicates, that the upper half of the data bus is valid.

Signal description (continued)

signal name	active	description
GATE2	low	Timing signal for device bus access. The signal is low for 6 ìP clock periods (−760ns) during a device bus access. (see figures 2 and 3)
GATE3	low	Timing signal for device bus access. This signal is low for 4 ìP clock periods (−600 ns) during a device bus access. (see figures 2 and 3)
HKBDIRQ	high	Interrupt line from keyboard controller
LDBDRQ	low	Device bus request. This signal can be pulled low by each of the hardware boards (wire'd OR). It generates a ìP interrupt
LHPIBIRQ	low	Interrupt line from HP-IB controller
RESET	low	RESET signal for the microprocessor, keyboard controller, HP-IB controller and MFP.
CE0 ... CE3	low	Chip select and write signals for the display modules on the front panel
DA0 ... DA4	high	display module address lines A0 ... A4
DD0 ... DD7	high	display module data lines D0 ... D7
FIN	high	Input signal of frequency counter
FL	low	Flash input on display modules
KBA0 ... KBA3	high	Unbuffered output lines of keyboard controller
RL0 ... RL7	high	lines on keyboard controller
S0 ... S7	high	Buffer output lines of keyboard controller
SL0 ... SL3	high	Scan lines of keyboard controller
FAN+, FAN-		Power supply for rear panel fan.
HDA0 ... HDA5	high	Device bus address lines
HDBD0 ... HDBD	high	Device bus data lines
LCEN0 ... LCEN2	low	Device bus card enable lines. A low signal indicates, that the correspondent slot is selected
LDBRHW	both	Device bus read/write. A low signal indicates a read cycle, a high signal indicates a write cycle
LDBV	low	Device bus valid. A low signal indicates that the device bus address and data lines are valid

Address Map

The **following** table lists and describes the addresses used by the system:

Address Map

Address	R/W	Description	Function
000000 ... 03FFFF	r	2*EPROM 128KByte or 64KByte)	EPROM
040001		GPIP General Purpose I/O	
0400031	\ER Active Edge Register		
040006		DDR Data Direction Register	
040007		(ERA Interrupt Enable Register A	
040009		(ERB Interrupt Enable Register B	
04000B		(PRA Interrupt Pending Register A	
04000D		(PRB Interrupt Pending Register B	
04000F		ISRA Interrupt In-Service Register A	
040011		ISRB Interrupt In-Service Register B	
040013		[MRA Interrupt **Mask** Register A	
040016		[MRB Interrupt **Mask** Register B	
040017	r/w	VR Vector Register	MFP
040019		TACR Timer A Control Register	
04001B		TBCR Timer B Control Register	
04001D		TCDCR Timer C and D Control Register	
04001F		TADR Timer A Data Register	
040021		TBDR Timer B Data Register	
040023		TCDR Timer C Data Register	
040026		TDDR Timer D Data Register	
040027		SCR Synchronous Character Register	
040029		UCR USART Control Register	
04002B		RSR Receiver Status Register	
04002D		TSR Transmitter Status Register	
04002F		USART Data Register	
040030 ... 07FFFF	r/w	**not** used	

Address Map (continued)

Address	R/W	Description	Function
080001		Keyboard Data	Keyboard
080003	r/w	Keyboard Status/Control	Controller
080004 ... OBFFFF		not used	
0C0001		Int status 0	
0C0003		Int status 1	
0C0005		Address Status	
0C0007	r	Bus Status	
0C0009		-NC-	
0C000B		-NC-	
0C000D		Command Pass Thru	
0C000F		Data in	HP-IB
0C0001		Int Mask 0	Controller
0C0003		Int Mask 1	
0C0005		-NC-	
0C0007	w	Auxiliary Command	
0C0009		Address	
0C000B		Serial Poll	
0C000D		Parallel Poll	
0C000F		Data Out	
0C0010 ... 0FFFFF		not used	
100001	r/w	Data	Freq.
100003	w	Address	counter
100004 ... 13FFFF		not used	

Address Map (continued)

Address	R/W	Description	Function
140001			
140003			
...	r/w	Slot 0	
14007F			
140081			
1400133			Device
...	r/w	Slot 1	Bus
1400FF			
140101			
140103			
...	r/w	lot 2	
14017F			
140180			
...		nc ised	
180001			
180003			HDSP
...	w	Display Modules	Display
1801FF			
180200			
...		not used	
LBFFFF			
1C0000			
...	r/w	2*RAM 32 kByte	RAM
1CFFFF			
1D0000			
...		not used	
LFFFFF			
200000			
...		not used (copy of address 0 . . . 1FFFFF)	
FFFFFF			

Timing Board - A5

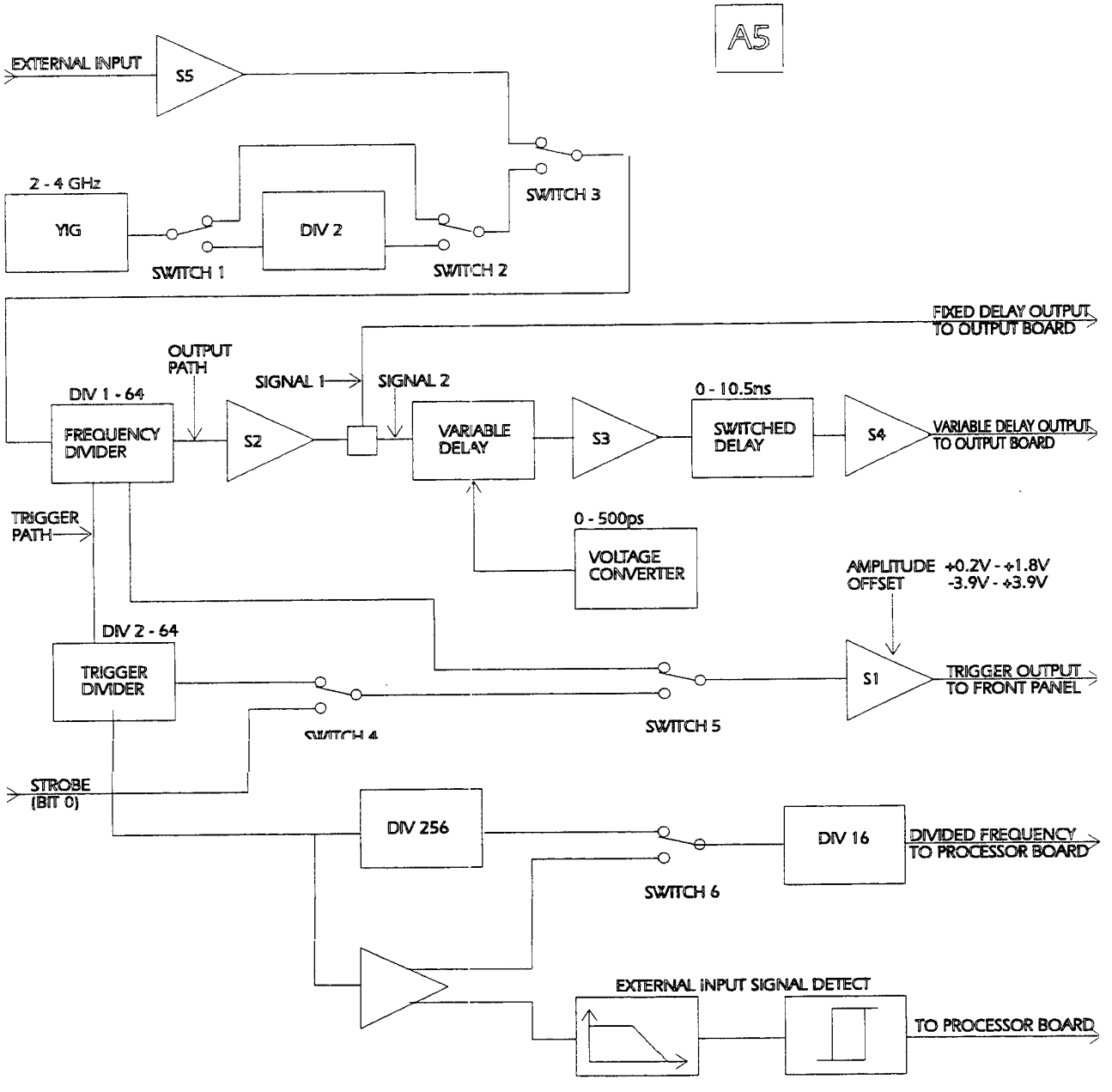


Figure 7-3. Functional Block Diagram of the Timing Board

YIG Oscillator

Timing is provided by a YIG oscillator, giving low jitter and high stability. The oscillator is programmable in the range: 2 GHz to 4 GHz. It is programmed by a 12 bit DAC, giving a period resolution of 1pS. A special reference ground plane on the pc board is provided for the circuit driving the YIG, to reduce noise and crosstalk. When the instrument is run below 2 GHz the signal of the YIG oscillator is divided by two. For output frequencies between 2GHz and 3GHz the divider is bypassed by 2 GaAs switches. The frequency divider is a bipolar ASIC with the following specifications:

Function	Specification
Input Frequency range	DC ... 3GHz
Dividing range	1, 2, 4, 8, 16, 32, 64
Output levels	ECL, differential
Input sensitivity	200mV pp single ended
or	100mV pp differential

The frequency divider provides a split output signal for the trigger path and the output path. An additional programmable divider is incorporated in the trigger path, providing division of 2, 4, 8, 16, 32 and 64. This provides a trigger for oscilloscopes that do not work up to 3GHz. It is preferable, however, to use an oscilloscope capable of being triggered at 3 GHz, as trigger performance is improved and jitter is reduced, allowing more accurate edge placement measurements. If the instrument runs in the data mode the trigger is synchronized to the data on the data board. In this mode the strobe signal from the data board is switched into the trigger path. The trigger output is conditioned by a shaping amplifier. This shaper is described in "Shaping Amplifier" The trigger output amplitude is programmable in the range 200mV to 1.8V, and offset in a -4V to +4V window. The programming resolution is 10mV. In the output path a second shaper is integrated to provide output amplitude of 2Vpp. The output signal is then split by a resistive divider into 2 signals. One signal goes directly the output board; the other is delayed in a delay block before going to the output board. The signals from the timing board to the output board are brought to the rear panel. There the signals are passed to the instrument through exchangeable links. This allows the delay between the channels to be varied by using cables of differing electrical length, thus avoiding the need for additional cable at the outputs of HP 8133A Pulse Generator, and preventing the introduction of distortion to the output waveforms.

Delay block

The delay block: consists of a variable delay, followed by a refresh amplifier, a switched delay, and an output shaping amplifier.

Variable Delay

The variable delay is a thickfilm hybrid. The delay is varied by the use of varactor diodes, each diode being capable of a variation in the range: 0.6pF and 2.1pF, by a voltage range of +1.5v and -36V.

Using automatic calibration by means of a DAC, a delay accuracy of ± 15ps is achieved across the whole delay and frequency range. A

shaping amplifier provides an output of 2Vpp at a transition time of better than 100ps.

Switched Delay

The switched delay is provided by GaAs switches fabricated in thinfilm. The different delays are achieved by switching between microstrip lines of differing length. The switches are fabricated on thin-film hybrids using GaAs switches. Resistors R1-R12 prevent distortion by compensating for the on-resistance of the GaAs switches. Compensation for insertion loss (typically 16dB at maximum delay) is provided **by** an amplifier having available gain in excess of 20dB.

The nominal electrical lengths of the delay lines are:

Table 7-6. Delay Line Nominal Lengths

Section	Nominal length
	222ps
	401ps
	748ps
	1421ps
	2727ps
	5261ps

By adding the delays, each variable between 0 and 222ps, a total delay of 0 to 11ns is produced. One channel of the HP 8133A Pulse Generator is delayed in this way by ±5ns (a total of 10ns delay) deskewing the two output channels to compensate for deviation in transmission times of the output boards.

Shaping Amplifier

The shaping amplifier is a four stage AC coupled GaAs FET discrete circuit with the following specifications:

Table 7-7. Shaping Amplifier Specifications

Function	Specification
Frequency range	10MHz to 3.5 GHz
Input Voltage range	0.2V. 2Vpp
Output amplitude	0.2V-2Vpp (adjustable)
Transmission times	better than 100ps

The amplifier works as follows: U901 determines the DC current I(FET) through R905 parallel R916 through L901, L913 and the FET Q901 itself by controlling the gate force voltage of the FET Q901. The current I(FET) is adjustable using RV901. For high frequencies C905 in parallel with C906 are shortcuts to ground and the inductors L913 and L901 have a very high impedance. Thus the input to each stage is terminated with 500 across the frequency range of the amplifier. The resistor at the gate of the FET prevents ringing and oscillations in the amplifier. The diodes CR901..CR903 protect the GaAs FET from damage when the power is switched on or off. They also protect the FET during a malfunction in the biasing circuit.

Frequency Counter

A frequency counter is incorporated in the HP 8133A Pulse Generator to provide the same precision of duty cycle, phase and delay for internal and external operating modes. A trigger divider works in the range: 10MHz to 3GHz. If the instrument runs without dividing the trigger, the trigger divider is bypassed and the trigger divider is programmed to divide by 64. When the trigger is divided by 2, 4, 8, 16, 32 or 64 the trigger signal goes through the trigger divider. Therefore, at the output of the trigger divider the maximum frequency is 1.5GHz (HP 8133A Pulse Generator runs at 3 GHz; the trigger is divided by two).

As the frequency counter works at frequencies down to 10 MHz at the external input, its range covers 150KHz (10MHz/64) to 1.5GHz (3GHz/2). Therefore the signal after the trigger divider runs through a dynamic divider. There, the signal is divided by 254. The signal is then converted to **TTL** level by a differential amplifier. One output of the amplifier feeds a low pass filter with a cutoff frequency of 15MHz. A schmitt trigger detects whether the frequency is below or above 15MHz, using its output to operate a switch, frequencies below 15MHz are routed through the differential amplifier, and frequencies above 15MHz are passed through the divider, where they are divided by 16 in a standard TTL divider and fed into the frequency counter on the microprocessor board. The frequency counter is an ASIC having the following key specifications:

Table 7-8. Frequency Counter Key Specifications

Function	Specification
Accuracy	better than 0.1%
Measurement time	300ms
Resolution	100KHz
Frequency range	2.0MHz-3.3GHz

Width Board - A7

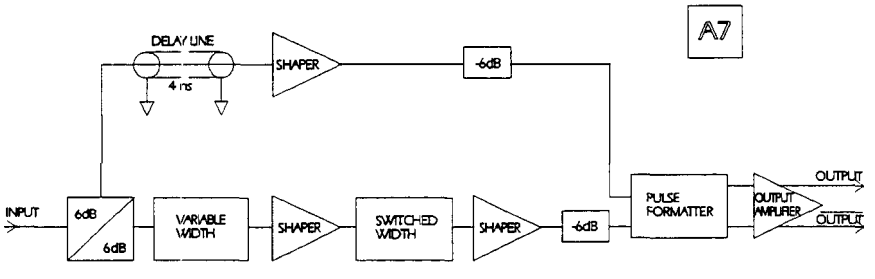


Figure 7-4. Functional Block Diagram of the Width Board

The delayed output signal of the Timing Board (single ended, squarewave) is the input signal to the Width Board. This board generates the variable pulse width and contains the Output Amplifier.

Variable Pulse Width Generation

The input signal is split into two signals. One of these signals is delayed by about 4ns with a fixed delay line (semi-rigid cable). The other signal is fed through a delay block that consists of two different hybrids (Variable Width Hybrid, Switched Width Hybrid) and two refresh amplifiers (Shaper Amplifier). The two hybrids and the refresh amplifiers are described in the section "Timing Board - A5". Thus, two signals with the same frequency are generated: One with a fixed delay of 4ns, the other one with a programmable delay of 4ns-14ns (4ns is the minimum delay of the delay block). In the pulse mode, the delay of the second signal is limited to 4ns plus actual period value by the instrument software.

The Pulseformatter

The delayed and undelayed signals are fed to the Pulseformatter. The Pulseformatter is a full-custom bipolar IC packaged on a thickfilm hybrid. It is a high-speed EXOR gate generating an output signal of a pulse width equal to the delay between the two input signals, at twice the input frequency. Initially, the frequency of the input signals is divided by two by an on-chip flip-flop, and they are now at the original frequency through the action of the EXOR gate. An additional EXOR gate gives a choice between Normal Mode and Complement Mode, depending on the control voltage at the appropriate input. The Pulseformatter can be switched between the Pulse Mode (Normal mode), described above, or the Complement Mode (Square Mode) by the control voltage.

In Square Mode, the input signal with the programmable delay is connected to the input of the Pulseformatter. Thus, the width capability can be switched off, producing an additional 0ns - 10ns delay capability instead. This is particularly useful in a Standard Instrument not fitted with the delay block on the Timing Board.

At switch-on the Pulseformatter always starts running in the Normal Mode (self-initialization). The Pulseformatter works from DC to 3.5GHz and can produce Pulse widths as narrow as 120ps or less. It has a fully differential output with a swing of 500mV and a typical transition time of approximately 80ps.

The Output Amplifier

The differential output of the Multiplexer provides the input signals to the Output Amplifier. Voltage and current sources, some of them programmable via the device bus interface, are used for biasing and programming the output amplitude and high level. Two voltage sources anti two current sources are programmable to adjust the pulse performance over frequency and temperature.

The amplifier consists of 2 identical, full-custom GaAs ICs packaged on a thickfilm hybrid. All voltage and current sources needed for the amplifier are located on the PC-Board and are decoupled by capacitors on the PC-board, in addition to printed bypass capacitors on the hybrid.

The ferrites F1 - F4 and the optional ferrites F5 and F6 reduce HF-ringing below 10GHz, improving output performance.

Data Board - A6

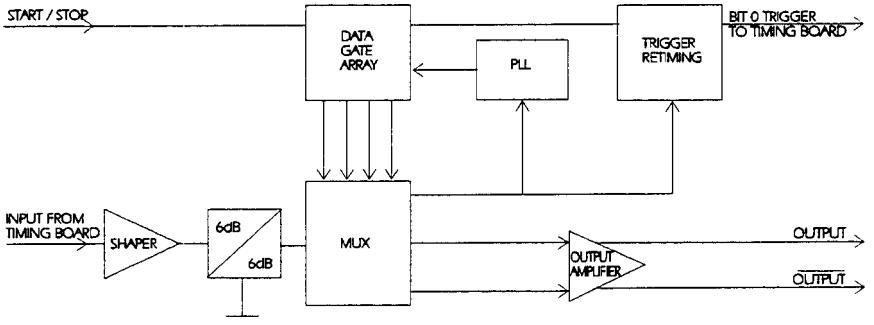


Figure 7-5.
Functional Block Diagram of the Data Board and the PLL

The undelayed output signal of the Timing Board (single ended, squarewave) is the input signal to the Data Board. This board converts the pulse train to digital data.

The Multiplexer:

The multiplexer is a 3 GHz ECL gatearray. Four differential CML inputs from the Data Gatearray are multiplexed to a differential ECL output in **RZ** (return to zero) and **NRZ** (= non return to zero) mode. Another output signal is the clock divided by 4 which is used to synchronize the four input data bits with the clock and for retiming the bitstream trigger signal (see data generator).

The AC coupled input requires a termination to the ECL threshold voltage. This termination voltage can also be shifted to the lower level when no valid signal is present in external clock mode. In this case the shaper is also switched off and the mode is set to **RZ.** So a static "0" is guaranteed at a data output.

The Data Generator:

An ECL gatearray generates the four bit data stream in the following modes:

***Datamode:**

32 static bits are multiplexed to **4** bits.

The Data mode has two additional modes: Burst and Single Burst These modes are only available via HP-IB commands.

***PRBS mode:**

An internal shift register generator provides a four bit data stream which is multiplexed to **a** 2^23 **-1** PRBS

The bitstream trigger signal is also generated in this gatearray. The memory clock (MEMCLK) signal is used for this purpose.

The PLL

A PLL is used to generate a negative delay to compensate for the long delay through the data generator and to ensure the right timing with respect to the multiplexer over the whole frequency range.

The phase detector is a digital phase and frequency sensitive ECL type with a maximum operation frequency of 80 MHz. It must have a range of 7 octaves.

The loop filter is a symmetrical low pass filter comprising an instrumentation amplifier and a PI (proportional integration) regulator. Gain switching of the filter is realized by varying the gain controlling resistors and a switchable double T attenuator.

The Output Amplifier

The differential output of the Multiplexer provides the input signals to the Output Amplifier. Voltage and current sources, some of them programmable via the device bus interface, are used for biasing and programming the output amplitude and high level. Two voltage sources and two current sources are programmable to adjust the pulse performance over frequency and temperature.

The amplifier consists of 2 identical, full-custom GaAs ICs packaged on a thickfilm hybrid. All voltage and current sources needed for the amplifier are located on the PC-Board and are decoupled by capacitors on the PC-board, in addition to printed bypass capacitors on the hybrid.

The ferrite:; F1 - F4 and the optional ferrites F5 and F6 reduce HF-ringing below 10GHz, improving output performance.

Bitstream Trigger Retiming

The retimirig which is done for the data bits in the multiplexer is also required for the bit 0 trigger signal, to avoid internal PLL jitter appearing at the output.

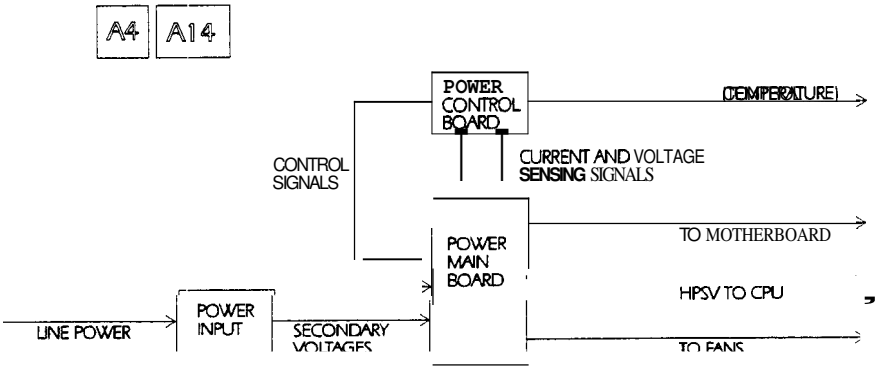


Figure 7-6.
Functional Block Diagram of the *HP* 8133A Pulse Generator Power Supplies

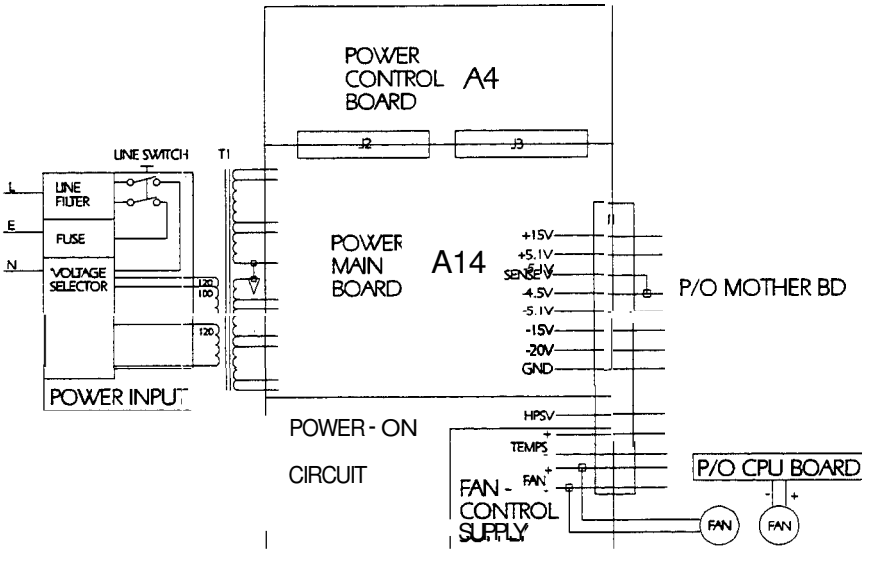


Figure 7-7.
Block Diagram of the Power Supplies Showing Power Connections

Power Input

The AC line voltage is applied to the power input module F1 which consists of

- A line filter for filtering RFI from the AC line voltage
- A line fuse F1
- A line voltage selector for 100/120/220/240 VAC operation.

The main on/off switch S1, isolates the input power from the voltage selector. Depending on the voltage selector setting, the primary windings of the transformer are connected in one of the following four modes:

1. 100V: the two 120V windings are connected in parallel, but power is supplied to the 100V tapping (A) - orange wire.
2. 120V the two 120V windings are connected in parallel and power is supplied to them (C), (D) - black, black-green wires.
3. 220V the two 120V windings are connected in series, but power is supplied to the 100V tapping (A) - orange wire.
4. 240V the two 120V windings are connected in series and power is supplied to (C)- black wire.

Caution

It is important to set the voltage selector according to the nominal Iine voltage supply. This is to prevent:

- Malfunction if the supply voltage is too low
- High power losses or blowing of fuse if the supply voltage is too high.

The transformer secondary windings are center tapped, and provide an additional high/low tapping for each of the four output voltage levels. They are all connected to the power main board.

Power Main Board

Regulation circuits are basically the same for all six output voltages, so only the +15 supply is described here.

+15 V Regulation

There are two complete regulation paths. They are applied together to:

- Have a common output at J1(31A,C;32A,C)
- Have a common control by feedback signals generated at R113
- Supply the power control board with:
- A voltage sensing signal +15 V fed to J3(14)-X3(14)
- A current sensing signal R+15 fed to J3(15)-X3(15)

The high tapping path is formed by:

- The Red 3 and Blue 3 wires of T1, J7(2,4)
- Schottky power diodes, CR101 and CR102, for full wave rectification
- Filtering capacitor C101
- Series voltage regulation via the power MOSFET Q101

The gate of Q101, is controlled by the voltage drop across R101, which is produced by controlling the current signal G+15H, from the power control board. Q101 is turned off when there is:

- No control current
- Control current producing a voltage drop below the gate threshold voltage.

The low tapping path acts in a similar manner with the following components:

- Red 4 and Blue 4 wires of T1,J7(1,3)
- CR103 and CR104
- c102
- Q102
- R102

The unregulated low tapping path voltage UL+ 15 is fed, via J3(6) and X3(6), to the power control board. The function of this path is to select which tapping path is activated (sometimes both). Line voltage tolerance, and t.o some degree the load state, determine which tapping path is activated.

Generally, the high tapping is activated at the line voltage that is below the nominal value, but still within tolerance. The low tapping is activated when the low voltage is below the nominal value, but still within tolerance. Both are active at around nominal line voltage. This keeps series regulator voltage drop and power losses as low as possible.

Control Power +UB

The high tapping AC voltage (from T1 wires Red 1 and Blue 1) is used by diodes CR123 and CR124 to generate +UB. This unregulated voltage is applied to the power control board via J3(19).

Power-on Reset

This circuit provides correct resetting of the MPU during power on, power off and fail, by:

- Monitoring the +5.1V output with U101
- Supplying the HPSV signal to the MPU via J1(3C).

The threshold voltage is approximately +4.85V at R119. If the +5.1V supply equals tlne threshold at power on, the reset signal is delayed for approximately 40ms by C120. HPSV then goes high (>4.35V). At power down, the signal change to low is not delayed.

Fan Control

The fan control circuit supplies voltage for the two fans. The value of this voltage is dependent on the temperature detected by the sensor mounted on the μP board. It is supplied by the unregulated low tapping voltages UL+ 15 and UL-15 and operates by current-flow to ground. The temperature sensor, U50, on the μP board is supplied with a current of approximately 1 mA from R123. It generates a voltage drop directly proportional to the absolute temperature value - 10 mV/K. This voltage is compared with the threshold voltage drop across R125, Which is supplied by a reference current of 1 mA from the control board.

Comparator U103A controls the output voltage of the power regulator U104. The control gain is set by feedback to (R126/R125 + 1). Thus, the threshold point is approximately 300°K (27°C) and its output voltage, approximately 14V, is determined by the voltage drop of VR103 and R125.

At temperatures below the threshold, the output voltage can not fall below (approximately) 13.3V and is determined by the sum of the voltage drop of VR103, U103A pins 1-4, CR125 and U104 pins 1 and 2. If the temperature exceeds the limit condition the output of U103A, pin 1 is decoupled by CR125. U out max is approximately 26.3 V.

Power Control Board

The Power control Board provides bias voltages, reference voltages and power control services:

Bias and Reference Voltages

The unregulated +UB voltage from J3 (19) is stabilized to +UBIAS by VRI, R66, Q15 and C15, this provides the bias for reference voltage generation, and some control circuits. By means of +UBIAS, U7 generates the reference voltage +5R, which is buffered by U8B, Q16 and C17. All other reference voltages are derived from +5R as follows:

1. -5R reference voltage is formed and buffed by U8A, R69, R70 and Q17.
2. Unregulated low tapping voltage UL-15 is stabilized by VR2, R72 and Q17 to the negative bias of U8A.
3. +10R reference voltage is formed by R67,R68 and U8D; it is buffed by C16.
4. The current source IREF is derived from the +10R reference by R71, U8C and Q18. The value of this current source 1mA and supplies the fan control circuit on the power main board.

Control Circuits

Most of the control circuits function in a similar way and the +15V control circuit is used as an example to describe all of them. The +5.1V and -3.23V control circuits are slightly different; these are described separately after the +15V control.

+15 V control

Voltage Control.

The voltage sensing feedback signal + 15V from J3(14) and X3(14), is divided and compared with reference voltage -5R by R9,R10 and U1B. If the voltage output goes high, the output voltage at U1B pin 7 also rises, taking more current via R6 than is injected by R4 at the node of emitters Q1 and Q2. This lower emmiter current lowers the gate control signals, G+15H and G+15L, at the collectors of Q1 and Q2, and thus to the output MOSFETS on the power main board. C2 provides frequency compensation to prevent oscillation.

High/Low Tapping Path Control.

Division of these two currents is controlled by the unregulated low tapping voltage UL+ 15 and the differential stage function of Q1, Q2, R1, R2, R3 and R5. If the line voltage is operating at low tolerance, Q2 conducts and only the high tapping path is activated and controlled; the low tapping path is switched off.. Around nominal line voltage both high and low tapping paths are activated because of the linear region operation of Q1 and Q2. This action is smoothed by C1

to damp ripple ,voltages. At high line voltage tolerance only Q1 is on and thus only the low tapping path is activated.

Foldback Current Limitation.

Feedback signal R+ 15 and + 15V represent the voltage drop of the output current sensing resistor. it is compared by U1A. It achieves control in a similar manner to voltage regulation, but limits the output current when active. Diodes CR1 and CR2 decouple operation during the most positive control voltage, therefore the limiting function is active.

When below the current limit, the voltage of U1a pin 1 is close to-5R, therefore CR2 is reverse biased and has no influence on voltage control. The foldback characteristic is achieved by lowering the threshold. As the output voltage decreases, so does the R+ 15 voltage in current limiting operation. At the output, the short circuit minimum foldback current limit is reached and R+ 15 is almost zero.

+5.1V Control

The output voltage of the operational amplifier U2 is buffered by Q6 and R19. The gate signals G+5H and G+5L are controlled by voltage, rather than current, via R17 and R18. Therefore at differential stage Q4/Q5 the transistor which is not conducting, is that corresponding to the active tapping path. At the same time the conducting transistor switches the other tapping path off. CR7 and CR8 lower the maximum output voltage, to prevent saturation of U2 at the highest gate voltage and conduction points. R73 prevents gate oscillation.

-4.5V Control

There is a separate voltage signal, -4.5VSENS, from the motherboard, that compensates for voltage drops of up to 0.1V. R34 in conjunction with the -4.5V signal prevents the output voltage rising more than approximately 0.1V if the -4.5VSENS line is open circuit.

8

Making adjustments to the HP 8133A Pulse Generator

All adjustments to the HP 8133A Pulse Generator are made under software control. The software is not supplied with the instrument. There are no user adjustments.

If the HP 8133A Pulse Generator needs recalibration, return the instrument to Hewlett Packard.

A

Component Level Information Package

The complete Component Level Information Package for the HP 8133A Pulse Generator **and** its options is not part of this Assembly-level Service Guide. It can be obtained seperately by ordering HP Part Number 08133-91031.

HEWLETT' PACKARD

Manual for Model Number	8133A
Manual printed on	May 1992
Manual Part Number	08133-91012

Make all ERRATA corrections.

Check the following table for your instrument serial prefix/serial number/EDC and make the listed changes to your manual

New Item

Serial Prefix or Serial Number	Manual Changes

ERRATA

(over)

ERRATA

On **page** 1-5, add

Mounting Hardware:

Front Handle Kit	P/N	5062-3989
Rack Mount Flange Kit		5062-3977
Front Handle & Flange Kit		5062-3983

HEWLETT' PACKARD

MANUAL CHANGES September, 1997

Manual for Model Number	8133A
Manual printed on	March 1994
	Edition 1.1 E0394
Manual Part Number	08133-91021

Make all ERRATA corrections.

Check the following table for your instrument serial prefix/serial number/EDC and make the listed changes to your manual

New Item

Serial Prefix or Serial Number	Manual Changes
ERRATA	
3318600451	1

ERRATA

On page **2-7** Operating:
add errata:
Altitude up to 2000m
Installation Category II
Pollution Degree 2
Warning: To prevent electrical shock, disconnect the HP model 8133A from mains before cleaning. Use a dry cloth or one slightly dampened with water to clean the external case parts. Do not attempt to clean internally.

! CHANGE TO NEW S E W NUMBER FORMAT !

last serial number old format:	3318600492
first serial number new format:	DE33500493

INDEX OF MANUAL CHANGE

MANUAL CHANGE / ERRATA	FRAME
1	MP300 MP620 MP621

MANUAL CHANGE 1

On Repl.Parts 6-9, Table 6-1 add:

MP300	7121-5584	CE-LABEL

On Repl.Parts 6-10, Table 6-1 change to read:

MP620,621	1400-0082	CLMP-CA