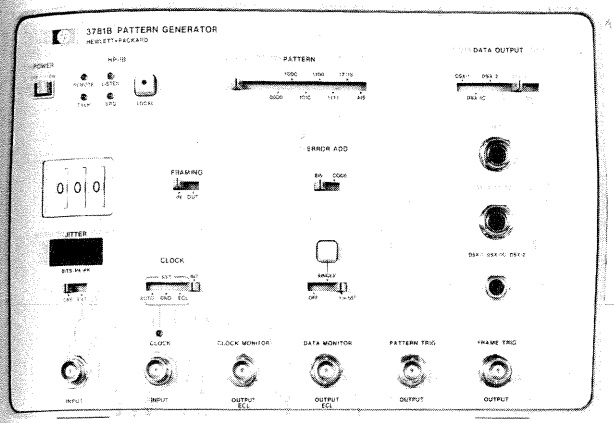
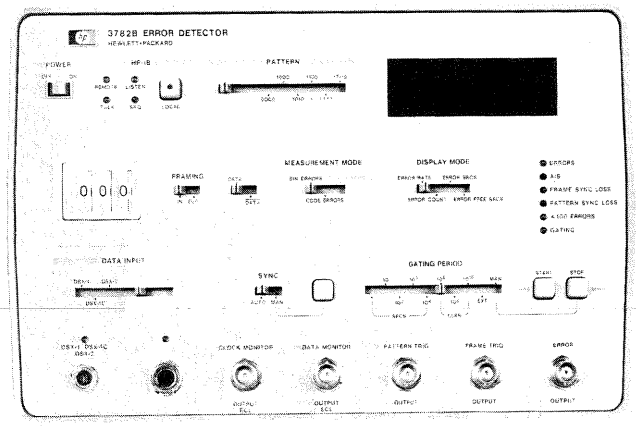
# Models 3781A, 3782A, 3781B, 3782B

3781A/B
- Versatile selection of test patterns
- Internal jitter modulation
- Additional delayed data output

3782A/B
- Binary and code error measurements
- Error ratio, error count, error seconds and error-free seconds displayed
- Powerful error distribution analysis




3781B




3782B

DESIGNED FOR HP-IB SYSTEMS

The 3781A Pattern Generator and 3782A Error Detector form a high performance error measuring system which complements the existing 3780A Pattern Generator/Error Detector. Designed to conform with CEPT and CCITT standards, the 3781A/3782A provide four bit rates (up to 50 Mb/s) of the digital hierarchy in one compact system. Applications of the system are in R&D, field trial and production testing, especially where an automatic and remote measurement capability via the HP-IB is required.

In the 3781A, binary or code errors can be injected as single shot or at $10^{-3}$ or $10^{-5}$ rates into a wide range of PRBS and 16-bit WORD test patterns coded in AMI or HDB3. The test patterns provided include standard $2^9-1$, $2^{15}-1$, and $2^{23}-1$ bit PRBS to CCITT Recommendations, fully programmable 16-bit WORD, and two 8-bit WORDS which may be alternated under the control of an external signal. Zero substitution (up to 120 zeros) for PRBS patterns is included to examine, for example, the clock recovery performance of regenerators. 75 Ω unbalanced and 120 Ω balanced pseudo-ternary outputs and binary TTL monitor outputs are provided. A jitter modulation input facility is provided for simple oscillator connection, with direct LED display of pk-pk bits of jitter. This can be used to measure the input jitter tolerance of digital transmission equipment. A second data output with 12 bits delay provides adequate simulation of an independent sequence for thorough testing of 4$\phi$PSK digital radio systems. As an option, four extra data outputs coded in AMI or HDB3 can be included on the rear panel for driving adjacent radio channels.

The 3782A detects binary or code errors which can be displayed in the form of error ratio, error count, error seconds, and error-free seconds over a wide choice of gating periods. All four results are computed simultaneously over the same gating period. For ease of use there is a built-in automatic check for compatibility of switch position combinations. An error code flashes on the display if incompatibility is detected. When the monitor mode is used, the 3782A can be used for in-service monitoring of digital transmission links.

Measurement results are available on the HP-IB and a rear panel result threshold switch allows pre-selection of an error threshold above which results will be printed. This provides useful data reduction and a first order error distribution analysis. With a built-in real-time clock, results can be output with time, if required.

## Ordering Information
3781A Pattern Generator
3782A Error Detector

The 3781B Pattern Generator and 3782B Error Detector form a dedicated error measurement system for testing and evaluating the performance of Bell digital transmission terminal and link equipment, up to and including the DS-3 level in the digital hierarchy. The 3781B/3782B can be used in production testing, field installation, and maintenance of the Bell digital transmission system, including PCM/TDM transmission over cable, radio, satellite, and fibre optic links. The principal application is at the DS-3 level in the Bell digital hierarchy.

The 3781B/3782B are designed to interface at Bell System standard cross connect points with appropriate ternary coding and interface voltage levels at each hierarchial level. Interfacing at the DS-1C and DS-2 levels is limited to T1-C and T2 line systems. At the DS-3 level, a choice of four data formats is available. Alternatively, binary ECL interfaces can be used.

The 3781B Pattern Generator provides a selection of standard $2^9-1$, $2^{15}-1$, and $2^{20}-1$ bit PRBS and fixed WORD test patterns with a choice of single error or 1 in $10^5$ error simulation on the digital data stream for normal measurements and troubleshooting. A pattern of 17 ones/15 zeros and zero substitution (up to 999 zeros) for PRBS patterns are included to examine phase sensitive circuitry such as clock recovery of regenerators. A jitter modulation input facility is provided for simple oscillator connection, with direct LED display of pk-pk bits of jitter. This can be used to measure the input jitter tolerance of digital transmission equipment. A second DS-3 output channel with 22 bits delay provides adequate simulation of an independent sequence for thorough testing of 4$\phi$ PSK digital radio systems. As an optional extra, four DSX-3 BNC outputs on the rear panel can be included for driving adjacent radio channels.

The 3782B Error Detector detects any binary or code errors generated by the system under test. At the DS-3 level, it can perform in-service or out-of-service measurements of parity errors within the digital transmission system. The 3782B can measure simultaneously error rate, error count, error seconds, and error free seconds over a single gating period. When the DS-3 MON facility is used, in-service measurements (eg parity errors) of live traffic are possible. For ease of use, there is a built-in automatic check for compatibility of switch position combinations. An error code flashes on the display if incompatibility is detected. Hard copies of results can be obtained on a printer via HP-IB control, either in the "talk-only" or "addressable" modes. In addition, a preselectable error rate threshold and a real time clock allows selection for printing results which exceed a defined threshold (with local time, if required).

## Ordering Information
3781B Pattern Generator
3782B Error Detector