Getting Started Guide

HP 1650B/HP 1651B Logic Analyzers

HEWLETT PACKARD

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Introduction

About this book . . .

Welcome to the new generation of HP logic analyzers. The HP 1650B/51B logic analyzers have been designed to be the easiest to use logic analyzers ever. In addition to being easy to use, these logic analyzers make a significant contribution to digital measurement technology.

That's why we'd like you to invest your time going through this *Getting Started* manual. Whether you're a novice logic analyzer user or just new to these particular models, this book will give you a working knowledge of the HP 1650B/51B so that you can start using it to solve your measurement problems. It covers:

- front panel organization;
- how to operate the front panel;
- learning the basic menus;
- how to set up the analyzer;
- how to make basic measurements.

To make the book easier to use, we have put the names of keys (**FORMAT**, **SELECT** etc.) in bold type. And we have highlighted actions (rotate the knob, press the **DISPLAY**) in color.

If you are an experienced HP logic analyzer user but new to this family of logic analyzers, you may feel like going directly to the reference manual. We'd like you to reconsider and read chapters 1 through 4 first. These chapters will only take a few minutes and you will find the user interface of the HP 1650B/51B very friendly and easy to learn.

Don't worry...we didn't try to cover every feature and function of the HP 1650B/51B logic analyzer in this manual. That's the job of your *HP 1650B/51B Front-Panel* manual.

If you're new to logic analysis...or just need a refresher, we think you'll find *Feeling Comfortable With Logic Analyzers* valuable reading. It will help you sort out any confusion you may have about their application and show you how to get the most out of your new logic analyzer.

1

Introducing the HP1650B/HP 1651B

What Are the HP 1650B and HP 1651B?

The HP 1650B/51B logic analyzers are new general-purpose logic analyzers with improved features to accommodate next-generation design tasks. They are basically the same as their predecessors the HP 1650A and HP 1651A, but now have State Compare, State Waveform, and State Chart modes. They both have HP-IB capabilities in addition to RS-232C. Both the 80-channel HP 1650B and the 32-channel HP 1651B logic analyzers are capable of 100 MHz timing analysis. The HP 1651B is capable of 25 MHz state analysis while the HP 1650B is capable of 35 MHz state analysis on all channels. The HP 1651B, while only having 32 channels, has basically the same features as the HP 1650B. That's why you have the same manual set regardless of whether you have an HP 1650B or HP 1651B.

The key features of the HP 1650B and HP 1651B are:

- Transitional or glitch timing modes
- Simultaneous state/state or state/timing modes
- 1k-deep memory on all channels
- Glitch detection on all channels
- Maker measurements
- Pattern, edge, and glitch triggering
- Overlapping of timing waveforms
- Eight sequence levels
- Eight pattern recognizers
- One range recognizer
- Small lightweight probing
- Time and number of states tagging
- Pre-store
- State Compare
- State Waveform
- State Chart

Not all of these features will be covered in this Getting Started manual. However, you can find the details of these and all the features of the HP 1650B/1651B in the *HP 1650B/HP 1651B Reference* manual.

Getting Ready to Operate

If you have just unpacked your new HP 1650B/51B logic analyzer, please take a few minutes to completely read this chapter. It tells you how to prepare your logic analyzer for applying power and turning it on. If you are learning how to use the logic analyzer and it is already turned on, start with with chapter 2 "Getting to Know the Front Panel".

Initial Inspection

Inspect the shipping container for damage. If the shipping container or packaging materials are damaged, you should keep them until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically.

If the contents of the shipping container have been damaged or the instrument does not operate properly, refer to the service manual.

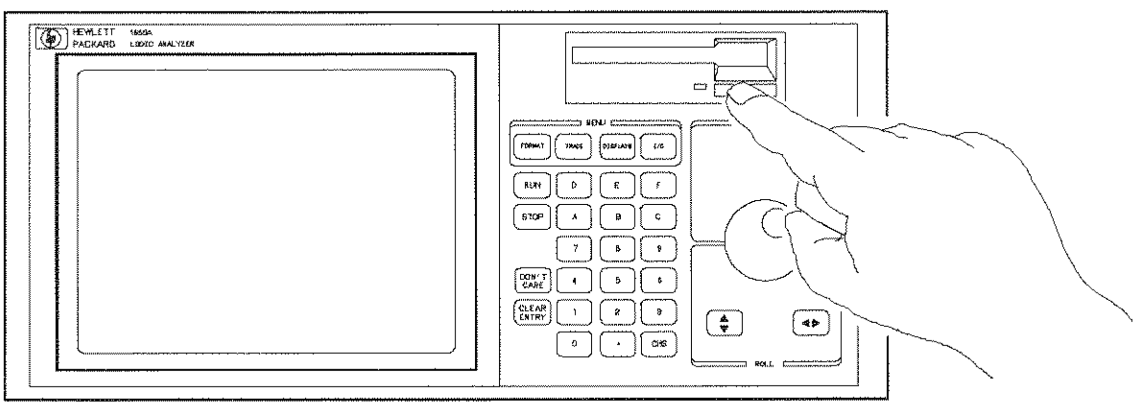
Accessories

In addition to checking the instrument for damage, you should also check to see that the accessories supplied with it are complete. Accessories can sometimes be lost in transit when the shipping container is damaged.

The *Front-Panel Reference* manual lists all the accessories for the HP 1650B/51B logic analyzers. If any of these items are missing contact your nearest Hewlett-Packard office.

Removing Yellow Shipping Disc

Your logic analyzer is shipped with a protective yellow shipping disk in the disk drive. Before you can insert the operating system disk you must remove the yellow shipping disk. Press the disk eject button as shown in the figure. The yellow shipping disk will pop out part way so you can pull it out of the disk drive.



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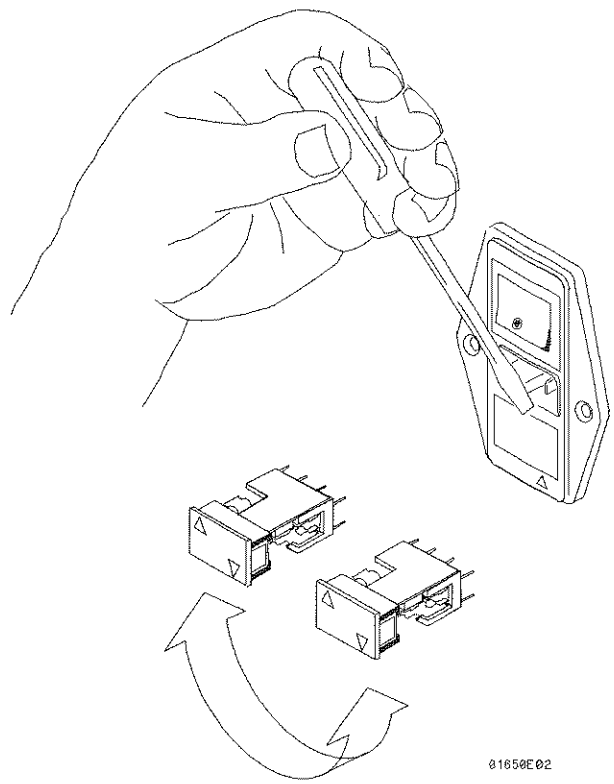
Selecting the Line Voltage

The line voltage selector has been factory set to the line voltage used in your country. It is a good idea to check the setting of the line voltage selector so you can become familiar with what it looks like. If the setting needs to be changed, follow the procedure in the next paragraph.

CAUTION

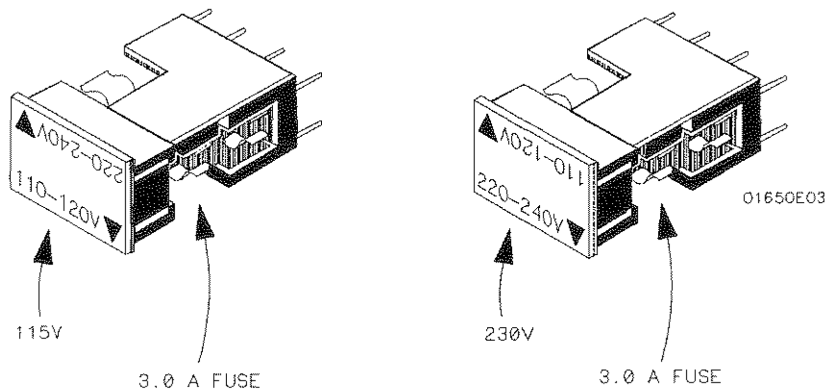
You can damage the logic analyzer if the module is not set to the correct position.



You change the line voltage setting by pulling the fuse module out and reinserting it with the proper arrows aligned. To remove the fuse module, carefully pry at the top center of the module (as shown) until you can grasp it and pull it out by hand.

Checking for the Correct Fuse

If you need to check for the correct fuses, remove the fuse module and look at the amperage and voltage of each fuse. The following figure will help you locate the 115 V and 230 V fuses. To remove the fuse module, carefully pry at the top center of the module until you can grasp it and pull it out by hand. (Refer to "Selecting the Line Voltage" on the previous page.)



Getting Power to the Instrument

The HP 1650B/51B comes with a 3-wire power cable. When you connect the cable to an appropriate AC power receptacle, a ground is provided for the instrument cabinet. The type of power cable you receive with the instrument depends on your country.

WARNING **To avoid possible shock hazard, you must connect the instrument to a properly grounded 3-wire receptacle.**

Operating Environment

You may operate your logic analyzer in a normal lab or office environment without any additional considerations. But don't block its ventilation. If you intend to use it in another type of environment, you must not exceed certain limits. You can find these limits in the *HP 1650B/HP 1651B Front-Panel Reference* manual.

Ventilation

You must provide an unrestricted airflow for the fan and ventilation openings in the rear of the logic analyzer. However, you may stack the logic analyzer under, over, or in-between other instruments as long as the surfaces of the other instruments aren't needed for their ventilation.

Loading the Operating System

Before you can operate the logic analyzer, it must transfer its operating system from a disk to its memory. This is called "loading the operating system" or "booting."

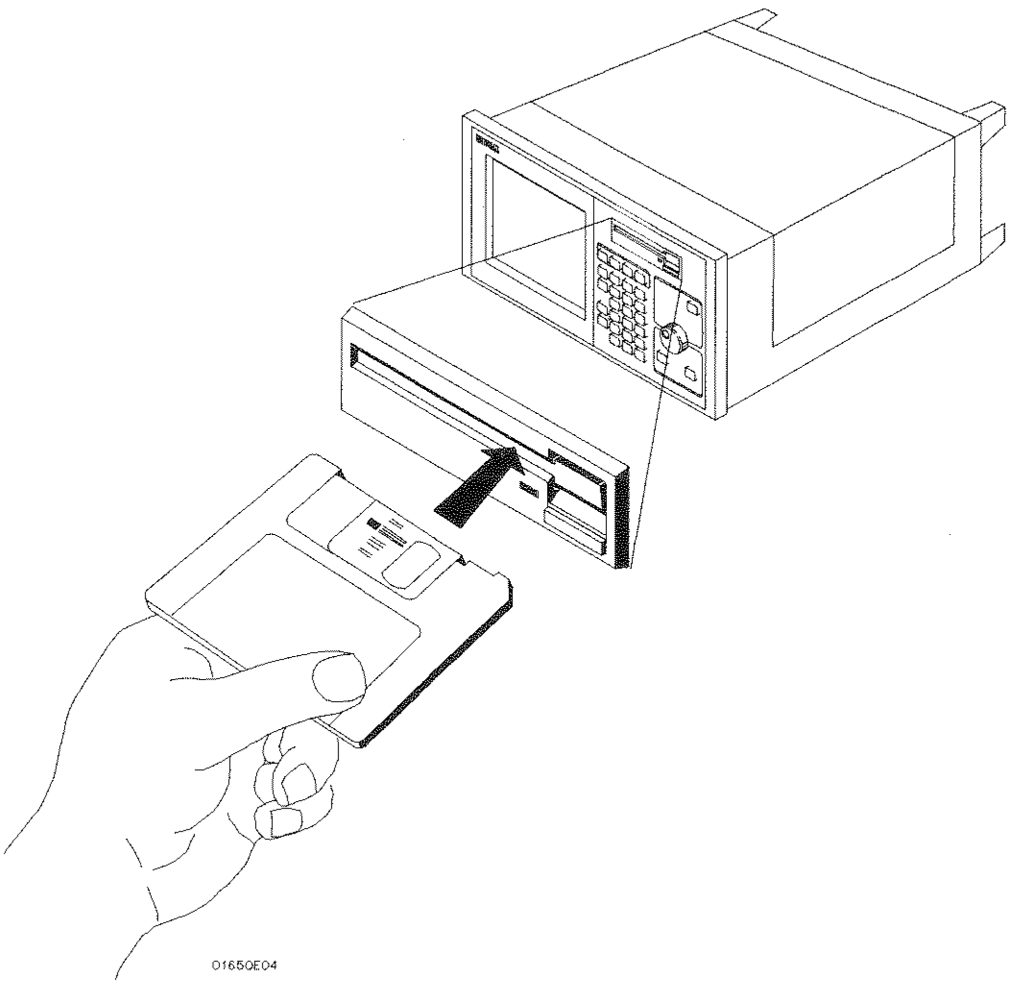
The logic analyzer operating system is a set of instructions that control the operation of the instrument. The operating system resides on a 3.5-inch flexible disk. You received two identical operating system disks. You should mark one of them **Master** and store it in a safe place. Mark the other one **Work** and use only the work copy. This will provide you with a back-up in case your work copy becomes corrupt.

CAUTION

To prevent damage to your operating system disk, DO NOT remove the disk from the disk drive while it is running. Only remove it after the indicator light has gone out.

Installing the Operating System Disc

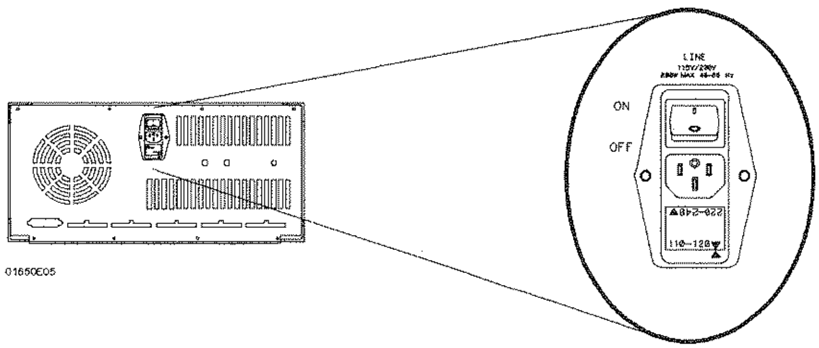
To load the logic analyzer's operating system, you must install the disk as shown below **before** you turn on the power. When the disk snaps into place, the disk eject button will pop out. Now you can turn on the logic analyzer.



The logic analyzer runs a series of self-tests and loads the operating system before it is ready to be operated.

Line Switch

The line switch is on the rear panel. You turn on the logic analyzer by pressing the 1 on the rocker switch. Make sure the operating system disk is in the disk drive before you turn it on. If you forget the disk, don't worry, you won't harm anything. You will merely have to repeat the turn-on procedure with the disk in the drive.



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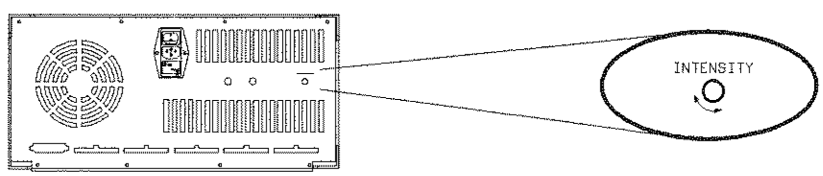
Intensity Control

Once you have turned on the instrument, you may want to set the display intensity to a different level that's more comfortable for you. You do this by turning the INTENSITY control on the rear panel.

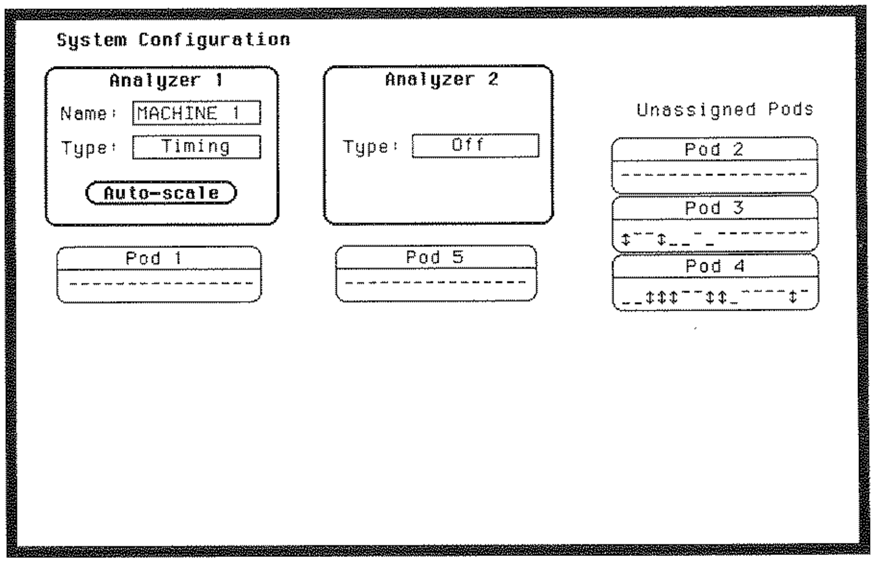


01650E06

Power-up Self-Test

When you turn on the logic analyzer, it performs a series of self- tests. When it has successfully completed these tests, it loads the operating system into memory from the disk.

When the logic analyzer has completely loaded the operating system it displays the System Configuration menu as shown below.



Note

This is the HP 1650B System Format Specification menu. If you have an HP 1651B, the only difference is pod 1 will be assigned to analyzer 1 and pod 2 will be assigned to analyzer 2. There won't be any pods in the **UNASSIGNED** area of the display.

Summary

Now that you have unpacked, inspected, and begun operating the logic analyzer, the next step will depend on your needs. If you are a first-time logic analyzer user who wanted to get the instrument running before reading *Feeling Comfortable with Logic Analyzers* you should read it now. If you are familiar with logic analysis, read either the rest of this *Getting Started Guide* or the *HP 1650B/HP 1651B Front-Panel Reference* Manual.

In a task format this *Getting Started Guide* teaches you the basics of how to operate the front panel and configure it for basic measurements.

The *HP 1650B/HP 1651B Front-Panel Reference* manual describes all the front-panel and programming functions of the logic analyzers. The *HP 1650B/HP 1651B Programming Reference* manual describes the programming commands and conventions for the logic analyzers. Once you feel comfortable with the basic operation of the front panel, use this book.

2

Getting to Know the Front Panel

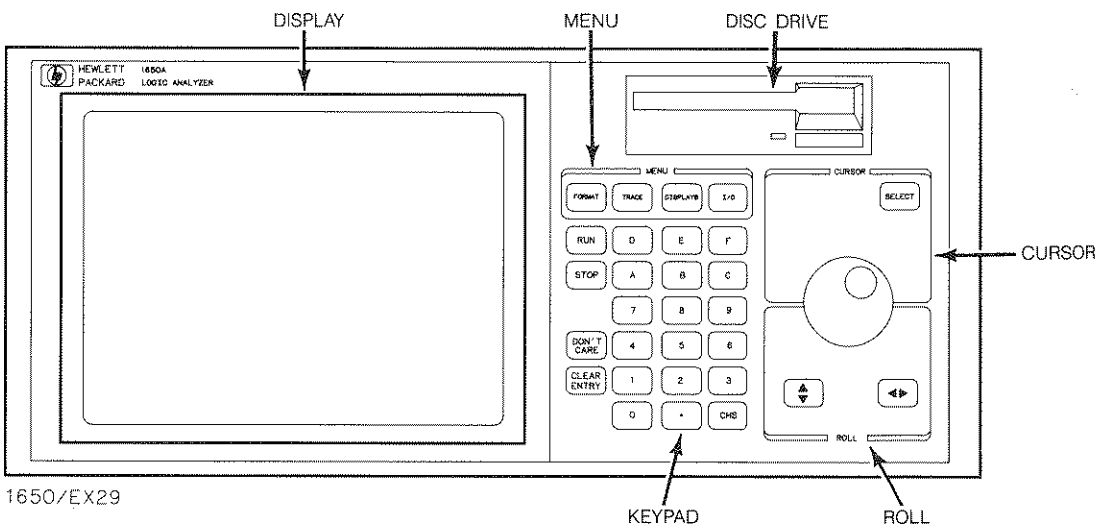
Introduction

The HP 1650B/51B logic analyzers have been designed to be very easy to use. The controls are located logically by function so you can learn how to use them quickly and easily.

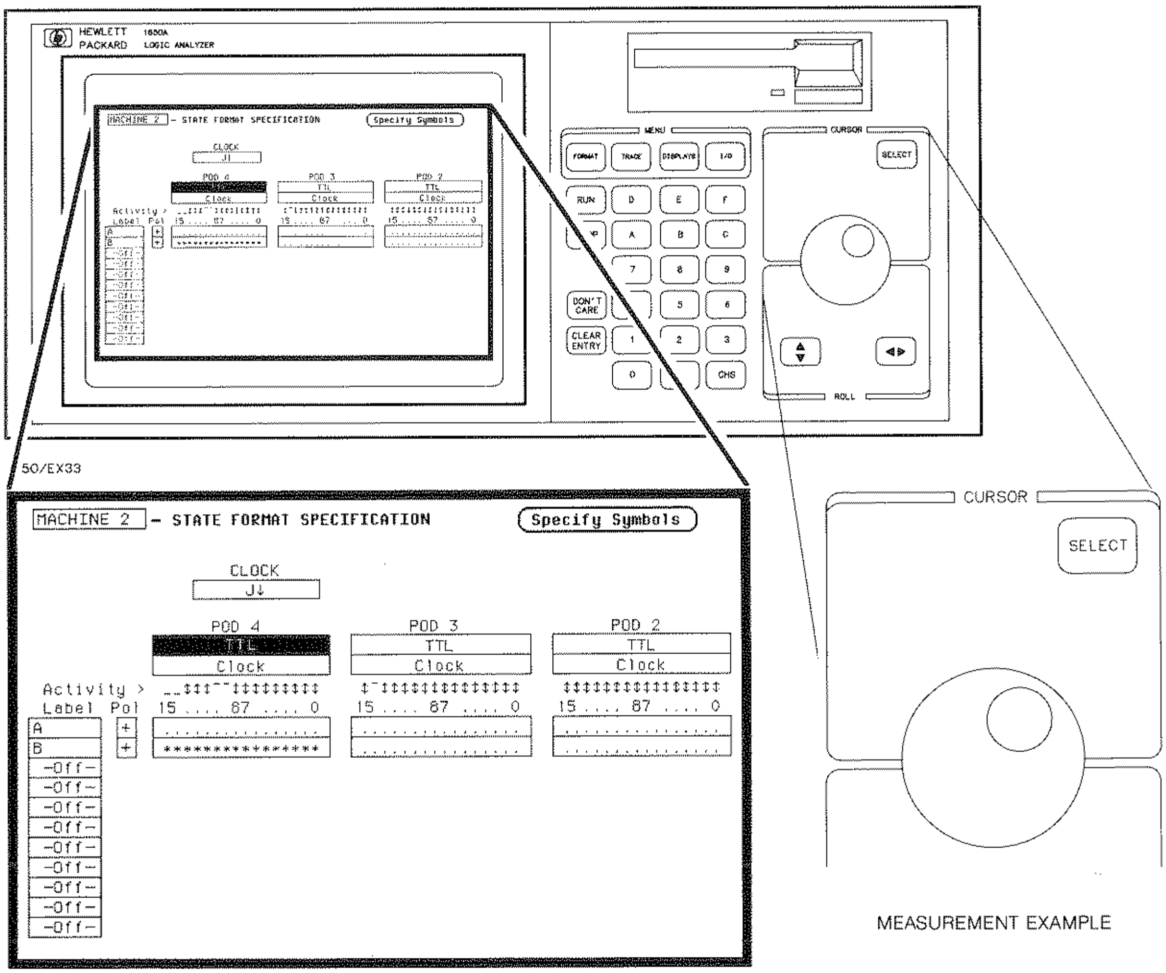
This chapter breaks down the front panel into these functional areas and gives you an overview of each area.

Front Panel Organization

The functional areas of the front panel are: display, MENU, keypad, CURSOR, ROLL and disk drive.



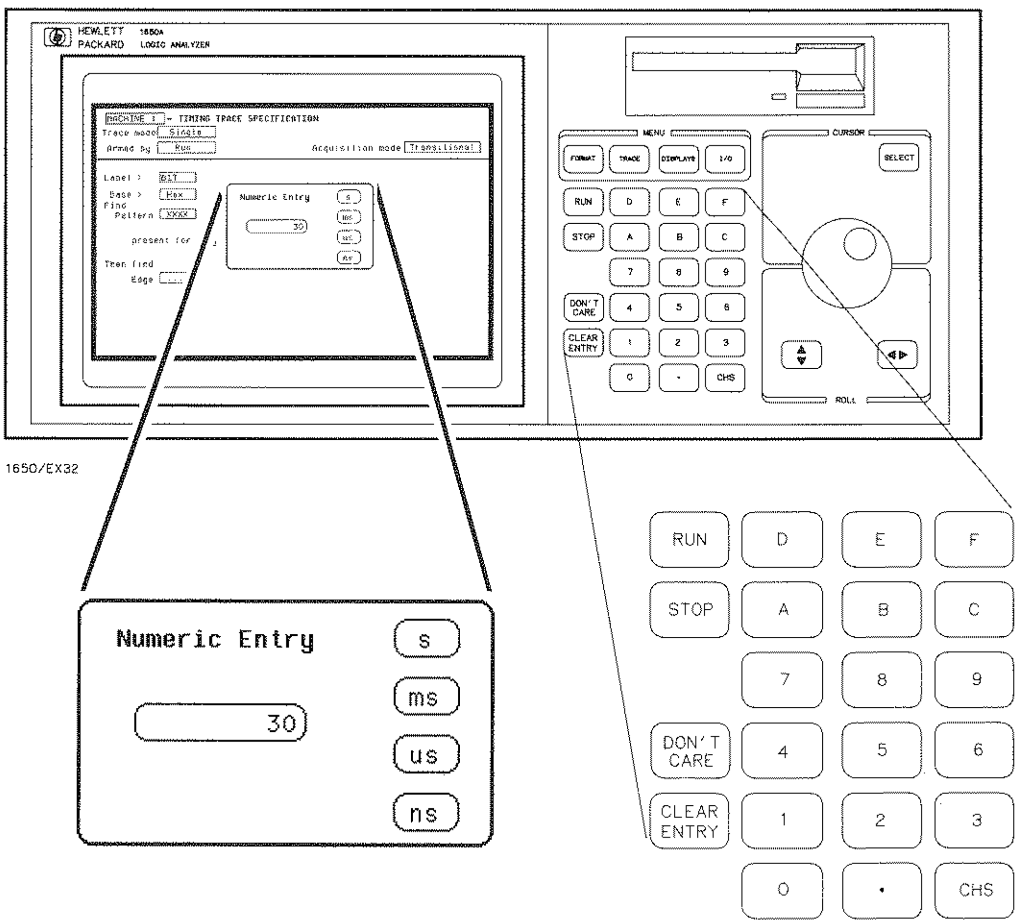
Cursor The CURSOR is a movable indicator on the display that allows you to access desired fields in each menu. It changes the field where it resides from the normal white background to the dark background (inverse video). The KNOB moves the cursor to the field (function) you wish to use. You activate the field (function) by pressing the **SELECT** key.



MEASUREMENT EXAMPLE

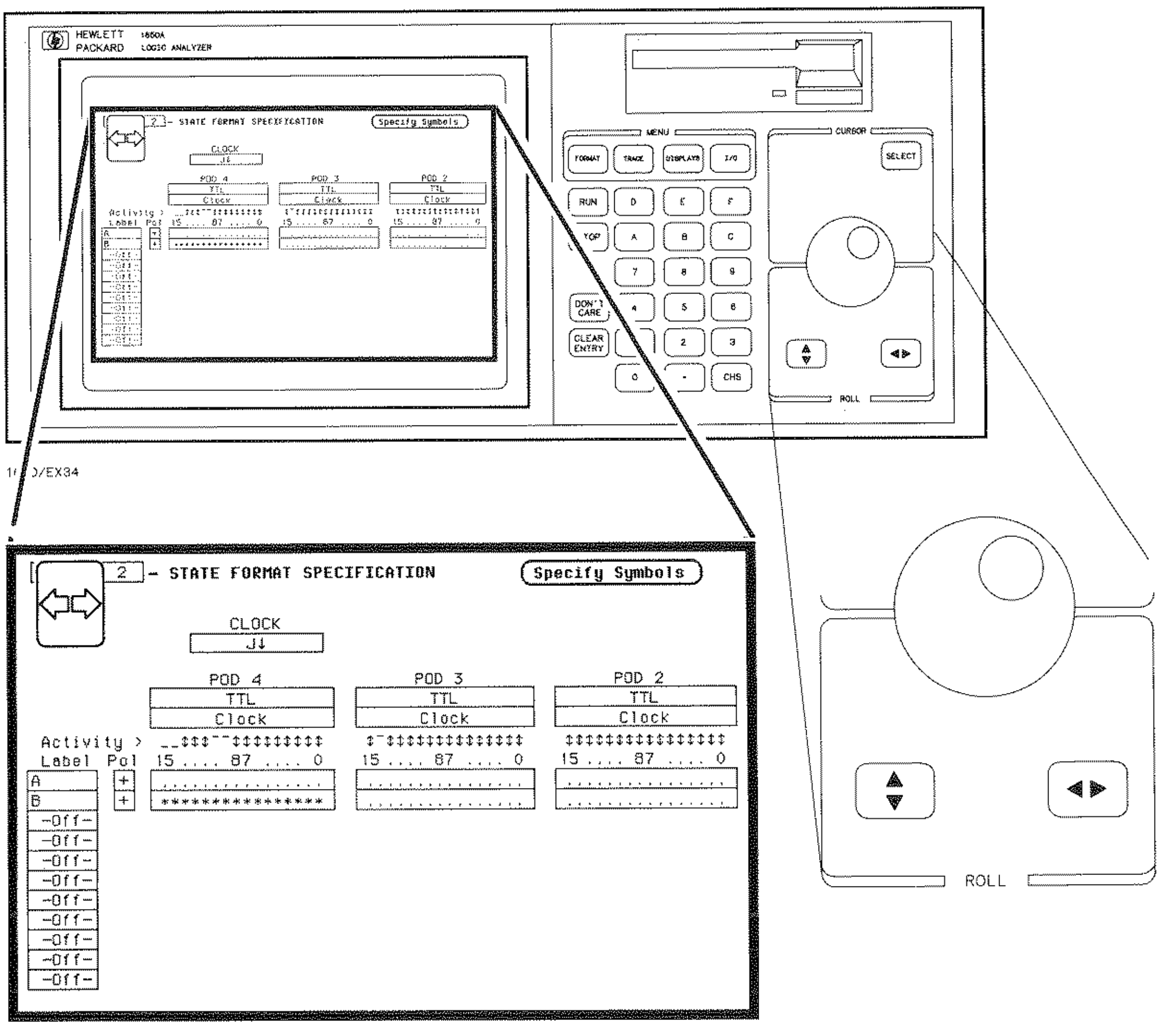
MENU EXAMPLE

Keypad The keypad allows you to start and stop data acquisition as well as enter alphanumeric data. Also in the keypad area are the **DON'T CARE** and **CLEAR ENTRY** keys.



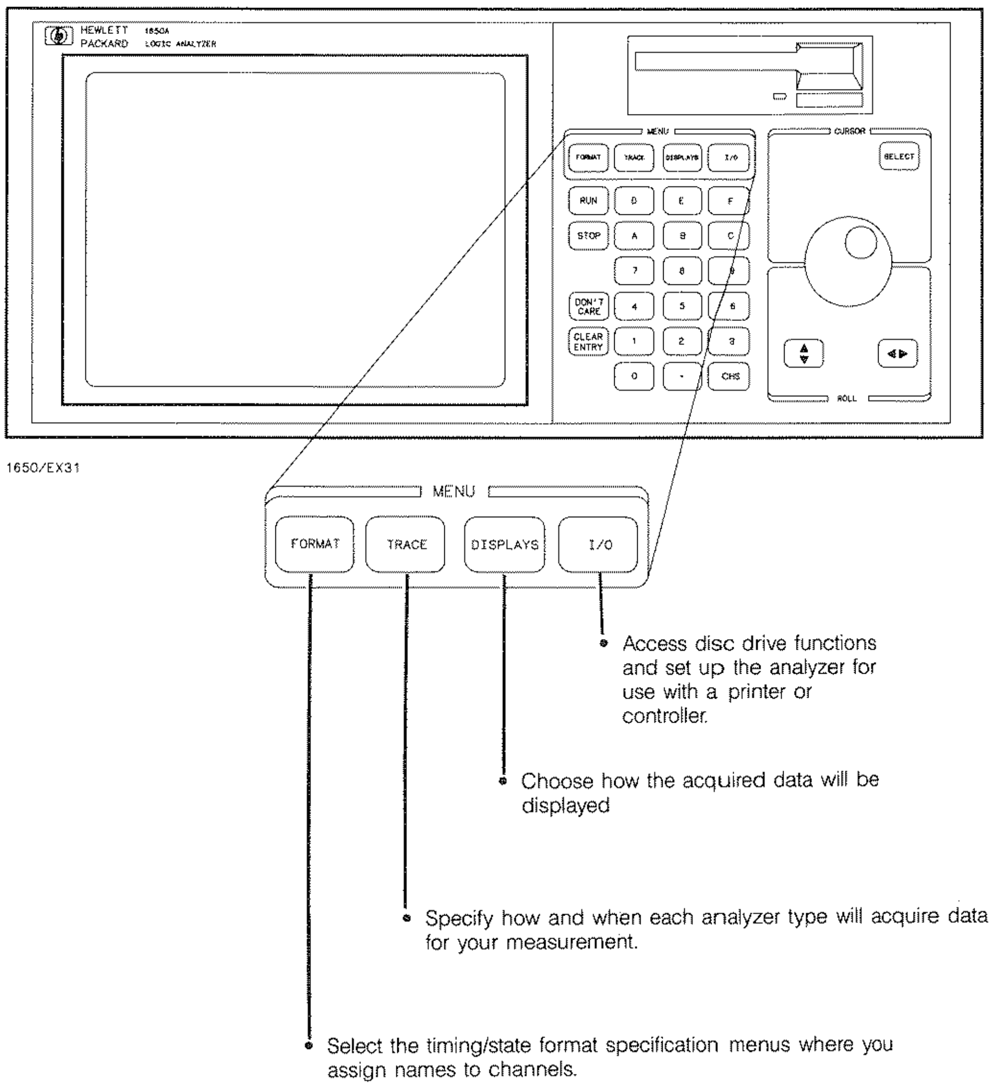
1650/EX32

Roll When part of the data display is off screen, the **ROLL** keys define which way the **KNOB** will move the displayed data. You will use these keys and the **KNOB** to roll displayed data up/down or left/right to view data that is off screen.



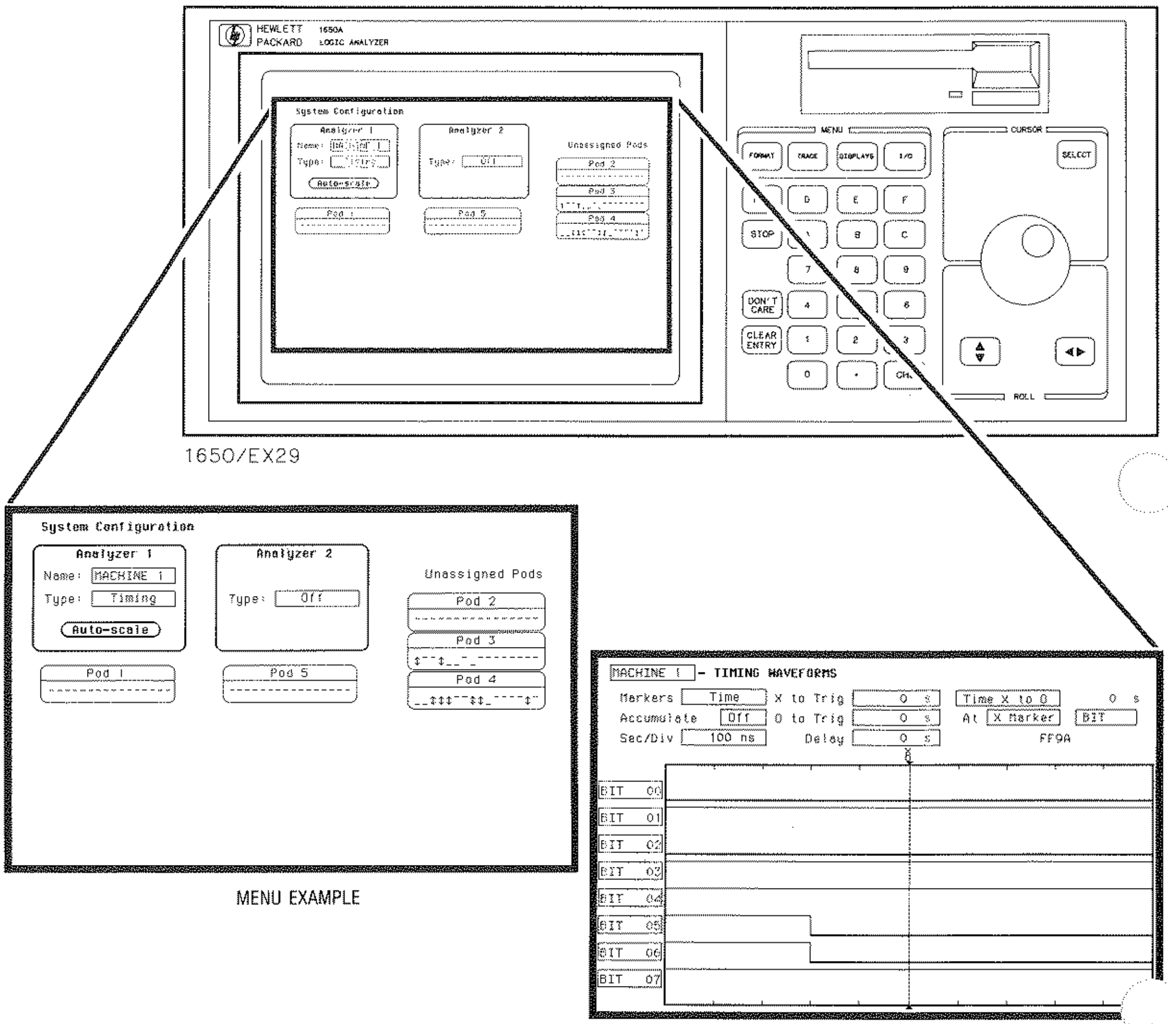
Menu

The MENU area contains keys that give you access to the four major menus of the logic analyzer. You use this area to:



1650/EX31

Display The display shows you the menus for configuring the logic analyzer and the results of your measurements.



MENU EXAMPLE

MEASUREMENT EXAMPLE

Disk Drive

The logic analyzer uses the disk drive every time you turn on the logic analyzer to load its operating system. The disk drive uses 3.5-inch flexible disks. You can also use the disk drive to store instrument configurations, acquired data, and inverse assemblers for later use. Complete details on the disk drive and its functions can be found in the *HP 1650B/HP 1651B Front-Panel Reference* manual.

Summary

Now that you are acquainted with the front panel organization, you will be able to decide where you want to go next. If you are just starting to learn logic analysis, you should read this entire manual. If you are experienced in logic analysis, you should continue to read chapters 3 and 4 to become more familiar with the operation of the front panel before you turn to the reference manual. These chapters will show you how easy the HP 1650B/51B logic analyzers are to operate.

3

How Do I Use the Front Panel?

Introduction

In this chapter you will learn how easy the HP 1650B/51B logic analyzer front panel controls are to use. You will also learn the front panel by following self-paced exercises.

This chapter starts you off in the System Configuration menu, the same place the logic analyzer starts after you turn it on. You will learn how easy it is to get in and out of this menu. You will also learn what the shapes of the menu fields mean.

Don't be concerned about not seeing measurement examples in this chapter. You will see them in chapters 5 through 8.

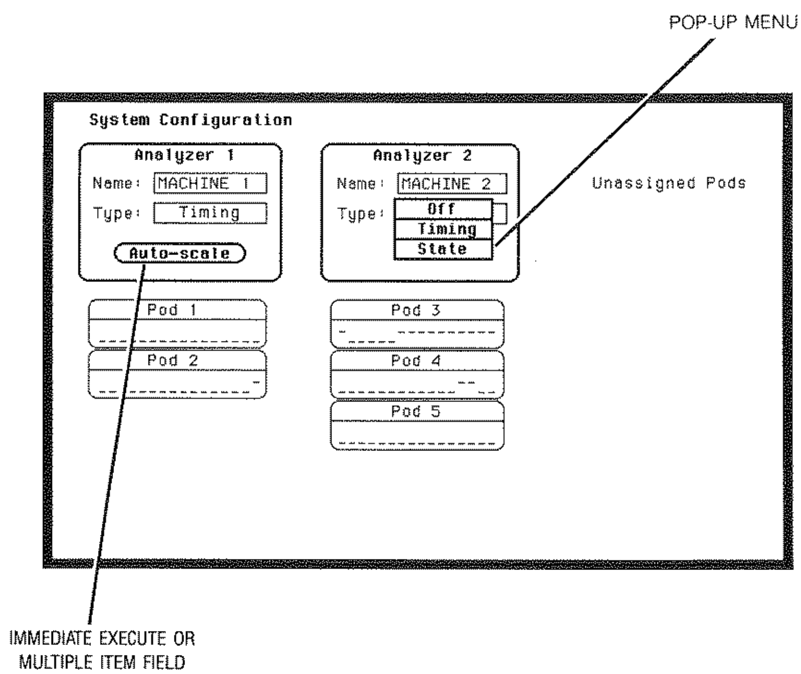
Menu Field Conventions

Before starting to work with the menus, you need to know the two menu field conventions. This allows you to quickly recognize what type of action will occur when you select a field.

There are two shapes that you should become familiar with: rectangles with square corners and rectangles with rounded corners.

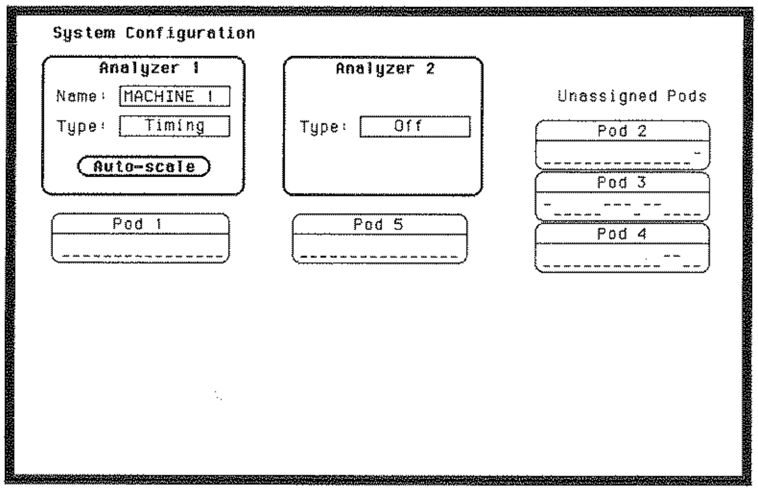
When you select a field with square corners, it pops up and lists two or more items. You must select a single item.

Fields with rounded corners will either execute the function immediately or pop up with a list of multiple items that you must specify.



Your First Step

When you turn on the logic analyzer and the operating system has finished loading, you will see the System Configuration menu. Notice the cursor is in one of the fields in this menu. Operating the HP 1650B/51B front panel is like learning to drive a car.



To "drive" around the menu, turn the **KNOB** and watch the cursor move from field to field. Most of the logic analyzer operation is accomplished by placing the cursor on the field you want to interact with and pressing the **SELECT** key. Depending on the field type (immediate execute or pop-up) pressing **SELECT** will either execute a function or open a pop-up menu.

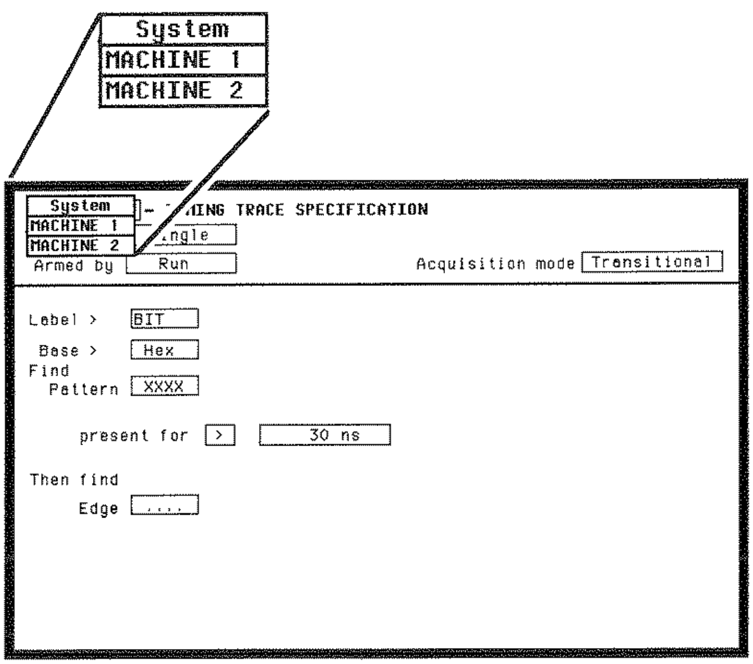
Note

This is the HP 1650B System Format Specification menu. If you have an HP 1651B, the only difference is pod 1 will be assigned to analyzer 1 and pod 2 will be assigned to analyzer 2. There won't be any pods in the **UNASSIGNED** area of the display.

Returning to the System Configuration Menu

When you leave the System Configuration menu, you can return to it at any time by following these steps:

1. Press either the **FORMAT**, **TRACE**, or **DISPLAY** key. You now see a new menu. All three of these menus have a field in the upper left corner. This field will display either **MACHINE 1** or **MACHINE 2** depending on how the logic analyzer was configured.
2. Place the cursor on this field and press **SELECT**. You will see the following pop-up menu.
3. Place the cursor on **System** and press **SELECT**. You will be returned to the System Configuration menu.



Exploring the System Configuration Menu

Now is a good time to explore the System Configuration menu by driving the cursor around and pressing **SELECT.** Don't worry, you can't hurt anything because no matter what field you select you will have an easy way out.

For example, select the **Name: MACHINE 1** field, and you will see a pop-up that you can use to name analyzer number 1. In this pop-up menu you will see a field named **Done** that lets you get out of this menu and back to the System Configuration menu where you started.

If you select **Auto-scale,** the logic analyzer will display a pop-up with the choices of **Cancel** and **Continue.** The **Cancel** allows you to change your mind before the auto-scale is executed. This is handy because auto-scale will **change** your previous configurations .

If you select **Continue,** the logic analyzer will display the TIMING WAVEFORMS menu. However, if there is no signal activity at the probes, the Waveforms menu will not display data and the label to the left of the waveform area will be **-off-.**

To get back to the System Configuration menu after executing **Auto-scale:**

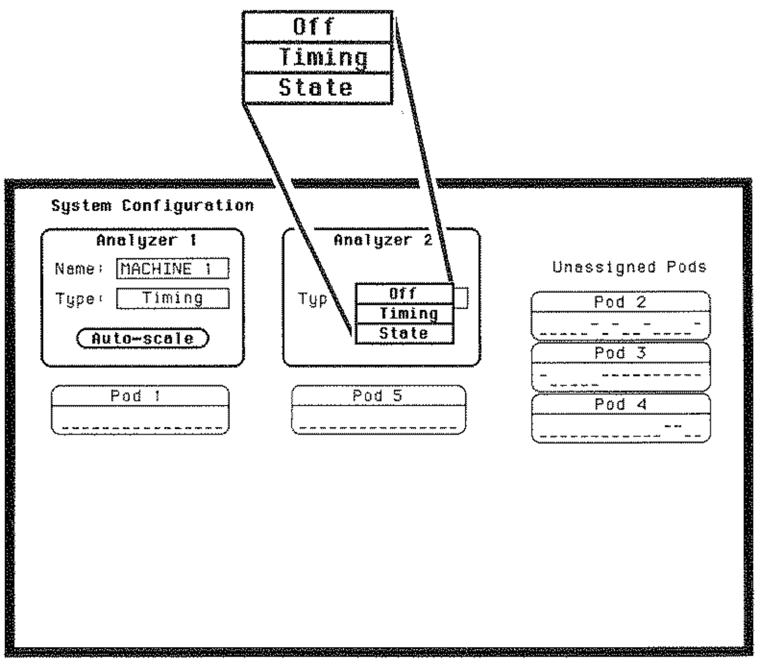
1. Place the cursor on the field in the upper left corner and press SELECT.
2. Place the cursor on **System** in the pop-up and press **SELECT**. You will now be back in the System Configuration menu.

Closing Pop-up Menus

In previous exercises, you closed the **Alpha Entry** pop-up by using the **Done** field. But, what if there is no **Done** in the other fields? Fields that don't have choices like **Done, Cancel,** or **Exit** will close automatically when you make your selection. For example, you have used this type of pop-up to get back to the System Configuration menu.

To see another example of a pop-up that automatically closes, follow these steps:

1. Rotate the **KNOB** until the cursor is on the **Off** field in the **ANALYZER 2** field, then press **SELECT**. You will now see the following pop-up:



2. Place the cursor on **State** and press **Select.**

The pop-up menu will automatically close, analyzer 2 is now on and the type will be State.

Summary

In this chapter you learned what menu the logic analyzer displays once you have turned it on and where you will usually start configuring the logic analyzer once you are ready to make measurements.

The next chapter will teach you the most common types of pop-up menus, which will help you progress towards making measurements as explained in chapters 5 through 7.

4

Learning the Basic Menus

Introduction

In this chapter you will learn the most common pop-up menu types by doing some basic exercises. The pop-up menu types you will learn in this chapter are:

- Selector
- Alpha Entry
- Numeric Entry
- Assignment/Specification

Selector Pop-up Menu

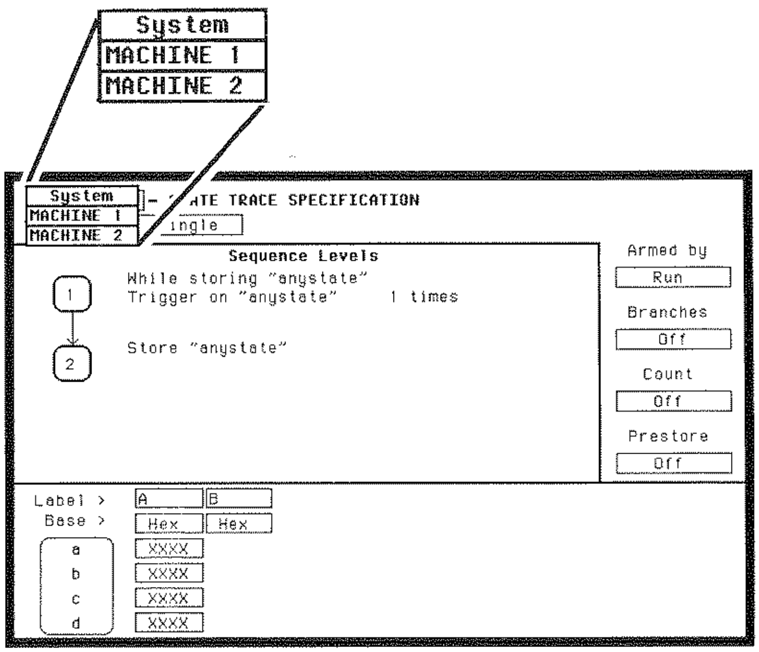
In the selector type of pop-up menu you do what the name implies, make a selection from two or more options. The best way to introduce you to a selector type of menu is to have you work with one right away.

Switching Between Analyzers

You will use a selector type of pop-up menu to switch between analyzers or get back to the System Configuration menu. You can switch analyzers in the FORMAT, TRACE and DISPLAY menus, without having to go back to the System Configuration menu. This is done easily by following these steps:

1. Press the **TRACE** key. You will now be in either the TIMING TRACE or STATE TRACE SPECIFICATION menu depending on what you did last in the System Configuration menu.

2. Place the cursor in the field in the upper left corner of the menu and press **SELECT.** A pop-up menu will appear displaying **System** and the current analyzer names (default names are **MACHINE 1** and **MACHINE 2**). The cursor will be on the current analyzer.



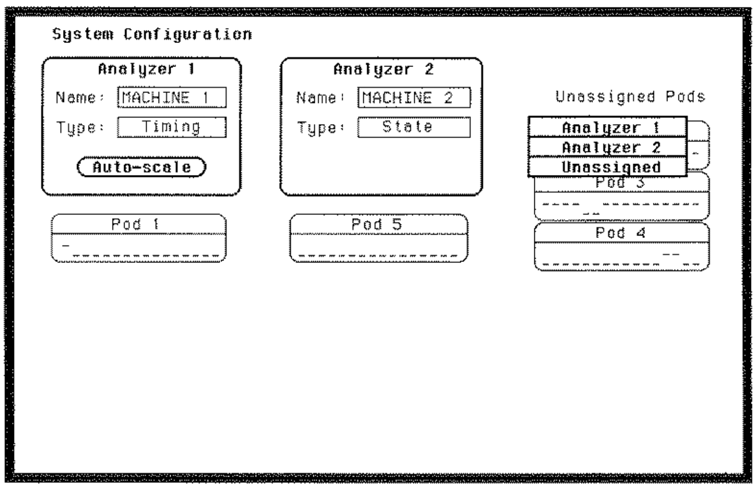
3. Move the cursor to the other machine (analyzer) and press **SELECT.** The pop-up will close and you will see the corresponding menu of the other analyzer on the display.

Assigning Pods

Another selector menu type you will use is assigning pods to the analyzers. To assign pods:

1. Get back to the System Configuration menu (refer to "Returning to the System Configuration Menu" in chapter 3 if you need a reminder).

2. Place the cursor on one of the pod fields on the right side of the display and press **SELECT.** You will see the following menu:



3. Place the cursor on **Analyzer 2** and press **SELECT.** The pop-up closes and your desired pod is now assigned to analyzer 2.

Alpha Entry Pop-up Menu

You can give specific names to several things. These names can represent your measurement specifically.

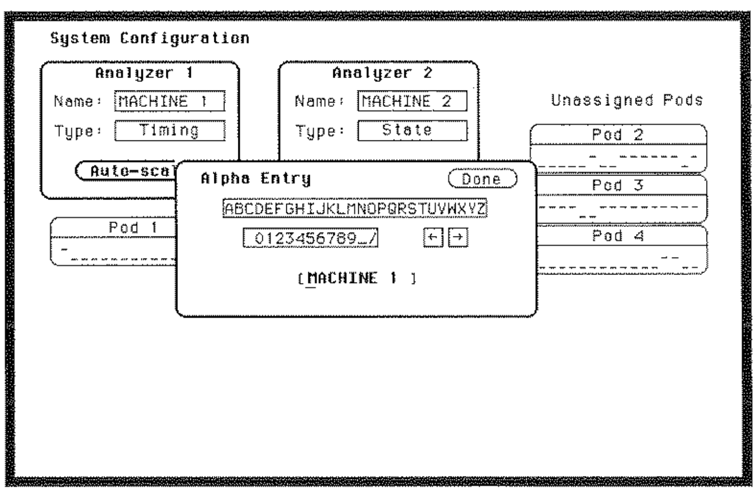
The two major examples of items that can be named are:

- Both analyzers
- Labels

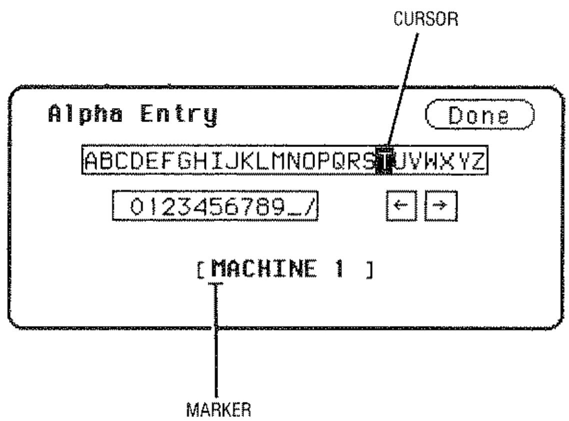
To learn how this type of pop-up works, you'll name analyzer 1 LEARN. However, LEARN will be misspelled when you finish entering it. Don't worry, this is intentional. You will then be shown how to correct it.

1. Get back to the System Configuration menu refer to "Returning to the System Configuration Menu" in chapter 3 if you need a reminder).
2. Rotate the **KNOB** until the cursor is over **MACHINE 1** and press **SELECT.**

You will now see a pop-up window in the System Configuration menu as shown in the example.



3. Rotate the **KNOB** and you will see how the cursor moves within the pop-up.



4. Now that you are ready to name analyzer 1, move the cursor so that it is on the L and press **SELECT**.

In the bottom of the pop-up, you will see an L in the far left corner of the bottom box. Also notice the under-score marker in the bottom box is now under the A of MACHINE. The under-score marker tells you in what space in the box your next selection will be placed.

5. Rotate the **KNOB** again until you have placed the cursor over the E, then press **SELECT**.

Note You can also make direct keypad entries. Your selection will be placed where the under-score marker is in the box.

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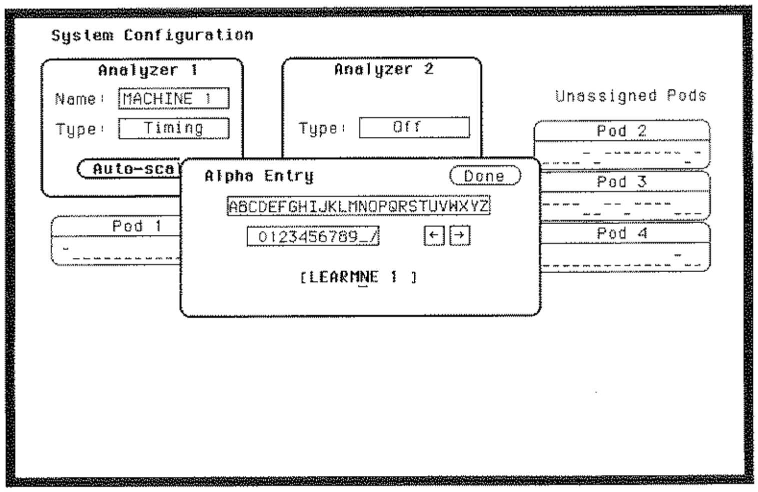
6. Repeat step 5 three more times selecting A, R, and M respectively.

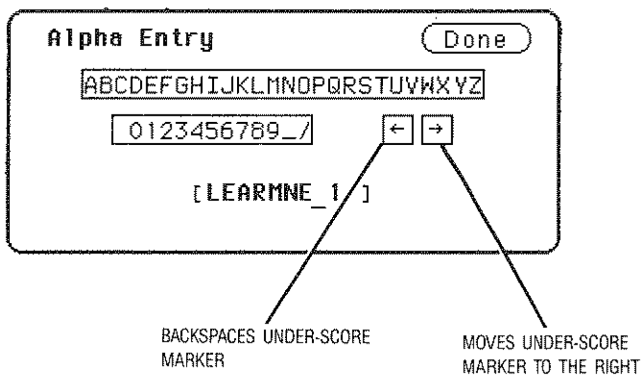
You should now see LEARMNE 1 in the bottom box. Since this is not the name you wanted, change the name.



Changing Alpha Entries

To make changes or corrections in the Alpha Entry field, place the under-score marker under the character you want to change.

To move the under-score marker to the left, place the cursor over the left arrow and press **SELECT** once for each backspace.



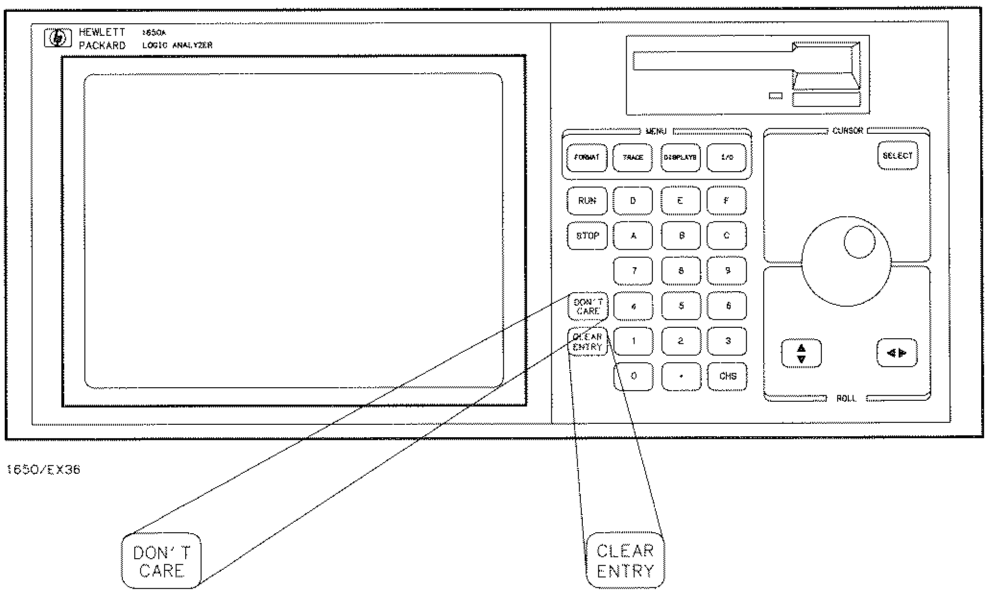
To move the under-score marker to the right, you either place the cursor on a desired character and press **SELECT**, or place it on the right arrow and press **SELECT**.

You can also use the **ROLL** Keys and the **KNOB** to move the underscore marker. To use this alternate method:

1. Press the left/right **ROLL** key.
2. Rotate the **KNOB** to place the under-score marker under the desired character.
3. Press the left/right **ROLL** key again to turn off the **ROLL** function.

If you want to erase the entire entry and place the under-score marker at the beginning of the name box, press the **CLEAR ENTRY** key on the front panel.

If you want to replace a character with a space, place the underscore marker under that character and press the **DON'T CARE** key on the front panel.



1650/EX36

Now that you have entered and edited a name, you will know how to use the Alpha Entry pop-up menu in other logic analyzer menus where it appears.

Numeric Entry Menus

There are many pop-up menus in which you enter numeric data. The two major types are:

- Numeric entry with fixed units (i.e. volts)
- Numeric entry with variable units (i.e. ms, μs, etc.)

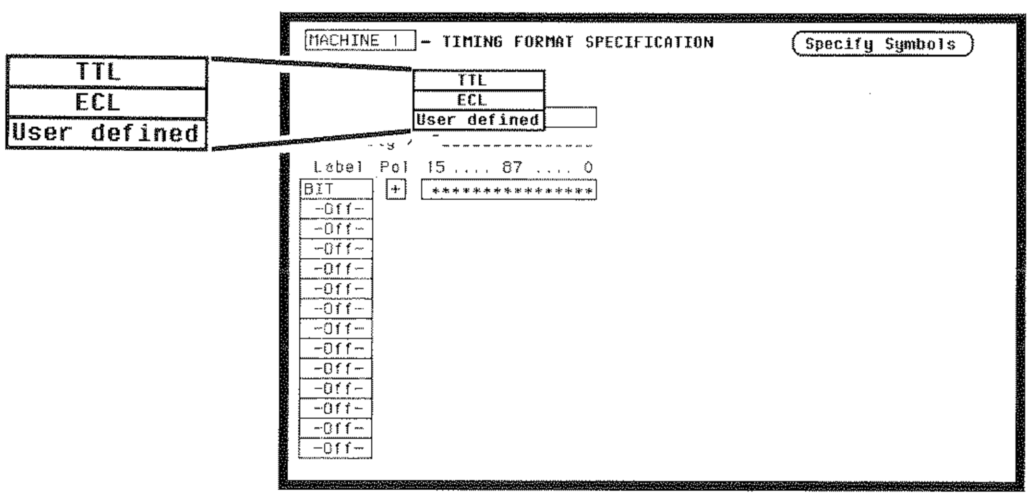
There are several numeric entry menus in which you only enter the value, and the units are fixed. One such type of numeric entry pop-up is the POD Threshold pop-up menu.

Besides being able to set the pod thresholds to either of the preset thresholds (TTL or ECL), you can set the thresholds to a specific voltage from –9.9 V to + 9.9 V.

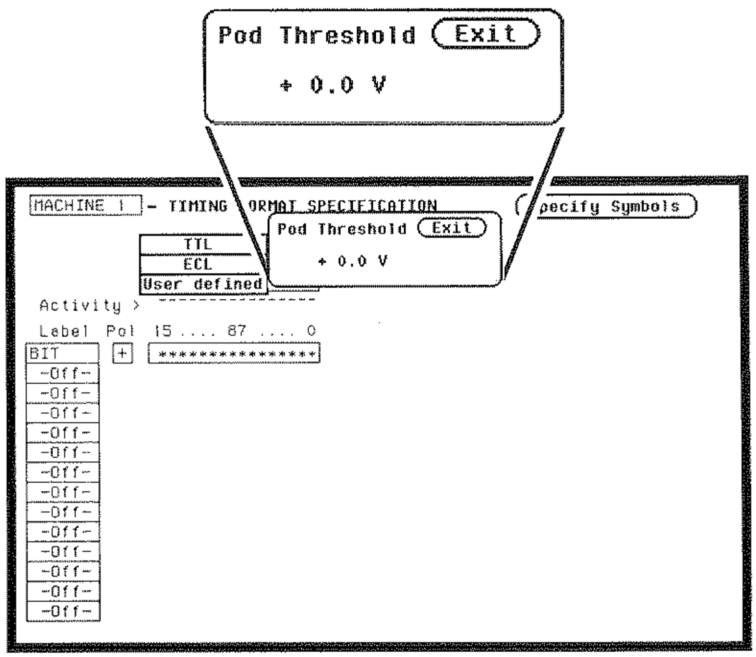
To set pod thresholds to a specific voltage, follow these steps:

1. Select either the TIMING or STATE FORMAT SPECIFICATION menu by pressing the **FORMAT** key. It doesn't matter whether you are in the TIMING or STATE FORMAT SPECIFICATION menu.

2. Rotate the **KNOB** to place the cursor in the TTL field of any pod displayed and press **SELECT.** You will now see a pop-up with the choices, **TTL, ECL,** and **User defined.**



3. Place the cursor on **User Defined** and press **SELECT**. Another pop-up menu will appear as shown.



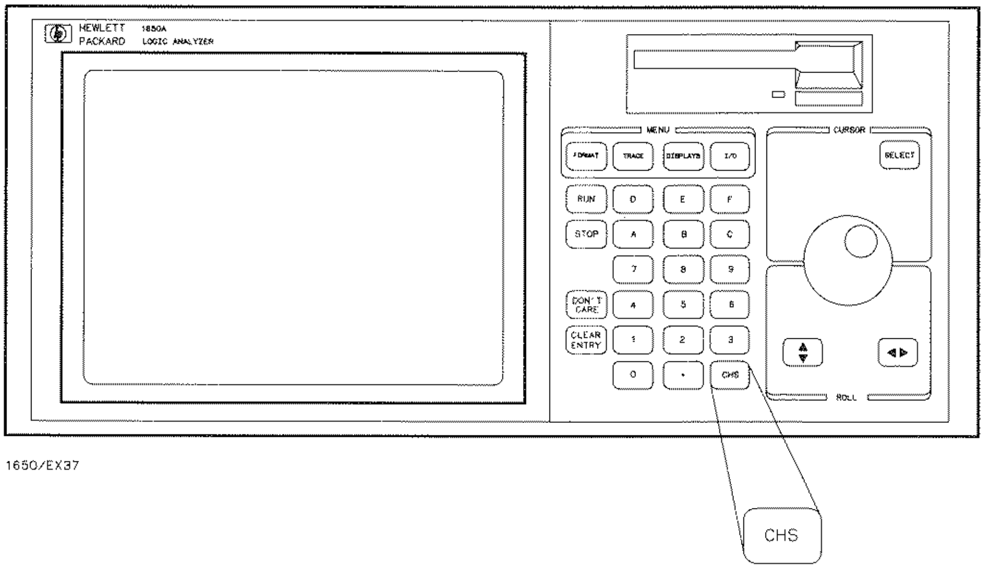
You can enter your desired threshold with either of two methods when the pod threshold pop-up is open. The first method is to rotate the **KNOB** until your desired threshold is displayed. Rotating the **KNOB** increments or decrements the value in small increments.

The second method is to use the keypad, which allows you to change large values quickly. With the keypad follow these simple steps to enter –5.0 V for the pod threshold:

4. Enter 5.0 from the keypad. You will see the 0.0 V replaced with 5.0.

5. Press the **CHS** (change sign) key on the front panel. You will now see –5.0 in the pop-up.

Also notice the cursor is in the upper right corner of the pop-up over the operative **Exit.** When you press **SELECT,** the pop-up will close and your new threshold will be placed in the Pod field.



1650/EX37

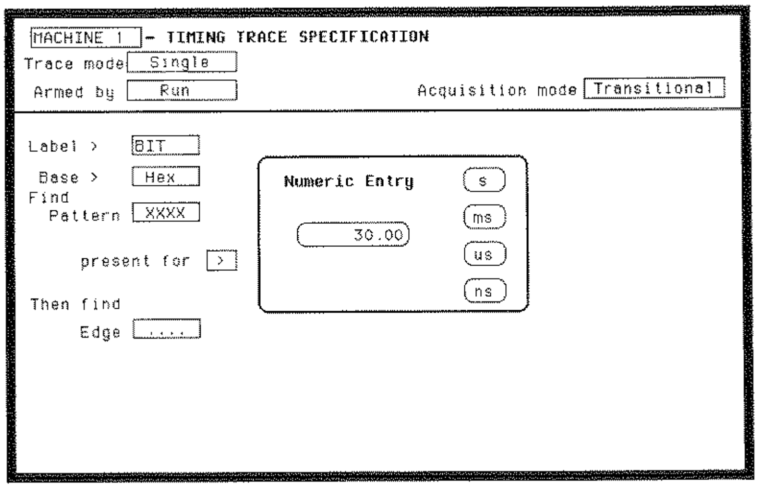
Another type of numeric entry you will use requires you to specify the units as well as the numeric value. The following steps show you how:

1. Select the TIMING TRACE SPECIFICATION menu by pressing the **TRACE** key.

Note If the STATE TRACE SPECIFICATION menu comes up, refer to "Switching Between Analyzers" in this chapter.

---

2. Rotate the **KNOB** to place the cursor in the **30 ns** box within the **present for> 30 ns** line and press **SELECT.** You will now see the following pop-up:



3. Enter a new value to replace 30.00 with the keypad. When you have entered your desired value, you can change the units type by rotating the **KNOB.**

Once you have selected the new value and the units, close the pop-up by pressing **SELECT.** The new value and the units will now be displayed in the **present for >** _____ field.

Assignment/ Specification Menus

There are a number of pop-up menus in which you assign or specify what you want the logic analyzer to do. The basic menus of this type consist of:

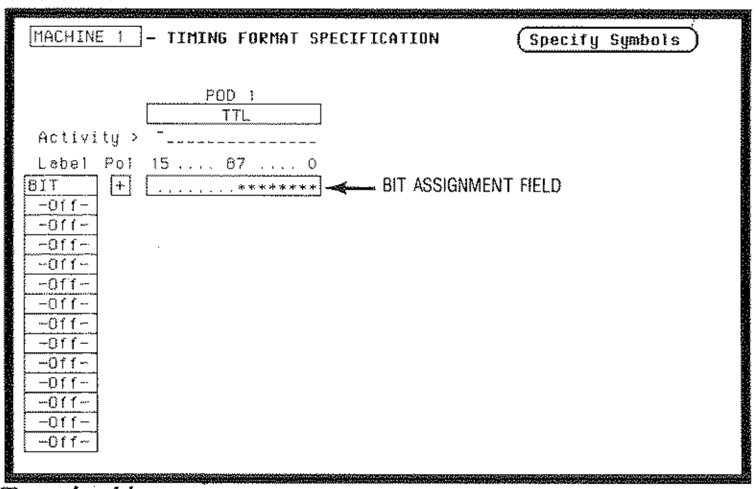
- Assigning bits to pods
- Specifying patterns
- Specifying edges

Assigning Bits to Pods

The bit assignment fields in both state and timing analyzers work identically. Before starting this exercise you need to know how the logic analyzer knows which bits are assigned and which ones are not assigned. The convention for bit assignment is:

*(asterisk) indicates assigned bits.
. (period) indicates un-assigned bits.

In the following menu example, bits 0 through 7 are assigned to the label **BIT.**



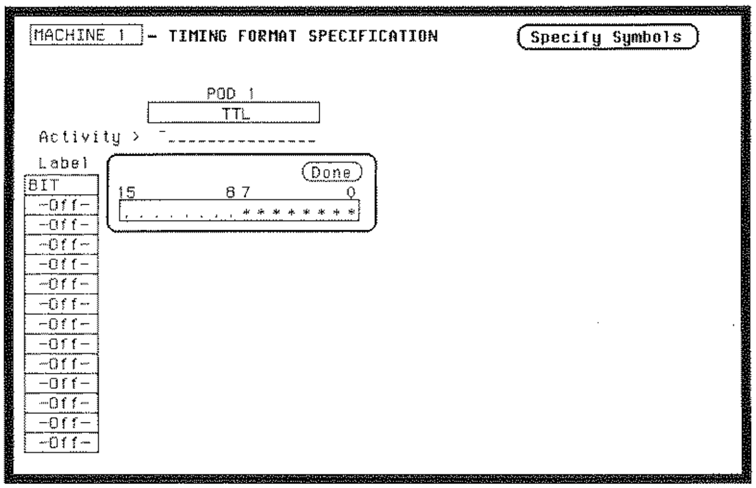
To assign bits:

1. Select either the TIMING or STATE FORMAT SPECIFICATION menu.

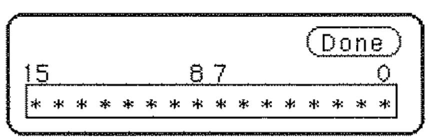
2. Place the cursor on one of the bit assignment fields and press **SELECT**. You will see the following pop-up menu.

Note

If you don't see any bit assignment fields, it merely means you don't have any pods assigned to this analyzer. Either switch analyzers or assign a pod to the analyzer you are working with.



3. Rotate the **KNOB** to place the cursor on one of the asterisks or periods in the pop-up and press **SELECT**. You will notice how the bit assignment toggles to the opposite state of what it was when the pop-up opened.



4. You close the pop-up by placing the cursor on **Done** and pressing **SELECT**.

Specifying Patterns

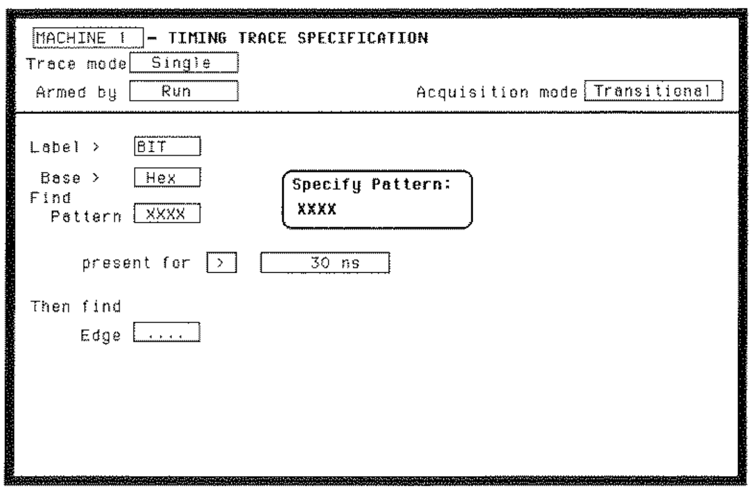
The Specify Patterns fields appear in several menus in both the timing and state analyzers. Patterns can be specified in one of several number bases; however, for now we'll use hexadecimal (HEX) since it is the default base.

Before starting this exercise you need to know how the logic analyzer knows which pattern to ignore (doesn't care about). Whenever you see an "X" in this type of menu, it indicates a "don't care."

To specify patterns:

1. Select the TIMING TRACE SPECIFICATION menu.

2. Place the cursor on the **Find Pattern**__________field and press **SELECT**. You will see the following pop-up menu.



3. Type in 2, 3, 4, and press the **DON'T CARE** key. You will see 234X in the pop-up. This will be the pattern in hexidecimal that you want the logic analyzer to recognize.

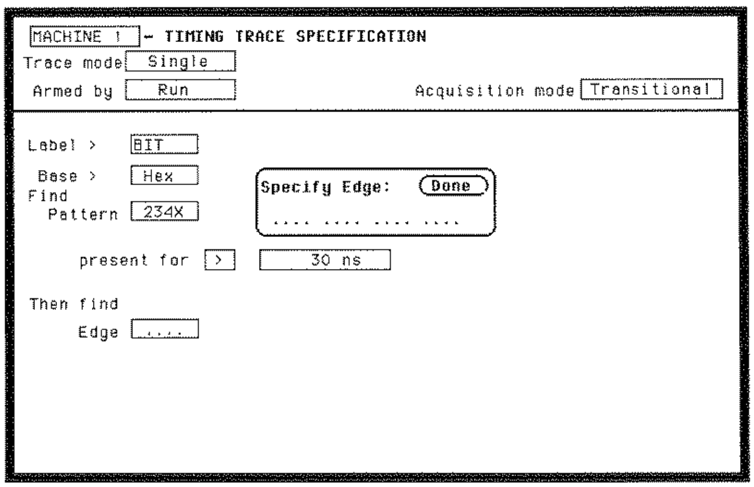
4. Close the pop-up by pressing **SELECT.**

Specifying Edges

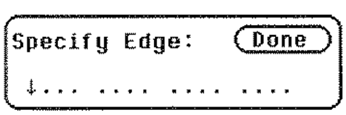
You specify edges in the TIMING TRACE SPECIFICATION menu by following these steps:

1. Press the **TRACE** key. Switch to the timing analyzer if the STATE TRACE SPECIFICATION menu is displayed.

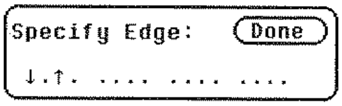
2. Place the cursor on the **Then find Edge . .** field under one of the labels and press **SELECT**. The following pop-up will appear.



You will notice 16 periods in the pop-up menu. Each period represents an unassigned bit for each bit assigned to the label. Don't be alarmed if you have a different number of unassigned bits; it merely means the number of bits in your label is different than the label in this example.



3. Place the cursor on one of the unassigned bit periods and press **SELECT** once. You will now see an arrow pointing down.

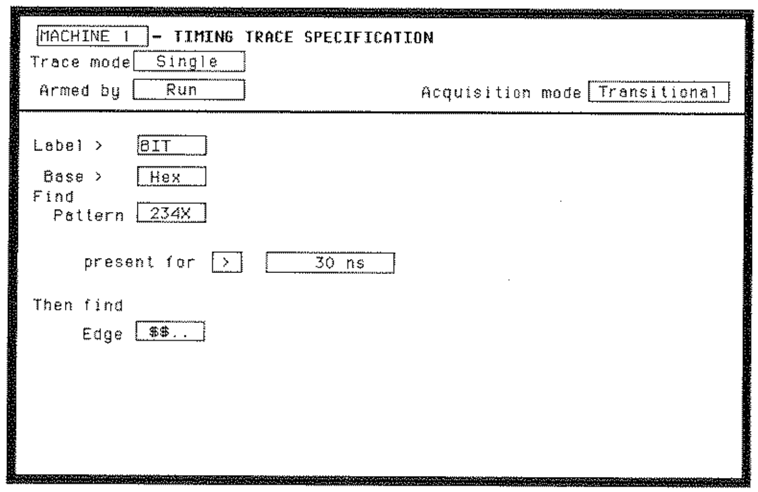


4. Move the cursor to another unassigned bit period and press **SELECT** twice. You will see an arrow pointing up.

5. Move the cursor to yet another unassigned bit period and press **SELECT** three times. You will see an arrow pointing both up and down.

You have just selected a positive-going (↑), negative-going (↓), and either edge (↕) for your edge parameter.

6. Place the cursor on **Done** and press **SELECT**. The pop-up will close and you will see the following display.



Note

When you close the pop-up after specifying edges, you will see dollar signs ($ $ . .) in the Then find Edge field if the logic analyzer can't display the edges correctly. This indicates the logic analyzer can't display the data correctly in the number base you have selected.

Summary

In this chapter you have learned some of the most common pop-up menu types. You will use these pop-up menus as you set up the logic analyzer in the measurement example exercises in chapters 5 through 7.

If you are already familiar with logic analysis and feel you are comfortable enough with the HP 1650B/51B user interface, you may be ready for the *HP 1650B/51B Front-Panel Reference.*

If you are not familiar with logic analyzers or logic analysis, you should continue with this manual.

5

Using the Timing Analyzer

Introduction

In this chapter you will learn how to use the timing analyzer by setting up the logic analyzer to make a simple measurement. We give you the measurement results as actually measured by the logic analyzer, since you may not have the same circuit available.

The exercise in this chapter is organized in a task format. The tasks are ordered in the same way you will most likely use them once you become an experienced user. The steps in this format are both numbered and lettered. The numbered steps state the step objective. The lettered steps explain how to accomplish each step objective. There is also an example of each menu after it has been properly set up.

How you use the steps depends on how much you remember from chapters 1 through 4. If you can set up each menu by just looking at the menu picture, go ahead and do so. If you need a reminder of what steps you need to perform, follow the numbered steps. If you still need more information about "how," use the lettered steps.

When you have finished configuring the logic analyzer for this exercise, you can load a file from the operating system disk. This file configures the logic analyzer the same way it is configured for this exercise. It also loads the same data acquired for this exercise so you can see what it looks like on screen.

In order to learn how to configure the logic analyzer, we recommend that you follow the exercise to "Acquiring the Data" before loading the file from the disk.

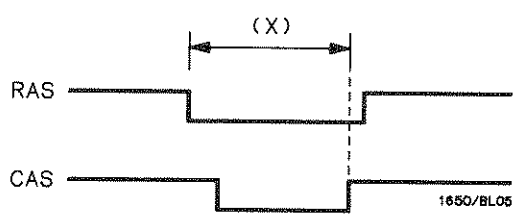
You can also compare your configuration with the one on the disk by printing it (if you have a printer) or making notes before you load the file.

Problem Solving with the Timing Analyzer

In this exercise, assume you are designing a dynamic RAM memory (DRAM) controller and you must verify the timing of the row address strobe (RAS) and the column address strobe (CAS). You are using a 4116 dynamic RAM and the data book specifies that the minimum time from when LRAS is asserted (goes low) to when LCAS is no longer asserted (goes high) is 250 ns. You could use an oscilloscope but you have an HP 1650B/51B on your bench. Since the timing analyzer will do just fine when you don't need voltage parametrics, you decide to go ahead and use the logic analyzer.

What Am I Going to Measure?

After configuring the logic analyzer and hooking it up to your circuit under test, you will be measuring the time (x) from when the RAS goes low to when the CAS goes high, as shown below.



How Do I Configure the Logic Analyzer?

In order to make this timing measurement, you must configure the logic analyzer as a timing analyzer. By following these steps you will configure Analyzer 1 as the timing analyzer.

If you are in the System Configuration menu you are in the right place to get started and you can start with step 2; otherwise, start with step 1.

1. Using the field in the upper left corner of the display, get the system Configuration menu on screen.

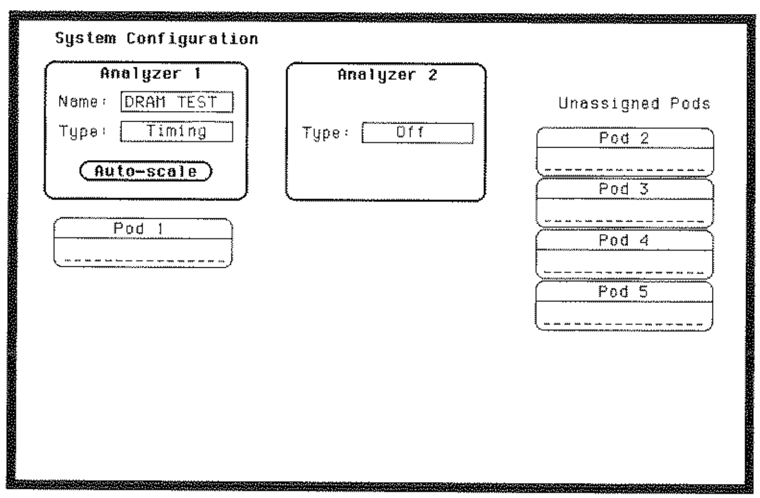
   a. Place the cursor on the field in the upper left corner of the display and press **SELECT.**

   b. Place the cursor on **System** and press **SELECT.**

2. In the System Configuration menu, change Analyzer 1 type to Timing. If analyzer 1 is already a timing analyzer, go on to step 3.

   a. Place the cursor on the **Type:** ________ field and press **SELECT.**

   b. Place the cursor on **Timing** and press **SELECT.**



3. Name Analyzer 1 "**DRAM TEST**" (optional)

   a. Place the cursor on the **Name:** _____field of Analyzer 1 and press **SELECT.**

   b. With the Alpha Entry pop-up, change the name to "DRAM TEST" (see "Alpha Entry Pop-up Menu" in chapter 4 if you need a reminder).

4. Assign pod 1 to the timing analyzer.

   a. Place the cursor on the **Pod 1** field and press **SELECT.**

   b. In the Pod 1 pop-up, place the cursor on **Analyzer 1** and press **SELECT.**

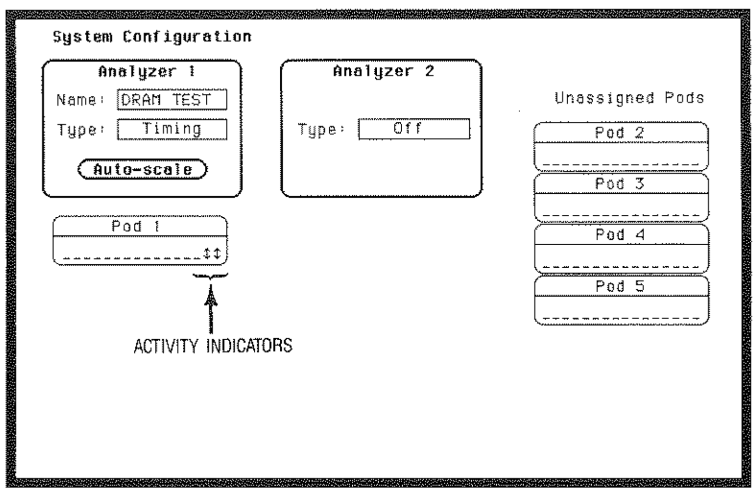
Connecting the Probes

At this point, if you had a target system with a 4116 DRAM memory IC, you would connect the logic analyzer to your system.

Since you will be assigning Pod 1 bit 0 to the RAS label, you connect Pod 1 bit 0 to the memory IC pin connected to the RAS signal. You connect Pod 1 bit 1 to the IC pin connected to the CAS signal.

Activity Indicators

When the logic analyzer is connected and your target system is running, you will see ↕ at the right-most end (least significant bits) of the **Pod 1** field in the System Configuration menu. This indicates the RAS and CAS signals are transitioning.



Configuring the Timing Analyzer

Now that you have configured the system, you are ready to configure the timing analyzer. You will be:

- Creating two names (labels) for the input signals
- Assigning the channels connected to the input signals
- Specifying a trigger condition

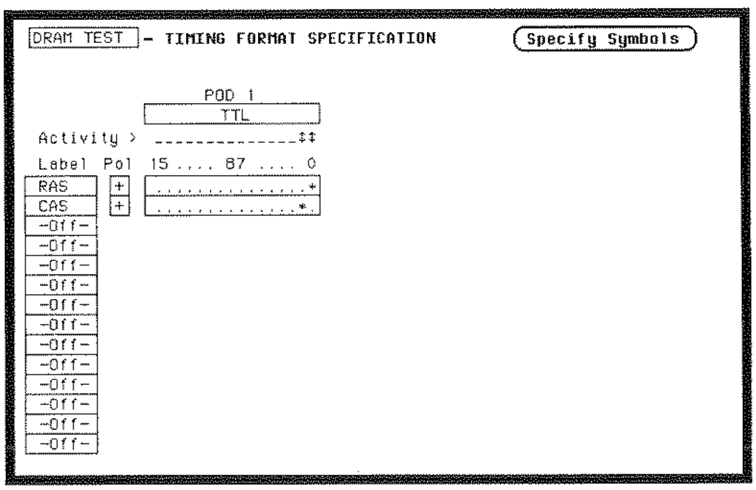
1.Display the TIMING FORMAT SPECIFICATION menu.

a. Press the **FORMAT** key on the front panel.

2.Name two labels, one RAS and one CAS.

a. Place the cursor on the top field in the label column and press **SELECT.**

b. Place the cursor on **Modify label** and press **SELECT.**



c. With the Alpha Entry pop-up, change the name of the label to RAS (see "Alpha Entry Pop-up Menu" in chapter 4 if you need a reminder).

d. Name the second label CAS by repeating steps a through c.

3. Assign the channels connected to the input signals (Pod 1 bits 0 and 1) to the labels RAS and CAS respectively.

a. Place the cursor on the bit assignment field below Pod 1 and to the right of RAS and press **SELECT.**

b. Any combination of bits may be assigned to this pod; however, you will want only bit 0 assigned to the RAS label. The easiest way to assign bits is to press the **CLEAR ENTRY** key to un-assign any assigned bits before you start.

c. Place the cursor on the period under the 0 in the bit assignment pop-up and press **SELECT.** This will place an asterisk in the pop-up for bit 0 indicating Pod 1 bit 0 is now assigned to the RAS label. Place cursor on **Done** and press **SELECT** to close the pop-up.

d. Assign Pod 1 bit 1 to the CAS label by moving the cursor to bit 1 and pressing **SELECT.**

Specifying a Trigger Condition

To capture the data and then place the data of interest in the center of the display of the TIMING WAVEFORMS menu, you need to tell the logic analyzer when to trigger. Since the first event of interest is when the LRAS is asserted (negative-going edge of RAS), you need to tell the logic analyzer to trigger on a negative-going edge of the RAS signal.

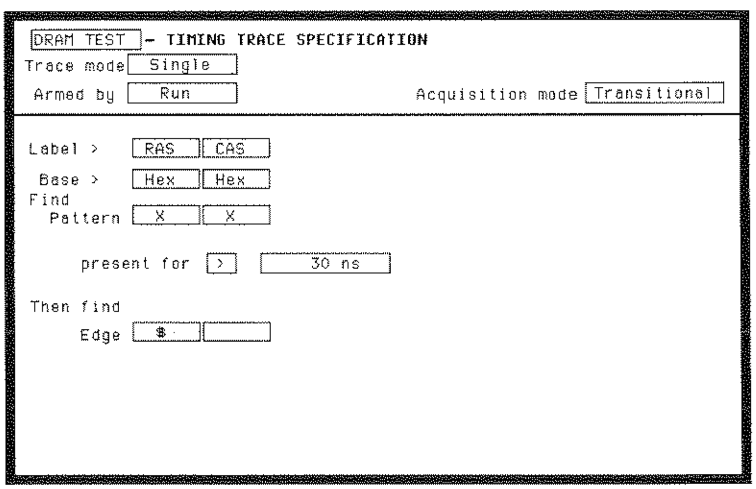
1. Select the TIMING TRACE menu by pressing the **TRACE** key.

2. Set the trigger so that the logic analyzer triggers on the negative-going edge of the RAS.

   a. Place the cursor on the **Then find Edge** field under the label RAS, then press **SELECT.**

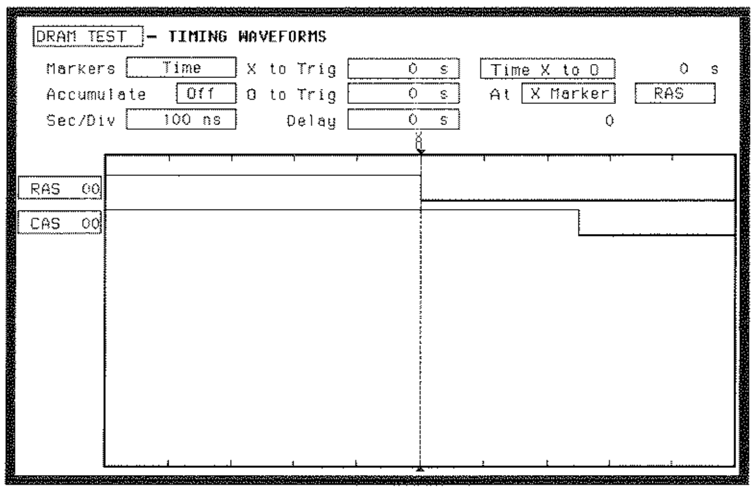
   b. Place the cursor on the **.** (period) in the pop-up and press **SELECT** once. Pressing **SELECT** once in this pop-up changes a period to ↓which indicates a negative- going edge.

   c. Place the cursor on **Done** and press **SELECT.** The pop-up closes and a $ will be located in this field. The $ indicated an edge has been specified even though it can't be shown in the HEX base.



Acquiring the Data

Now that you have configured and connected the logic analyzer, you acquire the data for your measurement by pressing the RUN key. The logic analyzer will look for a negative edge on the RAS signal and trigger if it sees one. When it triggers, the display switches to the TIMING WAVEFORMS menu.



The RAS label shows you the RAS signal and the CAS label shows you the CAS signal. Notice the RAS signal goes low at or near the center of the waveform display area (horizontal center).

Now is the time to load the timing measurement demo file from the disk if you wish. The file name is **TIMINGDEMO.** Follow the procedure in Appendix B to load the file.

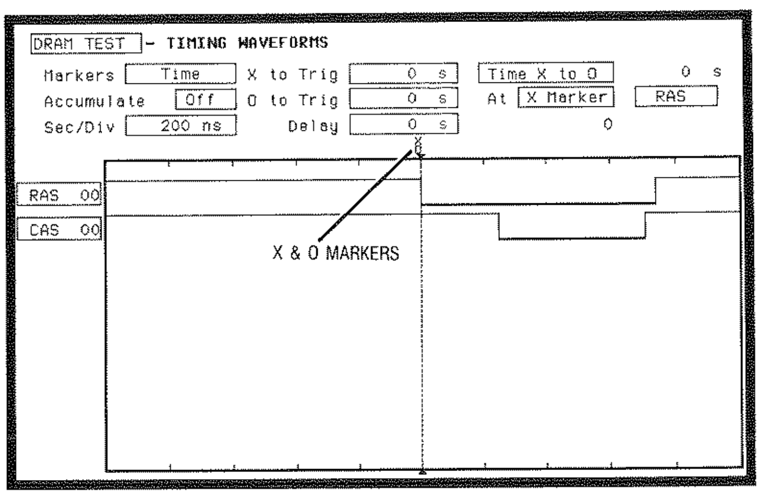
The Timing Waveforms Menu

The TIMING WAVEFORMS menu differs from the other menus you have used so far in this exercise. Besides displaying the acquired data, it has menu fields that you use to change the way the acquired data is displayed and fields that give you timing answers. Before you can use this menu to find answers, you need to know some of the special symbols and their functions. The symbols are:

- The X and O
- The ▼
- The vertical dotted line

The X and O

The X and O are markers you use to find your answer. You place them on the points of interest on your waveforms, and the logic analyzer displays the time between the markers. The X and O markers will be in the center of the display when **X to trig**(ger) and **O to trig**(ger) are both **0.000** s (see example below).

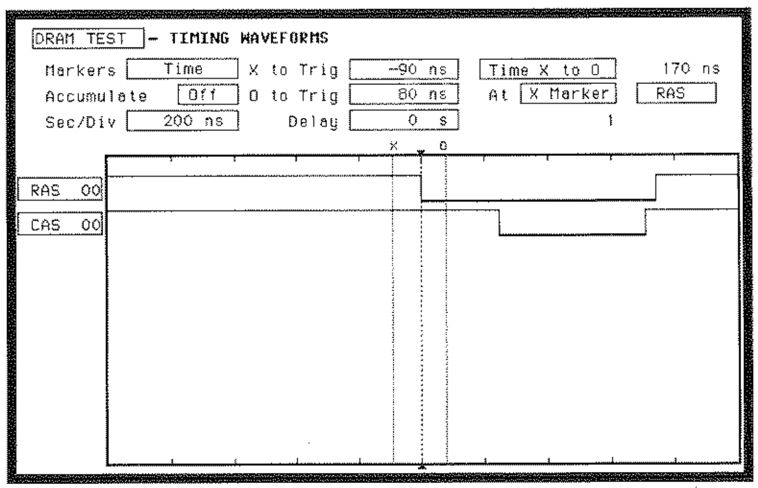


The ▼

The ▼ (inverted triangle) indicates the trace point. Remember, trace point = trigger + delay. Since delay in this example is 0.000 s, you will see the negative-going edge of the RAS signal at center screen under the ▼.

The Vertical Dotted Line

The vertical dotted line indicates the trigger point you specified in the TIMING TRACE SPECIFICATION menu. The vertical dotted line is at center screen under the ▼ and is superimposed on the negative-going edge of the RAS signal as shown.

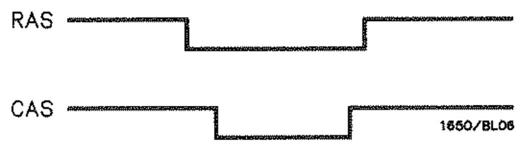


Configuring the Display

Now that you have acquired the RAS and CAS waveforms, you need to configure the TIMING WAVEFORMS menu for best resolution and to obtain your answer.

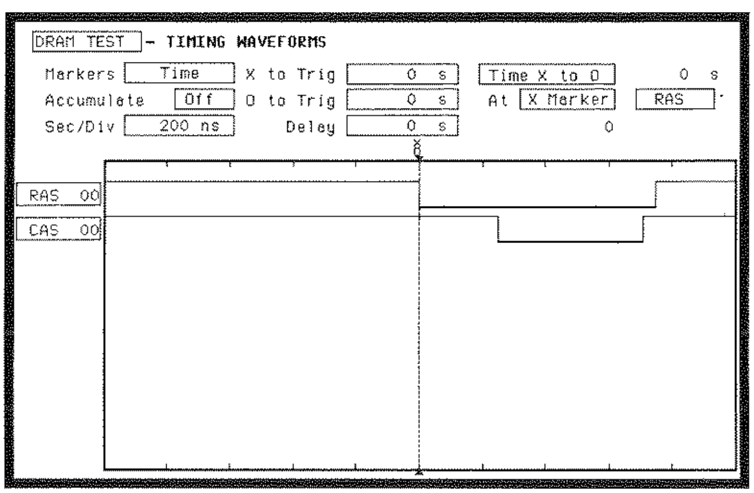
Display Resolution

You get the best resolution by changing the **Sec/Div** to a value that displays one negative-going edge of both the RAS and CAS waveforms. Set the **Sec/Div** by following these steps.



1. Place the cursor on **Sec/Div** and press **SELECT.** The Sec/Div pop-up appears, showing you the current setting.

2. While the pop-up is present, rotate the **KNOB** until your waveform shows you only one negative-going edge of the RAS waveform and one positive-going edge of the CAS waveform (see above). In this example 200 ns is best.



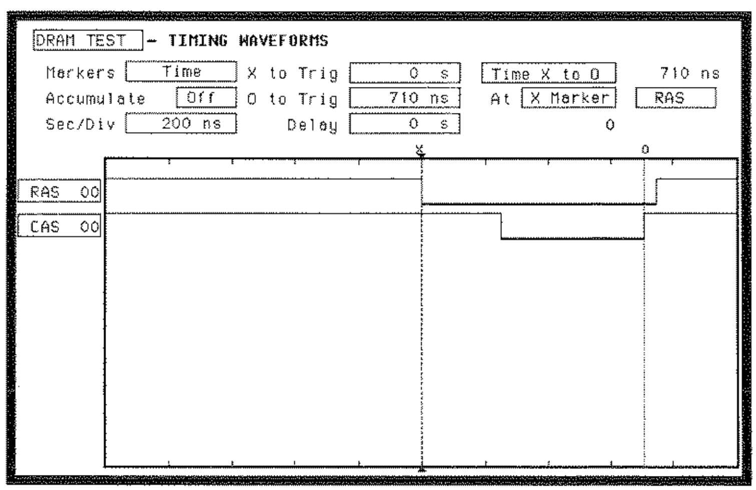
Making the Measurement

What you want to know is how much time elapses between the time RAS goes low and the time CAS goes high again. You will use the X and O markers to quickly find the answer. Remember, you specified the negative-going edge of the RAS to be your trigger point; therefore, the X marker should be on this edge if **X to Trig** = 0. If not, follow steps 1 and 2.

1. Place the cursor on the **X to Trig** field and press **SELECT.** A pop-up will appear showing you the current time from the X marker to the trigger; however, you don't need to worry about this number now.

2. Rotate the **KNOB** to place the X marker on the negative-going edge of the RAS waveform and press **SELECT.** The pop-up closes and displays **X to Trig** = 0.000 s.

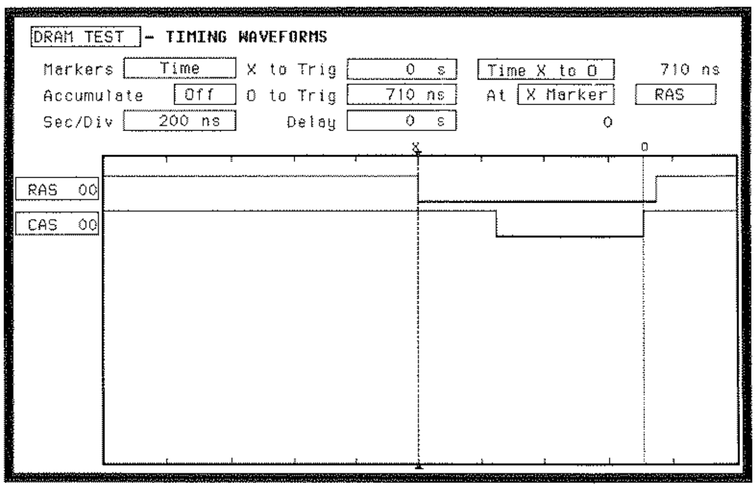
3. Place the cursor on **O to Trig** and press **SELECT.** Repeat step 2 except place the O maker on the positive-going edge of the CAS waveform and press **SELECT.** The pop-up closes and displays **O to Trig** = 710 ns.



Finding the Answer

Your answer could be calculated by adding the **X to Trig** and **O to Trig** times, but you don't need to bother. The logic analyzer has already calculated this answer and displays it in the **Time X to O**_____ field.

This example indicated the time is 710 ns. Since the data book specifies a minimum of 250 ns, it appears your DRAM controller circuit is designed properly.



Summary

You have just learned how to make a simple timing measurement with the HP 1650B/51B logic analyzer. You have:

- specified a timing analyzer
- assigned pod 1
- assigned bits
- assigned labels
- specified a trigger condition
- learned which probes to connect
- acquired the data
- configured the display
- set the Sec/Div for best resolutions
- positioned the markers for the measurement answer

You have seen how easy it is to use the timing analyzer to make timing measurements that you could have made with a scope. You can use the timing analyzer for any timing measurement that doesn't require voltage parametrics or doesn't go beyond the accuracy of the timing analyzer.

The next chapter teaches you how to use the state analyzer. You will go through a simple state measurement in the same way you did the timing measurement in this chapter.

6

Using the State Analyzer

Introduction

In this chapter you will learn how to use the state analyzer by setting up the logic analyzer to make a simple state measurement. We give you the measurement results as actually measured by the logic analyzer, since you may not have the same circuit available.

The exercise in this chapter is organized in a task format. The tasks are in the same order you will most likely use them once you become experienced. The steps in this format are both numbered and lettered. The numbered steps state the step objective. The lettered steps explain how to accomplish each step objective. There is also an example of each menu after it has been properly set up.

How you use the steps depends on how much you remember from chapters 1 through 4. If you can set up each menu by just looking at the menu picture, go ahead and do so. If you need a reminder of what steps to perform, follow the numbered steps. If you still need more information about "how," use the lettered steps.

When you have finished configuring the logic analyzer for this exercise, you can load a file from the operating system disk. This file configures the logic analyzer the same way it is configured for this exercise. It also loads the same data acquired for this exercise so you can see what it looks like on screen.

In order to learn how to configure the logic analyzer, we recommend that you follow the exercise to "Acquiring the Data" before loading the file from the disk.

You can also compare your configuration with the one on the disk by printing it (if you have a printer) or making notes before you load the file.

Problem Solving with the State Analyzer

In this example assume you have designed a microprocessor controlled circuit. You have completed the hardware, and the software designer has completed the software and programmed the ROM (read-only memory). When you turn your circuit on for the first time, your circuit doesn't work properly. You have checked the power supply voltages and the system clock and they are working properly.

Since the circuit has never worked before, you and the software engineer aren't sure if it is a hardware or software problem. You need to do some testing to find a solution.

What Am I Going to Measure?

You decide to start where the microprocessor starts when power is applied. We will describe a 68000 microprocessor; however, every processor has similar start-up routines.

When you power up a 68000 microprocessor, it is held in reset for a specific length of time before it starts doing anything to stabilize the power supplies. The time the microprocessor is held in reset ensures stable levels (states) on all the devices and buses in your circuit. When this reset period has ended, the 68000 performs a specific routine called "fetching the reset vector."

The first thing you check is the time the microprocessor is held in reset. You find the time is correct. The next thing to check is whether the microprocessor fetches the reset vector properly.

The steps of the 68000 reset vector fetch are:

1. Set the stack pointer to a location you specify, which is in ROM at address locations 0 and 2.

2. Find the first address location in memory where the microprocessor fetches its first instruction. This is also specified by you and stored in ROM at address locations 4 and 6.

What you decide to find out is:

1. What ROM address does the microprocessor look at for the location of the stack pointer, and what is the stack pointer location stored in ROM?

2. What ROM address does the microprocessor look at for the address where its first instruction is stored in ROM, and is the instruction correct?

3. Does the microprocessor then go to the address where its first instruction is stored?

4. Is the executable instruction stored in the first instruction location correct?

Your measurement, then, requires verification of the sequential addresses the microprocessor looks at, and of the data in ROM at these addresses. If the reset vector fetch is correct (in this example), you will see the following list of numbers in HEX (default base) when your measurement results are displayed.

```
+0000 000000 0000
+0001 000002 04FC
+0002 000004 0000
+0003 000006 8048
+0004 008048 3E7C
```

This list of numbers will be explained in detail later in this chapter in "The State Listing."

How Do I Configure the Logic Analyzer?

In order to make this state measurement, you must configure the logic analyzer as a state analyzer. By following these steps you will configure Analyzer 1 as the state analyzer.

If you are in the System Configuration menu you are in the right place to get started and you can start with step 2; otherwise, start with step 1.

1. Using the field in the upper left corner of the display, get the System Configuration menu on screen.

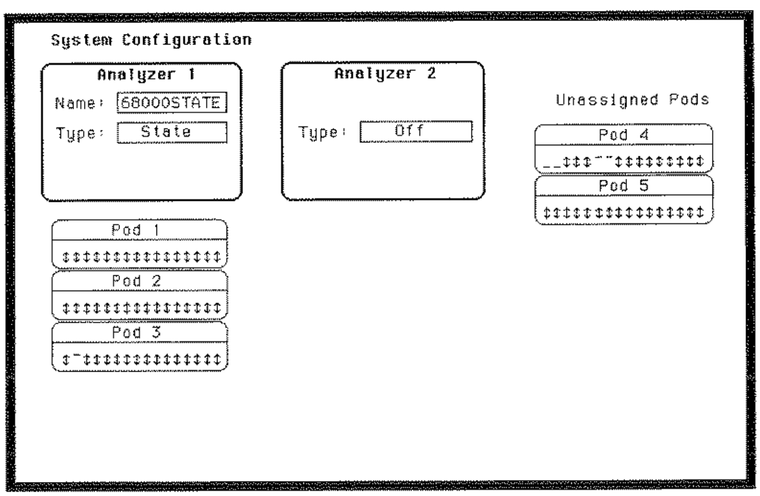
   a. Place the cursor on the field in the upper left corner of the display and press **SELECT.**

   b. Place the cursor on **System** and press **SELECT.**

2. In the System Configuration menu, change the Analyzer 1 type to State. If Analyzer 1 is already a state analyzer, go on to step 3.

   a. Place the cursor on the **Type:**_______ and press **SELECT.**

   b. Place the cursor on **State** and press **SELECT.**



3. Name Analyzer 1 **68000STATE** (optional)

   a. Place the cursor on the **Name:______** field of Analyzer 1 and press **SELECT.**

   b. With the Alpha Entry pop-up, change the name to **68000STATE** (see "Alpha Entry Pop-up Menu" in chapter 4 if you need a reminder).

4. Assign pods 1, 2, and 3 to the state analyzer.

   a. Place the cursor on the **Pod 1** field and press **SELECT.**

   b. In the Pod 1 pop-up, place the cursor on **Analyzer 1** and press **SELECT.**

   c. Repeat steps a and b for pods 2 and 3.

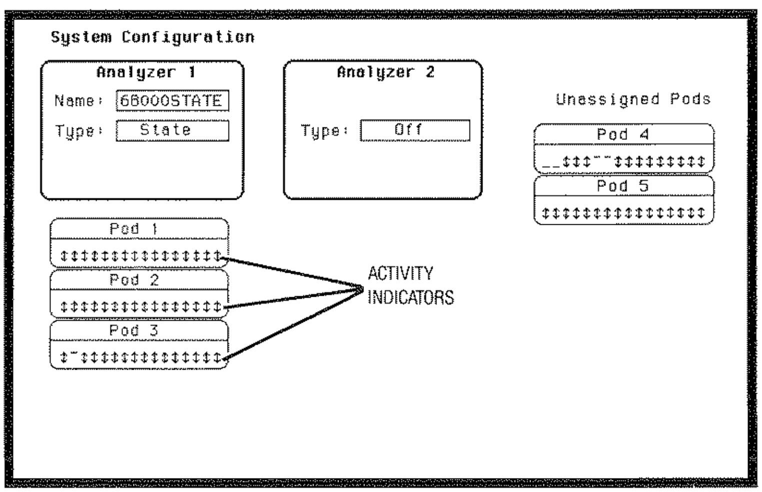
Connecting the Probes

At this point, if you had a target system with a 68000 microprocessor, you would connect the logic analyzer to your system. Since you will be assigning labels **ADDR** and **DATA**, you connect the probes to your system accordingly.

- Pod 1 probes 0 through 15 to the data bus lines D0 through D15.
- Pod 2 probes 0 through 15 to the address bus lines A0 through A15.
- Pod 3 probes 0 through 7 to the address bus lines A16 through A23.
- Pod 1, **CLK** (**J** clock) to the address strobe (LAS).

Activity Indicators

When the logic analyzer is connected and your target system is running, you will see ↕ in the Pod 1, 2, and 3 fields of the System Configuration menu. This indicates which signal lines are transitioning.



Configuring the State Analyzer

Now that you have configured the system, you are ready to configure the state analyzer. You will be:

- Creating two names (labels) for the input signals
- Assigning the channels connected to the input signals
- Specifying the State (J) clock
- Specifying a trigger condition

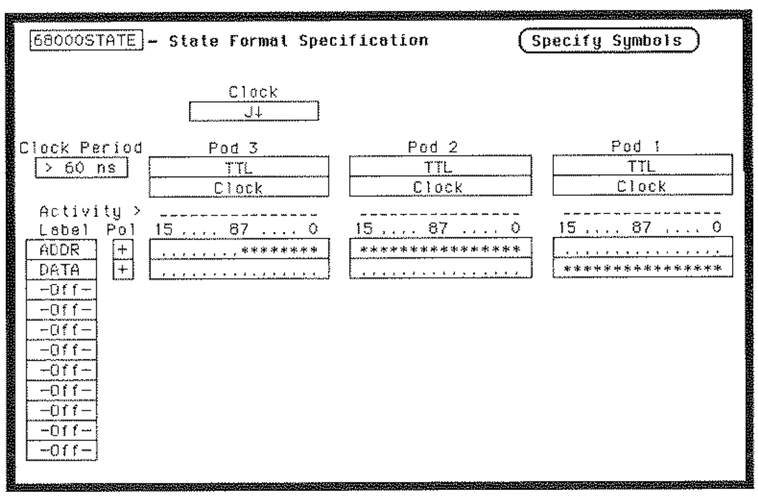
1. Display the STATE FORMAT SPECIFICATION menu.

   a. Press the **FORMAT** key on the front panel.

2. Name two labels, one **ADDR** and one **DATA.**

   a. Place the cursor on the top field in the label column and press **SELECT.**

   b. Place the cursor on **Modify label** and press **SELECT.**



c. With the Alpha Entry pop-up, change the name of the label to **ADDR** (see "Alpha Entry Pop-up Menu" in chapter 4 if you need a reminder).

d. Name the second label **DATA** by repeating steps a through c.

3. Assign Pod 1 bits 0 through 15 to the label DATA.

a. Place the cursor on the bit assignment field below Pod 1 and to the right of **DATA** and press **SELECT.**

b. Any combination of bits may already be assigned to this pod; however, you will want all 16 bits assigned to the **DATA** label. The easiest way to assign is to press the **CLEAR ENTRY** key to un-assigned any assigned bits before you start.

c. Place the cursor on the period under the 15 in the bit assignment pop-up and press **SELECT.** This will place an asterisk in the pop-up for bit 15, indicating Pod 1 bit 15 is now assigned to the **DATA** label. Repeat this procedure until all 16 bits have an asterisk under each bit number. Place the cursor on **Done** and press **SELECT** to close the pop-up.

d. Repeat step c for Pod 2 and the **ADDR** label to assign all 16 bits.

e. Repeat step c except you will assign the lower eight bits (0 - 7) of Pod 3 to the **ADDR** label.

Specifying the J Clock

If you remember from "What's a State Analyzer" in *Feeling Comfortable With Logic Analyzers,* the state analyzer samples the data under the control of an external clock, which is "synchronous" with your circuit under test. Therefore, you must specify which clock probe you will use for your measurement. In this exercise, you will use the **J** clock, which is accessible through pod 1.

1. Select the STATE FORMAT SPECIFICATION menu by pressing the **FORMAT** key.

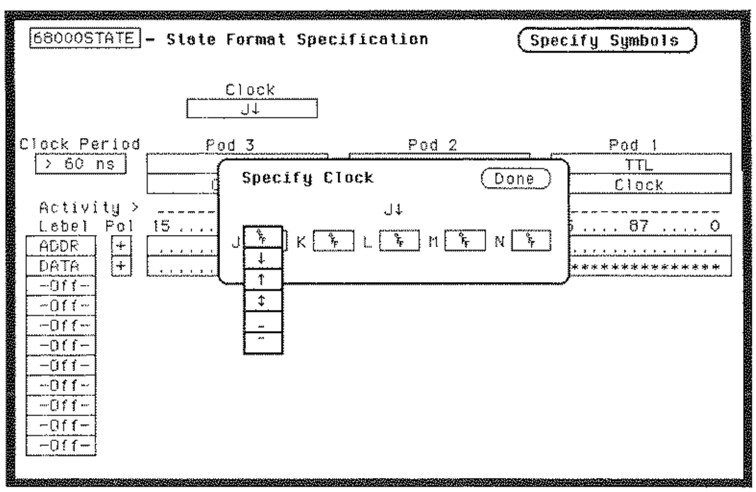
2. Set the **J** Clock to sample on a negative-going edge.

   a. Place the cursor on the **CLOCK** field and press **SELECT.**

   b. Place the cursor on the box just to the right of **J** in the pop-up (labeled **OFF**) and press **SELECT.**

   c. Place the cursor on ↓ and press **SELECT.**

   d. Place the cursor on **Done** and press **SELECT.**



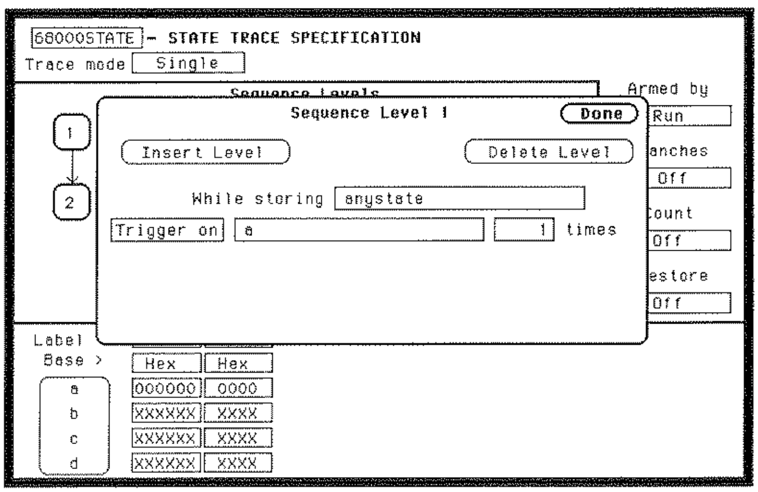
Specifying a Trigger Condition

To capture the data and place the data of interest in the center of the display of the STATE LISTING menu, you need to tell the state analyzer when to trigger. Since the first event of interest is address 0000, you need to tell the state analyzer to trigger when it detects address 0000 on the address bus.

1. Select the STATE TRACE SPECIFICATION menu by pressing the **TRACE** key.

2. Set the trigger so that the state analyzer triggers on address 0000.

   a. Place the cursor on the **1** in the **Sequence Levels** field of the menu and press **SELECT.**



   b. Place the cursor on the **anystate** field to the right of the **Trigger on** field and press **SELECT.** Another pop-up appears showing you a list of "trigger on" options. Options **a** through **h** are qualifiers. You can assign them a pattern for the trigger specification.

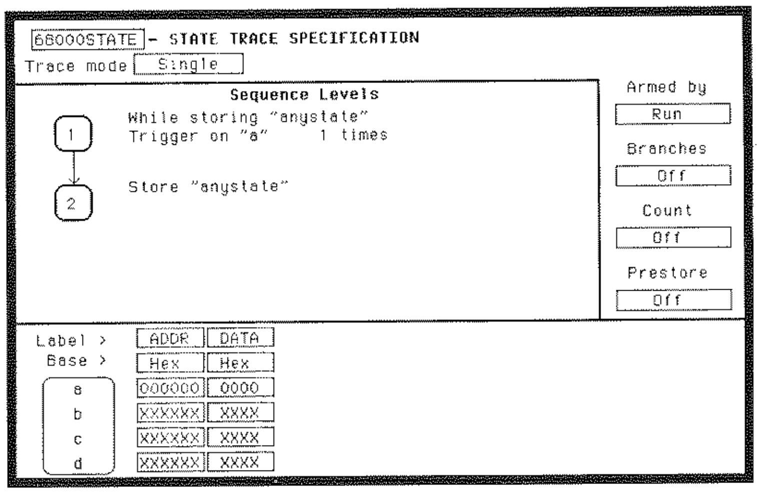
c. Place the cursor on the **a** option and press **SELECT.**

d. Place the cursor on **Done** in the **Sequence Levels** pop-up and press **SELECT.**

e. Place the cursor on the field to the right of the **a** under the label **ADDR** and press **SELECT.**

f. With the keypad, press 0 (zero) until there are all zeros in the **Specify Pattern:** pop-up and then press **SELECT.**

Your trigger specification now states: "While storing anystate, trigger on "a" once and then store anystate."



When the state analyzer is connected to your circuit and is acquiring data, it continuously stores until it sees 0000 on the address bus, then it will store anystate until the analyzer memory is filled.

Acquiring the Data

Since you want to capture the data when the microprocessor sends address 0000 on the bus after power-up, you press the **RUN** key to arm the state analyzer and then force a reset of your circuit. When the reset cycle ends, the microprocessor should send address 0000, trigger the state analyzer and switch the display to the STATE LISTING menu.

We'll assume this is what happens in this example, since the odds that the microprocessor won't send address 0000 are very low.

68000STATE - STATE LISTING

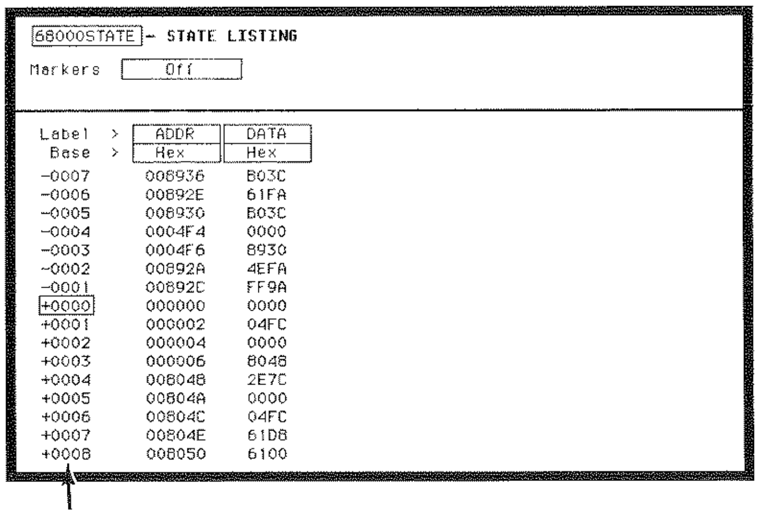
Markers Off

Label >	ADDR	DATA	
Base >	Hex	Hex	
-0007	008936	B03C	
-0006	00892E	61FA	
-0005	008930	B03C	
-0004	0004F4	0000	
-0003	0004F6	8930	
-0002	00892A	4EFA	
-0001	00892C	FF9A	
+0000	000000	0000	
+0001	000002	04FC	
+0002	000004	0000	RESET VECTOR FETCH ROUTINE
+0003	000006	8048	
+0004	008048	2E7C	
+0005	00804A	0000	
+0006	00804C	04FC	
+0007	00804E	61D8	
+0008	008050	6100	

Now is the time to load the state measurement demo file from the disk if you wish. The file name is **STATEDEMO.** Follow the procedure in Appendix B to load the file.

The State Listing

The state listing displays three columns of numbers as shown:



STATE LOCATIONS

The first column of numbers are the state line number locations as they relate to the trigger point. The trigger state is on line +0000 in the vertical center of the list area. The negative numbers indicate states occurring before the trigger and the positive numbers indicate states occurring after the trigger.

The second column of numbers are the states (listed in HEX) the state analyzer sees on the address bus. This column is labeled **ADDR.**

The third column of numbers are the states (listed in HEX) the state analyzer sees on the data bus. This column is labeled **DATA.**

Summary

You have just learned how to make a simple state measurement with the HP 1650B Logic Analyzer. You have:

- specified a state analyzer
- learned which probes to connect
- assigned pods 1, 2, and 3
- assigned labels
- assigned bits
- specified the J clock
- specified a trigger condition
- acquired the data
- interpreted the state listing

You have seen how easy it is to use the state analyzer to capture the data on the address and data buses. You can use this same technique to capture and display related data on the microprocessor status, control, and various strobe lines. You are not limited to using this technique on microprocessors. You can use this technique any time you need to capture data on multiple lines and need to sample the data relative to a system clock.

The next chapter teaches you how to use the logic analyzer as an interactive timing and state analyzer. You will see a simple measurement that shows you both timing waveforms and state listings and how they are correlated.

If you have an HP 1651B, you do not have enough channels to simultaneously capture all the data for a 68000. But, since you probably aren't working with 16-bit microprocessors, this example is still valuable because it shows you how to make the same kind of measurement on an eight-bit microprocessor.

7

Using the Timing/State Analyzer

Introduction

In this chapter you will learn how to use the timing and state analyzers interactively by setting up the logic analyzer to make a simple measurement. We give you the measurement results as actually measured by the logic analyzer, since you may not have the same circuit available.

The exercise in this chapter is organized differently than the exercises in the two previous chapters. Since you have already set up both the timing and state analyzers, you should be ready to set them up for this measurement by looking at the menu pictures.

Any new set-ups in this exercise will be explained in task format steps like the previous chapters.

How you use the steps depends on how much you remember from chapters 1 through 4. If you can set up each menu by just looking at the menu picture, go ahead and do so. If you need a reminder of what steps to perform, follow the numbered steps. If you still need more information about "how," use the lettered steps.

When you have finished configuring the logic analyzer for this exercise, you can load a file from the operating system disk. This file configures the logic analyzer the same way it is configured for this exercise. It also loads the same data acquired for this exercise so you can see what it looks like on screen.

In order to learn how to configure the logic analyzer, we recommend that you follow the exercise to "Acquiring the Data" before loading the file from the disk.

You can also compare your configuration with the one on the disk by printing it (if you have a printer) or making notes before you load the file.

Problem Solving with the Timing/State Analyzer

In this example assume you have designed a microprocessor-controlled circuit. You have completed the hardware, and the software designer has completed the software and programmed the ROM (read-only memory). When you turn your circuit on for the first time, your circuit doesn't work properly. You have checked the power supply voltages and the system clock, and they are working properly.

Since the circuit has never worked before, you and the software engineer aren't sure if it is a hardware or software problem. You need to do some testing to find a solution.

You also notice the circuit fails intermittently. More specifically, it only fails when the microprocessor attempts to address a routine that starts at address 8930,

What Am I Going to Measure?

To see what might be causing the failure, you decide to start where the microprocessor goes to the routine that starts at address 8930.

The first thing you check is whether the microprocessor actually addresses address 8930. The next thing you check is whether the code is correct in all the steps in this routine.

Your measurement, then, requires verification of:

- whether the microprocessor addresses location 8930
- whether all the addresses within the routine are correct
- whether all the data at the addresses in the routine are correct

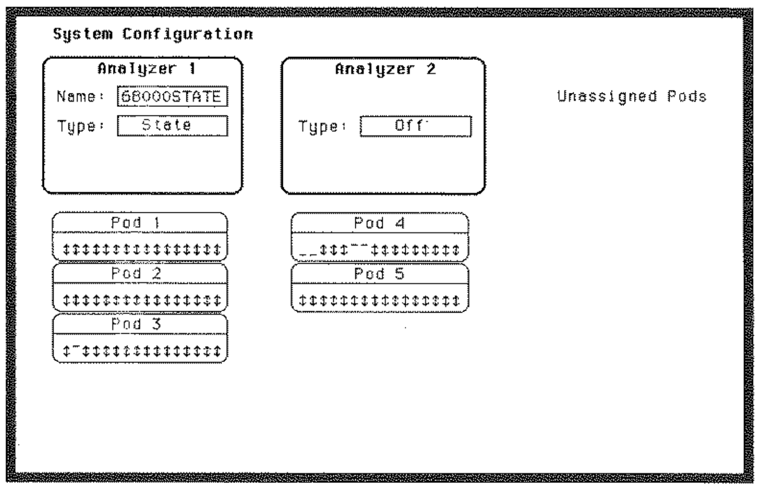
If the routine is correct, the state listing will display:

```
+0000  008930  B03C
+0001  008932  61FA
+0002  008934  67F8
+0003  008936  B03C
+0004  00892E  61FA
```

How Do I Configure the Logic Analyzer?

In order to make this measurement, you must configure the logic analyzer as a state analyzer because you want to trigger on a specific state (8930). You also want to verify that the addresses and data are correct in the states of this routine.

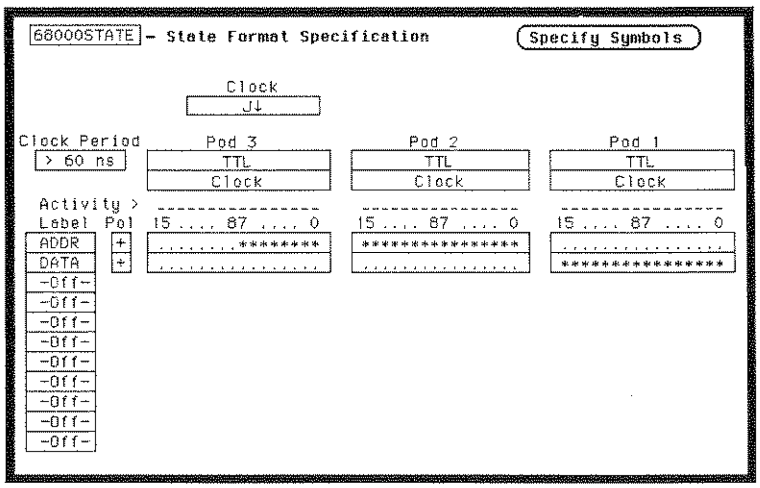
Configure the logic analyzer so that Analyzer 1 is a state analyzer as shown:



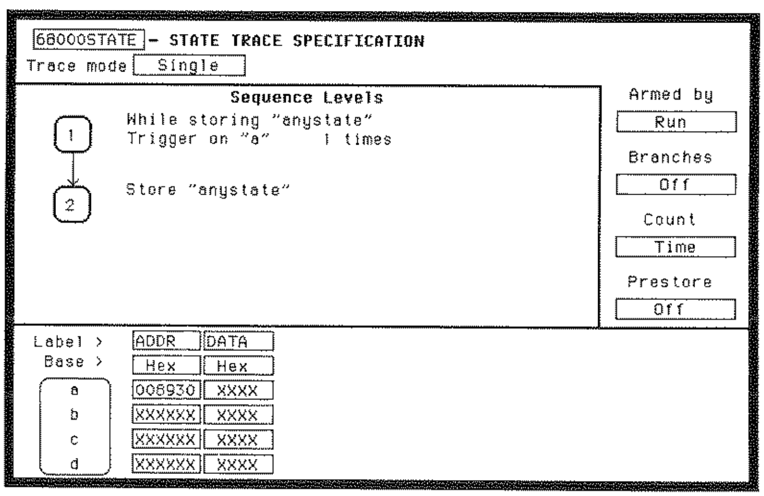
Configuring the State Analyzer

Now that you have configured the system, you are ready to configure the state analyzer.

Configure the STATE FORMAT SPECIFICATION menu as shown:



Configure the STATE TRACE SPECIFICATION menu as shown:



Connecting the Probes

At this point, if you had a target system with a 68000 microprocessor, you would connect the logic analyzer to your system. Since you will be assigning labels **ADDR** and **DATA**, you will hook the probes to your system accordingly.

- Pod 1 probes 0 through 15 to the data bus lines D0 through D15
- Pod 2 probes 0 through 15 to the address bus lines A0 through A15
- Pod 3 probes 0 through 7 to the address bus lines A16 through A23
- Pod 1, **CLK** (J clock) to the address strobe (LAS)

Acquiring the Data

Since you want to capture the data when the microprocessor sends address 8930 on the bus, you press the RUN key to arm the state analyzer. If the microprocessor sends address 8930, it will trigger the state analyzer and switch the display to the STATE LISTING menu.

We'll assume this is what happens in this example.

Finding the Problem

You look at this listing to see what the data is in states +0000 through +0004. You know your routine is five states long.

The 68000 does address location 8930, so you know that the routine is addressed. Now you need to compare the state listing with the following correct addresses and data:

+0000	008930	B03C
+0001	008932	61FA
+0002	008934	67F8
+0003	008936	B03C
+0004	00892E	61FA

As you compare the state listing (shown below) with the above data, you notice the data at address 8932 is incorrect. Now you need to find out why.

68000STATE - STATE LISTING

Markers Off

Label >	ADDR	DATA	
Base >	Hex	Hex	
-0007	0088CA	00FF	
-0006	0088CC	6730	
-0005	0088CE	48E7	
-0004	0088FE	4E75	
-0003	008900	3000	
-0002	0002B4	0000	
-0001	0002B6	8930	
+0000	008930	B03C	
+0001	008932	00FF	← INCORRECT DATA
+0002	008934	67F8	
+0003	008936	B03C	
+0004	00892E	61FA	
+0005	008930	B03C	
+0006	0002B4	0000	
+0007	0002B6	8930	
+0008	00892A	4EFA	

Your first assumption is that incorrect data is stored to this memory location. Assume this routine is in ROM since it is part of the operating system for your circuit. Since the ROM is programmed by the software designer, you have the software designer verify whether or not the data at address 8932 is correct. The software designer tells you that the data is correct. Now what do you do?

Now it's time to look at the hardware to see if it is causing incorrect data when the microprocessor reads this memory address. You decide you want to see what is happening on the address and data buses during this routine in the time domain.

In order to see the time domain, you need the timing analyzer.

What Additional Measurements Must I Make?

Since the problem exists during the routine that starts at address 8930, you decide you want to see the timing waveforms on the address and data bus when the routine is running. You also want to see the control signals that control the read cycle. You will then compare the waveforms with the timing diagrams in the 68000 data book.

Your measurement, then, requires verification of:

- correct timing of the control signals
- stable addresses and data during the memory read

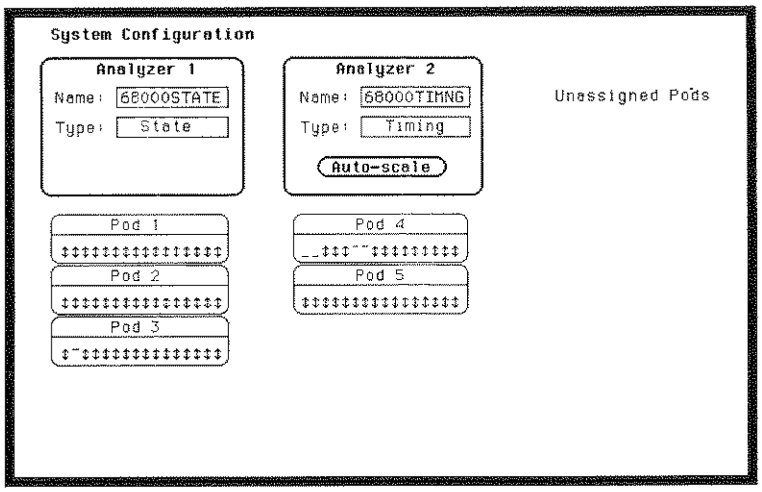
The control signals you must check are:

- system clock
- address strobe (AS)
- lower and upper data strobes (LDS and UDS)
- data transfer acknowledge (DTACK)
- read/write (R/W)

How Do I Re-configure the Logic Analyzer?

In order to make this measurement, you must re-configure the logic analyzer so Analyzer 2 is a timing analyzer. You leave Analyzer 1 as a state analyzer since you will use the state analyzer to trigger on address 8930.

Configure the logic analyzer so Analyzer 2 is a timing analyzer as shown:



Connecting the Timing Analyzer Probes

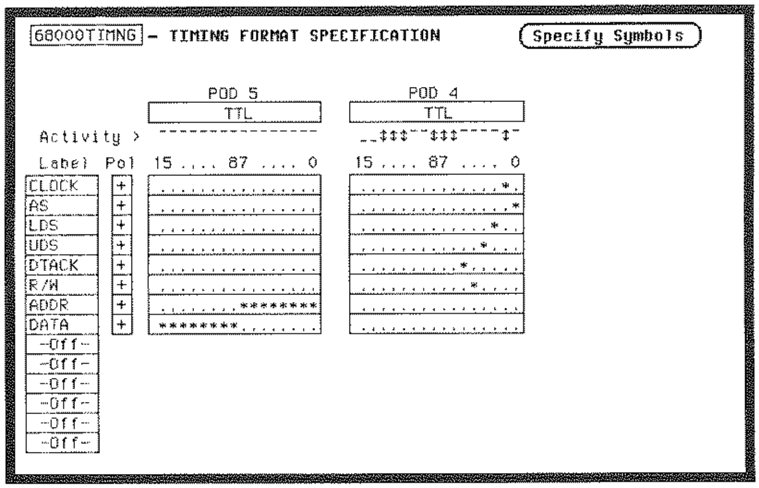
At this point you would connect the probes of pods 4 and 5 as follows:

- Pod 4 bit 0 to address strobe (AS)
- Pod 4 bit 1 to the system clock
- Pod 4 bit 2 to low data strobe (LDS)
- Pod 4 bit 3 to upper data strobe (UDS)
- Pod 4 bit 4 to the read/write (R/W)
- Pod 4 bit 5 to data transfer acknowledge (DTACK)
- Pod 5 bits 0 through 7 to address lines A0 through A7
- Pod 5 bits 8 through 15 to data lines D0 through D7

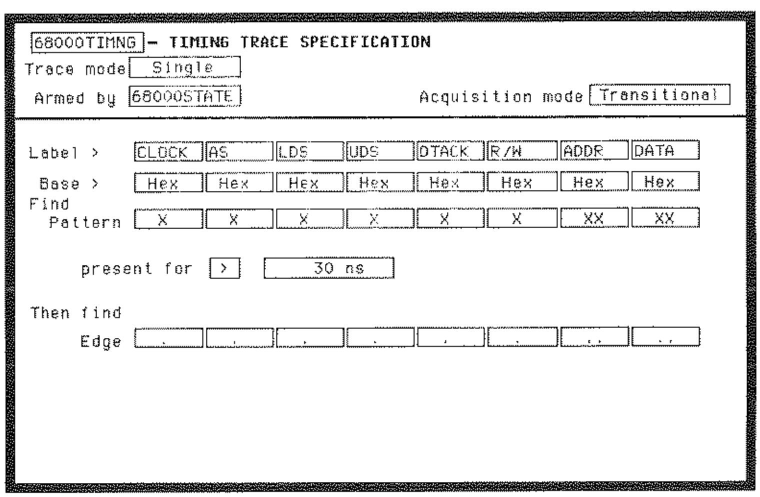
Configuring the Timing Analyzer

Now that you have configured the system, you are ready to configure the timing analyzer.

Configure the TIMING FORMAT SPECIFICATION menu as shown:



Configure the TIMING TRACE SPECIFICATION as shown:



Setting the Timing Analyzer Trigger

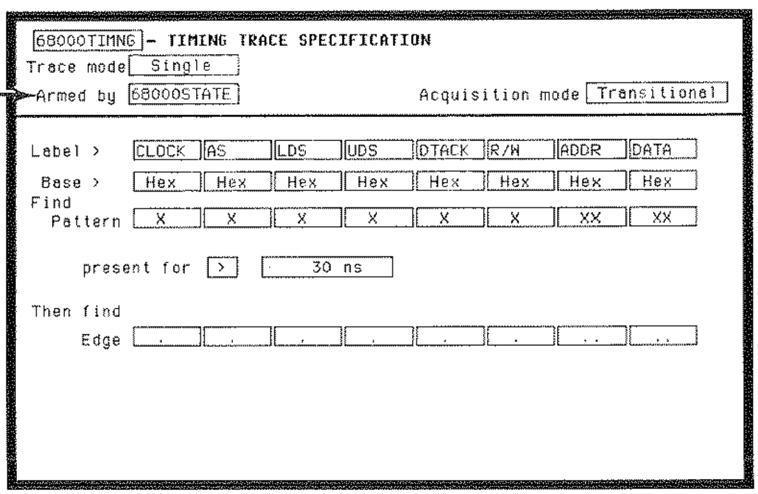
Your timing measurement requires the timing analyzer to display the timing waveforms present on the buses when the routine is running. Since you triggered the state analyzer on address 8930, you want to trigger the timing analyzer so the timing waveforms can be time correlated with the state listing.

To set up the logic analyzer so that the state analyzer triggers the timing analyzer, perform these steps:

1. Display the **TIMING TRACE SPECIFICATION** menu.
2. Place the cursor on the **Armed by** _____ field and press **SELECT.**
3. Place the cursor on the **68000STATE** option in the pop-up and press **SELECT.**

Your timing trace specification should match the menu shown:

STATE ANALYZER ARMS TIMING ANALYZER

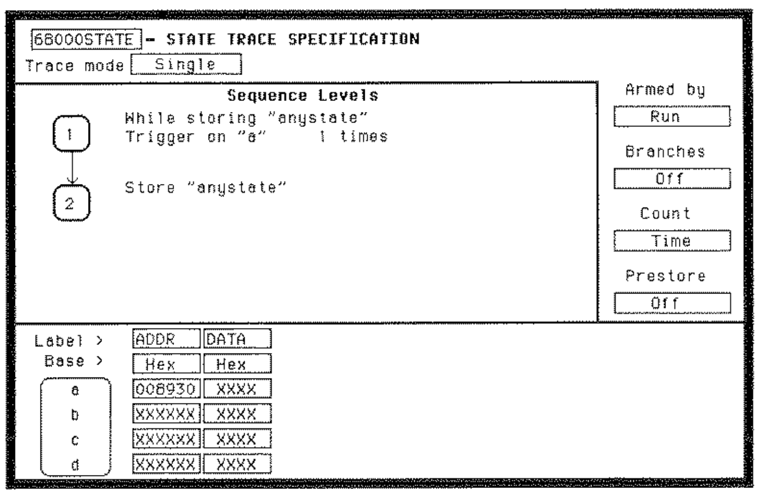


Time Correlating the Data

In order to time correlate the data, the logic analyzer must store the timing relationships between states. Since the timing analyzer samples asynchronously and the state analyzer samples synchronously, the logic analyzer must use the stored timing relationship of the data to reconstruct a time correlated display.

To set up the logic analyzer to keep track of these timing relationships, turn on a counter in the STATE TRACE SPECIFICATION menu. The following steps show you how;

1. Display the **STATE TRACE SPECIFICATION** menu.
2. Place the cursor in the field just below **Count** on the right side of the display and press **SELECT.**
3. Place the cursor on the **Time** option and press **SELECT.** The counter will now be able to keep track of time for the time correlation.



Re-acquiring the Data

After you connect the probes of pods 4 and 5 to your circuit, all you have to do is press **RUN**. When the logic analyzer acquires the data, it switches the display to the STATE LISTING menu unless you switched one of the other menus to the timing analyzer after reconfiguring the STATE TRACE menu. Regardless of which menu is displayed, change the display to the **Mixed mode.**

Now is the time to load the mixed measurement demo file from the disk if you wish. The file name is **MIXEDDEMO.** Follow the procedure in Appendix B to load the file.

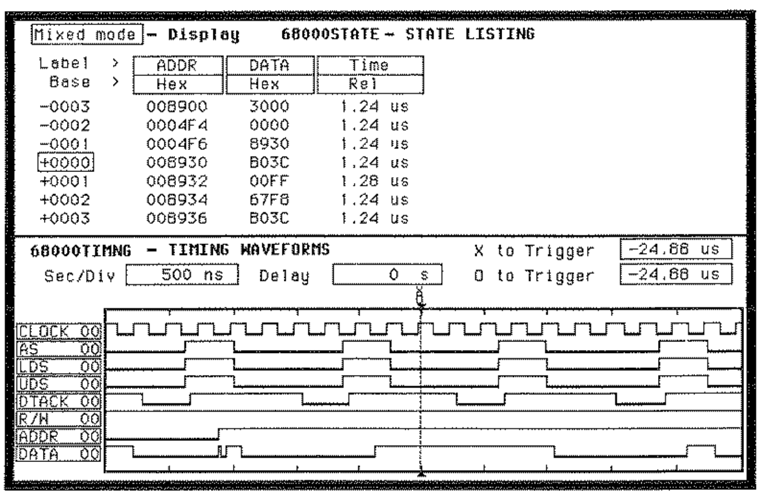
Mixed Mode Display

The **Mixed mode** display shows you both the STATE LISTING and TIMING WAVEFORMS menus simultaneously. To change the display to the **Mixed mode:**

1. Place the cursor on the field in the upper left corner of the display and press **SELECT.**

2. Place the cursor on **Mixed mode** and press **SELECT.**

You will now see the mixed display as shown:

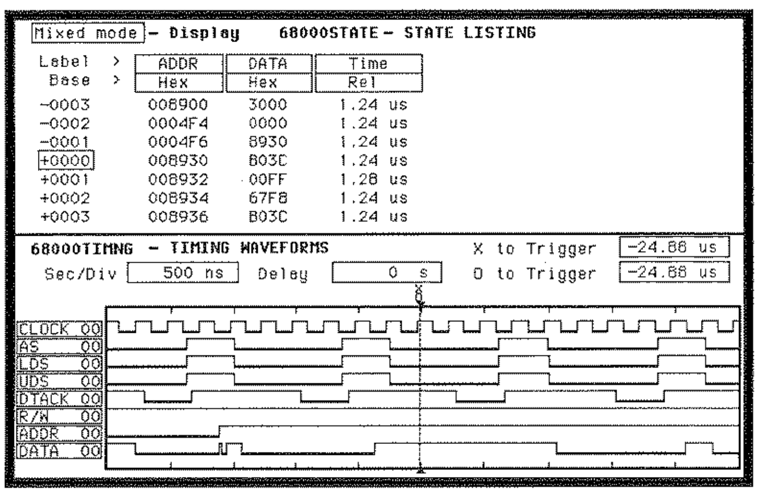


Interpreting the Display

In the **Mixed mode** display the state listing is in the top half of the screen and the timing waveforms are in the lower half. The important thing to remember is that you time correlated this display so you could see what is happening in the time domain during the faulty routine.

Notice that the trigger point in both parts of the display is the same as it was when the displays were separate. The trigger in the state listing is in the box containing +0000 and the trigger of the timing waveform is the vertical dotted line.

As you look at the mixed display, you notice nothing wrong except the data at address 8932 is incorrect. However, you are seeing only one bit each of the address and the data. To see all the data and addresses in the timing waveform part of the display, you must overlap them.



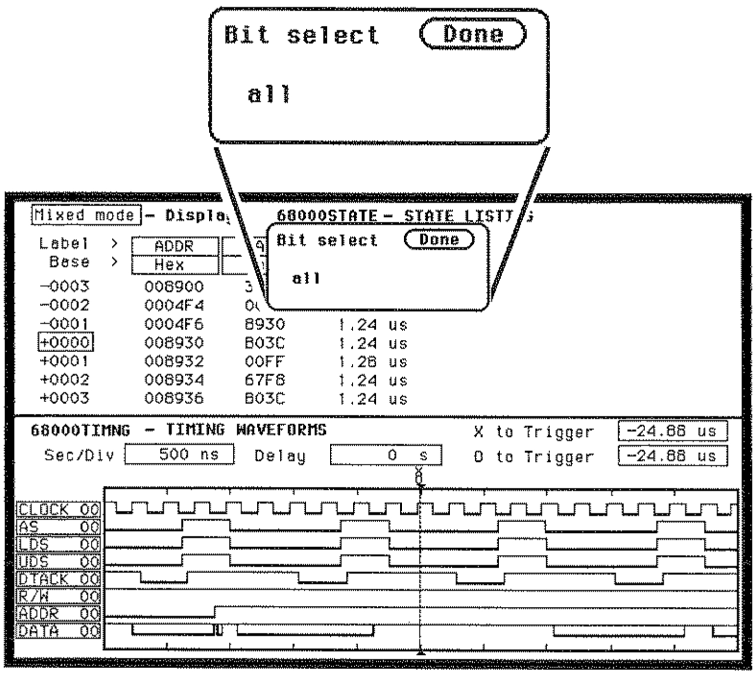
Overlapping Timing Waveforms

Since you see nothing wrong with the timing waveforms so far, you think unstable data may be on the data lines during the read cycle. In order to see unstable data, you must be able to see all the data lines during the read and look for transitions. Overlapping the waveforms allows you to do this. To overlap waveforms, follow these steps:

1. Place the cursor on the **00** of the **ADDR 00** label and press **SELECT**. The following pop-up opens in which you specify the bit or bits of the address bus you want to overlap.

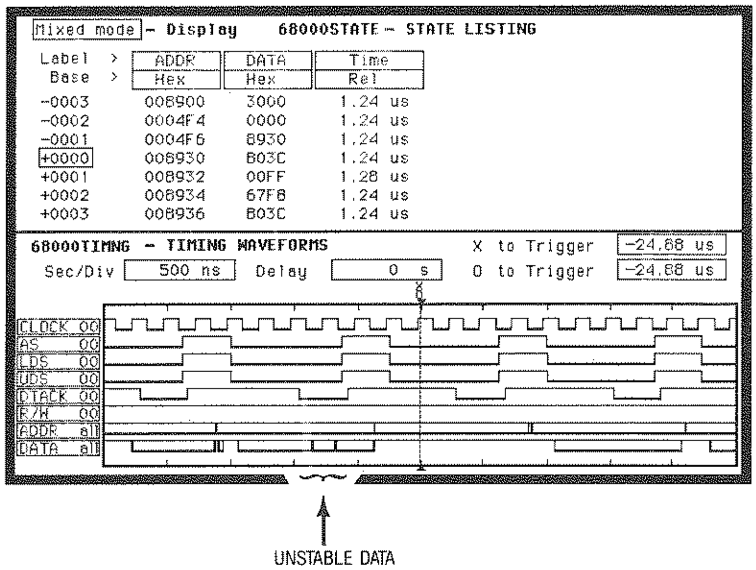
2. Rotate the **KNOB** until **all** is displayed and press **SELECT**. All the address bits will be overlapped on one line.

3. Repeat step 2 except overlap the data bits.



Finding the Answer

As you look at the overlapping waveforms, you notice there are transitions on the data lines during the read cycle, indicating the data is unstable. You have found the probable cause of the problem in this routine. Additional troubleshooting of the hardware will identify the actual cause.



Summary

You have just learned how to use the timing and state analyzers interactively to find a problem that first appeared to be a software problem, but actually was a hardware problem.

You have learned to:

- trigger one analyzer with the other
- time correlate measurement data
- interpret the Mixed mode display
- overlap timing waveforms

If you have an HP 1651B, you do not have enough channels to simultaneously capture all the data for a 68000. But, since you probably aren't working with 16-bit microprocessors, this exercise is still valuable because it shows you how to make the same kind of measurement on an eight-bit microprocessor.

8

Making Hardcopy Prints

Introduction

The HP 1650B/51B Logic Analyzers allow you to print the configurations, waveforms, and listings. Whenever your printer is connected to your logic analyzer and you instruct it to do so, it will print what is currently displayed on screen.

This chapter shows you how to set up the logic analyzer's HP-IB and RS-232C interfaces for printers. If you have a Hewlett-Packard ThinkJet, QuietJet, or LaserJet series printer with the RS-232C interface, the RS-232C interface is already set up for you.

If you have another kind of printer, refer to your printer manual for its interface requirements and change your logic analyzer's interface configuration as instructed.

Hooking Up Your Printer

If your printer is already connected to the logic analyzer, skip to "Setting RS-232C for HP Printers" or "Setting HP-IB for HP Printers." If not, hooking up your printer is just a matter of having the correct HP-IB or RS-232C interface cable. Refer to the *Front-Panel Reference* manual you received with your logic analyzer.

Setting RS-232C for HP Printers

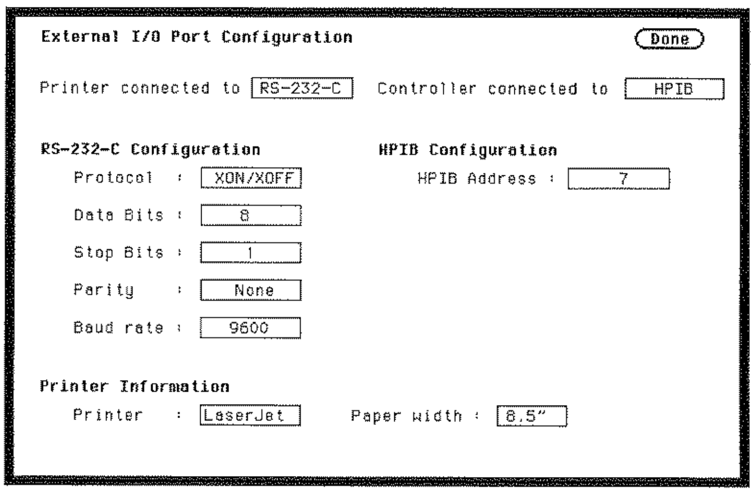
All you have to do to set the interface for any of the previously listed Hewlett-Packard series printers with the RS-232C interface is to set the printer type in the **External I/O Port Configuration** submenu.

To set the printer type, follow these steps:

1. Display the I/O menu by pressing the **I/O** key.

2. Place the cursor on **I/O Port Configuration** and press **SELECT.**

You will see the following submenu:



3. If the **Printer connected to** field displays **RS-232C** skip to step 4. Otherwise, place the cursor in the **Printer connected to HP-IB** field and press **SELECT.** The **Printer connected to** switches from **HP-IB** to **RS-232C.**

4. Place the cursor on the printer series type and press **SELECT.**

5. Place the cursor on **Done** and press **SELECT.** The logic analyzer will display the menu that was displayed when you selected the I/O menu.

Setting RS-232C for Your Non-HP Printer

The following attributes of the RS-232C interface must be set to the correct configuration for your printer:

- Protocol
- number of data bits
- number of stop bits
- parity type
- Baud rate
- paper width

You can set all of these attributes for your printer by following this procedure:

1. Press the **I/O** key to display the I/O menu.
2. Place the cursor on **I/O Port Configuration** and press **SELECT**.
3. Place the cursor on the attribute and press **SELECT**.
4. When the pop-up is open, place the cursor on the option your printer requires and press **SELECT**. The pop-up closes, placing your selection in the box. Repeat this step for all attributes that you need to change.
5. Place the cursor on **Done** and press **SELECT**. The logic analyzer will display the menu that was displayed when you selected the I/O menu.

Setting HP-IB for HP Printers

The HP 1650B/51B interfaces directly with HP PCL printers supporting the printer command language. These printers must also support HP-IB and "Listen Always." Printers currently available from Hewlett-Packard with these features include:

- HP 2225A ThinkJet
- HP 2227B QuietJet
- HP 3630A option 002 PaintJet

Note

The printer must be in "Listen Always" when HP-IB is the printer interface.

The HP 1650B/51B HP-IB port does not respond to service requests (SRQ) when controlling a printer. The SRQ enable setting for the HP-IB printer has no effect on the HP 1650B/1651B operation.

For HP-IB printers, the **Printer connect to** field must be set to **HP-IB** in the **I/O Port Configuration** menu. You access the **I/O Port Configuration** menu by first accessing the **I/O** menu, then the **I/O Port Configuration**.

Starting the Printout

When you are ready to print, you will need to know whether there is more data than is displayed on screen. In cases where data is off screen (i.e., format specifications with all pods assigned to a single analyzer), you need to decide whether you want all the data or just the data is on screen.

If you want just what is on screen, start the printout with the **Print Screen** option. If you want all the data, use the **Print All** option. Both options are in the I/O menu.

Once you decide which option to use, start the printout by placing the cursor on the print option (screen or all) and pressing **SELECT.**

I/O MENU

- Done
- Print Screen
- Print All
- Disc Operations
- I/O Port Configuration
- External BNC Configuration
- Selftests

Print Screen

The **Print Screen** option prints only what is displayed on screen at the time you initiate the printout. In the Print Screen mode, the printer uses its graphics capabilities so the printout will look just like the logic analyzer screen with only one exception: the cursor will not print.

Print All

The **Print all** option prints not only what is displayed on screen, but also what is off screen at the time you initiate the printout. In the Print All mode, the printout will be made in the text mode with only one exception: a timing waveform display will be printed in the graphics mode because it has no off-screen data.

Use this option when you want to print all the data in menus like:

- Timing and State Format Specifications
- State Trace Specifications
- State Listing

What Happens during a Printout?

When you press select to start the printout, the I/O menu pop-up disappears and an advisory **PRINT in progress** appears in the top center of the display. While the data is transferred to the printer, the logic analyzer's keyboard deactivates. When the logic analyzer has completed the data transfer to the printer, the advisory disappears and the keyboard reactivates.

Don't worry! The **Print in progress** advisory won't appear in your printout.

Summary

Now that you have configured the RS-232C or HP-IB interface for your printer, you can make hardcopy printouts of anything that the logic analyzer displays. This is a valuable feature when you need to keep records of configurations and measurements.

A

Logic Analyzer Turn-on Check List

This appendix summarizes the steps you take to turn on the HP 1650B/51B logic analyzers. The details of the turn-on procedures are in Chapter 1 of this booklet.

1. Check the rear-panel line voltage indicator for the proper setting. Change the setting if necessary.
2. Make sure you have the proper 3-wire grounded AC power cable.
3. Make sure the rear-panel line switch if **Off**.
4. Connect the power cable to the rear-panel line connector and a properly grounded power receptacle.
5. Make sure the yellow shipping disk is removed from the disk drive.
6. Insert the operating system disk in the disk drive.
7. Turn the logic analyzer on with the rear-panel line switch.

When the logic analyzer completes its self-tests, it then loads the operating system from the disk. When the operating system has been completely loaded, the **System Configuration** menu will be displayed.

B

Loading Demo Files from the Disk

To load the demo files from the disk, follow these steps:

1. Press the **I/O** key on the front panel
2. Place the cursor on *** Disk Operations** and press **SELECT.**

The disk drive indicator light will come on telling you the logic analyzer is reading the disk. When the disk is read, the logic analyzer will show you the directory of files on the disk.

3. Press the up/down ROLL key to activate the roll function.
4. Rotate the KNOB to place your file selection in the center of the screen. The center of the screen has an arrow on each side of the display area pointing toward the center.

When your file selection is in the center, it will be displayed in bold type.

5. Press the up/down **ROLL** key again to deactivate the file selection function.

Note

Check to see what is displayed in the field in the upper left of the menu. If **Load** is displayed, skip steps 6 and 7.

---

6. Place the cursor in the field in the upper left of the menu and press **SELECT.**
7. Place the cursor on **Load** and press **SELECT.** The pop-up will close and place **Load** in this field.

Verify that your file selection is displayed in the box to the right of **Load from file.** If it is not, repeat step 4. If the correct file is displayed, continue to step 8.

8. Place the cursor on **Execute** and press **SELECT**.

The logic analyzer will load the file and display **Load operation complete.** You resume normal logic analyzer operation by selecting the menu key for the menu you want to see.

Front-Panel Operation Reference

HP 1650B/HP 1651B Logic Analyzers

HEWLETT PACKARD

Printed in the U.S.A. August 1989

Manual Set Part Number 01650-90914

Product Warranty

This Hewlett-Packard product has a warranty against defects in material and workmanship for a period of one year from date of shipment. During warranty period, Hewlett-Packard Company will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Hewlett-Packard. However, warranty service for products installed by Hewlett-Packard and certain other products designated by Hewlett-Packard will be performed at the Buyer's facility at no charge within the Hewlett-Packard service travel area. Outside Hewlett-Packard service travel areas, warranty service will be performed at the Buyer's facility only upon Hewlett-Packard's prior agreement and the Buyer shall pay Hewlett-Packard's round trip travel expenses.

For products returned to Hewlett-Packard for warranty service, the Buyer shall prepay shipping charges to Hewlett-Packard and Hewlett-Packard shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to Hewlett-Packard from another country.

Hewlett-Packard warrants that its software and firmware designated by Hewlett-Packard for use with an instrument will execute its programming instructions when properly installed on that instrument. Hewlett-Packard does not warrant that the operation of the instrument software, or firmware will be uninterrupted or error free.

Limitation of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by the Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HEWLETT-PACKARD SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OR MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

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Assistance

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office.

Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

Safety

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this manual must be heeded.

Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition or a new update is published.

A software code may be printed before the date; this indicates the version level of the software product at the time of the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

Edition 1 August 1989 01650-90914

List of Effective Pages

The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. If an update is incorporated when a new edition of the manual is printed, the change dates are removed from the bottom of the pages and the new edition date is listed in Printing History and on the title page.

Pages	Effective Date
All	August 1989

Contents

Chapter 5: I/O Menu

Chapter 6: Disk Drive Operations

Chapter 10: Timing Trace Specification Menu

Chapter 11: Timing Waveforms Menu

Appendix E: Microprocessor Specific Measurements

1 General Information

Logic Analyzer Description

The HP 1650B and 1651B logic analyzers are new general purpose logic analyzers with improved features to accommodate next generation design tasks. They are basically the same as their predecessors the HP 1650A and HP 1651A, but now have State Compare, State Waveform, and State Chart modes. They both have HP-IB capabilities in addition to RS-232C.

Both the 80-channel HP 1650B and the 32-channel HP 1651B logic analyzers are capable of 100 MHz timing analysis. The HP 1651B is capable of 25 MHz state analysis on all channels while the HP 1650B is capable of 35 MHz state analysis on all channels. The HP 1651B, while only having 32 channels, has basically the same features as the HP 1650B. That's why you have the same manual set regardless of whether you have an HP 1650B or an HP 1651B.

These analyzers are designed as stand alone instruments for use by digital and microprocessor designers. Both the HP 1650B and HP 1651B have HP-IB and RS-232C interfaces for hardcopy printouts and control by a host computer.

User Interface

The user interface is easier to use than in previous generations for first-time and casual users as well as experienced logic analyzer users.

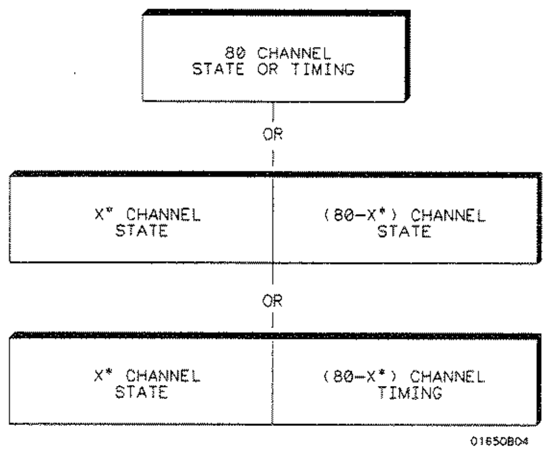
The front panel is controlled by a front-panel keyboard, and the addition of a "KNOB" allows you to move the cursor or change settings more quickly than before. The timing analyzer (a close cousin of the oscilloscope) now has oscilloscope-type controls which more closely match the type of measurements you make with the timing analyzer. Information is displayed on a nine-inch white phosphor CRT.

Configuration Capabilities

The HP 1650B/51B can be configured either as two independent machines (analyzers) or as two machines interactively. The configurations are:

HP 1650B

- Up to 80 channels state
- Up to 80 channels timing
- Two state machines with multiples of 16 channels per machine with a combined maximum of 80 channels
- One state and one timing machine with multiples of 16 channels per machine with a combined maximum of 80 channels



*multiples of 16 channels

Figure 1-1. HP 1650B Configuration Capabilities

HP 1651B

- Up to 32 channels state
- Up to 32 channels timing
- Two state machines with 16 channels per machine
- One state and one timing machine with 16 channels per machine

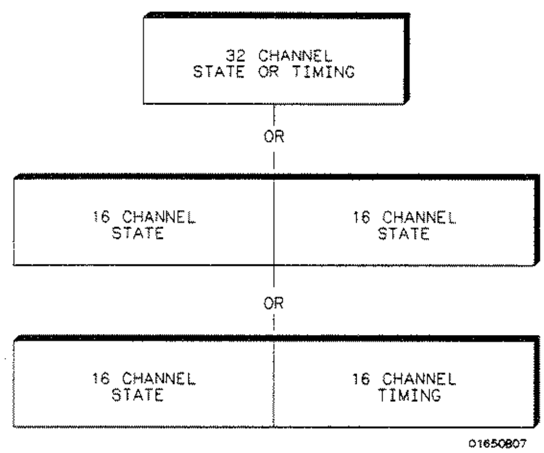


Figure 1-2. HP 1651B Configuration Capabilities

Key Features

A 3.5-inch disk drive is built into the instrument for storing logic analyzer configurations and acquired data. The disk drive also provides a way of loading inverse assembly configuration files into the logic analyzer for easy configuring.

Additional key features of both models include:

- Transitional timing for extended timing analyzer memory
- Lightweight passive probes for easy hook-up
- All channels can be used for state or timing at the maximum sample rate
- HP-IB and RS-232C interfaces for programming and printer output
- An external trigger BNC connector
- Transitional or glitch timing modes
- 1k-deep memory on all channels
- Glitch detection
- Marker measurements
- Triggering and pattern qualification
- Overlapping of timing waveforms
- Eight sequence levels
- Eight pattern recognizers
- One range recognizer
- Time and number-of-states tagging
- Pre-store
- Auto-scale
- Programmability
- Cross-domain triggering
- Interactive measurements
- Mixed-mode display
- Oscilloscope-type controls in the timing analyzer
- State Compare, Chart, and Waveform modes

Accessories Supplied

Table 1-1 lists the accessories supplied with your HP 1650B/51B. If you need additional accessories, refer to the "Accessories for the HP 1650B/HP 1651B and HP 16500A Logic Analyzers" data sheet. If any of these accessories were missing when you received the logic analyzer from the factory, contact your nearest Hewlett-Packard office.

Table 1-1. Accessories

Accessory	HP Part No.	Quantity	
		HP 1650B	HP 1651B
Probe assemblies	01650-61608	5	2
Probe cables	01650-61607	5	2
Grabbers (Note 1)	5959-0288	100	40
Probe Leads (Note 2)	5959-9333	85	34
Ground leads (long) (Note 2)	5959-9334	5	2
Ground leads (short) (Note 2)	5959-9335	10	4
RS-232C loop back adapter	01650-63202	1	1
Probe and probe cable numbering label card	01650-94303	1	1
AC power cable	Note 3	1	1
Operating system disk	01650-13520	2	2
Front-Panel Reference manual	01650-90914	1	1
Programming Reference manual	01650-90913	1	1
Service manual	01650-90915	1	1

Notes:

1. Package of 20 per part number. The quantity in the above table only indicates what is shipped with the instrument.

2. Package of 5 per part number. These items are shipped assembled as a 01650-61608. The part numbers are provided for replacement orders. The quantity in the above table only indicates what is shipped with the instrument.

3. The type of power cord you receive with your logic analyzer depends on your country. Complete information about the power cord options is in Appendix B of this manual.

Available Accessories

In addition to the accessories supplied, there are a number of accessories available that will make your measurement tasks easier and more accurate. You will find these listed in *Accessories for the HP 1650B/ HP 1651B and HP 16500A Logic Analyzers*.

Manuals Supplied

The manuals supplied with your logic analyzer are:

- *Feeling Comfortable with Logic Analyzers* - A primer on logic analyzers
- *Getting Started with the HP 1650/HP 1651B Logic Analyzer* - A tutorial for new and casual users
- *HP 1650/HP 1651B Front-Panel Reference Manual* - A complete operating manual
- *HP 1650/HP 1651B Programming Reference Manual* - A complete programming manual
- Service Manual - A guide to troubleshooting and module-level repair.

Turning On the Logic Analyzer

Don't turn on the logic analyzer before you remove the yellow shipping disk from the disk drive.

If you are unfamiliar with how to turn on the HP 1650B/51B logic analyzers, refer to the *Getting Started Guide* or Appendix B for information on how to remove the yellow shipping disk and turn the instrument on.

2

Probing

Introduction

This chapter contains a description of the probing system of the HP 1650B/51B logic analyzers. It also contains the information you need to connect the probe system components to each other, to the logic analyzer, and to the system under test.

Probing Options

You can connect the HP 1650B/51B logic analyzers to your system under test in one of four ways:

- HP 10320C User-definable Interface (optional)
- HP 10269C with microprocessor specific modules (optional)
- The standard HP 1650B/51B probes (general purpose probing)
- Direct connection to a 20-pin 3M® Series type header connector using the optional termination adapter (HP part number 01650-63201).

The HP 10320C User-Definable Interface

The optional HP 10320C User-definable Interface module combined with the optional HP 10269C General Purpose Probe Interface allows you to connect the HP 1650B/51B logic analyzers to the microprocessor in your target system. The HP 10320C includes a breadboard (HP 64651B) which you custom wire for your system.

Also available as an option that you can use with the HP 10320C is the HP 10321A Microprocessor Interface Kit. This kit includes sockets, bypass capacitors, a fuse for power distribution, and wire-wrap headers to simplify wiring of your interface when you need active devices to support the connection requirements of your system.

You will find additional information about the HP 10320C and HP 10321A in the *Accessories for the HP 1650B/HP1651B and HP 16500A Logic Analyzers* data sheet.

The HP 10269C General-Purpose Probe Interface

Instead of connecting the probe tips directly to the signal lines, you may use the HP 10269C General Purpose Probe Interface (optional). This allows you to connect the probe cables (without the probes) to connectors on the interface. When the appropriate preprocessor is installed in the interface, you will have a direct connection between the logic analyzer and the microprocessor under test. See figure 2-1 for a basic block diagram.

There are a number of microprocessor specific preprocessors available as optional accessories which are listed in the *Accessories for the HP 1650B/HP 1651B and HP 16500A Logic Analyzers* data sheet that came with your logic analyzer. Appendix E of this manual also introduces you to preprocessors and inverse assemblers.

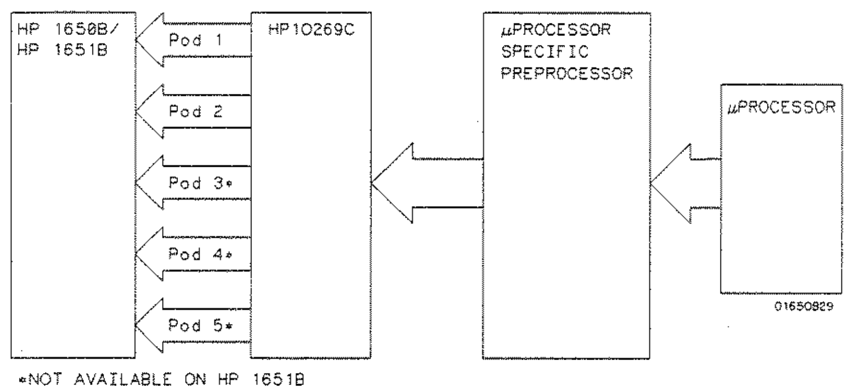


Figure 2-1. HP 10269C with Preprocessor

General-Purpose Probing

General-purpose probing involves connecting the probes directly to your target system without using the interface. General purpose probing does not limit you to specific hook-up schemes as the probe interface does.

The Termination Adapter

The optional termination adapter (HP part number 01650-63201) allows you to connect the probe cables directly to test ports on your target system without the probes. However, since the probes contain the proper termination for the logic analyzer inputs, a termination must be provided when you aren't using the probes. The termination adapter provides this termination.

The termination adapter is designed to connect to a 20 (2 by 10) position, 4-wall, low profile header connector, 3M® Series 3592 or equivalent.

You connect the termination adapter to the probe cable in place of the pod connector and connect the other end of the adapter directly to your test port.

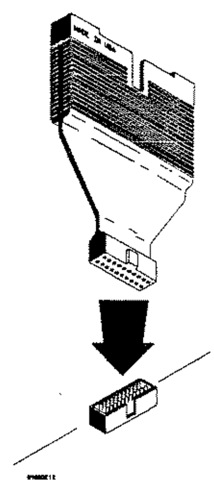


Figure 2-2. Termination Adapter

Termination Adapter Pinouts

Figure 2-3 shows the pinouts of the optional termination adapter.

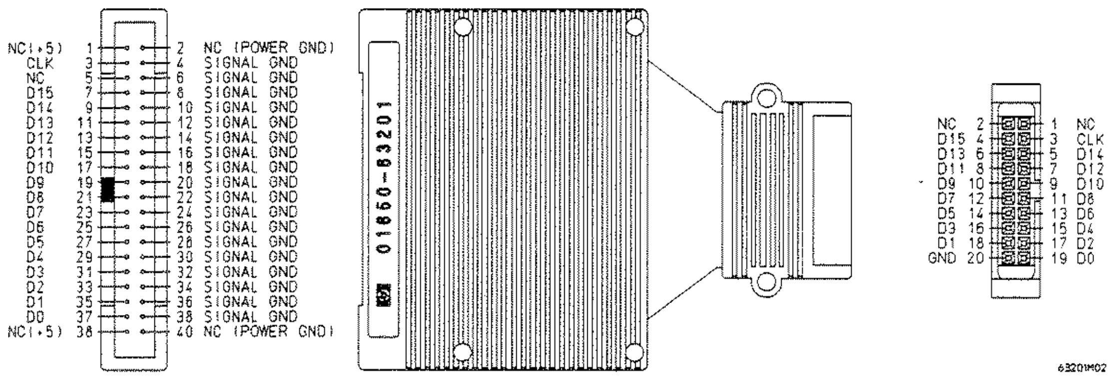


Figure 2-3. Termination Adapter Pinout

Figure 2-4 shows the pinout required on your target system if you are planning to connect the logic analyzer directly through the termination adapter.

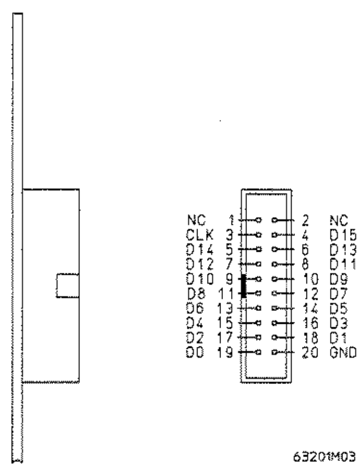


Figure 2-4. Connector Pinout (HP P/N 1251-8106)

The HP 1650B/51B Probing System

The standard HP 1650B/51B probing system consists of probes, pods, a probe cable and grabbers. This system is passive (has no active circuits at the outer end of the cable). This means that the pods and probes are smaller and lighter, making them easier to use.

The passive probe system is similar to the probe system used with high frequency oscilloscopes. It consists of a series R-C network (90.9 kΩ in parallel with 8 pF) at the probe tip, and a shielded resistive transmission line. The advantages of this system are:

- 2 ns risetime with ±5% perturbations
- 8 pF input capacitance at the probe tip
- Signal ground at the probe tip for higher speed timing signals
- Inexpensive removable probe tip assemblies

Probes and Probe Pods

Probes and probe pods allow you to connect the logic analyzer to your system under test without the HP 10269C Probe Interface. This general purpose probing is useful for discrete digital circuits. Each probe and pod assembly contains 16 data channels, one clock channel, and pod ground.

Probe Pod Assembly

The pods, as they will be referred to for consistency, are the probe housings (as shown below) that group the 16 data lines, one clock line, and grounds, corresponding to a logic analyzer pod.

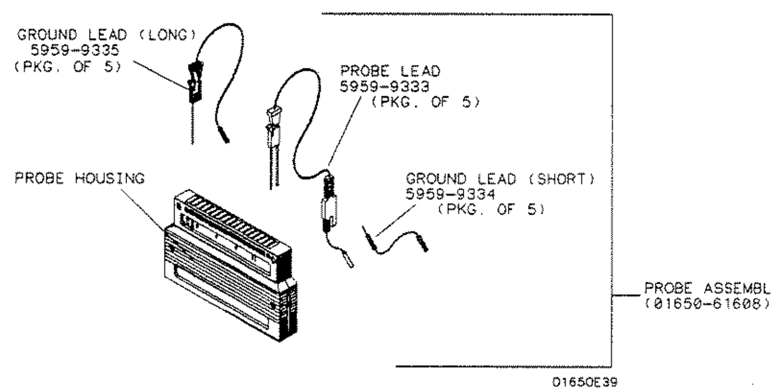


Figure 2-5. Probe Assembly

Probe Cable

The probe pod cable contains 17 signal lines, 34 chassis ground lines and two power lines that are woven together. It is 4.5 feet long.

Caution

The probe grounds are chassis (earth) grounds, not "floating" grounds.

Both ends of the cable are alike so it doesn't matter which end you connect to the pods or logic analyzer. Each cable is capable of carrying 0.60 amps for preprocessor power. DO NOT exceed this 0.60 amps per cable or the cable will be damaged. Also, the maximum power available from the logic analyzer (all cables) is 2 amps at 5 volts. DO NOT exceed 2 amps total even though the total of all cables is greater than 2 amps.

Note

The preprocessor power source is protected by a circuit breaker. If a preprocessor appears to be malfunctioning, refer to the service manual for instructions on checking the preprocessor power source.

The probe cable connects the logic analyzer to the pods, termination adapter, or the HP 10269C General Purpose Probe Interface.

Probes

Each probe is a 12-inch twisted pair cable and is connected to the probe cable at the pod. One end of each probe has a probe tip assembly where the input R-C network is housed and a lead that connects to the target system. The other end of the probe has a two-pin connector that connects to the probe cable.

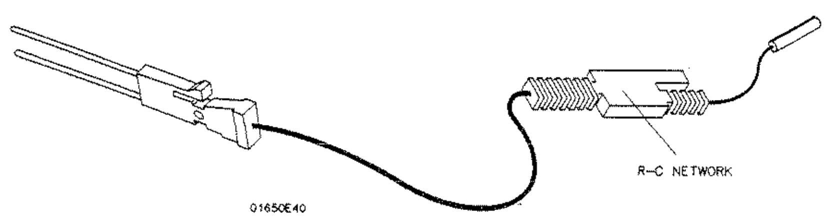


Figure 2-6. Probe

You can connect the probe directly to the test pins on your target system. To do so, you must use 0.63 mm (0.025 in) square pins or round pins with a diameter of between 0.66 mm (0.026 in) and 0.84 mm (0.033 in).

Each probe has an input impedance of 100 kΩ in parallel with approximately 8 pF.

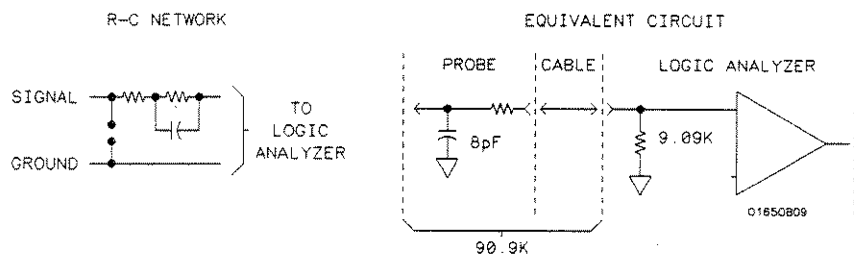


Figure 2-7. Probe Input Circuit

Probes can be grounded in one of two ways: a common pod ground and a probe ground for each probe.

Grabbers

The grabbers have a hook that fits around IC pins and component leads and connects to the probes and the ground leads. The grabbers have been designed to fit on adjacent IC pins.

Pod Grounds

Each pod is grounded by a pod ground lead that should always be used. You can connect the ground lead directly to a ground pin on your target system or use a grabber. The grabber connects to the ground lead the same way it connects to the probe lead.

To connect the ground lead to grounded pins on your target system you must use 0.63 mm (0.025 in.) square pins or round pins with a diameter of 0.66 mm (0.026 in.) to 0.84 mm (0.033 in.).

Probe Grounds

You can ground the probes in one of two ways. You can ground the probes with the pod ground only; however, the ground path won't be the same length as the signal path through the probe. If your probe ground path must be the same as your signal path, use the short ground lead (probe ground). The probe ground lead connects to the molded probe body via a pin and socket. You can then use a grabber or grounded pins on your target system the same way as the pod ground.

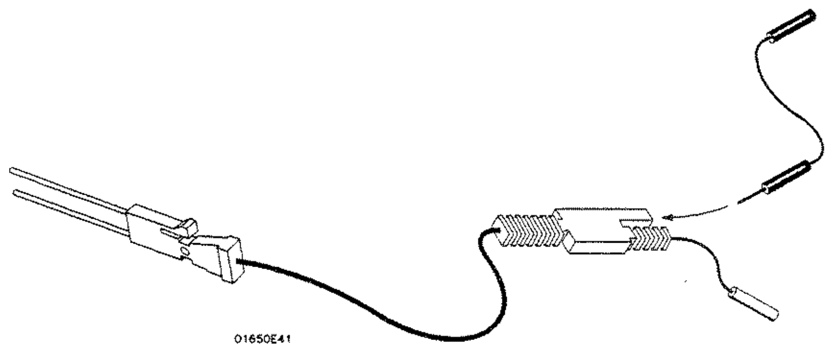


Figure 2-8. Probe Grounds

Note

For improved signal fidelity, use a probe ground for every four probes in addition to the pod ground.

If you need additional probe ground leads, order HP part number 5959-9334 (package of 5) from your nearest Hewlett-Packard sales office.

Signal Line Loading

Any signal line you intend to probe must be able to supply a minimum of 600 mV (from threshold) to the probe tip, which has an input impedance of 100 kΩ shunted by 8 pF. If the signal line is incapable of this, you will not only have an incorrect measurement but the system under test may also malfunction.

Maximum Probe Input Voltage

The maximum input voltage of each probe is ±40 volts peak.

Pod Thresholds

There are two preset thresholds and a user-definable pod threshold for each pod. The two preset thresholds are ECL (−1.3 V) and TTL (+ 1.6 V). The user-definable threshold can be set anywhere between −9.9 volts and + 9.9 volts in 0.1 volt increments.

The pod thresholds of pods 1 and 2 in the HP 1651B and of pods 1, 2, and 3 in the HP 1650B can be set independently. The pod thresholds of pods 4 and 5 in the HP 1650B are slaved together; therefore, when you set the threshold on either pod 4 or 5, both thresholds will be the same.

Connecting the Logic Analyzer to the Target System

There are four ways you can connect the logic analyzer to your target system as previously mentioned at the beginning of this chapter: the probes (general purpose probing); the HP 10320C User-definable Interface; the HP 10269C with microprocessor specific preprocessor modules; and direct connection to a 20 pin 3M® Series type header connector using the optional termination adapter (HP part number 01650-63201).

Since the probe interface hook-ups are microprocessor specific, they will be explained in their respective operating notes. The rest of this chapter is dedicated to general purpose probing with the HP 1650B/51B probes.

Connecting the Probe Cables to the Logic Analyzer

You connect the probe cables to the probe connectors on the rear panel of the logic analyzer. The connectors are keyed for proper orientation. You can connect either end of the cable to the rear panel since both ends of the cables are alike.

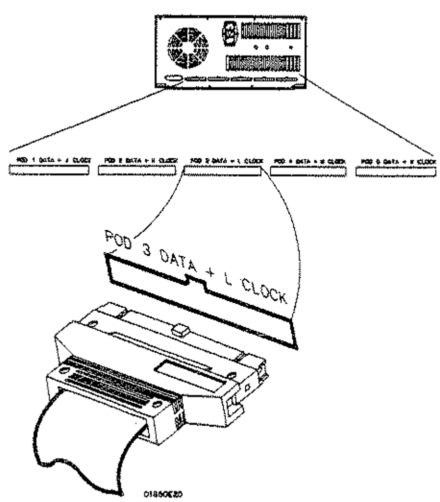


Figure 2-9. Probe Cable to Logic Analyzer

Connecting the Pods to the Probe Cable

The pods of the HP 1650/51B differ from other logic analyzers in that they are passive (have no active circuits at the outer end of the cable). The pods, as they will be referred to for consistency, are the connector bodies (as shown below) that the probes are installed in when you receive your logic analyzer.

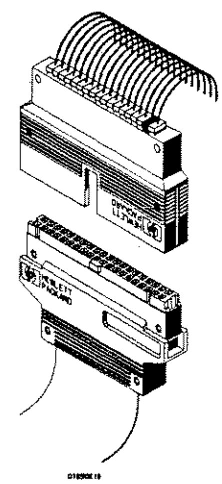


Figure 2-10. Connecting Pods to Probe Cables

To connect a pod to a cable, align the key on the cable connector with the slot on the pod connector and connect them the same way you connected the other end to the logic analyzer.

Disconnecting the Probes from the Pods

The probes are shipped already installed in the pods. However, you can disconnect any un-used probes from any of the pods. This keeps the un-used probes from getting in your way.

To disconnect a probe, insert the tip of a ball-point pen in the latch opening and push while gently pulling the probe out of the pod connector as shown below.

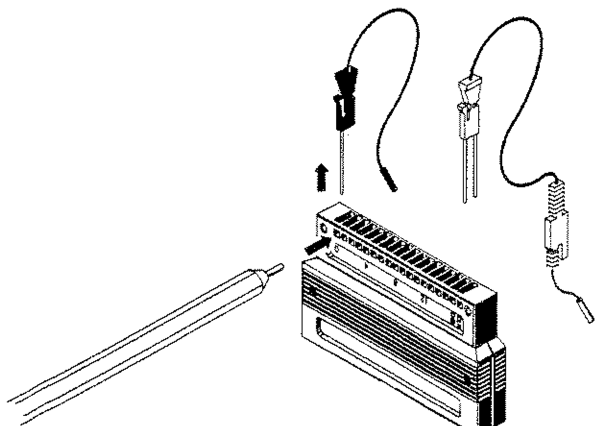


Figure 2-11. Disconnecting Probes from Pods

You connect the probes to the pods by inserting the double pin end of the probe into the pod. The probes and pod connector body are both keyed (beveled) so that they will fit together only one way.

Connecting the Grabbers to the Probes

You connect the grabbers to the probes by slipping the connector at the end of the probe onto the recessed pin in the side of the grabber. If you need to use grabbers for either the pod or the probe grounds connect them to the ground leads the same way you connect them to the probes.

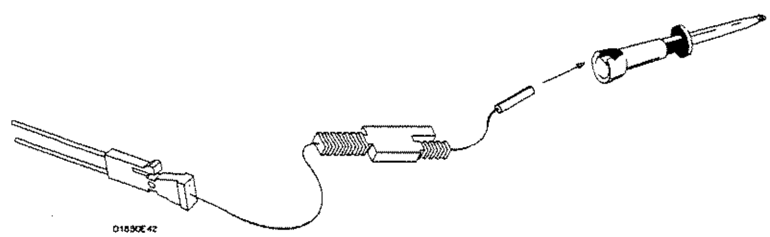


Figure 2-12. Connecting Grabbers to Probes

Connecting the Grabbers to the Test Points

The grabbers have a hook that fits around IC pins and component leads. You connect the grabber by pushing the rear of the grabber to expose the hook, hooking the lead and releasing your thumb as shown below.

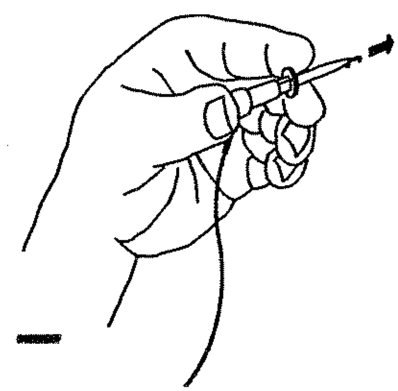


Figure 2-13. Connecting Grabbers to Test Points

Labeling Pods, Probes, and Cables

So you can find the pods and probes you want to connect to your target system, you need to be able to quickly identify them. Included with your logic analyzer are self-adhesive labels for each pod, cable and probe.

They come in sets. Each set has labels for each end of the cable – a label for the pod connector body, a label for the clock probe and 16 labels for each of the channels.

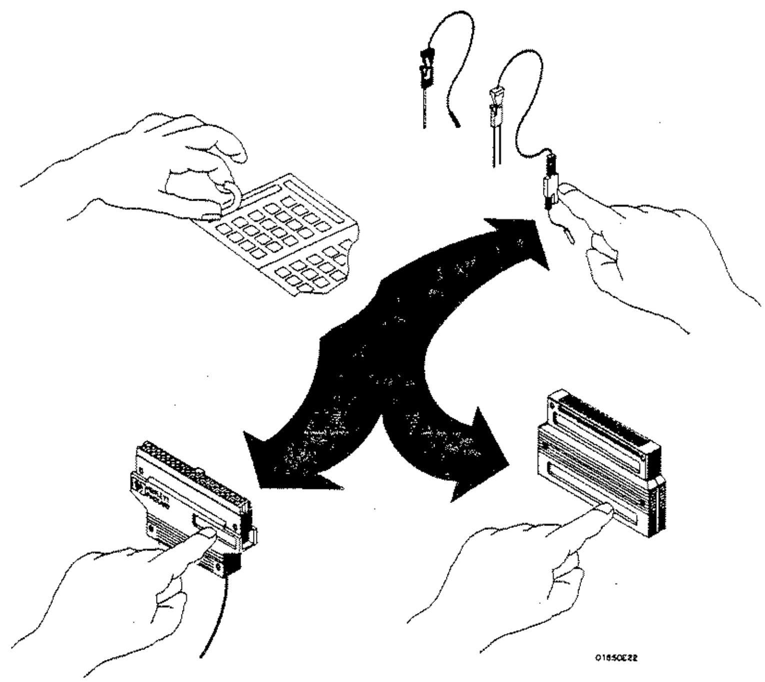


Figure 2-14. Labeling Pods, Probes, and Cables

3 Using the Front-Panel User Interface

Introduction

This chapter explains how to use the front-panel user interface. The front- and rear-panel controls and connectors are explained in the first part of this chapter followed by how to use explanations of the front-panel user interface.

The front-panel user interface consists of front-panel keys, the KNOB, and display. The interface allows you to configure the logic analyzer and each analyzer (machine) within the logic analyzer. It also displays acquired data and measurement results.

Using the front-panel user interface is a basic process of:

- selecting the desired menu with the menu keys
- placing the cursor on the desired field within the menu by rotating the KNOB
- displaying the field options or current data by pressing the SELECT key
- selecting the desired option by rotating the KNOB or entering new data by using the KNOB or the keypad
- starting and stopping data acquisition by using the RUN and STOP keys

Front-Panel Controls

In order to apply the user interface quickly, you should know what the front-panel controls do.

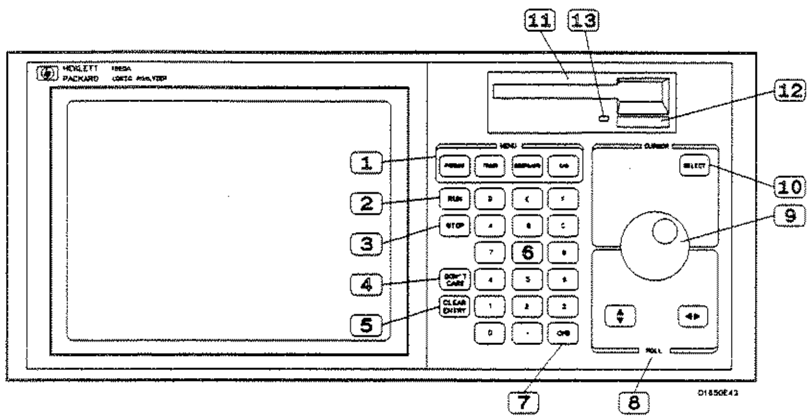


Figure 3-1. HP 1650B/51B Front Panel

1 **Menu Keys.** The menu keys allow you to select the main menus in the logic analyzer. These keys are FORMAT, TRACE, DISPLAY, and I/O. The Format, Trace, and Display keys will display the menus of either analyzer (machine) 1 or 2 respectively depending on what menu was last displayed or what you did in the System Configuration menu.

Format Menu Key. The FORMAT menu key allows you to access either the Timing Format or the State Format Specification menus. You exit the Format Specification menu by pressing another menu key or by returning to the System Configuration menu from this menu.

Trace Menu Key. The TRACE menu key allows you to access either the Timing Trace or the State Trace Specification menus. You exit the Trace Specification menu by pressing another menu key or by returning to the System Configuration menu from this menu.

Display Menu Key. The DISPLAY menu key allows you to access either the timing waveforms display or the state listing display. You exit the Timing Waveforms or State Listing menu by pressing another menu key or by returning to the System Configuration menu from this menu.

I/O Menu Key. The I/O menu key allows you to access the I/O menu. You can access the I/O menu from any other menu in either analyzer (timing or state) and at any time. Pressing the I/O menu key causes the I/O menu to pop up over the current menu on the display.

2 **Run Key.** The RUN key allows you to initiate a data acquisition and display cycle. An analyzer (state or timing) is automatically forced into its display menu when a run is initiated. The trace mode you select (in the Trace Specification menu) determines whether a single or multiple (repetitive) run occurs.

3 **Stop key.** The STOP key allows you to stop data acquisition or printing. A single press always stops the data acquisition. The data displayed on screen depends on which acquisition mode (single or repetitive) was used to acquire the data. In the repetitive mode, STOP causes the old display to remain unchanged as long as the old data is not corrupt. In single mode, STOP causes any new data to be displayed. If printing a hardcopy, the STOP key stops the print.

4 **Don't Care Key.** The DON'T CARE key allows you to enter don't cares in binary, octal, and hexadecimal pattern specification fields. In Alpha Entry fields, this key enters a space and moves the underscore marker to the next space.

5 **Clear Entry Key.** The CLEAR ENTRY key allows you to:

- return decimal values to the previous value in the decimal menu fields
- return values to don't cares in menu fields with number bases other than decimal
- clear Alpha Entry menus
- move the underscore marker or cursor to its original position in the menu fields

(6) **Hex(adecimal) Keypad.** The HEX keypad allows you to enter numeric values in numeric entry fields. You enter values in the number base selected for the field. The bases are:

- Binary
- Octal
- Decimal
- Hexadecimal

The A through F keys are used for both hexadecimal and alpha character entries.

(7) **CHS Key.** The CHS (change sign) key allows you to change the sign (±) of numeric variables.

(8) **Roll Keys.** When part of the data display is off screen, the ROLL keys define which way the KNOB will move the displayed data. These keys and the KNOB roll displayed data up/down or left/right so you can view off-screen data.

(9) **Knob.** The KNOB has four major functions depending on what menu or pop-up menu you are in. The KNOB allows you to:

- move the cursor from field to field within the System Configuration and main menus
- roll the display left or right and up or down
- position the cursor on options within pop-up menus
- increment/decrement numeric values in numeric pop-up menus

(10) **Select Key.** The SELECT key allows you to open pop-up menus, choose options in them, cancel selections, and close pop-up menus. When the cursor is in a main menu (i.e., Format Specification) pressing the SELECT key either opens a pop-up, or toggles options (when there are only two options possible) in that field.

When a pop-up menu appears, the cursor will be on the current option. You use the KNOB to move the cursor to your desired option. Pressing the SELECT key tells the logic analyzer this is the option you want. This either automatically selects the option and closes the pop-up, opens another pop-up, or changes options. If the pop-up doesn't automatically close, it will contain the Done field. In this case you close the pop-up by placing the cursor on Done and pressing SELECT.

11 **Disk Drive.** A 3.5 inch, double-sided, double density drive. Besides loading the operating system, it allows you to store and load logic analyzer configurations and inverse assembler files.

12 **Disk Eject Button.** Press this button to eject a flexible disk from the disk drive.

13 **Indicator Light.** Illuminated when the disk drive is operating. Wait until this light is out before removing or inserting disks.

Rear-Panel Controls and Connectors

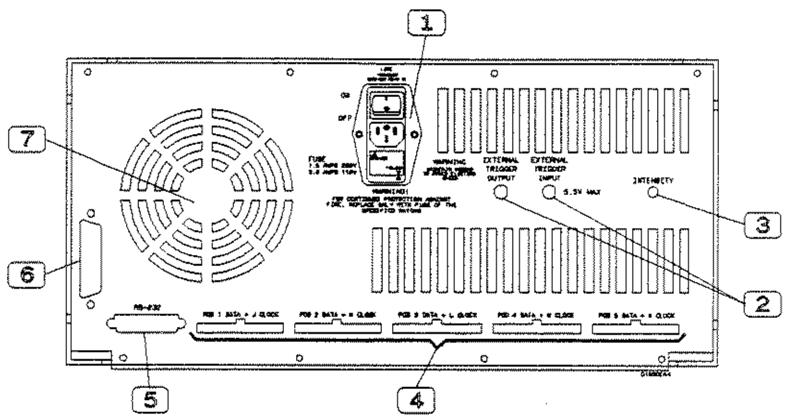


Figure 3-2. HP 1650B/51B Rear Panel

1. **Line Power Module.** Permits selection of 110-120 or 220-240 Vac and contains the fuses for each of these voltage ranges. The On/Off switch is also part of the module.
2. **External Trigger BNCs.** Provide arm out and arm in connections.
3. **Intensity Control.** Allows you to set the display intensity to a comfortable level.
4. **Pod Cable Connectors.** Keyed connectors for connecting the pod cables.

Note The HP 1651B rear panel has connectors for pods 1 and 2 only.

5. **RS-232C Interface Connector.** Standard DB-25 type connector for connecting an RS-232C printer or controller.

6 **HP-IB Interface Connector.** Standard HP-IB connector for connecting an HP-IB printer or controller.

7 **Fan.** Provides cooling for the logic analyzer. Make sure air is not restricted from the fan and rear-panel openings.

The Cursor

The cursor (inverse video) highlights interactive fields within the menus that you want to use. Interactive fields are enclosed in boxes in each menu. When you rotate the KNOB, the cursor moves from one field to another.

How to Select Menus

You select the main menus by pressing the appropriate menu key. The menu keys are:

- FORMAT
- TRACE
- DISPLAY
- I/O

When the menu is displayed, you can access fields within the menus.

The FORMAT, TRACE, and DISPLAY menu keys provide access to their respective menus. If more than one analyzer (machine) is on you see the selected menu of either analyzer 1 or analyzer 2 depending on what analyzer menu was last displayed or what you did in the System Configuration menu. To switch from one of these menus to another menu within the same analyzer (machine) press the desired menu key. If more than one analyzer is on, you can switch between analyzers in any of these main menus except the I/O menu.

The I/O menu differs from the other three main menus in that it is a pop-up menu that appears on top of the currently displayed menu when you press the I/O key.

How to Switch between Analyzers

When both analyzers are on, you can switch between them in any main menu except the I/O menu. To switch between analyzers, place the cursor on the field in the upper left corner of the FORMAT, TRACE, or DISPLAY (timing or state) menu and press SELECT. A pop-up menu appears with the options:

- System
- MACHINE 1 (or your analyzer name)
- MACHINE 2 (or your analyzer name)
- Mixed Mode (if both machines are on)

Place the cursor on the opposite analyzer (machine) and press SELECT. The logic analyzer will display the same menu type (i.e. format, trace, etc.) in the other machine. For example, if you were in the TRACE menu of machine 1, you will now see the TRACE menu of machine 2.

Returning to the System Configuration Menu

You can return to the System Configuration menu directly from the FORMAT, TRACE, or DISPLAY menus. To return to the System Configuration menu, place the cursor on the field in the upper left corner of any of these menus and press SELECT. A pop-up menu appears with the options:

- System
- MACHINE 1 (or your analyzer name)
- MACHINE 2 (or your analyzer name)
- Mixed Mode (if both machines are on)

Place the cursor on System and press SELECT. The System Configuration menu will now be displayed.

How to Select Fields

You select fields within the main menus by placing the cursor on the desired field and pressing SELECT. Depending on what type of field you select, you will either see a pop-up menu or a new option in fields that toggle.

Pop-Up Menus

The pop-up menu is the most common type of menu you see when you select a field. When a pop-up appears you see a list of two or more options from which you select an option or options. Two pop-up menu types are described in "How to Select Options" in this chapter.

How to Close Pop-Up Menus

Pop-up menus without the Done option automatically close when you place the cursor on an option and press SELECT. After closing, the logic analyzer places your choice in the main menu field from which you opened the pop-up.

Pop-up menus that contain the Done option don't automatically close when you make your selection. To close the pop-up, you place the cursor on the Done option and press SELECT.

These two pop-up menu types are described in "How to Select Options" in this chapter.

How to Select Options

How to select options depends on what type of pop-up menu appears when you press select. When the pop-up appears, you will see a list of options. You select the option you want by placing the cursor on it and pressing SELECT. In most cases the pop-up menu closes and your desired option is now displayed in the field in the main menu.

There are also pop-up menus where each option within the pop-up menu has more than one option available. In these cases, when you place the cursor on one of the options and press select, another pop-up will appear.

An example of one of these is the clock field in the State Format Specification menu. When you select the clock field in this menu it will pop-up and show you all five clocks (J, K, L, M, and N) for an HP 1650B or both clocks (J and K) for an HP 1651B.

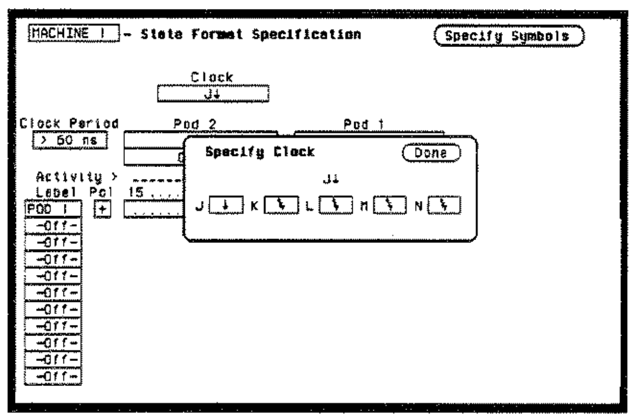


Figure 3-3. State Clock Pop-Up Menu

When you place the cursor on one of the clocks and press SELECT another pop-up appears, showing you the choices of clock specifications available.

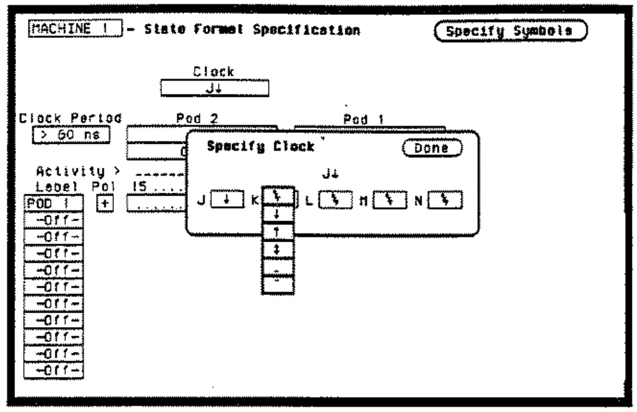


Figure 3-4. State Clock Pop-Up with K Pop-Up Open

When you choose one of these and press SELECT this pop-up will close, however, the original clock pop-up still remains open. When you are finished specifying the choices for the clocks, you close the original pop-up menu by placing the cursor on Done and pressing SELECT.

Toggle Fields

Some fields will toggle between two options (i.e., off and on). When you place the cursor on one of these fields and press SELECT, the displayed option toggles to the other choice and no additional pop-up appears.

How to Enter Numeric Data

There are a number of pop-up menus in which you enter numeric data. The two major types are:

- Numeric entry with fixed units (i.e. volts)
- Numeric entry with selectable units (i.e. ms, µs, etc.)

An example of a numeric entry menu in which you only enter the value with fixed units is the pod threshold pop-up menu.

You can set the pod thresholds to either of the preset thresholds (TTL or ECL) or to a specific voltage from - 9.9 V to + 9.9 V.

To set pod thresholds to a specific voltage, place the cursor in the threshold portion of the pod field (TTL, ECL, or User-defined) of any pod and press SELECT.

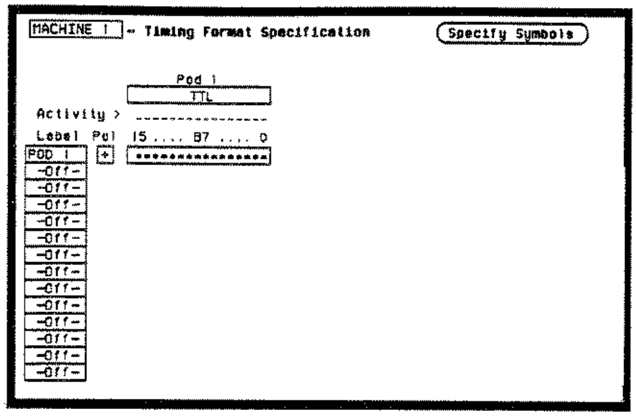


Figure 3-5. Pod Threshold

Select the User-defined option and another pop-up appears for you to specify the pod threshold voltage.

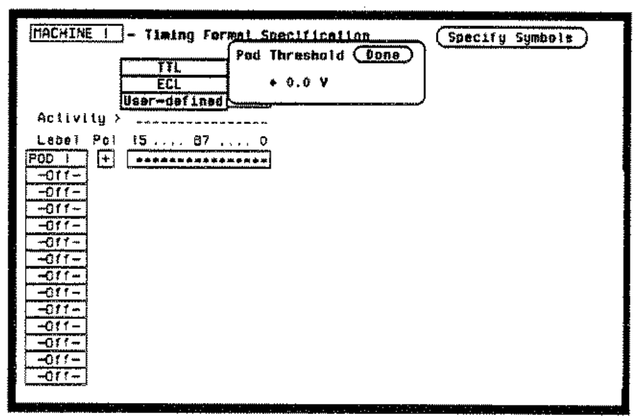


Figure 3-6. User-Defined Pop-Up

You can select your desired threshold by rotating the KNOB until your desired threshold voltage is displayed. Rotating the KNOB increments or decrements the value in small steps. Or you can change the value with the keypad. It allows you to make large value changes quickly. Entering the new value from the keypad replaces the previous value.

If you want a negative voltage for the threshold, press the CHS (change sign) key on the front panel. The minus (–) sign will appear in the pop-up.

Notice, the cursor stays in the upper right corner of the pop-up over Done. When you press SELECT, the pop-up will close and your new threshold will be placed in the Pod field.

In another type of numeric entry pop-up menu you must specify the units as well as the numeric value. The pattern duration specification in the Timing Trace Specification menu is an example. When you place the cursor on the value in the **present for** ______ field and press SELECT, you will see the following pop-up:

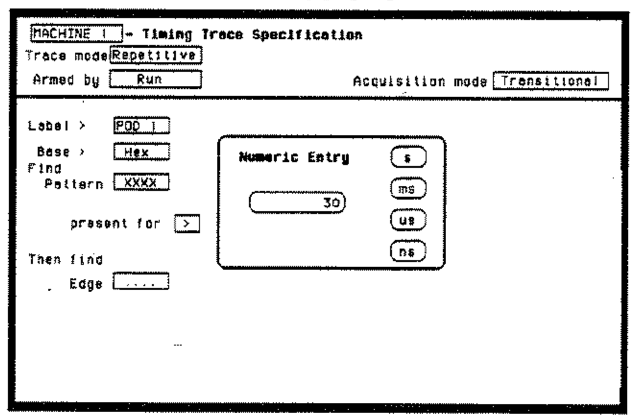


Figure 3-7. Numeric Entry Pop-Up

You enter a new value from the keypad. When you have entered your desired value, you can change the units (i.e., ns, µs, ms, s) by rotating the KNOB.

Once you select the new value and the units, close the pop-up by pressing SELECT. The new value and the units will be displayed in the **present for** ______ field.

In all numeric entry fields except the pod threshold field, you can open the pop-up without pressing SELECT. To open the pop-up without pressing SELECT, place the cursor on the field and press any number that particular field accepts. The pop-up will appear with the new number in the pop-up.

Note

You must remember that any time the cursor is on one of the numeric entry fields and you unintentionally press a key that the field accepts, the pop-up will appear and the number you pressed will replace your current value. To close the pop-up and return the original value, press the CLEAR ENTRY key.

How to Enter Alpha Data

You can customize your analyzer configuration by giving names to several items.

The items that can be named are:

- The name of each analyzer
- Labels
- Symbols
- Filenames
- File descriptions

For example, you can give each analyzer a name that is representative of your measurement. The default names for the analyzers within the logic analyzer are MACHINE 1 and MACHINE 2. To rename an analyzer, place the cursor on the name you wish to change in the System Configuration menu and press SELECT. You will see the Alpha Entry pop-up menu:

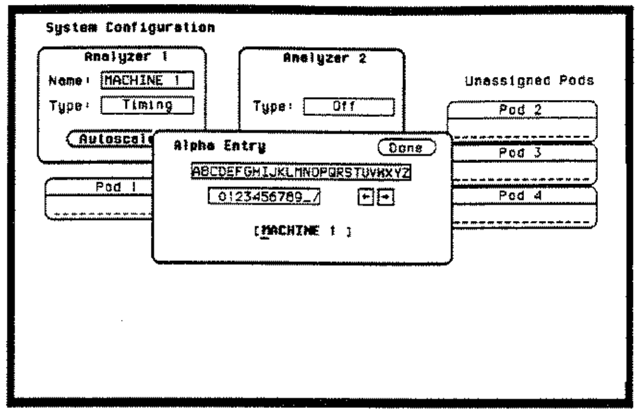


Figure 3-8. Alpha Entry Pop-Up

The top two lines enclosed in boxes in the pop-up contain the complete alphanumeric set you use for names in these types of fields. The bottom line (enclosed in brackets) contains the name that existed when you opened the Alpha Entry pop-up. To enter alpha characters in the brackets (where the default or old name appears) position the cursor on the desired character and press SELECT. The new character will be placed in the brackets where the underscore marker is located. If you want to place a new character in the brackets at a location not marked by the underscore marker, move the underscore marker to where you want the new character to be placed. Moving the underscore marker is explained in "Changing Alpha Entries" in this chapter.

Note You can also make direct keypad entries. Your selection will be placed where the underscore marker is in the box.

Changing Alpha Entries

To make changes or corrections in the Alpha Entry field, position the underscore marker under the character you want to change.

To move the underscore marker to the left, place the cursor over the left arrow and press SELECT once for each backspace.

To move the underscore marker to the right, you either place the cursor on a desired character and press SELECT, or place it on the right arrow and press SELECT.

You can also use the ROLL keys and the KNOB to move the underscore marker. To use this alternate method press the left/right ROLL key and rotate the KNOB until the underscore marker is under the desired character. To return the KNOB to controlling the cursor's movement, press the left/right ROLL key again or press SELECT.

If you want to erase the entire entry and place the underscore marker at the beginning of the name box, press the CLEAR ENTRY key on the front panel.

If you want to replace a character with a space, place the underscore marker under that character and press the DON'T CARE key on the front panel.

How to Roll Data

To roll data, you press either the left/right or up/down ROLL keys and rotate the KNOB. The roll function is only available when there is more data in the menu than can fit on screen. If there is off-screen data, pressing the ROLL keys causes an indicator to appear in the upper left corner of the display and activates the roll function of the KNOB. If there is no off-screen data, the indicator will not appear.

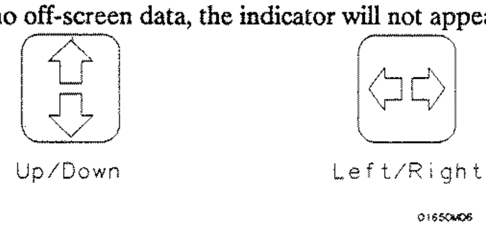


Figure 3-9. Roll Function Keys

One example of a menu with off-screen data is the STATE LISTING menu. The state listing can contain up to 1024 lines; however, the display is only capable of showing you 16 lines at a time. To roll the off-screen data, press the up/down ROLL key and then rotate the KNOB to view the off-screen data.

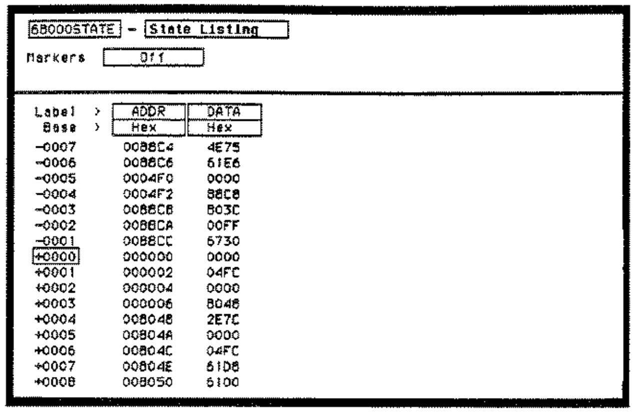


Figure 3-10. Typical State Listing Menu

Assignment/ Specification Menus

There are a number of pop-up menus in which you assign or specify what you want the logic analyzer to do. The basic menus of this type consist of:

- Assigning pod bits to labels
- Specifying patterns
- Specifying edges

Assigning Pod Bits to Labels

The bit assignment fields in both state and timing analyzers work identically. The convention for bit assignment is:

* (asterisk) indicates assigned bits
. (period) indicates un-assigned bits

An example of assigning bits is in either the Timing or State Format Specification menu.

Note

If you don't see any bit assignment fields, it merely means you don't have any pods assigned to this analyzer. Either switch analyzers or assign a pod to the analyzer you are working with.

To assign bits in these menus, place the cursor on one of the bit assignment fields and press SELECT. You will see the following pop-up menu:

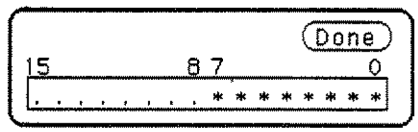


Figure 3-11. Bit Assignment Pop-Up

Place the cursor on the left-most asterisk or period in the pop-up that you want to change and press SELECT. The bit assignment will toggle to the opposite state of what it was when the pop-up opened and move the cursor one bit to the right. Holding the SELECT key repeats bit assignment. You close the pop-up by placing the cursor on Done and pressing SELECT.

Specifying Patterns

The Specify Patterns fields appear in several menus in both the timing and state analyzers. Patterns can be specified in one of the available number bases, except ASCII.

The convention for "don't cares" in these menus is an "X" except in the decimal base. If the base is set to decimal after a "don't care" is specified, a $ will be displayed.

An example of a Specify Patterns field is the Find Pattern_____ field in the Timing Trace Specification menu.

When you place the cursor on the Find Pattern _____ field and press SELECT, you will see the following pop-up menu:

Figure 3-12. Find Pattern ________ field Pop-Up

When the pop-up is open, you enter your desired pattern from the keypad (including don't cares). When you finish entering your pattern, close the pop-up by pressing SELECT.

Specifying Edges

You can select positive-going (↑), negative-going (↓), or either edge (↕) as part of your trigger specification. You specify edges in the Timing Trace Specification menu by placing the cursor on the Then find Edge . . field under the desired label and pressing SELECT. You will see the following menu:

Figure 3-13. Edge Pop-Up

You will notice a number of periods in the pop-up menu. Each period represents an unassigned bit for each bit assigned to the label. Don't be alarmed if you see a different number of unassigned bits, it merely means the number of bits in your label is different than the number in the label for this example.

To select a desired edge, place the cursor on your desired bit position in the pop-up and press SELECT until you see the desired edge, or unassign (.) the bit. Pressing SELECT changes the bit sequentially from (.) to ↓ to ↑ to ↕ and back to (.).

When you finish your edge specification, place the cursor on Done and press SELECT. This closes the pop-up and places your edge specification in the menu field.

Note

When you close the pop-up after specifying edges, you will see dollar signs ($ $ . .) in the Then find Edge field if the logic analyzer can't display the edges correctly. This indicates the logic analyzer can't display the data correctly in the number base you have selected.

4

System Configuration Menu

Introduction

This chapter describes the System Configuration menu and pop-up menus within the System Configuration menu.

The purpose and functions of each field are explained in detail, and we have included illustrations and examples to make the explanations clearer.

System Configuration Menu

The System Configuration menu can be considered a system level menu in that it contains fields that you use to start the configuration process for both analyzer 1 and analyzer 2. You use this menu to:

- Specify analyzer type (timing and state)
- Assign pods to the individual machines within the logic analyzer
- Initiate Autoscale in the timing analyzer
- Name each analyzer

It is in this menu that you configure your logic analyzer in one of four ways:

- Timing analyzer only
- State analyzer only
- Two state analyzers
- One timing analyzer and one state analyzer

The System Configuration menu for the HP 1650B Logic Analyzer is shown below. The menu for the HP 1651B is similar except that there are only two pods, with Pod 2 assigned to Analyzer 2.

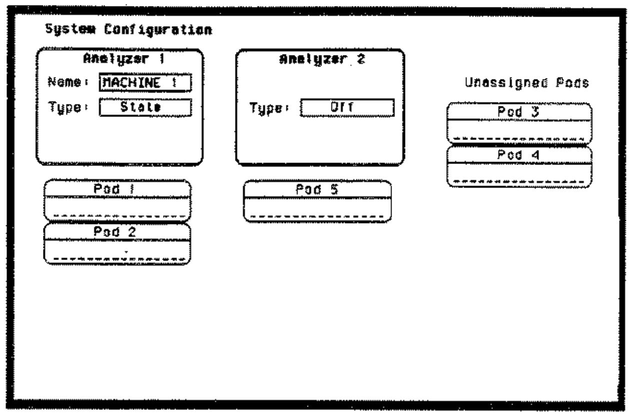


Figure 4-1. System Configuration Menu (HP 1650B)

Accessing the System Configuration Menu

The System Configuration menu is the default display when the logic analyzer is turned on and the operating system has loaded. Once the logic analyzer is on and you are in a menu other than the System Configuration menu, you access the System Configuration menu by placing the cursor in the field in the upper left corner and press SELECT. This field will be displaying either Machine 1, Machine 2, or a user-defined name for the current machine before you press SELECT.

You then place the cursor on **System** in the pop-up menu and press SELECT. When the pop-up closes the System Configuration menu will be displayed.

System Configuration Menu Fields

The System Configuration fields are described in the follow paragraphs. The fields are:

- Name
- Type
- Autoscale
- Pods

Name

You name an analyzer by selecting the **Name** field under it. An Alpha Entry pop-up menu will open. The pop-up contains a row of alpha characters, a row of numeric characters, two arrows, and a box at the bottom of the menu in which the name appears. In the name box is an underscore marker. This marker indicates in what space your next selection will be placed.

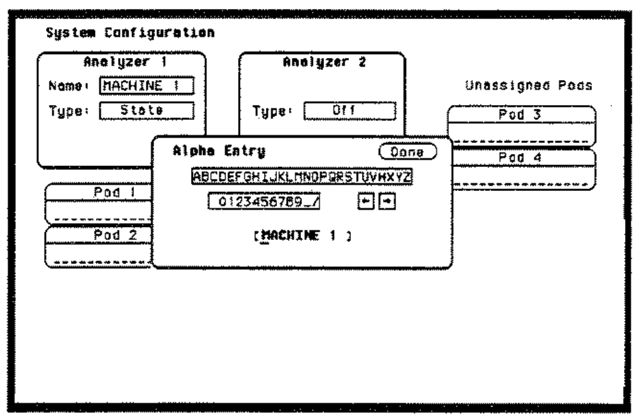


Figure 4-2. Name Pop-Up Menu

You can name the analyzer in one of two ways. The first way is to position the cursor over the desired character in the pop-up using the KNOB, then press SELECT. The character appears in the name box.

The second method is to use the keypad on the front panel. With this keypad you can enter the letters A through F and the numbers 0 through 9 instead of using the characters in the pop-up.

The arrows in the pop-up move the underscore marker forward or backward. To move the marker forward, position the cursor over the right-pointing arrow and press SELECT. To backspace the marker position the cursor over the left-pointing arrow and press SELECT.

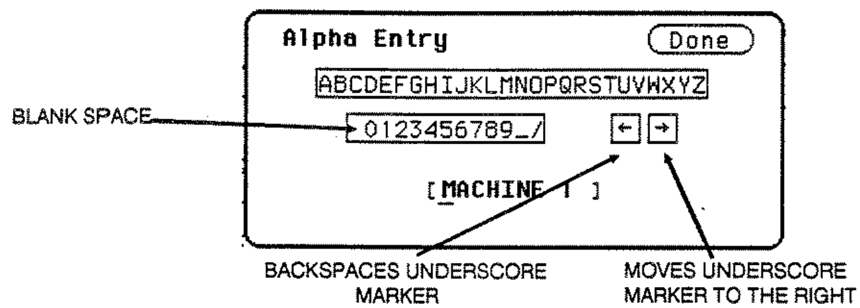


Figure 4-3. Alpha Entry Pop-Up Menu

You can also move the underscore marker with the ROLL keys and the KNOB. Pressing the left/right ROLL key activates the marker. Rotating the KNOB places the marker under the desired character.

You can replace a character with a space in one of two ways. Position the cursor over the space in the pop-up and press SELECT, or press the DON'T CARE key on the front panel.

If you want to erase the entire entry and place the underscore marker at the beginning of the name box, press the CLEAR ENTRY key on the front panel.

When you have entered the correct name, position the cursor over **Done** and press SELECT.

Type

The **Type** field defines the machine as either a state analyzer or a timing analyzer or indicates that a system performance analysis (SPA) can be done by that analyzer (optional). When this field is selected, a pop-up menu appears. You choose the machine type by using the KNOB to move the cursor within the menu to the desired selection and pressing SELECT.

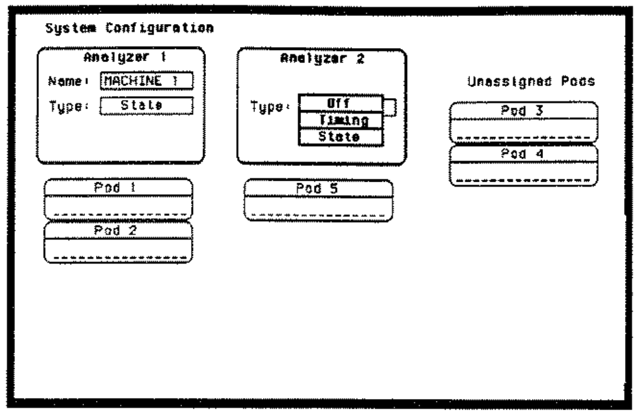


Figure 4-4. Type Pop-Up Menu

Autoscale

The purpose of **Autoscale** is to provide a starting point for setting up a measurement. The Autoscale field only appears on a timing analyzer. When you select **Autoscale**, you will see a pop-up with two options: **Cancel** and **Continue**. If you select Cancel, the autoscale is cancelled and control is returned to the **System Configuration** menu.

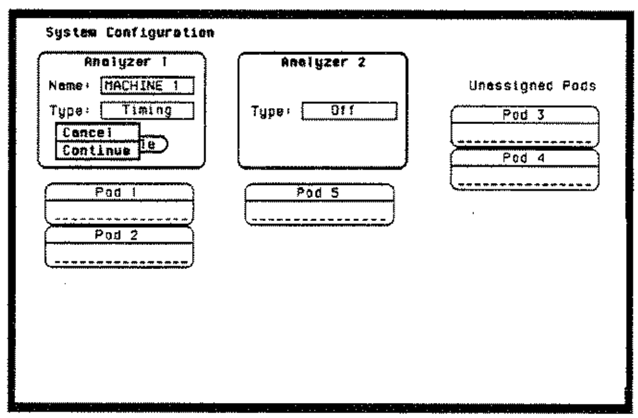


Figure 4-5. Autoscale Pop-Up Menu

If you choose Continue, autoscale configures the Timing Format, Trace Specification, and the Timing Waveforms menus. Any previous configuration that you have done will be lost. Autoscale searches for channels with activity on the pods assigned to the timing analyzer and displays them in the Waveforms menu.

Note

Choosing Autoscale erases all previous configurations for your timing analyzer and turns the other analyzer off if it was on. If you don't want this to happen, select Cancel in the pop-up.

Pods

Each pod can be assigned to one of the analyzers. When the HP 1650B Logic Analyzer is powered up, Pod 1 is assigned to Analyzer 1 and Pod 5 is assigned to Analyzer 2. When the HP 1651B is powered up, Pod 1 is assigned to Analyzer 1 and Pod 2 is assigned to Analyzer 2.

To assign a pod, position the cursor on one of the pod fields and press SELECT. With the pop-up that appears, you can assign the pod to Analyzer 1 , Analyzer 2 , or Unassign it. Pressing the SELECT key closes the pop-up.

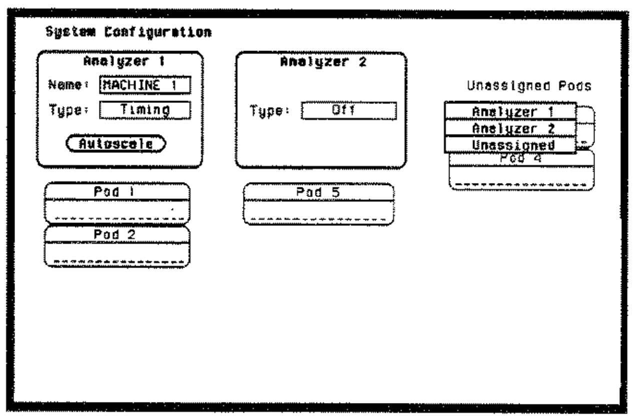


Figure 4-6. Pod Assignment Pop-Up Menu

Where to Go Next

When you complete the system level configuration for the logic analyzer in this menu, you need to complete the individual analyzer configurations for analyzer 1, analyzer 2, or both. To configure an individual analyzer you will normally configure the Format menu first and then the Trace menu.

For the timing analyzer start with chapter 8, "The Timing Analyzer." For the state analyzer start with chapter 13, "The State Analyzer."

5

I/O Menu

Introduction

This chapter describes the I/O and pop-up menus that you will use on your logic analyzer. The purpose and functions of each menu are explained in detail, and we have included many illustrations and examples to make the explanations clearer.

The I/O menu allows you to perform I/O tasks with your logic analyzer. The tasks you can do with this menu are:

- Print screens and data listings
- Perform disk operations
- Configure the HP-IB Interface
- Configure the RS-232C Interface
- Enable the analyzer to perform external triggering
- Run self tests on the analyzer

These menus and their functions are described in the following pages.

Accessing the I/O Menu

You can access the I/O menu from any other menu in the system by pressing the **I/O** key on the front panel. Use the KNOB to roll the cursor through the menu. When the cursor is positioned over the option you desire, press SELECT. It lists these seven options:

- Done
- Print Screen
- Print All
- Disk Operations
- I/O Port Configuration
- External BNC Configuration
- Self Tests

To exit the I/O menu, position the cursor over the **Done** option and press SELECT. This returns you to the menu you were in before you pressed the I/O key.

The other six options will be covered in detail in the remainder of this section.

Print Screen

When you select the **Print Screen** option, the information on the screen is frozen and the message "PRINT in progress" appears at the top of the display. This message will not print. Only the STOP key is operational while data is being transferred to the printer. If you wish to stop a printout before it is completed, press the STOP key.

Print All

The **Print All** option prints not only what is displayed on screen but what is below, and, in the Format Specification, what is to the right of the screen at the time you initiate the printout.

Note

Make sure the first line you wish to print is on screen when you select Print All. Lines above screen will not print.

Use this option when you want to print all the data in menus like:

- Timing Format Specification
- State Format Specification
- State Trace Specification
- State Listing
- Disk Directory
- Symbols

If there is information below the screen, the information will be printed on multiple pages. In Timing and State Format Specifications, the print will be compressed when necessary to print data that is off-screen to the right.

When you select the Print All option, the information on the screen is frozen, and the message "PRINT in progress" appears at the top of the display. This message will not print. If you wish to stop the printout before it is completed, press the STOP key on the front panel.

Disk Operations

The Disk Operations option allows you to perform operations on your disk and with the files on your disk. For example, you can load a file from your disk, store a file to your disk, or format a disk. The following pages describe the disk operations. For additional information on the disk operations, refer to Chapter 6, "Disk Drive Operations."

When you select Disk Operations , a new menu pops up. This menu is divided in two sections separated by a horizontal line. The top section displays the disk operation that is to be performed and the file or files that will be affected.

The bottom section displays the files on the disk in alphabetical order. It also states the type of the file and a description, if one was specified at storage. If no disk is in the disk drive or if the disk is not a supported format, the appropriate message will be displayed.

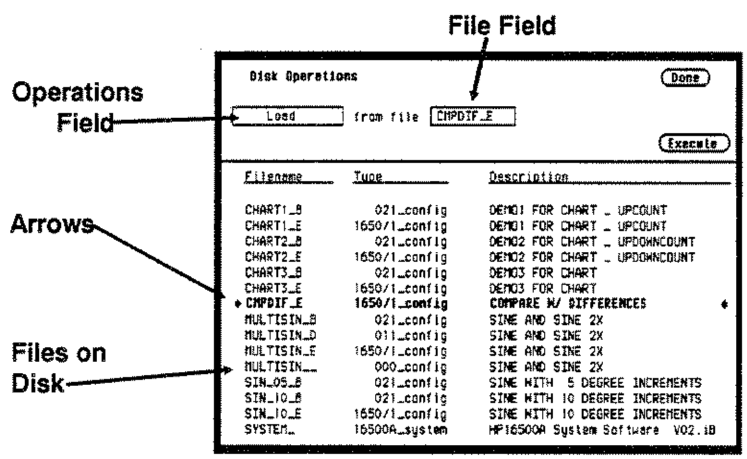


Figure 5-1. Disk Operations Menu

Halfway down the bottom display are arrows at each side of the screen. These arrows tell you which file is to be operated on. To roll through the list of files, press the up/down ROLL key and rotate the KNOB. The file that is between the arrows in boldface type also appears in the FILE field in the top section of the display.

The top section of the menu contains different types of fields. Pressing the Done field exits the Disk Operations menu and the I/O menu, returning you to the menu you were in before you pressed the I/O key. The field on the left-most side of the display is the operations field. It tells you which disk operation is to be performed. Next to that will usually be one or two file fields that tell you which file or files are to be acted upon. For several operations another field will appear in the top section.

The Execute field executes the disk operation appearing in the operations field. For non-destructive operations, when Execute is selected the operation is immediately performed. For destructive operations a pop-up appears with two options: Cancel and Continue. Cancel lets you change your mind before the action is taken preventing any data from being lost mistakenly. Continue executes the operation.

If you select the operations field, you will see a pop-up menu with nine options for disk operations, as shown. Each operation will now be discussed in detail.

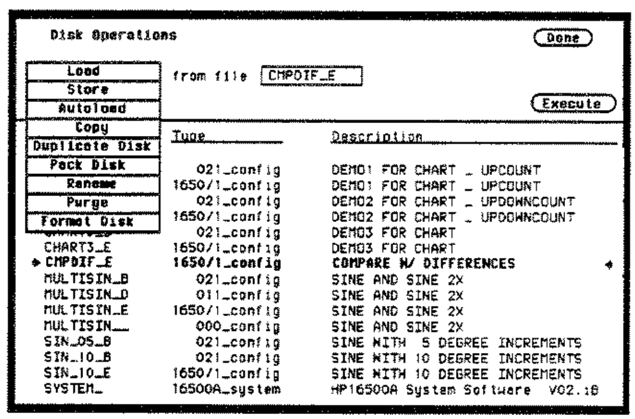


Figure 5-2. Disk Operations Pop-Up Menu

Load

The Load operation allows you to load configuration files (including symbol tables), and inverse assemblers from a disk. Executing a Load operation loads the logic analyzer with the file whose name appears in the file field in the top section of the Disk Operations menu. Loading symbols or inverse assemblers replaces those that are linked to the current configuration.

When a Load operation is executed, a message "Loading file from disk" appears at the top of the display. After the file has been loaded, this message is replaced by "Load operation complete."

Figure 5-3. Load Operation

Store

The Store operation allows you to store all the set-up information, data and inverse assembler links for the analyzer in a configuration file. You cannot store information for only one of the internal analyzers. The information and data present in the logic analyzer at the time the Store is initiated is stored on the disk.

When you select Store from the operations pop-up menu, the top section of the Disk Operations menu looks similar to that shown in figure 5-4. In addition to the operations and file fields, there is a File description field. You can write an optional description of the file you are storing in this field. A file description is not necessary but may help identify a file in the future.

When you name the file that you are storing, you must begin the file name with a letter. The name can contain up to ten characters. It can be any combination of letters and numbers, but it cannot contain any spaces.

Entering a file description is similar to naming a file with three exceptions: you can enter up to 32 characters, start the description with a number, and enter spaces.

When you Execute the Store operation, the message "Storing configuration to disk" appears at the top of the display. After the file has been stored, the message is replaced with "Store operation complete" and the file name appears in the bottom section of the Disk Operations menu with its file type and a description, if you gave it one.

Figure 5-4. Store Operation

Autoload

The Autoload operation allows a specified configuration file to be loaded at power up. When you select Autoload, the top section of the Disk Operations menu looks similar to that shown below. A field appears next to the operation field. When you select this field, a pop-up menu appears with the choices Enable and Disable . Enable causes the specified file to be automatically loaded at power up. Disable prevents any file from being loaded at power up.

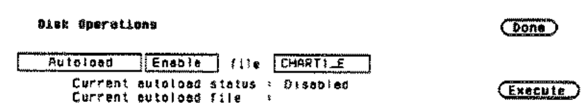


Figure 5-5. Autoload Operation

The file name in the file field can be changed with one of two methods. One method is to press the up/down ROLL key and rotate the KNOB to scroll through the list of files until the name of the desired file appears in the file field. The other method is to select the file field and use the Alpha Entry pop-up menu and the front-panel keypad to enter the name.

Below the operations and file fields are two information lines. The first line indicates the status of autoload (Enable or Disable), and the second line tells you which file, if any, is enabled for autoload. When you select either Enable or Disable the autoload status of a file will not change until you select Execute.

When you select Execute, after selecting Enable, the file whose name appears in the file field is selected for autoloading. The autoload status line will say **enabled**, and the autoload file line will state the name of the file. Also, a file labeled AUTOLOAD is added to the bottom section of the display. This file is not a configuration file. It contains information the logic analyzer needs to load the chosen file at power up. If you disable autoloading, the file labeled AUTOLOAD does not disappear. You must Purge it to erase it from your disk. The Purge disk operation is covered later in this chapter. If Autoload is disabled, the logic analyzer will load the default configuration at power up.

Copy

The Copy operation allows you to copy a file to the same disk or to another disk. When you select Copy, the top section of the Disk Operations menu will look similar to that below.

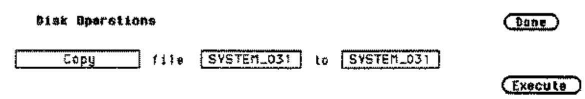


Figure 5-6. Copy Operation

Notice that there are two file fields. You can specify the file you are copying from and the file you are copying to. When you select either file field, you will get an Alpha Entry pop-up menu. You can use this menu and the keypad on the front panel to enter the name of the file. For the file that you are copying from, it is usually easier to use the up/down ROLL key and the KNOB to select one of the files on the disk rather than to use the Alpha Entry menu.

When you select Execute you will see a pop-up that tells you to insert the disk onto which you want to copy the file. There are also two fields in the pop-up. One is labeled **Continue**. You select Continue after you have inserted the disk and are ready to copy the file. The other field is labeled **Stop**. Selecting the Stop field halts the copy and returns you to the Disk Operations menu.

If you insert the destination disk and select **Continue**, the file will be copied. If the file is long, you might have to swap the source and destination disks again. The logic analyzer tells you if you need to reinsert the source disk to continue copying the file. You can also copy to the same disk, making the source and destination disk the same.

Duplicate Disk

The Duplicate Disk operation allows you to duplicate all the files on one disk to another. When you select this option, only the operations field appears in the top section of the Disk Operations menu. The disk is automatically formatted in this operation.

Figure 5-7. Duplicate Disk Operation

When you select Execute, you will see a pop-up with a message telling you what occurs when a disk is duplicated. The pop-up also contains two fields: Cancel and Continue. Cancel stops the duplicating process and returns you to the Disk Operations menu. Continue executes the operation. If you select **Continue**, the display goes blank except for the message "Insert source disk - hit select when ready." Insert the disk you want to duplicate and press SELECT. After the logic analyzer reads the disk, it displays the message "Insert destination disk - hit select when ready." Insert the disk to which you want to copy and press SELECT. The analyzer will tell you that it's writing to the disk.

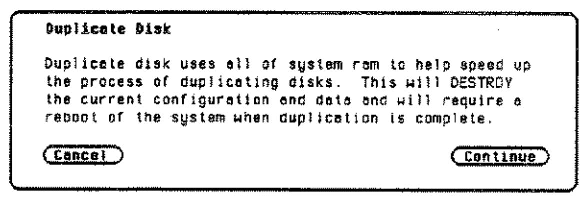


Figure 5-8. Duplicate Disk Pop-Up Menu

The process of duplicating a disk is an iterative one; i.e., more than one swapping of disks may be necessary before all files are transferred. If this is the case the logic analyzer will repeat the message telling you to insert the source disk. Insert the source disk and press SELECT. The analyzer remembers where it stopped duplicating the first time and starts reading from that location. When the analyzer is ready, insert the destination disk and press SELECT. You will never have to swap disks more than three times.

After the duplication process is complete, the logic analyzer displays a message telling you what to do next. If you want to copy another disk, press the FORMAT key on the front panel. The analyzer will repeat its message to insert the source disk. If you do not want to copy any more disks, insert the system disk and press the SELECT key. This reboots the system.

Note

Duplicating a disk destroys any existing configurations and data on the destination disk. Make sure that the disk to which you are duplicating is the correct disk.

Pack Disk

The Pack Disk operation reorganizes the files on the disk, making room for more. When files are purged, blank areas appear on the disk (between files) that are too small for the new files you are creating. Packing the disk packs the current files together, removing unused areas from between the files so that more space is available for files at the end of the disk..

When you select **Pack Disk**, the top section of the Disk Operations menu looks similar to that shown below. Selecting Execute starts the process. After the packing is completed, the message "Disk packing complete" appears at the top of the screen.

Figure 5-9. Pack Disk Operation

Rename

The Rename operation lets you rename a file. When you select this option, the display will look similar to that shown in figure 5-10.

You will see a file field that tells you what the current name of the file is, and a file field that allows you to specify what the new name will be. If you select either one of the file fields, an Alpha Entry pop-up menu appears. You can use this menu and the keypad on the front panel to enter the name of the file. For the field with the old file name, it is usually easier to use the up/down ROLL key and the KNOB to select the desired file rather than to use the Alpha Entry pop-up menu.

To start the rename operation, select Execute . The file will be renamed and relocated alphabetically in the file list in the bottom section of the Disk Operations menu.

If you try to rename a file with a name that already exists, a message will tell you that a file already exists with that name, and the file will not be renamed.

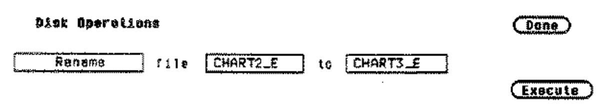


Figure 5-10. Rename Operation

Purge

The Purge operation allows you to delete a file from a disk. When you select this option, the display will look similar to that shown below.

The file field contains the name of the file to be purged. You can change the file in this field either by positioning the cursor on the field and selecting it to access an Alpha Entry pop-up menu, or by using the up/down ROLL key and the KNOB to move among the files.

When you select Execute you will see a pop-up with the choices **Cancel** and **Continue**. Cancel lets you stop the Purge operation and returns you to the Disk Operations menu. Continue purges the file whose name appears in the file field.

Note

A purged file cannot be recovered. Make sure the file that is being purged is the correct one.

Figure 5-11. Purge Operation

Format Disk

The Format Disk operation formats a disk, purging all previous files on the disk. When you select this option, the display will look similar to that shown in figure 5-12.

Selecting **Execute** gives you a pop-up with the choices **Cancel** and **Continue**. **Cancel** stops the format operation and returns you to the Disk Operation menu. If you select **Continue,** the disk will be formatted. The message "Disk format in progress" will appear at the top of the screen. When the formatting is complete, all the files will be deleted.

Note

Formatting a disk purges all the files on the disk. Make sure the disk is the correct one to be formatted because purged files cannot be recovered.

Figure 5-12. Format Disk Operation

I/O Port Configuration

The I/O Port Configuration option in the I/O menu enables you to configure the logic analyzer for sending configuration, waveforms and listings to a printer or controller via HP-IB or RS-232C.

When you place the cursor on the External I/O Configuration option and press SELECT, you will see the menu shown in figure 5-13.

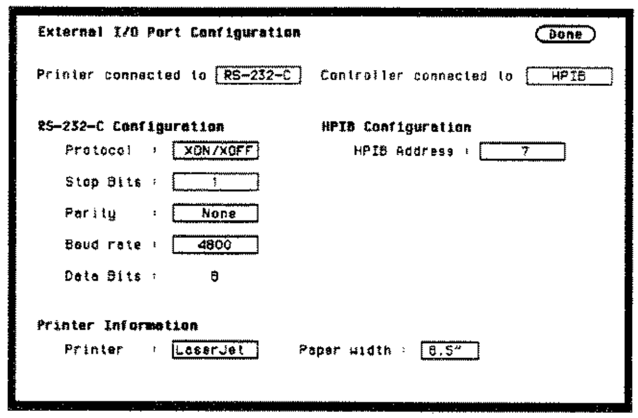


Figure 5-13. External I/O Port Configuration Menu

The HP 1650B/51B is equipped with a standard RS-232C interface and an HP-IB interface that allows you to connect to a printer or controller. Connecting a controller gives you remote access for running measurements, up-loading and down-loading configurations and data, and outputting to a printer. The controller interface is explained in more detail in the *HP 1650B/51B Programming Reference Manual.*

Various HP-IB and RS-232C graphics printers can be connected to the logic analyzer. Configured menus as well as waveforms and other data can be printed for complete measurement documentation. The printer interface is explained in more detail in Chapter 7, "Making Hardcopy Prints."

Configuring the Interfaces

You configure the HP-IB or RS-232C interfaces for a controller or a printer by first selecting the I/O menu. Then you select the **I/O Port Configuration** field to display the External I/O Port Configuration menu. When the menu appears, select either field at the top of the menu to switch the interfaces between a printer and a controller. Whenever you change the configuration for one interface, the other interface automatically changes to the opposite configuration.

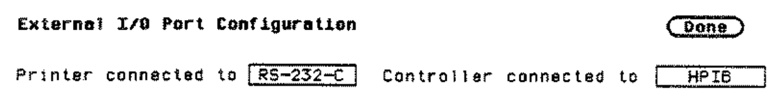


Figure 5-14. Interface Configurations

The HP-IB printer must be set to **Listen Always** for the HP-IB interface. In this mode, no HP-IB addressing is necessary. There are two fields at the bottom of the menu that allow you to select the printer type and paper width.

The HP-IB Interface

The Hewlett-Packard Interface Bus (HP-IB) is Hewlett-Packard's implementation of IEEE Standard 488-1978, "Standard Digital Interface for Programmable Instrumentation." The HP-IB is a carefully defined interface that simplifies the integration of various instruments and computers into systems. It uses an addressing technique to ensure that each device on the bus (interconnected by HP-IB cables) receives only the data intended for it. To accomplish this, each device is set to a different address and this address is used to communicate with other devices on the bus.

Selecting an Address. The HP-IB address can be set to 32 different HP-IB addresses, from 0 to 31. Simply choose an address that is compatible with your device and/or software. The default is 7.

To select an address:

1. Select the External I/O Port Configuration menu and place the cursor in the field directly to the right of **HP-IB Address:**. Press SELECT and an Integer Entry pop-up appears as shown in figure 5-15.

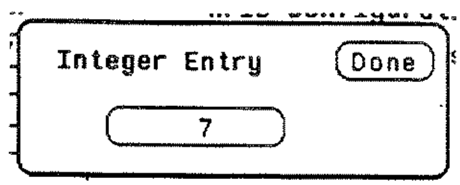


Figure 5-15. Integer Entry Pop-Up Menu

2. When the pop-up appears, either rotate the knob or use the keypad to enter the address. If you enter an address greater than 31, the address will default to 31 when you select **Done**.

3. When you are finished entering the HP-IB address, select **Done**. The pop-up closes, placing your selection in the appropriate field.

The RS-232C Interface

The RS-232C interface in this instrument is Hewlett-Packard's implementation of EIA Recommended Standard RS-232C, "Interface Between Data Terminal Equipment and Data Communications Equipment Employing Serial Binary Data Interchange." With this interface, data is sent one bit at a time and characters are not synchronized with preceding or subsequent data characters. Each character is sent as a complete entity without relationship to other events.

Protocol. Protocol governs the flow of data between the instrument and the external device. The protocol options are **None** and **XON/XOFF**. The default setting is XON/XOFF.

Figure 5-16. Protocol Pop-Up Menu

With less than a 5-wire interface, selecting **None** does not allow the sending or receiving device to control how fast the data is being sent. No control over the data flow increases the possibility of missing data or transferring incomplete data. With a full 5-wire interface, selecting **None** allows a hardware handshake to occur. With a hardware handshake, hardware signals control data flow. The HP 13242G cable allows the HP 1650B/51B to support hardware handshake.

With **Xon/Xoff**, the receiver controls the data flow. By sending XOFF (ASCII decimal 19) over its transmit data line, the receiver requests that the sender disables data transmission. A subsequent XON (ASCII decimal 17) allows the sending device to resume data transmission.

Data Bits. Data bits are the number of bits sent and received per character that represent the binary code of that character. The HP 1650B/51B supports 8-bit only.

Stop Bits. Stop bits are used to identify the end of the character. The number of stop bits must be the same for both the controller and the logic analyzer. The options are **1**, **1.5**, or **2** stop bits per character. The default setting is 1.

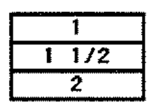


Figure 5-17. Stop Bits Pop-Up Menu

Parity. The parity bit detects errors as incoming characters are received. If the parity bit does not match the expected value, the character is assumed to be incorrectly received. The action taken when an error is detected depends on how the interface and the device program are configured.

Parity is determined by the requirements of the system. The parity bit may be included or omitted from each character by enabling or disabling the parity function. The options are **None**, **Odd**, or **Even**. The default setting is None.

Figure 5-19. Parity Pop-Up Menu

Baud Rate. The baud rate is the rate at which bits are transferred between the interface and the peripheral. The baud rate must be set to transmit and receive at the same rate as the peripheral, or data cannot be successfully transferred. The available baud rates are 110 to 19200. The default setting is 9600.

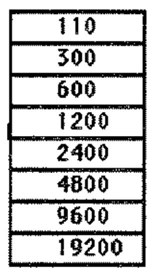


Figure 5-18. Baud Rate Pop-Up Menu

Printer. You can specify which printer you are using by selecting the **Printer** attribute field and choosing one of the options in the pop-up. The options are **ThinkJet**, **QuietJet**, **LaserJet**, and **Alternate**. Alternate allows you to use an Epson® compatible printer. The default printer option is **ThinkJet**.

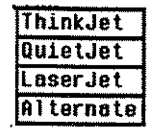


Figure 5-20. Printer Pop-Up Menu

Paper Width. The logic analyzer offers two options for paper width: **8.5** and **13.5** inches. Selecting the **Paper Width** attribute field gives you a pop-up with which you can make your choice.

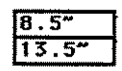


Figure 5-21. Paper Width Pop-Up Menu

The HP ThinkJet and HP LaserJet series printers require a paper width of 8.5 inches and the HP QuietJet series printers can use a paper width of 8.5 or 13.5 inches.

If 13.5 inches (132 characters per line) is selected for other than an HP Quietjet printer, the listings are printed in a compressed mode. Compressed mode uses smaller characters to allow the printer to print more characters in a given width.

If an HP Quietjet printer is used and 13.5 inches is selected, it will print a full 132 characters per line. When 8.5 inches (80 characters per line) is selected for any printer, a maximum of 80 characters are printed per line.

External BNC Configuration

On the rear panel of the logic analyzer are two BNC connectors with which you can hook the logic analyzer to other instruments. The **External BNC Configuration** option in the I/O menu identifies one of the two internal machines to be the trigger for an external instrument.

When you select this option you will see a field next to the words "BNC output armed by." Selecting this field gives you a pop-up with either two or three options. One option is **Off.** This indicates that the logic analyzer will not trigger an external instrument. The other options are the internal analyzers, listed by name. You can select the analyzer for triggering your external instrument by using the KNOB to position the cursor on the appropriate name and pressing SELECT.

If for some reason both of the internal analyzers are off, selecting the **External BNC Configuration** option gives you the message "BNC output armed by : Off (note: both machines are off)."

Self-Tests

The **Self Tests** option in the I/O menu allows you to run a self test on the logic analyzer. The self test is on the master disk. Selecting this option gives you a pop-up telling you what effect the self test has on the analyzer. The pop-up also contains two fields: **Cancel** and **Start Self Test. Cancel** lets you change your mind about running the self test. Selecting this field returns you to the I/O menu. Selecting the **Start Self Test** field causes your logic analyzer to load the self test from the disk and run through it. Before selecting this field you must insert the master disk with the self test on it.

Note

Running the self test destroys all current configurations and data. Make sure that you save any important configurations on a disk before running any of the self tests.

6 Disk Drive Operations

Introduction

This chapter describes the disk operations of the HP 1650B/51B in a task format. The disk operations are described in detail in the "Disk Operations" section of chapter 5.

The Disk Operations Available

Nine disk operations are available:

- Load - Instrument configurations and data can be loaded from the disk. Inverse assemblers can be loaded.
- Store - Instrument configurations and data can be stored on disk. System files cannot be stored.
- Autoload - Designates a configuration file to be loaded automatically the next time the HP 1650B/51B is turned on.
- Copy - Any file on the disk can be copied from one disk to another or to the same disk.
- Duplicate Disk - All files from one disk are copied to another disk. The directory and all files on the destination disk will be destroyed with this operation. The copied files are packed on the new disk as they are copied.
- Pack Disk - This function packs files on a disk. Packing removes all empty or unused sectors between files on a disk so that more space is available for files at the end of the disk.
- Rename - Any filename on a disk can be changed to another name.
- Purge - Any file on a disk can be purged (deleted) from the disk.
- Format Disk - Any two-sided 3.5-inch floppy disk can be formatted or initialized. The directory and all files on the disk will be destroyed with this operation.

Although default values are provided for these disk operations, you may have to specify additional information. This information is entered by selecting the appropriate fields displayed for each disk operation. Disk operations are initiated by selecting the Execute field. If there is a problem or additional information is needed to execute an operation, an advisory appears near the top center of the screen displaying the status of the operation (an error message prompts to swap disks, etc.).

If executing a disk operation could destroy or damage a file, another pop-up appears with the options Cancel and Continue when you select Execute. If you don't want to complete the operation, select Cancel to cancel the operation. Otherwise, select Continue and the operation will be executed.

Accessing the Disk Menu

To display the Disk Operations menu press the I/O menu key.

When the I/O pop-up menu appears, place the cursor on Disk Operations and press SELECT. You will see the Disk Operations menu.

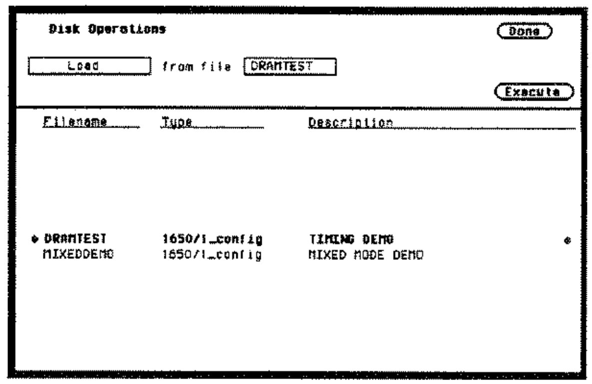


Figure 6-1. Disk Operations Menu

Selecting a Disk Operation

To select a disk operation, place the cursor on the field directly below Disk Operations and press SELECT. You will see the following pop-up:

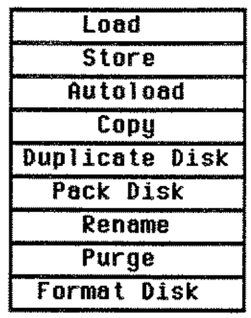


Figure 6-2. Disk Operations Pop-Up Menu

When the pop-up appears, place the cursor on the operation you want and press SELECT. After you select an option, the pop-up closes and displays the fields required for your operation. For example, select Store. The Disk Operations menu now looks like this:

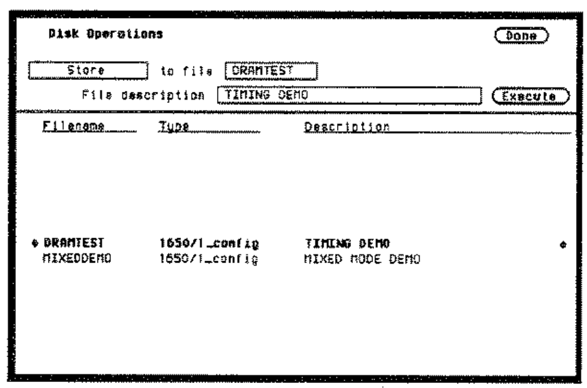


Figure 6-3. Store Operation

Disk Operation Parameters

The disk operation parameters consist of the information that the disk operation acts upon. They tell the logic analyzer the names types, and descriptions of files being manipulated. To change these parameters, select the appropriate field and the field will either toggle to the opposite function or a pop-up will appear. If a pop-up appears, select the appropriate option or enter data with the keypad.

To initiate the disk operation function you have selected, place the cursor on Execute. A pop-up appears with Continue and Cancel. To continue, place the cursor on Continue and press SELECT. To cancel place the cursor on Cancel and press SELECT. The Autoload, Pack Disk and Rename functions immediately execute since they are not destructive to the files. These functions do not give you the Cancel and Continue options.

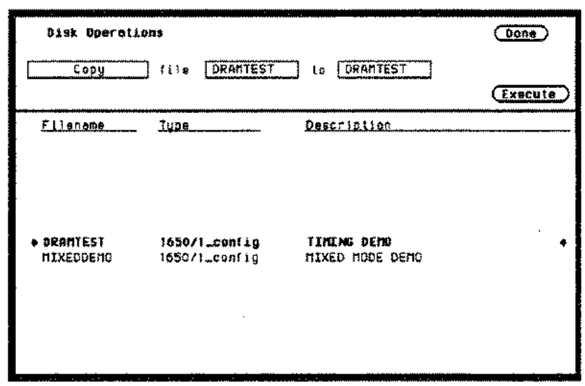


Figure 6-4. Disk Operation Parameters

Installing a Blank Disk

Included with the HP 1650B/51B is a blank 3.5-inch flexible disk for your own use. To install the blank disk, hold the disk so that the Hewlett-Packard label is on top and the metal auto-shutter is away from you. Push the disk gently, but firmly, into the front disk drive until it clicks into place.

Note

The HP 1650B/51B disk drives use the gray Hewlett-Packard double-sided disks, which can be ordered in a package of ten with the Hewlett-Packard part number 92192A. DO NOT use single-sided disks with the HP 1650B/51B.

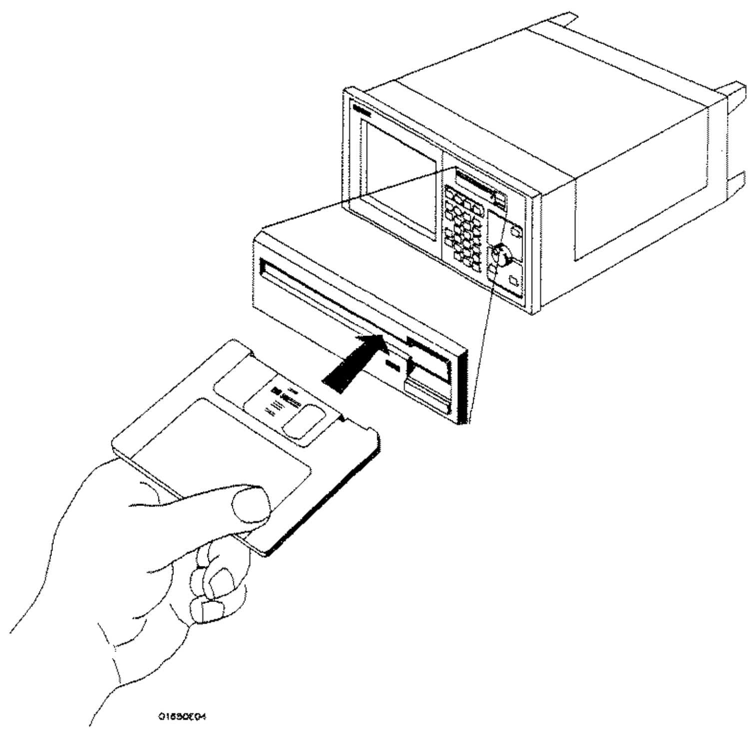


Figure 6-5. Installing a Disk

Formatting a Disk

Before any information can be stored on a new disk, you must first format it. Formatting marks off the sectors of the disk and creates the LIF (Logical Interchange Format) directory on the disk. If you initiate a Duplicate Disk operation, the logic analyzer will automatically format the destination disk.

Note

The HP 1650B/51B does not support track sparing. If a bad track is found, the disk is considered bad. If a disk has been formatted elsewhere with track sparing, the HP 1650B/51B will only read up to the first spared track.

Select the Format Disk operation.

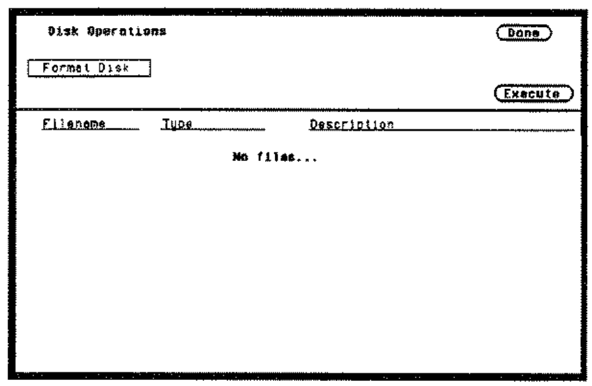


Figure 6-6. Format Disk Operation

After the Format Disk operation menu appears, the instrument reads the disk and tells its condition. One of three conditions can exist:

- If this is a new disk, or a disk formatted by a disk drive not using the LIF format, the menu will display UNSUPPORTED DISK FORMAT on the lower portion of the menu.
- If the disk is already formatted, but has no files, the menu will display No Files.

- If the disk already has files, a list of file names will appear on the lower portion of the menu along with a file type and description.

If any of the listed files need to be saved, copy them to another disk before initiating the Format Disk function. To initiate the Format Disk function, select Execute. When the pop-up appears, select Continue and the instrument will format the disk. Otherwise, select Cancel to cancel the Format Disk operation.

Caution

Once you press Continue, the Format Disk operation starts and permanently erases all the existing information from the disk. After that, there is no way to retrieve the original information.

Storing to a Disk

The Store operation allows you to store your configurations and data to a file with a description of its contents. You must assign a file name for each file in which you wish to store data.

Select the Store operation.

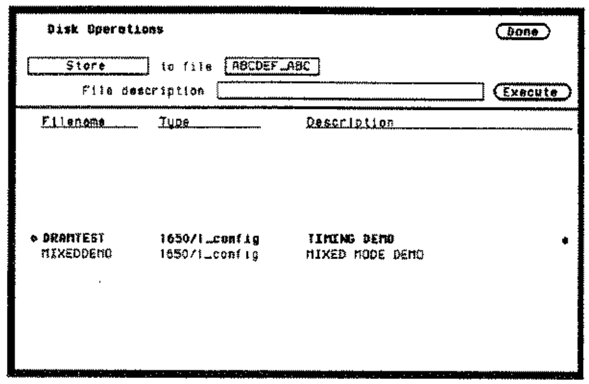


Figure 6-7. The Store Operation

To name your file, place the cursor on the field to the right of "to file" and press SELECT. The Alpha Entry pop-up appears.

Enter a filename that starts with a letter and contains up to ten characters. It can be any combination of letters and numbers, but there can be no blank spaces between any of the characters.

Entering a file description is the same process as naming a file except you can enter up to 32 characters, start the description with a number, and enter spaces between characters.

Note

The field for "file description" makes it easier to identify the type of data in each file. This is for your convenience but you can leave this field blank.

When you have completed entering the file name and file description, you initiate the store operation by placing the cursor on Execute and pressing SELECT. A pop-up appears with Continue and Cancel. To continue, place the cursor on Continue and press SELECT. To cancel, place the cursor on Cancel and press SELECT.

Caution

If you store a new configuration and data to an existing file, they are written over the original information "DESTROYING" the original information in that file.

The Load Operation

The Load operation allows you to load previously stored configuration and data from a file on the disk.

Select the Load operation.

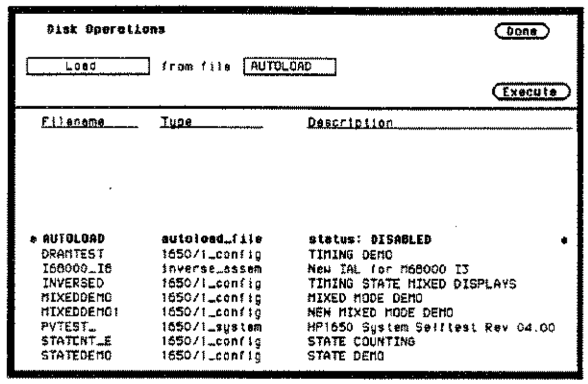


Figure 6-8. The Load Operation

Note

The Load operation is type dependent. This means that you cannot load a system file. For example, if you try to load the file "SYSTEM_," an advisory "Warning: Invalid file type" appears in the top center of the display.

To load the desired file, press the up/down ROLL key and rotate the KNOB until the desired file appears in the field to the right of "from file."

Note

Another way to enter the name of the file in the field to the right of "from file" is to select this field. When the Alpha Entry pop-up appears, enter the correct filename.

Renaming a File

The Rename operation allows you to change the name of a file. The only restriction is that you cannot rename a file to an already existing filename.

Select the Rename operation. When you have completed entering a new file name and description, you initiate the Rename operation by placing the cursor on Execute and pressing SELECT.

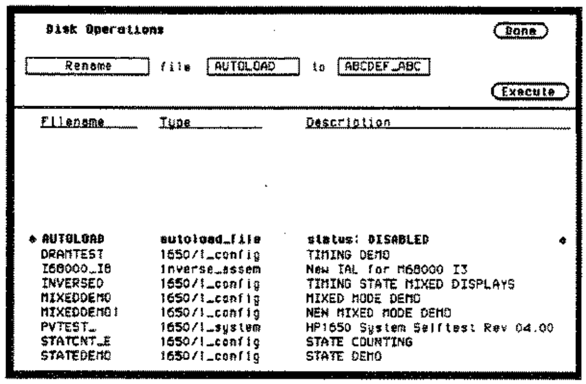


Figure 6-9. Renaming a File

Use either the KNOB or the Alpha Entry pop-up to enter the filename you wish to change in the field to the right of "file."

Move the cursor to the field to the right of "to" and press SELECT. When the Alpha Entry pop-up appears, enter the new file name. When you have completed entering the new file name, you initiate the rename operation by placing the cursor on Execute and pressing SELECT. The rename operation immediately executes and when it is completed, an advisory "Rename operation complete" is displayed.

The Autoload Operation

Autoload allows you to designate a configuration file to be loaded automatically the next time the HP 1650B/51B is turned on. When the Autoload operation is Enabled, your designated configuration file is loaded instead of the default configuration file. This allows you to change the default configuration of certain menus to a configuration that better fits your needs.

Select the Autoload operation. To Enable Autoload, select the Disable field and when the pop-up appears, select Enable.

With the up/down ROLL key and KNOB or the Alpha Entry pop-up enter the name of the configuration file you wish to load in the field to the right of "File" and select Execute. The Autoload function is Enabled as shown after "Current Autoload status:" on the display.

Note

When power is applied to the logic analyzer, Autoload On or Off is determined by the presence of an enabled autoload file on the disk. If an enabled autoload file is present on the disk, the logic analyzer will load this configuration file instead of the standard configuration file.

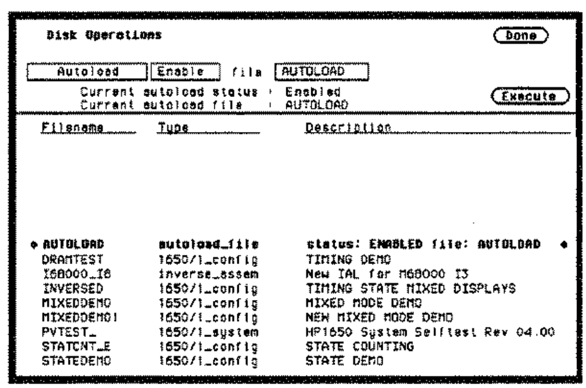


Figure 6-10. Autoload Operation Enabled

To Disable the Autoload operation, select Enable and when the pop-up appears, select Disable. When the pop-up closes, select Execute and the Autoload function is disabled.

Purging a File

Select the Purge operation to Purge (delete) a file. With either the up/down ROLL key and KNOB or the Alpha Entry pop-up enter the file you wish to purge in the field to the right of "file." Select Execute and when the pop-up appears, select Continue and the file is purged from the disk.

Caution Once EXECUTED, the Purge operation permanently erases the file. After that, there is no way to retrieve the original information.

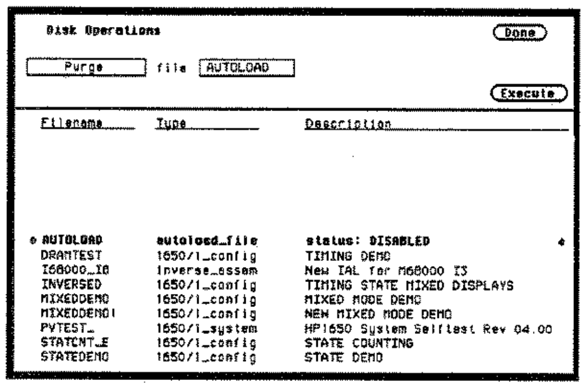


Figure 6-11. Purging a File

Copying a File

The Copy operation allows you to copy a file to the same disk or another disk. Select the Copy operation. With either the up/down ROLL key and the KNOB or the Alpha Entry pop-up, enter the filename you wish to copy in the field to the right of "file." Select the field to the right of "to" and when the Alpha Entry pop-up appears, enter the name of the file you want to "copy to."

You can also copy a file to the same filename on another disk. To do this, select the "To" filename field, press the CLEAR ENTRY key place the cursor on Done and press SELECT. This copies the original filename in the "To" filename field.

Select Execute to start the copy operation. A pop-up appears with instructions on what to do with the disks. Since you can copy a file to the same disk or another disk, simply follow the instructions as they apply to your situation and select Continue to continue.

When "Insert the destination disk" appears, remove the source disk and insert the destination disk into the disk drive if you are copying the file to another disk. The cursor is located on "Continue," so to continue, press SELECT; otherwise, place the cursor on "Stop" and press SELECT. If you are copying to the same disk, press "Continue" without moving the disk.

If the file cannot be copied in a single operation, the instruction "Insert the source disk" will appear in the pop-up. Remove the destination disk, re-insert the source disk and select Continue. The logic analyzer reads another segment of the source file. It will then tell you when to re-insert the destination disk and continue.

Note

If the source file is large (i.e., System file) you should use the Duplicate Disk operation. Duplicating large files using the Copy operation requires changing disks many times. This invites the possibility of losing track of the disk changes, which will destroy part or all of the files on the source disk.

When the copy operation is complete, you will see the new file name in the directory. The new file name will be inserted in the directory in alphabetical order.

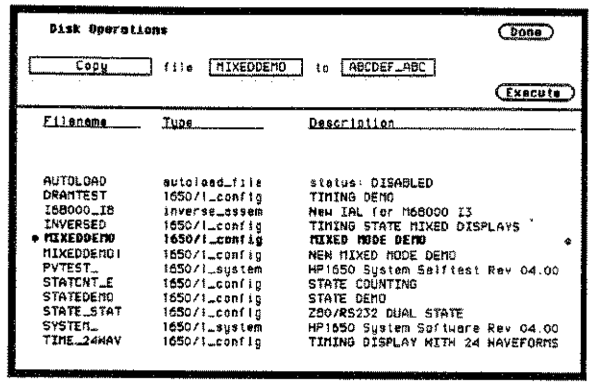


Figure 6-12. Copy File Operation

The Pack Disk Operation

By deleting files from the disk and adding other files, you end up with blank areas on the disk (between files) that are too small for the new files you are creating. The Pack Disk operation packs the current files together, removing unused areas from between the files so that more space is available for files at the end of the disk.

Select the Pack Disk operation. To pack the disk, select Execute.

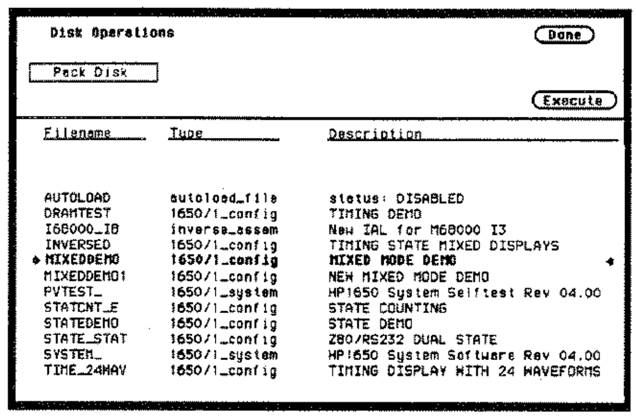


Figure 6-13. The Pack Disk Operation

Duplicating the Operating System Disk

The Duplicate Disk operation allows you to duplicate all the files on one disk to another disk. You use this operation to make a back-up copy of your important disks so you won't lose important data in the event the disk wears out, is damaged, or a file is accidently deleted.

Select the Duplicate Disk operation and press Execute. When the pop-up appears you will see the following advisory:

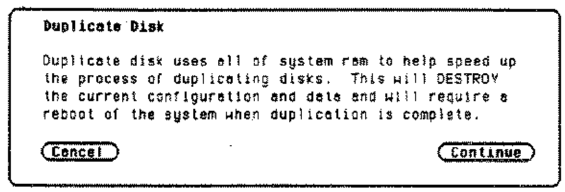


Figure 6-14. Duplicate Disk Pop-Up

Caution

The original directory and files on the destination disk are destroyed by the DUPLICATE DISK operation.

To continue, select Continue. The instruction "Insert disk to be copied-hit select when ready" will be displayed. Insert the source disk and press SELECT. The logic analyzer reads the source disk and displays "Reading from source disk. Please wait..."

When the logic analyzer has filled memory or has read the entire source disk, it displays "Insert destination disk-hit select when ready." Remove the source disk, insert the destination disk and press SELECT. When the logic analyzer starts writing to the destination disk, you will see "Writing to destination disk. Please wait..."

Note

If the destination disk has not been formatted, the logic analyzer will automatically format the disk before it writes to it.

If the amount of data on the source disk exceeds the available memory in the logic analyzer, the logic analyzer will display "Insert the source disk-hit select when ready" again, and you will need to repeat the process of inserting the source disk, then the destination disk. Follow the directions on screen until the entire disk is duplicated.

When the entire disk is duplicated, you will see "Hit FORMAT key to copy another disk or insert system disk and hit SELECT to reboot." If you are finished duplicating disks, insert the system disk and press SELECT. The logic analyzer will load the system file and return you to the System Configuration menu.

7

Making Hardcopy Prints

Introduction

The HP 1650B/51B Logic Analyzers allow you to print configurations, waveforms, and listings. Whenever your printer is connected to the logic analyzer and you instruct it to do so, it will print what is currently displayed on screen or all data in the menus having off-screen data.

This chapter shows you how to set up the logic analyzer's HP-IB and RS-232C interfaces for printers. If you have a Hewlett-Packard ThinkJet, QuietJet, or LaserJet series printer with the RS-232C interface, the RS-232C interface is already set up for you with the exception of the printer type and page width.

If you have another kind of printer, refer to your printer manual for its interface requirements and change the logic analyzer's interface configuration as instructed.

Supported Printers

The HP 1650B/51B logic analyzers will support the following printers with HP-IB or RS-232C capabilities. For the following RS-232C printers, these configurations should be used:

- HP ThinkJet (RS-232C switches set for HP controllers)
- HP QuietJet (factory settings)
- HP LaserJet (factory settings)
- Alternate

Alternate Printers

In addition to HP printers, the logic analyzers support Epson® compatible RS-232C printers. These alternate printers must support graphics.

When the logic analyzer's RS-232C configuration is set for alternate printers, it transmits data to the printer in the Epson® format.

Printers incompatible with either HP or Epson data transfer formats will not work with the HP 1650B/51B logic analyzers.

Hooking Up Your Printer

If your printer is already connected to the logic analyzer, skip to "Setting the RS-232C for HP Printers" or "Setting the HP-IB for HP Printers" in this chapter. Otherwise hooking up your HP printer is just a matter of having the correct HP-IB or RS-232C interface cable.

If you have an alternate printer, the type of connector on the printer end of the cable depends on your printer.

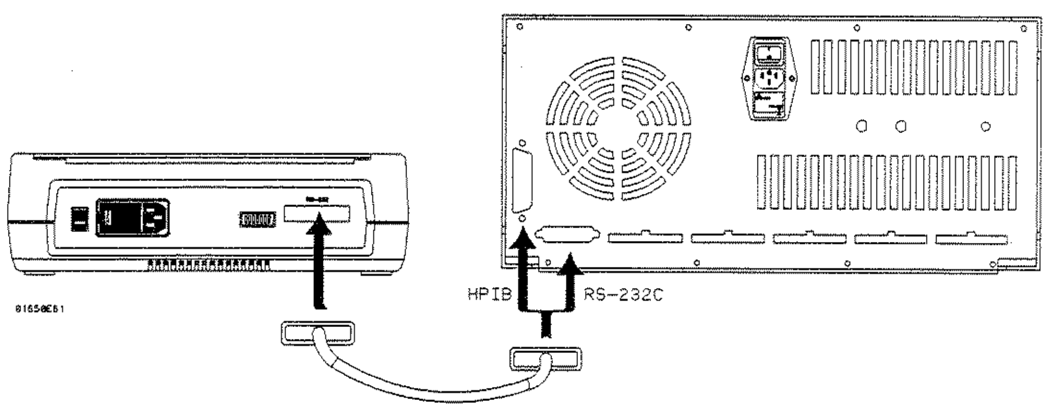


Figure 7-1. Logic Analyzer to Printer Hook-Up

HP-IB Printer Cables

You can use any standard HP-IB cable to connect the logic analyzer to the printer. The specific HP-IB cable only depends on the length you need.

RS-232C Printer Cables

You can use either an HP 13242G or HP 92219H cable to connect the logic analyzer to the printer. However, the HP 13242G is the preferred cable since it can be used with either no protocol (hardware handshake) or XON/XOFF.

HP 13242G Cable

The HP 13242G cable has standard DB-25 connectors on each end and is wired for hardware handshake. The cable schematic is shown below.

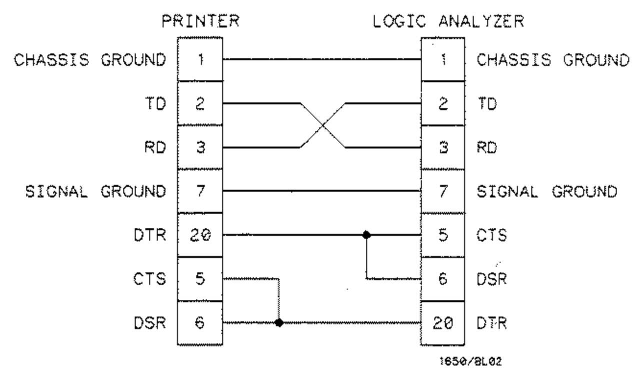


Figure 7-2. HP 13242G Cable Schematic

Note

HP 13242G cable is symmetrical, therefore it doesn't matter which end of the cable is connected to which piece of equipment.

HP 92219H Cable

The HP 92219H cable has standard DB-25 connectors on each end and is wired for XON/XOFF handshake. The cable schematic is shown below.

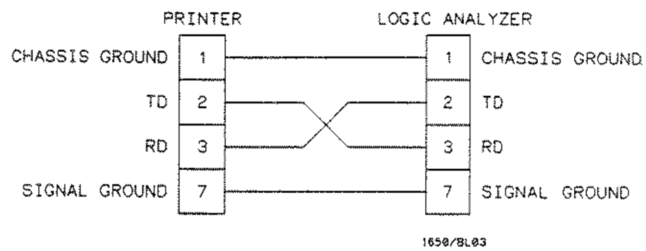


Figure 7-3. HP 92219H Cable Schematic

Setting HP-IB for HP Printers

The HP 1650B/51B interfaces directly with HP PCL printers supporting the printer command language. These printers must also support HP-IB and "Listen Always." Printers currently available from Hewlett-Packard with these features include:

- HP 2225A ThinkJet
- HP 2227B QuietJet
- HP 3630A option 002 PaintJet

Note

The printer must be in "Listen Always" when HP-IB is the printer interface. The HP 1650B/51B HP-IB port does not respond to service requests (SRQ) when controlling a printer. The SRQ enable setting for the HP-IB printer has no effect on the HP 1650B/51B operation.

For HP-IB printers, the Printer connected to field must be set to HP-IB in the I/O Port Configuration menu. You access the I/O Port Configuration menu by first accessing the I/O menu, then the I/O Port Configuration.

Setting RS-232C for HP Printers

All three series of HP printers (HP ThinkJet, HP LaserJet, and HP QuietJet) use the logic analyzer's RS-232C default configuration with only one or two changes depending on which printer you have.

Since the logic analyzer's default RS-232C configuration is set for the HP ThinkJet printer, no changes are needed for the HP ThinkJet.

For RS-232C printers, the Printer connected to field must be set to RS-232C in the I/O Port Configuration menu. You access the I/O Port Configuration menu by first accessing the I/O menu, then the I/O Port Configuration.

The changes you need to make for the other HP printers are:

- Printer type for the HP LaserJet and HP QuietJet
- Paper width for the HP QuietJet

You access the printer type and page width fields by first accessing the I/O menu, then the I/O Port Configuration menu.

Setting RS-232C for Your Non-HP Printer

The following attributes of the RS-232C interface must be set to the correct configuration for your printer:

- protocol
- number of data bits
- number of stop bits
- parity type
- baud rate
- paper width

You access these fields by first accessing the I/O menu then the I/O Port Configuration menu.

Setting Paper Width

Paper width is set by toggling the Paper width : _____ field in the I/O Port Configuration menu. It tells the printer that you are sending up to 80 or 132 characters per line (only when you Print All) and is totally independent of the printer itself.

- If you select 132 characters per line (13.5 inches) when using other than an HP QuietJet selection, the listings are printed in a compressed mode. Compressed mode uses smaller characters to allow the printer to print more characters in a given width.
- If you select 132 characters per line (13.5 inches) on an HP QuietJet, it will print a full 132 characters per line.
- If you select 80 characters per line for any printer, a maximum of 80 characters are printed per line.

RS-232C Default Configuration

You can use the logic analyzer's default configuration (except for printer type and paper width) for all supported printers if you haven't changed the printer's RS-232C configuration.

The logic analyzer's default configuration is:

Protocol: XON/XOFF
Data Bits: 8
Stop Bits: 1
Parity: none
Baud rate: 9600
Printer: ThinkJet
Paper width: 8.5 inches

Recommended Protocol

The recommended protocol is XON/XOFF. This allows you to use the simpler three-wire hook-ups.

Starting the Printout

When you are ready to print, you need to know whether there is more data than is displayed on screen. In cases where data is off screen (i.e., format specifications with all pods assigned to a single analyzer), you need to decide whether you want just the data that is on screen or all the data.

If you want just what is on screen, start the printout with the Print Screen option. If you want all the data, use the Print All option. Both options are in the I/O menu. Once you decide which option to use, start the printout by placing the cursor on the print option (screen or all) and pressing SELECT.

I/O MENU

- Done
- Print Screen
- Print All
- Disk Operations
- I/O Port Configuration
- External BNC Configuration
- Self Tests

Figure 7-4. I/O Menu

Print Screen

The Print Screen option prints only what is displayed on screen at the time you initiate the printout. In the Print Screen mode, the printer uses its graphics capabilities and the printout will look just like the logic analyzer screen with only one exception: the cursor will not print.

Print All

The Print All option prints not only what is displayed on screen, but also what is below, and, in the Format Specification, what is to the right of the screen at the time you initiate the printout.

Note

Make sure the first line you wish to print is at the top of the screen when you select Print All. Lines above the screen will not print.

Use this option when you want to print all the data in menus like:

- Timing Format Specifications
- State Format Specifications
- State Trace Specifications
- State Listing
- Symbols
- Disk Directory

What Happens During a Printout?

When you press SELECT to start the printout, the I/O menu pop-up disappears and an advisory "PRINT in progress" appears in the top center of the display. While the data is transferred to the printer, the only useable key is the STOP key. When the logic analyzer has completed the data transfer to the printer, the advisory "PRINT complete" appears and the keyboard becomes useable again.

The PRINT in progress advisory won't appear in your printout. If you press STOP while the data is being transferred to the printer the transfer stops and the data already sent will print out. This causes an incomplete printout.

Connecting to Other HP Printers

The HP 1650B/51B can also be used with Hewlett-Packard printers that have RS-232C interface options. Simply connect the printer with the HP 13242G cable. Refer to table 7-1 for the appropriate selection for the RS-232C configuration of the HP 1650B/51B.

Table 7-1. HP Printer Selection

For this HP Printer	Select this Printer in I/O Port Configuration menu
HP 2631	QuietJet
HP 2671	ThinkJet
HP 2673	ThinkJet

The above printers should work with the HP 1650B/51B logic analyzers. However, no tests have been made to verify that they will work completely. Therefore, proper operation is neither promised nor supported by Hewlett-Packard.

8

The Timing Analyzer

Introduction

This chapter introduces the timing analyzer and contains the timing analyzer menu maps.

Chapters 9 through 11 explain each of the Timing Analyzer menus as follows:

- Chapter 9 explains the Timing Format Menu
- Chapter 10 explains the Timing Trace Menu
- Chapter 11 explains the Timing Waveforms Menu
- Chapter 12 gives you a basic Timing Analyzer Measurement example.

The Timing Analyzer (An Overview)

The timing analyzer acquires data asynchronously using an internal sample clock. This asynchronous data acquisition technique is similar to a digitizing oscilloscope. The acquired data is displayed in the form of one or more waveforms. The timing waveforms differ from a digitizing oscilloscope in that the timing analyzer only stores and displays two levels (one above and one below threshold).

Timing Analyzer Menu Maps

The Timing Analyzer menu maps show you the fields and the available options of each field within the three menus. The menu maps will help you get an overview of each menu as well as provide you with a quick reference of what each menu contains.

Timing Format Menu Map

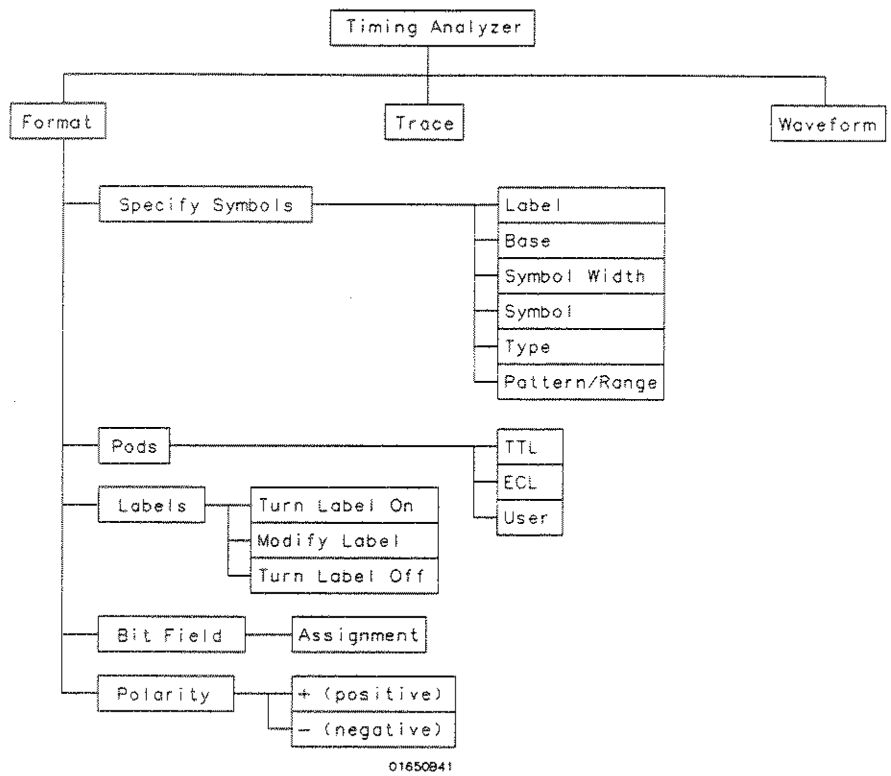


Figure 8-1. Timing Format Menu Map

Timing Trace Menu Map

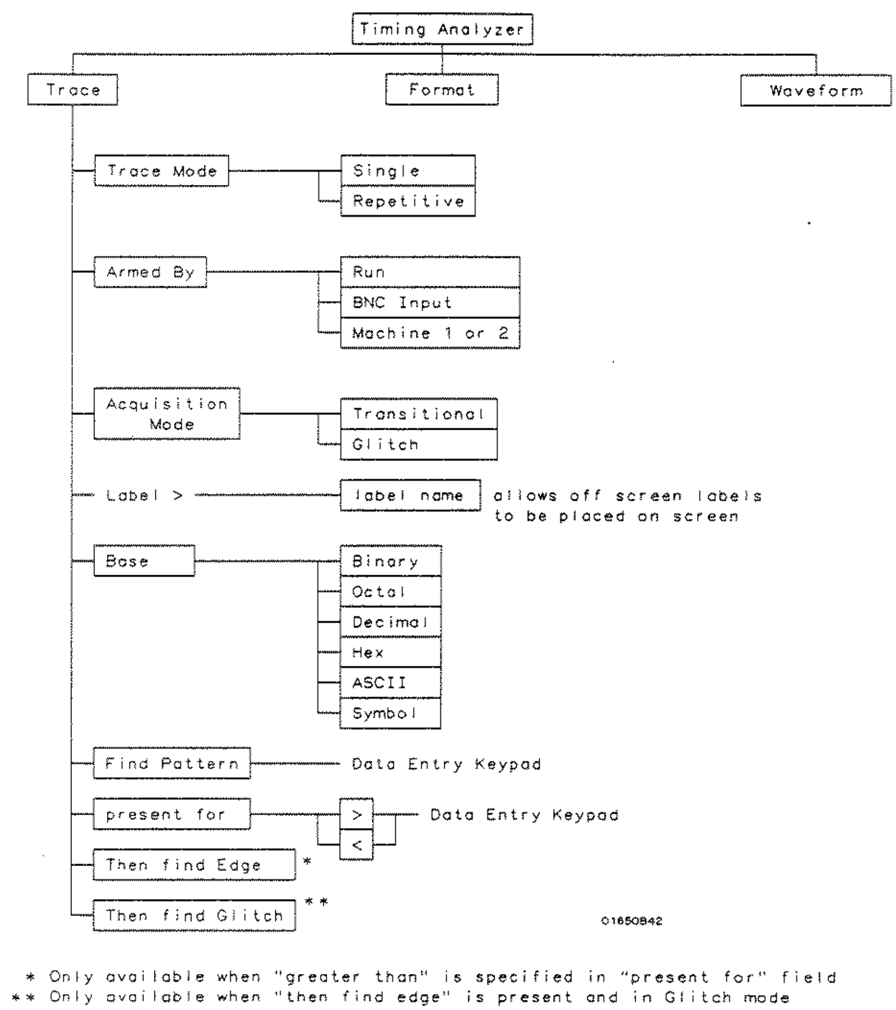


Figure 8-2. Timing Trace Menu Map

Timing Waveform Menu Map

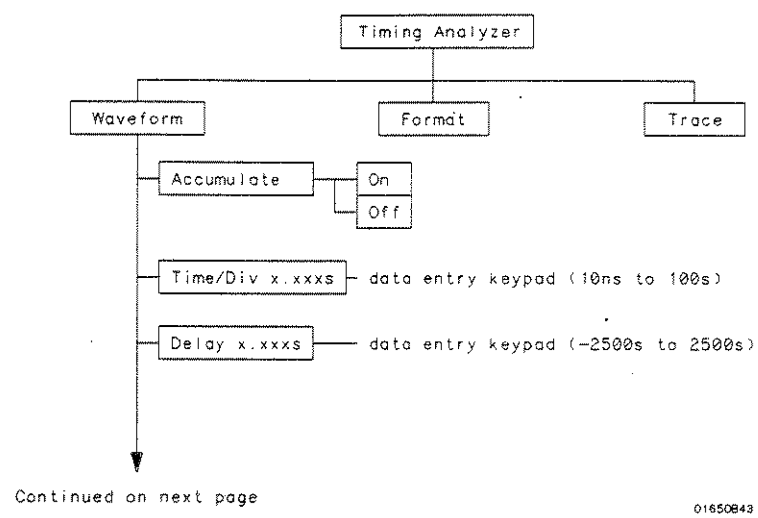


Figure 8-3. Timing Waveform Menu Map

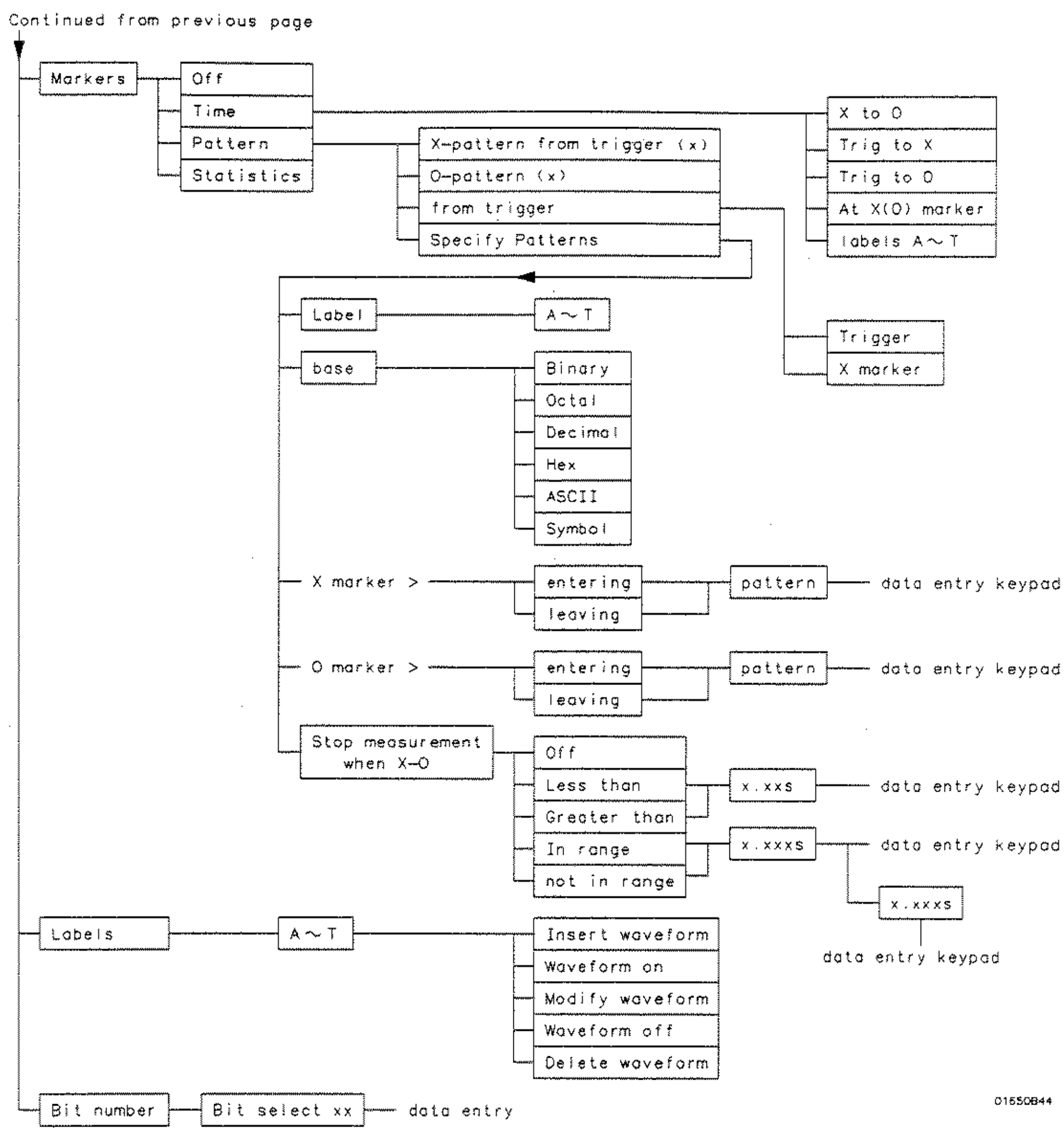


Figure 8-3. Timing Waveform Menu Map (Continued)

9

Timing Format Specification Menu

Introduction

This chapter describes the Timing Format Specification menu and all the pop-up menus that you will use on your timing analyzer. The purpose and function of each pop-up menu is explained in detail, and we have included many illustrations and examples to make the explanations clearer.

Accessing the Timing Format Menu

The Timing Format Specification menu can be accessed by pressing the FORMAT key on the front panel. If the State Format Specification Menu is displayed when you press the FORMAT key, you will have to switch analyzers. This is not a problem, it merely indicates that the last action you performed in the System Configuration Menu was on the state analyzer.

Timing Format Specification Menu

The Timing Format Specification menu lets you configure the timing analyzer to group channels from your microprocessor into labels you assign for your measurements. You can set the threshold levels of the pods assigned to the analyzer, assign labels and channels, and specify symbols.

At power up, the logic analyzer is configured with a default setting. You can use this default setting to make a test measurement on the system under test. It can give you an idea of where to start your measurement. For an example of setting up configurations for the Timing analyzer, refer to the *Getting Started Guide* or "Timing Analyzer Measurement Example" in chapter 12 of this manual.

At power up the Timing Format Specification menu looks like that shown below:

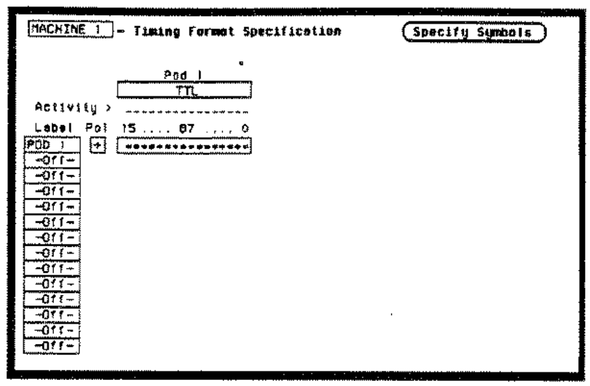


Figure 9-1. Timing Format Specification Menu

The Timing Format Specification menu for the HP 1651B is similar to that for the HP 1650B except that Pod 2 appears in the menu instead of Pod 5.

This menu shows only one pod assigned to each analyzer, which is the case at power up. Any number of pods can be assigned to one analyzer, from none to all five for the HP 1650B, and from none to two for the HP 1651B. In the Timing Format Specification menu, only three pods appear at a time in the display. To view any pods that are off screen, press the left/right ROLL key and rotate the KNOB. The pods are always positioned so that the lowest numbered pod is on the right and the highest numbered pod is on the left.

Timing Format Specification Menu Fields

Five types of fields are present in the menu. They are:

- Label
- Polarity (Pol)
- Bit assignments
- Pod threshold
- Specify Symbols

A portion of the menu that is not a field is the Activity Indicators display. The indicators appear under the active bits of each pod, next to "Activity." When the logic analyzer is connected to your target system and the system is running, you will see ↕ in the Activity Indicators display for each channel that has activity. These tell you that the signals on the channels are transitioning.

The fields in the Format menus are described in the following sections.

Label

The label column contains 20 Label fields that you can define. Of the 20 labels, the logic analyzer displays only 14 in the Timing Format Specification menu at one time. To view the labels that are off screen, press the up/down ROLL key and rotate the KNOB. The labels scroll up and down. To deactivate the scrolling, press the ROLL key again.

To access one of the Label fields, place the cursor on the field and press SELECT. You will see a pop-up menu like that shown below.

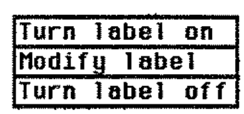


Figure 9-2. Label Pop-Up Menu

Turn Label On

Selecting this option turns the label on and gives it a default letter name. If you turned all the labels on they would be named A through T from top to bottom. When a label is turned on bit assignment fields for the label appear to the right of the label under the pods.

Modify Label

If you want to change the name of a label, or want to turn a label on and give it a specific name, you would select the Modify label option. When you do, an Alpha Entry pop-up menu appears. You can use the pop-up menu and the keypad on the front panel to name the label. A label name can be a maximum of six characters.

Turn Label Off

Selecting this option turns the label off. When a label is turned off, the bit assignments are saved by the logic analyzer. This gives you the option of turning the label back on and still having the bit assignments if you need them. The waveforms are also saved.

You can give the same name to a label in the state analyzer as in the timing analyzer without causing an error. The logic analyzer distinguishes between them. An example of this appears in "Using the Timing/State Analyzer" in chapter 7 of the *Getting Started Guide*.

Polarity (Pol)

Each label has a polarity assigned to it. The default for all the labels is positive (+) polarity. You can change the polarity of a label by placing the cursor on the polarity field and pressing SELECT. This toggles the polarity between positive (+) and negative (–).

In the timing analyzer, negative polarity inverts the data.

Bit Assignment

The bit assignment fields allow you to assign bits (channels) to labels. Above each column of bit assignment fields is a line that tells you the bit numbers from 0 to 15, with the left bit numbered 15 and the right bit numbered 0. This line helps you know exactly which bits you are assigning.

The convention for bit assignment is:

* (asterisk) indicates assigned bit
. (period) indicates unassigned bit

At power up the 16 bits of Pod 1 are assigned to the timing analyzer and the 16 bits of Pod 5 are assigned to the state analyzer. To change a bit assignment configuration, place the cursor on a bit assignment field and press SELECT. You will see the following pop-up menu.

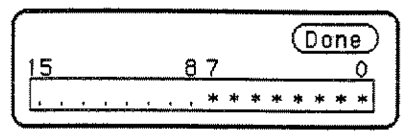


Figure 9-3. Bit Assignment Pop-Up Menu

Use the KNOB to move the cursor to an asterisk or a period and press SELECT. The bit assignment toggles to the opposite state of what it was before. When the bits (channels) are assigned as desired place the cursor on Done and press SELECT. This closes the pop-up and displays the new bit assignment.

Assigning one channel per label may be handy in some applications. This is illustrated in "Using the Timing/State Analyzer" in chapter 7 of the *Getting Started Guide* and chapter 12 of this manual. Also, you can assign a channel to more than one label, but this usually isn't desired.

Labels may have from 1 to 32 channels assigned to them. If you try to assign more than 32 channels to a label, the logic analyzer will beep, indicating an error, and a message will appear at the top of the screen telling you that 32 channels per label is the maximum.

Channels assigned to a label are numbered from right to left by the logic analyzer. The least significant assigned bit (LSB) on the far right is numbered 0, the next assigned bit is numbered 1, and so on. Since 32 channels can be assigned to one label at most, the highest number that can be given to a channel is 31. Although labels can contain split fields, assigned channels are always numbered consecutively within a label as shown in figure 9-4.

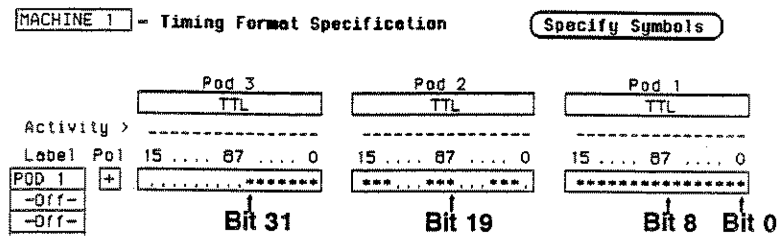


Figure 9-4. Numbering of Assigned Bits

Pod Threshold

Each pod has a threshold level assigned to it. For the HP 1651B Logic Analyzer, threshold levels may be defined for Pods 1 and 2 individually. For the HP 1650B Logic Analyzer, threshold levels may be defined for Pods 1, 2 and 3 individually, and one threshold for Pods 4 and 5. It does not matter if Pods 4 and 5 are assigned to different analyzers. Changing the threshold of one will change the threshold of the other.

If you place the cursor on one of the pod threshold fields and press SELECT, you will see the following pop-up menu.

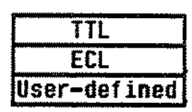


Figure 9-5. Pod Threshold Pop-Up Menu

TTL sets the threshold at + 1.6 volts, and ECL sets the threshold at − 1.3 volts.

The User-defined option lets you set the threshold to a specific voltage between − 9.9 V and + 9.9 V. If you select this option you will see a Numeric Entry pop-up menu as shown.

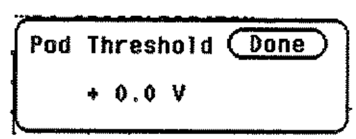


Figure 9-6. User-Defined Numeric Entry Pop-Up Menu

You can change the value in the pop-up either with the keypad on the front panel or with the KNOB, which you rotate until you get the desired voltage. When the correct voltage is displayed, press SELECT. The pop-up will close and your new threshold will be placed in the pod threshold field.

Specify Symbols Menu

The Specify Symbols field differs from the other fields in the Timing Format Specification menu in that it displays a complete menu instead of a pop-up.

The logic analyzer supplies Timing and State Symbol Tables in which you can define a mnemonic for a specific bit pattern of a label. When measurements are made by the timing analyzer, the mnemonic is displayed where the bit pattern occurs if the Symbol base is selected.

It is possible for you to specify up to 200 symbols in the logic analyzer. If you have only one of the internal analyzers on, all 200 symbols can be defined in it. If both analyzers are on, the 200 symbols are split between the two. For example, analyzer 1 may have 150, leaving 50 available for analyzer 2.

To access the Symbol Table in the Timing Format Specification menu, place the cursor on the Specify Symbols field and press SELECT. You will see a new menu as shown in figure 9-7. This is the default setting for the Symbol Table in both the timing and state analyzers.

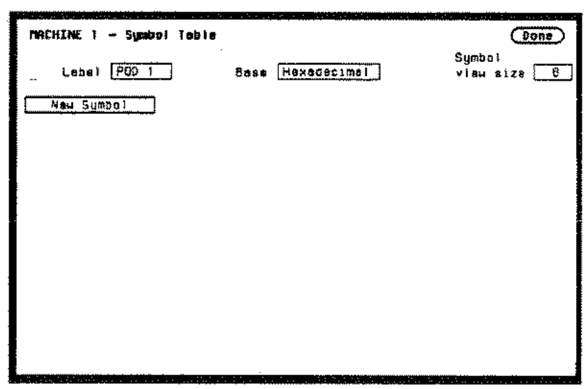


Figure 9-7. Symbol Table Menu

Specify Symbols Menu Fields

There are four fields in the Symbol Table menu. They are:

- Label
- Base
- Symbol view size
- Symbol name

Label

The Label field identifies the label for which you are specifying symbols. If you select this field, you will get a pop-up that lists all the labels turned on for that analyzer.

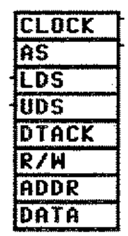


Figure 9-8. Label Pop-Up Menu

Each label has a separate symbol table. This allows you to give the same name to symbols defined under different labels. In the Label pop-up select the label for which you wish to specify symbols.

Base

The Base field tells you the numeric base in which the pattern will be specified. The base you choose here will affect the Find Pattern field of the Timing Trace Specification menu. This is covered later in this chapter.

To change the base, place the cursor on the Base field and press SELECT. You will see the following pop-up menu.

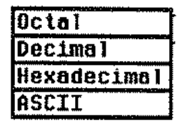


Figure 9-9. Base Pop-Up Menu

If more than 20 channels are assigned to a label, the Binary option is not offered in the pop-up. The reason for this is that when a symbol is specified as a range, there is only enough room for 20 bits to be displayed on the screen.

Decide which base you want to work in and choose that option from the numeric Base pop-up menu.

If you choose the ASCII option, you can see what ASCII characters the patterns and ranges defined by your symbols represent. ASCII characters represented by the decimal numbers 0 to 127 (hex 00 to 7F) are offered on your logic analyzer. Specifying patterns and ranges for symbols is discussed in the next section.

Note

You cannot specify a pattern or range when the base is ASCII. First define the pattern or range in one of the other bases, then switch to ASCII to see the ASCII characters.

Symbol View Size

The Symbol view size field lets you specify how many characters of the symbol name will be displayed when the symbol is referenced in the Timing Trace Specification menu and the Timing Waveforms menu. Selecting this field gives you the following pop-up.

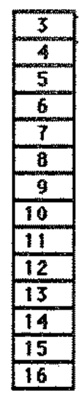


Figure 9-10. Symbol View Size Pop-Up Menu

You can have the logic analyzer display from 3 to all 16 of the characters in the symbol name. For more information see "Timing Trace Specification Menu" in Chapter 10 and the "Timing Waveforms Menu" in Chapter 11.

Symbol Name

When you first access the Symbol Table, there are no symbols specified. The symbol name field reads "New Symbol." If you select this field, you will see an Alpha Entry pop-up menu on the display. Use the pop-up menu and the keypad on the front panel to enter the name of your symbol. A maximum of 16 characters can be used in a symbol name. When you select the Done field in the Alpha Entry pop-up menu the name that appears in the symbol name field is assigned and two more fields appear in the display.

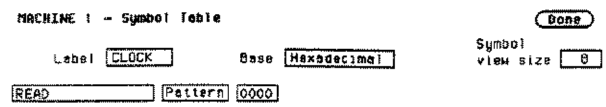


Figure 9-11. Symbol Defined as a Pattern

The first of these fields defines the symbol as either a **Pattern** or a **Range**. If you place the cursor on this field and press SELECT, it will toggle between **Pattern** and **Range**.

When the symbol is defined as a pattern, one field appears to specify what the pattern is. Selecting this field gives you a pop-up with which you can specify the pattern. Use the keypad and the DON'T CARE key on the front panel to enter the pattern. Be sure to enter the pattern in the numeric base that you specified in the **Base** field.

Figure 9-12. Specify Pattern Pop-Up

If the symbol is defined as a range, two fields appear in which you specify the upper and lower boundaries of the range.

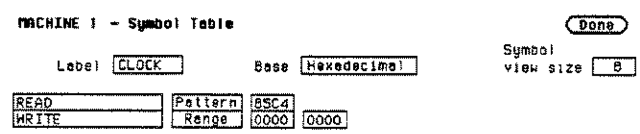


Figure 9-13. Symbol Defined as a Range

Selecting either of these fields gives you a pop-up with which you can specify the boundary of the range.

Figure 9-14. Specify Range Pop-Up

You can specify ranges that overlap or are nested within each other. Don't cares are not allowed.

To add more symbols to your symbol table, place the cursor on the last symbol defined and press SELECT. A pop-up menu appears as shown.

Modify symbol
Insert new symbol
Delete symbol

Figure 9-15. Symbol Pop-Up Menu

The first option in the pop-up is Modify symbol. If you select this option, you will see an Alpha Entry pop-up menu with which you can change the name of the symbol.

The second option in the pop-up is Insert new symbol. It allows you to specify another symbol. When you select it, you will see an Alpha Entry pop-up menu. Use the menu and the keypad on the front panel to enter the name of your new symbol. When you select Done, your new symbol will appear in the Symbol Table. The third option in the pop-up is Delete symbol. If you select this option, the symbol will be deleted from the Symbol Table.

Leaving the Symbol Table Menu

When you have specified all your symbols, you can leave the Symbol Table menu in one of two ways. One method is to place the cursor on the Done field and press SELECT. This puts you back in the Format Specification menu that you were in before entering the Symbol Table. The other method is to press the FORMAT, TRACE, or DISPLAY keys on the front panel to get you into the respective menu.

10

Timing Trace Specification Menu

Introduction

This chapter describes Timing Trace Specification menu and all the pop-up menus that you will use on your timing analyzer. The purpose and function of each pop-up menu is explained in detail, and we have included many illustrations and examples to make the explanations clearer.

Accessing the Timing Trace Specification Menu

The Timing Trace Specification menu can be accessed by pressing the TRACE key on the front panel. If the State Trace Specification menu is displayed when you press the TRACE key, you will have to switch analyzers. This is not a problem, it merely indicates that the last action you performed in the System Configuration Menus was on the state analyzer.

Timing Trace Specification Menu

The Trace Specification menus allow you to configure the logic analyzer to capture only the data of interest in your measurement. In the timing analyzer you can configure the analyzer to trigger on specific patterns, edges, or glitches. The Timing Trace Specification menu lets you specify the trigger point for the logic analyzer to start capturing data and the manner in which the analyzer will capture data. You configure the timing analyzer to find a pattern first and then a transition in the signal or signals.

At power up, the logic analyzer is configured with a default setting. You can use this default setting to make a test measurement on the system under test. It can give you an idea of where to start your measurement. For an example on setting up configurations for the Timing analyzer, refer to the *Getting Started Guide* or "Timing Analyzer Measurement Example" in Chapter 12 of this manual.

At power up the Timing Trace menu looks like that shown below.

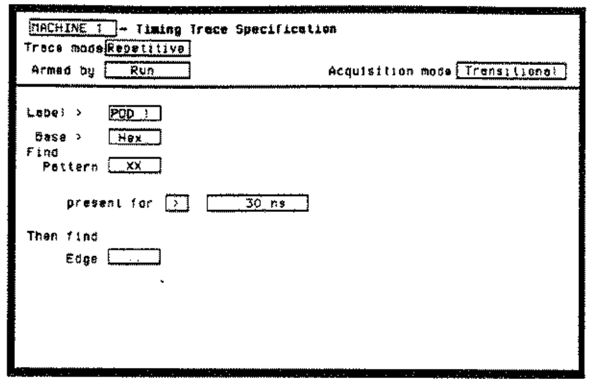


Figure 10-1. Timing Trace Specification Menu

The menu is divided into two sections by a horizontal line. The top section contains the fields that you use to specify the data acquisition. The bottom section contains the fields for setting the trigger point.

Timing Trace Specification Menu Fields

The fields in the Timing Trace Specification menu are:

- Trace mode
- Armed by
- Acquisition mode
- Label
- Base
- Find Pattern
- Pattern Duration (present for ____)
- Then find Edge

These are described in the following sections.

Trace Mode

With the Trace Mode field you specify the mode in which the timing analyzer will trace. You have two choices for Trace mode: Single and Repetitive. If you place the cursor on the field and press SELECT, the field toggles from one mode to the other.

Single Trace mode acquires data once per trace. Repetitive Trace mode repeats single acquisitions until the STOP key on the front panel is pressed, or if Stop measurement has been selected and the stop measurement condition has been met.

If both analyzers are on, only one trace mode can be specified. Specifying one trace mode for one analyzer sets the same trace mode for the other analyzer.

Armed By

The Armed by field lets you specify how your timing analyzer is to be armed. The analyzer can be armed by the RUN key, the other analyzer, or an external instrument through the BNC Input port.

When you select the Armed by field, a pop-up menu appears like that shown below. Use this menu to select the arming option for your analyzer.

Figure10-2. Armed By Pop-Up Menu

Acquisition Mode

The Acquisition mode field allows you to specify the mode in which you want the timing analyzer to acquire data. You are given two choices for the mode of acquisition: Transitional and Glitch . If you place the cursor on this field and press SELECT, the field toggles from one mode to the other.

Transitional Acquisition Mode

When the logic analyzer is operating in the Transitional Acquisition mode, it samples the data at regular intervals, but it stores data in memory only on transitions in the signals. A time tag that is stored with each sample allows reconstruction of the samples in the Timing Waveforms display.

Transitional timing always samples at a rate of 100 MHz (10 ns/sample). This provides maximum timing resolution even in records that span long time windows. Time covered by a full memory acquisition varies with the number of pattern changes in the data. If there are many transitions, the data may end prior to the time window desired because the memory is full. However, a prestore qualification in your logic analyzer insures that data will be captured and displayed between the left side of the screen and the trigger point.

Figure 10-3 illustrates Transitional acquisition, comparing it to Traditional acquisition.

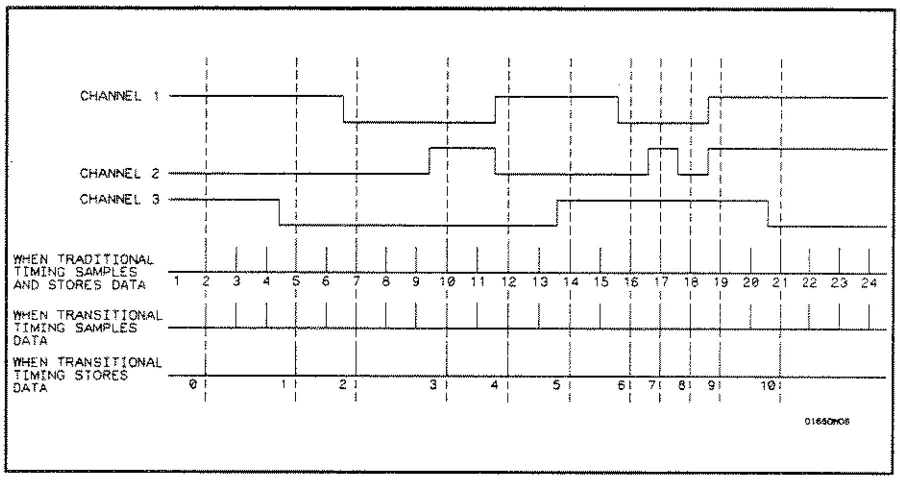


Figure 10-3. Transitional vs. Traditional Acquisition

Traditional timing samples and stores data at regular intervals. Transitional timing samples data at regular intervals but stores a sample only when there has been a transition on one or more of the channels. This makes it possible for Transitional timing to store more information in the same amount of memory.

Glitch Acquisition Mode

A glitch is defined as any transition that crosses logic threshold more than once between samples. It can be caused by capacitive coupling between traces, by power supply ripples, or a number of other events. Since a glitch can cause major problems in your system, you can use the Glitch mode to find it.

Your logic analyzer has the capability of triggering on a glitch and capturing all the data that occurred before it. The glitch must have a width of at least 5 ns at threshold in order for the analyzer to detect it.

If you want your timing analyzer to trigger on a glitch in the data set the Acquisition mode to Glitch. This causes several changes in the analyzer. One change is that a field for glitch detection in each label is added to the Timing Trace Specification menu, as shown:

```
Then find
     Edge  [....]
      or
    Glitch [....]
```

Figure 10-4. Glitch Specification Field

With these glitch detection fields you specify on which channel or channels you want the analyzer to look for a glitch. These fields are discussed in more detail in "Then Find Edge" later in this chapter.

Glitch Acquisition mode causes the storage memory to be cut in half from 1k to 512. Half the memory (512) is allocated for storing the data sample, and the other half for storing the second transition of a glitch in a sample. Every sample is stored.

The sample rate varies from 20 Hz to 50 MHz (50 ms/sample to 20 ns/sample) and is automatically selected by the timing analyzer to insure complete data in the window of interest.

When your timing analyzer triggers on a glitch and displays the data, the glitch appears in the waveform display as shown below.

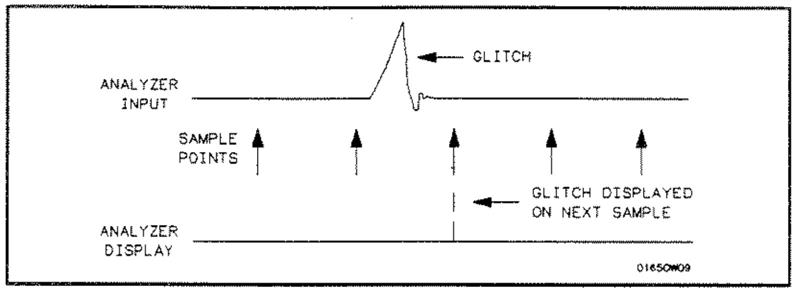


Figure 10-5. Glitch in Timing Waveform

Label The Label fields contain the labels that you define in the Timing Format Specification menu. If there are more labels than can fit on screen, use the left/right ROLL key and the KNOB to view those that are not displayed.

Base The Base fields allow you to specify the numeric base in which you want to define a pattern for a label. The Base fields also let you use a symbol that was specified in the Timing Symbol Table for the pattern. Each label has its own base defined separately from the other labels. If you select one of the Base fields, you will see the following pop-up menu. Decide which base you want to define your pattern in and select that option.

Binary
Octal
Decimal
Hexadecimal
ASCII
Symbol

Figure 10-6. Base Pop-up Menu

One of the options in the Base pop-up is ASCII . It allows you to see characters that are represented by the pattern you specified in the Find Pattern field.

```
Label >    [ POD 1 ]
 Base >    [ ASCII ]
Find
  Pattern   $   %
```

Figure 10-7. ASCII Defined as Numeric Base

Notice in the figure above that the Find Pattern field is no longer a selectable field when the base is ASCII . You cannot specify ASCII characters directly. You must specify a pattern in one of the other bases; then you can switch the base to ASCII and see what characters the pattern represents.

The Symbol option in the Base pop-up allows you to use a symbol that has been specified in the Timing Symbol Tables as a pattern or specify absolute and enter another pattern. You specify the symbol you want to use in the Find Pattern field.

Find Pattern

With the Find Pattern fields, you configure your timing analyzer to look for a certain pattern in the data. Each label has its own pattern field that you use to specify a pattern for that label.

During a run, the logic analyzer looks for a pattern in your data which is the logical AND of all the labels' patterns. That is, it looks for a simultaneous occurrence of the specified patterns. When it finds the pattern, it triggers at the point that you specified in the Then find Edge fields. See "Then Find Edge" later in this chapter for more information about edge triggering.

You select a Find Pattern field with one of two methods. The first method is to place the cursor on the Find Pattern field and press SELECT. The second method is to place the cursor on the Find Pattern field and press one of the alphanumeric keys on the front-panel keypad. Both methods give you a pop-up similar to that shown in figure 10-8.

```
Specify Pattern:
2425
```

Figure 10-8. Specify Pattern Pop-Up for Find Pattern

The pop-up will vary depending on the base you choose and the number of channels you assign to that label. If you press a key on the keypad to open the pop-up, the character on the key is placed in the first location of the pattern.

Enter your pattern in the pop-up and press SELECT. The pattern appears under the label in the Find Pattern field.

As mentioned previously in "Base", if you specify ASCII as the base for the label, you won't be able to enter a pattern. You must specify one of the other numeric bases to enter the pattern. Then you can switch the base to ASCII and see what ASCII characters the pattern represents. If you choose Symbols in the Base field, you can use one of the symbols specified in the Timing Symbol Tables as the pattern. The Find Pattern field looks similar to that below:

```
Label >    [    POD 1     ]
 Base >    [    Symbol    ]
Find
  Pattern  [absolute 2425 ]
```

Figure 10-9. Symbol Defined in Base Field

If you select this field you get a pop-up similar to that shown:

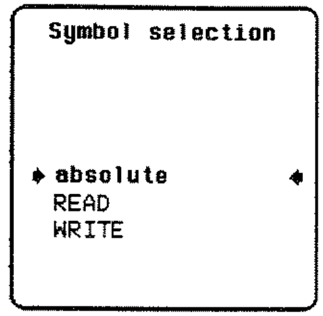


Figure 10-10. Symbol Selection Pop-Up for Find Pattern

The pop-up lists all the symbols defined for that label. It also contains an option "absolute xxxx." Choosing this option gives you another pop-up with which you specify a pattern not given by one of your symbols.

To select an option from the pop-up, use the KNOB to scroll the symbols up and down until the desired symbol is between the two arrows. Press SELECT. The symbol name appears in the Find Pattern field under the label.

When you specify symbols in the Timing Symbol Tables, you also specify the number of characters in the symbol name that are to be displayed. If you specify only three characters of a symbol name in the Symbol menu, only REA of READ and WRI of WRITE would be displayed in the Find Pattern Field. In addition, only the first three letters of "absolute" would be displayed.

Pattern Duration (present for ___)

There are two fields with which you specify the Pattern Duration. They are located next to present for ______ in the Timing Trace Specification menu. You use these fields to tell the timing analyzer to trigger before or after the specified pattern has occurred for a given length of time.

The first field can be set to " > " (greater than) or " < " (less than). If you place the cursor on this field and press SELECT, it toggles between > and < . The second field specifies the duration of the pattern. If you select > in the first field, you can set the duration to a value between 30 ns and 10 ms. If you select < in the first field, you can set the duration to a value between 40 ns and 10 ms. If you attempt to set the duration to a value outside the given range, the analyzer will automatically set it to the nearest limit.

To change the value of the pattern duration, place the cursor on the second field and either press SELECT to get a pop-up menu, or just press one of the numeric keys on the front-panel keypad. Both methods give you a Numeric Entry pop-up similar to that shown.

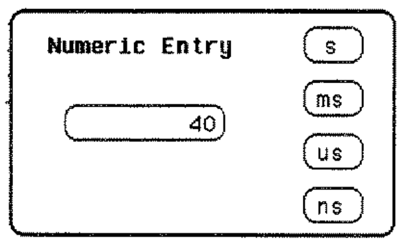


Figure 10-11. Pattern Duration (present for) Pop-Up

With the front-panel keypad enter the desired pattern duration. Use the KNOB to place the cursor on the correct timing units, then press SELECT. Your value for Pattern Duration will appear in the field.

Note

If you press a key on the keypad to open the pop-up, the number that you pressed will appear in the entry field replacing the previous value. To restore the original value press the CLEAR ENTRY key.

As an example, suppose you configure the present for ____ field as shown:

```
present for [>] [   50 ns   ]
```

Figure 10-12. Example of Pattern Duration (Greater Than)

This configuration tells the timing analyzer to look for the pattern you specified that occurs for a period of time greater than 50 ns. Once the timing analyzer has found the pattern, it can look for the trigger.

Choosing < (less than) forces glitch and edge triggering off, and the timing analyzer triggers immediately at the end of the pattern that meets the duration requirements. The fields with which you specify edges and glitches don't appear in the menu. For instance, if you configure the present for ____ field as shown:

```
present for [<] [   100 ns   ]
```

Figure 10-13. Example of Pattern Duration (Less Than)

The analyzer will trigger when it sees the pattern you specified that occurs for a period less than 100 ns. The pattern must also be valid for at least 20 ns.

Then Find Edge

With the Then find Edge fields you can specify the edges (transitions) of the data on which your timing analyzer triggers. You can specify a positive edge, a negative edge, or either edge. Each label has its own edge trigger specification field so that you can specify an edge on any channel.

When you specify an edge on more than one channel, the timing analyzer logically ORs them together to look for the trigger point. That is, it triggers when it sees any one of the edges you specified. It also ANDs the edges with the pattern you specified in the Find Pattern fields. The logic analyzer triggers on an edge following the valid duration of the pattern while the pattern is still present. To specify an edge, place the cursor on one of the Then find Edge fields and press SELECT. You will see a pop-up similar to that shown in the following figure.

```
Specify Edge:      (Done)
.... .... .... ....
```

Figure 10-14. Specify Edge Pop-Up for Then Find Edge

Your pop-up may look different than this depending on the number of channels you assigned to the label. Each period in the pop-up indicates that no edge is specified for that channel.

To specify a negative edge, place the cursor on one of the periods in the pop-up and press SELECT once. The period changes to ↓, as shown:

```
Specify Edge:      (Done)
↓... .... .... ....
```

Figure 10-15. Negative Edge Specified

To specify a positive edge, place the cursor on one of the periods and press SELECT twice. The period changes to ↑, as shown:

```
Specify Edge:      (Done)
↓.↑. .... .... ....
```

Figure 10-16. Positive Edge Specified

If you want the analyzer to trigger on either a positive or a negative edge, place the cursor on a period and press SELECT three times. The period changes to↕ , as shown:

```
Specify Edge:      (Done)
↓.↑. ↕... .... ....
```

Figure 10-17. Either Edge Specified

If you want to delete an edge specification, place the cursor on the arrow for that channel and press SELECT until you see a period. To clear an entire label, press the CLEAR ENTRY key on the front panel.

When you have finished specifying edges, place the cursor on the Done field and press SELECT to close the pop-up.

Note

If you are not in Binary base, you will see dollar signs ($$..) in the Then find Edge field when you close the pop-up. These indicate that edges have been specified; however, the logic analyzer can't display them correctly unless you have selected Binary for the base.

Glitch Triggering. When you set the Acquisition mode on Glitch a glitch detection field for each label is added to the screen. These fields allow you to specify glitch triggering on your timing analyzer. Selecting one of these fields brings up the following pop-up menu.

Figure 10-18. Specify Glitch Pop-Up for Then Find Glitch

Your pop-up may look different depending on the number of channels you have assigned to the label. Each period indicates that the channel has not been specified for glitch triggering.

To specify a channel for glitch triggering, place the cursor on one of the periods and press SELECT. The period is replaced with an asterisk, indicating that the logic analyzer will trigger on a glitch on this channel.

Figure 10-19. Glitches Specified

If you want to delete a glitch specification, place the cursor on the asterisk and press SELECT. The asterisk is replaced with a period.

Note If you are not in Binary base, you will see dollar signs ($$..) in the Glitch field when you close the pop-up. This indicates that glitches have been specified; however, the logic analyzer can't display them correctly unless you have selected Binary for the base.

When more than one glitch has been specified, the logic analyzer logically ORs them together. In addition, the logic analyzer ORs the glitch specifications with the edge specifications, then ANDs the result with the pattern you specified in the Find Pattern fields in order to find the trigger point. A boolean expression illustrating this is:

(glitch + glitch + edge + edge) * pattern

Note If you select < (less than) in the present for____field, edge and glitch triggering are turned off. The Then find Edge or Glitch field no longer appears on the screen. The logic analyzer then triggers only on the pattern specified in the Find Pattern fields.

11

Timing Waveforms Menu

Introduction

The Timing Waveforms menu is the display menu of the timing analyzer. This chapter describes the Timing Waveforms menu and how to interpret it. It also tells you how to use the fields to manipulate the displayed data so you can find your measurement answers.

There are two different areas of the timing waveforms display: the menu area and the waveforms area. The menu area is in the top one-fourth of the screen and the waveforms area is the bottom three-fourths of the screen.

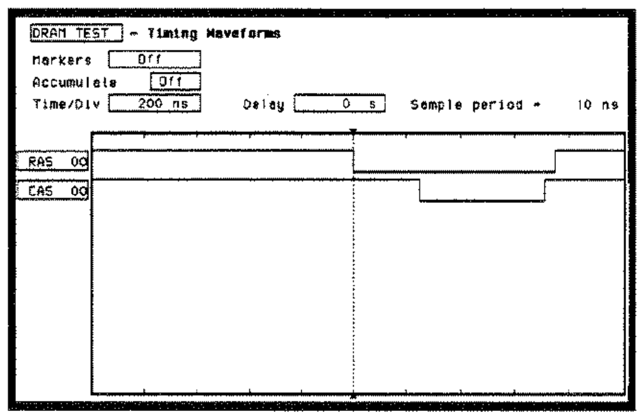


Figure 11-1. Timing Waveforms Menu

The waveforms area displays the data that the timing analyzer acquires. The data is displayed in a format similar to an oscilloscope with the horizontal axis representing time and the vertical axis representing amplitude. The basic differences between an oscilloscope display and the timing waveforms display are: in the timing waveforms display the vertical axis only displays highs (above threshold) and lows (below threshold). Also, the waveform lows are represented by a thicker line for easy differentiation.

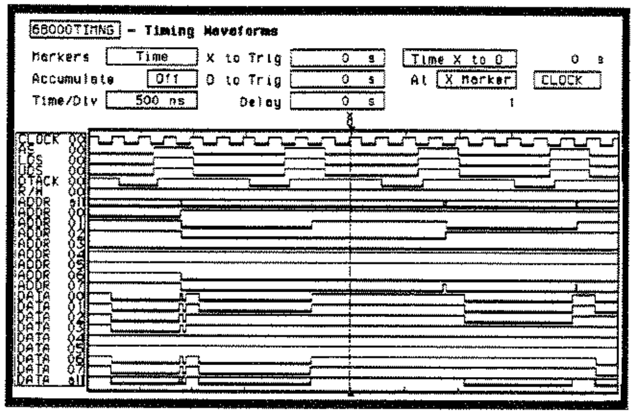


Figure 11-2. Timing Waveforms Menu with 24 Waveforms

Accessing the Timing Waveforms Menu

The Timing Waveforms Menu is accessed by the pressing the DISPLAY key on the front panel when the timing analyzer is on. It will automatically be displayed when you press RUN.

Timing Waveforms Menu Fields

The menu area contains fields that allow you to change the display parameters, place markers, and display waveform measurement parameters.

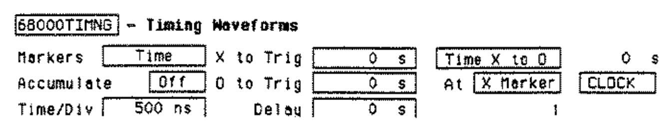


Figure 11-3. Timing Waveforms Menu Fields

Markers

The Markers field allows you to specify how the X and O markers will be positioned on the timing data. The options are:

- Off
- Time
- Patterns
- Statistics
- Markers Off/Sample Period

When the markers are off they are not visible and the sample period is displayed. In transitional timing mode, the sample period will always be 10 ns. In Glitch, the sample period is controlled by the Time/Div setting and can be monitored by turning the markers off.

Note

The sample period displayed is the sample period of the last acquisition. If you change the Time/Div setting, you must press RUN to initiate another acquisition before the sample period is updated.

Although the markers are off, the logic analyzer still performs statistics, so if you have specified a stop measurement condition the measurement will stop if the pattern specified for the markers is found.

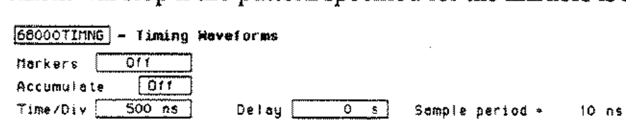


Figure 11-4. Markers Off

Markers Time

When the markers are set to Time, you can place the markers on the waveforms at events of interest and the logic analyzer will tell you:

- Time X to Trig(ger)
- Time O to Trig(ger)
- Time X to O

To position the markers, move the cursor to the field of the marker you wish to position and press SELECT. A pop-up will appear showing the current time for that marker. Either rotate the KNOB or enter a numeric value from the keypad to change the position of that marker. Pressing SELECT when you are finished positions the marker and closes the pop-up.

When the cursor is on either the X to Trig or O to Trig fields, you can also enter a value directly from the keypad without pressing SELECT.

Figure 11-5. Markers Time

The Time X to O field will change according to the position of the X and O markers. If you place the cursor on the Time X to O field and press SELECT, another pop-up will appear showing you all three times: X to Trigger, O to Trigger, and Time X to O.

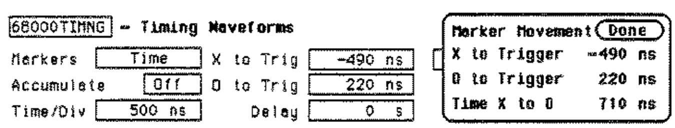


Figure 11-6. Time X to O Pop-up

If you rotate the KNOB while this pop-up is open, both X and O markers will move, but the relative placement between them will not change.

Markers Patterns

When the markers are set to patterns, you can specify the patterns on which the logic analyzer will place the markers. You can also specify how many occurrences of each marker pattern the logic analyzer looks for. This use of the markers allows you to find time between specific patterns in the acquired data.

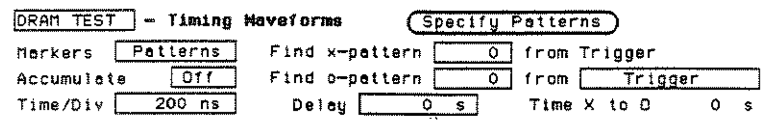


Figure 11-7. Markers Patterns

Patterns for each marker (X and O) can be specified. Patterns can be specified for both markers in each label. The logic analyzer searches for the logical "and" of patterns for all labels even though only one label can be displayed at a time. You can also specify whether the marker is placed on the pattern at the beginning of its occurrence (entering) or at the end of its occurrence (leaving) as shown in figure 11-8.

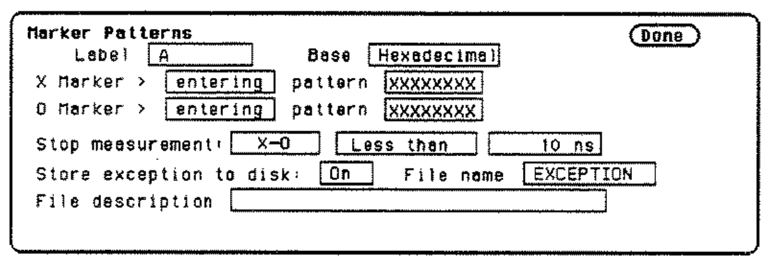


Figure 11-8. Marker Patterns Pop-up menu

Stop Measurement. Another feature of markers set to patterns is the Stop measurement when **Time X-O** ____. The options are: Less than, Greater than, In range, Not in range

With this feature you can use the logic analyzer to look for a specified time or range of time between the marked patterns and have it stop acquiring data when it sees this time between markers. (The X marker must precede the O marker.)

Also available is **Store exception to disk** which allows you to specify a file on the disk that exceptions can be stored in. The default filename is EXCEPTION.

Note

The upper and lower range boundaries must not be the same value. For example, if you want to stop a measurement when the X and O markers are in range of 200 ns, you should set the range values to 190 ns and 210 ns. This eliminates erroneous measurement termination.

Markers Statistics

When statistics are specified for markers, the logic analyzer will display the:

- Number of total runs
- Number of valid runs (runs where markers were able to be placed on specified patterns)
- Minimum time between the X and O markers
- Maximum time between the X and O markers
- Average time between the X and O markers

Statistics are based on the time between markers which are placed on specific patterns. If a marker pattern is not specified, the marker will be placed on the trigger point by the logic analyzer. In this case the statistical measurement will be the time from the trigger to the specified marker. How the statistics will be updated depends on the timing trace mode (repetitive or single).

In repetitive, statistics will be updated each time a valid run occurs until you press STOP. When you press RUN after STOP, the statistics will be cleared and will restart from zero.

In single, each time you press RUN an additional valid run will be added to the data and the statistics will be updated. This will continue unless you change the placement of the X and O markers between runs.

Accumulate Mode

Accumulate mode is selected by toggling the Accumulate ON/OFF field in the Timing Waveforms menu. When accumulate is on, the timing analyzer displays the data from a current acquisition on top of the previously acquired data.

When the old data is cleared depends on whether the trace mode is in single or repetitive. In single, new data will be displayed on top of the old each time RUN is selected as long as you stay in the Timing Waveforms menu between runs. Leaving the Timing Waveforms menu always clears the accumulated data. In repetitive mode, data is cleared from the screen only when you start a run after stopping acquisition with the STOP key.

AT ____ Marker ____

The At X (or O) Marker _______ fields allow you to select either the X or O markers. You can place these markers on the waveforms of any label and have the logic analyzer tell you what the pattern is. For example, in the timing waveforms display (figure 6-8) the number 35 to the right of the Delay ______ field is the pattern in hexadecimal that is marked by the O marker. The base of the displayed field is determined by the base of the specified label you selected in the Timing Trace menu.

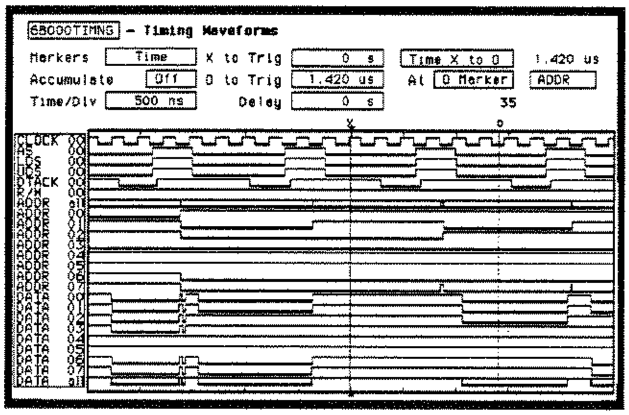


Figure 11-9. At O Marker ADDR fields

This display tells you that 35H is the pattern on the address label lines where the O marker is located.

You can toggle the At _______ Marker field between the X and O markers.

The next field to the right of the At _____ Marker field will pop up when selected and show you all the labels assigned to the timing analyzer as shown below.

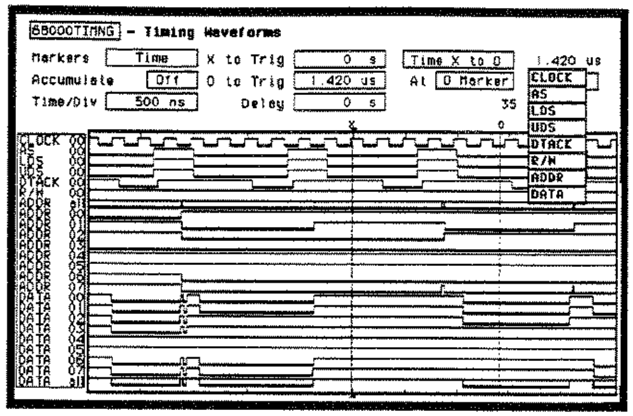


Figure 11-10. Label Option Pop-up

Time/Div (time per division) Field

The time per division field allows you to change the width of the time window of the Timing Waveforms menu.

When the pop-up is open you can change the time per division by rotating the KNOB or entering a numeric value from the keypad. When you rotate the KNOB, the time per division increments or decrements in 1-2-5 sequence from 10 ns/div to 50 ms/div.

Note Sample period is fixed at 10 ns in the Transitional acquisition mode.

When you enter a value from the keypad, the time per division does not have to be a 1-2-5 sequence.

Note In Glitch mode, changing the Time/Div setting changes the sample period for the next run. To view the sample period after the next run, turn the markers off if they are on and press RUN.

Delay Field

The Delay field allows you to enter a delay. The delay can be either positive or negative. Delay allows you to place the time window (selected by Time/Div) of the acquired data at center screen.

The inverted triangle in the horizontal center of the waveforms area of the display represents trigger + delay. The vertical dotted line represents the trigger point (see figure 6-10).

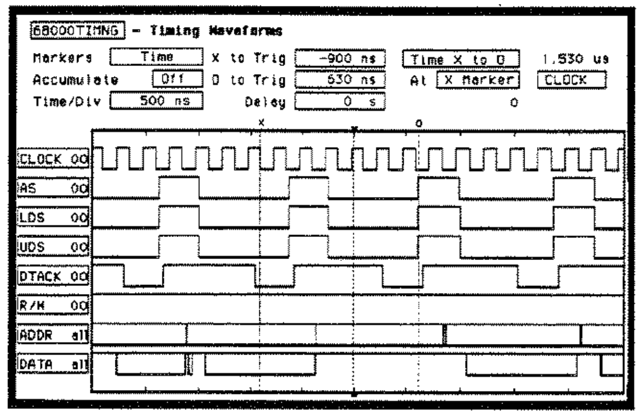


Figure 11-11. Trigger and Trace Points

If you want to trace after the trigger point, enter a positive delay. If you want to trace before the trigger point (similar to negative time) enter a negative delay. The logic analyzer is capable of maximum delays of − 2500 seconds to + 2500 seconds. In Transitional mode the maximum delay is determined by the number of transitions of the incoming data. Data may not be displayed at all settings of Time/Div and Delay.

In Glitch mode the maximum delay is 25 seconds, which is controlled by memory and sample period (512 x 50ms). The sample rate is also dependent on the delay setting. It is represented by the following formula:

if delay $<$ 20 ns
  Hwdelay = 20 ns (this is an instrument constant)

if delay $>$ 10 ms
  Hwdelay = 10 ms

else Hwdelay = delay (delay setting in timing waveforms menu)

Sample period = larger of:

  Time/Div $\div$ 25 or

  absolute value [(delay $-$ Hwdelay) $\div$ 256]

If sample period $>$ 50 ms

Then sample period = 50 ms

12

Timing Analyzer Measurement Example

Introduction

In this chapter you will learn how to use the timing analyzer by setting up the logic analyzer to make a simple measurement. We give you the measurement results as actually measured by the logic analyzer, since you may not have the same circuit available.

The exercise in this chapter is organized in a task format. The tasks are ordered in the same way you will most likely use them once you become an experienced user. The steps in this format are both numbered and lettered. The numbered steps state the step objective. The lettered steps explain how to accomplish each step objective. There is also an example of each menu after it has been properly set up.

How you use the steps depends on how much you remember from chapters 1 through 4 of the *Getting Started Guide*. If you can set up each menu by just looking at the menu picture, go ahead and do so. If you need a reminder of what steps you need to perform, follow the numbered steps. If you still need more information about "how," use the lettered steps.

When you have finished configuring the logic analyzer for this exercise, you can load a file from the operating system disc. This file configures the logic analyzer the same way it is configured for this exercise. It also loads the same data acquired for this exercise so you can see what it looks like on screen.

In order to learn how to configure the logic analyzer, we recommend that you follow the exercise to "Acquiring the Data" before loading the file from the disc.

You can also compare your configuration with the one on the disc by printing it (if you have a printer) or making notes before you load the file.

Problem Solving with the Timing Analyzer

In this exercise, assume you are designing a dynamic RAM memory (DRAM) controller and you must verify the timing of the row address strobe (RAS) and the column address strobe (CAS). You are using a 4116 dynamic RAM and the data book specifies that the minimum time from when LRAS is asserted (goes low) to when LCAS is no longer asserted (goes high) is 250 ns. You could use an oscilloscope but you have an HP 1650A/51A on your bench. Since the timing analyzer will do just fine when you don't need voltage parametrics you decide to go ahead and use the logic analyzer.

What Am I Going to Measure?

After configuring the logic analyzer and hooking it up to your circuit under test, you will be measuring the time (x) from when the RAS goes low to when the CAS goes high, as shown below.

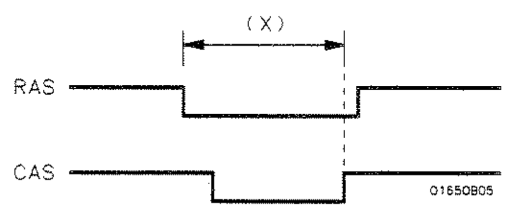


Figure 12-1. RAS and CAS Signals

How Do I Configure the Logic Analyzer?

In order to make this timing measurement, you must configure the logic analyzer as a timing analyzer. By following these steps you will configure Analyzer 1 as the timing analyzer.

If you are in the System Configuration menu you are in the right place to get started and you can start with step 2; otherwise, start with step 1.

1. Using the field in the upper left corner of the display, get the System Configuration menu on screen.

   a. Place the cursor on the field in the upper left corner of the display and press SELECT.

   b. Place the cursor on System and press SELECT.

2. In the System Configuration menu, change Analyzer 1 type to Timing. If analyzer 1 is already a timing analyzer, go on to step 3.

   a. Place the cursor on the Type: ____ field and press SELECT.

   b. Place the cursor on Timing and press SELECT.

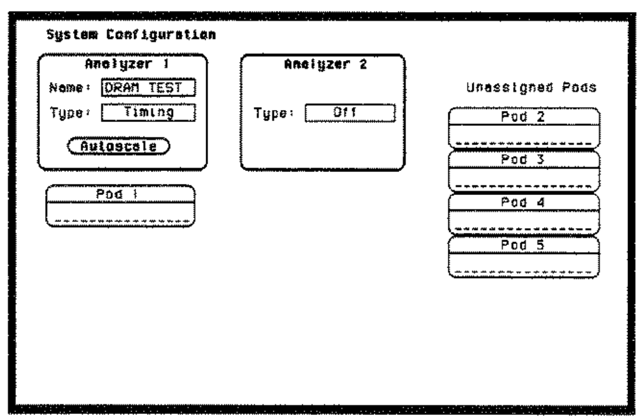


Figure 12-2. System Configuration Menu

3. Name Analyzer 1 "DRAM TEST" (optional)

   a. Place the cursor on the Name: ____ field of Analyzer 1 and press SELECT.

   b. With the Alpha Entry pop-up, change the name to "DRAM TEST" (see "How to Enter Alpha Data" in chapter 3 if you need a reminder).

4. Assign pod 1 to the timing analyzer.

   a. Place the cursor on the Pod 1 field and press SELECT.

   b. In the Pod 1 pop-up, place the cursor on Analyzer 1 and press SELECT.

Connecting the Probes

At this point, if you had a target system with a 4116 DRAM memory IC, you would connect the logic analyzer to your system.

Since you will be assigning Pod 1 bit 0 to the RAS label, you hook Pod 1 bit 0 to the memory IC pin connected to the RAS signal. You hook Pod 1 bit 1 to the IC pin connected to the CAS signal.

Activity Indicators

When the logic analyzer is connected and your target system is running, you will see ↕ at the right-most end (least significant bits) of the Pod 1 field in the System Configuration menu. This indicates the RAS and CAS signals are transitioning.

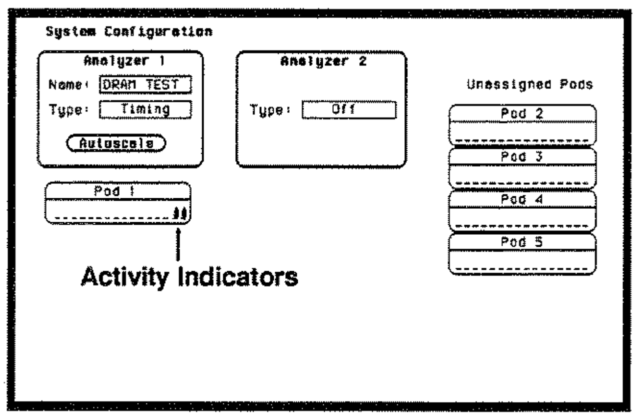


Figure 12-3. Activity Indicators

Configuring the Timing Analyzer

Now that you have configured the system, you are ready to configure the timing analyzer. You will be:

- Creating two names (labels) for the input signals
- Assigning the channels connected to the input signals
- Specifying a trigger condition

1. Display the TIMING FORMAT SPECIFICATION menu.

   a. Press the FORMAT key on the front panel.

2. Name two labels, one RAS and one CAS.

   a. Place the cursor on the top field in the label column and press SELECT.

   b. Place the cursor on Modify label and press SELECT .

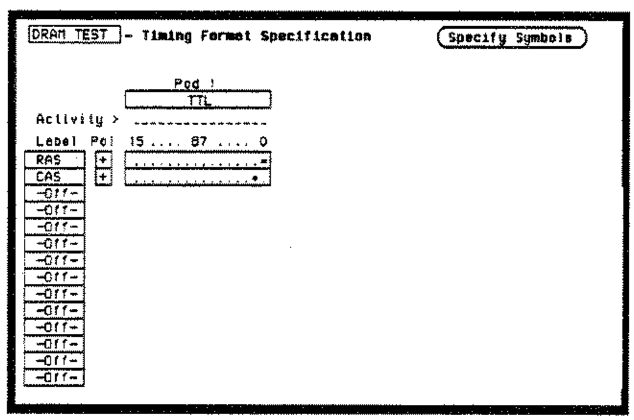


Figure 12-4. Timing Format Specification Menu

c. With the Alpha Entry pop-up, change the name of the label to RAS.

d. Name the second label CAS by repeating steps a through c.

3. Assign the channels connected to the input signals (Pod 1 bits 0 and 1) to the labels RAS and CAS respectively.

a. Place the cursor on the bit assignment field below Pod 1 and to the right of RAS and press SELECT.

b. Any combination of bits may be assigned to this pod; however, you will want only bit 0 assigned to the RAS label. The easiest way to assign bits is to press the CLEAR ENTRY key to unassign any assigned bits before you start.

c. Place the cursor on the period under the 0 in the bit assignment pop-up and press SELECT . This will place an asterisk in the pop-up for bit 0 indicating Pod 1 bit 0 is now assigned to the RAS label. Place cursor on Done and press SELECT to close the pop-up.

d. Assign Pod 1 bit 1 to the CAS label by moving the cursor to bit 1 and pressing SELECT.

Specifying a Trigger Condition

To capture the data and then place the data of interest in the center of the display of the TIMING WAVEFORMS menu, you need to tell the logic analyzer when to trigger. Since the first event of interest is when the LRAS is asserted (negative-going edge of RAS), you need to tell the logic analyzer to trigger on a negative-going edge of the RAS signal.

1. Select the TIMING TRACE menu by pressing the TRACE key.

2. Set the trigger so that the logic analyzer triggers on the negative-going edge of the RAS.

   a. Place the cursor on the Then find Edge field under the label RAS, then press SELECT.

   b. Place the cursor on the . (period) in the pop-up and press SELECT once. Pressing SELECT once in this pop-up changes a period to ↓ which indicates a negative-going edge.

   c. Place the cursor on Done and press SELECT. The pop-up closes and a $ will be located in this field. The $ indicates an edge has been specified even though it can't be shown in the HEX base.

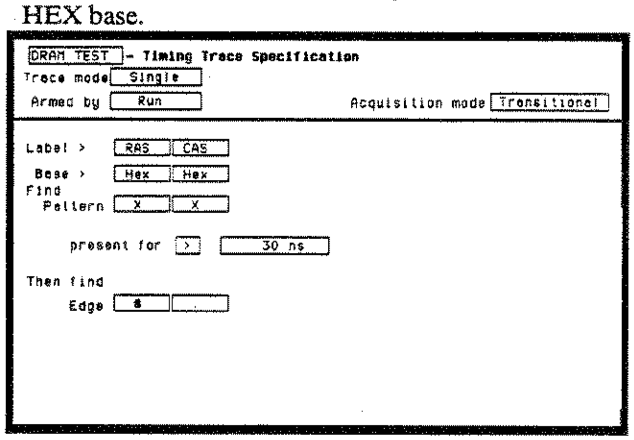


Figure 12-5. Trigger Edge Specified

Acquiring the Data

Now that you have configured and connected the logic analyzer, you acquire the data for your measurement by pressing the RUN key. The logic analyzer will look for a negative edge on the RAS signal and trigger if it sees one. When it triggers, the display switches to the TIMING WAVEFORMS menu.

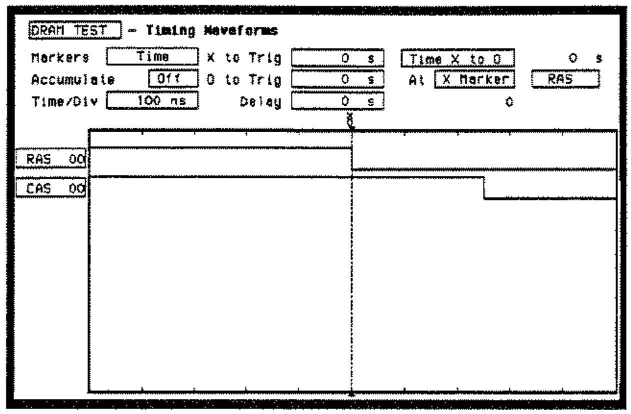


Figure 12-6. Timing Waveforms Menu

The RAS label shows you the RAS signal and the CAS label shows you the CAS signal. Notice the RAS signal goes low at or near the center of the waveform display area (horizontal center).

Now is the time to load the timing measurement demo file from the disc if you wish. The file name is TIMINGDEMO. Refer to "Load Operation" in chapter 6 if you need a reminder on how to load a file.

The Timing Waveforms Menu

The Timing Waveforms menu differs from the other menus you have used so far in this exercise. Besides displaying the acquired data, it has menu fields that you use to change the way the acquired data is displayed and fields that give you timing answers. Before you can use this menu to find answers, you need to know some of the special symbols and their functions. The symbols are:

- The X and O
- The ▼
- The vertical dotted line

The X and O

The X and O are markers you use to find your answer. You place them on the points of interest on your waveforms, and the logic analyzer displays the time between the markers. The X and O markers will be in the center of the display when X to trig (ger) and O to trig (ger) are both 0.000 s (see example below).

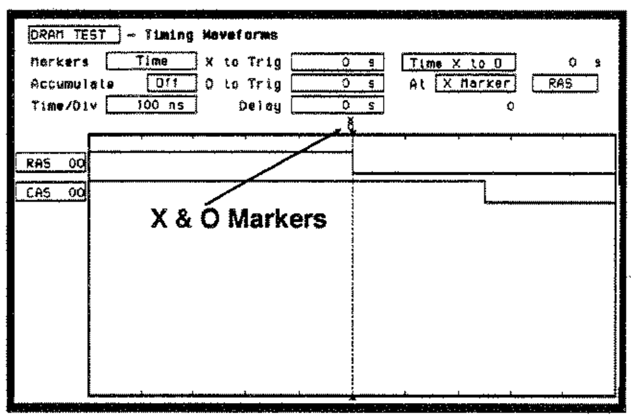


Figure 12-7. X & O Markers

The ▼

The ▼(inverted triangle) indicates the trace point. Remember, trace point = trigger + delay. Since delay in this example is 0.000 s, you will see the negative-going edge of the RAS signal at center screen under the ▼.

The Vertical Dotted Line

The vertical dotted line indicates the trigger point you specified in the Timing Trace Specification menu. The vertical dotted line is at center screen under the inverted triangle and is superimposed on the negative-going edge of the RAS signal.

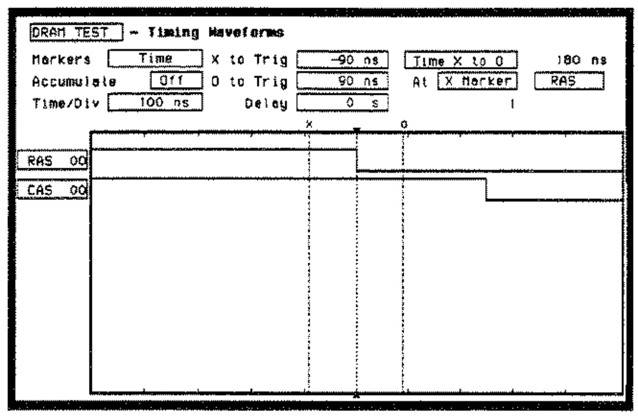


Figure 12-8. Inverted Triangle & Vertical Dotted Line

Configuring the Display

Now that you have acquired the RAS and CAS waveforms, you need to configure the Timing Waveforms menu for best resolution and to obtain your answer.

Display Resolution

You get the best resolution by changing the Time/Div to a value that displays one negative-going edge of both the RAS and CAS waveforms. Set the Time/Div by following these steps.

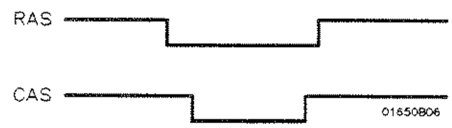


Figure 12-9. RAS and CAS Signals

1. Place the cursor on Time/Div and press SELECT . The Time/Div pop-up appears, showing you the current setting.

2. While the pop-up is present, rotate the KNOB until your waveform shows you only one negative-going edge of the RAS waveform and one positive-going edge of the CAS waveform (see above). In this example 200 ns is best.

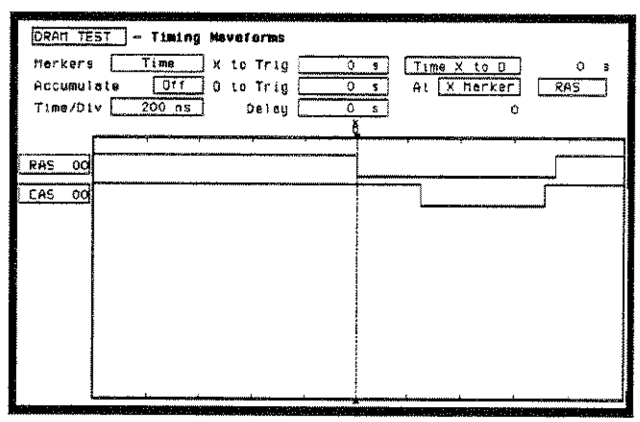


Figure 12-10. Changing Time/Div

Making the Measurement

What you want to know is how much time elapses between the time RAS goes low and the time CAS goes high again. You will use the X and O markers to quickly find the answer. Remember, you specified the negative-going edge of the RAS to be your trigger point; therefore, the X marker should be on this edge if X to Trig = 0. If not, follow steps 1 and 2.

1. Place the cursor on the X to Trig field and press SELECT . A pop-up will appear showing you the current time from the X marker to the trigger; however, you don't need to worry about this number now.

2. Rotate the KNOB to place the X marker on the negative-going edge of the RAS waveform and press SELECT . The pop-up closes and displays X to Trig = 0.000 s.

3. Place the cursor on O to Trig and press SELECT . Repeat step 2 except place the O marker on the positive-going edge of the CAS waveform and press SELECT. The pop-up closes and displays O to Trig = 710 ns.

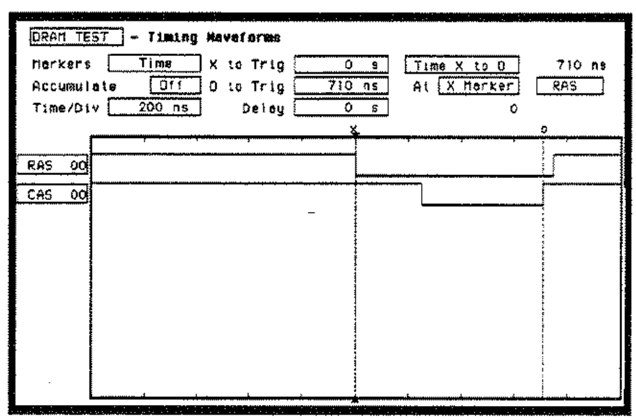


Figure 12-11. Marker Placement

Finding the Answer

Your answer could be calculated by adding the X to Trig and O to Trig times, but you don't need to bother. The logic analyzer has already calculated this answer and displays it in the Time X to O ____ field.

This example indicates the time is 710 ns. Since the data book specifies a minimum of 250 ns, it appears your DRAM controller circuit is designed properly.

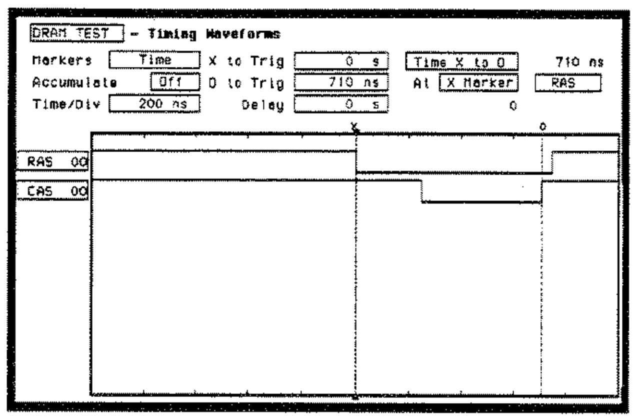


Figure 12-12. Time X to O

Summary

You have just learned how to make a simple timing measurement with the HP 1650A/51A logic analyzer. You have:

- specified a timing analyzer
- assigned pod 1
- assigned bits
- assigned labels
- specified a trigger condition
- learned which probes to connect
- acquired the data
- configured the display
- set the Time/Div for best resolution
- positioned the markers for the measurement answer

You have seen how easy it is to use the timing analyzer to make timing measurements that you could have made with a scope. You can use the timing analyzer for any timing measurement that doesn't require voltage parametrics or doesn't go beyond the accuracy of the timing analyzer.

13

The State Analyzer

Introduction

This chapter introduces the state analyzer and contains the state analyzer menu maps.

- Chapter 14 explains the State Format menu
- Chapter 15 explains the State Trace menu
- Chapter 16 explains the State Listing menu
- Chapter 17 explains the State Compare menu
- Chapter 18 explains the State Chart menu
- Chapter 19 explains the State Waveform menu
- Chapter 20 gives you a basic State Analyzer Measurement example

The State Analyzer (An Overview)

The state analyzer acquires data synchronously using the system-under-test to clock the acquired data. The acquired data is displayed in a list form in the State Listing menu and in waveform form in the State Waveform menu. The state analyzer differs from the timing analyzer in that the acquisition clock is provided by the system-under-test instead of the internal acquisition clock used by the timing analyzer. Therefore, the State Waveform menu displays the state waveforms referenced by states per division and not seconds per division as in the timing analyzer.

State Analyzer Menu Maps

The State Analyzer menu maps show you the fields and the available options of each field within the six menus. The menu maps will help you get an overview of each menu as well as provide you with a quick reference of what each menu contains.

State Format Menu Map

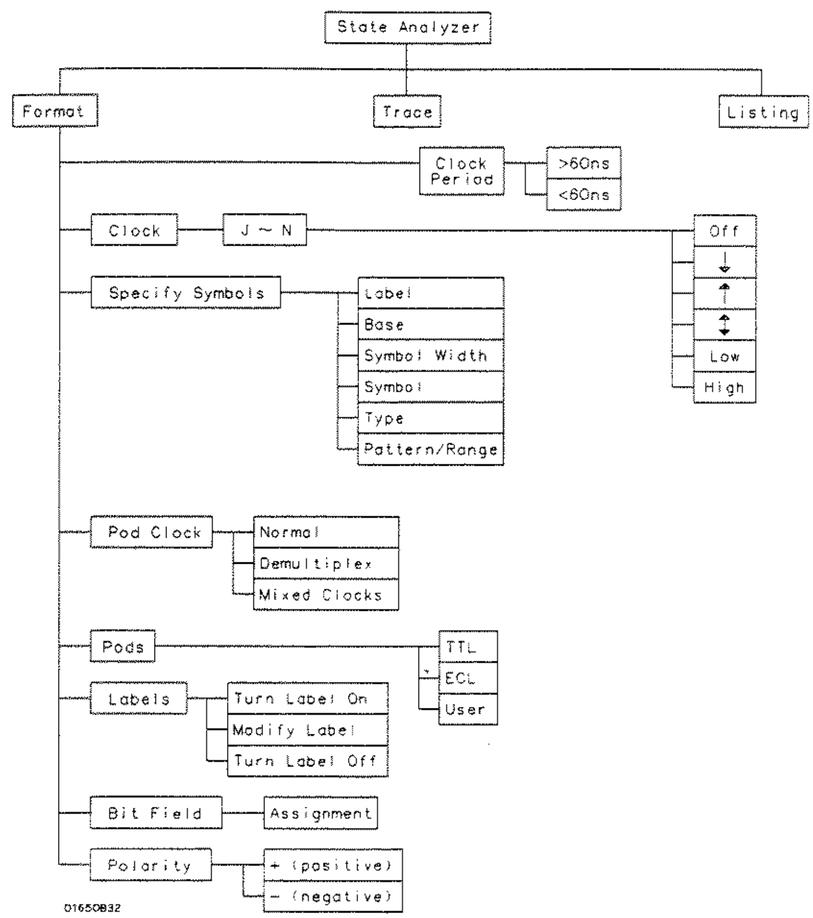


Figure 13-1. State Format Menu Map

State Trace Menu Map

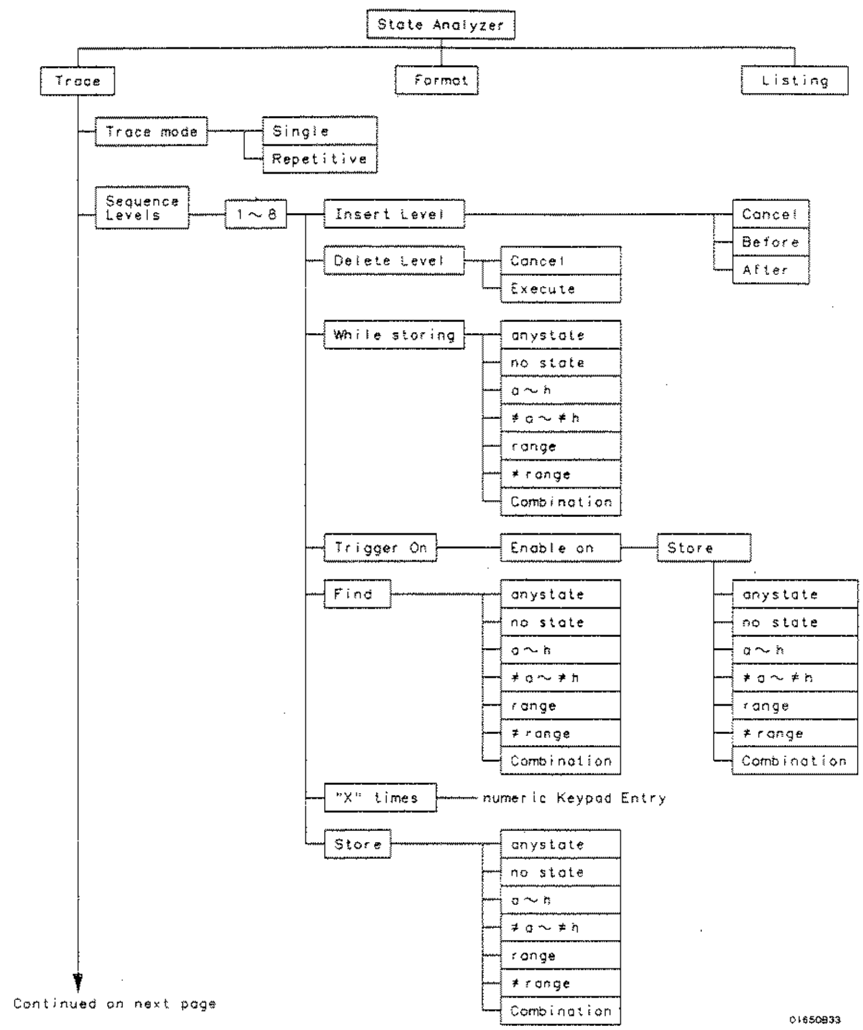


Figure 13-2. State Trace Menu Map

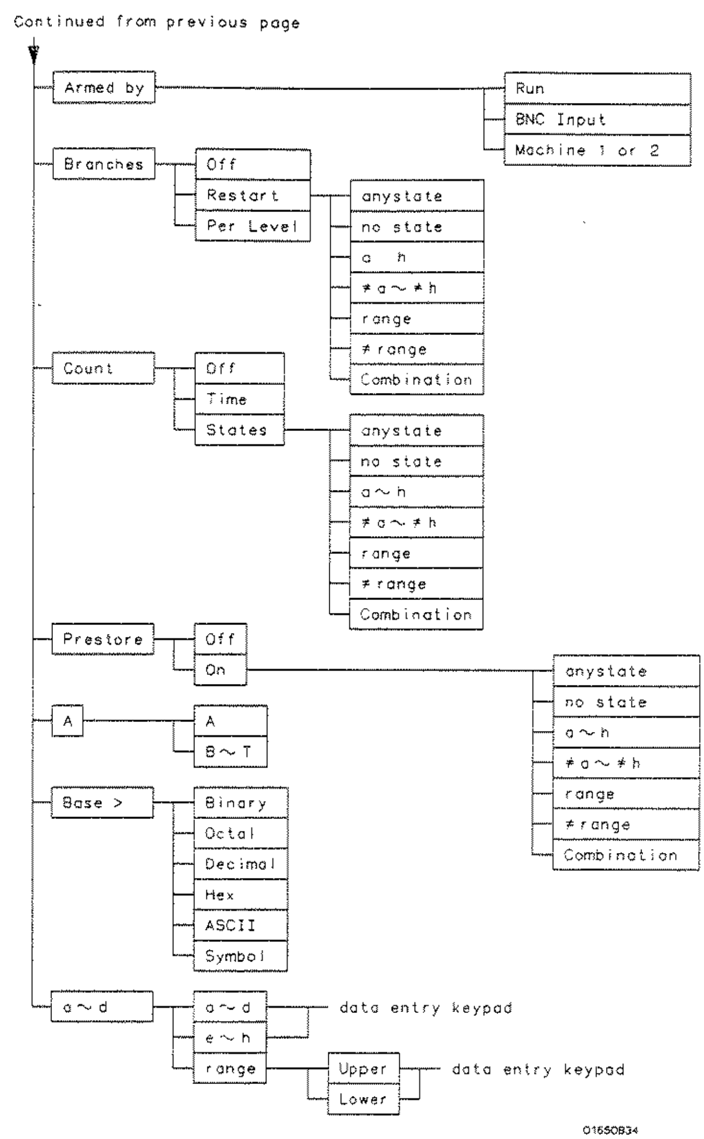


Figure 13-2. State Trace Menu Map (continued)

State Listing Menu Map

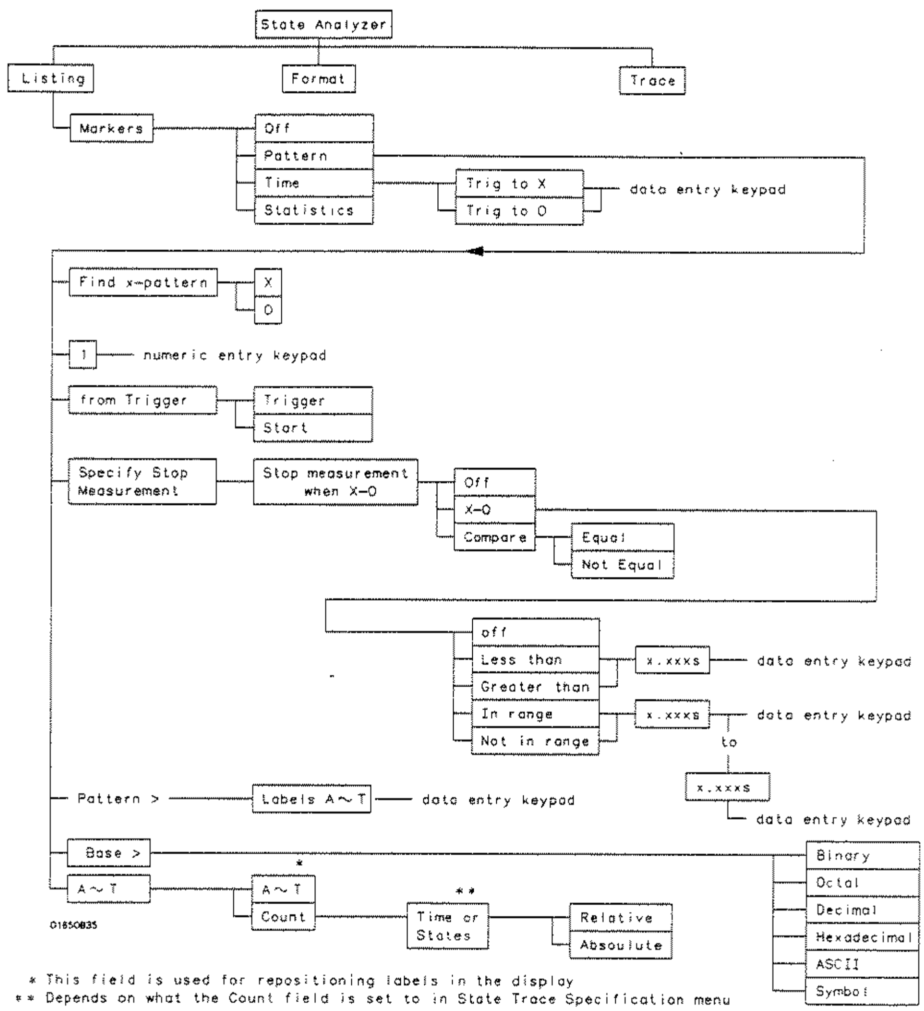


Figure 13-3. State Listing Menu Map

State Compare Menu Map

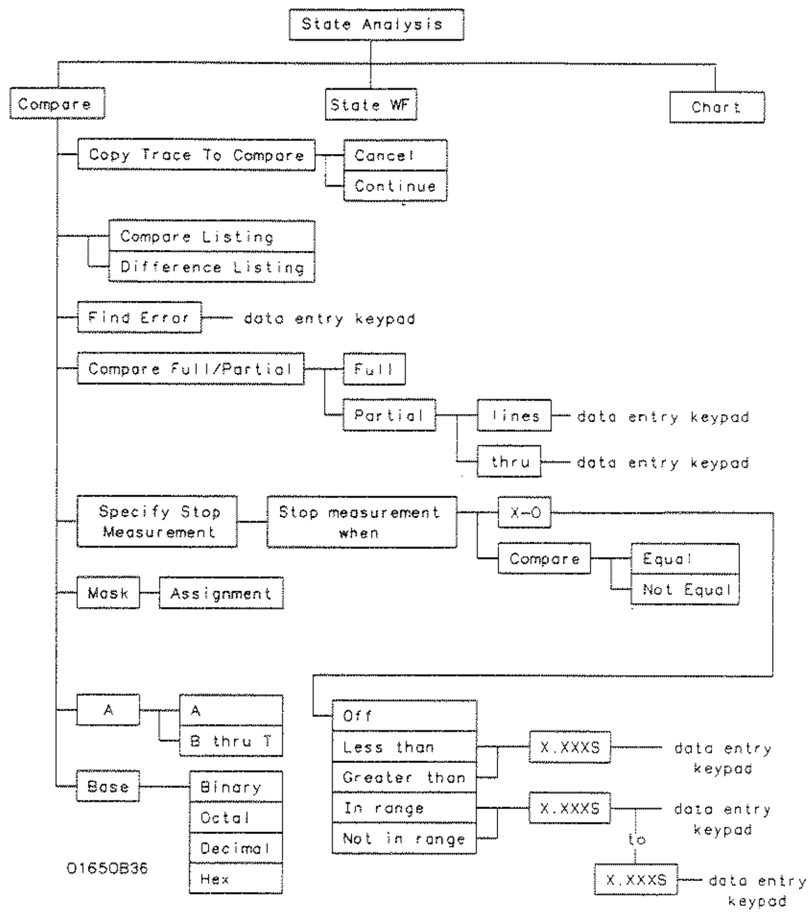


Figure 13-4. State Compare Menu Map

State Waveform Menu Map

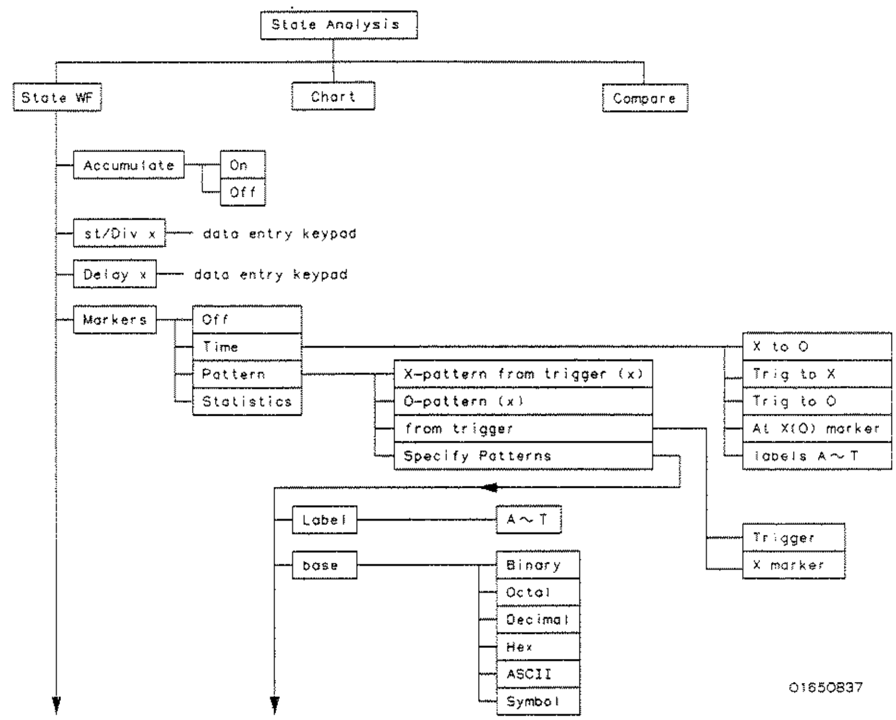


Figure 13-5. State Waveform Menu Map

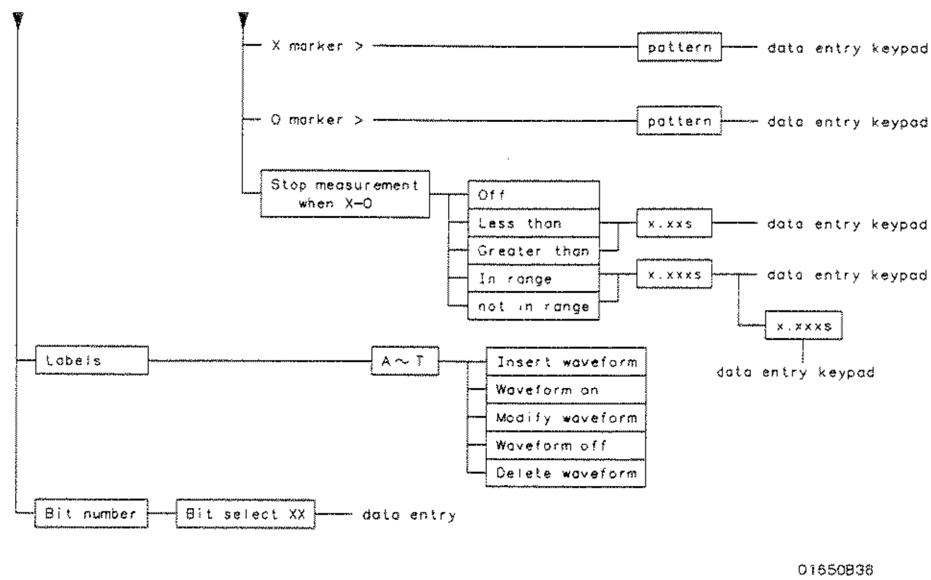


Figure 13-5. State Waveform Menu Map (continued)

State Chart Menu Map

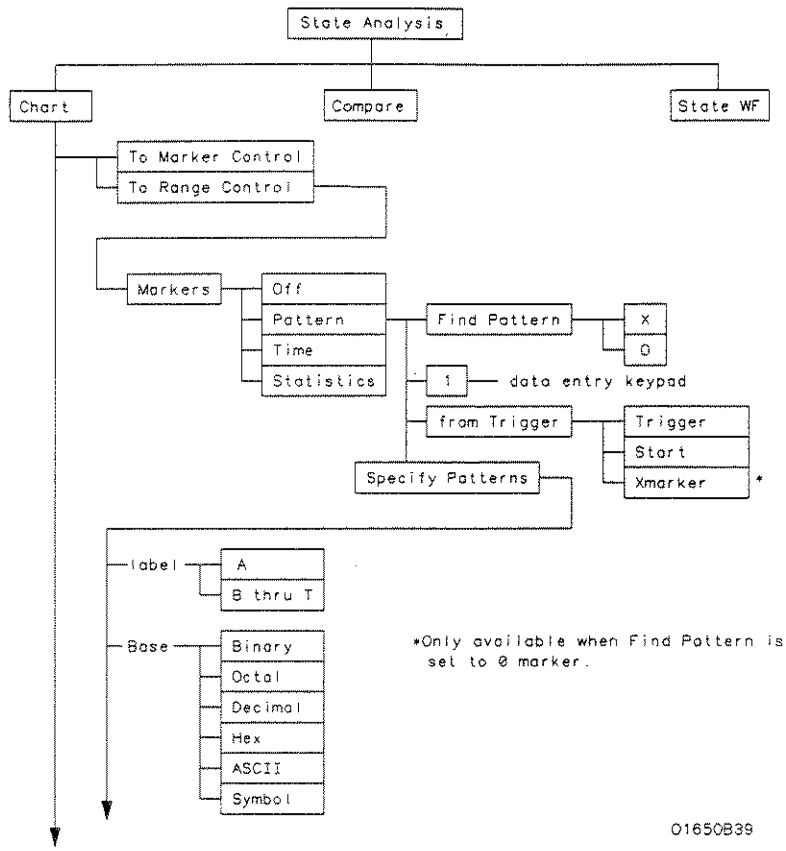


Figure 13-6. State Chart Menu Map

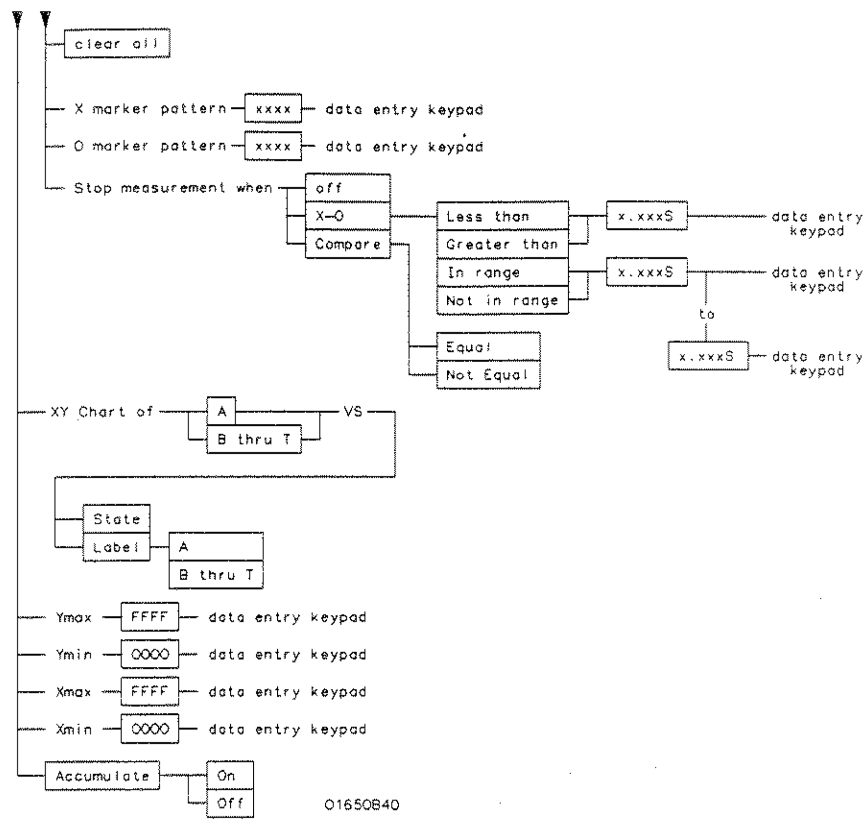


Figure 13-6. State Chart Menu Map (continued)

14

State Format Specification Menu

Introduction

This chapter describes the State Format Specification menu and all pop-up menus that you will use on your state analyzer. The purpose and functions of each menu are explained in detail, and we have included many illustrations and examples to make the explanations clearer.

Accessing the State Format Specification Menu

The State Format Specification menu can be accessed by pressing the FORMAT key on the front panel. If the Timing Format Specification Menu is displayed when you press the FORMAT key, you will have to switch analyzers. This is not a problem, it merely indicates that the last action you performed in the System Configuration Menu was on the timing analyzer.

State Format Specification Menu

The State Format Specification menu lets you configure the logic analyzer to group channels from your microprocessor into labels you assign for your measurements. You can set the threshold levels of the pods assigned to the state analyzer, assign labels and channels, specify symbols, and set clocks for triggering.

At power up, the logic analyzer is configured with a default setting. You can use this default setting to make a test measurement on the system under test. It can give you an idea of where to start your measurement. For an example of setting up configurations for the a State analyzer, refer to your *Getting Started Guide* or "State Analyzer Measurement Example" in Chapter 20 of this manual.

At power up the State Format Specification menu looks like that shown below:

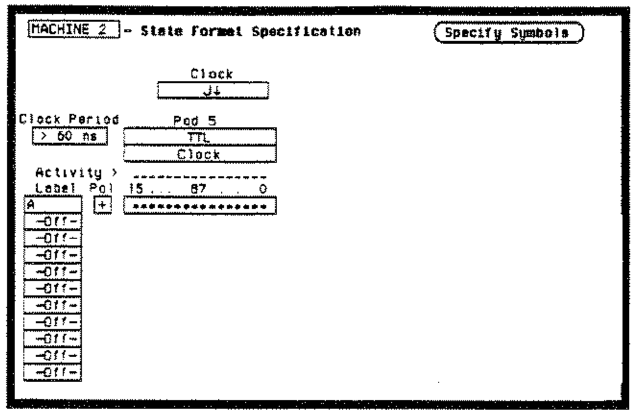


Figure 14-1. State Format Specification Menu

The State Format Specification menu for the HP 1651B is similar to that for the HP 1650B except that Pod 2 appears in the menu instead of Pod 5.

This menu shows only one pod assigned to each analyzer, which is the case at power up. Any number of pods can be assigned to one analyzer, from none to all five for the HP 1650B, and from none to two for the HP 1651B. In the State Format Specification menu, only three pods appear at a time in the display. To view any pods that are off screen, press the left/right ROLL key and rotate the KNOB. The pods are always positioned so that the lowest numbered pod is on the right and the highest numbered pod is on the left.

State Format Specification Menu Fields

Seven types of fields are present in the menus. They are:

- Label
- Polarity (Pol)
- Bit assignments
- Pod threshold
- Specify Symbols
- Clock
- Pod Clock
- Clock Period

A portion of the menu that is not a field is the Activity Indicators display. The indicators appear under the active bits of each pod, next to "Activity > ." When the logic analyzer is connected to your target system and the system is running, you will see ↕ in the Activity Indicators display for each channel that has activity. These tell you that the signals on the channels are transitioning.

The fields in the Format menus are described in the following sections.

Label

The label column contains 20 Label fields that you can define. Of the 20 labels, the state analyzer displays only 11 labels at one time. To view the labels that are off screen, press the up/down ROLL key and rotate the KNOB. The labels scroll up and down. To deactivate the scrolling, press the ROLL key again.

To access one of the Label fields, place the cursor on the field and press SELECT. You will see a pop-up menu like that shown below.

```
Turn label on
Modify label
Turn label off
```

Figure 14-2. Label Pop-Up Menu

Turn Label On

Selecting this option turns the label on and gives it a default letter name. If you turned all the labels on they would be named A through T from top to bottom. When a label is turned on, bit assignment fields for the label appear to the right of the label under the pods.

Modify Label

If you want to change the name of a label, or want to turn a label on and give it a specific name, you would select the Modify label option. When you do, an Alpha Entry pop-up menu appears. You can use the pop-up menu and the keypad on the front panel to name the label. A label name can be a maximum of six characters.

Turn Label Off

Selecting this option turns the label off. When a label is turned off, the bit assignments are saved by the logic analyzer. This gives you the option of turning the label back on and still having the bit assignments if you need them. The waveforms and state listings are also saved.

You can give the same name to a label in the state analyzer as in the timing analyzer without causing an error. The logic analyzer distinguishes between them. An example of this appears in the *Getting Started Guide* and in chapter 20 of this manual.

Polarity (Pol)

Each label has a polarity assigned to it. The default for all the labels is positive (+) polarity. You can change the polarity of a label by placing the cursor on the polarity field and pressing SELECT. This toggles the polarity between positive (+) and negative (−).

In the state analyzer, negative polarity inverts the data.

Bit Assignment

The bit assignment fields allow you to assign bits (channels) to labels. Above each column of bit assignment fields is a line that tells you the bit numbers from 0 to 15, with the left bit numbered 15 and the right bit numbered 0. This line helps you know exactly which bits you are assigning.

The convention for bit assignment is:

* (asterisk) indicates assigned bit
. (period) indicates unassigned bit

At power up the 16 bits of Pod 1 are assigned to the timing analyzer and the 16 bits of Pod 5 are assigned to the state analyzer.

To change a bit assignment configuration, place the cursor on a bit assignment field and press SELECT. You will see the following pop-up menu.

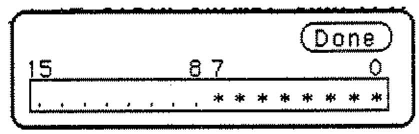


Figure 14-3. Bit Assignment Pop-Up Menu

Use the KNOB to move the cursor to an asterisk or a period and press SELECT. The bit assignment toggles to the opposite state of what it was before. When the bits (channels) are assigned as desired, place the cursor on Done and press SELECT. This closes the pop-up and displays the new bit assignment.

Assigning one channel per label may be handy in some applications. This is illustrated in chapter 8 of the *Getting Started Guide*. Also, you can assign a channel to more than one label, but this usually isn't desired.

Labels may have from 1 to 32 channels assigned to them. If you try to assign more than 32 channels to a label, the logic analyzer will beep, indicating an error, and a message will appear at the top of the screen telling you that 32 channels per label is the maximum.

Channels assigned to a label are numbered from right to left by the logic analyzer. The least significant assigned bit (LSB) on the far right is numbered 0, the next assigned bit is numbered 1, and so on. Since 32 channels can be assigned to one label at most, the highest number that can be given to a channel is 31.

Although labels can contain split fields, assigned channels are always numbered consecutively within a label. The numbering of channels is illustrated with the figure below.

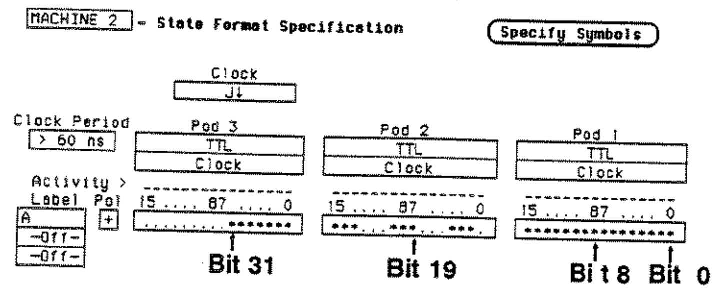


Figure 14-4. Numbering of Assigning Bits

Pod Threshold

Each pod has a threshold level assigned to it. For the HP 1651B Logic Analyzer, threshold levels may be defined for Pods 1 and 2 individually. For the HP 1650B Logic Analyzer, threshold levels may be defined for Pods 1, 2 and 3 individually, and one threshold for Pods 4 and 5. It does not matter if Pods 4 and 5 are assigned to different analyzers. Changing the threshold of one will change the threshold of the other.

If you place the cursor on one of the pod threshold fields and press SELECT, you will see the following pop-up menu.

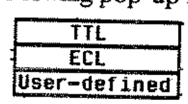


Figure 14-5. Pod Threshold Pop-Up Menu

TTL sets the threshold at + 1.6 volts, and ECL sets the threshold at – 1.3 volts.

The User-defined option lets you set the threshold to a specific voltage between -9.9 V and $+9.9$ V. If you select this option you will see a Numeric Entry pop-up menu as shown.

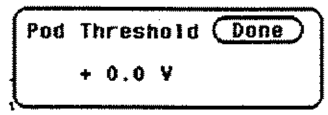


Figure 14-6. User-defined Numeric Entry Pop-Up Menu

You can change the value in the pop-up either with the keypad on the front panel or with the KNOB, which you rotate until you get the desired voltage. When the correct voltage is displayed, press SELECT. The pop-up will close and your new threshold will be placed in the pod threshold field.

The threshold level you specify for the 16 data bits also applies to a pod's clock threshold.

Specify Symbols

This field provides access to the Specify Symbols menu. It differs from the other fields in the State Format Specification menu in that it displays a complete menu instead of a pop-up. The complete description of the Specify Symbols Menu follows the State Format Specification Menu fields later in this chapter.

Clock

The Clock field in the Format Specification menu displays the clocks for clocking your system. The display will be referred to as the "clocking arrangement."

The HP 1650B Logic Analyzer has five clock channels, each of which is on a pod. The clocks are connected through the pods simply for convenience. The clock channels are labeled J, K, L, M, and N and are on pods 1 through 5, respectively. The clocking of the state analyzer is synchronous with your system because your analyzer uses the signals present in your system. The signal you use must clock the analyzer when the data you want to acquire is valid.

The HP 1651B Logic Analyzer has two clock channels, each on one of the pods. The J clock is on pod 1 and the K clock is on pod 2.

When you select the Clock field, you will see the following pop-up menu with which you specify the clock.

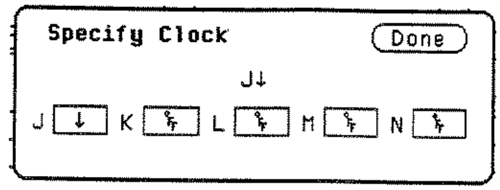


Figure 14-7. Clock Pop-Up Menu

You can use one of the clocks alone or combine them to build one clocking arrangement. If you select a field to the right of one of the clocks in the pop-up you will see another pop-up menu:

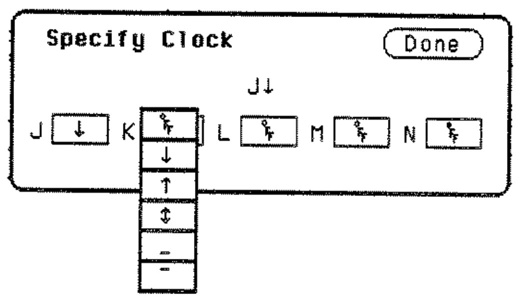


Figure 14-8. Single Clock Pop-Up Menu

You can specify the negative edge of the clock, the positive edge either edge, a high level, a low level, or the clock to be off.

The clocks are combined by ORing and ANDing them. Clock edges are ORed to clock edges, clock levels are ORed to clock levels, and clock edges are ANDed to clock levels.

For example, if you select ↓ for the J clock, ↑ for the K clock, _ for the M clock, and ‾ for the N clock, the resulting clocking arrangement will appear in the display as:

```
Clock
( J↓ + K↑ ) • ( M_ + N‾ )
```

Figure 14-9. Example of a Clocking Arrangement

With this arrangement, the state analyzer will clock the data when there is a negative edge of the J clock OR a positive edge of the K clock, AND when there is a low level on the M clock OR a high level on the N clock.

You must always specify at least one clock edge. If you try to use only clock levels, the logic analyzer will display a message telling you that at least one edge is required.

Pod Clock

Your logic analyzer has the capability of clocking data in three different ways. The pod Clock fields in the State Format Specification menu allow you to specify which of the three ways you want to clock the data.

Each pod assigned to the state analyzer has a pod Clock field associated with it. Selecting one of the pod Clock fields gives you the following pop-up menu:

```
Normal
Demultiplex
Mixed Clocks
```

Figure 14-10. Pod clock Field Pop-Up Menu

Normal

This option specifies that clocking will be done in single phase. That is the clocking arrangement located in the Clock field above the pods in the State Format Specification menu will be used to clock all the pods assigned to this machine.

For example, suppose that the Clock field looks like the following:

```
   Clock
( J↓ + K↑ )
```

Figure 14-11. Example of a Clocking Arrangement

In Normal mode the state analyzer will sample the data on any assigned pods on a negative edge of the J clock OR on a positive edge of the K clock.

Demultiplex

With the HP 1650B/51B Logic Analyzers, you can clock two different types of data that occur on the same lines. For instance, lines that transfer both address and data information need to be clocked at different times in order to get the right information at the right time. The Demultiplex option provides the means to do this.

When you select the Demultiplex option, the pod Clock field changes to "Master | Slave," and two clock fields appear above the pods where just one Clock field used to be. These fields are the Master Clock and Slave Clock, as shown:

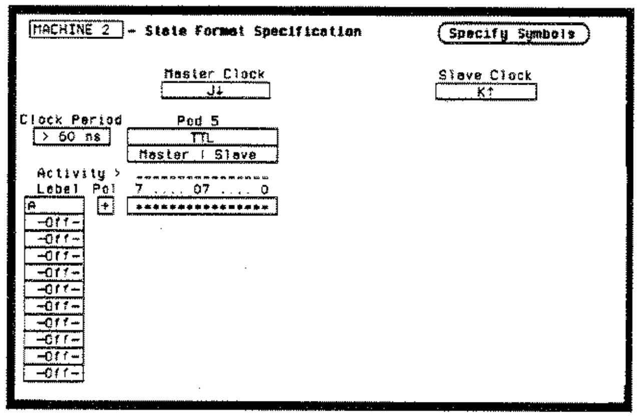


Figure 14-12. Master Clock and Slave Clock

Demultiplexing is done on the data lines of the specified pod to read only the lower eight bits. This is two-phase clocking, with the Master Clock following the Slave Clock. The analyzer first looks for the clocking arrangement that you specify in the Slave Clock. When it sees this arrangement, the analyzer clocks the data present on bits 0-7 of the pod, then waits for the clocking arrangement that you specify in the Master Clock. When it sees this arrangement, it again clocks the data present on bits 0-7 of the pod. The upper eight bits of the pods are ignored and don't need to be connected to your system.

Notice, the bit numbers that appear above the bit assignment field have changed. The bits are now numbered 7....07....0 instead of 15....87....0 . This helps you set up the analyzer to clock the right information at the right time.

The address/data lines AD0-AD7 on the 8085 microprocessor are an example of Demultiplex. During part of the operating time the lines have an address on them, and during other times they have data on them. Hook the lower eight bits of one of the pods to these eight lines and set the Slave and Master Clocks so that they clock the data and the address at the proper time.

In this example, you may choose to assign the bits in the State Format Specification menu similarly to that shown below. In this case you would want to clock the address with the Slave Clock and the data with the Master Clock.

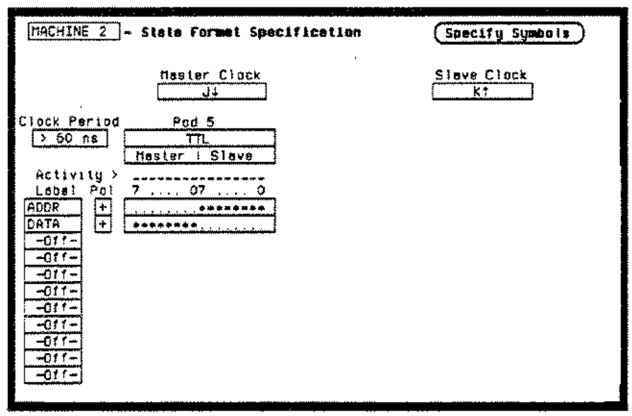


Figure 14-13. Master and Slave Clock Bit Assignments

The Master and Slave Clocks can have the same clocking arrangements. The clocking is still done the same way, with the lower eight bits being clocked first on the Slave Clock, then on the Master Clock.

Mixed Clocks

The Mixed Clocks option allows you to clock the lower eight bits of a pod separately from the upper eight bits. The state analyzer uses Master and Slave Clocks to do this. If you select this option from the pod Clock pop-up, the pod Clock field changes to "Master | Slave," and two Clock fields, Master and Slave, appear above the pods.

As in Demultiplex, the Master Clock follows the Slave Clock. The state analyzer looks for the clocking arrangement given by the Slave Clock and clocks the lower eight bits. Then it looks for the clock arrangement given by the Master Clock and clocks the upper eight bits. Unlike Demultiplex, all 16 bits of a pod are sampled.

The Master and Slave Clocks can have the same clocking arrangements. The clocking is still done the same way, with the lower eight bits clocked on the Slave Clock and the upper eight bits clocked on the Master Clock.

Clock Period

This field provides greater measurement accuracy when your state input clock period is greater than 60 ns. When you select **> 60 ns**, the state analyzer provides greater immunity against noise or ringing in the state input clock signal; also, the logic analyzer provides greater accuracy when triggering another state or timing analyzer or the BNC trigger out.

If your State input clock period is less than 60 ns, you should select **< 60 ns**. This and disables the Count field in the State Trace Specification menu because the maximum clock rate when counting is 16.67 MHz (60 ns clock period). This also turns Prestore off.

Specify Symbols Menu

The logic analyzer supplies Timing and State Symbol Tables in which you can define a mnemonic for a specific bit pattern of a label. When measurements are made by the state analyzer, the mnemonic is displayed where the bit pattern occurs if the Symbol base is selected.

It is possible for you to specify up to 200 symbols in the logic analyzer. If you have only one of the internal analyzers on, all 200 symbols can be defined in it. If both analyzers are on, the 200 symbols are split between the two. For example, analyzer 1 may have 150, leaving 50 available for analyzer 2.

To access the Symbol Table in the State Format Specification menu, place the cursor on the Specify Symbols field and press SELECT. You will see a new menu as shown. This is the default setting for the Symbol Table in both the timing and state analyzers.

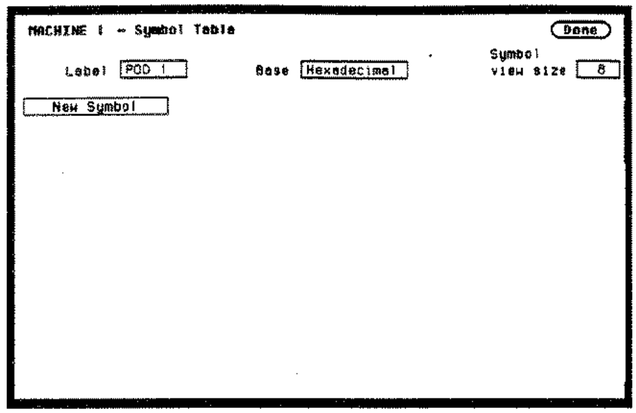


Figure 14-14. Symbol Table Menu

Specify Symbols Menu Fields

There are four fields in the Symbol Table menu. They are:

- Label
- Base
- Symbol view size
- Symbol name

Label

The Label field identifies the label for which you are specifying symbols. If you select this field, you will get a pop-up that lists all the labels turned on for that analyzer.

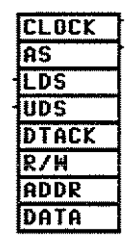


Figure 14-15. Lable Pop-Up Menu

Each label has a separate symbol table. This allows you to give the same name to symbols defined under different labels. In the Label pop-up select the label for which you wish to specify symbols.

Base The Base field tells you the numeric base in which the pattern will be specified. The base you choose here will affect the pattern field of the State Trace Specification menu. This is covered later in this chapter.

To change the base, place the cursor on the field and press SELECT. You will see the following pop-up menu.

Octal
Decimal
Hexadecimal
ASCII

Figure 14-16. Base Pop-Up Menu

If more than 20 channels are assigned to a label, the Binary option is not offered in the pop-up. The reason for this is that when a symbol is specified as a range, there is only enough room for 20 bits to be displayed on the screen.

Decide which base you want to work in and choose that option from the numeric Base pop-up menu.

If you choose the ASCII option, you can see what ASCII characters the patterns and ranges defined by your symbols represent. ASCII characters represented by the decimal numbers 0 to 127 (hex 00 to 7F) are offered on your logic analyzer. Specifying patterns and ranges for symbols is discussed in the next section.

Note You cannot specify a pattern or range when the base is ASCII. First define the pattern or range in one of the other bases, then switch to ASCII to see the ASCII characters.

Symbol View Size

The Symbol view size field lets you specify how many characters of the symbol name will be displayed when the symbol is referenced in the State Trace Specification menu and the State Listing menu. Selecting this field gives you the following pop-up.

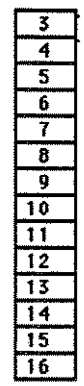


Figure 14-17. Symbol View Size Pop-Up Menu

You can have the logic analyzer display from 3 to all 16 of the characters in the symbol name. For more information see "State Trace Specification Menu" and "State Listing Menu" later in this chapter.

Symbol Name

When you first access the Symbol Table, there are no symbols specified. The symbol name field reads "New Symbol." If you select this field, you will see an Alpha Entry pop-up menu on the display. Use the pop-up menu and the keypad on the front panel to enter the name of your symbol. A maximum of 16 characters can be used in a symbol name.

When you select the Done field in the Alpha Entry pop-up menu the name that appears in the symbol name field is assigned and two more fields appear in the display.

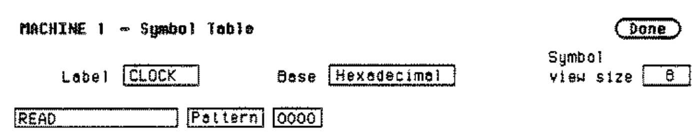


Figure 14-18. Symbol Defined as a Pattern

The first of these fields defines the symbol as either a Pattern or a Range. If you place the cursor on this field and press SELECT, it will toggle between Pattern and Range.

When the symbol is defined as a pattern, one field appears to specify what the pattern is. Selecting this field gives you a pop-up with which you can specify the pattern. Use the keypad and the DON'T CARE key on the front panel to enter the pattern. Be sure to enter the pattern in the numeric base that you specified in the Base field.

Figure 14-19. Specify Pattern Pop-Up Menu

If the symbol is defined as a range, two fields appear in which you specify the upper and lower boundaries of the range.

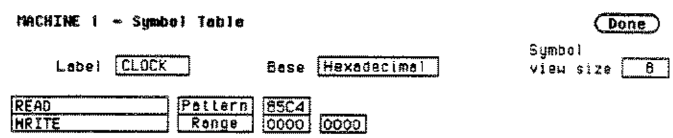


Figure 14-20. Symbol Defined as a Range

Selecting either of these fields gives you a pop-up with which you can specify the boundary of the range.

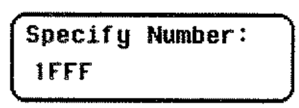


Figure 14-21. Specify Range Pop-Up Menu

You can specify ranges that overlap or are nested within each other. Don't cares are not allowed.

To add more symbols to your symbol table, place the cursor on the last symbol defined and press SELECT. A pop-up menu appears as shown.

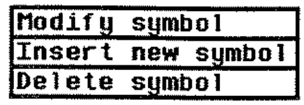


Figure 14-22. Symbol Pop-Up Menu

The first option in the pop-up is Modify symbol. If you select this option, you will see an Alpha Entry pop-up menu with which you can change the name of the symbol.

The second option in the pop-up is Insert new symbol. It allows you to specify another symbol. When you select it, you will see an Alpha Entry pop-up menu. Use the menu and the keypad on the front panel to enter the name of your new symbol. When you select Done, your new symbol will appear in the Symbol Table. The third option in the pop-up is Delete symbol. If you select this option, the symbol will be deleted from the Symbol Table.

Leaving the Symbol Table Menu

When you have specified all your symbols, you can leave the Symbol Table menu in one of two ways. One method is to place the cursor on the Done field and press SELECT. This puts you back in the Format Specification menu that you were in before entering the Symbol Table. The other method is to press the FORMAT, TRACE, or DISPLAY keys on the front panel to get you into the respective menu.

15

State Trace Menu

Introduction

This chapter describes the State Trace menu and the pop-up menus that you will use on your state analyzer. The purpose and functions are described in detail, and we have included many illustrations and examples to make the explanations clearer.

The Trace Specification menu allows you to configure the state analyzer to capture only the data of interest for your measurement. In the state analyzer you can configure the analyzer to trigger on a sequence of states. The default setting is shown in figure 15-1 below.

For an example of setting up a trace configuration for a State analyzer, refer to your *Getting Started Guide* or "State Analyzer Measuement Example" in Chapter 20 of this manual.

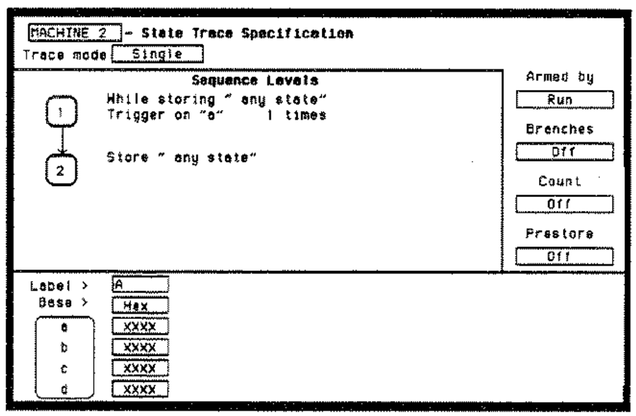


Figure 15-1. State Trace Specification Menu

Accessing the State Trace Menu

The State Trace menu can be accessed by pressing the TRACE key on the front panel. If the Timing Trace Specification menu is displayed when you press the TRACE key, you will have to switch analyzers. This is not a problem, it merely indicates that the last action you performed in the System Configuration Menus was on the timing analyzer.

State Trace Menu Fields

The menu is divided into three sections: the Sequence Levels in the large center box, the acquisition fields at the top and right of the screen, and the qualifier and pattern fields at the bottom of the screen.

Before describing the fields in the menu, we need to define a few terms. These terms will be used in the discussions of the fields, so understanding their meanings is essential.

Pattern Recognizers: a pattern of bits (0, 1, or X) in each label. There are eight recognizers available when one state analyzer is on. Four are available to each analyzer when two state analyzers are on. The pattern recognizers are given the names a through h and are partitioned into groups of four, a-d and e-h.

Range Recognizer: recognizes data which is numerically between or on two specified patterns. One range term is available and is assigned to the first state analyzer created by assigning pods to it or if only one analyzer is on, then the range term is assigned to it.

Qualifier: user-specified term that can be anystate, nostate, a single pattern recognizer, a range recognizer, the complement of a pattern or range recognizer, or a logical combination of pattern and range recognizers. When you select a field to specify a qualifier, you will see the following qualifier pop-up menu.

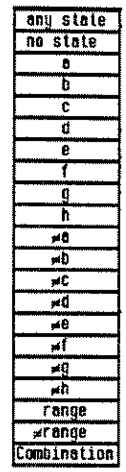


Figure 15-2. Qualifier Pop-Up Menu

If you select the Combination option in the pop-up, you will see a pop-up similar to that shown below.

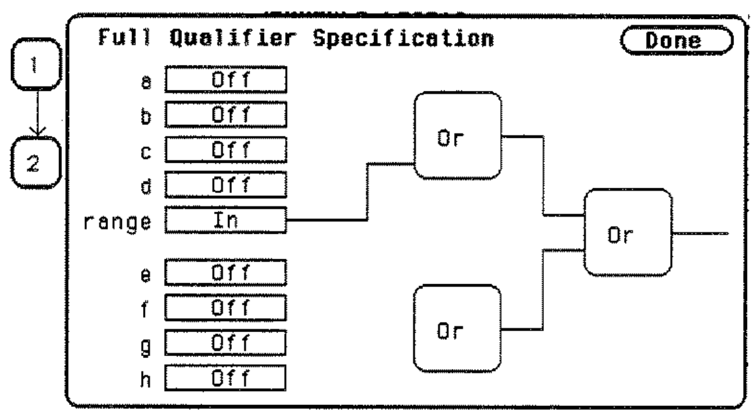


Figure 15-3. Full Qualifier Specification Pop-Up

Note

If two multi-pod state analyzers are on, the qualifier pop-up menu will show that only four pattern recognizers are available to each analyzer. Pattern recognizers a-d and the range recognizer are assigned to the first analyzer created, and pattern recognizers e-h go with the second analyzer. In the Full Qualifier Specification pop-up there will be only one OR gate and one set of pattern recognizers.

With this **Full Qualifier Specification** pop-up, you specify a logical combination of patterns or ranges as the qualifier. The pattern recognizers are always partitioned into the groups of four shown. Only one operator is allowed between the patterns in a group. Patterns in uncomplimented form (a, b, etc.) can only be ORed.

The complements of patterns (≠ a, ≠ b, etc.) can only be ANDed. For example, if the first OR field (gate) is changed to AND, all the patterns for that gate are complemented, as shown below.

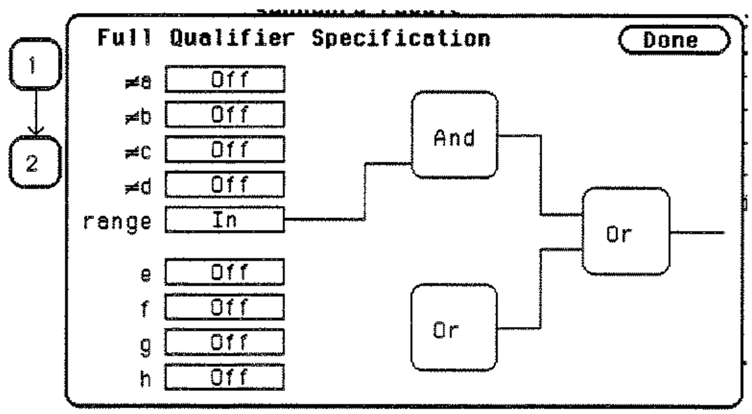


Figure 15-4. Complemented Patterns

To specify a pattern to be used in the combination, place the cursor on the pattern recognizer field and press SELECT. The field toggles from Off to On and a connection is drawn from the pattern field to the gate. In figure 15-5, patterns b, c and d and the range are ORed together, and e and g are ANDed together.

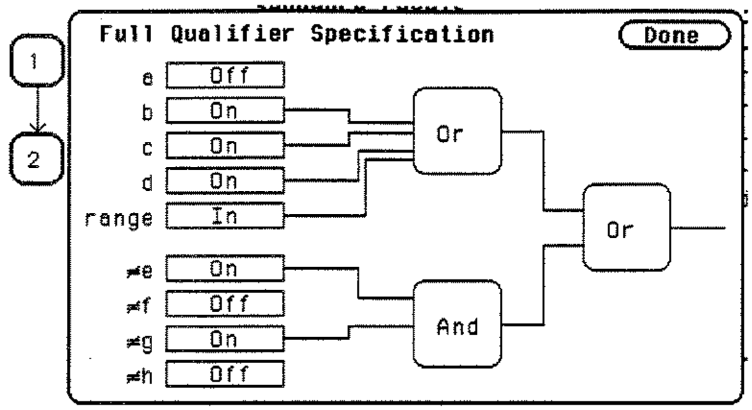


Figure 15-5. Patterns Assigned for Logical Combinations

As shown in the previous figures, the range is included with the first group of patterns (a-d). If you select the range field, you will see the following pop-up menu.

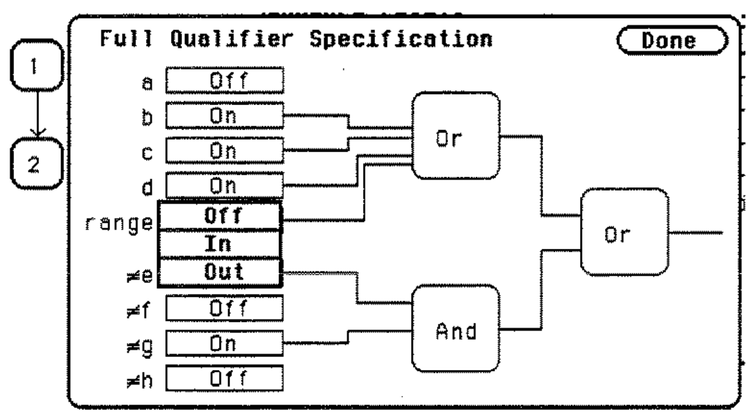


Figure 15-6. Range Specification Pop-Up Menu

Off disconnects the range from the qualifier specification. In indicates that the contents of the range are to be in the qualifier specification, and Out indicates that the complement of the range is to be in the qualifier specification.

When you have specified your combination qualifier, select Done. The **Full Qualifier Specification** pop-up closes and the Boolean expression for your qualifier appears in the field for which you specified it.

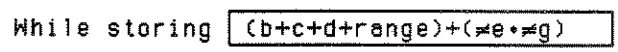


Figure 15-7. Boolean Expression for Qualifier

Sequence Levels

There are eight trigger sequence levels available in the state analyzer. You can add and delete levels so that you have from two to eight levels at a time.

Only three levels appear in the Sequence Levels display at one time. To display other levels so that they can be accessed, press the up/down ROLL key and rotate the KNOB.

If you select level 1 shown in figure 15-1, you will see the following pop-up menu:

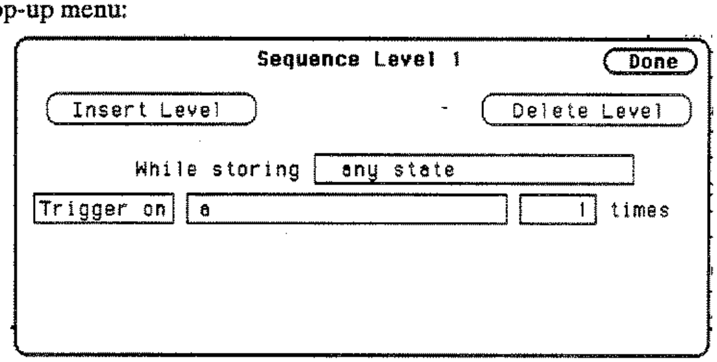


Figure 15-8. Sequence Level Pop-Up Menu

Not all sequence level pop-up menus look like this one. This happens to be the trigger sequence level in which you specify the state on which the analyzer is to trigger. The trigger term can occur in any of the first seven levels, and it is not necessarily a selectable field. The fields in the menu of figure 15-8 are described on the following pages.

Insert Level

To insert a level, place the cursor on the field labeled **Insert Level** and press SELECT. You will see the following pop-up menu.

Cancel
Before
After

Figure 15-9. Insert Level Pop-Up Menu

Cancel returns you to the sequence level pop-up without inserting a level. **Before** inserts a level before the present level. **After** inserts a level after the present level. If there are eight levels, the **Insert Level** field doesn't appear in the sequence level pop-ups.

Delete Level

If you want to delete the present level, select the field labeled **Delete Level**. You will see a pop-up menu with the choices Cancel and **Execute**. **Cancel** returns you to the sequence level pop-up without deleting the level. **Execute** deletes the present level and returns you to the State Trace Specification menu.

Note

If there are only two levels, neither field can be deleted even though the Delete Level field still appears in the menu. There will always be a trigger term level and a store term level in Sequence Levels. Therefore, if you try to delete either of these, all terms you have specified in these levels will be set to default terms, and, the trigger and store term levels will remain.

Storage Qualifier

Each sequence level has a storage qualifier. The storage qualifier specifies the states that are to be stored and displayed in the **State Listing**. Selecting this field gives you the qualifier pop-up menu shown in figure 15-2, with which you specify the qualifier.

As an example, suppose you specify the storage qualifier in a sequence level as shown below.

```
While storing [a+d                    ]
```

Figure 15-10. Storage Qualifier Example

The only states that will be stored and displayed are the states given by pattern recognizers a and d.

Branching Qualifier

Every sequence level except the last has a primary branching qualifier. With the branching qualifier, you tell the analyzer to look for a specific state or states. The primary branching qualifier advances the sequencer to the next level if its qualifier is satisfied.

In the example of figure 15-8, the branching qualifier tells the analyzer when to trigger. In other sequence levels, the qualifier may simply specify a state that the analyzer is to look for before continuing to the next level.

Some sequence levels also have a secondary branching qualifier. The secondary branch will, if satisfied, route the sequencer to a level that you define. This is covered in more detail in "Branches" later in this chapter.

Occurrence Counter

The primary branching qualifier has an occurrence counter. With the occurrence counter field you specify the number of times the branching qualifier is to occur before moving to the next level.

To change the value of the occurrence counter, position the cursor on the field and either press SELECT or press a numeric key on the front-panel keypad. You will see a pop-up similar to that shown below.

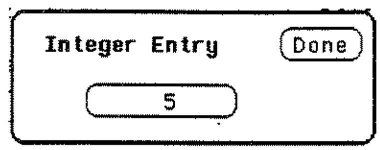


Figure 15-11. Occurrence Counter Pop-Up Menu

You can change the value by either rotating the KNOB or pressing the appropriate numeric keys. The qualifier can be specified to occur from one to 65535 times.

Storage Macro

Your logic analyzer has the capability of post-trigger storage through a storage macro. The storage macro is available only in the second to last level, and it consumes both that level and the last level. The field in figure 15-8 allows you to configure the state analyzer for post-trigger storage. This field does not always say Trigger on. If the sequence level is not a trigger level, the field will say Then find, as shown below.

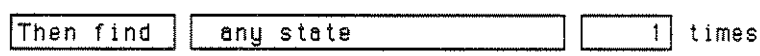


Figure 15-12. Then Find Branching Qualifier

Selecting the field gives you a pop-up with two options. One option is what the field said previously. The other option is Enable on. If you select this option, the Sequence Level pop-up changes to look similar to that shown below.

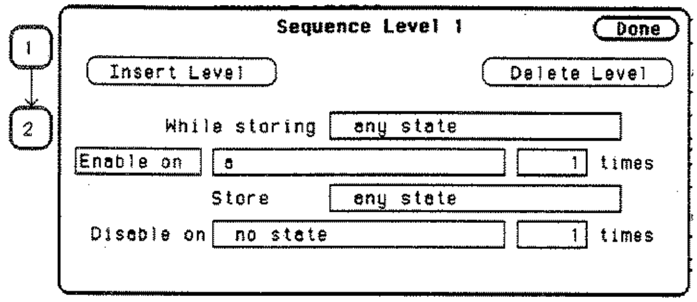


Figure 15-13. Storage Macro Sequence Level Example

Note

Enable on can only be the next to last term, and when on, the last term is combined with the Enable term.

You specify qualifiers for the states on which you want the macro to enable, the states you want to store, and the states on which you want the macro to disable. The storage macro is a loop that keeps repeating itself until memory is full. The loop is repeated when the disable qualifier is satisfied. As an example, suppose you configure the sequence level of figure 15-13 to look like that shown below.

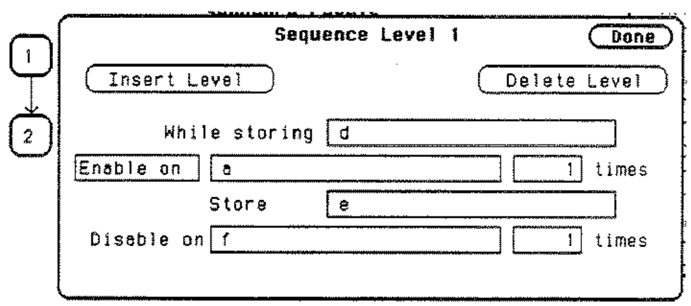


Figure 15-14. Sequence Level Pop-up with Storage Macro

The logic analyzer will store the state given by pattern recognizer **d** until it comes across the state given by **a**. When it sees state **a**, the logic analyzer starts to store the state given by pattern recognizer **e**. It stores that state until it sees the state given by **f**, at which time it disables and starts the process all over again. The analyzer repeats this process until its memory is full.

Reading the Sequence Level Display

Reading the display is fairly straightforward. For example, suppose your display looks like that shown below.

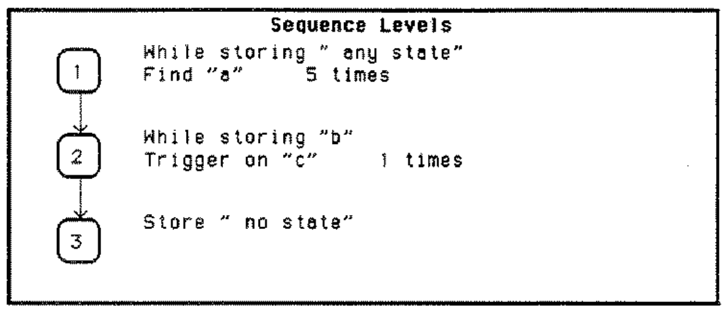


Figure 15-15. Sequence Level Display Example

In level 1 anystate is stored while the logic analyzer searches for five occurrences of the pattern given by pattern recognizer a. When the five occurrences are found, the sequencer moves on to level 2. In level 2 the state given by pattern recognizer b is stored until one occurrence of the pattern given by pattern recognizer c is found and the logic analyzer triggers. In level 3 nostate is stored, so the last state stored is the trigger state.

An example of a state listing for the previous State Trace configuration is shown below. The state patterns specified are:

a = B03C
b = 0000
c = 8930

```
MACHINE 2     -    STATE LISTING

Label    >  A
Base     >   Hex

 -0028       4E75
 -0027       61E6
 -0026       0000
 -0025       88C8
 -0024       B03C
 -0023       00FF
 -0022       6730
 -0021       48E7
 -0020       4E75
 -0019       3000
 -0018       0000
 -0017       8930
 -0016       B03C
 -0015       00FF
 -0014       67F8
 -0013       B03C
 -0012       61FA
 -0011       B03C
 -0010       0000
 -0009       8930
 -0008       4EFA
 -0007       FF9A
 -0006       61E6
 -0005       B03C
 -0004       0000
 -0003       0000
 -0002       0000
 -0001       0000
 +0000       8930
```

Figure 15-16. State Listing Example

Anystate was stored while the analyzer looked for five occurrences of the state B03C. After the fifth occurrence was found, only state 0000 was stored until state 8930 was found, and the analyzer triggered. After the trigger, no states were stored.

Acquisition Fields

The acquisition fields are comprised of the Trace mode, Armed by Branches, Count, and Prestore fields, as shown below.

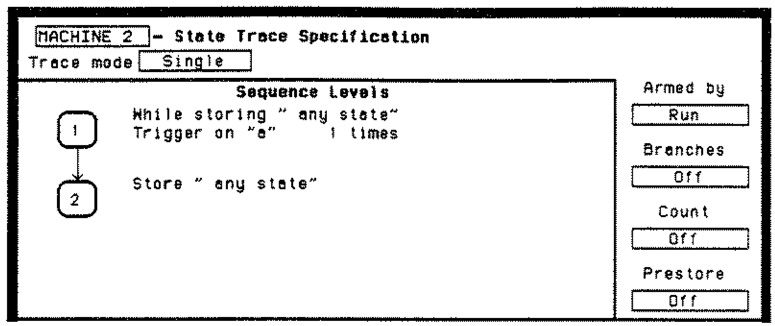


Figure 15-17. State Trace Acquisition Fields

Trace Mode

You specify the mode in which the state analyzer will trace with the Trace mode field. You have two choices for trace mode: Single and Repetitive. If you place the cursor on the field and press SELECT the field toggles from one mode to the other.

Single Trace mode acquires data once per trace. Repetitive Trace mode repeats single acquisitions until the STOP key on the front panel is pressed, or if Stop measurement is on, until conditions specified with the X and O markers in the State Listing menu are met.

If both analyzers are on, only one trace mode can be specified. Specifying one trace mode for one analyzer sets the same trace mode for the other analyzer.

Armed By

The Armed by field lets you specify how your state analyzer is to be armed. The analyzer can be armed by the RUN key, the other analyzer, or an external instrument through the BNC Input port. Any of these can tell the analyzer when to start capturing data.

When you select the Armed by field, a pop-up menu appears like that shown below. The first two options always appear in the pop-up. The third option will give the name of the other analyzer. If the other analyzer is off, or if the other machine is being armed by this machine, this option will not be available.

```
Armed by
Run
BNC Input
MACHINE 1
```

Figure 15-18. Armed By Pop-Up Menu

Branches

The Branches field allows you to configure the sequencer of the state analyzer to branch from one sequence level to another with secondary branching qualifiers, or to restart when a certain condition is met. Selecting this field gives you the following pop-up menu.

```
Branches
Off
Restart
Per level
```

Figure 15-19. Branches Pop-Up Menu

Off

If you select Off, all secondary branching qualifiers are deleted from the sequence levels. Only the primary branches remain.

Restart

The Restart option allows you to start over from sequence level 1 when a specified condition is met. This can be handy if you have code that branches off in several paths and you want the analyzer to follow one certain path. If the analyzer goes off on an undesired path, you would want the analyzer to stop and go back to the beginning and take the correct path.

If you select the Restart option, you will see a qualifier pop-up menu like that shown in figure 15-2. With the pop-up you select the qualifier for the pattern on which you want your analyzer to start over.

When your state analyzer is reading data it proceeds through the sequence. If a term doesn't match the branching qualifier, it is then checked against Restart. If the term matches, the state analyzer jumps back the sequence level 1.

Per Level

Selecting the Per level option allows you to define a secondary branching qualifier for each sequence level. A statement is added in each level so that you can configure the analyzer to move to a different level when a specified condition is met. An example of a sequence level with a secondary branching qualifier is shown in the figure below.

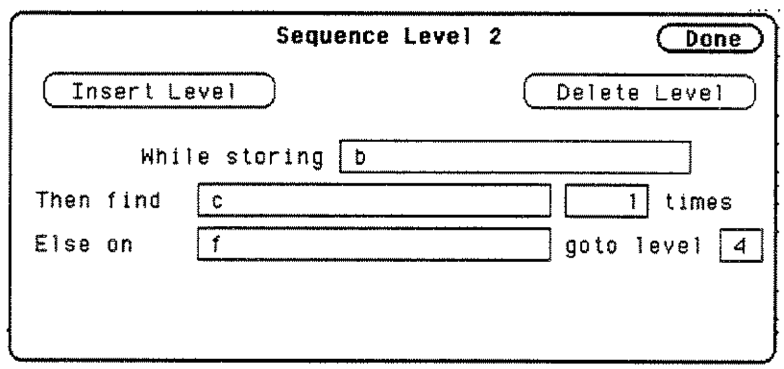


Figure 15-20. Secondary Branching Qualifier

With this configuration, the state analyzer will store b until it finds c. If it finds f before it finds c, it will branch to sequence level 4. If you have specified a storage macro in the next to last sequence level the Else on statement will not appear in that level since a secondary branching qualifier already exists for that level.

In the last sequence level, which only specifies states that are to be stored, the secondary branching qualifier statement looks like that shown below.

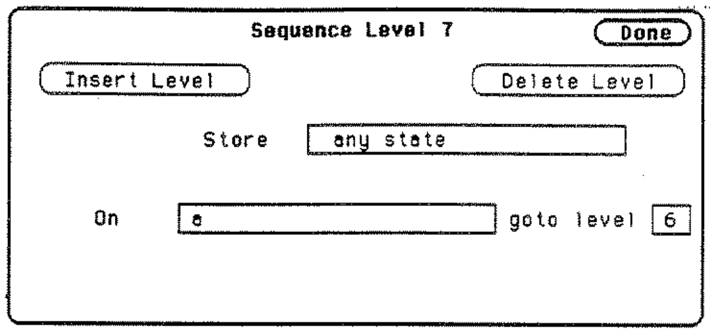


Figure 15-21. Secondary Branch Qualifier in Last Level

In this example, as the state analyzer stores anystate, it will branch to sequence level 6 if it finds the state given by qualifier e.

The trigger sequence level is used as a boundary for branching between levels. This level and the levels that occur before it cannot branch to levels that occur after the trigger level, and vice versa. Therefore, if there are eight sequence levels and level 5 is the trigger sequence level, then levels 1 through 5 can branch to levels 1 through 5 only, and levels 6 through 8 can branch to levels 6 through 8 only.

You can tell if secondary branch qualifiers have been specified by looking at the Sequence Levels display. Figure 15-22 shows how the display looks with the configuration that was given in figure 15-20. An arrow is drawn out of level 2, indicating that branching originates from that level, and an arrow is drawn to level 4 to indicate that a branch is going to that level.

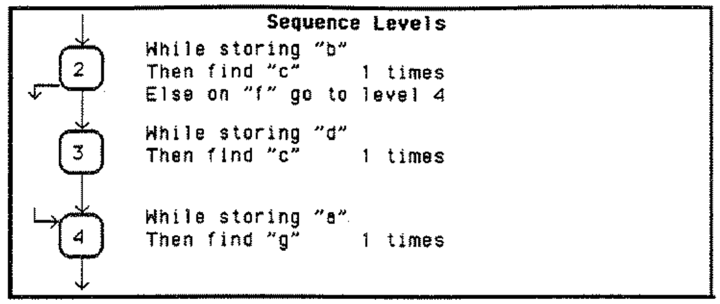


Figure 15-22. Branching Between Sequence Levels

Each sequence level can branch to only one level through a secondary branching qualifier. However, the number of times to which a level can be branched is limited only by the number of levels present. A level can have only one arrow pointing away from it, but it can have two pointing to it if more than one other level is branching to it. An example of this is shown in the figure below. The arrow with two tails indicates that a level above and a level below branch to this level.

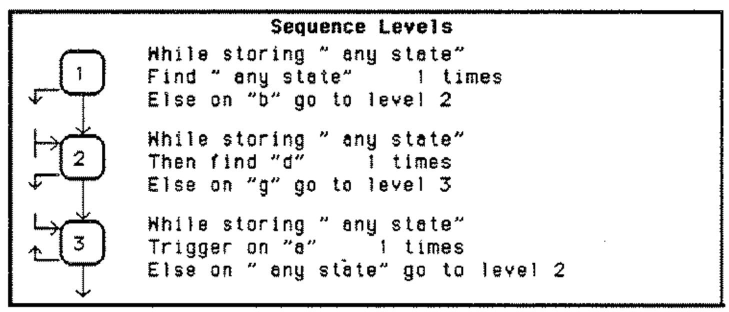


Figure 15-23. Multiple Branching Between Levels

Count

The Count field allows you to place tags on states so you can count them. Counting cuts the acquisition memory in half from 1k to 512 and the maximum clock rate is reduced to 16.67 MHz.

Note

Count (State Trace menu) is turned off when "Clock Period" is set to < 60 ns in the State Format Specification menu since the clock rate is greater than 16.67 MHz. If you select Count, the clock period automatically changes to > 60 ns.

Figure 15-24. Count Pop-Up Menu

Selecting this field gives you the following pop-up menu.

Off

If you select Off, the states are not counted in the next measurement.

Time

If you select Time counting, the time between stored states is measured and displayed (after the next run) in the State Listing under the label Time. The time displayed can be either relative to the previous state or to the trigger. The maximum time between states is 48 hours.

An example of a state listing with time tagging relative to the previous state is shown in figure 15-25.

68000STATE - State Listing

Markers Off

Label >	DATA	Time
Base >	Hex	Rel
-0007	00FF	1.24 us
-0006	6730	1.28 us
-0005	48E7	1.24 us
-0004	4E75	1.72 us
-0003	3000	1.28 us
-0002	0000	1.24 us
-0001	8930	1.24 us
+0000	803C	1.24 us
+0001	00FF	1.24 us
+0002	67F8	1.28 us
+0003	803C	1.24 us
+0004	61FA	1.72 us
+0005	803C	1.28 us
+0006	0000	1.96 us
+0007	8930	1.52 us
+0008	4EFA	1.24 us

Figure 15-25. Relative Time Tagging

An example of a state listing with time tagging relative to the trigger is shown below.

68000STATE - State Listing

Markers Off

Label >	DATA	Time
Base >	Hex	Abs
-0007	00FF	-9.24 us
-0006	6730	-7.96 us
-0005	48E7	-6.72 us
-0004	4E75	-5.00 us
-0003	3000	-3.72 us
-0002	0000	-2.48 us
-0001	8930	-1.24 us
+0000	803C	0 s
+0001	00FF	1.24 us
+0002	67F8	2.52 us
+0003	803C	3.76 us
+0004	61FA	5.48 us
+0005	803C	6.76 us
+0006	0000	8.72 us
+0007	8930	10.24 us
+0008	4EFA	11.48 us

Figure 15-26. Absolute Time Tagging

States

State tagging counts the number of qualified states between each stored state. If you select this option, you will see a qualifier pop-up menu like that shown in figure 15-2. You select the qualifier for the state that you want to count.

In the State Listing, the state count is displayed (after the next run) under the label States . The count can be relative to the previous stored state or to the trigger. The maximum count is 4.4 X 10E12.

An example of a state listing with state tagging relative to the previous state is shown below.

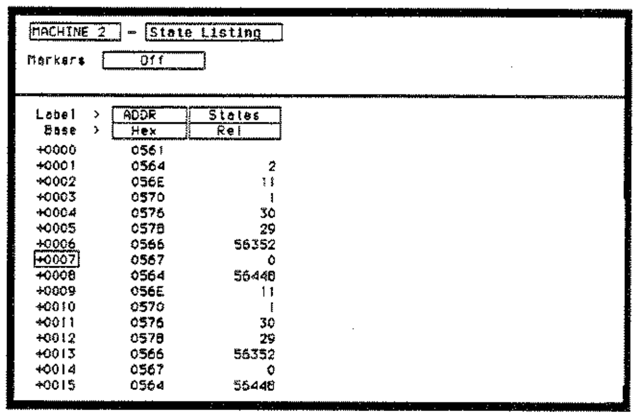


Figure 15-27. Relative State Tagging

An example of a state listing with state tagging relative to the trigger is shown below.

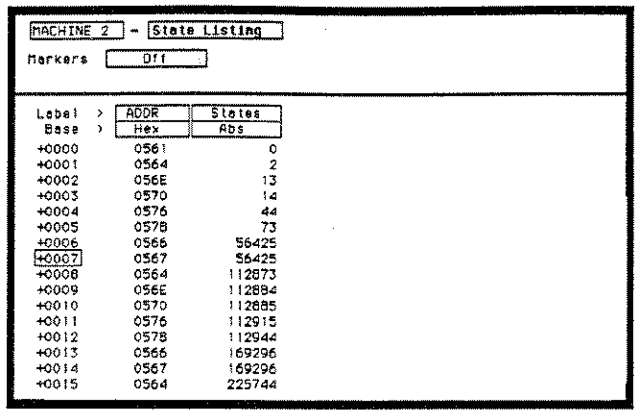


Figure 15-28. Absolute State Tagging

Prestore

Prestore allows you to store two qualified states before each state that is stored. There is only one qualifier that enables prestore for each sequence level. If you select this field, you will see a pop-up with the options **Off** and **On** . Selecting On gives you a qualifier pop-up menu like that in figure 15-2, from which you choose the pattern range or combination of patterns and ranges that you want to prestore.

Note

Prestore is only available when clock period is > 60 ns. If you select Prestore, the clock period automatically changes to > 60ns if it was previously set to < 60 ns.

During a measurement, the state analyzer stores in prestore memory occurrences of the states you specify for prestore. A maximum of two occurrences can be stored. If there are more than two occurrences previous ones are pushed out. When the analyzer finds a state that has been specified for storage, the prestore states are pushed on top of the stored state in memory and are displayed in the State Listing.

Qualifier and Pattern Fields

The qualifier and pattern fields appear at the bottom of the State Trace Specification menu. They allow you to specify patterns for the qualifiers that are used in the sequence levels.

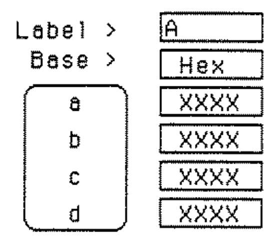


Figure 15-29. Qualifier and Pattern Fields

Label

The Label fields display the labels that you specified in the State Format Specification menu. The labels appear in the order that you specified them; however, you can change the order. Select one of the label fields and you will see a pop-up menu with all the labels. Decide which label you want to appear in the label field and select that label. The label that was there previously switches positions with the label you selected from the pop-up.

Base

The base fields allow you to specify the numeric base in which you want to define a pattern for a label. The base fields also let you use a symbol that was specified in the State Symbol Table for the pattern. Each label has its own base defined separately from the other labels. If you select one of the base fields, you will see the following pop-up menu. Decide which base you want to define your pattern in and select that option.

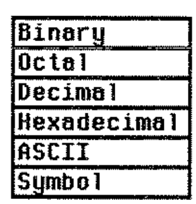


Figure 15-30. Numeric Base Pop-Up Menu

One of the options in the Base pop-up is ASCII . It allows you to see the ASCII characters that are represented by the pattern you specify in the pattern fields.

Note

You cannot define ASCII characters directly. You must first define the pattern in one of the other numeric bases; then you can switch the base to ASCII to see the ASCII characters.

The Symbol option in the Base pop-up allows you to use a symbol that has been specified in the State Symbol Tables as a pattern. In the pattern fields you specify the symbols you want to use.

Qualifier Field

If you select the qualifier field, you will see the following pop-up menu.

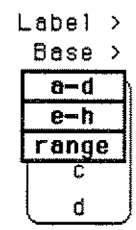


Figure 15-31. Qualifier Field Pop-Up Menu

Patterns

The pattern recognizers are in two groups of four: a-d and e-h. If you select one of these two options, the qualifier field will contain only those pattern recognizers. For instance, the qualifier field in figure 15-29 contains only the recognizers a-d.

Ranges

If you select the range option, the qualifier and pattern fields look similar to that shown below.

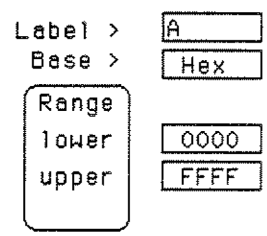


Figure 15-32. Range Qualifier and Pattern Fields

Only one range can be defined, and it can be defined over only one label, hence over only 32 channels. The channels don't have to be adjacent to each other. The logic analyzer selects the label over which the range will be defined by looking at the labels in order and choosing the first one that has channels assigned under only two pods. A label that contains channels from more than two pods cannot be selected for range definition. If all the labels have channels assigned under more than two pods, the range option is not offered in the qualifier field pop-up menu. However, in the HP 1651B, the range option will always be offered since the analyzer has only two pods.

Pattern Fields

The pattern fields allow you to specify the states that you want the state analyzer to search for and store. Each label has its own pattern field that you use to specify a pattern for that label (if you are defining a pattern for a pattern recognizer).

During a run, the state analyzer looks for a specified pattern in the data. When it finds the pattern, it either stores the state or states or it triggers, depending on the step that the sequencer is on.

16

State Listing Menu

Introduction

This chapter describes the State Listing menus and how to interpret it. It also tells you how to use the fields to manipulate the displayed data so you can find your measurement answers. The State Listing menu is the display menu of the state analyzer.

There are two different areas of the state listing display, the menu area and the listing area. The menu area is in the top one-fourth of the screen and the listing area is the bottom three-fourths of the screen.

The listing area displays the data that the state analyzer acquires. The data is displayed in a listing format as shown below.

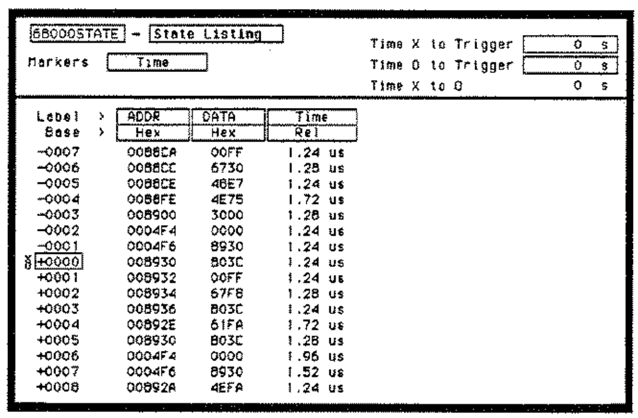


Figure 16-1. State Listing Menu

This listing display shows you 16 of the possible 1024 lines of data at one time. You can use the ROLL keys and the KNOB to roll the listing to the lines of interest.

The column of numbers at the far left represents the location of the acquired data in the state analyzer's memory. The trigger state is always 0000. At the vertical center of this column you will see a box containing a number. The box is used to quickly select another location in the state listing. The rest of the columns (except the Time/States column) represent the data acquired by the state analyzer. The data is grouped by label and displayed in the number base you have selected (hexadecimal is the default base).

When the Time or States option is selected in the Count field (State Trace Specification Menu), the acquired data will be displayed with time or state tags.

The Time column displays either the Rel(ative) time (time from one state to the next) or Abs(olute) time (time from each state to the trigger).

The States column displays the number of qualified states Rel(ative) to the previously stored state or the trigger (absolute).

Accessing the State Listing Menu

The State Listing Menu is accessed by pressing the DISPLAY key on the front panel when the state analyzer is on. It will automatically be displayed when you press RUN. If the Timing Waveforms is displayed when you press the DISPLAY key, you will have to switch analyzers. This is not a problem, it merely indicates that you were in the timing analyzer or you had performed an action to the timing analyzer in the System Configuration Menu.

State Listing Menu Fields

The menu area contains fields that allow you to change the display parameters, place markers, and display listing measurement parameters.

Figure 16-2. State Listing Menu Fields

Markers

The Markers field allows you to specify how the X and O markers will be positioned on the state listing. The State Trace Specifications menu options are:

If Count in the State Trace menu is Off the marker options are:

- Off
- Pattern

If Count in the State Trace menu is set to Time the marker options are:

- Off
- Pattern
- Time
- Statistics

If Count in the State Trace menu is set to State the marker options are:

- Off
- Pattern
- State

Markers Off

When the markers are off they are not displayed, but are still placed at the specified points in the data. If Stop measurement is on and the Stop measurement criteria are present in the data, the measurement will stop even though the markers are off.

Markers Patterns

When the markers are set to patterns, you can specify patterns on which the logic analyzer will place the markers. You can also specify how many occurrences of each marker pattern the logic analyzer looks for. This use of the markers allows you to find a specific pattern for each label in the acquired data.

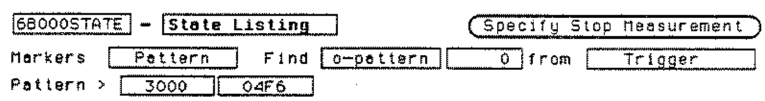


Figure 16-3. Markers Set to Patterns

Patterns for each marker (X and O) can be specified. They can be specified for both markers in each label. The logic analyzer searches for the logical "and" of patterns in all labels.

In the Find X (O)-pattern 0 from Trigger field you specify how many occurrences of the marked pattern from a reference point you want the logic analyzer to search for. The reference points are:

- Trigger
- Start (of a trace)
- X Marker (only available in O marker pattern specification)

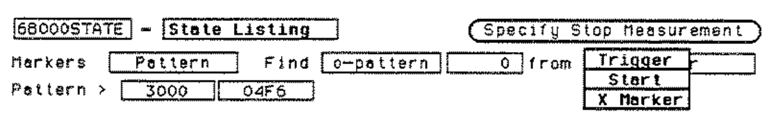


Figure 16-4. Search Reference Pop-Up Menu

Stop Measurement. Another feature of markers set to patterns is Stop Measurement. You can specify either stop measurement when **X-O is _____** or **Compare is ____.** The options for X-O are: Less than, Greater than, In range, Not in range. The options for Compare are: Equal and Not Equal (see figure 16-5).

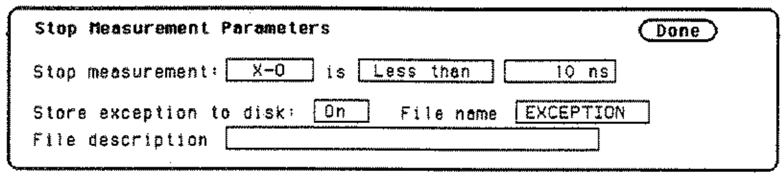


Figure 16-5. Markers Patterns Pop-Up Menu

With this feature you can use the logic analyzer to look for a specified time or range of time between the marked patterns and to stop acquiring data when it finds this time between markers. The X marker must precede the O marker.

Also available is **Store exception to disk** which allows you to specify a file on the disk that exceptions can be stored in. The default filename is EXCEPTION. When the trace mode is repetitive and Store exception to disk is on, the following process takes place: data is acquired until the stop criteria is met, data acquisition will stop, data in the acquisition memory will be stored on the disk, and data acquisition will resume when the data is stored. This process continues until the disk is full. The data is stored in the same file name; however, the last three characters will automatically be replaced with a numerical serial number. For example, EXCEPTION will change to EXCEPT001 the second time memory is stored.

Note

The upper and lower range boundaries must not be the same value. For example, if you want to stop a measurement when the X and O markers are in range of 200 ns, you should set the range values to 190 ns and 210 ns. This eliminates erroneous measurement termination.

Markers Time

When the markers are set to Time, you can place the markers on states in the listing of interest and the logic analyzer will tell you:

- Time X to Trig(ger)
- Time O to Trig(ger)
- Time X to O

To position the markers, move the cursor to the field of the marker you wish to position and press SELECT. A pop-up will appear showing the current time for that marker. Either rotate the KNOB or enter a numeric value from the keypad to change the position of that marker. Pressing SELECT when you are finished positions the marker and closes the pop-up.

Figure 16-6. Markers Set to Time

The Time X to O field will change according to the position of the X and O markers. It displays the total time between the states marked by the X and O markers.

Markers Statistics

When statistics are specified for markers, the logic analyzer will display the:

- Number of total runs
- Number of valid runs (runs where markers were able to be placed on specified patterns)
- Minimum time between the X and O markers * Maximum time between the X and O markers
- Average time between the X and O markers

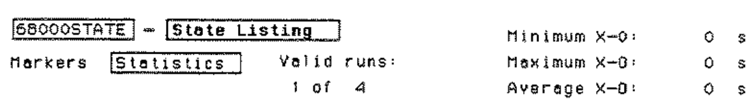


Figure 16-7. Markers Set to Statistics

How the statistics will be updated depends on the state trace mode (repetitive or single).

In repetitive, statistics will be updated each time a valid run occurs until you press STOP. When you press RUN after STOP, the statistics will be cleared and will restart from zero.

In single, each time you press RUN an additional valid run will be added to the data and the statistics will be updated. This will continue unless you change the placement of the X and O markers between runs.

Pattern ___ Field

You use the Pattern ___ field to specify the patterns for the X and O markers for each label.

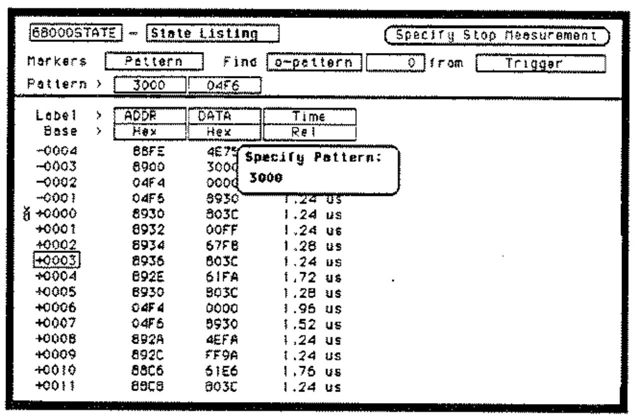


Figure 16-8. Pattern ________ Field Pop-Up Menu

When x-pattern is specified in the Find ___ from __ field, the pop-ups in the Pattern ____ field allow you to specify a pattern for the X marker in each label.

When the O-pattern is specified, the pop-ups in the Pattern _____ field allow you to specify the patterns for the O marker in each label.

17

State Compare Menu

Introduction

State compare is a software post-processing feature that provides the ability to do a bit by bit comparison between the acquired state data listing and a compare data image. You can view the acquired data and the compare image separately. In addition, there is a separate difference listing that highlights the bits in the acquired data that do not match the corresponding bits in the compare image. Each state machine has its own Compare and Difference listings.

You can use the editing capabilities to modify the compare image. Masking capabilities are provided for you to specify the bits that you do not want to compare. "Don't compare" bits can be specified individually for a given label and state row, or specified by channel across all state rows. A range of states can be selected for a comparison. When a range is selected, only the bits in states on or between the specified boundaries are compared.

The comparison between the acquired state listing data and the compare image data is done relative to the trigger points. This means that the two data records are aligned at the trigger points and then compared bit by bit. Any bits in the acquired data that do not match the bits in the compare image are treated as unequal. The don't compare bits in the compare image are ignored for the comparison.

When a logic analyzer configuration is saved to or loaded from a disk, any valid compare data including the data image, etc. is also saved or loaded.

Accessing the Compare Menu

The Compare menu is accessed from the State Listing menu. To access the Compare menu place the cursor on the field **State Listing** and press SELECT. A pop-up appears with the following options:

- State Listing
- State Waveforms
- State Chart
- State Compare

Place the cursor on **State Compare** and press SELECT. The pop-up will close and display the State Compare menu.

The Compare and Difference Listing Displays

Two menus (or displays) in addition to the normal State Listing, are available for making comparison measurements: the Compare Listing and the Difference Listing.

The Compare Listing

The Compare Listing contains the image (or template) that acquired data is compared to during a comparison measurement. The boundaries of the image (or size of the template) can be controlled by using the channel masking and compare range functions described below. Any bits inside the image displayed as "X" have been set to don't compare bits.

The Difference Listing

The Difference Listing highlights the entire row with inverse video, if any differences exist, in the acquired data that differs from those in the compare image. In addition, when the base is hexadecimal, octal, or binary, the bit (or digit containing the bit) that differs from the compare image is underlined (see figures 17-2 and 17-3). If the base is inverse assembled symbols, the display does not change; however, the stop measurement functions still function.

To display the Compare Listing or the Difference Listing, place the cursor on the field directly to the right of **Show** in the upper left part of the display and press SELECT. The field will toggle between **Compare Listing** and **Difference Listing.**

The controls that roll the listing in all three menus, the normal State Listing, the Compare Listing, and the Difference Listing are synchronized unless the number of pre-trigger states differ between the Compare listing and the acquired data. This means that when you change the current row position in the Difference Listing, the logic analyzer automatically updates the current row in the acquired State Listing, Compare Listing and vice-versa.

If the three listings are synchronized and you re-acquire data, the Compare Listing may have a different number of pre-trigger states depending on the state trace trigger criteria. The Compare Listing can be resynchronized to the State and Difference Listings (if different) by entering the desired state (acquisition memory) location from the front-panel keypad.

This allows you to view corresponding areas of the two lists, to cross check the alignment, and analyze the bits that do not match.

Since time tags are not required to perform the compare, they do not appear in either the compare image or difference displays. However, correlation is possible since the displays are locked together.

To move between the State Listing and Compare Listing in the HP 1650B/51B, select the field directly to the right of **Show** in the upper left part of the screen and press SELECT. This field toggles between Compare Listing and Difference Listing.

Creating a Compare Image

An initial compare image can be generated by copying acquired data into the compare image buffer. When you place the cursor on the **Copy Trace to Compare** field in the Compare Listing menu a pop-up appears with the options **Cancel** and **Continue.** If the **Continue** is selected, the contents of the acquisition data structure for the current machine are copied to the compare image buffer. The previous compare image is lost if it has not been saved to a disk. If you select **Cancel** the current compare image remains unchanged.

Bit Editing of the Compare Image

Bit editing allows you to modify the values of individual bits in the compare image or specify them as don't compare bits. The bit editing fields are located in the center of the Compare Listing display to the right of the listing number field (see figure 17-1). A bit editing field exists for every label in the display unless the label's base is ASCII or inverse assembled symbols. You can access any data in the Compare Listing by rolling the desired row vertically until it is located in the bit editing field for that label (column).

When you select one of the bit editing fields a pop-up appears in which you enter your desired pattern or don't compare for each bit.

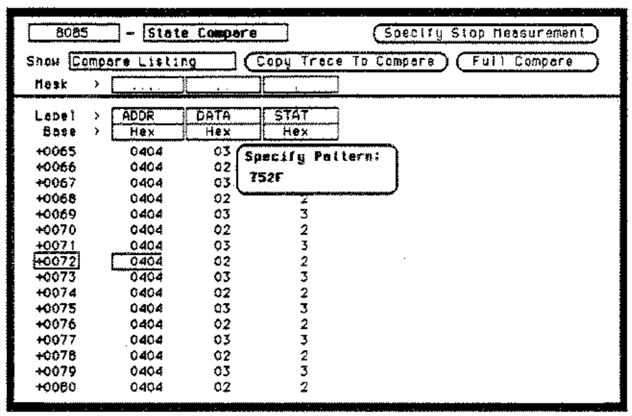


Figure 17-1. Bit Editing Fields

Masking Channels in the Compare Image

The channel masking function allows you to specify a bit, or bits in each label that you do not want compared. This causes the corresponding bits in all states to be ignored in the comparison. The compare data image itself remains unchanged on the display. The Mask fields are directly above the label and base fields at the top of both the Compare and Difference listings (see figure17-2). When you select one of these fields a pop-up appears in which you specify which channels are to be compared and which channels are to be masked. A "." (period) indicates a don't compare mask for that channel and an "*" (asterisk) indicates that channel is to be compared.

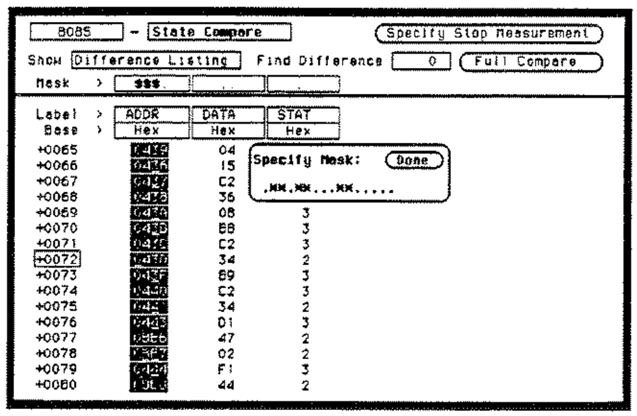


Figure 17-2. Bit Masking Fields

Specifying a Compare Range

The Compare Range function allows you to define a subset of the total number of states in the compare image to be used in the comparison. The range is specified by setting start and stop boundaries. Only bits in states (lines) on or between the boundaries are compared against the acquired data.

The Compare mode is accessed by selecting the **Full Compare/Partial Compare** field in either the Compare or Difference listing menus. When selected, a pop-up appears in which you select either the **Full** or **Partial** option. When you select the Partial option, fields for setting the start state and stop state values appear (see figure 17-3).

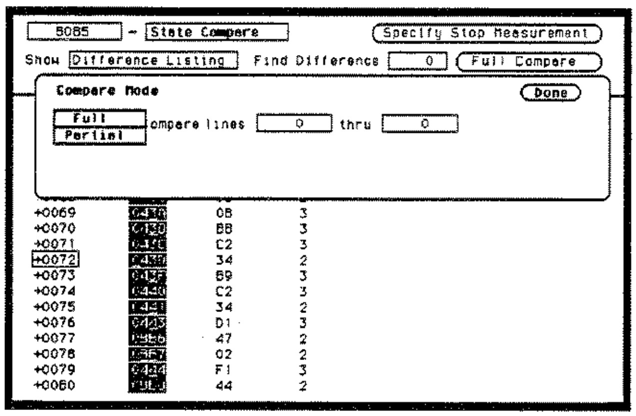


Figure 17-3. Compare Full/Compare Partial Field

Repetitive Comparisons with a Stop Condition

When you do a comparison in the repetitive trace mode, a stop condition may be specified. The stop condition is either **Stop Measurement** when Compare is **Equal** or **Not Equal.** In the case of Equal, bits in the compare image must match the corresponding bits in the acquired data image for the stop condition to be a true. In the case of Not Equal, a mismatch on a single bit will cause the stop condition to be true. When stop conditions are specified in two analyzers, both analyzers stop when the stop condition of either analyzer is satisfied. It is an OR function.

You access the stop measurement function by selecting the **Specify Stop Measurement** field in either the Compare or Difference Listing menus. When you select this field, the Stop Measurement Parameters pop-up appears (see figure 17-4). The first field in this pop-up, just to the right of Stop measurement contains either **Off**, **X-O** or **Compare.**

When this field is selected, a pop-up appears in which you select **Compare.** When you select the Compare option, you can access and select either the **Equal** or **Not Equal** option in the next field to the right.

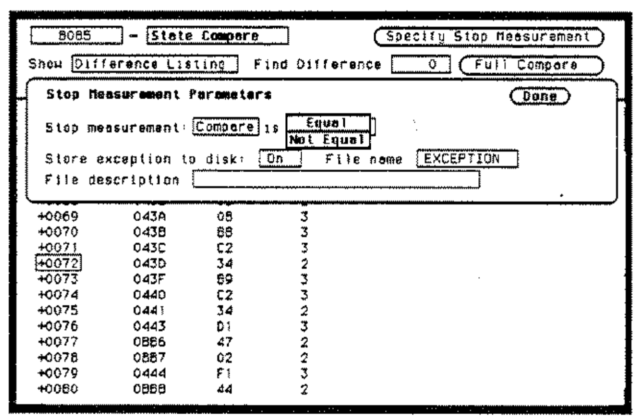


Figure 17-4. Specify Stop Measurement Field

Also available is **Store exception to disk** which allows you to specify a file on the disk that exceptions can be stored in. The default filename is EXCEPTION.

When the trace mode is repetitive and Store exception to disk is on, the following process takes place: data is acquired until the stop criteria is met, data acquistion will stop, data in the acquisition memory will be stored on the disk, and data acquisition will resume when the data is stored. This process continues until the disk is full. The data is stored in the same file name; however, the last three characters will automatically be replaced with a numerical serial number. For example, EXCEPTION will change to EXCEPT001 the second time memory is stored.

Note

You may also specify a stop measurement based on time between the X and O markers in the Compare or Difference Listing menus. This is available only when **Count** is set to **Time** in the State Trace menu. If the Stop Measurement is set to run until Compare Equal or Compare Not Equal in the Compare or Difference Listings, the Stop Measurement on time X to O will change to run until Compare Equal or Compare Not Equal in the other state display menus (i.e. State Listing).

Locating Mismatches in the Difference Listing

The **Find Difference** feature allows you to easily locate any patterns that did not match in the last comparison. Occurrences of differences are found in numerical ascending order from the start of the listing. The first occurrence of an error has the numerical value of one.

This feature is controlled by the **Find Difference**____ field in the Difference Listing menu. When you select this field an Integer Entry pop-up appears in which you enter a number indicating which difference you want to find. The listing is then scanned sequentially until the specified occurrence is found and rolled into view.

Saving Compare Images

When you save a logic analyzer configuration to a disk, the compare images for both state analyzers are saved with it. The compare data is compacted to conserve disk space. Likewise, when you load a configuration from disk, valid compare data will also be loaded.

18

State Chart Menu

Introduction

The State Chart Menu allows you to build X-Y plots of label activity using state data. The Y-axis always represents data values for a specified label. You can select whether the X-axis represents states (ie. rows in the State List) or the data values for another label. You can scale both the axes to selectively view data of interest. An accumulate mode is available that allows the chart display to build up over several runs. When **State** is selected for the X-axis, X & O markers are available which allows the current sample (state or time) relative to trace point to be displayed. Marker placement is synchronized with the normal State Listing.

Accessing the State Chart Menu

The Chart menu is accessed from the State Listing menu. To access the Chart menu place the cursor on the field **State Listing** and press SELECT. A pop-up appears with the following options:

- State Listing
- State Waveforms
- State Chart
- State Compare

Place the cursor on State Chart and press SELECT. The pop-up will close and display the State Chart menu.

Selecting the Axes for the Chart

When using the State Chart display, you should first select what data you want plotted on each axis. Assigning a label to the vertical axis of the chart is accomplished by positioning the cursor on the Y-axis **Label** field in the menu. When selected, a pop up appears in which you select one of the labels that were defined in the State Format Specification Menu. The X-axis assignment field, toggles between **State** and **Label** when selected. When label is selected, a third field appears to the right of **Label** that pops up when selected in which you select one of the defined state labels.

Scaling the Axes

Either axis of the X - Y chart can be scaled by using the associated vertical or horizontal **min** (minimum) or **max** (maximum) value fields. When selected, a **Specify Number** pop up appears in which you specify the actual minimum and maximum values that will be displayed on the chart.

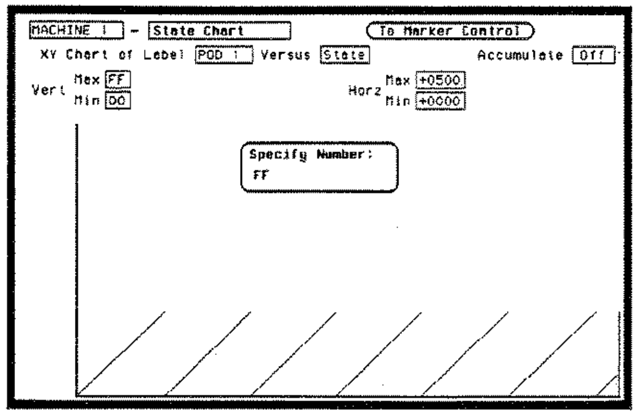


Figure 18-1. Axis Scaling Pop-up Menu

When **State** is selected for the X-axis, state acquisition memory locations are plotted on the X-axis. The minimum and maximum values can range from -1023 to + 1023 depending on the trace point location. The minimum and maximum values for labels can range from 00000000H to FFFFFFFFH (0 to 2^{32-1}) regardless of axis, since labels are restricted to 32 bits.

The Label Value vs. States Chart

The Label Value versus State chart is a plot of label activity versus the memory location in which the label data is stored. The label value is plotted against successive analyzer memory locations. For example, in the following figure, label activity of POD 1 is plotted on the Y axis and the memory locations (State) are plotted on the X axis.

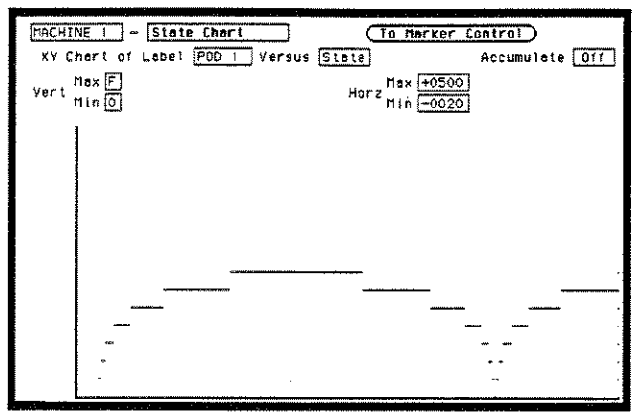


Figure 18-2. Label vs. State Chart

The Label Value vs. Label Value Chart

When labels are assigned to both axis, the chart shows how one label varies in relation to the other for a particular state trace record. Label values are always plotted in ascending order from the bottom to the top of the chart and in ascending order from left to right across the chart. Plotting a label against itself will result in a diagonal line from the lower left to upper right corner. X & O markers are disabled when operating in this mode.

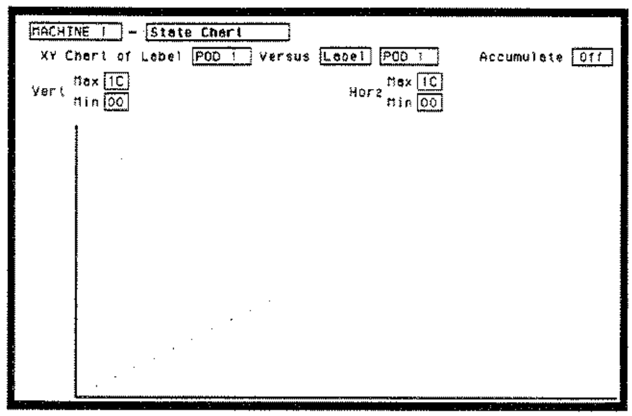


Figure 18-3. Label vs. Label Chart

X & O Markers and Readouts for Chart

When **State** is specified for the X-axis, X & O markers are available which can be moved horizontally. The markers are synchronized with the X and O markers in the normal State Listing.

To select the marker mode for Chart (if it is not presently displayed), place the cursor on the **To Marker Control** field and press SELECT. This field will toggle to **To Range Control** and the marker fields will be displayed (see figure 18-4).

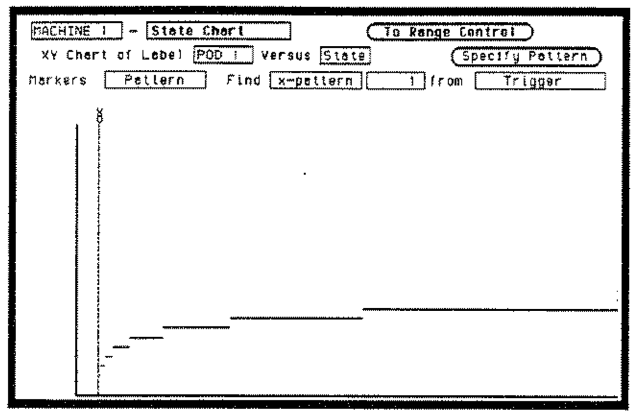


Figure 18-4. Marker Fields

When a marker is positioned in the State Chart menu, it is also positioned in the State Listing menu and vice-versa. The Chart marker operation is identical to the markers in the State Listing menu (see chapter 16).

Marker Options

The marker options in the State Chart menu depend on what **Count** is set to in the State Listing menu.

When Count is set to **Off** the Chart markers can be set to:

- Off
- Pattern

When Count is set to **Time** the Chart markers can be set to:

- Off
- Pattern
- Time
- Statistics

When Count is set to **States** the Chart markers can be set to:

- Pattern
- States

19

State Waveforms Menu

Introduction

The State Waveforms Menu allows you to view state data in the form of waveforms identified by label name and bit number. Up to 24 waveforms can be displayed simultaneously. Only state data from the current state machine can be displayed as waveforms in the State Waveforms menu.

The presentation and user interface is generally the same as the Timing Waveform menu, except the X-axis of the state waveform display represents only samples, or states instead of time (seconds). This is true regardless of whether **Count** (in the State Trace menu) is set to **Time** or **Off**. As a result, the horizontal axis of the display is scaled by States/Div and Delay in terms of samples from trigger. Marker features are the same as for State List in that Time or States will only be available when **Count** is set to **Time** or **States**. The Sample Rate display is not available in State Waveform even when markers are off.

Accessing the State Waveforms Menu

The State Waveforms menu is accessed from the State Listing menu. To access the State Waveforms menu place the cursor on the State Listing field and press SELECT. A pop-up appears with the following options:

- State Listing
- State Waveforms
- State Chart
- State Compare

Place the cursor on State Waveforms and press SELECT. The pop-up will close and display the State Waveforms menu.

Selecting a Waveform

You can display up to 24 waveforms on screen at one time. Each waveform is a representation of a predefined label. To select a waveform, place the cursor on a label name on the left side of the display and press SELECT. A pop-up appears in which you:

- Insert waveforms
- Turn on waveforms
- Modify waveforms (waveform labels)
- Turn off waveforms
- Delete waveforms

Just to the right of each label name is a two-digit number or the word "all." The number indicates which bit of the label the waveform represents; or, all the bits of the label when "all" is displayed (see figure 19-1).

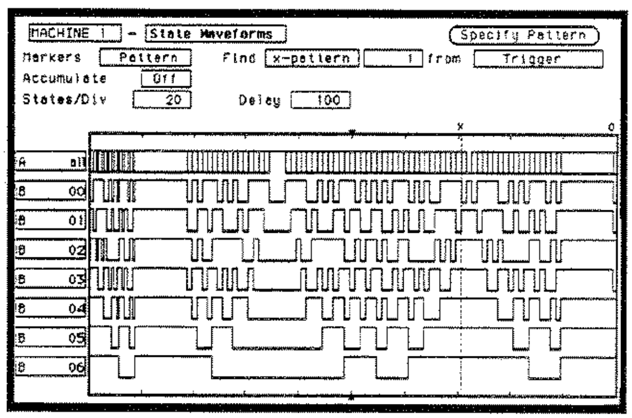


Figure 19-1. State Waveforms Menu

In the above figure, label A has "all" specified displaying all the bits overlaid in a single waveform. Label B however, has seven of its bits displayed individually (bits 0 through 6).

Replacing Waveforms

You can replace a currently displayed waveform (label) with another one of the predefined waveforms (labels). To replace one waveform with another, place the cursor on the waveform you wish to replace and press SELECT. A pop-up appears in which you select **Modify Waveform** as shown in the following figure.

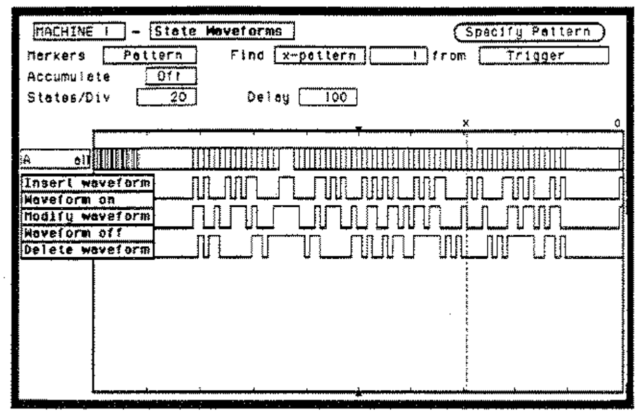


Figure 19-2. Waveform Selection Pop-up Menu

Another pop-up appears in which you select the waveform (label) you wish to display (see figure 19-3). When you place the cursor on the new waveform (label) and press SELECT the new waveform replaces the old waveform.

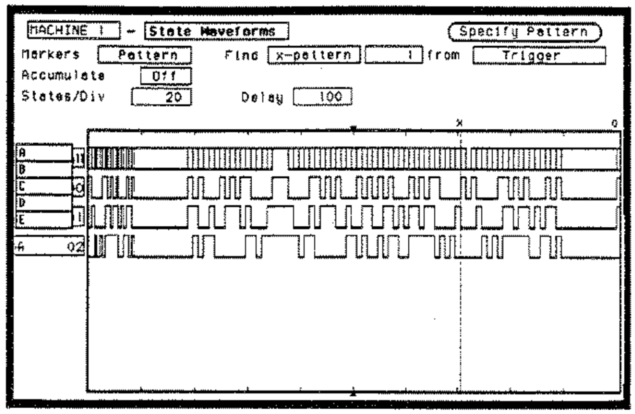


Figure 19-3. Available Waveforms Pop-up Menu

Deleting Waveforms

You can delete any of the currently displayed waveforms by placing the cursor on the waveform you wish to delete and pressing SELECT. When the pop-up appears place the cursor on **Delete waveform** and press SELECT.

Selecting States per Division

You can specify the states per division by placing the cursor on the field just to the right of **States/Div**, pressing SELECT, and either entering the number of states per division with the keypad or the knob. The range is from 1 to 1024 per division.

Delay from Trigger

You can specify the delay from trigger by specifying the number of states from the trigger. The delay will affect only the position of the State Waveforms display. It does not affect data acquisition. The minimum is − 1024 and the maximum is 1024 independent of trace position in the record. Delay is not limited to the window containing data.

State Waveform Display Features

The waveform display features of the State Waveform menu are the same as the Timing Waveform menu with regard to:

- low levels (below threshold) are represented by darker line
- dotted lines representing the X and O markers
- inverted triangle representing the trigger point
- Accumulate Mode
- graticule frame with 10 horizontal divisions

X and O Markers for State Waveform

Markers can be placed on the waveform display by specifying the number of states from trigger or start in the case of the X marker or number of states from either the trigger, start, or X marker in the case of the O marker.

Markers can be automatically placed on the waveform by searching for specific patterns assigned to each marker.

The X and O marker operation is identical to the marker operation in the Timing Waveform Menu (see chapter 11).

20

State Analyzer Measurement Example

Introduction

In this chapter you will learn how to use the state analyzer by setting up the logic analyzer to make a simple state measurement. We give you the measurement results as actually measured by the logic analyzer, since you may not have the same circuit available.

The exercise in this chapter is organized in a task format. The tasks are in the same order you will most likely use them once you become experienced. The steps in this format are both numbered and lettered. The numbered steps state the step objective. The lettered steps explain how to accomplish each step objective. There is also an example of each menu after it has been properly set up.

How you use the steps depends on how much you remember from chapters 1 through 4 of the *Getting Started Guide*. If you can set up each menu by just looking at the menu picture, go ahead and do so. If you need a reminder of what steps to perform, follow the numbered steps. If you still need more information about "how," use the lettered steps.

When you have finished configuring the logic analyzer for this exercise, you can load a file from the operating system disc. This file configures the logic analyzer the same way it is configured for this exercise. It also loads the same data acquired for this exercise so you can see what it looks like on screen.

In order to learn how to configure the logic analyzer, we recommend that you follow the exercise to "Acquiring the Data" before loading the file from the disc.

You can also compare your configuration with the one on the disc by printing it (if you have a printer) or making notes before you load the file.

Problem Solving with the State Analyzer

In this example assume you have designed a microprocessor controlled circuit. You have completed the hardware, and the software designer has completed the software and programmed the ROM (read-only memory). When you turn your circuit on for the first time, your circuit doesn't work properly. You have checked the power supply voltages and the system clock and they are working properly.

Since the circuit has never worked before, you and the software engineer aren't sure if it is a hardware or software problem. You need to do some testing to find a solution.

What Am I Going to Measure?

You decide to start where the microprocessor starts when power is applied. We will describe a 68000 microprocessor; however, every processor has similar start-up routines.

When you power up a 68000 microprocessor, it is held in reset for a specific length of time before it starts doing anything to stabilize the power supplies. The time the microprocessor is held in reset ensures stable levels (states) on all the devices and buses in your circuit. When this reset period has ended, the 68000 performs a specific routine called "fetching the reset vector."

The first thing you check is the time the microprocessor is held in reset. You find the time is correct. The next thing to check is whether the microprocessor fetches the reset vector properly.

The steps of the 68000 reset vector fetch are:

1. Set the stack pointer to a location you specify, which is in ROM at address locations 0 and 2.

2. Find the first address location in memory where the microprocessor fetches its first instruction. This is also specified by you and stored in ROM at address locations 4 and 6.

What you decide to find out is:

1. What ROM address does the microprocessor look at for the location of the stack pointer, and what is the stack pointer location stored in ROM?
2. What ROM address does the microprocessor look at for the address where its first instruction is stored in ROM, and is the instruction correct?
3. Does the microprocessor then go to the address where its first instruction is stored?
4. Is the executable instruction stored in the first instruction location correct?

Your measurement, then, requires verification of the sequential addresses the microprocessor looks at, and of the data in ROM at these addresses. If the reset vector fetch is correct (in this example) you will see the following list of numbers in HEX (default base) when your measurement results are displayed.

```
+ 0000  000000  0000
+ 0001  000002  04FC
+ 0002  000004  0000
+ 0003  000006  8048
+ 0004  008048  3E7C
```

This list of numbers will be explained in detail later in this chapter in "The State Listing."

How Do I Configure the Logic Analyzer?

In order to make this state measurement, you must configure the logic analyzer as a state analyzer. By following these steps you will configure Analyzer 1 as the state analyzer.

If you are in the System Configuration menu you are in the right place to get started and you can start with step 2; otherwise, start with step 1.

1. Using the field in the upper left corner of the display, get the System Configuration menu on screen.
   a. Place the cursor on the field in the upper left corner of the display and press SELECT.
   b. Place the cursor on System and press SELECT.
2. In the System Configuration menu, change the Analyzer 1 type to State. If Analyzer 1 is already a state analyzer, go on to step 3.
   a. Place the cursor on the Type: ____ and press SELECT.
   b. Place the cursor on State and press SELECT.

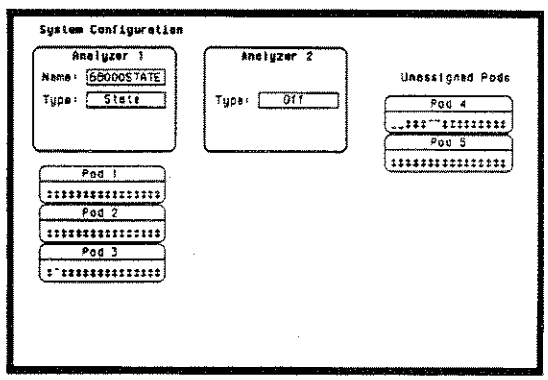


Figure 20-1. System Configuration Menu

3. Name Analyzer 1 68000STATE (optional).

   a. Place the cursor on the Name: ____ field of Analyzer 1 and press SELECT.

   b. With the Alpha Entry pop-up, change the name to 68000STATE.

4. Assign pods 1, 2, and 3 to the state analyzer.

   a. Place the cursor on the Pod 1 field and press SELECT.

   b. In the Pod 1 pop-up, place the cursor on Analyzer 1 and press SELECT.

   c. Repeat steps a and b for pods 2 and 3.

Connecting the Probes

At this point, if you had a target system with a 68000 microprocessor, you would connect the logic analyzer to your system. Since you will be assigning labels ADDR and DATA, you hook the probes to your system accordingly.

- Pod 1 probes 0 through 15 to the data bus lines D0 through D15.
- Pod 2 probes 0 through 15 to the address bus lines A0 through A15.
- Pod 3 probes 0 through 7 to the address bus lines A16 through A23.
- Pod 1, CLK (J clock) to the address strobe (LAS).

Activity Indicators

When the logic analyzer is connected and your target system is running, you will see ↕ in the Pod 1, 2, and 3 fields of the System Configuration menu. This indicates which signal lines are transitioning.

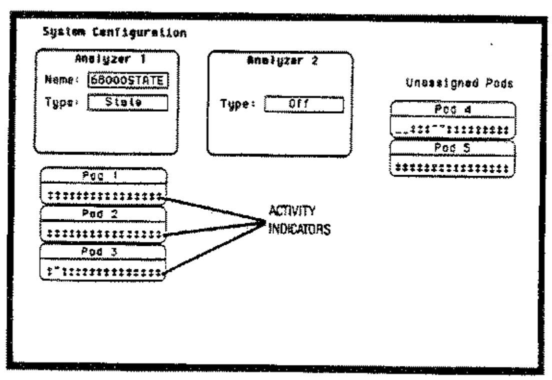


Figure 20-2. Activity Indicators

Configuring the State Analyzer

Now that you have configured the system, you are ready to configure the state analyzer. You will be:

- Creating two names (labels) for the input signals
- Assigning the channels connected to the input signals
- Specifying the State (J) clock
- Specifying a trigger condition

1. Display the STATE FORMAT SPECIFICATION menu.

a. Press the FORMAT key on the front panel.

2. Name two labels, one ADDR and one DATA.

a. Place the cursor on the top field in the label column and press SELECT.

b. Place the cursor on Modify label and press SELECT.

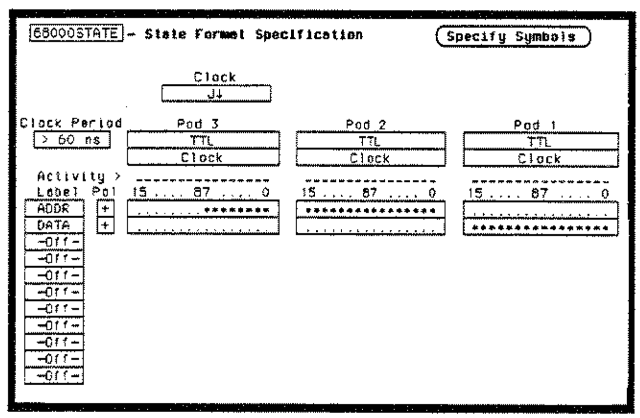


Figure 20-3. State Format Specification Menu

c. With the Alpha Entry pop-up, change the name of the label to ADDR.

d. Name the second label DATA by repeating steps a through c.

3. Assign Pod 1 bits 0 through 15 to the label DATA.

a. Place the cursor on the bit assignment field below Pod 1 and to the right of DATA and press SELECT.

b. Any combination of bits may already be assigned to this pod; however, you will want all 16 bits assigned to the DATA label. The easiest way to assign is to press the CLEAR ENTRY key to unassign any assigned bits before you start.

c. Place the cursor on the period under the 15 in the bit assignment pop-up and press SELECT. This will place an asterisk in the pop-up for bit 15, indicating Pod 1 bit 15 is now assigned to the DATA label. Repeat this procedure until all 16 bits have an asterisk under each bit number. Place the cursor on Done and press SELECT to close the pop-up.

d. Repeat step c for Pod 2 and the ADDR label to assign all 16 bits.

e. Repeat step c except you will assign the lower eight bits (0 - 7) of Pod 3 to the ADDR label.

Specifying the J Clock

If you remember from "What's a State Analyzer" in *Feeling Comfortable With Logic Analyzers*, the state analyzer samples the data under the control of an external clock, which is "synchronous" with your circuit under test. Therefore, you must specify which clock probe you will use for your measurement. In this exercise, you will use the J clock, which is accessible through pod 1.

1. Select the STATE FORMAT SPECIFICATION menu by pressing the FORMAT key.

2. Set the J Clock to sample on a negative-going edge.

   a. Place the cursor on the CLOCK field and press SELECT.

   b. Place the cursor on the box just to the right of J in the pop-up (labeled OFF) and press SELECT.

   c. Place the cursor on ↓ and press SELECT.

   d. Place the cursor on Done and press SELECT.

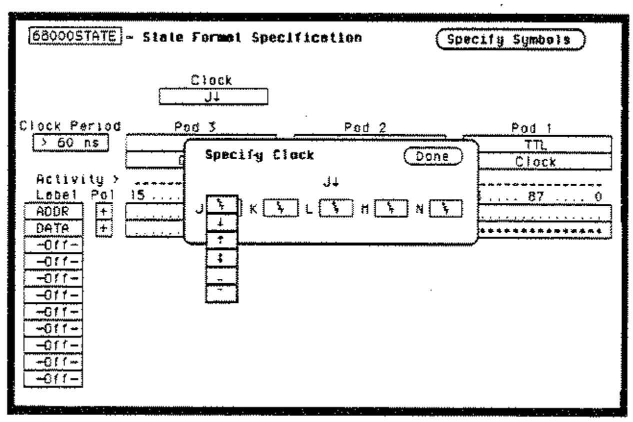


Figure 20-4. Specifying the J Clock

Specifying a Trigger Condition

To capture the data and place the data of interest in the center of the display of the STATE LISTING menu, you need to tell the state analyzer when to trigger. Since the first event of interest is address 0000, you need to tell the state analyzer to trigger when it detects address 0000 on the address bus.

1. Select the STATE TRACE SPECIFICATION menu by pressing the TRACE key.

2. Set the trigger so that the state analyzer triggers on address 0000. If the Trigger on option is not already a perform steps a through d. If the option is a skip to step e.

   a. Place the cursor on the 1 in the Sequence Levels field of the menu and press SELECT.

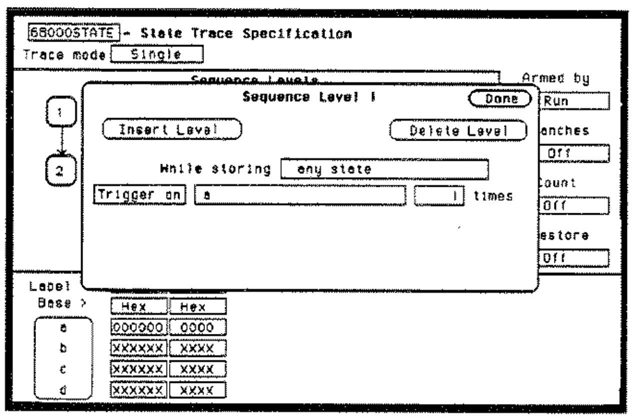


Figure 20-5. State Trace Specification Menu

   b. Place the cursor on the field to the right of the Trigger on field and press SELECT. Another pop-up appears showing you a list of "trigger on" options. Options a through h are qualifiers. You can assign them a pattern for the trigger specification.

c. Place the cursor on the a option and press SELECT.

d. Place the cursor on Done in the Sequence Levels pop-up and press SELECT.

e. Place the cursor on the field to the right of the a under the label ADDR and press SELECT.

f. With the keypad, press 0 (zero) until there are all zeros in the Specify Pattern: pop-up and then press SELECT.

Your trigger specification now states: "While storing anystate trigger on "a" once and then store anystate."

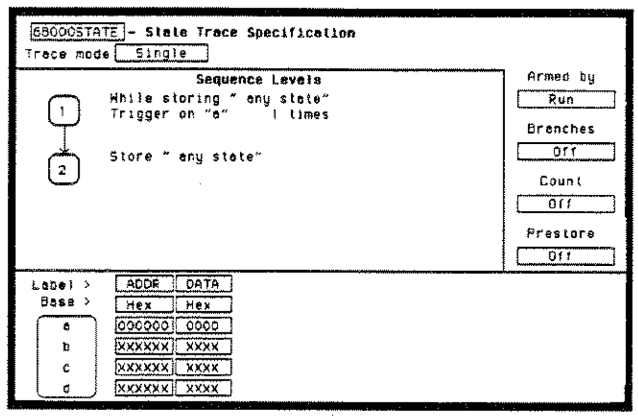


Figure 20-6. State Trace Specification

When the state analyzer is connected to your circuit and is acquiring data, it continuously stores until it sees 0000 on the address bus, then it will store anystate until the analyzer memory is filled.

Acquiring the Data

Since you want to capture the data when the microprocessor sends address 0000 on the bus after power-up, you press the RUN key to arm the state analyzer and then force a reset of your circuit. When the reset cycle ends, the microprocessor should send address 0000 trigger the state analyzer and switch the display to the STATE LISTING menu.

We'll assume this is what happens in this example, since the odds that the microprocessor won't send address 0000 are very low.

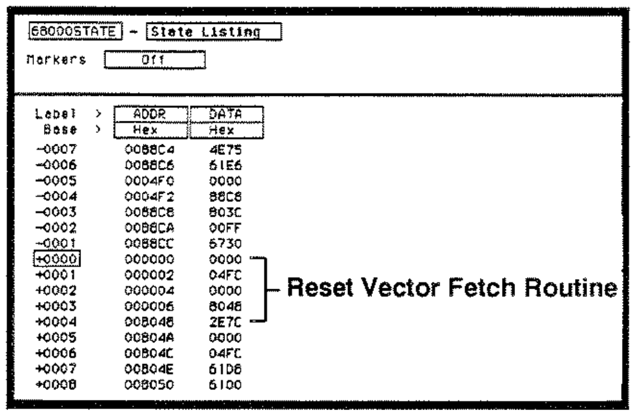


Figure 20-7. Reset Vector Fetch Routine

Now is the time to load the state measurement demo file from the disc if you wish. The file name is STATEDEMO. Refer to "Load Operation" in chapter 6 if you need a reminder on how to load a file.

The State Listing

The state listing displays three columns of numbers as shown:

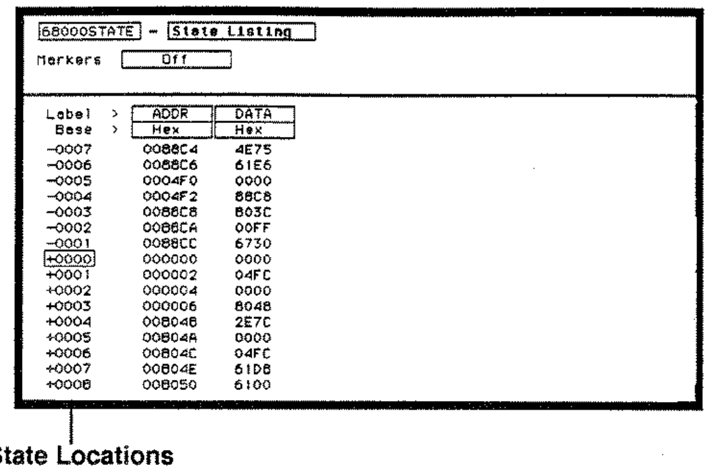


Figure 20-8. State Locations

The first column of numbers are the state line number locations as they relate to the trigger point. The trigger state is on line + 0000 in the vertical center of the list area. The negative numbers indicate states occurring before the trigger and the positive numbers indicate states occurring after the trigger.

The second column of numbers are the states (listed in HEX) the state analyzer sees on the address bus. This column is labeled ADDR.

The third column of numbers are the states (listed in HEX) the state analyzer sees on the data bus. This column is labeled DATA.

Finding the Answer

Your answer is now found in the listing of states + 0000 through + 0004.

The 68000 always reads address locations 0, 2, 4, and 6 to find the stack pointer location and memory location for the instruction it fetches after power-up. The 68000 uses two words for each of the locations that it is looking for, a high word and a low word. When the software designers program the ROM, they must put the stack pointer location at address locations 0 and 2. 0 is the high word location and 2 is the low word location. Similarly, the high word of the instruction fetch location must be in address location 4 and the low word in location 6.

In order for the 68000 to do this, the software design calls for the reset vector to:

1. set the stack pointer to 04FC, and

2. read memory address location 8048 for its first instruction fetch.

Therefore, you are interested in what is on both the address bus and the data bus in states 0 through 3.

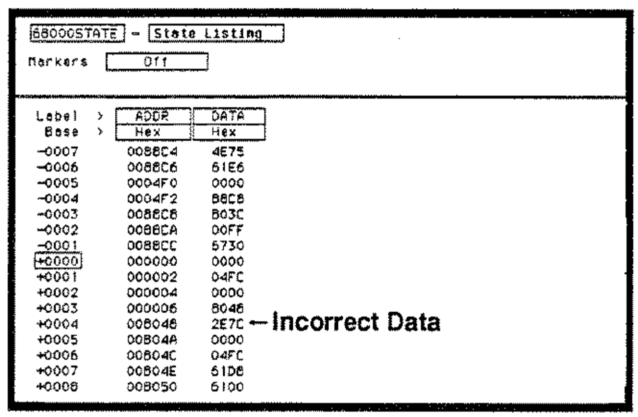
You look at the following listing and see that states 0 and 1 do contain address locations 0 and 2 under the ADDR label, indicating the microprocessor did look at the correct locations for the stack pointer data. You also see that the data contained in these ROM locations are 0000 and 04FC, which are correct.

You then look at states 2 and 3. You see that the next two address locations are 4 and 6, which is correct, and the data found at these locations is 0000 and 8048, which is also correct.

```
+ 0000  000000  0000
+ 0001  000002  04FC
+ 0002  000004  0000
+ 0003  000006  8048
+ 0004  008048  3E7C
```

So far you have verified that the microprocessor has correctly performed the reset vector search. The next thing you must verify is whether the microprocessor addresses the correct location in ROM that it was instructed to address in state 4 and whether the data is correct in this ROM location. From the listing you see that the address in state 4 is 008048, which is correct, but the instruction found in this location is 2E7C, which is not correct. You have found your problem: incorrect data stored in ROM for the microprocessor's first instruction.

+ 0000 000000 0000 (high word of stack pointer location)
+ 0001 000002 04FC (low word of stack pointer location)
+ 0002 000004 0000 (high word of instruction fetch location)
+ 0003 000006 8048 (low word of instruction fetch location)
+ 0004 008048 2E7C (first microprocessor instruction)


68000STATE - State Listing

Markers Off

Label >	ADDR	DATA
Base >	Hex	Hex
-0007	0088C4	4E75
-0006	0088C6	61E6
-0005	0004F0	0000
-0004	0004F2	88C8
-0003	0088C8	B03C
-0002	0088CA	00FF
-0001	0088CC	5730
+0000	000000	0000
+0001	000002	04FC
+0002	000004	0000
+0003	000006	8048
+0004	008048	2E7C ← Incorrect Data
+0005	00804A	0000
+0006	00804C	04FC
+0007	00804E	61D8
+0008	008050	6100

Figure 20-9. Incorrect Data

Summary

You have just learned how to make a simple state measurement with the HP 1650B Logic Analyzer. You have:

- specified a state analyzer
- learned which probes to connect
- assigned pods 1, 2, and 3
- assigned labels
- assigned bits
- specified the J clock
- specified a trigger condition
- acquired the data
- interpreted the state listing

You have seen how easy it is to use the state analyzer to capture the data on the address and data buses. You can use this same technique to capture and display related data on the microprocessor status control, and various strobe lines. You are not limited to using this technique on microprocessors. You can use this technique any time you need to capture data on multiple lines and need to sample the data relative to a system clock.

Chapter 20 shows you how to use the logic analyzer as an interactive timing and state analyzer. You will see a simple measurement that shows you both timing waveforms and state listings and how they are correlated.

If you have an HP 1651B, you do not have enough channels to simultaneously capture all the data for a 68000. But, since you probably aren't working with 16-bit microprocessors, this example is still valuable because it shows you how to make the same kind of measurement on an eight-bit microprocessor.

21

Mixed Mode Displays

Introduction

This chapter shows you both a timing/state and a state/state mixed mode display. The detailed operation of each individual type of display is in their respective chapters. Only the unique features of the mixed modes displays are given here.

Accessing Mixed Mode Displays

You can access mixed mode displays when both analyzers are on and **Count** is set to **Time** in the State Trace Specification menu. Mixed mode displays are only available for two state analyzers or one timing and one state analyzer. To display mixed mode, place the cursor on the field in the upper left corner of the display and press SELECT. When the pop-up appears you will see the **Mixed mode** option. Place the cursor on this option and press SELECT. When the pop-up closes, mixed mode will be displayed.

Timing/State Mixed Mode Display

When both timing and state analyzers are on you can display both the State Listing and the Timing Waveforms simultaneously as shown.

The data in both parts of the display can be time-correlated as long as Count (State Trace menu) is set to Time.

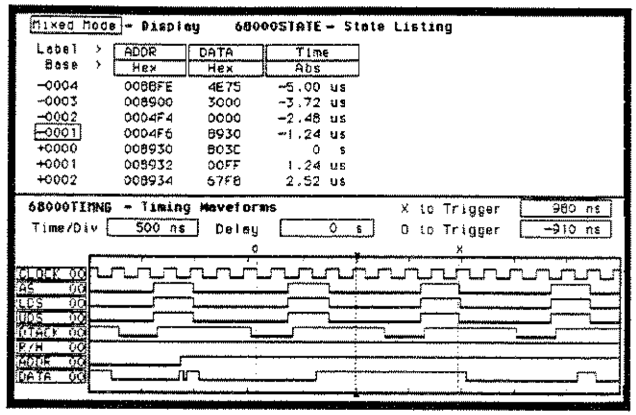


Figure 21-1. Timing/State Mixed Mode Display

The markers for the State Listing and the Timing Waveform in time-correlated Mixed Mode are different from the markers in the individual displays. You will need to place the markers on your points of interest in the time-correlated Mixed Mode even though you have placed them in the individual displays.

State/State Mixed Mode Display

When two state analyzers are on, the logic analyzer will display both state listings as shown below. Data from state machine 1 is the data with the normal memory location columns filled and with normal black on white video. State machine 2 data is interlaced and displayed in inverse video (white on black). Its memory locations are offset to the right in a column.

To time-correlate data from two state machines, you must set the Count (State Trace menu) for both machines to Time.

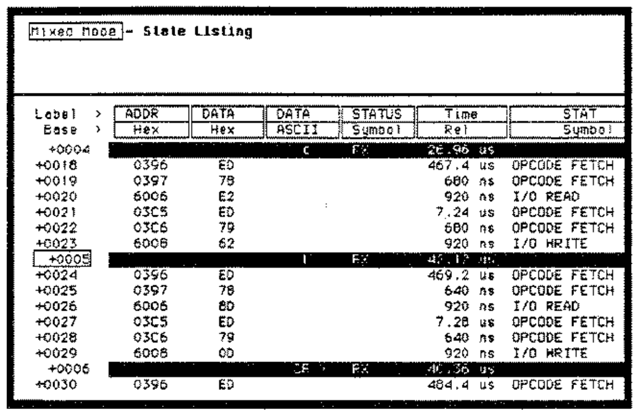


Figure 21-2. Dual-State Machine Mixed Mode Display

The markers for a State/State time-correlated Mixed Mode will be the same as the markers placed in each of the individual State Listings.

Time-Correlated Displays

The HP1650B/51B Logic Analyzers can time-correlate data between the timing analyzer and the state analyzer (see Timing/State Mixed Mode Display) and between two state analyzers (see State/State Mixed Mode Display). In order for the logic analyzer to time-correlate data, the **Count** in the State Trace menu must be set to **Time** before you start an acquisition.

The logic analyzer uses a counter to keep track of the time between the triggering of one analyzer and the triggering of the second. It uses this count in the mixed mode displays to reconstruct time-correlated data.

22

Timing/State Measurement Example

Introduction

In this chapter you will learn how to use the timing and state analyzers interactively by setting up the logic analyzer to make a simple measurement. We give you the measurement results as actually measured by the logic analyzer, since you may not have the same circuit available.

The exercise in this chapter is organized differently than the exercises in the two previous chapters. Since you have already set up both the timing and state analyzers, you should be ready to set them up for this measurement by looking at the menu pictures.

Any new set-ups in this exercise will be explained in task format steps like the previous chapters.

How you use the steps depends on how much you remember from chapters 1 through 4 of the *Getting Started Guide*. If you can set up each menu by just looking at the menu picture, go ahead and do so. If you need a reminder of what steps to perform, follow the numbered steps. If you still need more information about "how," use the lettered steps.

When you have finished configuring the logic analyzer for this exercise, you can load a file from the operating system disk. This file configures the logic analyzer the same way it is configured for this exercise. It also loads the same data acquired for this exercise so you can see what it looks like on screen.

In order to learn how to configure the logic analyzer, we recommend that you follow the exercise to "Acquiring the Data" before loading the file from the disk.

You can also compare your configuration with the one on the disk by printing it (if you have a printer) or making notes before you load the file.

Problem Solving with the Timing/State Analyzer

In this example assume you have designed a microprocessor-controlled circuit. You have completed the hardware, and the software designer has completed the software and programmed the ROM (read-only memory). When you turn your circuit on for the first time, your circuit doesn't work properly. You have checked the power supply voltages and the system clock, and they are working properly.

Since the circuit has never worked before, you and the software engineer aren't sure if it is a hardware or software problem. You need to do some testing to find a solution.

You also notice the circuit fails intermittently. More specifically, it only fails when the microprocessor attempts to address a routine that starts at address 8930.

What Am I Going to Measure?

To see what might be causing the failure, you decide to start where the microprocessor goes to the routine that starts at address 8930. The first thing you check is whether the microprocessor actually addresses address 8930. The next thing you check is whether the code is correct in all the steps in this routine.

Your measurement, then, requires verification of:

- whether the microprocessor addresses location 8930
- whether all the addresses within the routine are correct
- whether all the data at the addresses in the routine are correct

If the routine is correct, the state listing will display:

```
+ 0000  008930  B03C
+ 0001  008932  61FA
+ 0002  008934  67F8
+ 0003  008936  B03C
+ 0004  00892E  61FA
```

How Do I Configure the Logic Analyzer?

In order to make this measurement, you must configure the logic analyzer as a state analyzer because you want to trigger on a specific state (8930). You also want to verify that the addresses and data are correct in the states of this routine.

Configure the logic analyzer so that Analyzer 1 is a state analyzer as shown:

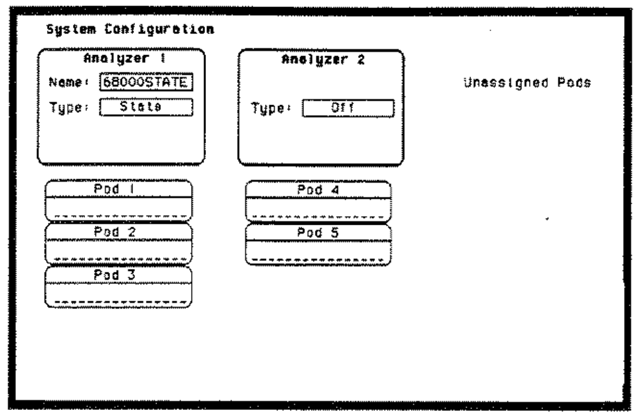


Figure 22-1. System Configuration Menu

Configuring the State Analyzer

Now that you have configured the system, you are ready to configure the state analyzer. Configure the STATE FORMAT SPECIFICATION menu as shown:

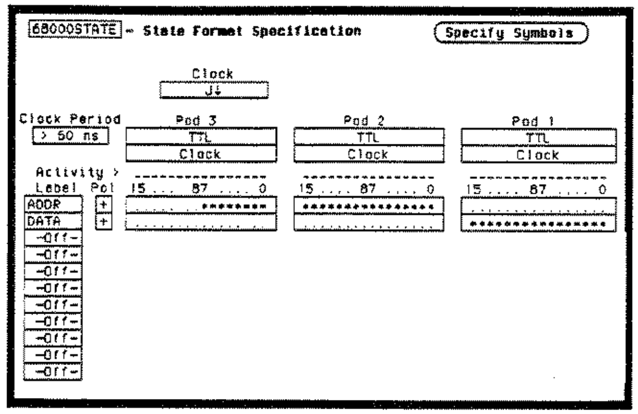


Figure 22-2. State Format Specification Menu

Configure the STATE TRACE SPECIFICATION menu as shown:

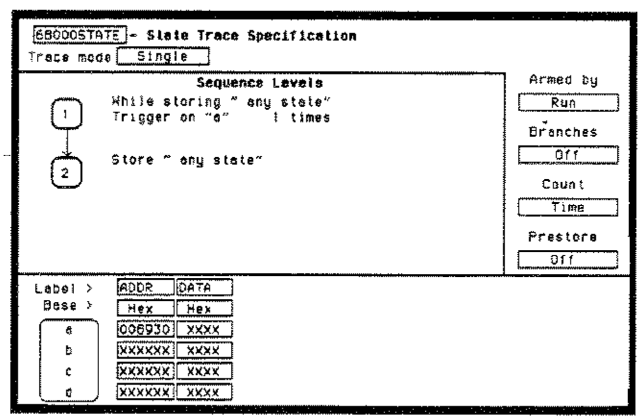


Figure 22-3. State Trace Specification Menu

Connecting the Probes

At this point, if you had a target system with a 68000 microprocessor, you would connect the logic analyzer to your system. Since you will be assigning labels ADDR and DATA, you will hook the probes to your system accordingly.

- Pod 1 probes 0 through 15 to the data bus lines D0 through D15
- Pod 2 probes 0 through 15 to the address bus lines A0 through A15
- Pod 3 probes 0 through 7 to the address bus lines A16 through A23
- Pod 1, CLK (J clock) to the address strobe (LAS)

Acquiring the Data

Since you want to capture the data when the microprocessor sends address 8930 on the bus, you press the RUN key to arm the state analyzer. If the microprocessor sends address 8930, it will trigger the state analyzer and switch the display to the STATE LISTING menu.

We'll assume this is what happens in this example.

Finding the Problem

You look at this listing to see what the data is in states + 0000 through + 0004. You know your routine is five states long.

The 68000 does address location 8930, so you know that the routine is addressed. Now you need to compare the state listing with the following correct addresses and data:

+ 0000	008930	B03C
+ 0001	008932	61FA
+ 0002	008934	67F8
+ 0003	008936	B03C
+ 0004	00892E	61FA

As you compare the state listing (shown below) with the above data you notice the data at address 8932 is incorrect. Now you need to find out why.

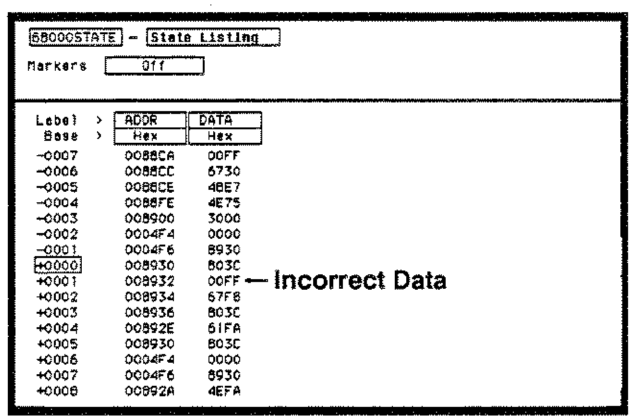


Figure 22-4. Incorrect Data

Your first assumption is that incorrect data is stored to this memory location. Assume this routine is in ROM since it is part of the operating system for your circuit. Since the ROM is programmed by the software designer, you have the software designer verify whether or not the data at address 8932 is correct. The software designer tells you that the data is correct. Now what do you do?

Now it's time to look at the hardware to see if it is causing incorrect data when the microprocessor reads this memory address. You decide you want to see what is happening on the address and data buses during this routine in the time domain.

In order to see the time domain, you need the timing analyzer.

What Additional Measurements Must I Make?

Since the problem exists during the routine that starts at address 8930, you decide you want to see the timing waveforms on the address and data bus when the routine is running. You also want to see the control signals that control the read cycle. You will then compare the waveforms with the timing diagrams in the 68000 data book.

Your measurement, then, requires verification of:

- correct timing of the control signals
- stable addresses and data during the memory read

The control signals you must check are:

- system clock
- address strobe (AS)
- lower and upper data strobes (LDS and UDS)
- data transfer acknowledge (DTACK)
- read/write (R/W)

How Do I Re-Configure the Logic Analyzer?

In order to make this measurement, you must re-configure the logic analyzer so Analyzer 2 is a timing analyzer. You leave Analyzer 1 as a state analyzer since you will use the state analyzer to trigger on address 8930.

Configure the logic analyzer so Analyzer 2 is a timing analyzer as shown:

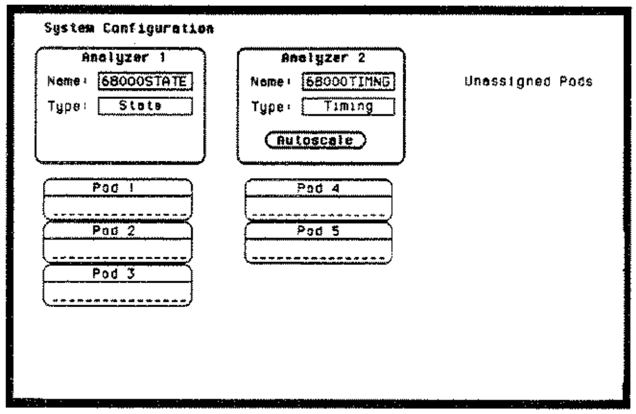


Figure 22-5. System Configuration Menu

Connecting the Timing Analyzer Probes

At this point you would connect the probes of pods 4 and 5 as follows:

- Pod 4 bit 0 to address strobe (AS)
- Pod 4 bit 1 to the system clock
- Pod 4 bit 2 to low data strobe (LDS)
- Pod 4 bit 3 to upper data strobe (UDS)
- Pod 4 bit 4 to the read/write (R/W)
- Pod 4 bit 5 to data transfer acknowledge (DTACK)
- Pod 5 bits 0 through 7 to address lines A0 through A7
- Pod 5 bits 8 through 15 to data lines D0 through D7

Configuring the Timing Analyzer

Now that you have configured the system, you are ready to configure the timing analyzer. Configure the TIMING FORMAT SPECIFICATION menu as shown:

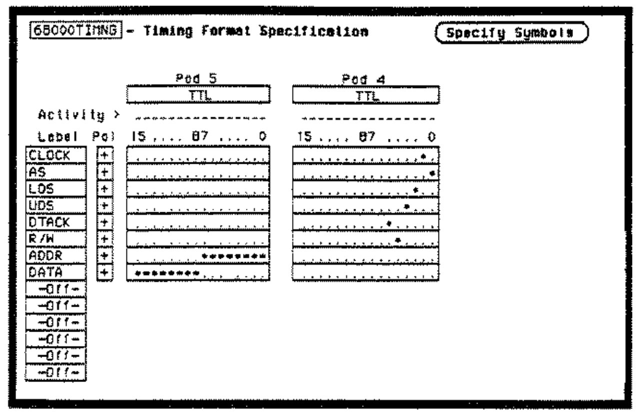


Figure 22-6. Timing Format Specification Menu

Configure the TIMING TRACE SPECIFICATION as shown:

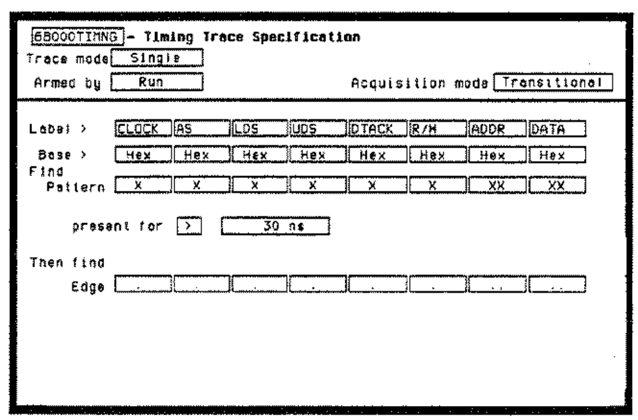


Figure 22-7. Timing Trace Specification Menu

Setting the Timing Analyzer Trigger

Your timing measurement requires the timing analyzer to display the timing waveforms present on the buses when the routine is running. Since you triggered the state analyzer on address 8930, you want to trigger the timing analyzer so the timing waveforms can be time correlated with the state listing.

To set up the logic analyzer so that the state analyzer triggers the timing analyzer, perform these steps:

1. Display the TIMING TRACE SPECIFICATION menu.
2. Place the cursor on the Armed by ____ field and press SELECT.
3. Place the cursor on the 68000STATE option in the pop-up and press SELECT.

Your timing trace specification should match the menu shown:

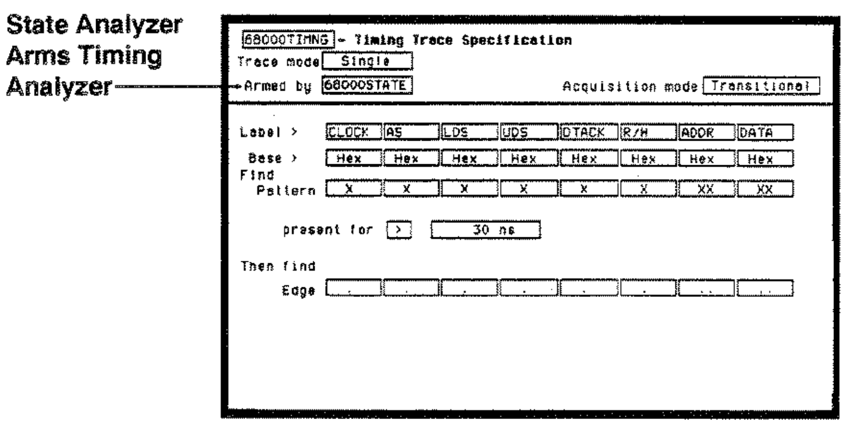


Figure 22-8. Armed by 68000 STATE

Time Correlating the Data

In order to time correlate the data, the logic analyzer must store the timing relationships between states. Since the timing analyzer samples asynchronously and the state analyzer samples synchronously, the logic analyzer must use the stored timing relationship of the data to reconstruct a time correlated display.

To set up the logic analyzer to keep track of these timing relationships, turn on a counter in the STATE TRACE SPECIFICATION menu. The following steps show you how:

1. Display the STATE TRACE SPECIFICATION menu.

2. Place the cursor in the field just below Count on the right side of the display and press SELECT.

3. Place the cursor on the Time option and press SELECT. The counter will now be able to keep track of time for the time correlation.

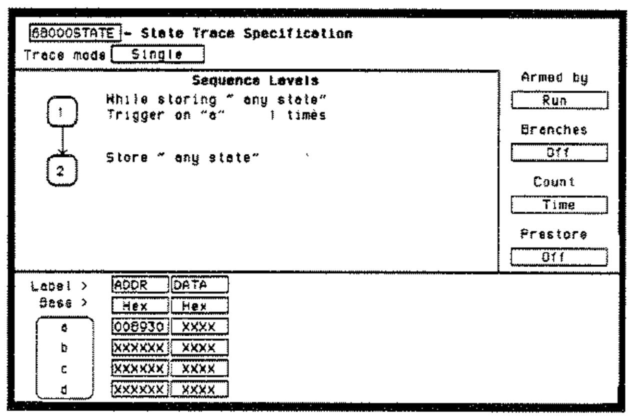


Figure 22-9. Count Set to Time

Re-Acquiring the Data

After you connect the probes of pods 4 and 5 to your circuit, all you have to do is press RUN. When the logic analyzer acquires the data it switches the display to the STATE LISTING menu unless you switched one of the other menus to the timing analyzer after reconfiguring the STATE TRACE menu. Regardless of which menu is displayed, change the display to the Mixed mode.

Mixed Mode Display

The Mixed mode display shows you both the STATE LISTING and TIMING WAVEFORMS menus simultaneously. To change the display to the Mixed mode:

1. Place the cursor on the field in the upper left corner of the display and press SELECT.

2. Place the cursor on Mixed mode and press SELECT. You will now see the mixed display as shown:

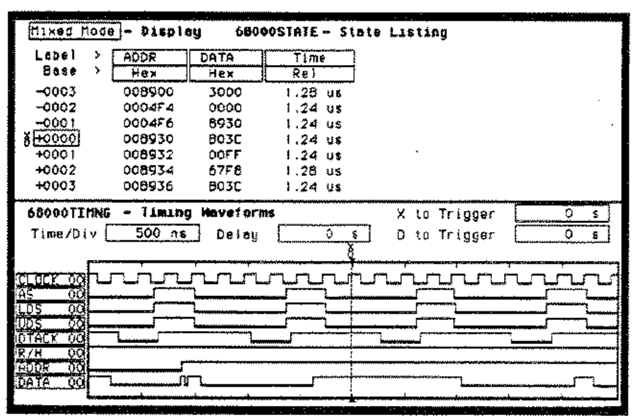


Figure 22-10. Mixed Mode Display

Interpreting the Display

In the Mixed mode display the state listing is in the top half of the screen and the timing waveforms are in the lower half. The important thing to remember is that you time correlated this display so you could see what is happening in the time domain during the faulty routine.

Notice that the trigger point in both parts of the display is the same as it was when the displays were separate. The trigger in the state listing is in the box containing + 0000 and the trigger of the timing waveform is the vertical dotted line.

As you look at the mixed display, you notice nothing wrong except the data at address 8932 is incorrect. However, you are seeing only one bit each of the address and the data. To see all the data and addresses in the timing waveform part of the display, you must overlap them.

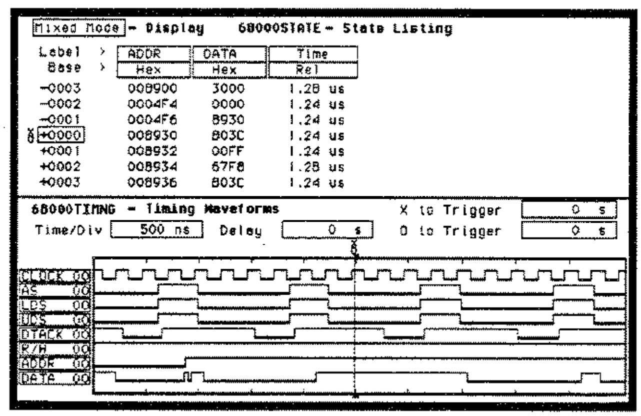


Figure 22-11. Interpreting the Display

Overlapping Timing Waveforms

Since you see nothing wrong with the timing waveforms so far, you think unstable data may be on the data lines during the read cycle. In order to see unstable data, you must be able to see all the data lines during the read and look for transitions. Overlapping the waveforms allows you to do this. To overlap waveforms, follow these steps:

1. Place the cursor on the 00 of the ADDR 00 label and press SELECT. The following pop-up opens in which you specify the bit or bits of the address bus you want to overlap.

2. Rotate the KNOB until all is displayed and press SELECT. All the address bits will be overlapped on one line.

3. Repeat step 2 except overlap the data bits.

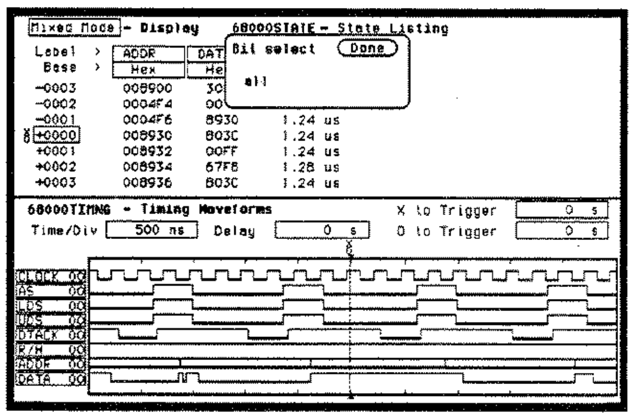


Figure 22-12. Overlapping Timing Waveforms

Finding the Answer

As you look at the overlapping waveforms, you notice there are transitions on the data lines during the read cycle, indicating the data is unstable. You have found the probable cause of the problem in this routine. Additional troubleshooting of the hardware will identify the actual cause.

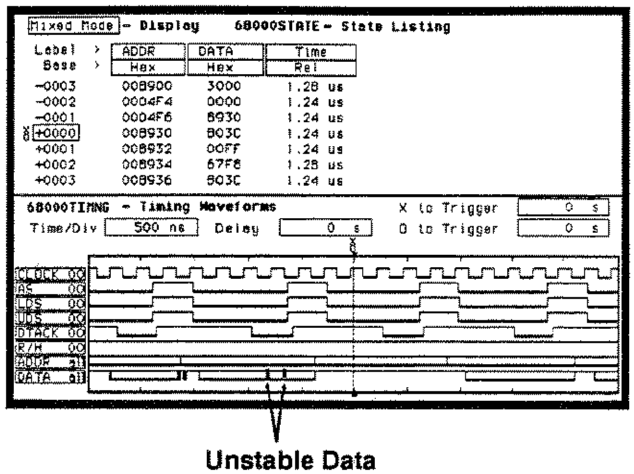


Figure 22-13. Unstable Data

Summary

You have just learned how to use the timing and state analyzers interactively to find a problem that first appeared to be a software problem, but actually was a hardware problem.

You have learned to:

- trigger one analyzer with the other
- time correlate measurement data
- interpret the Mixed mode display
- overlap timing waveforms

If you have an HP 1651B, you do not have enough channels to simultaneously capture all the data for a 68000. But, since you probably aren't working with 16-bit microprocessors, this exercise is still valuable because it shows you how to make the same kind of measurement on an eight-bit microprocessor.

A

Error Messages

Introduction

This appendix lists the error messages that require corrective action to restore proper operation of the logic analyzer. There are several messages that you will see that are merely advisories and are not listed here. For example, "Load operation complete" is one of these advisories.

The messages are listed in alphabetical order and in bold type.

Acquisition aborted. This message is displayed whenever data acquisition is stopped.

At least one edge is required. A state clock specification requires at least one clock edge. This message only occurs if you turn off all edges in the state clock specification.

Autoload file not of proper type. This message is displayed if any file other than an HP 1650B/51B configuration file is specified for an autoload file and the logic analyzer is powered up.

Autoscale aborted. This message is displayed when the STOP key is pressed or if a signal is not found 15 seconds after the initiation of autoscale.

BNC is being used as an ARM IN and cannot be used as an ARM OUT. This message is displayed when BNC arms machine 1 (or 2), machine 1 (or 2) arms machine 2 (or 1), and the BNC is specified as ARM OUT. It will not occur if BNC arms machine 1 (or 2), and machine 1 (or 2) arms BNC.

Configuration not loaded. Indicates a bad configuration file. Try to reload the file again. If the configuration file will still not load, a new disk and/or configuration file is required.

Copy operation complete. Indicates the copy operation has either successfully completed or has been stopped.

Correlation counter overflow. The correlation counter overflows when the time from when one machine's trigger to the second machine's trigger exceeds the maximum count. It may be possible to add a "dummy" state to the second machine's trigger specification that is closer in time to the trigger of the first machine.

Data can not be correlated-Time count need to be turned on. "Count" must be set to "Time" in both machines to properly correlate the data.

Destination write protected-file not copied. Make sure you are trying to copy to the correct disk. If so, set the write protect tab to the non-protect position and repeat the copy operation.

File not copied to disk-check disk. The HP 1650B/51B does not support track sparing. If a bad track is found, the disk is considered bad. If the disk has been formatted elsewhere with track sparing, the HP 1650B/51B will only read up to the first spared disk.

Hardware ERROR: trace point in count block. Indicates the data from the last acquisition is not reliable and may have been caused by a hardware problem. Repeat the data acquisition to verify the condition. If this message re-appears, the logic analyzer requires the attention of service personnel.

Insufficient memory to load IAL - load aborted. This message indicates that there is not a block of free memory large enough for the inverse assembler you are attempting to load even though there may be enough memory in several smaller blocks. Try to load the inverse assembler again. If this load is unsuccessful, load the configuration and inverse assembler separately.

Invalid file name. Check the file name. A file name must start with an alpha character and cannot contain spaces or slashes (/).

Inverse assembler not loaded-bad object code. Indicates a bad inverse assembler file on the disk. A new disk or file is required.

Maximum of 32 channels per label. Indicates an attempt to assign more than 32 channels to a label. Reassign channels so that no more than 32 are assigned to a label.

No room on destination-file not copied. Indicates the destination disk doesn't have enough room for the file you are attempting to copy. Try packing the disk and repeating the copy operation. If this is unsuccessful, you will need to use a different disk.

(x) Occurrences Remaining in Sequence. Indicates the logic analyzer is waiting for (x) number of occurrences in a sequence level of the trigger specification before it can go on to the next sequence level.

PRINT has been stopped. This message appears when the print operation has been stopped.

(x) Secs Remaining in Trace. Indicates the amount of time remaining until acquisition is complete in Glitch mode.

Search failed - O pattern not found. Indicates the O pattern does not exist in the acquired data. Check for a correct O marker pattern specification.

Search failed - X pattern not found. Indicates the X pattern does not exist in the acquired data. Check for a correct X marker pattern specification.

Slow Clock or Waiting for Arm. Indicates the state analyzer is waiting for a clock or arm from the other machine. Re-check the state clock or arming specification.

Slow or missing Clock. Indicates the state analyzer has not recognized a clock for 100 ms. Check for a missing clock if the intended clock is faster than 100 ms. If clock is present but is slower than 100 ms, the data will still be acquired when a clock is recognized and should be valid.

Specified inverse assembler not found. Indicates the inverse assembler specified cannot be found on the disk.

State clock violates overdrive specification. Indicates the data from the last acquisition is not reliable due to the state clock signal not being reliable. Check the clock threshold for proper setting and the probes for proper grounding.

States Remaining to Post Store. Indicates the number of states required until memory is filled and acquisition is complete.

Time count need to be turned on. This message appears when the logic analyzer attempts to time correlate data and "Count" is not set to "Time."

Transitions Remaining to Post Store. Indicates the number of transitions required until memory is filled and acquisition is complete.

Unsupported destination format-file not copied. Indicates the disk you have attempted to copy to is either not formatted or formatted in a format not used by the logic analyzer. Format the disk or use a properly formatted disk and repeat the copy operation.

Value out of range. Set to limit. Indicates an attempt to enter a value that is out of range for the specific variable. The logic analyzer will set the value to the limit of the variable range automatically.

Waiting for Arm. Indicates the arming condition has not occurred.

Waiting for Prestore. Indicates the prestore condition has not occurred (timing analyzer only).

Waiting for Trigger. Indicates the trigger condition has not occurred.

Warning: Chips not successfully running. Indicates the acquisition chips in the logic analyzer are not running properly. Press STOP and then RUN again. If the warning message reappears, refer the logic analyzer to service personnel.

Warning: Chips not successfully stopped. Indicates the acquisition chips in the logic analyzer are not stopping properly. Press RUN and then STOP again. If the warning message reappears, refer the logic analyzer to service personnel.

Warning: Duplicate label name. Indicates an attempt to assign an existing name to a new label.

Warning: Duplicate symbol name. Indicates an attempt to assign an existing name to a new symbol.

Warning: Invalid file type. Indicates an attempt to load an invalid file type. For example, the SYSTEM file can only be loaded on power-up and if you attempt to load it from the I/O menu, this message will appear.

Warning: No clock edge in other clock, added clock edge. This message only occurs in a state analyzer using mixed or demultiplexed clocks. It indicates there is no edge specified in either the master or slave clock. There must be at least one edge in each of the clocks.

Warning: Symbol memory full. Max 200 symbols. Indicates an attempt to store more than 200 symbols.

Warning: Run HALTED due to variable change. Indicates a variable has been changed during data acquisition in the continuous trace mode. The data acquisition will be halted and this message will be displayed when any variable affecting the system configuration, clock thresholds, clock multiplexing, or trace specification menus is changed during data acquisition.

B

Installation and Maintenance

Introduction

This appendix contains information and instructions necessary for preparing the HP 1650B/51B Logic Analyzers for use. Included in this section are inspection procedures, power requirements packaging information, and operating environment. It also tells you how to load the operating system and turn the logic analyzer on. Maintenance that you can do as an operator is included in this appendix.

Initial Inspection

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Accessories supplied with the instrument are listed under Accessories Supplied in section 1 of this manual. An overview of the self-test procedure is in Appendix C of this manual. The complete details of the procedure are in Chapter 6 of the *Service Manual*. Electrical performance verification functions are also in Chapter 3 of the *Service Manual*.

If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the Self Test Performance Verification, notify the nearest Hewlett-Packard Office. If the shipping container is damaged, or the cushioning materials show signs of stress, notify the carrier as well as the Hewlett-Packard Office. Keep all shipping materials for the carrier's inspection. The Hewlett-Packard office will arrange for repair or replacement at HP option without waiting for claim settlement.

Operating Environment

You may operate your logic analyzer in a normal lab or office type environment without any additional considerations. If you intend to use it in another type of environment, refer to Table D-2 in Appendix E for complete operating environment specifications. Note the non-condensing humidity limitation. Condensation within the instrument cabinet can cause poor operation or malfunction. Protection should be provided against temperature extremes which cause condensation.

Ventilation

You must provide an unrestricted airflow for the fan and ventilation openings in the rear of the logic analyzer. However, you may stack the logic analyzer under, over, or in-between other instruments as long the surfaces of the other instruments are not needed for their ventilation.

Storage and Shipping

This instrument may be stored or shipped in environments within the following limitations:

- Temperature: $-40\,^\circ C$ to $+75\,^\circ C$
- Humidity: Up to 90% at $65\,^\circ C$
- Altitude: Up to 15,300 meters (50,000 feet)

Tagging for Service

If the instrument is to be shipped to a Hewlett-Packard office for service or repair, attach a tag to the instrument identifying owner address of owner, complete instrument model and serial numbers and a description of the service required.

Original Packaging

If the original packaging material is unavailable or unserviceable materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is to be shipped to a Hewlett-Packard office for service, tag the instrument (see "Tagging for Service" in this appendix). Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

Other Packaging

The following general instructions should be followed for repacking with commercially available materials.

1. Wrap the instrument in heavy paper or plastic.
2. Use a strong shipping container. A double-wall carton made of 350 lb. test material is adequate.
3. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inches) thick around all sides of the instrument to firmly cushion and prevent movement inside the container. Protect the control panel with cardboard.
4. Seal the shipping container securely.
5. Mark the shipping container FRAGILE to ensure careful handling.
6. In any correspondence, refer to the instrument by model number and full serial number.

Power Requirements

The HP 1650B/51B requires a power source of either 115 or 230 Vac −22% to + 10%; single phase, 48 to 66 Hz; 200 Watts maximum power.

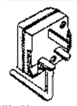
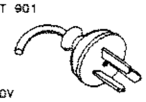
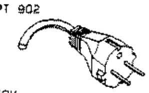
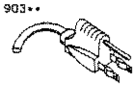
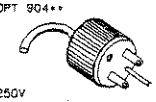
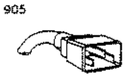
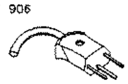
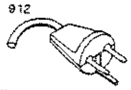
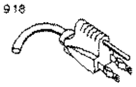
Power Cable

This instrument is provided with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. Refer to Table B-1 for power plugs and HP part numbers for the available plug configurations.

Warning

BEFORE CONNECTING THIS INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (Mains) power cord. The Mains plug must be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two conductor outlet does not provide an instrument ground.

Table B-1. Power Cord Configurations

PLUG TYPE	CABLE PART NO.	PLUG DESCRIPTION	LENGTH IN/CM	COLOR	COUNTRY
OPT 900  250V	8120-1351 8120-1703	Straight *BS1363A 90°	90/228 90/228	Gray Mint Gray	United Kingdom, Cyprus, Nigeria, Zimbabwe, Singapore
OPT 901  250V	8120-1369 8120-0696	Straight *NZSS198/ASC 90°	79/200 87/221	Gray Mint Gray	Australia New Zealand
OPT 902  250V	8120-1689 8120-1692 8120-2857	Straight *CEE7-Y11 90° Straight (Shielded)	79/200 79/200 79/200	Mint Gray Mint Gray Coco Brown	East and West Europe, Saudi Arabia, So. Africa, India (Unpolarized in many nations)
OPT 903**  125V	8120-1378 8120-1521 8120-1992	Straight *NEMA5-15P 90° Straight (Medical) UL544	90/228 90/228 96/244	Jade Gray Jade Gray Black	United States, Canada, Mexico, Phillipines, Taiwan
OPT 904**  250V	8120-0698	Straight *NEMA6-15P	90/228	Black	United States, Canada
OPT 905  250V	8120-1396 8120-1625	CEE22-V1 (System Cabinet Use) 250V	30/76 96/244	Jade Gray	For interconnecting system components and peripherals. United States and Canada only
OPT 906  250V	8120-2104 8120-2296	Straight *SEV1011 1959-24507 Type 12 90°	79/200 79/200	Mint Gray Mint Gray	Switzerland
OPT 912  220V	8120-2956 8120-2957	Straight *DHCK107 90°	79/200 79/200	Mint Gray Mint Gray	Denmark
OPT 917  250V	8120-4211 8120-4600	Straight SABS164 90°	79/200 79/200	Jade Gray	Republic of South Africa India
OPT 918  100V	8120-4753 8120-4754	Straight Miti 90°	90/230 90/230	Dark Gray	Japan

Rev 11NOV88 ART00019

*Part number shown for plug is industry identifier for plug only. Number shown for cable is HP part number for complete cable including plug.
**These cords are included in the CSA certification approval of the equipment.
E=Earth Ground
L=Line
N=Neutral

Removing Yellow Shipping Disk

Your logic analyzer is shipped with a protective yellow shipping disk in the disk drive. Before you can insert the operating system disk you must remove the yellow shipping disk. Press the disk eject button as shown in figure B-1. The yellow shipping disk will pop out part way so you can pull it out of the disk drive.

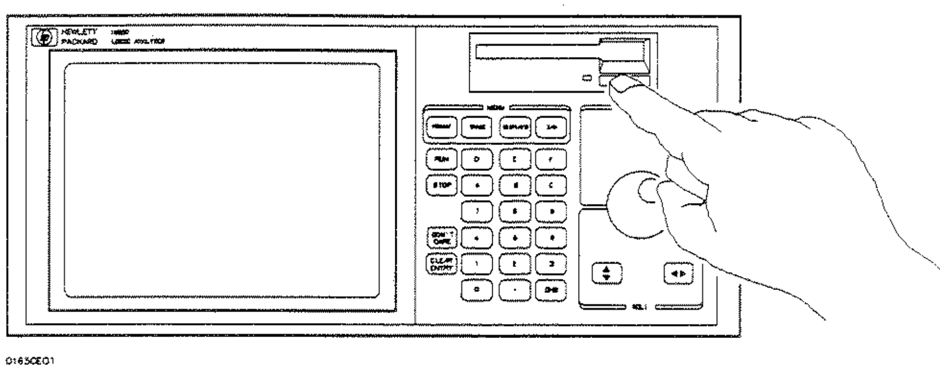


Figure B-1. Removing Yellow Shipping Disk

Selecting the Line Voltage

The line voltage selector has been factory set to the line voltage used in your country. It is a good idea to check the setting of the line voltage selector so you become familiar with what it looks like. If the setting needs to be changed, follow the procedure in the next paragraph.

Caution

You can damage the logic analyzer if the module is not set to the correct position.

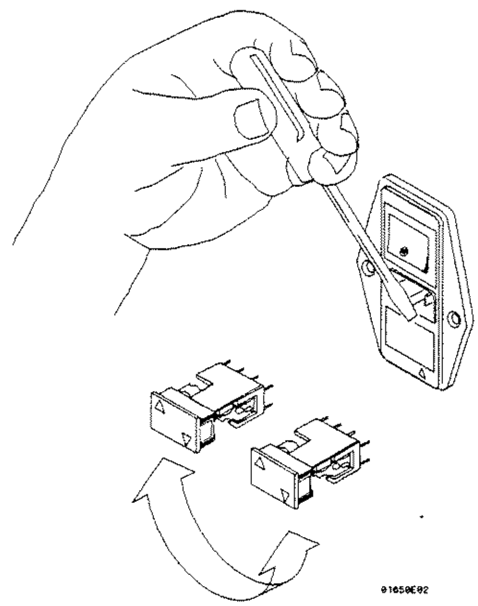


Figure B-2. Selecting the Line Voltage

You change the proper line voltage by pulling the fuse module out and reinserting it with the proper arrows aligned. To remove the fuse module, carefully pry at the top center of the module (as shown) until you can grasp and pull it out by hand.

Checking for the Correct Fuse

If you find it necessary to check or change fuses, remove the fuse module and look at each fuse for its amperage and voltage. Refer to figure B-3 to locate the 115 V and 230 V fuse locations. To remove the fuse module, carefully pry at the top center of the module (see figure B-2) until you can grasp and pull it out by hand.

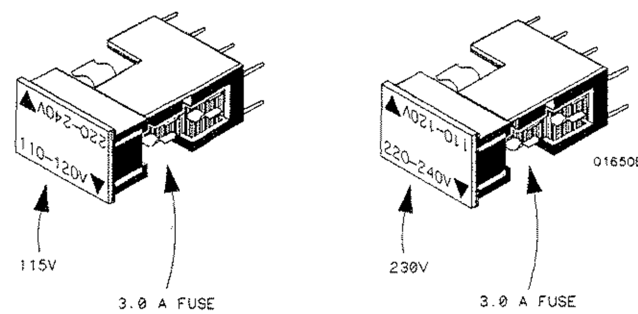


Figure B-3. Checking for the Correct Fuse

Applying Power

When power is applied to the HP 1650B/51B, a power-up self test will be performed automatically. For information on the power-up self test, refer to Appendix C and Section 3 of the *Service Manual*.

Loading the Operating System

Before you can operate the instrument, you must load the operating system from the operating system disk. You received two identical operating system disks. You should mark one of them Master and store it in a safe place. Mark the other one Work and use only the work copy. This will provide you with a back-up in case your work copy becomes corrupt.

Caution

To prevent damage to your operating system disk, DO NOT remove the disk from the disk drive while it is running. Only remove it after the indicator light has gone out.

Installing the Operating System Disk

To load the logic analyzer's operating system, you must install the disk as shown below before you turn on the power. When the disk snaps into place, the disk eject button pops out and you are ready to turn on the logic analyzer.

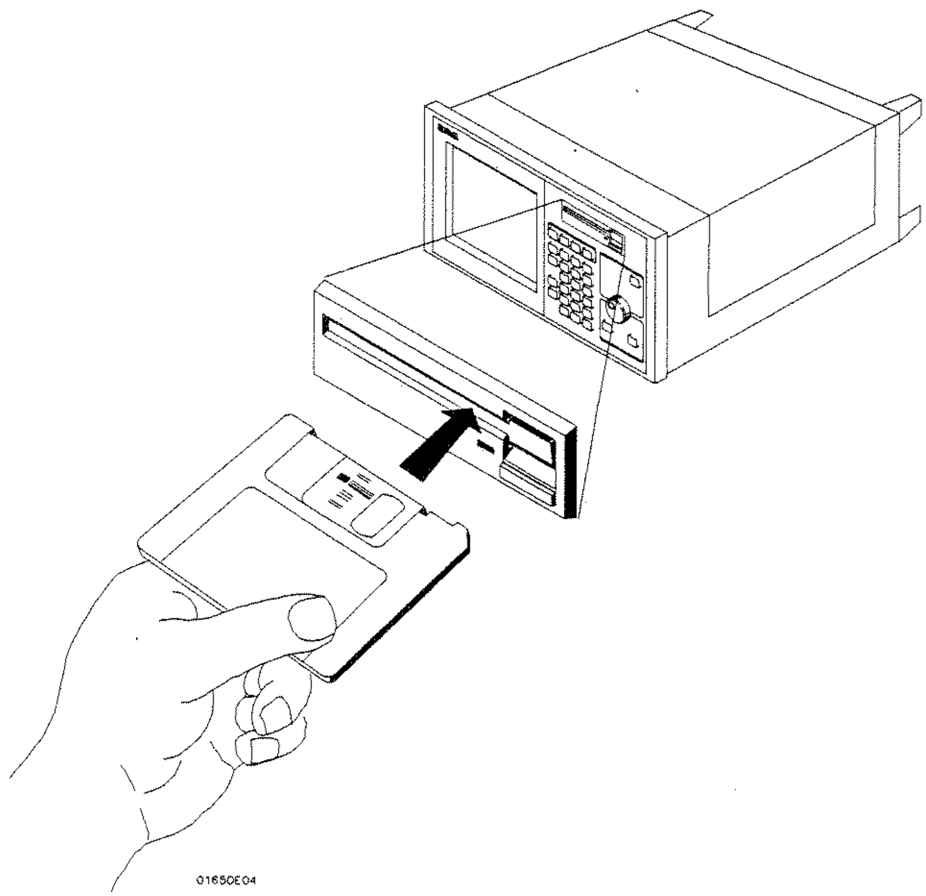


Figure B-4. Installing the Operating System Disk

The logic analyzer will read the disk and load the operating system. It will also run self-tests before it is ready for you to operate.

Line Switch

The line switch is located on the rear panel. You turn the instrument on by pressing the 1 on the rocker switch. Make sure the operating system disk is in the disk drive before you turn on the logic analyzer. If you forget the disk, don't worry, you won't harm anything. You will merely have to repeat the turn-on procedure with the disk in the drive.

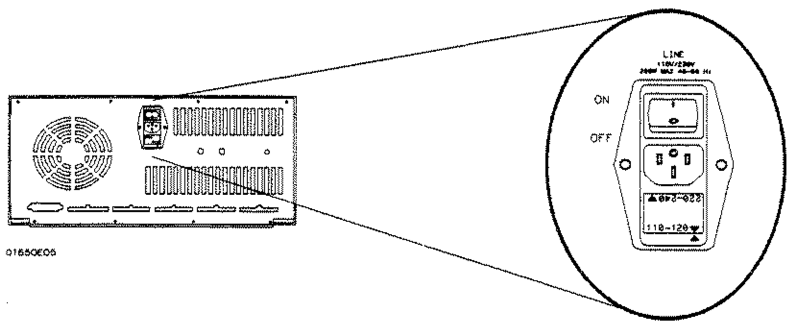


Figure B-5. Line Switch

Intensity Control

Once you have turned the instrument on, you may want to set the display intensity to a level that's more comfortable for you. You do this by turning the INTENSITY control on the rear panel.

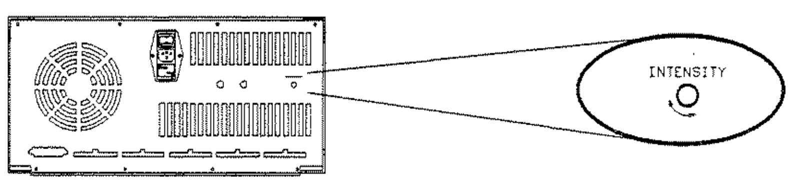


Figure B-6. Intensity Control

Power-Up Self-Test

When you turn on the logic analyzer, it performs a series of self-tests. When it has successfully completed these tests, it loads the operating system into memory from the disk.

When the logic analyzer has completely loaded the operating system it displays the System Configuration menu as shown below.

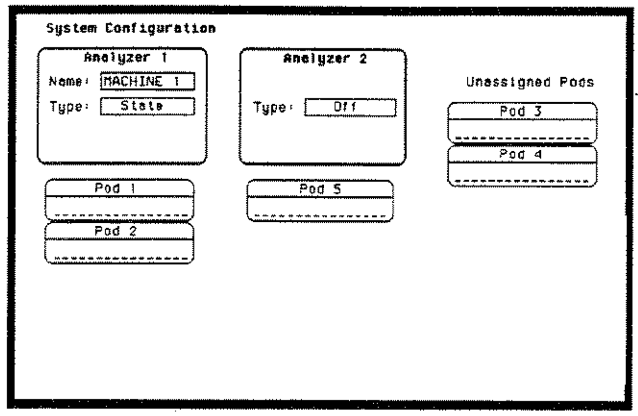


Figure B-7. System Configuration Menu

Note

This is the HP 1650B System Format Specification menu. If you have an HP 1651B, pod 1 will be assigned to analyzer 1 and pod 2 will be assigned to analyzer 2. There won't be any pods in the Unassigned Pods area of the display.

Operator's Maintenance

The only maintenance you need to do is clean the instrument exterior and periodically check the rear panel for air restrictions.

Use only MILD SOAP and WATER to clean the cabinet and front panel. DO NOT use a harsh soap which will damage the water-base paint finish of the instrument.

C

Operator Self-Tests

Introduction

This appendix gives you an overview of the self tests the logic analyzer runs when you turn it on. You can also access the self tests from the I/O menu. This appendix is not intended to provide service information, but to acquaint you with the tests. If service is required, it should be performed by qualified service personnel.

Self-Tests

The power-up self test is a set of tests that are automatically performed when you apply power to the logic analyzer. You may perform the self tests individually to have a higher level of confidence that the instrument is operating properly. A message that the instrument has failed a test will appear if any problem is encountered during a test. The individual self tests are listed in the self test menu which is accessed via the I/O menu. The HP 1650B/51B self tests are on the operating system disk and the disk is required to run the tests.

Power-Up Self-Test

The power-up self test is automatically initiated at power-up by the HP 1650B/51B Logic Analyzer. The revision number of the operating system firmware is given in the upper right of the screen during the power-up self test. As each test is completed, either "passed" or "failed" will be displayed before the name of the test as shown.

PERFORMING POWER-UP SELF TESTS

passed ROM test
passed RAM test
passed Interrupt test
passed Display test
passed Keyboard test
passed Acquisition test
passed Threshold test
passed Disk test

LOADING SYSTEM FILE

As indicated by the last message, the HP 1650B/51B will automatically load the operating system from the disk in the disk drive. If the operating system disk is not in the disk drive, the message "SYSTEM DISK NOT FOUND" will be displayed at the bottom of the screen and "NO DISK" will be displayed in front of disk test in place of "passed."

If the "NO DISK" message appears, insert the operating system disk into the disk drive, and press any front-panel key.

Selectable Self Tests

Seven self tests may be accessed individually in the Self

Test menu. The seven selectable self tests are:

- Data Acquisition
- RS-232C
- External Trigger BNCs
- Keyboard
- RAM
- ROM
- Disk Drive
- Cycle through all tests

To select a test, place the cursor on the test name and press SELECT. A pop-up menu appears with a description of the test. The self test does not begin until the cursor is placed on Execute and the SELECT key is pressed.

When the test is complete, either "Passed","Failed", or "Tested" will be displayed in the Self Test menu in front of the test. These tests are also used as troubleshooting aids. If a test fails, refer to Section 6 of the Service manual for information on the individual tests used for troubleshooting.

D

Specifications and Operating Characteristics

Introduction

This appendix lists the specifications, operating characteristics, and supplemental characteristics of the HP 1650B and HP 1651B Logic Analyzers.

Specifications

Probes

Minimum Swing: 600 mV peak-to-peak.

Threshold Accuracy:

Voltage	Range Accuracy
− 2.0 V to + 2.0 V	+ 150 mV
− 9.9 V to - 2.1 V	+ 300 mV
+ 2.1 V to + 9.9 V	− 300 mV

State Mode

Clock Repetition Rate: Single phase is 35 MHz maximum (25 MHz on the HP 1651B). With time or state counting, minimum time between states is 60 ns. Both mixed and demultiplexed clocking use master-slave clock timing; master clock must follow slave clock by at least 10 ns and precede the next slave clock by 50 ns.

Clock Pulse Width: ≥ 10 ns at threshold.

Setup Time: Data must be present prior to clock transition, ≥ 10 ns.

Hold Time: Data must be present after rising clock transition; 0 ns.

Data must be present after falling clock transition, 0 ns (HP 1651B); data must be present after falling L clock transition, 0 ns (HP 1650B); data must be present after falling J, K, M, and N clock transition, 1 ns (HP 1650B).

Timing Mode

Minimum Detectable Glitch: 5 ns wide at the threshold.

Characteristics

Probes

Input RC: 100 kΩ ±2% shunted by approximately 8 pF at the probe tip.

TTL Threshold Preset: + 1.6 volts.

ECL Threshold Preset: − 1.3 volts.

Threshold Range: −9.9 to + 9.9 volts in 0.1 V increments.

Threshold Setting: Threshold levels may be defined for pods 1 and 2 individually (HP 1651B). Threshold levels may be defined for pods 1, 2, and 3 individually and one threshold may be defined for pods 4 and 5 (HP 1650B).

Minimum Input Overdrive: 250 mV or 30% of the input amplitude whichever is greater.

Maximum Voltage: ±40 volts peak.

Dynamic Range: ±10 volts about the threshold.

Measurement Configurations

Analyzer Configurations:

Analyzer 1	Analyzer 2
Timing	Off
Off	Timing
State	Off
Off	State
Timing	State
State	Timing
State	State
Off	Off

Channel Assignment: Each group of 16 channels (a pod) can be assigned to Analyzer 1, Analyzer 2, or remain unassigned. The HP 1650B contains 5 pods; the HP 1651B contains 2 pods.

State Analysis

Memory

Data Acquisition: 1024 samples/channel.

Trace Specification

Clocks: Five clocks (HP 1650B) or two clocks (HP 1651B) are available and can be used by either one or two state analyzers at any time. Clock edges can be ORed together and operate in single phase, two phase demultiplexing, or two phase mixed mode. Clock edge is selectable as positive, negative, or both edges for each clock.

Clock Qualifier: The high or low level of four ORed clocks (HP 1650B) or one clock (HP1651B) can be ANDed with the clock specification. Setup time: 20 ns; hold time: 5 ns.

Pattern Recognizers: Each recognizer is the AND combination of bit (0, 1, or X) patterns in each label. Eight pattern recognizers are available when one state analyzer is on. Four are available to each analyzer when two state analyzers are on.

Range Recognizers: Recognizes data which is numerically between or on two specified patterns (ANDed combination of 0s and/or 1s). One range term is available and is assigned to the first state analyzer turned on. The maximum size is 32 bits.

Qualifier: A user-specified term that can be anystate, nostate, a single pattern recognizer, range recognizer, or logical combination of pattern and range recognizers.

Sequence Levels: There are eight levels available to determine the sequence of events required for trigger. The trigger term can occur anywhere in the first seven sequence levels.

Branching: Each sequence level has a branching qualifier. When satisfied, the analyzer will restart the sequence or branch to another sequence level.

Occurrence Counter: Sequence qualifier may be specified to occur up to 65535 times before advancing to the next level.

Storage Qualification: Each sequence level has a storage qualifier that specifies the states that are to be stored.

Enable/Disable: Defines a window of post-trigger storage. States stored in this window can be qualified.

Prestore: Stores two qualified states that precede states that are stored.

Tagging

State Tagging: Counts the number of qualified states between each stored state. Measurement can be shown relative to the previous state or relative to trigger. Maximum count is 4.4 X (10 to the 12th power).

Time Tagging: Measures the time between stored states, relative to either the previous state or the trigger. Maximum time between states is 48 hours.

With tagging on, the acquisition memory is halved; minimum time between states is 60 ns.

Symbols

Pattern Symbols: User can define a mnemonic for the specific bit pattern of a label. When data display is SYMBOL, mnemonic is displayed where the bit pattern occurs. Bit pattern can include 0s, 1s, and don't cares.

Range Symbols: User can define a mnemonic covering a range of values. Bit pattern for lower and upper limits must be defined as a pattern of 0s and 1s. When data display is SYMBOL, values within the specified range are displayed as mnemonic ± offset from base of range.

Number of Pattern and Range Symbols: 200 total. Symbols can be down-loaded over RS-232C.

Timing Analysis

Transitional Timing Mode

Sample is stored in acquisition memory only when the data changes. A time tag stored with each sample allows reconstruction of waveform display. Time covered by a full memory acquisition varies with the number of pattern changes in the data.

Sample Period: 10 ns.

Maximum Time Covered by Data: 5000 seconds.

Minimum Time Covered by Data: 10.24 µs.

Glitch Capture Mode

Data sample and glitch information stored every sample period.

Sample Period: 20 ns to 50 ms in a 1-2-5 sequence dependent on sec/div and delay settings.

Memory Depth: 512 samples/channel.

Time Covered by Data: Sample period × 512.

Waveform Display

Sec/div: 10 ns to 100 s; 0.01% resolution.

Delay: − 2500 s to 2500 s; presence of data dependent on the number of transitions in data between trigger and trigger plus delay (transitional timing).

Accumulate: Waveform display is not erased between successive acquisitions.

Overlay Mode: Multiple channels can be displayed on one waveform display line. Primary use is to view summary of bus activity.

Maximum Number of Displayed Waveforms: 24

Channel-to-Channel Skew: 4 ns typical.

Time Interval Accuracy: ± (sample period + channel-to-channel skew + 0.01% of time interval reading).

Trigger Specification

Asynchronous Pattern: Trigger on an asynchronous pattern less than or greater than specified duration. Pattern is the logical AND of specified low, high, or don't care for each assigned channel. If pattern is valid but duration is invalid, there is a 20 ns reset time before looking for patterns again.

Greater Than Duration: Minimum duration is 30 ns to 10 ms with 10 ns or 0.01% resolution, whichever is greater. Accuracy is + 0 ns to − 20 ns. Trigger occurs at pattern + duration.

Less Than Duration: Maximum duration is 40 ns to 10 ms with 10 ns or 0.01% resolution, whichever is greater. Pattern must be valid for at least 20 ns. Accuracy is + 20 ns to − 0 ns. Trigger occurs at the end of the pattern.

Glitch/Edge Triggering: Trigger on glitch or edge following valid duration of asynchronous pattern while the pattern is still present. Edge can be specified as rising, falling or either. Less than duration forces glitch and edge triggering off.

Measurement and Display Functions

Autoscale (Timing Analyzer Only)

Autoscale searches for and displays channels with activity on the pods assigned to the timing analyzer.

Acquisition Specifications

Arming: Each analyzer can be armed by the run key, the other analyzer, or the external trigger in port.

Trace Mode: Single mode acquires data once per trace specification; repetitive mode repeats single mode acquisitions until stop is pressed or until time interval between two specified patterns is less than or greater than a specified value, or within or not within a specified range. There is only one trace mode when two analyzers are on.

Labels

Channels may be grouped together and given a six character name. Up to 20 labels in each analyzer may be assigned with up to 32 channels per label. Primary use is for naming groups of channels such as address, data, and control busses.

Indicators

Activity Indicators: Provided in the Configuration, State Format and Timing Format menus for identifying high, low, or changing states on the inputs.

Markers: Two markers (X and 0) are shown as dashed lines on the Timing Waveforms display.

Trigger: Displayed as a vertical dashed line in the timing waveform display and as line 0 in the state listing display.

Marker Functions

Time Interval: The X and 0 markers measure the time interval between one point on a timing waveform and trigger, two points on the same timing waveform, two points on different waveforms, or two states (time tagging on).

Delta States (State Analyzer Only): The X and 0 markers measure the number of tagged states between one state and trigger, or between two states.

Patterns: The X and 0 markers can be used to locate the nth occurrence of a specified pattern before or after trigger, or after the beginning of data. The 0 marker can also find the nth occurrence of a pattern before or after the X marker.

Statistics: X to 0 marker statistics are calculated for repetitive acquisitions. Patterns must be specified, for both markers and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum X to 0 time, maximum X to 0 time, average X to 0 time, and ratio of valid runs to total runs.

Run/Stop Functions

Run: Starts acquisition of data in specified trace mode.

Stop: In single trace mode or the first run of a repetitive acquisition, STOP halts acquisition and displays the current acquisition data. For subsequent runs in repetitive mode, STOP halts acquisition of data and does not change current display.

Data Display/Entry

Display Modes: State listing State waveform; State chart; State compare; timing waveforms; interleaved, time- correlated listing of two state analyzers (time tagging on); time- correlated state listing and timing waveform display (state listing in upper half, timing waveform in lower half, and time tagging on).

Timing Waveform: Pattern readout of timing waveforms at X or 0 marker.

Bases: Binary, Octal, Decimal, Hexadecimal, ASCII (display only) and User-defined symbols.

State Compare Mode

Performs post-processing bit-by-bit comparison of the acquired state data and compare data image.

Compare Image. Created by copying a state acquisition into the compare image buffer. Allows editing of any bit in the compare image to a 1, 0, or don't care.

Compare Image Boundaries. Each channel (column) in the compare image can be enabled or disabled via bit masks in the compare image. Upper and lower ranges of states (rows) in the compare image can be specified. Any data bits that do not fall within the enabled channels and the specified range are not compared.

Stop Measurement. Repetitive acquisitions may be halted when the comparison between the current state acquisition and the current compare image is equal or not equal.

Displays. Compare Listing display shows the compare image and bit masks. Difference Listing display highlights differences between the current state acquisition and the current compare image.

State X-Y Chart Display

Plots value of specified label (on y-axis) vs. states or another label (on x-axis). Both axes can be scaled by the user.

Markers. Correlated to state listing, state compare, and state waveform displays. Available as pattern, time or statistics (with time counting on), and states (with state counting on).

Accumulate. Chart display is not erased between successive acquisitions.

State Waveform Display

Displays state acquisition in waveform format.

States/div. 1 to 104.

Delay. 0 to 1024.

Accumulate. Waveform display is not erased between successive acquisitions.

Overlay Mode. Multiple channels can be displayed on one waveform display line. Primary use is to view summary of bus activity.

Maximum Number of Displayed Waveforms. 24.

Markers. Correlated to state listing, state compare, and state chart displays. Available as pattern, time or statistics (with time counting on), and states (with state counting on).

Operating Environment

Temperature: Instruments, 0° to 55° C (+ 32° to 131° F); probes and cables, 0° to 65° C (+ 32° to 149° F). Recommended temperature range for disk media, 10° to 50° C (+ 50° to 122° F).

Humidity: Instruments up to 95% relative humidity at + 40° C; (104° F). Recommended humidity range for disk media, 8% to 80% relative humidity at + 40° C (+ 104° F).

Altitude: To 4600 m (15,000 ft).

Vibration

Operating: Random vibration 5-500 Hz, 10 minutes per axis, ≈ 2.41 g (rms).

Non-operating: Random vibration 5-500 Hz, 10 minutes per axis, ≈ 2.41 g (rms); and swept sine resonant search, 5-500 Hz 0.75 g (0-peak), 5 minute resonant dwell @ 4 resonances per axis.

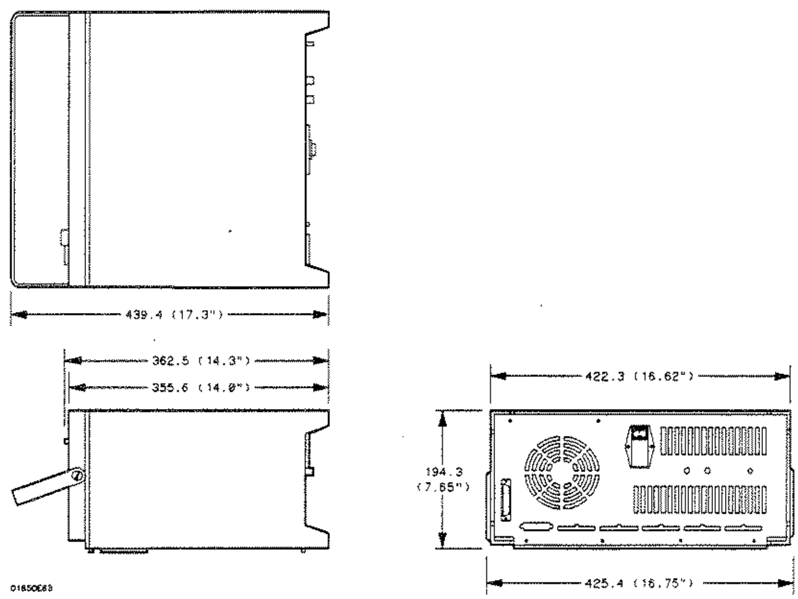
Weight: 10.0 kg (22 lbs) net; 18.2 kg (40 lbs) shipping.

Power: 115V/230V, 48-66 Hz, 200 W_{max}.

Dimensions

Notes: 1. Dimensions are for general information only. If dimensions are required for building special enclosures, contact your HP field engineer.

2. Dimensions are in millimeters and (inches).



E

Microprocessor Specific Measurements

Introduction

This appendix contains information about the optional accessories available for microprocessor specific measurements. In-depth measurement descriptions are included in the operating notes that come with each of these accessories. The accessories you will be introduced to in this appendix are the preprocessor modules and the HP 10269C General Purpose Probe Interface.

Microprocessor Measurements

A preprocessor module enables you to quickly and easily connect the logic analyzer to your microprocessor under test. Most of the preprocessor modules require the HP 10269C General Purpose Probe Interface. The preprocessor descriptions in the following sections indicate which preprocessors require it.

Included with each preprocessor module is a 3.5-inch disk which contains a configuration file and an inverse assembler file. When you load the configuration file, it configures the logic analyzer for making state measurements on the microprocessor for which the preprocessor is designed. It also loads in the inverse assembler file.

The inverse assembler file is a software routine that will display captured information in a specific microprocessor's mnemonics. The DATA field in the STATE LISTING is replaced with an inverse assembly field (see Figure E-1). The inverse assembler software is designed to provide a display that closely resembles the original assembly language listing of the microprocessor's software. It also identifies the microprocessor bus cycles captured, such as Memory Read, Interrupt Acknowledge, or I/O write.

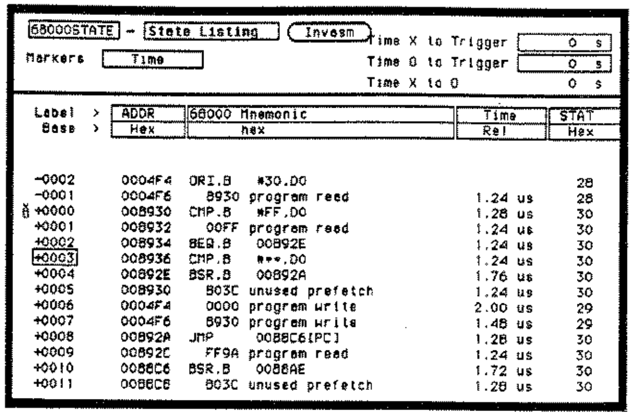


Figure E-1. State Listing with Mnemonics

Microprocessors Supported by Preprocessors

This section lists the microprocessors that are supported by Hewlett-Packard preprocessors and the logic analyzer model that each preprocessor requires. Most of the preprocessors require the HP 10269C General Purpose Probe Interface. The HP 10269C accepts the specific preprocessor PC board and connects it to five connectors on the general purpose interface to which the logic analyzer probe cables connect.

Note

This appendix lists the preprocessors available at the time of printing. However, new preprocessors may become available as new microprocessors are introduced. Check with the nearest Hewlett-Packard sales office periodically for availability of new preprocessors.

Z80

CPU Package: 40-pin DIP

Accessories Required: HP 10300B Preprocessor
HP 10269C General Purpose Probe Interface

Maximum Clock Speed: 10 MHz clock input

Signal Line Loading: Maximum of one 74LS TTL load + 35 pF on any line

Microprocessor Cycles Identified: Memory read/write
I/O read/write
Opcode fetch
Interrupt acknowledge
RAM refresh cycles

Maximum Power Required: 0.3 A at + 5 V dc, supplied by logic analyzer

Logic Analyzer Required: HP 1650B or HP 1651B

Number of Probes Used: Two 16-channel probes

NSC 800

CPU Package: 40-pin DIP

Accessories Required: HP 10303B Preprocessor
HP 10269C General Purpose Probe Interface

Maximum Clock Speed: 4 MHz clock input

Signal Line Loading: Maximum of one HCMOS load + 35 pF on any line

Microprocessor Cycles Identified: Memory read/write
I/O read/write
Opcode fetch
Interrupt acknowledge
RAM refresh cycles
DMA cycles

Maximum Power Required: 0.1A at + 5 V dc, supplied by logic analyzer

Logic Analyzer Required: HP 1650B or HP 1651B

Number of Probes Used: Two 16-channel probes

8085

CPU Package: 40-pin DIP

Accessories Required: HP 10304B Preprocessor
HP 10269C General Purpose Probe Interface

Maximum Clock Speed: 6 MHz clock output (12 MHz clock input)

Signal Line Loading: Maximum of one 74LS TTL load + 35 pF on any line

Microprocessor Cycle Identified: Memory read/write
I/O read/write
Opcode fetch
Interrupt acknowledge

Maximum Power Required: 0.8 A at + 5 V dc, supplied by logic analyzer

Logic Analyzer Required: HP 1650B or HP 1651B

Number of Probes Used: Two 16-channel probes

8086 or 8088

CPU Package: 40-pin DIP

Accessories Required: HP 10305B Preprocessor
HP 10269C General Purpose Probe Interface

Maximum Clock Speed: 10 MHz clock input (at CLK)

Signal Line Loading: Maximum of two 74ALS TTL loads + 40 pF on any line

Microprocessor Cycles Identified: Memory read/write
I/O read/write
Code fetch
Interrupt acknowledge
Halt acknowledge
Transfer to 8087 or 8089 co-processors

Additional Capabilities: The 8086 or 8088 can be operating in Minimum or Maximum modes. The logic analyzer can capture all bus cycles (including prefetches) or can capture only executed instructions. To capture only executed instructions, the 8086or 8088 must be operating in the Maximum mode.

Maximum Power Required: 1.0 A at + 5 V dc, supplied by the logic analyzer

Logic Analyzer Required: HP 1650B

Number of Probes Used: Three 16-channel probes

80186 or 80C186

CPU Package: 68-pin PGA

Accessories Required: HP 10306G Preprocessor

Maximum Clock Speed: 12.5 MHz clock output (25 MHz clock input)

Signal Line Loading: Maximum of 100 kΩ + 18 pF on any line

Microprocessor Cycles Identified:
- Memory read/write (DMA and non-DMA)
- I/O read/write (DMA and non-DMA)
- Code fetch
- Interrupt acknowledge
- Halt acknowledge
- Transfer to 8087, 8089, or 82586 co-processors

Additional Capabilities: The 80186 can be operating in Normal or Queue Status modes. The logic analyzer can capture all bus cycles (including prefetches) or can capture only executed instructions.

Maximum Power Required: 0.08 A at + 5 V dc, supplied by system under test.

Logic Analyzer Required: HP 1650B

Number of Probes Used: Four 16-channel probes

80286

CPU Package: 68-contact LCC or 68-pin PGA

Accessories Required: HP 10312D Preprocessor
HP 10269C General Purpose Probe Interface

Maximum Clock Speed: 10 MHz clock output (20 MHz clock input)

Signal Line Loading: Maximum of two 74ALS TTL loads + 40 pF on any line

Microprocessor Cycles Identified: Memory read/write
I/O read/write
Code fetch
Interrupt acknowledge
Halt
Hold acknowledge
Lock
Transfer to 80287 co-processor

Additional Capabilities: The logic analyzer captures all bus cycles including prefetches

Maximum Power Required: 0.66 A at + 5 V dc, supplied by logic analyzer. 80286 operating current from system under test.

Logic Analyzer Required: HP 1650B

Number of Probes Used: Three 16-channel probes

80386

CPU Package: 132-pin PGA

Accessories Required: HP 10314B Preprocessor
HP 10269C General Purpose Probe Interface

Maximum Clock Speed: 20 MHz clock output (40 MHz clock input)

Signal Line Loading: Maximum of two 74ALS TTL loads + 35 pF on any line

Microprocessor Cycles Identified: Memory read/write
I/O read/write
Code fetch
Interrupt acknowledge, type 0-255
Halt
Shutdown
Transfer to 8087, 80287, or 80387 co-processors

Additional Capabilities: The logic analyzer captures all bus cycles including prefetches

Maximum Power Required: 1.0 A at + 5 V dc, supplied by logic analyzer

Logic Analyzer Required: HP 1650B

Number of Probes Used: Five 16-channel probes

6800 or 6802

CPU Package: 40-pin DIP

Accessories Required: HP 10307B Preprocessor
HP 10269C General Purpose Probe Interface

Maximum Clock Speed: 2 MHz clock input

Signal Line Loading: Maximum of 1 74LS TTL load + 35 pF on any line

Microprocessor Cycle Identified: Memory read/write
DMA read/write
Opcode fetch/operand
Subroutine enter/exit
System stack push/pull
Halt
Interrupt acknowledge
Interrupt or reset vector

Maximum Power Required: 0.8A at + 5 V dc, supplied by logic analyzer

Logic Analyzer Required: HP 1650B or HP 1651B

Number of Probes Used: Two 16-channel probes

6809 or 6809E

CPU Package: 40-pin DIP

Accessories Required: HP 10308B Preprocessor
HP 10269C General Purpose Probe Interface

Maximum Clock Speed: 2 MHz clock input

Signal Line Loading: Maximum of one 74ALS TTL load + 35 pF on any line

Microprocessor Cycles Identified: Memory read/write
DMA read/write
Opcode fetch/operand
Vector fetch
Halt
Interrupt

Additional Capabilities: The preprocessor can be adapted to 6809/09E systems that use a Memory Management Unit (MMU). This adaptation allows the capture of all address lines on a physical address bus up to 24 bits wide.

Maximum Power Required: 1.0 A at + 5 V dc, supplied by logic analyzer

Logic Analyzer Required: HP 1650B or HP 1651B

Number of Probes Used: Two 16-channel probes

68008

CPU Package: 40-pin DIP

Accessories Required: HP 10310B Preprocessor
HP 10269C General Purpose Probe Interface

Maximum Clock Speed: 10 MHz clock input

Signal Line Loading: Maximum of one 74S TTL load + one 74F TTL load + 35 pF on any line

Microprocessor Cycles Identified: User data read/write
User program read
Supervisor read/write
Supervisor program read
Interrupt acknowledge
Bus grant
6800 cycle

Additional Capabilities: The logic analyzer captures all bus cycles including prefetches

Maximum Power Required: 0.4 A at + 5 V dc, supplied by logic analyzer

Logic Analyzer Required: HP 1650B

Number of Probes Used: Three 16-channel probes

68000 and 68010 (64-pin DIP)

CPU Package: 64-pin DIP

Accessories Required: HP 10311B Preprocessor
HP 10269C General Purpose Probe Interface

Maximum Clock Speed: 12.5 MHz clock input

Signal Line Loading: Maximum of one 74S TTL load + one 74F TTL load + 35 pF on any line

Microprocessor Cycles Identified: User data read/write
User program read
Supervisor read/write
Supervisor program read
Interrupt acknowledge
Bus Grant
6800 cycle

Additional Capabilities: The logic analyzer captures all bus cycles including prefetches

Maximum Power Required: 0.4 A at + 5 V dc, supplied by the logic analyzer

Logic Analyzer Required: HP 1650B

Number of Probes Used: Three 16-channel probes

68000 and 68010 (68-pin PGA)

CPU Package: 68-pin PGA

Accessories Required: HP 10311G Preprocessor

Maximum Clock Speed: 12.5 MHz clock input

Signal Line Loading: 100 kΩ + 10 pF on any line

Microprocessor Cycles Identified: User data read/write
User program read
Supervisor read/write
Supervisor program read
Interrupt acknowledge
Bus Grant
6800 cycle

Additional Capabilities: The logic analyzer captures all bus cycles including prefetches.

Maximum Power Required: None

Logic Analyzer Required: HP 1650B

Number of Probes Used: Three 16-channel probes

68020

CPU Package: 114-pin PGA

Accessories Required: HP 10313G

Maximum Clock Speed: 25 MHz clock input

Signal Line Loading: 100 kΩ + 10 pF on any line

Microprocessor Cycles Identified:
- User data read/write
- User program read
- Supervisor read/write
- Supervisor program read
- Bus Grant
- CPU space accesses including:
  - Breakpoint acknowledge
  - Access level control
  - Coprocessor communication
  - Interrupt acknowledge

Additional Capabilities: The logic analyzer captures all bus cycles including prefetches. The 68020 microprocessor must be operating with the internal cache memory disabled for the logic analyzer to provide inverse assembly.

Maximum Power Required: None

Logic Analyzer Required: HP 1650B

Number of Probes Used: Five 16-channel probes

68030 CPU Package: 128-pin PGA

Accessories Required: HP 10316G

Maximum Clock Speed: 25 MHz input

Signal Line Loading: 100 KΩ plus 18 pF on all lines except DSACK0 and DSACK1.

Microprocessor Cycles Identified:
- User data read/write
- User program read
- Supervisor program read
- Bus grant
- CPU space accesses including:
  - Breakpoint acknowledge
  - Access level control
  - Coprocessor communication
  - Interrupt acknowledge

Additional Capabilities: The logic analyzer captures all bus cycles, including prefetches. The 68030 microprocessor must be operating with the internal cache memory and MMU disabled for the logic analyzer to provide inverse assembly.

Maximum Power Required: None

Logic Analyzer Required: HP 1650B

Number of Probes Used: Five 16-channel probes

68HC11

CPU Package: 48-pin dual-in-line

Accessories Required: HP 10315G

Maximum Clock Speed: 8.4 MHz input

Signal Line Loading: 100 KΩ plus 12 pF on all lines.

Microprocessor Cycles Identified:
- Data read/write
- Opcode/operand fetches
- Index offsets
- Branch offsets
- Irrelevant cycles

Additional Capabilities: The 68HC11 must be operating in the expanded multiplexed mode (addressing external memory and/or peripheral devices) for the logic analyzer to provide inverse assembly.

Maximum Power Required: None

Logic Analyzer Required: HP 1650B/51B

Number of Probes Used: Two 16-channel probes for state analysis and one to four for timing analysis.

Loading Inverse Assembler Files

You load the inverse assembler file by loading the appropriate configuration file. Loading the configuration file automatically loads the inverse assembler file.

Selecting the Correct File

Most inverse assembler disks contain more than one file. Each disk usually contains an inverse assembler file for use with the HP 10269C and preprocessor as well as a file for general purpose probing. Each inverse assembler filename has a suffix which indicates whether it is for the HP 10269C and preprocessor or general purpose probing. For example, filename C68000_I indicates a 68000 inverse assembler file for use with the HP 10269C and the 68000 preprocessor. Filename C68000_P is for general purpose probing. Specific file descriptions and recommended usage are contained in each preprocessor operating note.

Loading the Desired File

To load the inverse assembler file you want, insert the 3.5-inch disk you received with your preprocessor in the disk drive. Select the I/O menu. In the I/O menu, select DISK OPERATIONS. The logic analyzer will read the disk and display the disk directory.

Select the Load option and place the filename you want to load in the "from file" box. Place the cursor on Execute and press SELECT.

Place the cursor on the analyzer you want the file loaded into and press SELECT. An advisory "Loading file from disk" is displayed. When the logic analyzer has finished loading the file, you will see "Load operation complete."

The file is now loaded and the logic analyzer is configured for disassembly of acquired data.

Connecting the Logic Analyzer Probes

The specific preprocessor and inverse assembler you are using determines how you connect the logic analyzer probes. Since the inverse assembler files configure the System Configuration, State Format Specification, and State Trace Specification menus, you must connect the logic analyzer probe cables accordingly so that the acquired data is properly grouped for inverse assembly. Refer to the specific inverse assembler operating note for the proper connections.

How to Display Inverse Assembled Data

The specific preprocessor and inverse assembler you are using determines how the inverse assembled data is displayed. When you press RUN, the logic analyzer acquires data and displays the State Listing menu.

The State Listing menu will display as much information about the captured data as possible. For some microprocessors, the display will show a completely disassembled state listing.

Some of the preprocessors and/or the microprocessors under test do not provide enough status information to disassemble the data correctly. In this case, you will need to specify additional information (i.e., tell the logic analyzer what state contains the first word of an opcode fetch). When this is necessary an additional field (INVASM) will appear in the top center of the State Listing menu (see below). This field allows you to point to the first state of an Op Code fetch.

```
[68000STATE] - [State Listing] (Invasm)    Minimum X-O:   0  s
Markers [Statistics]   Valid runs:         Maximum X-O:   0  s
                       16 of 16            Average X-O:   0  s
```

Figure E-2. Inverse Assemble Field

For complete details refer to the Operating Note for the specific preprocessor.

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