MS2602A

SPECTRUM ANALYZER

SERVICE MANUAL
(PART 1)

FIRST EDITION

MEASURING INSTRUMENTS DIVISION
ANRITSU CORPORATION

JUN.
1995

MS2602A
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SERVICE MANUAL (PART 1)

MAY 1993 (FIRST EDITION)

Printed in Japan

WARNING

- *The protective earth terminal of this instrument must be connected to ground. The three-core power cord supplied with the instrument can be plugged into a grounded two pole AC outlet. If no grounded two pole AC outlet is available, the ground pin of the power cord or the earth terminal on the rear panel must be connected to ground before turning on the instrument. Failure to do so could cause dangerous or possibly fatal electric shocks.*
- *Replacing fuses with the power cord still plugged into an AC outlet could also cause electric shocks.*
- ***Meaning of the  on the rear panel:***

  Disassembly, adjustment, maintenance, or other access inside this instrument by unqualified personnel should be avoided. Maintenance of this instrument should be performed only by Anritsu trained service personnel who are familiar with the risks involved of fire and electric shock. Potentially lethal voltages existing inside this instrument, if contacted accidentally, may result in personal injury or death, or in the possibility of damage to precision components.

■ SAFETY CONSIDERATIONS:

Anritsu uses the following labels to identify safety precautions which should be followed to prevent personal injury or product damage. Please familiarize yourself with them before operating this product.

Labels used in this manual:

WARNING : Indicates that the procedure could result in personal injury if not correctly performed. Do not proceed before you fully understand the explanation given with this symbol and meet the required conditions.

CAUTION : Indicates that the operating procedure could result in damage to the product if not correctly performed. Do not proceed before you fully understand the explanation given with this symbol and meet the required conditions.

Note : Indicates that information helpful in understanding the operation of the product is about to be presented.

† : Used to indicate footnotes. Footnotes provide supplementary information other than the WARNING, CAUTION, and Note information mentioned above. Footnotes should always be placed at the bottom of the same page as the words to which they refer. They are usually referenced by either an asterisk (*) or by an asterisk followed by a number. However, since the asterisk is used as part of the GPIB common command in this manual, footnotes are referenced by either a dagger (†) or a dagger followed by a number.

Labels or symbols used on / in the product:

高圧危険
DANGER
HIGH VOLTAGE

: This warning symbol (red color) indicates that the operator should not touch the labeled location. Servicing should only be performed by qualified personnel.

: This symbol indicates hazardous voltages. Be careful (not used in this instrument).

: This international caution symbol indicates that the operator should refer to the operation manual before beginning a procedure.

: This symbol indicates an earth (ground) terminal. The product should be grounded via the earth terminal if a three prong power cord is not used.

CERTIFICATION

ANRITSU CORPORATION certifies that this instrument has been thoroughly tested and inspected, and found to meet published specifications prior to shipping.
Anritsu further certifies that its calibration measurements are based on the Japanese Electrotechnical Laboratory and Radio Research Laboratory standards.

WARRANTY

All parts of this product are warranted by Anritsu Corporation of Japan against defects in material or workmanship for a period of one year from the date of delivery.
In the event of a defect occurring during the warranty period, Anritsu Corporation will repair or replace this product within a reasonable period of time after notification, free-of-charge, provided that: it is returned to Anritsu; has not been misused; has not been damaged by an act of God; and that the user has followed the instructions in the operation manual.

Any unauthorized modification, repair, or attempt to repair, will render this warranty void.

This warranty is effective only for the original purchaser of this product and is not transferable if it is resold.

ALL OTHER EXPRESSED WARRANTIES ARE DISCLAIMED AND ALL IMPLIED WARRANTIES FOR THIS PRODUCT, INCLUDING THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE LIMITED IN DURATION TO A PERIOD OF ONE YEAR FROM THE DATE OF DELIVERY. IN NO EVENT SHALL ANRITSU CORPORATION BE LIABLE TO THE CUSTOMER FOR ANY DAMAGES, INCLUDING LOST PROFITS, OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES, ARISING OUT OF THE USE OR INABILITY TO USE THIS PRODUCT.

All requests for repair or replacement under this warranty must be made as soon as possible after the defect has been noticed and must be directed to Anritsu Corporation or its representative in your area.

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MEMORY BACK-UP BATTERY REPLACEMENT

The power for memory back-up is supplied by a Poly-carbomonofluoride Lithium Battery. This battery should only be replaced by a battery of the same type; since replacement can only be made by Anritsu, contact the nearest Anritsu representative when replacement is required.

STORAGE MEDIUM

This equipment stores data and programs using Plug - in Memory cards (PMC) and backed - up memories. Data and programs may be lost due to improper use or failure. ANRITSU therefore recommends that you back-up the memory.

Storing program is possible only when option 04/05 Personal Test Automation (PTA) is installed.

ANRITSU CANNOT COMPENSATE FOR ANY MEMORY LOSS.

Please pay careful attention to the following points. Do not remove the IC card and backed-up memory from equipment being accessed.

(PMC)

- Isolate the card from static electricity.
- The back-up battery in the card has a limited life; renew the battery periodically.

(Backed-up memory)

- Isolate the memory from static electricity.

Note: *The battery life is about 7 years. Early battery replacement is recommended.*

Note 1:

1. The instrument is operable on a nominal voltage of 100 to 127 Vac or 200 to 250 Vac by changing a slide switch on the Power Supply Unit (Section 2).

   The voltage and current ratings are indicated on the rear panel when the instrument is shipped from the factory.

   To operate on the other voltage, change the slide switch setting. The plate on the rear panel indicating the voltage and current ratings should be changed to the appropriate one. Order the plate from ANRITSU CORPORATION if needed.

2. In this manual, the power supply voltage and current ratings are represented by **Vac and ***A, respectively.

3. The relationship between power supply voltage and current ratings is shown below.

**Vac	***A (Time lag type) for MS2602A
100 to 127 V	6.3 A
200 to 250 V	3.15 A

Part Names & Part Numbers

Please specify the part numbers shown in the parts list when making inquiries or when ordering parts. There may be a difference between the names of parts used in this manual and the parts actually used in the equipment or supplied for repair. This is because equivalent parts with the same functions, performance and reliability as the parts specified in the circuit diagrams and parts list have been used or supplied. Since the parts are equivalent, they have absolutely no adverse effect on the equipment specified functions, performance or reliability.

TABLE OF CONTENTS

SECTION 1
GENERAL

The MS2602A's service manual consists of two parts (Part 1 and Part 2).

Besides,troubleshooting procedure is divided into two steps. One is to locate the faulty unit and to replace it. The other is to repair the faulty unit.

The part 1 is used for the former procedure. And the part 2 is used for the latter procedure.

The part 1 service manual is composed of the following sections.

SECTION 2 CIRCUIT DISCRIPTION

This section describes the operation of each units.

SECTION 3 TROUBLESHOOTING AND ADJUSTMENT

This section describes troubleshooting procedures at unit level.

SECTION 4 OVERALL ADJUSTMENT AND CALIBRATION OF COMPENSATION DATA

This section describes overall adjustment procedure, and how to enter the compensation data for internal characteristics after repair.

SECTION 5 MECHANICAL CONFIGURATION

This section describes the mechanical parts and how to disassemble each unit (Block, PC-board)

Part 2 of the service manual is a non-public document and is for the use of Anritsu's service personnel only.

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SECTION 1
GENERAL

1.1 Product Outline

The MS2602A is a wide-band spectrum analyzer covering a wide frequency range from 100 Hz to 8.5 GHz. This instrument employs a fully-synthesized local oscillator with 1 Hz resolution as a local signal. It therefore provides stable measurement over the entire frequency range, even when a resolution bandwidth of 10 Hz is selected. It also allows sideband noise to be suppressed below −115 dBc / Hz (below 4 GHz frequency, at 50 kHz offset).

This instrument also incorporates a 625 kHz calibration oscillator and a 1 dB step calibration attenuator as an internal calibration signal source. This accurately calibrates switching errors such as linear scale, resolution bandwidth, reference level as well as log scale linearity. This instrument, before delivery from the factory, is set so that the frequency response calibration for data compensation is stored in the EEPROM. This provides a highly accurate level measurement over a wide frequency range.

The MS2602A has not only a rotary knob, TEN (numeric) keys, and step keys for setting measurement conditions, but also a one-touch signal search key to make it easier to observe signals. It is also designed with emphasis placed on the waveform display function, which switches at one-touch from frequency domain to time domain and vice-versa to analyze signals efficiently on both the frequency axis and time axis. The MS2602A also provides a marker function that works with Anritsu's own original zone marker, and a multimarker function that can display up to ten markers simultaneously.

The MEASURE functions of the MS2602A allow various measurements to be made to meet a variety of applications without external calculation. In addition to general measurements such as frequency, noise, etc. this instrument facilitates measurements of radio equipment such as occupied frequency bandwidth and adjacent-channel leakage power. Moreover, the burst average power and burst waveform template measurements make it easier to measure various types of digital mobile communications equipment.

■ Applications

The MS2602A Spectrum Analyzer can be used for a wide range of applications such as development, adjustment, inspection, and maintenance of electronic parts and equipment in the following fields:

- AM / FM radio equipment
- Digital cellular telephone / cordless telephone
- Satellite broadcasting and TV equipment

WA-01
NOISE-GEN

SECTION 2
CIRCUIT DESCRIPTION

2.1 Overall Circuit Description

Please refer to Fig. 2-1 (P2-3) Overall Block Diagram.

The MS2602A is a superheterodyne system scanning-type spectrum analyzer.

In the MS2602A, the input signal route varies according to the measurement frequency range. When the measurement range is in the 0 band (2 GHz max. or 1.7 GHz max. at AUTO band), the input signal is switched to the 2 GHz MIX route. When the measurement range is in bands 1−, and 1+ (1.7GHz min.), the input signal is switched to the 8.5 GHz MIX route.

When the input signal is in band 0 (0 to 2 GHz), the input signal is mixed with the 1st LOCAL signal at the 1st MIXER and is converted to a 2.5214 GHz 1st IF signal.

The 1st IF signal is mixed with the 2nd LOCAL signal at the 2nd MIXER and is converted to a 521.4 MHz 2nd IF signal.

When using the 8.5 GHz MIX and the measurement range is in bands 1− and 1+ (8.5 GHz max.), the input signal is mixed with the 1st LOCAL signal at the 1st MIXER and is converted to a 521.4 MHz 1st IF signal. In this case, the input signal is passed through a YTF *1 (preselector) to drop the image signal.

The 1st and 2nd LOCAL OSC frequencies are stabilized in the PLL (Phase Locked Loop) circuits based on the reference signal supplied by REFERENCE OSC. The SCAN GENERATOR circuit of [SCAN] sweeps the YTO *2 (1st LOCAL OSC) frequency.

The 521.4 MHz 2nd IF signal or the 521.4 MHz signal from the 8.5 GHz MIX is mixed with the 3rd LOCAL signal at the 3rd MIXER and is converted to the 21.4 MHz final IF signal.

The 21.4 MHz IF signal passes through BPFs and variable gain amplifiers of [IF BPF] which determine RBW (resolution bandwidth) and also passes through LOG or LIN amplifiers of [IF LOG/DET] for detection.

The internal calibration signal is used for calibration of LOG LINIARITY, REFERENCE LEVEL (gain error and RBW switching error), and CENTER FREQ (IF BBF tuning error).

The detected signal passes through the VF (Video Filter) and is converted to a digital signal by the A/D converter.

The CPU block is composed of three CPU boards which are [MAIN CPU], [MEAS CPU], and [DISP CPU].

The converted digital signal is processed at [MEAS CPU] and sent to [DISP CPU] via COMMON RAM for display on the CRT.

The data (frequency, reference level value, etc.) entered at the [FRONT PANEL] panel keys is sent to the [MAIN CPU] which controls each unit depending on the data content.

[MAIN CPU] , [MEAS CPU] and [DISP CPU] have each one CPU, and configure the multi-processor system through a common bus and common RAM. (Refer to Fig.2-1) The [INTERFACE (1), INTERFACE (2), or INTERFACE (3)] is connected to the [MAIN CPU] I/O bus. The [FRONT PANEL] is connected with COMMON bus.

Notes: *1 YTF:YIG Tuned Filter
*2 YTO:YIG Tuned Oscillator

·The PMC is connected to COMMON BUS via connectors. Each analog circuit is controlled by the [MEAS CPU].

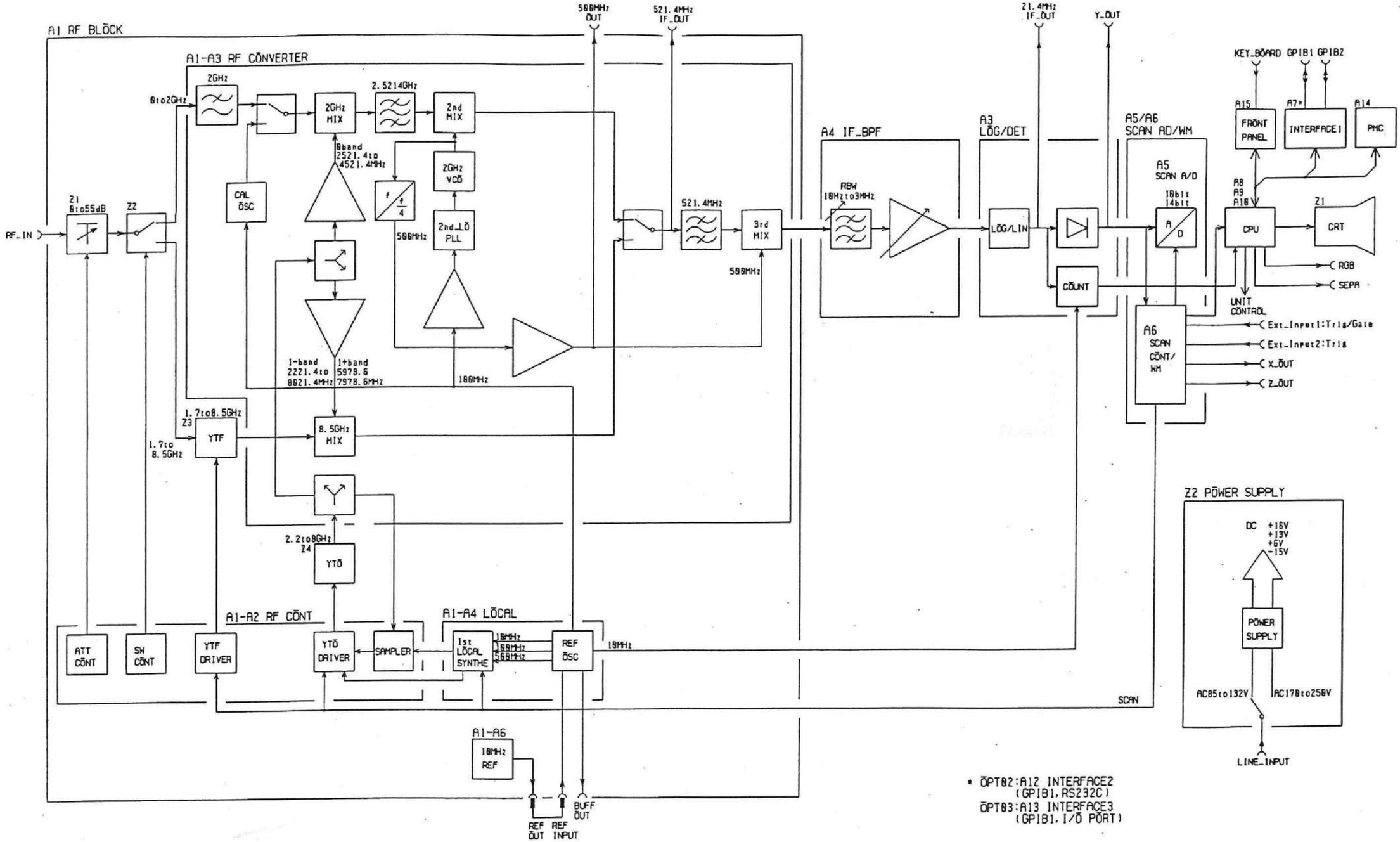

Fig. 2-1 MS2602A Overall Block Diagram

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2.2 A1-A3 RF Converter

2.2.1 2 GHz MIX route

(1) (A1-A3-) Z1 2 GHz LPF

This LPF prevents reception of spurious signals such as image frequencies of the A1-A3-Z2 2 GHz MIXER.

(2) (A1-A3-) A1 SW/EQ

This circuit switches RF signal to 625 kHz CAL signal or vice versa.

(3) (A1-A3-) A6 1st LO AMP

This circuit amplifies the 1st-local signal from the Z4 YTO, and sends it to the Z2 2 GHz MIXER and Z4 8 GHz MIX. YTO stands for YIG tuned oscillator.

(4) (A1-A3-) Z2 2 GHz MIXER

This circuit mixes the input signal with the 1st local signal from A6 1st LO AMP to convert it to a 2.5214 GHz 1st IF signal.

(5) DF

This filter allows only the 2.5214 GHz signal (from the Z2 2 GHz MIXER) to pass through and sends it to the A3 2.5214 GHz IF AMP.

(6) (A1-A3-) A3 2.5214 GHz IF AMP

This circuit amplifies the 1st IF signal.

(7) (A1-A3-) A4 2.5214 GHz BPF

This is the 1st IF BPF that consists of dielectric filters.

Since the signal is converted to 521.4 MHz by the A8 2nd CONVERTER, this filter is designed to suppress the image frequency that is 1042.8 MHz apart from the true frequency.

(8) (A1-A3-) A5 LPF

This LPF prevents generation of spurious signals such as residual responses born from interaction between 1st-local signals (including harmonics) and 2nd-local signals (including harmonics).

(9) (A1-A3-) A8 2nd CONVERTER

The 2nd converter circuit mixes the 2.5214 GHz 1st IF signal with the 2 GHz 2nd-local oscillator signal, and converts it to a 521.4 MHz 2nd IF signal.

(10) (A1-A3-) A7 2 GHz PLL

This block includes the circuit for locking the 2 GHz VCO (2nd local OSC) to 100 MHz Ref OSC signal.

The output of the 2 GHz VCO is passed through a 1/4 divider and compared with the 100 MHz reference signal in Sampling Phase Detector (S.P.D) to create the loop-error voltage which is used for phase locking the 2 GHz VCO.

The output of the 1/4 divider used also for 3rd local OSC (500 MHz).

(11) (A1-A3-) A9 3rd CONVERTER

This circuit includes a switch which switches the input signal between 2 GHz MIX route output (521.4 MHz) and 8 GHz MIX route output (the same 521.4 MHz) .

The 521.4 MHz 2nd-IF signal (1st-IF signal for 1.7 to 8.5 GHz band) is mixed with a 500 MHz 3rd-local oscillator signal (derived from A7 2 GHz PLL), and a 21.4 MHz IF signal is derived.

The 21.4 MHz IF signal is fed to A4 IF BPF UNIT.

(12) (A1-A3-) A10 CAL /CONT

This circuit generates a 625 kHz standard signal which is used for the calibration of the instrument.

The 625 kHz output level is accurately varied during the calibration processing.

2.2.2 8 GHz MIX route

(1) (A1-A3-) Z4 8 GHz MIX

The mixer down-converts the RF input signal to a 521.4 MHz IF signal. The low pass filter prevents the generation of spurious responses.

(2) (A1-A3-) A11 521.4 MHz IF AMP

The 1st IF signal is amplified and fed to A9 3rd converter which is common circuits for 2 GHz MIX route output and 8 GHz MIX route output.

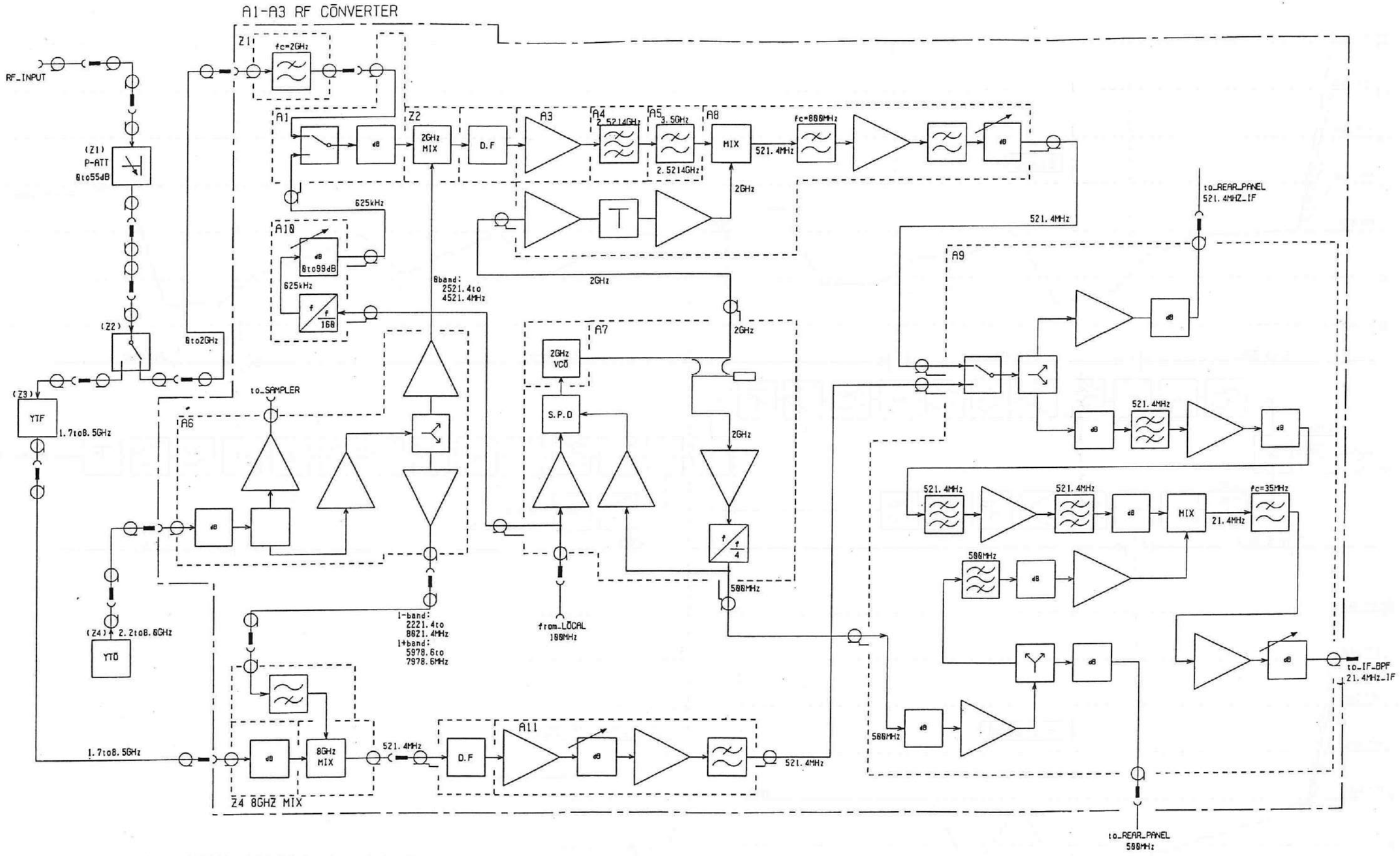


Fig. 2-2 A1-A3 RF CONVERTER Block Diagram

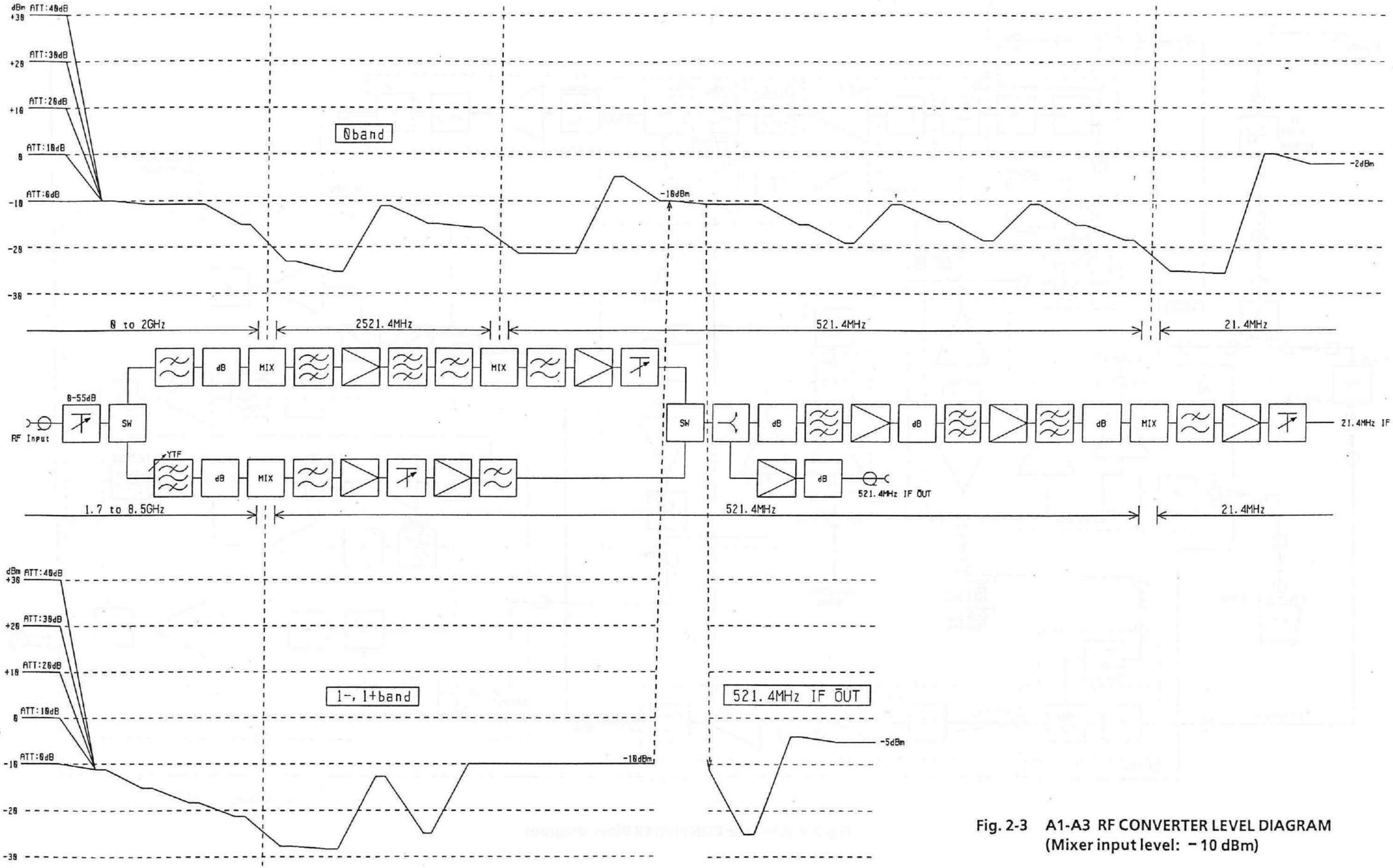


Fig. 2-3 A1-A3 RF CONVERTER LEVEL DIAGRAM
(Mixer input level: −10 dBm)

2.3 A1-A4 LOCAL

MS2602A utilizes "LOCK & SWEEP" technique to generate the 1st local frequency signal. This local signal is used to convert the RF input frequency to a suitable fixed IF frequency (2521.4 MHz for 0 to 2 GHz band and 521.4 MHz for 1.7 GHz to 8.5 GHz frequency band.

1st local start frequency = RF input start freq + 2521.4 MHz for Band 0 (0 to 2 GHz)

1st local start frequency = RF input start freq + 521.4 MHz for Band 1 − (1.7 to 7.5 GHz)

1st local start frequency = RF input start freq − 521.4 MHz for Band 1 + (2.2 to 8.5 GHz)

The above calculation gives the start frequency at which the YTO is locked. Similarly it is possible to obtain the 1st local stop frequency. If the difference between the 1st local stop frequency and 1st local start frequency is greater than 1 MHz, the YTO is first locked at the start frequency and then rolled in the required frequency span. If the above difference is less than or equal to 1 MHz, the YTO frequency is forced to be changed while remaining in the locked state.

Eg: For RF start frequency of 4 GHz (Band 1−) and span 1 MHz

1st local start frequency = 4000 + 521.4 = 4521.4 MHz

1st local stop frequency = 4001 + 521.4 = 4522.4 MHz

Hence the 1st local frequency span being 1 MHz, the YTO frequency is moved in the locked state by moving the REFERENCE frequency of the YTO PLL.

Eg: For RF start frequency of 4 GHz (Band 1−) and span 2.5 MHz

1st local start frequency = 4000 + 521.4 = 4521.4 MHz

1st local stop frequency = 4002.5 + 521.4 = 4523.9 MHz

Hence the 1st local frequency span being greater than1 MHz, the YTO frequency is first locked at the start frequency 4521.4 MHz and then rolled in the 2.5 MHz frequency span.

How YTO locking is obtained (Corresponding circuits on A1-A2-A1 RF CONT 1 + A1-A2-A3 SAMPLER)

A1-Z4 YTO is brought near the required 1st local frequency by applying a tuning voltage by means of a D/A network (two 12-bit D/A for tuning 2000 to 8050 MHz, thus giving a tuning constant of 1 MHz/bit). The YTO is locked by placing it in a Phase Locked Loop (PLL) whose reference frequency is synthesized so as to make sure that the YTO output frequency is equal to the pre-decided (calculated) frequency.

Since the YTO being a current tuning oscillator (200 MHz/mA tuning constant), a loop error voltage to current converter (YTO drive circuit) is used. To reduce the frequency band of the synthesized reference and synthesized sampling signal, a polarity reversal technique is used at the loop filter output. In the sampler, the frequency-down conversion occurs so as to ensure.

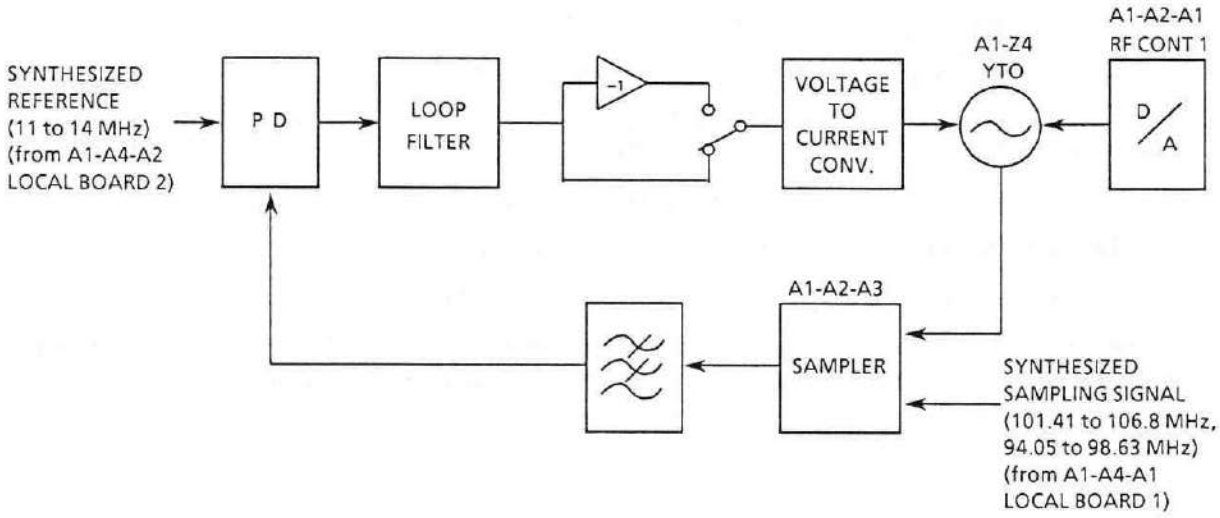


Fig. 2-4 YTO PLL Loop

How 1st local frequency span greater than 1 MHz is obtained. (Related circuit is on A1-A2-A1 RF CONT 1)

At first, the YTO is locked at the 1st local starting frequency as explained above. After achiving the locking, the loop error voltage is held in a capacitor by using a Sample/Hold (S/H) integrated circuit (IC). In this time, the phase-locked loop is opened. Then a sweep signal of appropriate level is applied to the YTO to make it swing through the required frequency span.

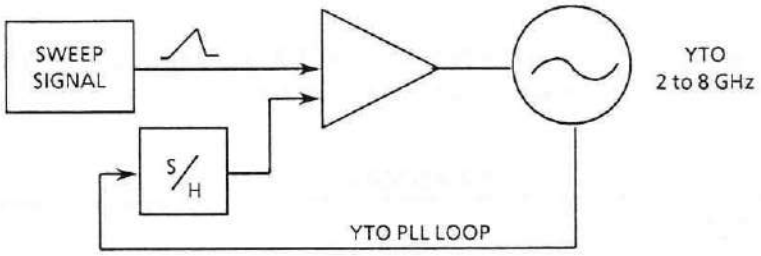


Fig. 2-5

How the synthesized reference synthesized sampling signals are generated. (Using A1-A4-A1 LOCAL BOARD 1 + A1-A4-A2 LOCAL BOARD 2)

The frequency of synthesized reference signal and synthesized sampling signal are calculated by MS2602A's CPU by an algorithem as shown in page 2-16 to 2-18 and thereby the required frequency output of each voltage controlled oscillator (VCO) is decided. A 1 Hz step synthesizer controls the last four digits (0 Hz to 9999 Hz of the 1st local start frequency expressed in terms of Hz, while next two digits (10 kHz to 990 kHz) are taken care of by 10 kHz step synthesizer and the next two (1 MHz to 99 MHz) are managed by 1 MHz step synthesizer. Their combining relationship is shown in Table 2-1.

Incidentally, sweep signal is applied to 10 kHz SYNTHE when SPAN is 1.00 MHz to 10.1 kHz, and is applied to 1 Hz SYNTHE when span is 10 kHz to 100 Hz.

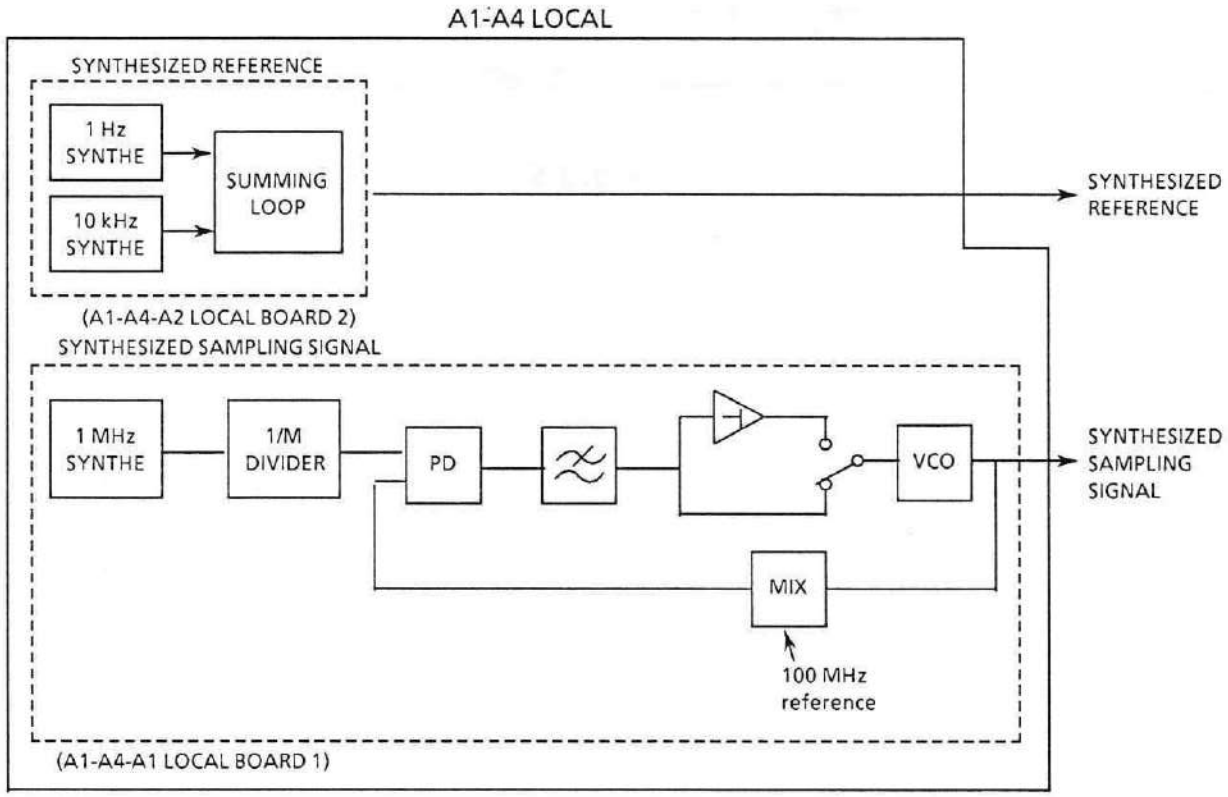


Fig. 2-6 Simplified Block Diagram of A1-A4 LOCAL

Table 2-1 The relationship between the frequency of YTO (f_{YTO}) and the frequency of synthesized sampling signal (f_{SAMPL}).

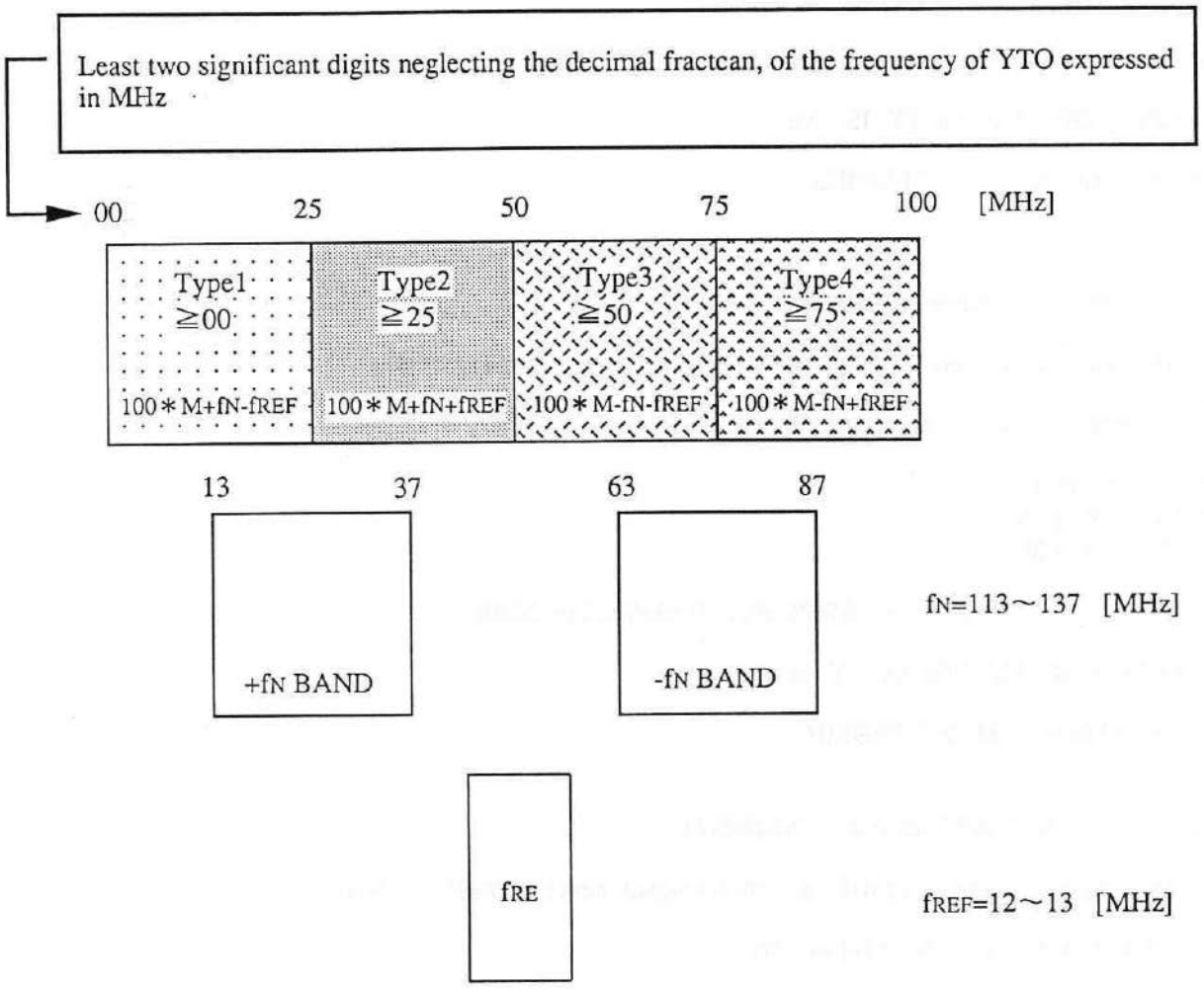
TYPE	f_{YTO} [MHz]		f_{REF} [MHz]	M	f_N [MHz]	f_{SAMPL} [MHz]
(1)	$100*M+f_N-f_{REF}$	$100*M+f_N$	$-f_{REF}$			$100+f_N/M$
	2200 to 2201	2213	13 to 12	21	113	105.3809524
	2224 to 2225	2237	13 to 12	21	137	106.5238095
(2)	$100*M+f_N+f_{REF}$	$100*M+f_N$	$+f_{REF}$			$100+f_N/M$
	2225 to 2226	2213	12 to 13	21	113	105.3809524
	2249 to 2250	2237	12 to 13	21	137	106.5238095
(3)	$100*M-f_N-f_{REF}$	$100*M-f_N$	$-f_{REF}$			$100-f_N/M$
	2250 to 2251	2263	13 to 12	24	137	94.291667
	2274 to 2275	2287	13 to 12	24	113	95.291667
(4)	$100*M-f_N+f_{REF}$	$100*M-f_N$	$+f_{REF}$			$100-f_N/M$
	2275 to 2276	2263	12 to 13	24	137	94.291667
	2299 to 2300	2287	12 to 13	24	113	95.291667
(1)	$100*M+f_N-f_{REF}$	$100*M+f_N$	$-f_{REF}$			$100+f_N/M$
	2300 to 2301	2313	13 to 12	22	113	105.1363636
	2324 to 2325	2337	13 to 12	22	137	106.2272727
(2)	$100*M+f_N+f_{REF}$	$100*M+f_N$	$+f_{REF}$			$100+f_N/M$
	2325 to 2326	2313	12 to 13	22	113	105.1363636
	2349 to 2350	2337	12 to 13	22	137	106.2272727
(3)	$10*M-f_N-f_{REF}$	$100*M-f_N$	$-f_{REF}$			$100-f_N/M$
	2350 to 2351	2363	13 to 12	25	137	94.52
	2374 to 2375	2387	13 to 12	25	113	95.48
(4)	$100*M-f_N+f_{REF}$	$100*M-f_N$	$+f_{REF}$			$100-f_N/M$
	2375 to 2376	2363	12 to 13	25	137	94.52
	2399 to 2400	2387	12 to 13	25	113	95.48
(1)	$100*M+f_N-f_{REF}$	$100*M+f_N$	$-f_{REF}$			$100+f_N/M$
	2400 to 2401	2413	13 to 12	23	113	104.9130435
	2424 to 2425	2437	13 to 12	23	137	105.9565217
(2)	$100*M+f_N+f_{REF}$	$100*M+f_N$	$+f_{REF}$			$100+f_N/M$
	2425 to 2426	2413	12 to 13	23	113	104.9130435
	2449 to 2450	2437	12 to 13	23	137	105.9565217

Table 2-1 The relationship between the frequency of YTO (f_{YTO}) and the frequency of synthesized sampling signal (f_{SAMPL}). (Continued)

TYPE	f_{YTO} [MHz]		f_{REF} [MHz]	M	f_N [MHz]	f_{SAMPL} [MHz]
(1)	$100*M+f_N-f_{REF}$	$100*M+f_N$	$-f_{REF}$			$100+f_N/M$
	7800 to 7801	7813	13 to 12	77	113	101.4675325
	7824 to 7825	7837	13 to 12	77	137	101.7792208
(2)	$100*M+f_N+f_{REF}$	$100*M+f_N$	$+f_{REF}$			$100+f_N/M$
	7825 to 7826	7813	12 to 13	77	113	101.4675325
	7849 to 7850	7837	12 to 13	77	137	
(3)	$100*M-f_N-f_{REF}$	$100*M-f_N$	$-f_{REF}$			$100-f_N/M$
	7850 to 7851	7863	13 to 12	80	137	98.2875
	7874 to 7875	7887	13 to 12	80	113	98.5875
(4)	$100*M-f_N+f_{REF}$	$100*M-f_N$	$+f_{REF}$			$100-f_N/M$
	7875 to 7876	7863	12 to 13	80	137	98.2875
	7899 to 7900	7887	12 to 13	80	113	98.5875
(1)	$100*M+f_N-f_{REF}$	$100*M+f_N$	$-f_{REF}$			$100+f_N/M$
	7900 to 7901	7913	13 to 12	78	113	101.4487179
	7924 to 7925	7937	13 to 12	78	137	101.7564103
(2)	$100*M+f_N+f_{REF}$	$100*M+f_N$	$+f_{REF}$			$100+f_N/M$
	7925 to 7926	7913	12 to 13	78	113	101.4487179
	7949 to 7950	7937	12 to 13	78	137	101.7564103
(3)	$100*M-f_N-f_{REF}$	$100*M-f_N$	$-f_{REF}$			$100-f_N/M$
	7950 to 7951	7963	13 to 12	81	137	98.308642
	7974 to 7975	7987	13 to 12	81	113	98.604938
(4)	$100*M-f_N+f_{REF}$	$100*M-f_N$	$+f_{REF}$			$100-f_N/M$
	7975 to 7976	7963	12 to 13	81	137	98.308642
	7999 to 8000	7987	12 to 13	81	113	98.604938

There are four expressions for the YTO frequency (f_{YTO}) depends on the types of the frequency synthesis.

Type 1 : 100 * M+f_N-f_{REF}
Type 2 : 100 * M+f_N+f_{REF}
Type 3 : 100 * M-f_N-f_{REF}
Type 4 : 100 * M-f_N+f_{REF}



The method for calculating f_{SAMPL} frequency from f_{YTO}.

eg(1) f_{YTO}=2460.8MHz(case≧50M, MODE (3))

0.8MHz part comes from 12MHz to 13MHz signal hence f_{REF}=12.2MHz

$f_{YTO}=100*M-f_N-f_{REF}$ but f_{REF}=12.2

2460.8MHz=100 * M-f_N-12.2
2473MHz=100 * M-f_N
f_N=100 * M-2473

but f_N=113～137[MHz] → M=26 then f_N=127 (2600-2473)

SAMPLE OSC POLARITY IS - ive

$f_{SAMPLE}=100-f_N/M$=95.1154MHz

eg(2) f_{YTO}=2731.4MHz(case≧25, MODE (2))

0.4MHz part comes from 12MHz to 13MHz signal hence f_{REF}=12.4MHz

$f_{YTO}=100*M+f_N+f_{REF}$ but f_{REF}=12.4

2731.4=100 * M+f_N+12.4
2719=100 * M+f_N
f_N=2719-100 * M

but f_N=113～137[MHz] → M=26 then f_N=119 (2719-2600)

SAMPLE OSC PLL POLARITY IS + ive

$f_{SAMPLE}=100+f_N/M$=104.5769MHz

eg(3) f_{YTO}7987.36MHz(case≧75, MODE(4))

0.36MHz part comes from 12MHz to 13MHz signal hence f_{REF}=12.36MHz

$f_{YTO}=100*M-f_N+f_{REF}$ but f_{REF}=12.36

7987.36MHz=100 * M-f_N+12.36MHz
7975MHz=100 * M-f_N
f_N=100 * M-7975

but f_N=113～137[MHz] → M= 81 then f_N=125(8100-7975)

SAMPLE OSC PLL POLARITY IS - ive

$f_{SAMPLE}=100-f_N/M$=98.4568MHz

The expression of synthesized reference signal frequency.

$f_{REF}=f_{10kHz\ VCO}/10+f_{1Hz\ VCO}/1000$ [MHz]
($f_{SUMVCO}=f_{10kHz\ VCO}+f_{1Hz\ VCO}$)

The method for calculating the frequency of the 10kHz VCO, the 1kHz VCO, and the Summing VCO, from f_{YTO}.
The frequency of synthesized sampling signal(f_{SAMPLE}) is the one-tenth of f_{SUMVCO}

10kHz VCO=117.8～127.7MHz ; 1Hz VCO=220～230MHz

fyto in MHz=XXXX · $\underbrace{Y_6 Y_5}\ \underbrace{Z_4 Z_3 Z_2 Z_1}$ MHz

$Y_6Y_5/10=FK$ $\quad \frac{Z_4Z_3Z_2Z_1}{1000}=FH$

Type(1) & Type(3)
10kHz VCO=(127.7-FK)MHz
1Hz VCO =(230-FH)MHz

Type(2) & Type(4)
10kHz VCO=(117.7+FK)MHz
1Hz VCO =(220+FH)MHz

} Polarity same as YTO PLL Polarity

Now consider the previous 3 examples

eg(1) f_{YTO}=2460.8MHz, f_{REF}=12.2MHz

$FK=\frac{80}{10}=8$ $\quad FH=\frac{0000}{1000}=0$

Type(3)hence 10kHz VCO=127.7-FK=119.7MHz
1Hz VCO=230-FH=230MHz

Sum VCO=10kHz VCO+ $\frac{\text{1Hz VCO}}{100}$ =122MHz

eg(2) f_{YTO}=2731.4MHz, f_{REF}=12.4MHz

$$FK=\frac{40}{10}=\underline{4} \qquad FH=\frac{0000}{1000}=\underline{0}$$

Type(2)hence 10kHz VCO=117.8+4=<u>121.8MHz</u>
1Hz VCO=220+0=<u>220MHz</u>

$$\text{Sum VCO=10kHz VCO+}\frac{\text{1Hz VCO}}{100}=\underline{124MHz}$$

eg(3) f_{YTO}=7987.36MHz, f_{REF}=12.36MHz

$$FK=\frac{36}{10}=3.6 \qquad FH=\frac{0000}{1000}=0$$

Type(4)hence 10kHz VCO=117.8+4=<u>121.8MHz</u>
1Hz VCO=220+0=<u>220MHz</u>

$$\text{Sum VCO=10kHz VCO+}\frac{\text{1Hz VCO}}{100}=\underline{123.6MHz}$$

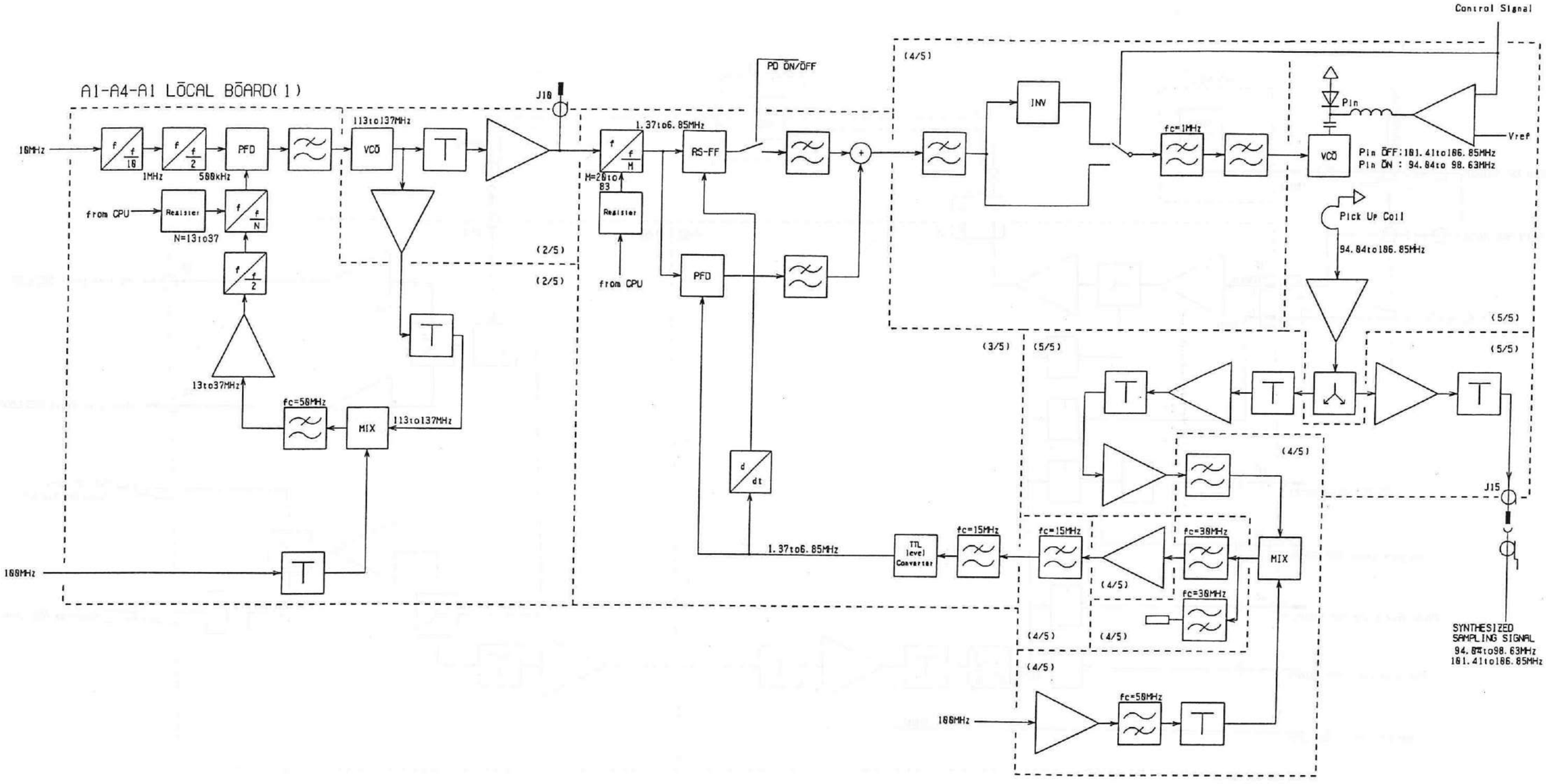


Fig. 2-7 (1/2) A1-A4-A1 LOCAL BOARD 1 Block Diagram

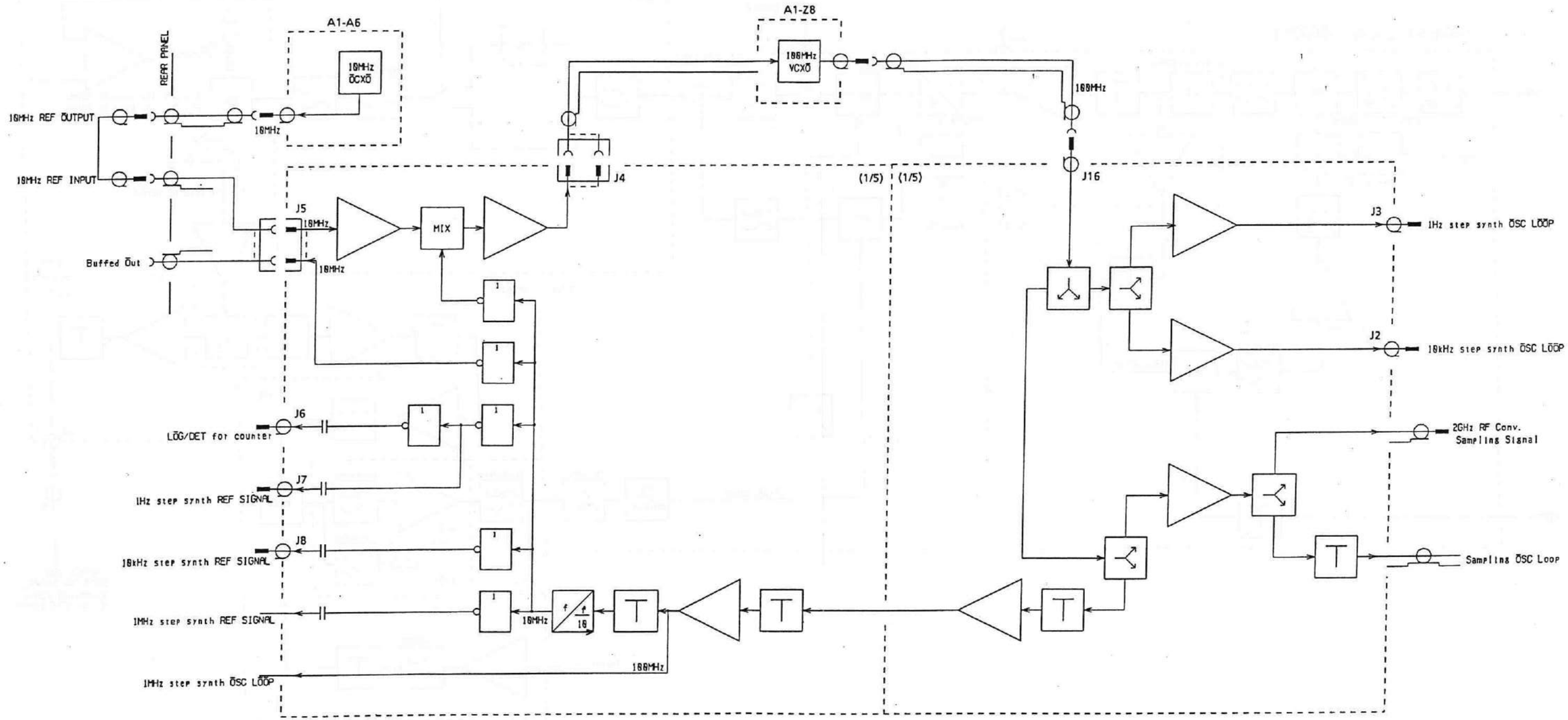
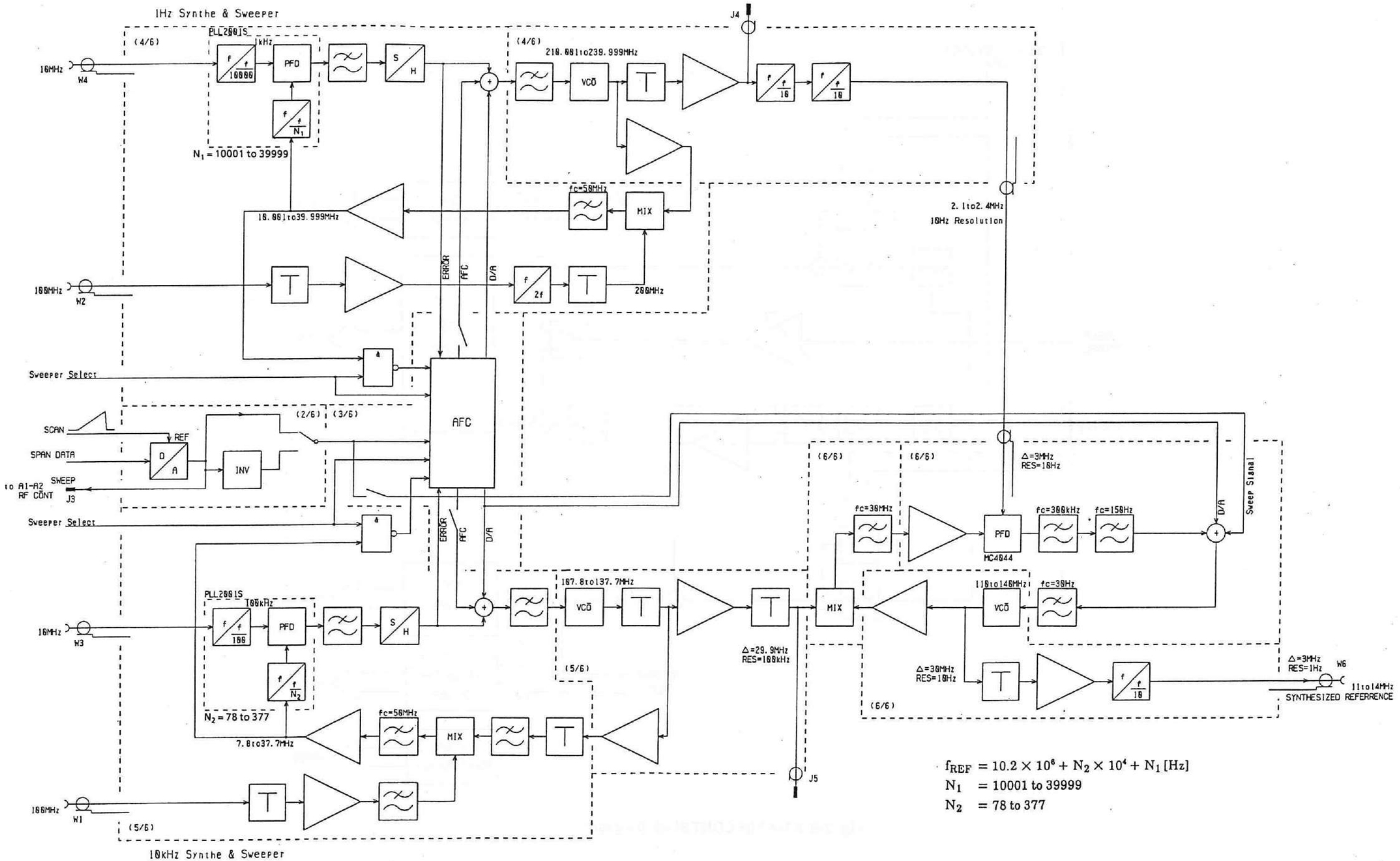


Fig. 2-7 (2/2) A1-A4-A1 LOCAL BOARD 1 Block Diagram



$$f_{REF} = 10.2 \times 10^6 + N_2 \times 10^4 + N_1 \text{ [Hz]}$$
$$N_1 = 10001 \text{ to } 39999$$
$$N_2 = 78 \text{ to } 377$$

Fig. 2-8 A1-A4-A2 LOCAL BOARD Block Diagram

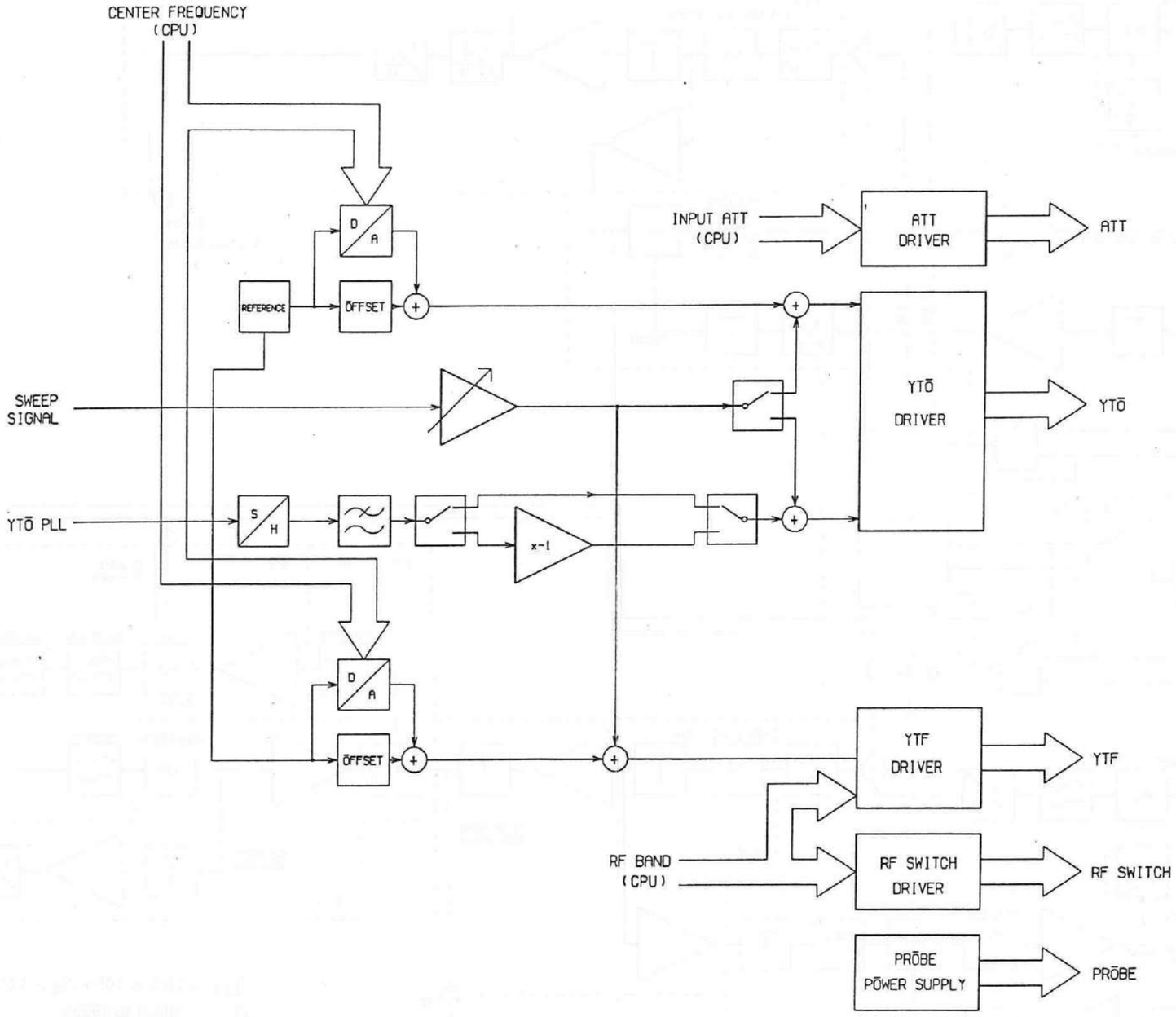


Fig. 2-9 A1-A2 RF CONT Block Diagram

2.4 A4 IF BPF

This block determines the amplifier gain in accordance with the reference level, and RBW.

(a) Switching section

When the RBW is 30 kHz max., the 21.4 MHz IF signal from the [RF CONVERTER] is sent to STEP AMP&BPF (1) via the frequency converter; when the RBW is 100 kHz min., is sent directly to the STEP AMP&BPF (2).

(b) Frequency converter

When the RBW is 30 kHz max., the 21.4 MHz signal is converted to 450 kHz by the 20.95 MHz LOCAL signal and then it is sent to STEP AMP&RPF (1). After it has passed through STEP AMP&BPF (1), it is reconverted to the 21.4 MHz IF signal again and sent to STEP AMP&BPF (2).

(c) STEP AMP&BPF (1)

This is composed of a 3-stage step amplifier and 5-stage bandpass filter.

The STEP AMP is composed of a 2-stage 0/10 dB STEP AMP and a 1-stage 0/10/20 STEP AMP and the gain is changed according to the reference level and RF ATT.

The bandpass filter circuit composition is changed according to the RBW. When the RBW is 300 kHz max., a crystal filter is inserted; when it is 1 kHz min., it becomes an LC filter.

The principle of the 1 kHz to 30 kHz LC filters is described below.

The signal V is supplied to the high-Q LC parallel resonance circuit via the variable resistance R as shown below.

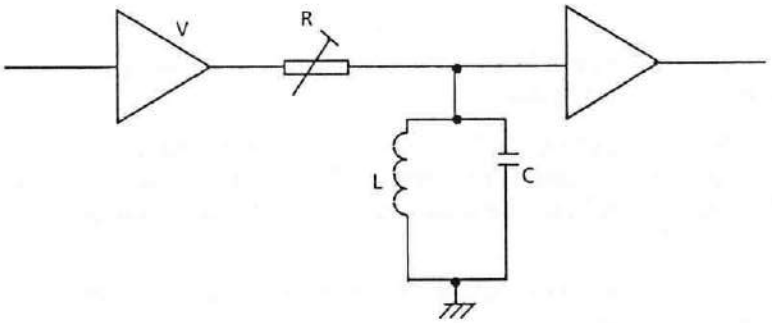


Fig. 2-10 Principle of LC Filter

Tht signal V is divided by the variable resistance R and the LC resonator because the input impedance of the buffer amplifier is high. If the L and C are ideal elements without any loss, the impedance of the LC resonator will be infinity at the resonance frequency, and the signal will be transmitted without any loss regardless of value R. When the frequency separates from the resonance frequency, the impedance of the resonator becomes small and the transmission loss becomes large because the signal V is divided by R. Therefore, when R becomes large, the BPF bandwidth becomes small and is controlled by the value R.

The principle of the 10 Hz to 300 Hz crystal filter is described below.

The crystal filter is composed of C1, which cancels the parastic capacity such as the parallel capacity of crystal X1 and the output buffer amplifier, and the resonance circuits L and C2 as shown below.

By this parastic capacity cancellation, the equivalent circuit becomes the LC-series resonance circuit as shown below.

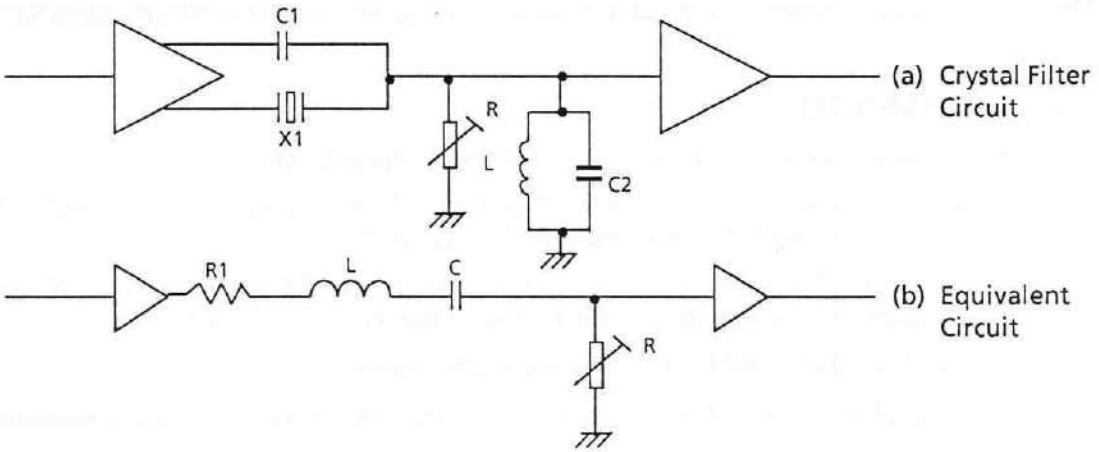


Fig. 2-11 Principle of Crystal Filter

If the crystal equivalent resistance is small enough and the buffer amplifier input impedance is high, the transmission loss is negligible.

When the signal frequency separates from the resonance frequency, the impedance of the crystal resonator becomes high and the signal is divided by R so that the transmission loss becomes large. Therefore, when R becomes small, the bandpass-filter bandwidth becomes small and the bandwidth is controlled by the value R.

In the actual circuit, the resonance circuit for crystal-filter parastic capacity cancelling is the same as the LC-filter resonance circuit.

Also, since neither the LC-filter circuit nor the crystal-filter circuit is an ideal resonance circuit, the loss changes when the bandwidth (RBW) is switched. The amplifier gain is changed by the switch circuit to reduce the deviation when the RBW is switched.

(d) STEP AMP&BPF (2)

This block is composed of a 5-stage STEP AMP and a 4-stage (RBW 100 kHz min.) bandpass filter.

The STEP AMP is composed of a 3-stage 10/20 dB STEP AMP, a 1-stage 4/8 dB STEP AMP and a 1-stage 1/2/3 dB STEP AMP, and the gain is changed according to the reference level and RF ATT. The bandpass filter is composed of an LC filter. The operation principles are the same as the STEP AMP&BPF (1).

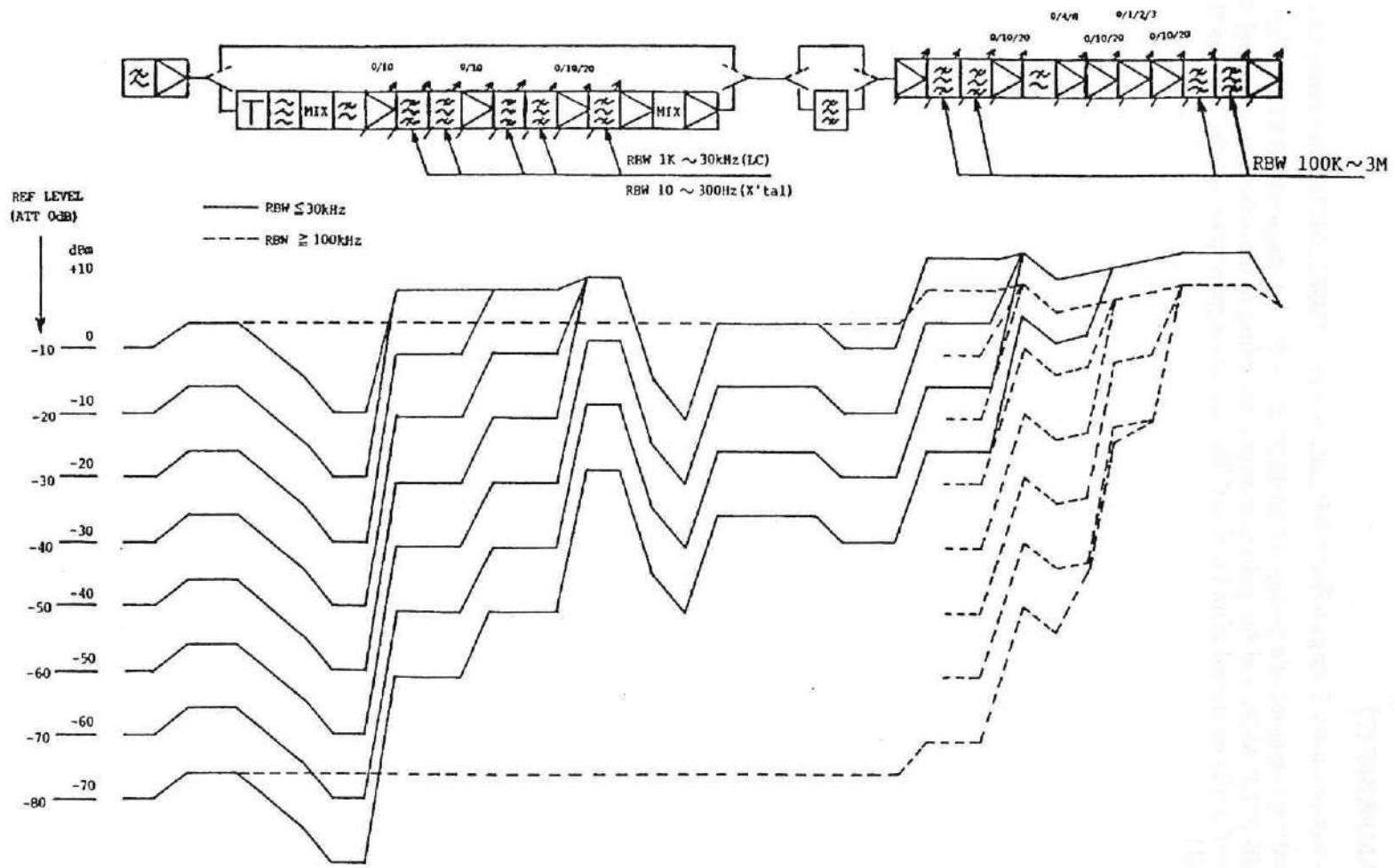


Fig. 2-12 MS2602A IF BPF Level Diagram

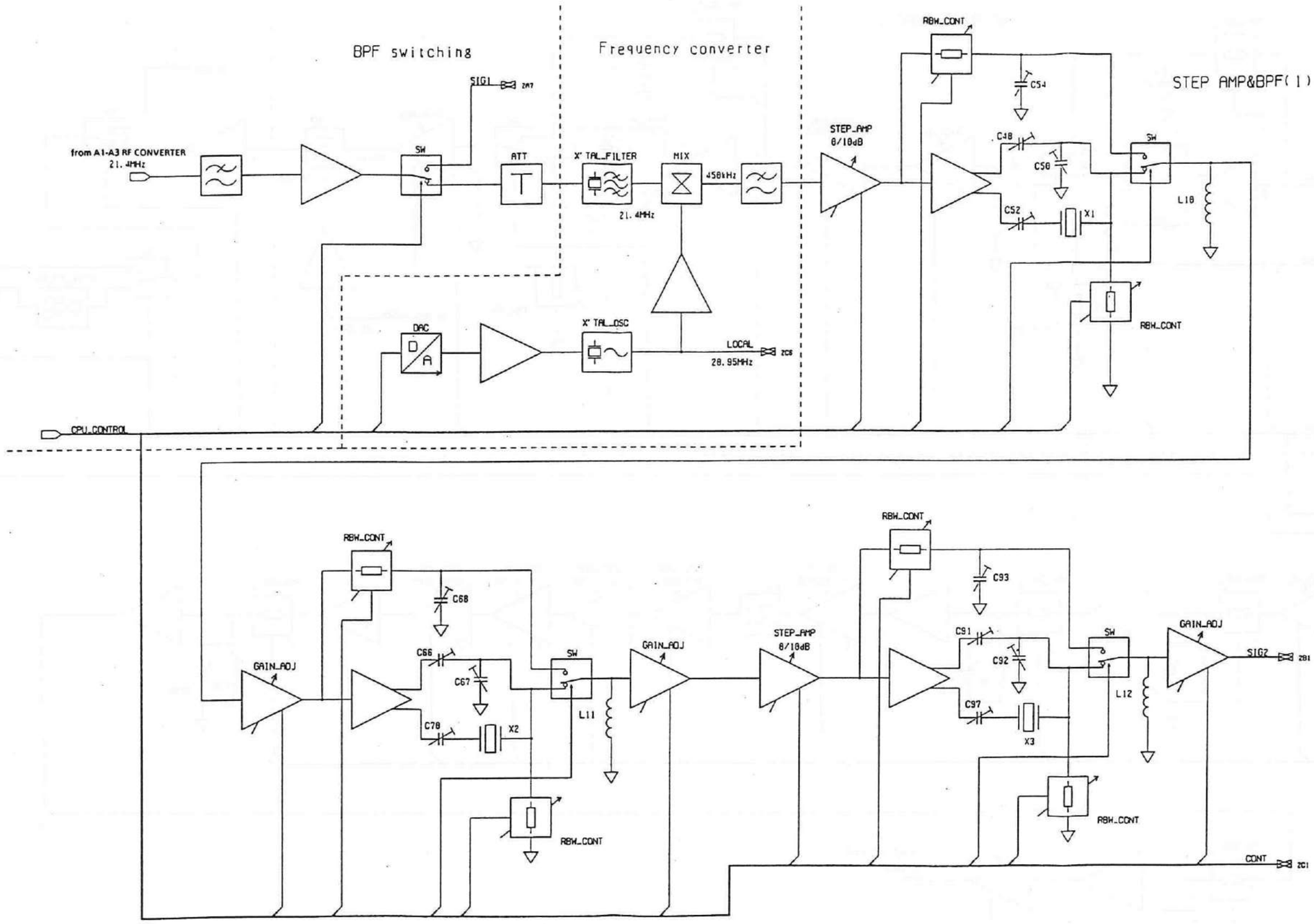


Fig. 2-13 (1/2) A4 IF BPF Block Diagram

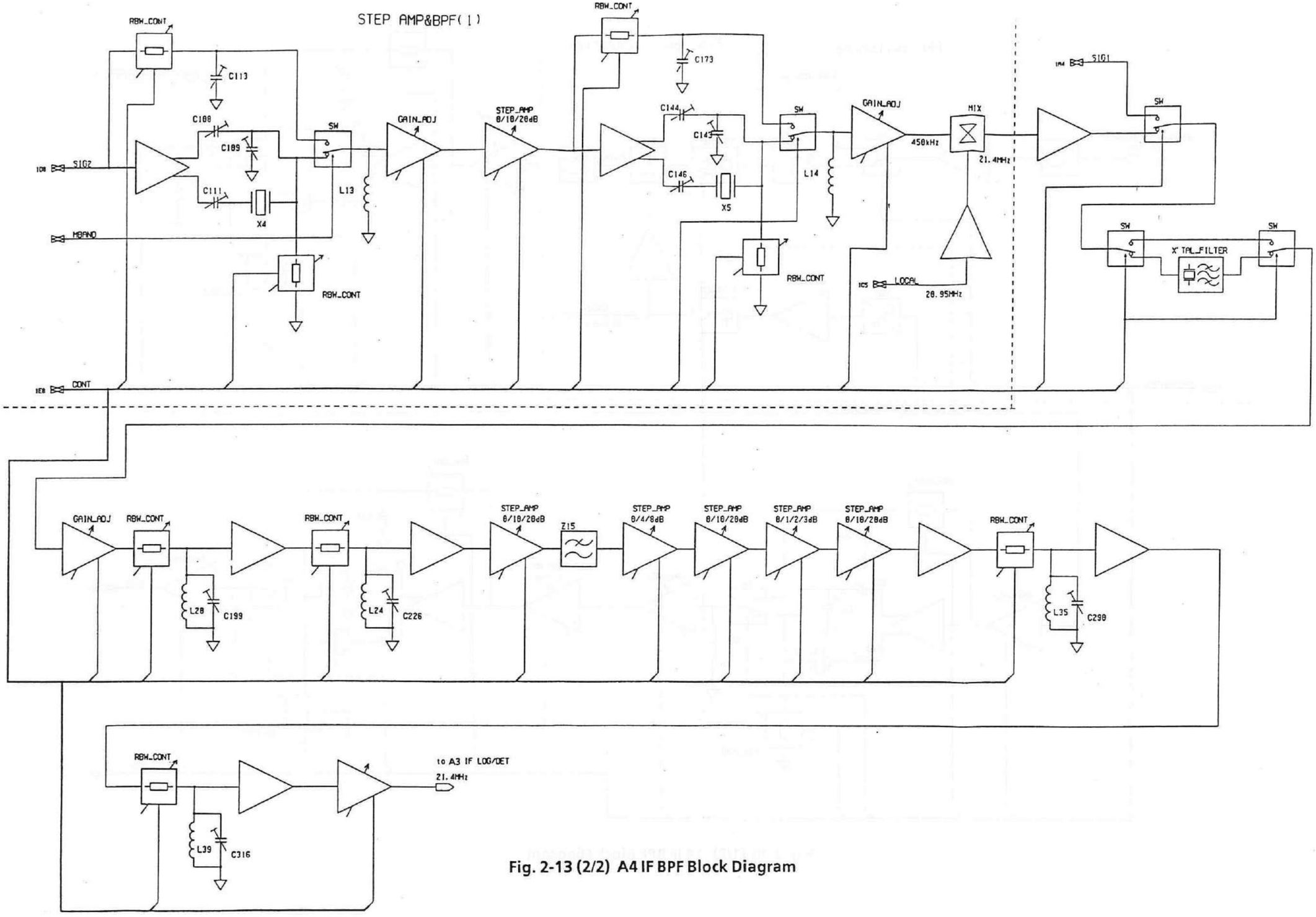


Fig. 2-13 (2/2) A4 IF BPF Block Diagram

2.5 A3 IF LOG/DET

After A3 LOG/DET has log-compressed the 21.4 MHz signal from A4 IF BPF with the LOG/LIN amplifier, it is detected by the envelope detector. After the detected signal has been passed through the video filter (LPF), it is sent to A5 SCAN/AD to be converted to a digital signal by the A/D converter.

In addition, the frequencyof the IF signal referenced to 21.4 MHz is converted to a voltage by two FM demodulators. When "FM MONITOR" function key is selected in time domain mode (zero span mode), this signal is sent to the A/D converter instead of the envelope detector output. Thus, the display which has a vertical axis of frequency deviation referenced to the center frequency and a horizontal axis of time can be obtained.

The envelope detector output and FM demodulator output are used also for "SOUND MONITOR".

Incidentally, the IF signal is counted by counter circuit. The count signal is generated by dividing the 10 MHz. The frequency of required spectrum is obtained by calculating the combination of this counter circuit output (IF frequency) and local frequency.

(a) LOG/LIN AMP

LOG/LIN AMP is composed of a 9-stage log-compression amplifier with a gain of approx. 12 dB at each stage. The LOG scale has a dynamic range of 100 dB min.

In the LIN mode, the last two stages operate as a linear amplifier and the other stages operate as a gain-1 amplifier.

(b) Detector

The 21.4 MHz signal that has passed through the LOG/LIN AMP is full-wave rectified and converted to a DC voltage.

(c) Video filter

This is a cut-off frequency variable RC-type LPF.

(d) FM demodulator

Demodulator 1 has wide frequency range but less sensitive. So sensitive demodulator 2 is also provided, of which reference frequency is 10.7 MHz and act as 21.4 MHz referenced demodulator preceded by a frequency halver.

(Blank)

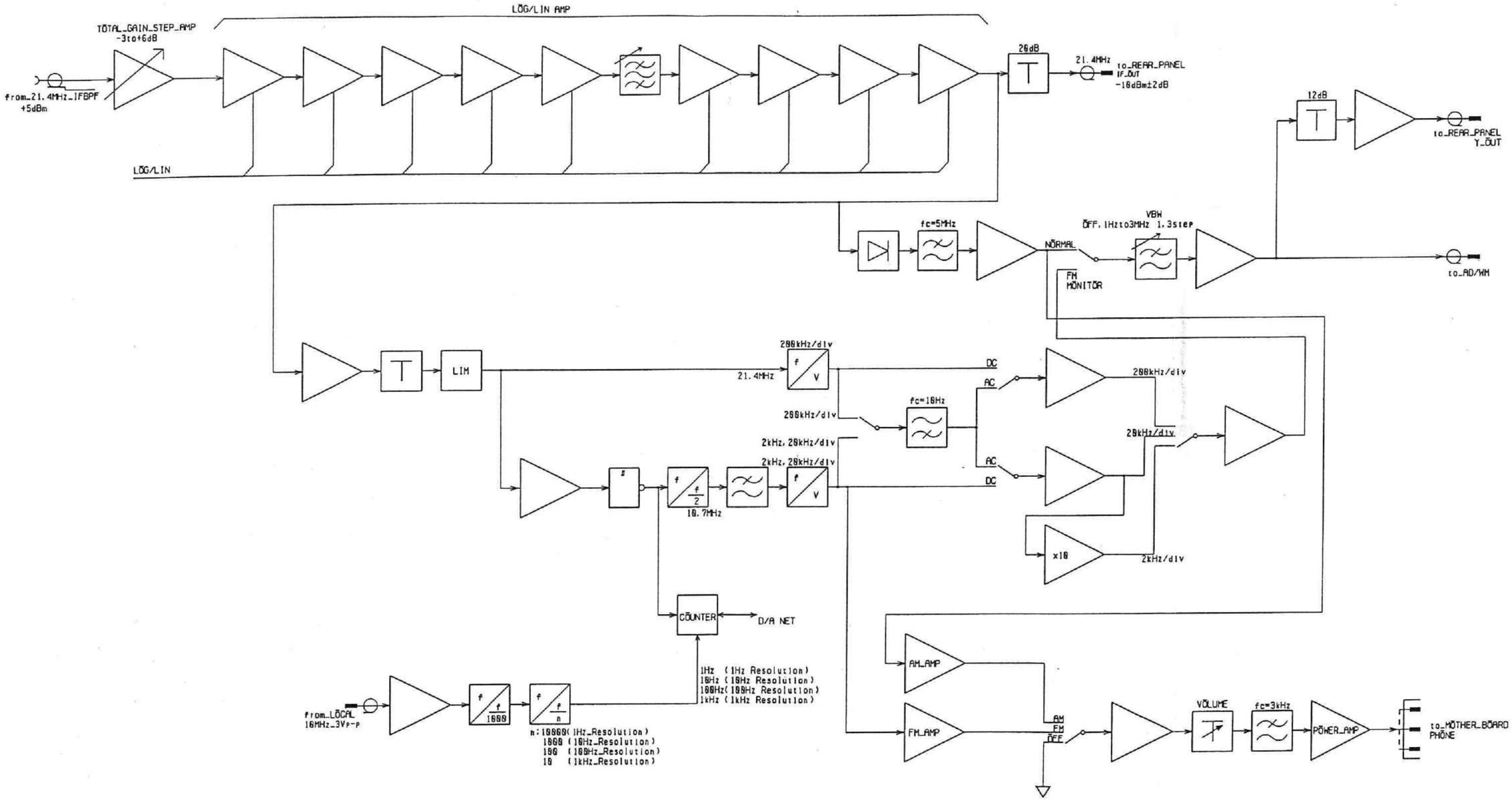


Fig. 2-14 A3 IF LOG/DET Block Diagram

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2.6 SCAN BLOCK

Scan signal and sampling signal generator, A/D converter, Wave Memory for sampled data, and their related circuits are implemented in A5 SCAN/AD and A6 SCAN CONT/WM.

A5 SCAN/AD includes A/D converter trigger circuit and sweep signal generator which is controlled by A6 SCAN CONT/WM. The sweep signal generator which is used for sweeping the LOCAL frequency also generates count up signal.

This count up signal is sent to A6 SCAN CONT/WM to generates the sampling signal and next address signal which are used for sampling the A/D converter in A5 SCAN/AD. When sweep time is greater than or equal to 50ms, 14bit A/D converter is used. Contrary, when sweep time is less than 50ms, 10 bit A/D converter is used. Sampled data are sent for A6 SCAN CONT/WM and stored in WAVE MEMORY.

The address of the Wave Memory is set by Wave Memory Address Counter which counts up the Wave Memory Clock signal. This clock signal and the write pulse for Wave Memory are made from sampling signal.

In time domain (zero span) mode, TIME BASE signal instead of COUNT UP signal is used for make sampling signal.

Incidentally, pre and post trigger control circuits consists of pre point counter and trig int delay circuits are included in A6 SCAN CONT/WM. Gate signal generator is also included in A6 SCAN CONT/WM.

2.6.1 A5 SCAN/AD

(a) Sweep signal generator

This circuit operates when the display mode is not TIME. It generates a saw-tooth wave by charging current to a capacitor with a charge time that corresponds to the sweep time. This signal, on which the SPAN voltage for sweeping the LOCAL frequency is created, is supplied to A1-A4-A2 LOCAL BOARD (2). The SPAN frequency is changed by varying the D/A converter output voltage.

(b) X address·counter

X address corresponds to the data-point number on the screen horizontal axis. It is set by the sampling clock count at the counter as described below. The counter output is input to the D/A converter and this output becomes the X-SCAN signal. When the display mode is not TIME, the sweep signal voltage and the X-SCAN voltage are compared by the comparator and the output becomes the sampling clock. This clock is counted at the counter and the counter output is sent to the D/A converter; the X-SCAN signal voltage is increased at each count and the next clock is generated by comparison with the sweep signal. This operation is repeated until the stop point counter in A6 SCAN CONT/WM output the SWEEP END signal.

(c) Trigger

The trigger can be performed by the detection signal from A3 IF LOG/DET, LINE signal or an external input signal. A reference signal correspoinding to the trigger level is created by the D/A converter and this is compared with the input signal by the comparator. The comparator output is logic-converted by the rising and falling edge of the trigger and output to become the CPU interrupt signal.

(d) A/D converter

When sweep time is greater than or equal to 50 ms the 14-bit A/D converter is used. Contraly, when sweep time is less than 50 ms, the 10-bit A/D converter is used. The PEAK HOLD and DIP HOLD circuits precedes the 14-bit A/D converter. The PEAK HOLD and DIP HOLD circuits save the maximum and minimum value, respectively, of the detected signal between each sampling point.

The converted digital data is sent to A6 SCAN CONT/WM.

The A/D control circuits generate the PEAK/DIP HOLD detection-circuit reset signal, the A/D start signal and channel-switching signal at 2ch-sweep based on the sampling clock.

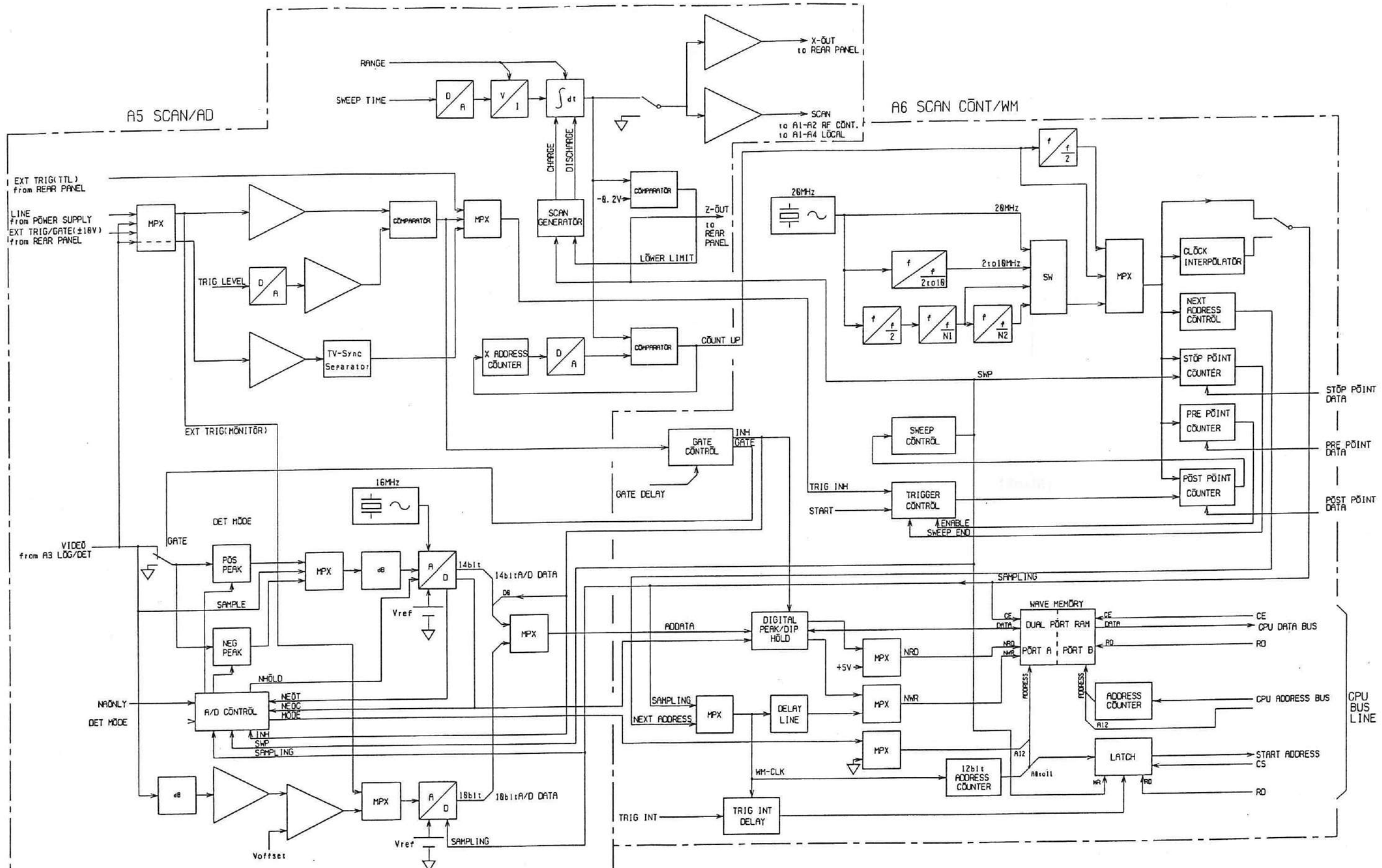

Fig. 2-15 A5 SCAN/AD, A6 SCAN CONT/WM Block Diagram

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2.6.2 A6 SCAN CONT/WM (Wave Memory)

(a) Clock generator

When the display mode is TIME, the clock generator outputs the sampling clock based on the signal which is made by dividing the 20 MHz quartz crystal oscillator.

(b) Sampling clock generator

The sampling clock and the clock address signal are generated based on the X-address-counter comparator output and the clock generated by the clock generator.

When the sweep time is more than 200 ms, the clock interval time becomes long, the voltage holding time (in the A5 SCAN/AD PEAK-HOLD/DIP-HOLD) becomes long, and then the measurement error is increased. To suppress the measurement error, the sampling clock becomes the signal with the clock inserted in the basic clock signal interval.

(c) GATE signal generator

When the burst-signal ON/OFF control signal is input externally, the INHIBIT signal synchronized to the sampling clock is output to the CPU. The CPU does not display the data on the screen when the INHIBIT signal is L level.

(d) Wave Memory

This Wave Memory (WM) stores the data which are sampled at A/D converters. The "MEASURE CPU" reads the data from this WM and transfer them to the "DISP CPU" after processing. The writing and reading are not synchronized. In gate mode, during the gate period which is designated by gate delay and gate length referenced to gate trigger, "PERMIT" symbol is stamped on least significant bit of each address's data. Contrary, "INHIBIT" symbol is stamped on to the data except gate period. The "DISP CPU" doesn't display the "INHIBIT" stamped data.

2.7 Digital Section

2.7.1 A8 MEAS CPU

(1) Composition

The A8 MEAS CPU block composition is shown below.

- CPU (MC68000, 12 MHz)

  This executes the program in the ROM and performs the processes for contorlling the measurement system and fetching the measurement data.

- ROM (4 Mbits × 1)

  This ROM contains the firmware program.

- RAM (4 Mbits × 1)

  This RAM contains the various types of data required by the CPU to execute the program.

- Measurement system controller LSI (ASIC)

  The "analog" units in the MS2602A are controlled by A8 MEAS CPU. Another words, A8 MEAS CPU and the "analog units" in the MS2602A makes the "measurement system".

  This application-specific LSI functions as a master for controlling the measurement system.

  The same LSI (slave) is also used on the "analog unit" side. The master and slave communicate data serially.

- Common bus interface circuit

  This is the common bus interface circuit for sending and receiving data to/from other CPUs via the common memory on the A14 PMC BOARD.

- EEPROM (64 kbits × 1)

  This ROM stores the system calibration data of the MS2602A.

(2) Outline of functions

The A8 MEAS CPU function is divided into the following main 2 functions.

① Controlling measurement system

② Fetching and calculating measurement data

The principles of operation for these functions are explained as follows.

① When the measurement system is controlled in accordance with the front-panel key and data knob operations or as a result of receiving a command from the GP-IB, first, A10 MAIN CPU sends this main information to A8 MEAS CPU via the common bus and common memory. When A8 MEAS CPU receives this "MAIN" information, it analyzes the contents and performs the required settings for the measurement system. In this case, the CPU uses the measurement system controller LSI to control the A1·A2 RF CONT, the A4 LOCAL unit, the A4 IF BPF unit, and the A3 IF LOG/DET unit.

② The A8 MEAS CPU fetchs the spectrum data from the Wave Memory in the A6 SCAN CONT/WM. The data is composed of 14 bits per point; at 2-channel sweeping, it is transferred to A8 MEAS CPU in the sequence A → B → A → B for each point. And calculation is performed. When each compensation value is added and it is written as waveform data in the common memory, at the same time, an interrupt is generated via the common bus to A9 DISP CPU. When A9 DISP CPU confirms the interrupt from A8 MEAS CPU; it reads the waveform data from the common memory via the common bus, performs the calculation, and displays the spectrum on the CRT using the display controller LSI.

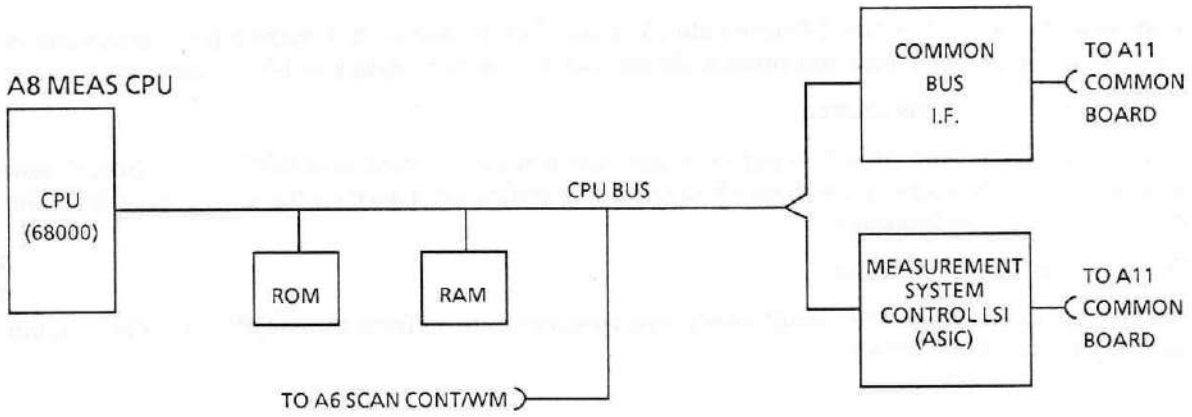


Fig. 2-16

2.7.2 A9 DISP CPU

(1) Composition

The A9 DISP CPU board is composed of the following blocks.

- CPU (MC68000, 12 MHz)

  This executes the program in the ROM and performs the processes for displaying measured waveforms and characters on the CRT.

- ROM (4 Mbits × 1)

  This ROM contains the firmware program.

- RAM (1 Mbits × 2)

  This RAM contains the various types of data required by the CPU to execute the program.

- Display controller LSI (HD63484 × 2)

  This LSI controls conversion of the plotting data (logical data from the CPU) to displaying information (physical data) and storage in the video memory.

- Video RAM (1 Mbits × 8)

  This memory saves bit-image data displayed on the CRT. Two sets (since two display-controller LSIs) of 640 × 400-dot × 4 frames (managed frame per one display-controller LSI) are saved in this video RAM.

- Shift register circuit (74AC166 × 16)

  This converts the bit-image parallel data (output from the video RAM) to serial data according to the CRT scanning direction.

- Video palette circuit

  This weights each bit of the 8-frame data (8 bits) of each video RAM managed by each display controller LSI, and converts and outputs the data as 4-bit binary data and 1-bit control data.

- Video signal output driver circuit

  This has a CRT driver circuit, separate-video-output driver circuit, and RGB driver circuit; and generates the video signals corresponding to each specification based on the data output from the previous video palette circuit.

- Common bus interface circuit

  This common bus interface circuit sends and receives data to/from other CPUs via the commn memory on A14 PMC BOARD.

(2) Outline of functions

The A9 DISP CPU board main functions are divided into the following two functions.

① Displaying measured waveform

② Displaying characters, lines and menus other than the measured waveform.

The principles of operation are described below.

① When sweeping starts and A8 MEAS CPU obains the spectrum data from the Wave Memory in A6 SCAN CONT/WM; it writes the measured data as dBm values via the common bus to the common memory on A14 PMC BOARD, and generates an interrupt to A9 DISP CPU. When A9 DISP CPU receives the interrupt; it reads the data from the common memory via the common bus, converts it to X- and Y-coordinate plotting data for display on the CRT, and sends this data to the display controller LSIs (2). When the display controller LSIs (2) read the plotting data from the CPU, they convert it to video data and store it in the video RAM. The display data stored in the video RAM is sent to the appropriate shift register using the control signal from the display controller LSIs (2) and, after this register circuit converts the data from parallel data to serial data, it is either output via the video palette and video-signal-output driver circuit to the CRT or output externally as the separate-video or RGB signals.

② When the measurement parameters are changed as a result of using the front-panel keys or data knob, or receiving a command via the GP-IB; this data is written to the common memory via A10 MAIN CPU → A8 MEAS CPU. (Depending on the parameter type, A10 MAIN CPU can write the data directly to the common memory.) When this data should be written on the CRT; A9 DISP CPU receives an interrupt for this data, reads the data from the common memory and sends it along with the display-position coordinates to a display controller LSI (1). The subsequent processing is the same as in item ①.

A9 DISP CPU

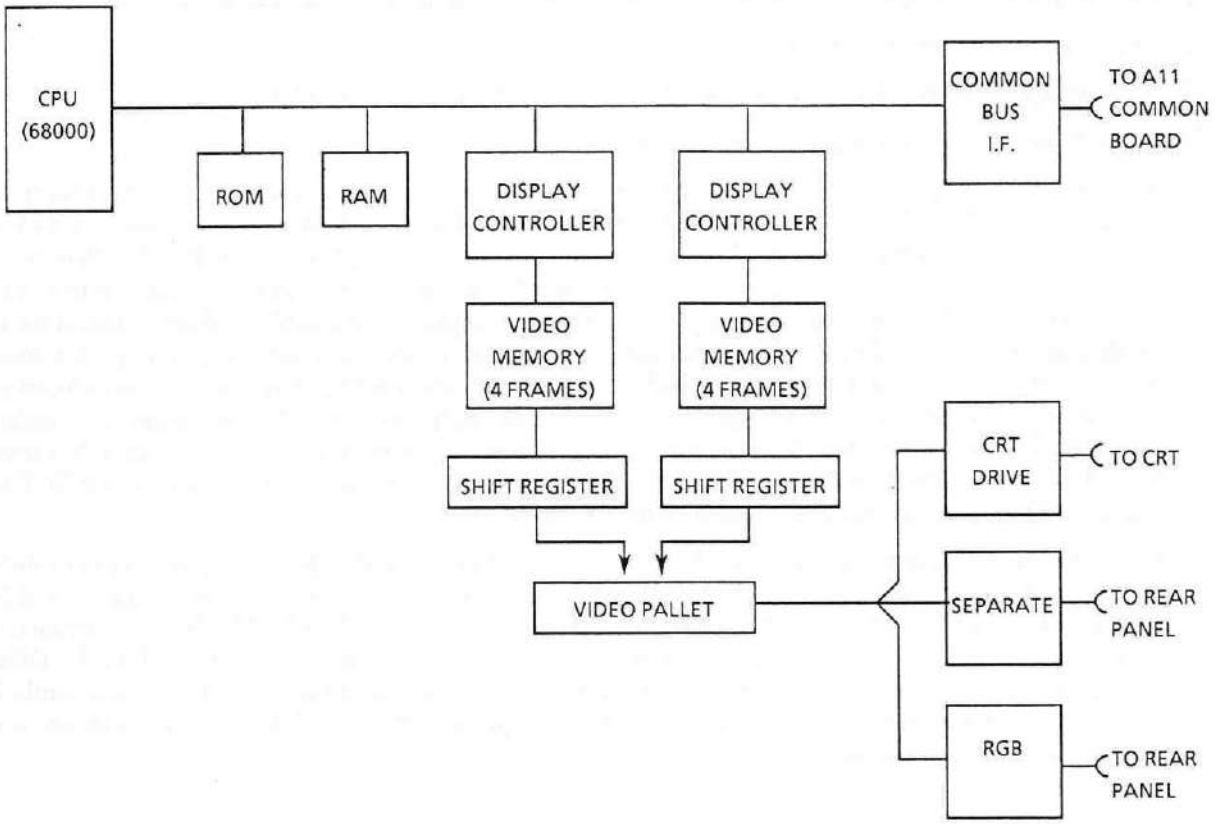


Fig. 2-17

2.7.3 A10 MAIN CPU

(1) Composition

The A10 MAIN CPU board is composed of the following blocks.

- CPU (MC68000, 12 MHz)

  This executes the program in the ROM and mainly performs the front-panel, GP-IB and PMC, etc. processing.

- ROM (4 Mbits × 2)

  This ROM contains the firmware program.

- RAM (4 Mbits × 1, 1 Mbits × 2)

  This RAM contains the various types of data required by the CPU to execute the program. In addition, this memory also saves PTA (option) user programs. So that the PTA user program is not lost even when the power is turned off, this 1 Mbit × 2 RAM is backed-up by a battery.

- Calculation LSI (MC68881)

  This high-speed LSI calculates the trigonometric functions and logarithms during execution of the PTA computations.

- Timer LSI (μPD71054)

  This LSI generates the fixed-cycle interrupt to the CPU.

- Common bus interface circuit

  This is the common bus interface circuit for sending/receiving data to/from other CPUs via the common memory on A14 PMC BOARD.

- I/O bus interface circuit

  This is the I/O bus interface circuit for sending/receiving GP-IB and PTA keyboard data.

- PTA keyboard interface LSI (μPD71051)

  This is the LSI for converting the parallel data (sent from the PTA keyboard via the I/O interface) to serial data and generating the interrupt to the CPU.

(2) Outline of functions

The A10 MAIN CPU main functions can be divided into the following four functions.

① Processing for front-panel key and data knob operations and controlling LEDs.

② Processing for command and data I/O from theGP-IB, RS-232C (option 02) and I/O port (option 03)

③ Processing for PMC (in MC8104A Data Storage Unit)

④ Processing for PTA

These principles of operation are explained on the next page.

① When a front-panel key or data knob operation occurs, that data is transferred to the CPU via the common bus using an interrupt or CPU polling operation. The CPU analyzes the data and performs the processing. When processing is required by another CPU, the data is sent via the common bus in accordance with the processing contents.

② First, command reception is verified, the processing corresponding to the command input from the GP-IB is transferred to the GP-IB LSI (TMS9914A) on the interface board, and then an interupt is sent to the CPU. The CPU that received the interrupt, reads the command data via the common bus, analyzes it and processes it. Even in this case, when processing is required by another CPU, the data is sent via the common bus in accordance with the processing contents. In additon, the same processing is performed by the hardware when the RS-232C (option 02) and I/O port (option 03) options are installed.

③ When a PMC processing request is generated from the front panel or GP-IB, the data is sent/received to/from the PMC (inserted by user from front panel) on A14 PMC BOARD or the PMC (or FDD) of the MC8104A Data Storage Unit. In the former case, it is sent to the PMC via the common bus; in the latter case, it is output externally via the I/O bus and GP-IB LSI on the interface board (GP-IB 2 side).

④ The data (serial) input from the PTA external keyboard is input to the CPU board via the I/O bus. The input serial data is converted to parallel data by the PTA keyboard interface LSI and transferred to the CPU.

In addition, the command or statements (input from the PTA keyboard) or the PTA user program (loaded from the PMC) are analyzed and processed by the CPU, but the trigonometric and logarithmic calculations, etc. are performed by the calculation (arithmetic) LSI.

The calculation LSI operates as a the CPU coprocessor.

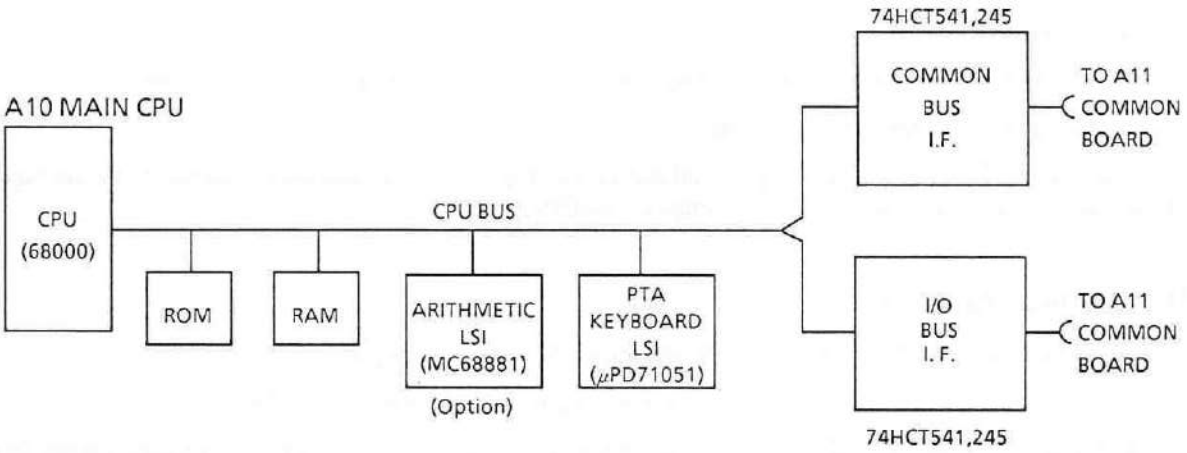


Fig. 2-18

2.7.4 A7 INTERFACE 1

The A7 INTERFACE board 1 is composed of the following blocks.

- GP-IB1 side GP-IB dedicated LSI (TMS9914) and driver

  This controls the external bus for the GP-IB1 side which operates as a normal device port. GP-IB commands sent from outside are input to the LSI through the driver. When the LSI receives the data, it generates an interrupt to A10 MAIN CPU via the I/O bus. When A10 MAIN CPU receives the interurpt, it fetches the data from the LSI via the I/O bus.

- GP-IB2 side GP-IB dedicated LSI (TMS9914) and driver

  This LSI controls the external bus for the GP-IB2 side which operates as a controller port. When data is output to the GP-IB2 port, A10 MAIN CPU sends the data to the LSI via the I/O bus. When the LSI receives the data from the CPU, it outputs the data on the external bus via the driver.

- DIP SW

  The maintenance DIP SW on A7 INTERFACE board 1 is not used.

2.7.5 A12 INTERFACE 2 ····· Option 03

The A12 INTERFACE board 2 is composed of the following blocks.

- GP-IB1 side GP-IB dedicated LSI (TMS9914) and driver

  This controls the external bus for the GP-IB1 side which operates as a normal device port. GP-IB commands sent from outside are input to the LSI through the driver. When the LSI receives the data, it generates an interrupt to A10 MAIN CPU via the I/O bus. When A10 MAIN CPU receives the interrupt, it fetches the data from the LSI via the I/O bus.

- I/O port controller

  This inputs/outputs data from controller to external bus by reading/writing the data from/to I/O-port controller via I/O bus using A10 MAIN CPU.

- DIP SW

  The maintenance DIP SW on A12 INTERFACE 2 is not used.

2.7.6 A13 INTERFACE 3 ····· Option 02

The A13 INTERFACE board 3 is composed of the following blocks.

- GP-IB1 side GP-IB dedicated LSI (TMS9914) and driver

  This controls the external bus for the GP-IB1 side which operates as a normal device port. GP-IB commands sent from outside are input to the LSI through the driver. When the LSI receives the data, it generates an interurpt to A10 MAIN CPU via the I/O bus. When A10 MAIN CPU receives the interrupt, it fetches the data from the LSI via the I/O bus.

- RS-232C firmware and driver circuit

  To process the RS-232C data, this circuit is composed of CPU (8085, for RS-232C data processing), ROM, RAM, and their peripheral control circuits as well as a parallel-to-serial data-conversion LSI and a driver for external I/O. Communication with A10 MAIN CPU is performed via the I/O bus and the communication register on A13 INTERFACE 3.

- DIP SW

  This switches the RS-232C communication control mode between full-duplex/half-duplex, X ON/OFF and BUSY/READY. The switch status is read and the software processing is determined immediately after A10 MAIN CPU is powered-on.

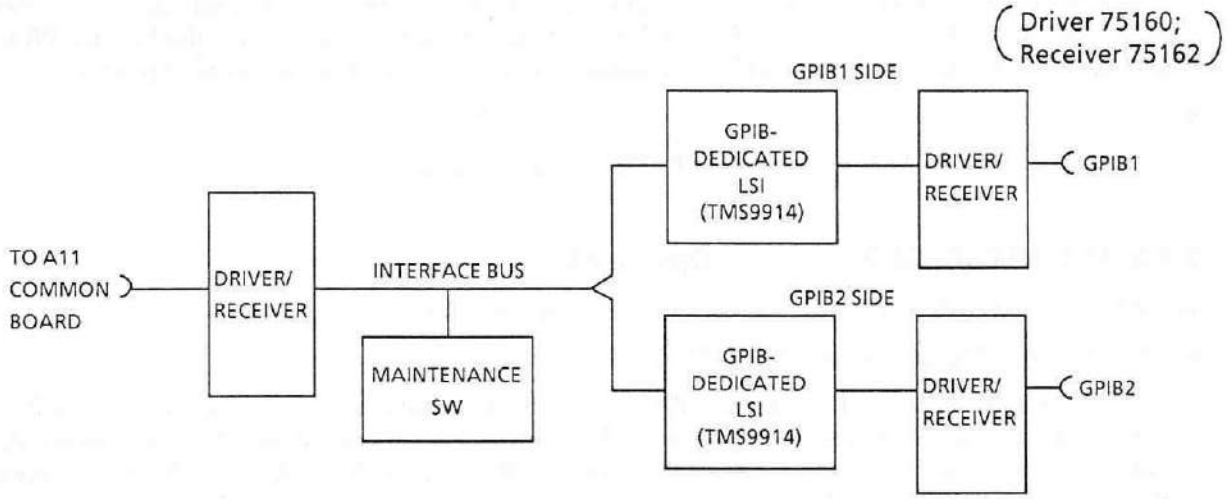


Fig. 2-19 A7 Interface 1

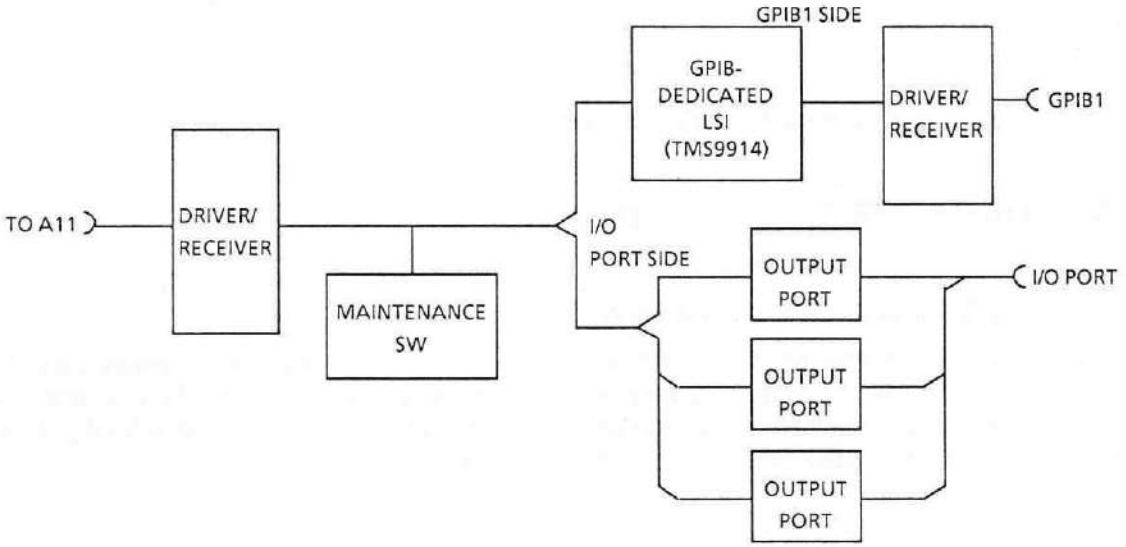


Fig. 2-20 A12 Interface 2

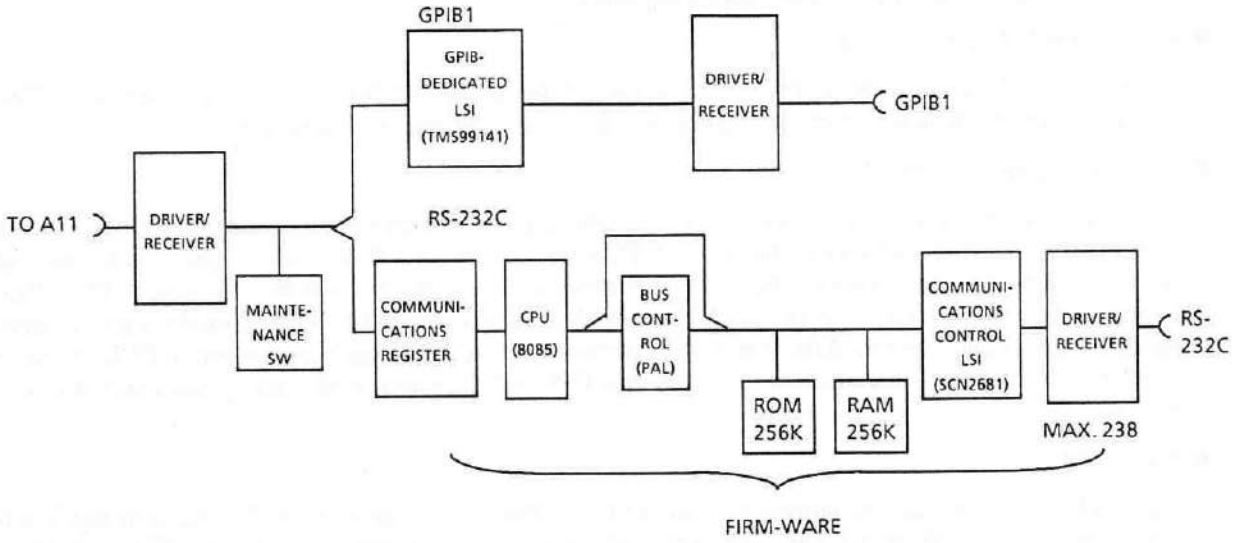


Fig. 2-21 A13 Interface 3

2.7.7 A14 PMC BOARD

A14 PMC BOARD is composed of the following blocks.

- Common RAM (1 Mbits × 2)

  This battery backed-up memory can be accessed by all the CPUs via the common bus. The measurement parameters and the calibration data are all stored in this memory.

- Common bus arbiter circuit

  When a CPU is using the common bus (common communication resource), this circuit works as the arbiter so that collisions between CPUs do not occur. When the signals (requesting permission to use the common bus) is generated at the same time from different CPUs. The common bus is handed over to the CPU which has the priority. The priority rule is pre-determined by the system. After the CPU starts using the common bus, the other CPUs cannot use the common bus and must wait until the CPU (that is currently using the common bus) releases it.

- Clock LSI

  This battery backed-up LSI stores the current time. The clock is set at factory shipment but when the PTA is ON, A10 MAIN CPU can set and read the clock time by using the PTA command called SYSTEM VARIABLE.

- PMC interface circuit

  The common-bus address space is divided into a number of banks. Of these banks, one bank is allotted for use by the PMC. When A10 MAIN CPU has accessed this address in the bank, data can be read/written from/to the PMC using only the PMC interface circuit. In addition, the voltage of the power supply to the PMC from the measuring instrtument side as well as the PMC internal power supply voltage is sensed in this circuit.

- Panel interface circuit

  The address for interfacing the panel is allocated one address space on the bank-divided common bus, and A15 FRONT PANEL and A10 MAIN CPU read/write the data via this panel interface circuit.

- Power supply ON/STANDBY switch circuit and power supply cut-off circuit

  The power supply ON/STANDBY switch circuit, and an automatic power supply cut-off circuit, which is activated by an increase in the measuring-instrument internal temperature, are on A15 FRONT PANEL. When a rise in the instrument internal temperature is sensed by the temperature sensor on the A3 LOCAL unit, a signal is input to the control circuit on A14 PMC BOARD via A17 MOHER BOARD and A11 COMMON board. This signal voltage is compared by the level comparator, and when it exceeds the specified voltage (specified temperature), a relay is activated to cut the main power supply. To resupply power, LINE switch on the rear panel of the main unit must be set to ON.

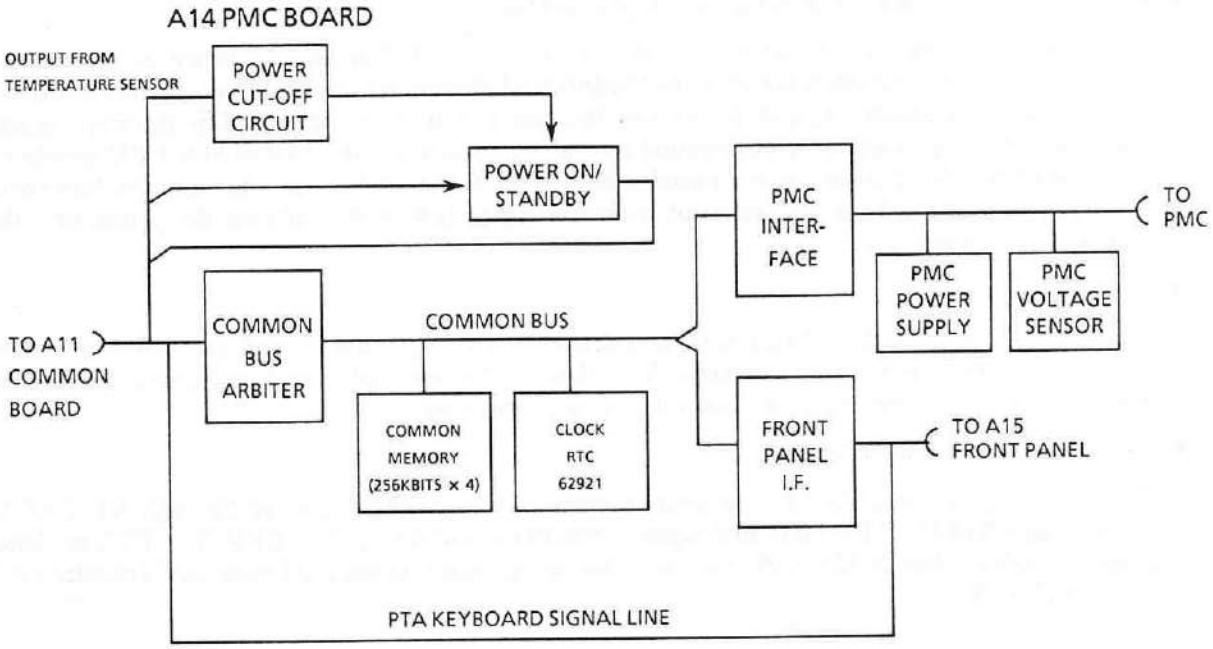


Fig. 2-22

2.7.8 A11 COMMON BOARD

A11 COMMON BOARD is connected electrically between each A8 to A10 CPU boards, A7/A12/A13 INTERFACE boards, A14 PMC board and A17 MOTHER BOARD for supplying voltages (5 V, 12 V) from the power supply unit to each board for digital circuits. It also supplies 12 V power to the CRT.

2.7.9 A15 FRONT PANEL

The A15 FRONT PANEL board is composed of the following blocks.

- Panel keys and panel-key encoder circuit

  The key code (8 bits) corresponding to the pressed key is generated and sent as an interrupt via the common bus to A10 MAIN CPU. The interrupt is released automatically and at the same time A10 MAIN CPU reads the prior contents from the shift register.

- Rotary encoder (data knob) and controller LSI (μPD4701)

  When the rotary encoder is turned, a pulse train with a 180° phase difference is generated in accordance with the rotation direction by the internal photodiode and photosensor. The controller LSI detects the number of pulse trains and the phase difference, and the LSI internal register stores the detected data as a corresponding signed binary value. A10 MAIN CPU reads the contents of the front-panel rotary-encoder controller LSI register via the common bus (when triggered by the fixed-period interrupt from the timer LSI) and performs the processing that corresponds to the vlaue.

- LEDs

  These LEDs indicate that [REMOTE] and [SHIFT], etc are enabled, and are connected to the common bus via the register (driver), A10 MAIN CPU controls the lamp status (on/off) by operating the bits corresponding to each lamp on the register.

- Signal relay from PTA keyboard

  The serial signal (from the PTA keyboard connected externally) is passed through A15 FRONT PANEL and A14 PMC BOARD, and input to the I/O bus of A10 MAIN CPU. The PTA keyboard interface LSI on A10 MAIN CPU converts the serial signal to parallel data, and transfers it to A10 MAIN CPU.

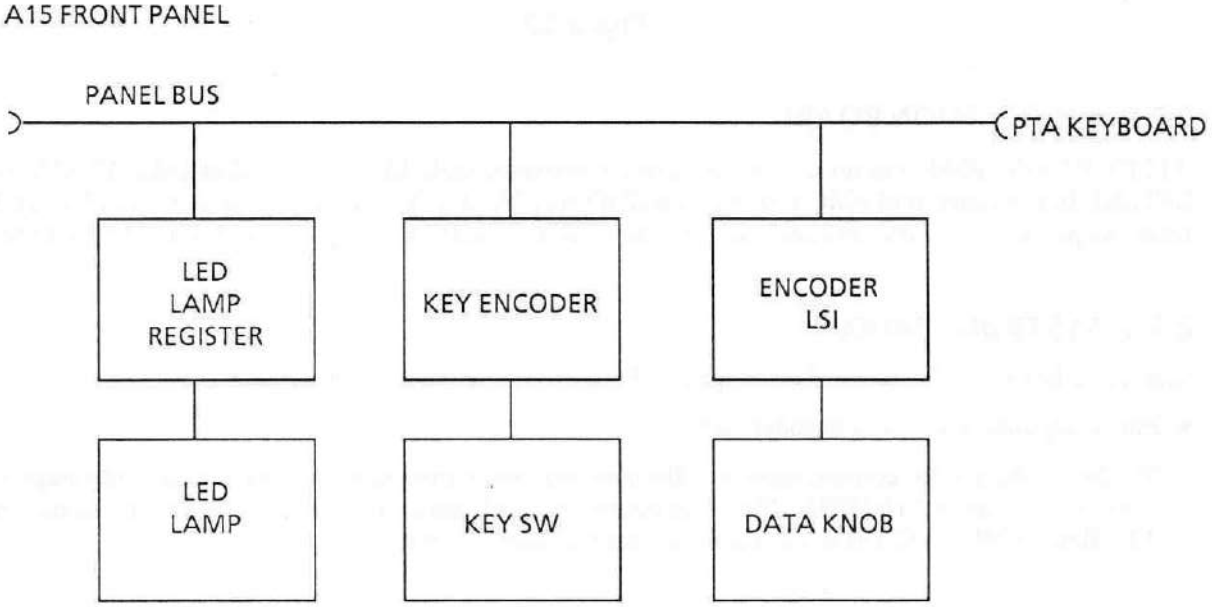


Fig. 2-23

SECTION 3
TROUBLESHOOTING AND ADJUSTMENT

3.1 Introduction

3.1.1 Composition

This section describes how to troubleshoot the MS2602A.

Table 3-3 lists the circuit diagrams, parts lists and PC-Boards.

Notes: Calibration of compensation data

The MS2602A measuring accuracy can be improved by entering the compensa-tion data shown below in the built-in memory.

1. RF gain compensation data
2. CAL level and CAL ATT compensation data
3. RF ATT switching deviation compensation data
4. Preselector offset compensation data

If the specifications are not met for the performance test described in Section 5 of the Operation Manual (Basic Operations) after the circuit (related to these compensation data) has been repaired, the compensation data must be reentered. The input method is described in Part 2.

3.1.2 Checking and replacement of parts

(1) Explanation of identification markings on the PC-Board

As shown in Fig. 3-1, the MS2602A PC-Board has the A number, PC-Board number with the revision number, PC-Board name, and test point name.

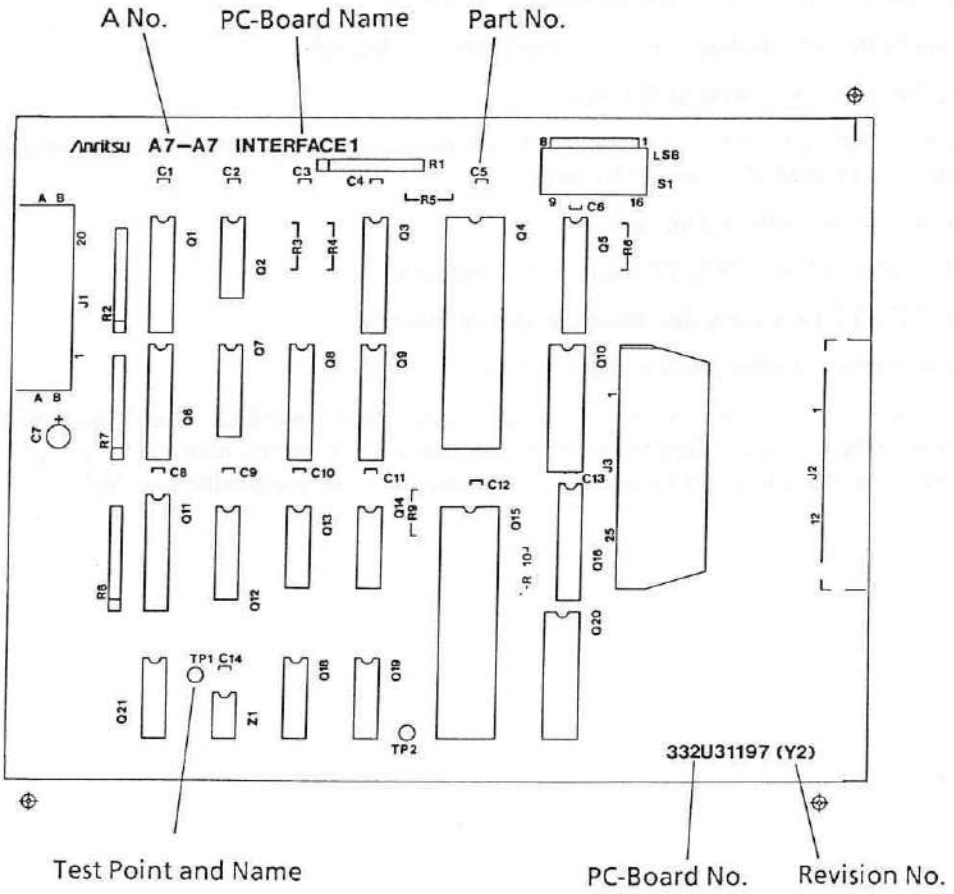


Fig. 3-1 PC-Board Identification Markings

(2) Notes on soldering

1. Use an ordinary 30 to 40 watt pencil type soldering iron.
2. Before using the soldering iron, be sure it is insulated. If not, it may damage the part.
3. When removing a soldered part from a circuit board or soldering in a new part, nip the part lead with tweezers to shunt heat.
4. The tips of major part leads are bend behind the PC-Board to ensure tight support. To remove a part, first lift up the tips of the leads and then remove the part.

(3) Transistor and diode check

(a) Check of transistors mounted on the PC-Board

Transistors can be checked for acceptable quality in the operating state by measuring the base and emitter potentials. The NPN type silicon transistor shows a value that the base potential is 0.6 or 0.7 V higher than the emitter potential. In the PNP silicon transistor, the former is 0.6 or 0.7 V lower than the latter. Transistors are, therefore, faulty if these relationships are not satisfied.

(b) Check of transisotrs removed from the PC-Board

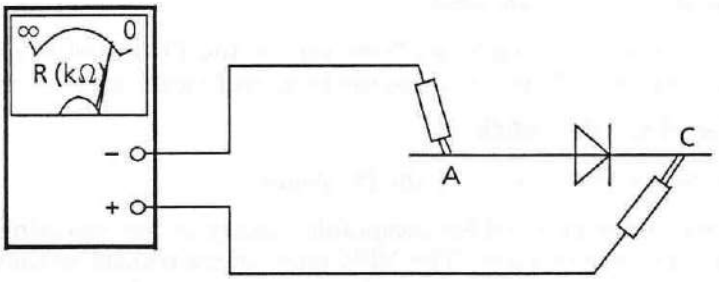
Transistors can be checked by measuring the resistance values among the emitter, base, and collector using a circuit tester. Standard values are given in Table 3-1. Note that this check should be performed at a measuring current of less than 100 μA.

Table 3-1 Test of Transistors Removed from the PC-Board

Type of transistor	Connector Ohmmeter		Resistance to be measured (ohm)
	Positive lead to	Negative lead to	
PNP silicon	Emitter, collector	Base	1 to 10 k
	Emitter	Collector	Very high
NPN silicon	Base	Emitter, Collector	1 to 10 k
	Emitter	Collector	Very high

(c) Check of diodes removed from the PC-Board

Diodes can be checked by measuring the resistance between the anode and cathode and the cathode and anode. If the resistance between the anode and cathode (A-C) is high and the resistance betwee C-A is low, when measured with an ohmmeter as shown in Fig. 3-2, the diode is normal.

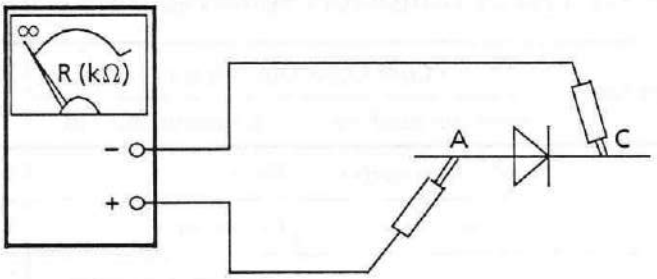


(1) Between C-A

Example: 1S953

A-C: ∞

C-A: ≒9 kΩ



(2) Between A-C

Fig. 3-2 Diode Check

3.1.3 Service kit

The ordering number for service kits is 34Y102972.

Table 3-2 Service Kit for MS2602A

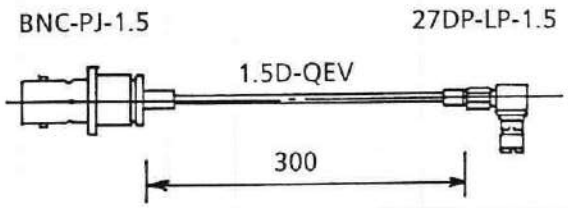
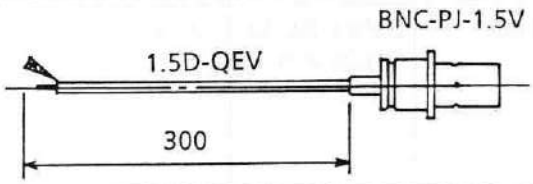
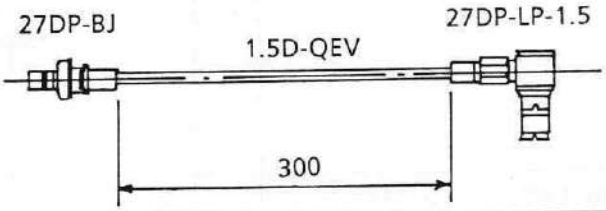
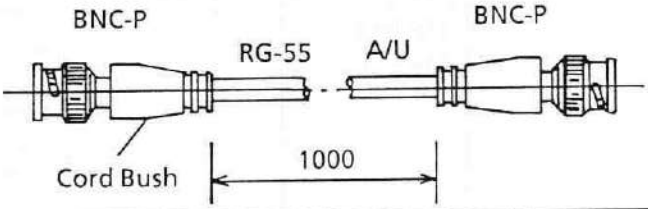
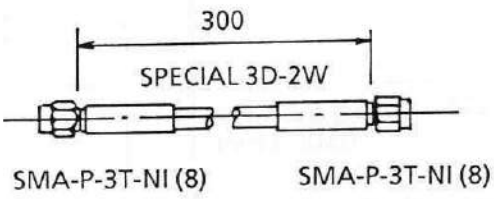
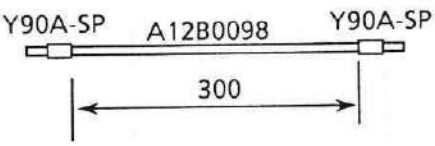
No.	Dwg. No.	Accessory Name	Q'ty	Remarks
1	34J92837F	Extender Cable	3	
2	34J94206	Extender Cable	1	
3	34J94207	Extender Cable	3	
4	S4J10001F	Extender Cable	2	
5	S4W10184C	Extender Cable	3	
6	S4J10211F	Extender Cable	3	

Table 3-2 Service Kit for MS2602A (Continued)

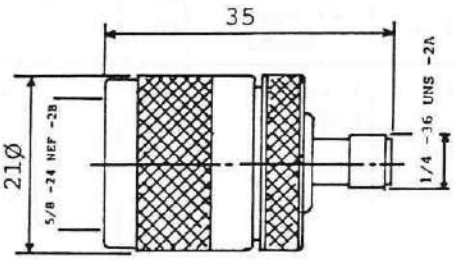
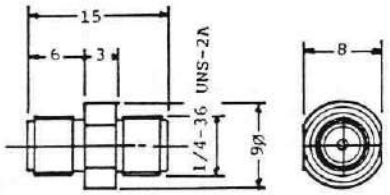
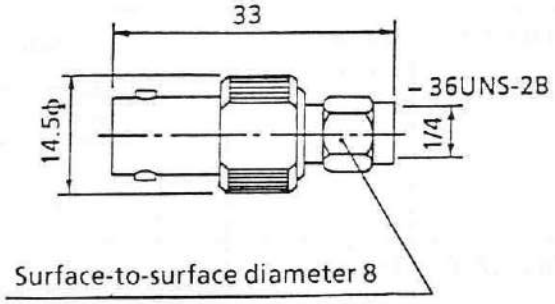
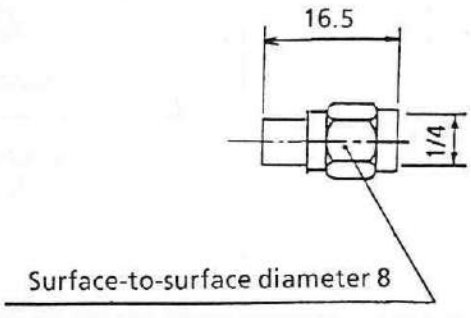
No.	Dwg. No.	Accessory Name	Q'ty	Remarks
7	No. 1305	NP-SMAJ (HRM554S) Adapter	1	
8	No. 1305	SMAJ-SMAJ (HRM501) Adapter	2	
9	No. 1305	SMAP-BNCJ (HRM517) Adapter	2	
10	No. 1274	SMAP-Y90J (DMP-Y90J) Adapter	3	

Table 3-2 Service Kit for MS2602A (Continued)

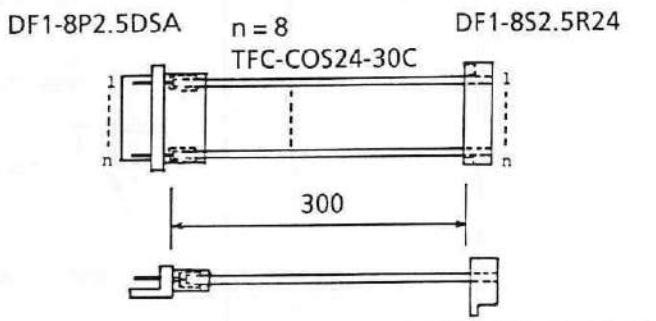
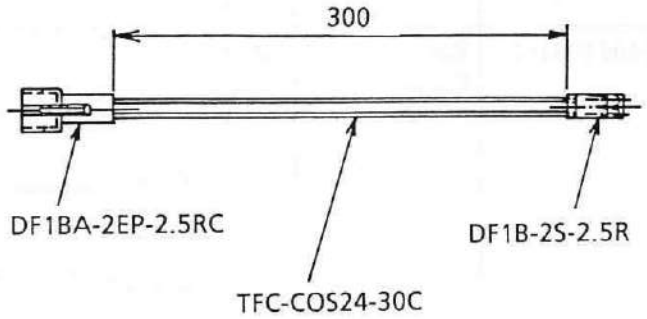
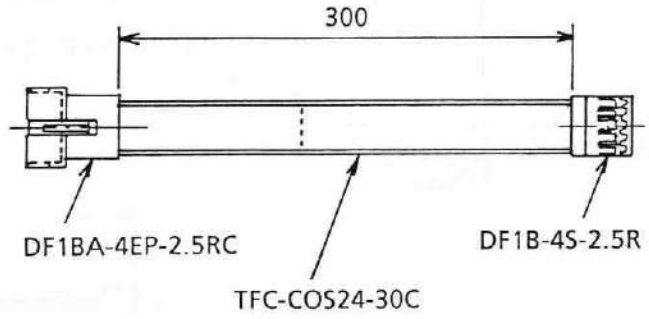
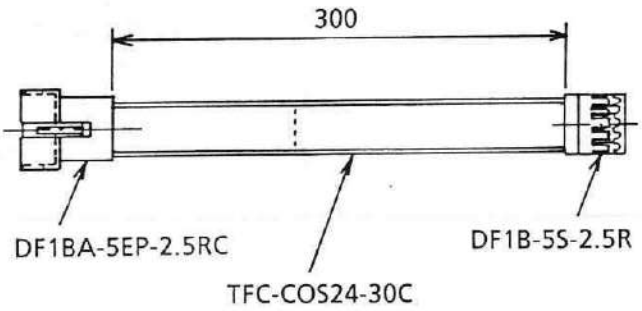
No.	Dwg. No.	Accessory Name	Q'ty	Remarks
11	449J81722C	Extender Cable	1	
12	349J99345	Extender Cable	1	
13	349J103161	Extender Cable	1	
14	349J99346	Extender Cable	4	

Table 3-2 Service Kit for MS2602A (Continued)

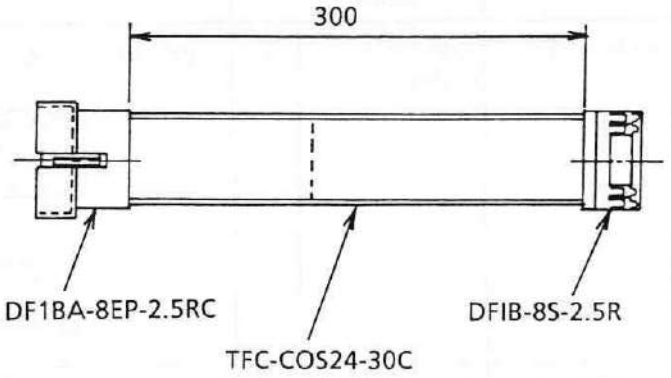
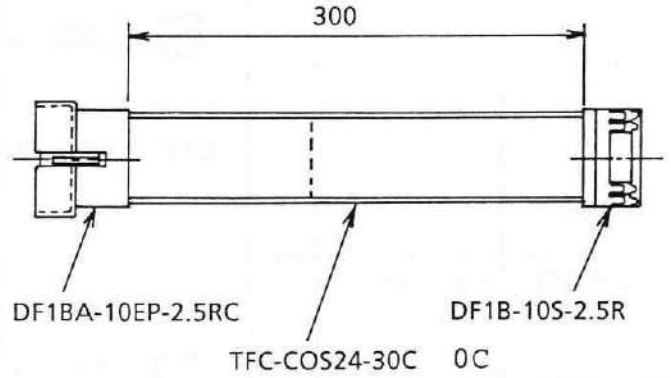
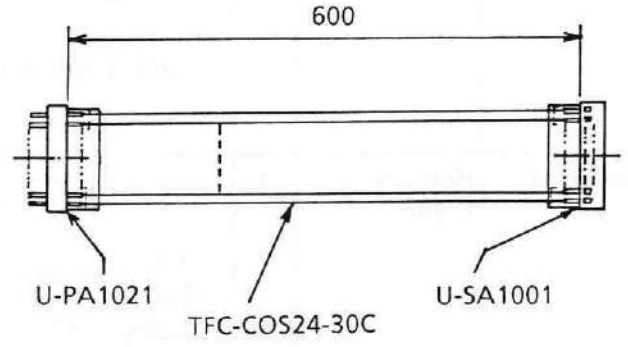
No.	Dwg. No.	Accessory Name	Q'ty	Remarks
15	349J99347	Extender Cable	2	
16	349J103162	Extender Cable	2	
17	349J99700	Extender Cable	2	

Table 3-2 Service Kit for MS2602A (Continued)

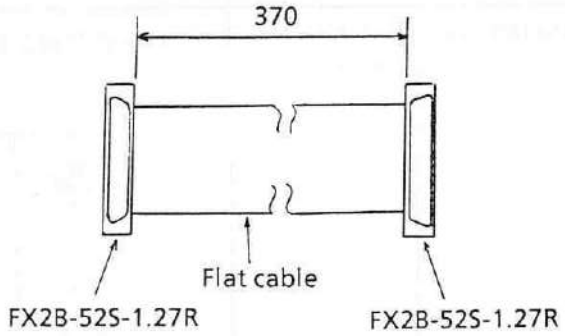
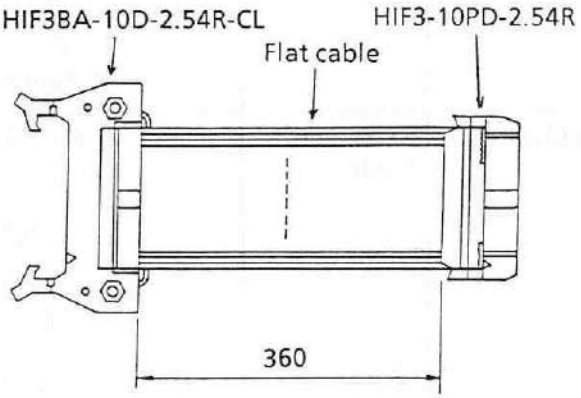
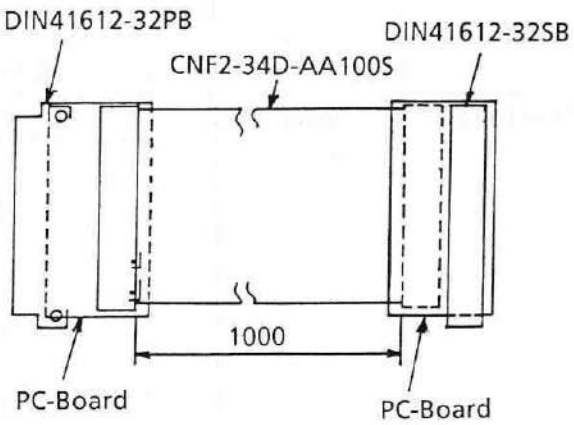
No.	Dwg. No.	Accessory Name	Q'ty	Remarks
18	34J100843B	Extender Cable	1	
19	44J95055N	Extender Cable	1	
20	343J99494	Extender Cable	1	

Table 3-2 Service Kit for MS2602A (Continued)

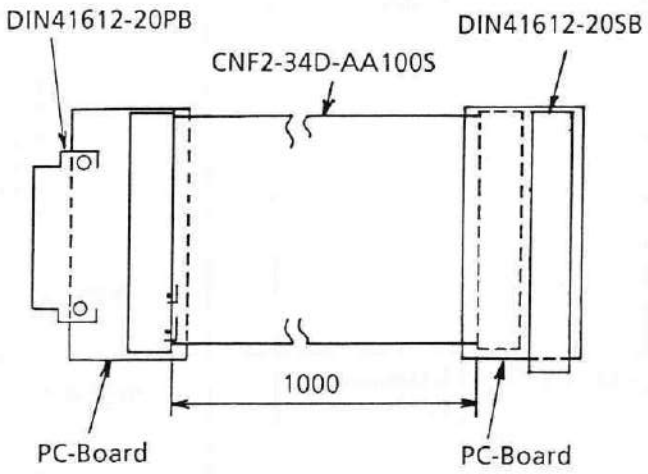
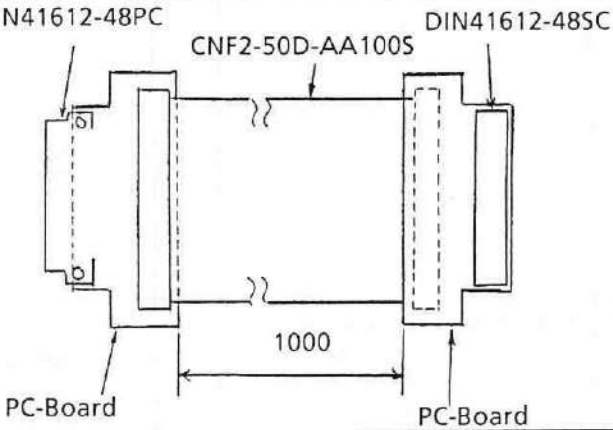
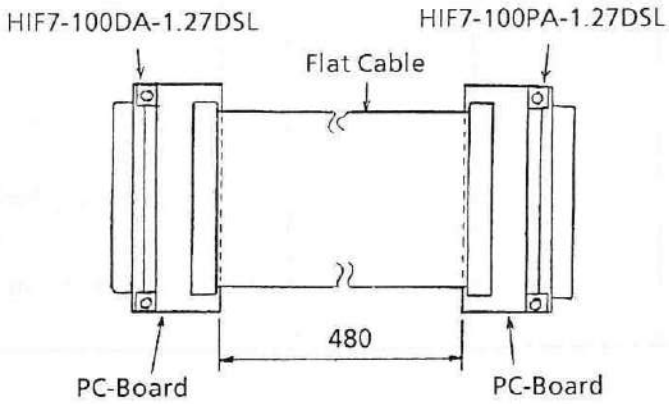
No.	Dwg. No.	Accessory Name	Q'ty	Remarks
21	343J103155	Extender Cable	1	
22	343J103156	Extender Cable	1	
23	343J100163	Extender Cable	1	

Table 3-2 Service Kit for MS2602A (Continued)

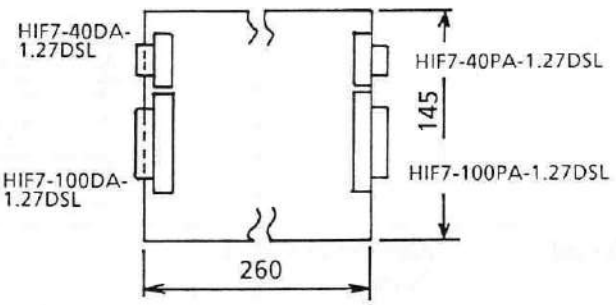
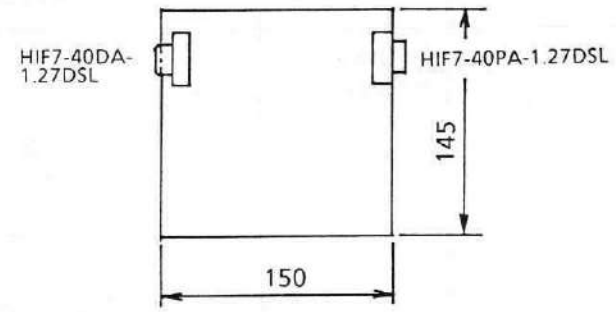
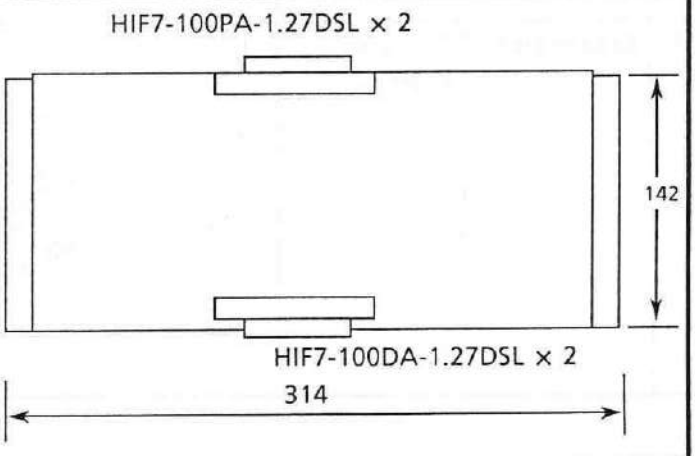
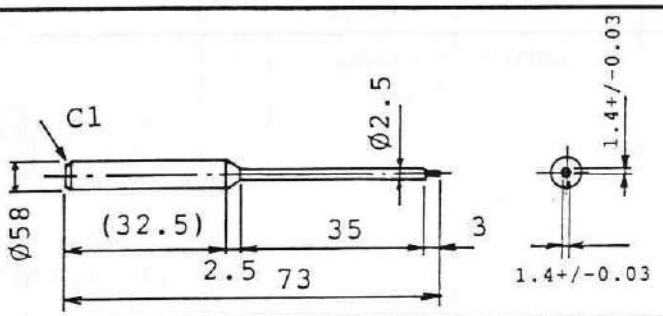
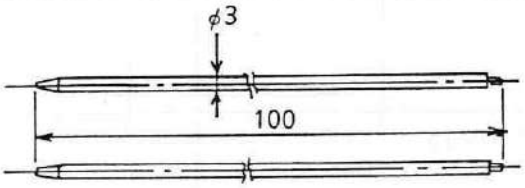
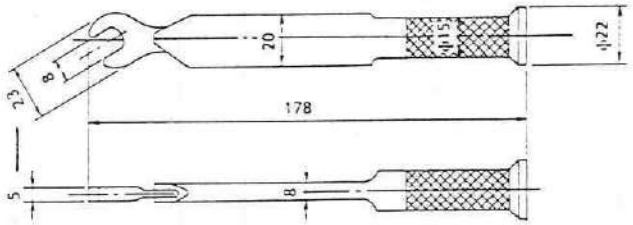
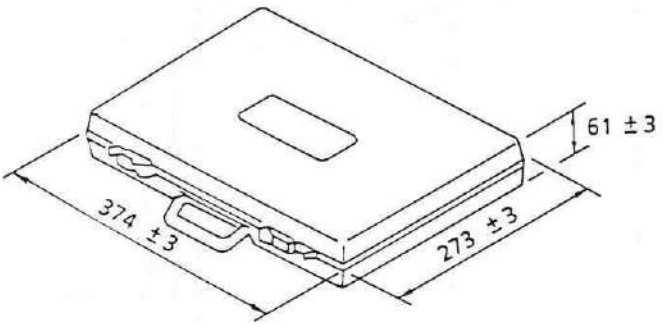
No.	Dwg. No.	Accessory Name	Q'ty	Remarks
24	343J100162	Extender Board	1	
25	343J103157	Extender Board	1	
26	344J103158	Extender Board	1	

Table 3-2 Service Kit for MS2602A (Continued)

No.	Dwg. No.	Accessory Name	Q'ty	Remarks
27	34Z99432	Adjustment Driver	1	
28	34Z81433	Adjustment Driver	1	
29	34B35154	Torque Wrench	1	
30	343Z103165	Carrying Case	1	

3.1.4 Circuit reference

This paragraph supplied the circuit diagram of the MS2602A main unit (MS2602A overall, A1 RF BLOCK, A1-A1 RF MOTHER BOARD, A1-A2 RF CONT, A1-A3 RF CONVERTER, A1-A4 LOCAL, and A17 MOTHER BOARD).

For the other circuit diagram, parts list, and PC-Board, refer to the separate service manual (Part 2).

Table 3-3 MS2602A Circuit Reference

Schematic No.	"A" No.	Name	Circuit diagram No.	Parts list No.	PC-Board No.
1	------	MS2602A Overall	33W33208	34W100961	------
2	A1	RF BLOCK	33W033289	34W101080	------
3	A 1	RF MOTHER BOARD	33W033320	34W101081	332U33128 (332U33697a)
4	A 2	RF CONT	33W033317	34W101148	------
5	A1	RF CONT 1	33W033178	34W100802	322U11980
6	A2	RF CONT 2	33W033179	34W100803	332U33132 (332U33697b)
7	A3	SAMPLER	33W033318	34W101149	322U11976
8	A4	ISOLATION AMP	33W033319	34W101150	332U33172
9	A 3	RF CONVERTER	33W033290	34W101082	------
10	A1	SW/EQ	33W033292	34W101084	332U33134d
11	A3	2.5214 GHz IF AMP	33W033293	34W101085	332U33134e
12	A4	2.5214 GHz BPF	33W033293	34W101086	332U33134a
13	A5	LPF	33W033293	------	332U33134b
14	A6	1ST LO AMP	33W033296	34W101088	332U33134c
15	A7	2 GHz PLL	33W033297	34W101089	332U33138a
16	A8	2ND CONV	33W033298	34W101090	332U33138b

Table 3-4 MS2602A Circuit Reference (Continued)

Schematic No.	"A" No.			Name	Circuit diagram No.	Parts list No.	PC-Board No.
17	A1	A3	A9	3RD CONV	33W033299	34W101091	332U33140
18			A10	CAL/CONT	33W033300	34W101092	332U33154
19			A11	521.4 MHz IF AMP	33W033304	34W101096	332U33138c
20		A 4		LOCAL	33W33174	34W100787	------
21			A1	LOCAL BOARD 1	33W33175	34W100788	322U11972
22			A2	LOCAL BOARD 2	33W33176	34W100789	322U11974
23		A6		10 MHz REF	34W97060	34W97065	342U96830
24	A3			IF LOG/DET	33W32316	34W100755	322U11978
25	A4			IF BPF	33W33352	34W101237	322U12084
26	A5			SCAN/AD	33W33095	34W100639	322U11982
27	A6			SCAN CONT/WM	33W33096	34W100640	322U11984
28	A7			INTERFACE 1	33W31295	34W96808	332U31197
29	A8			MEAS CPU	33W32980	34W100392	332U33144
30	A9			DISP CPU	33W32979	34W100391	332U33146
31	A10			MAIN CPU	33W32978	34W100390	332U33148
32	A11			COMMON BOARD	33W32983	34W100395	332U33150
33	A14			PMC BOARD	33W32981	34W100393	322U11986
34	A15			FRONT PANEL	33W32982	34W100394	322U11988 (322U12207a)
35	A17			MOTHER BOARD	33W33209	34W100962	332U33152

Table 3-4 MS2602A Circuit Reference (Continued)

Schematic No.	"A" No.	Name	Circuit diagram No.	Parts list No.	PC-Board No.
36	A18	FILTER BOARD	33W33210	34W100963	342U100813 (322U12207b)
------	OPTIONS	------	------	------	------
37	A1-A5	TG (OPT)	------	------	------
38	A1-A6	10 MHz REF (OPT)	34W97061	34W97066	342U96694
39	A12	INTERFACE 2 (OPT)	33W32985	34W100397	332U33358
40	A13	INTERFACE 3 (OPT)	33W31297	34W96810	332U31205

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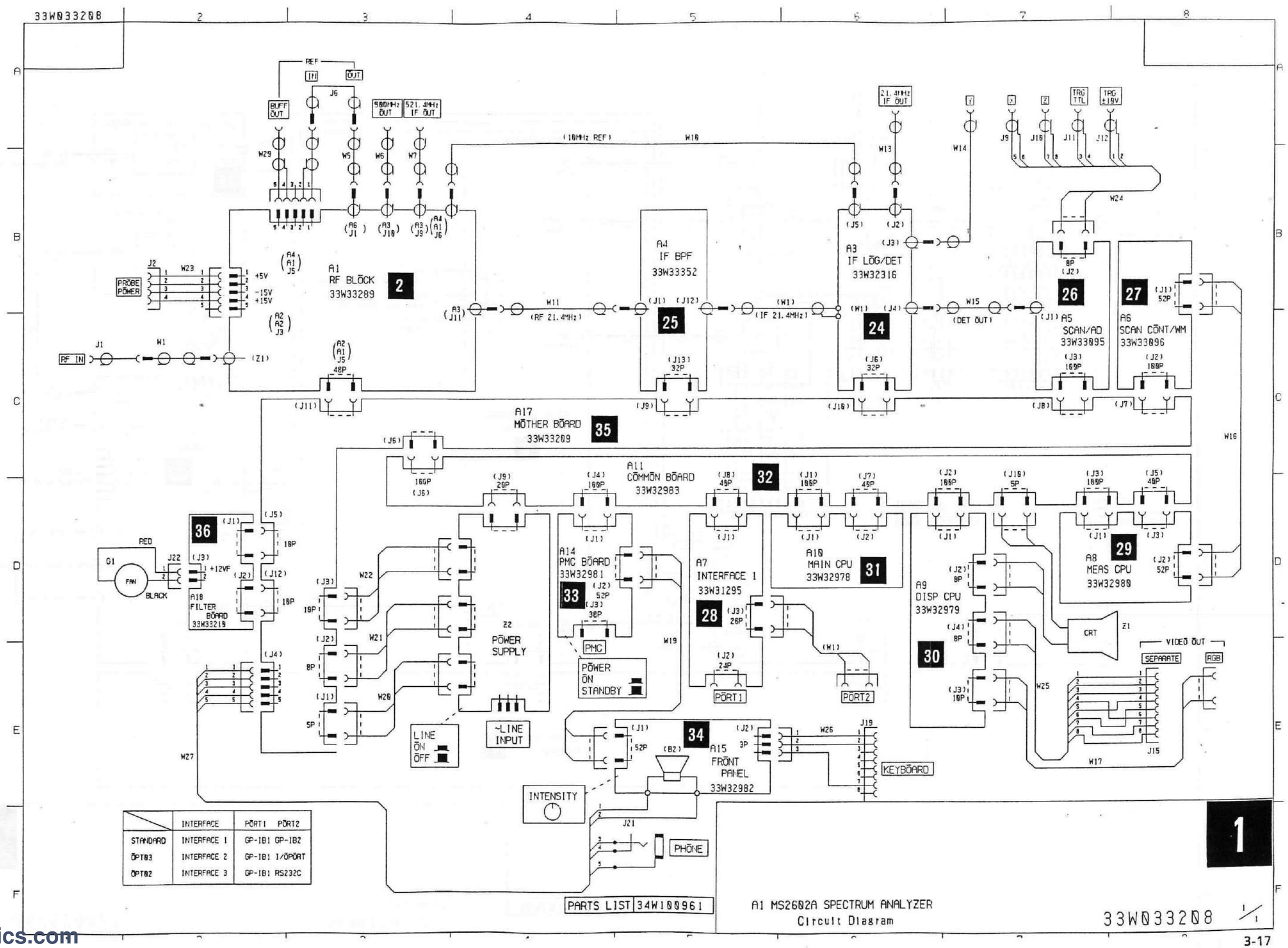


	INTERFACE	PORT1 PORT2
STANDARD	INTERFACE 1	GP-IB1 GP-IB2
OPT03	INTERFACE 2	GP-IB1 I/OPORT
OPT02	INTERFACE 3	GP-IB1 RS232C

33W033289

To (W1)
(From front panel: RF INPUT)

Z1 ATT
Z2 ISOL
Z3 YTF
Z4 YTO

W1 W2 W3 W4 W5 W11 W13 W14 W15 W17

(A2-J2) (A2-J1) (A1-J3) (A1-J2) (A1-J4) (A1-J1) (A1-J5) (A2-J5) (A2-J3)

To (W23)
(To front panel: PROBE POWER)

A2 RF CONT
33W033317
4

(Z1) 8-20GHz
(Z4-RF) 1.7-8.5GHz
(J4) 2.2-8.1GHz
(J1) 94-197MHz
(J2) 2-8GHz
(J4) 2-8GHz (TG opt)
(J6) 2-8GHz
(J12) 166MHz

(J9) 521.4MHz To (W7) (To rear panel:521.4MHz IF OUT)
(J10) 500MHz To (W6) (To rear panel:500MHz OUT)
(J11) 21.4MHz To (W11) (To IF BPF)

A3 RF CONVERTER
33W033290
9

(W11)

A6 10MHz REF 34W103064
(J1) 10MHz To (W5) (To rear panel:REF OUT)
+12VS +12V (C3) E
23

Z8 100MHz VCXO
155MHz -12V E
W21 W22
(J1-J4)
(A1-J16) 155MHz
(A1-J6) 10MHz To (W10) (To A3-J5)

A4 LOCAL
33W033174
20

(W6) 13 0 (W6) 11-14MHz
W9
(A1-J15) 94-197MHz
(A1-J5) 10MHz To (W29) (To rear panel:REF IN/BUFFER OUT)
(A1-J16) (1MHz step)
(A2-J5) (10kHz step) Check point
(A2-J4) (1Hz step)
(W5) 1 0 (W5) 166MHz

(A19-J1)
(J1) (J2) (J3)

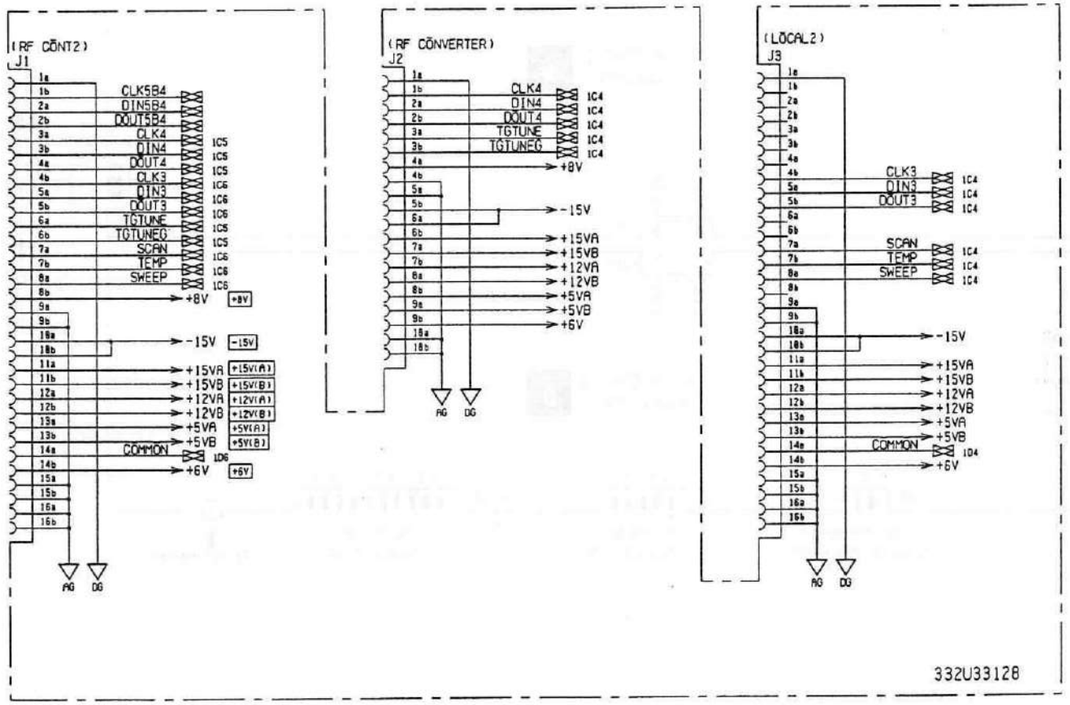
To (A17-J11)

A1 RF MOTHER BOARD
33W033320
3

PARTS LIST 34W101080

2

A1 RF BLOCK
Circuit Diagram
33W033289 1 1

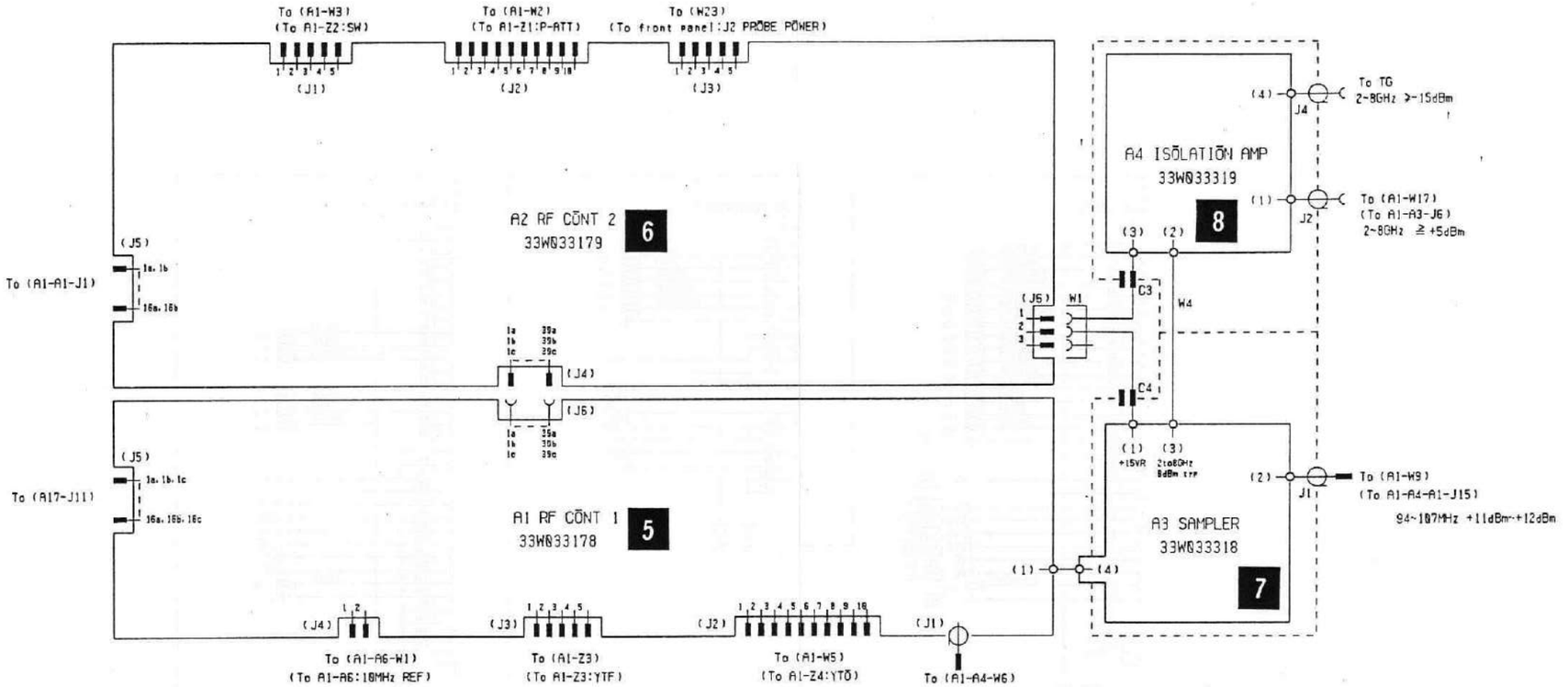


PARTS LIST 34W101081

A1-A1 RF MOTHER BOARD
Circuit Diagram

33W033320

3

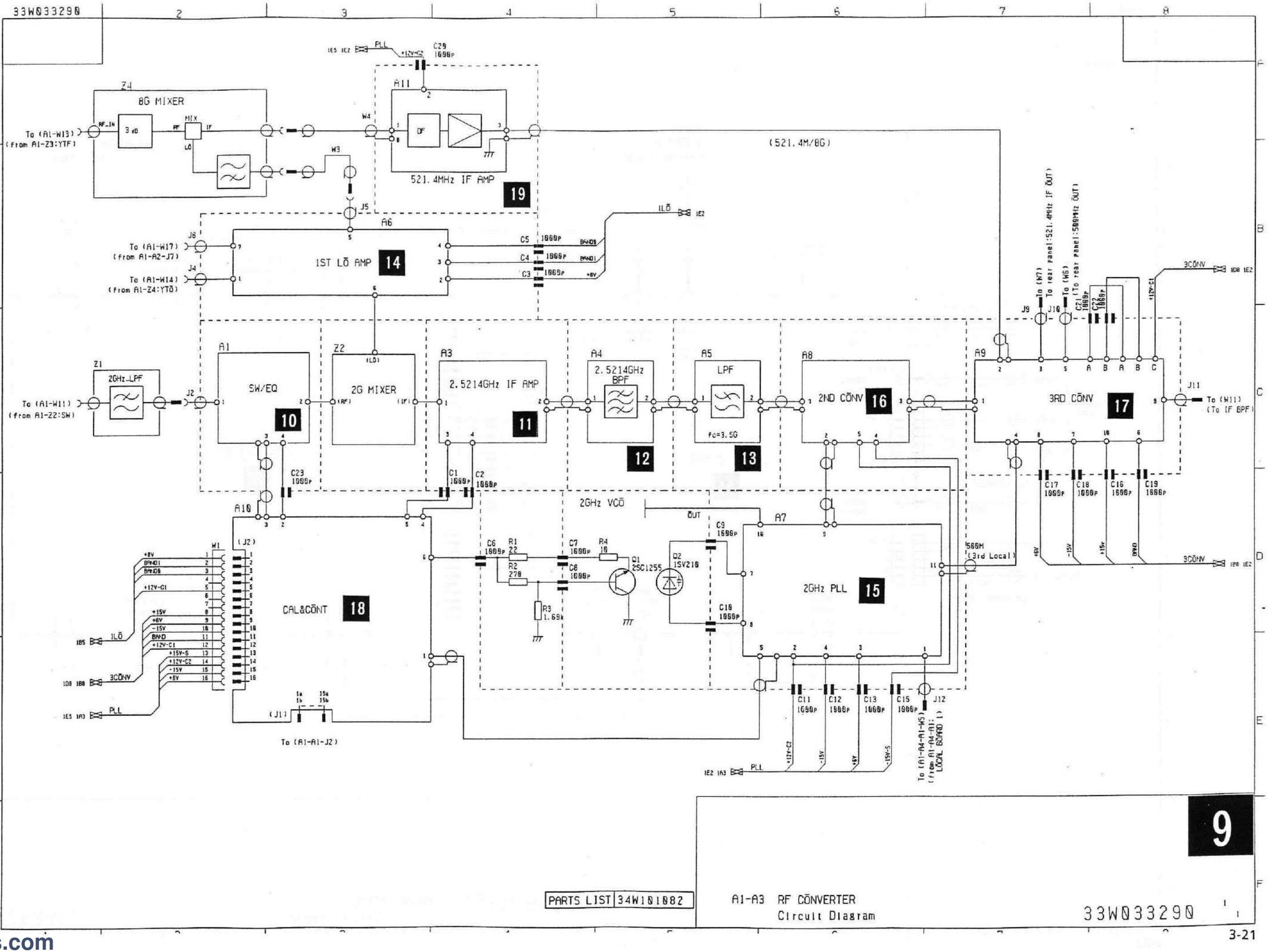


PARTS LIST 34W101148

4

A1-A2 RF CONT
Circuit Diagram

33W033317

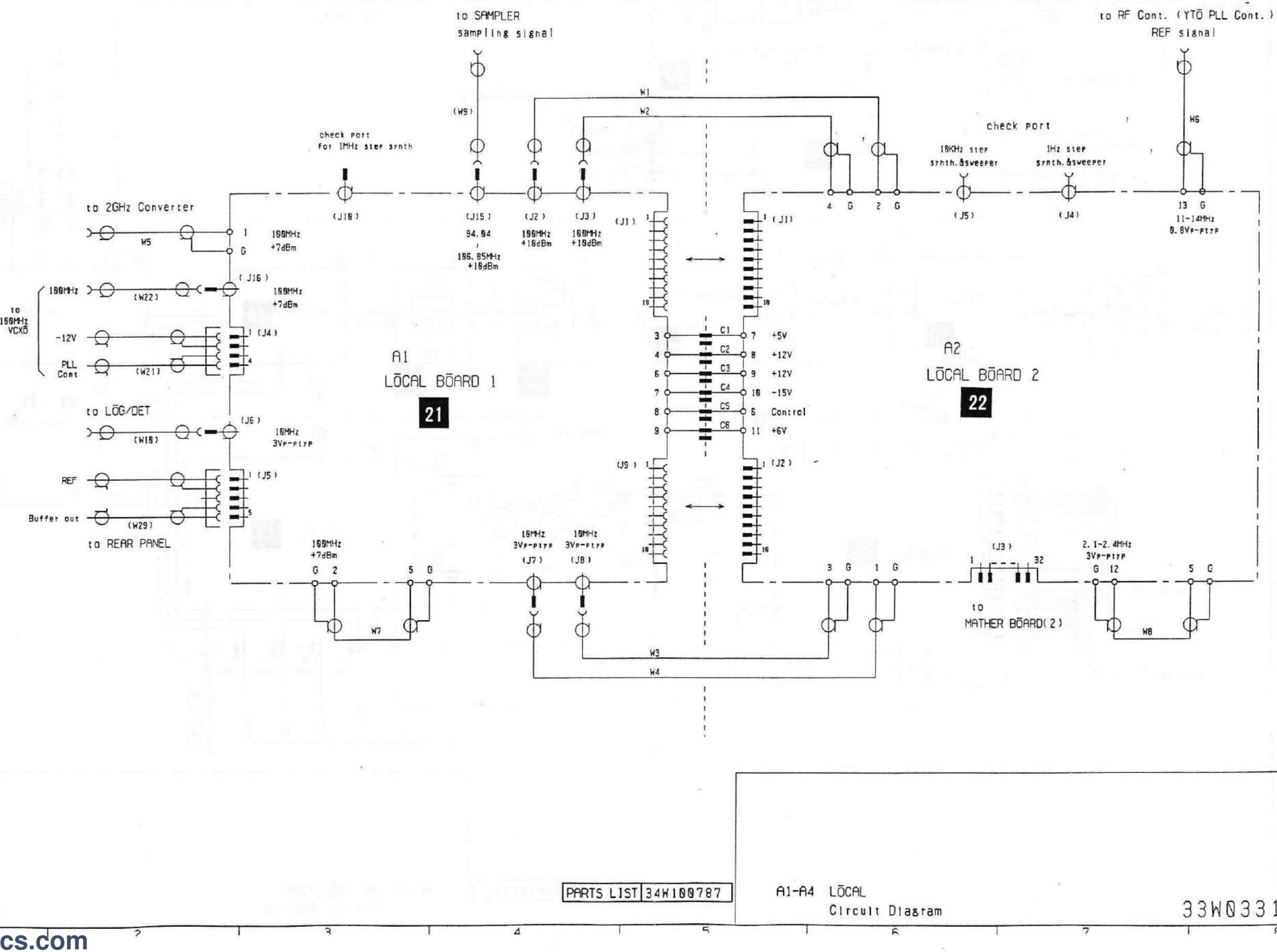


9

PARTS LIST 34W101082

A1-A3 RF CŌNVERTER
Circuit Diagram

33W033290

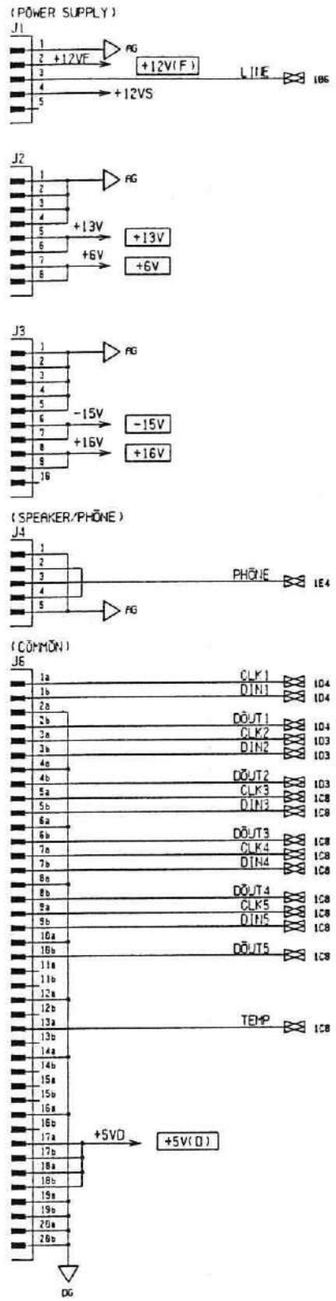


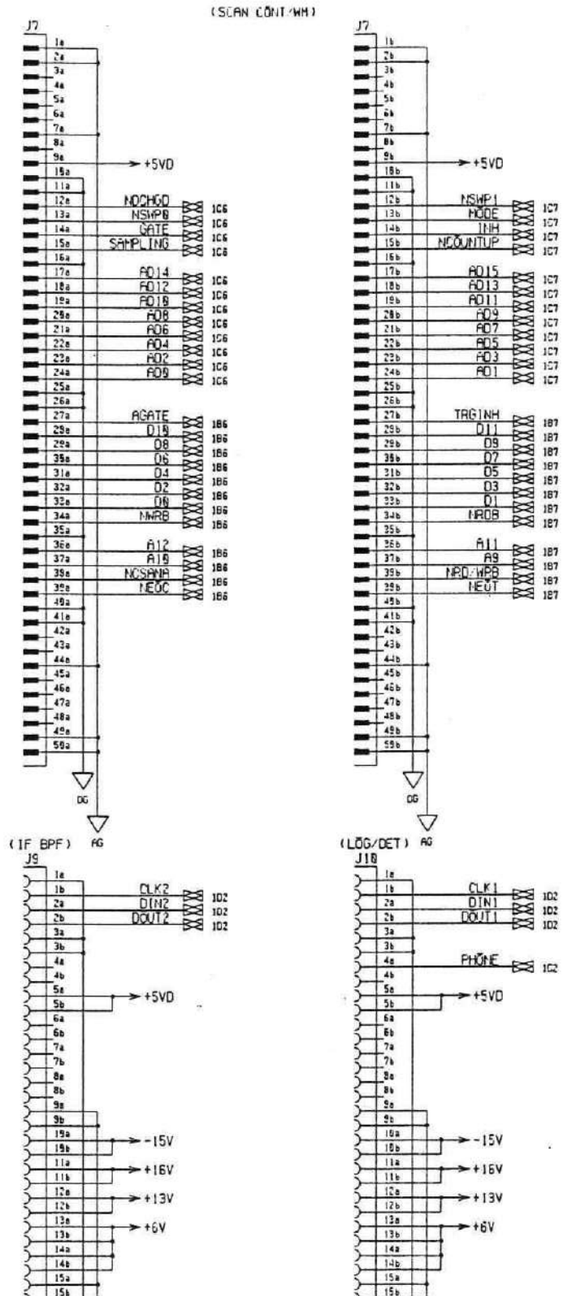
PARTS LIST 34W100787

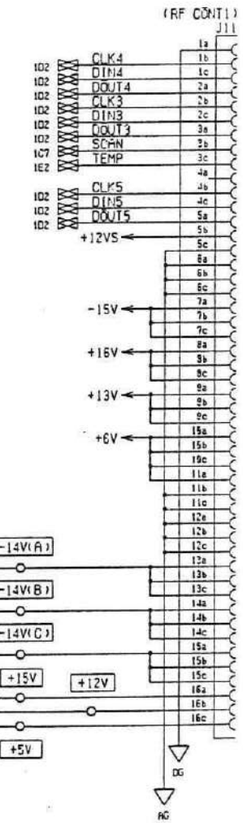
A1-A4 LOCAL
Circuit Diagram

33W033174

20







PARTS LIST 34W100962

35

A17 MOTHER BOARD
Circuit Diagram

33W033209

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3.2 Overall Troubleshooting

3.2.1 Faulty block location troubleshooting 1, 2

Basically, a spectrum analyzer is composed of Signal Route, Local Block, Digital Block, Display Unit, and Power Supply unit.

Figure 3-3 shows the way to locate the faulty block among them.

Also to know how each blocks operates can help easy troubleshooting. The information about the operation of some blocks are described below.

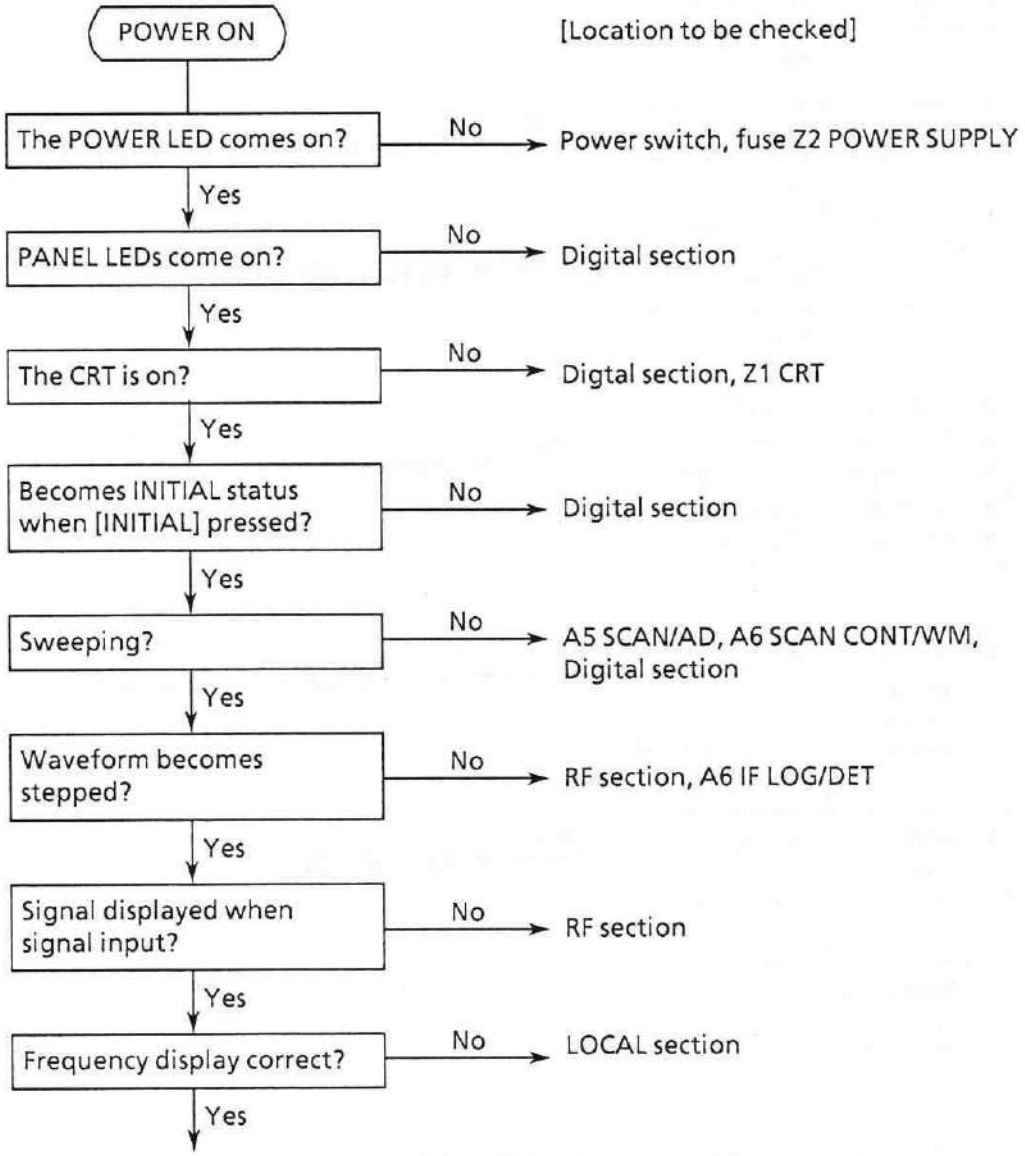

Fig. 3-3 Faulty Block Location Troubleshooting Flowchart (1/2)

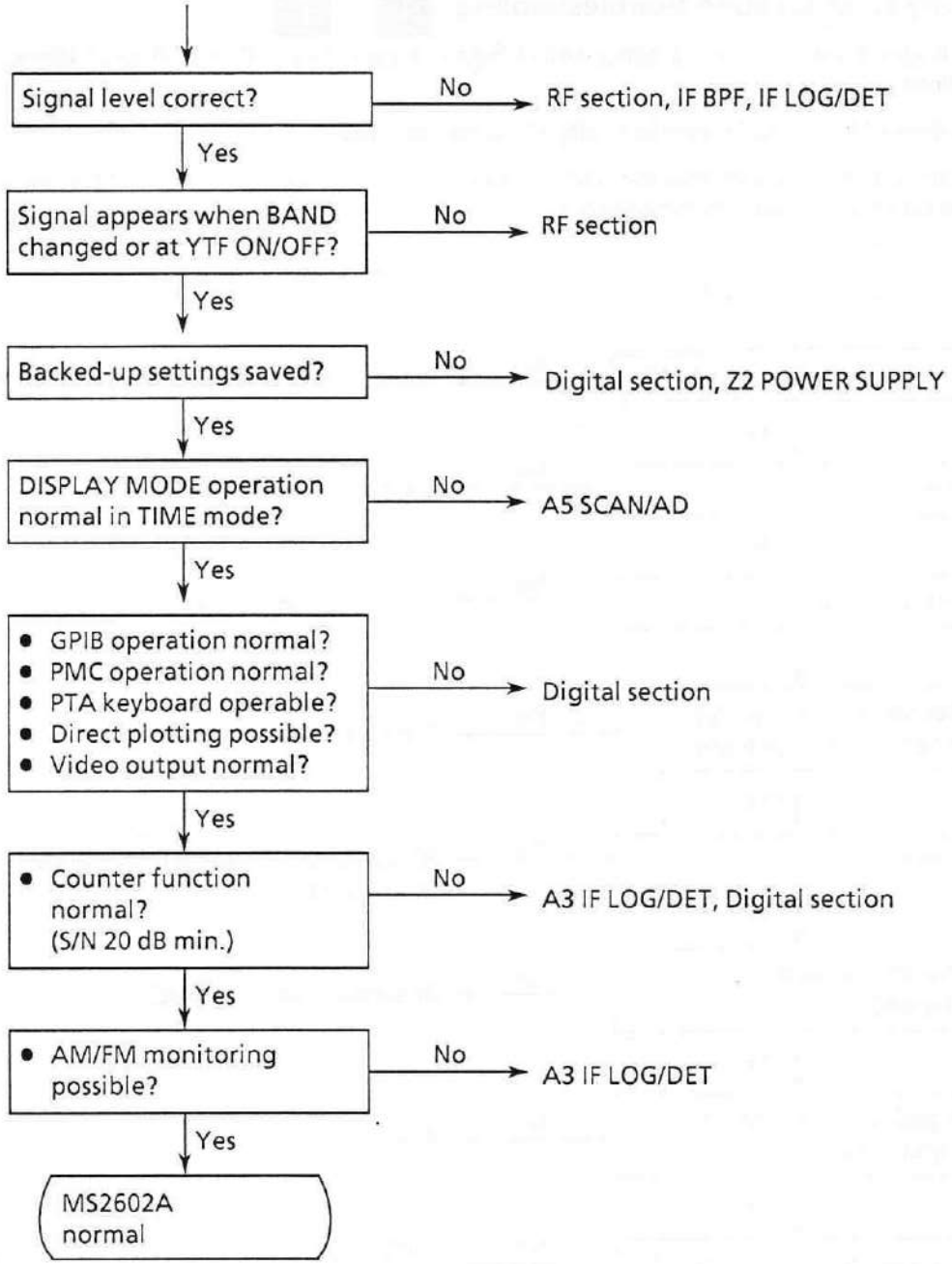

Fig. 3-3 Faulty Block Location Troubleshooting Flowchart (2/2)

3.2.2 Signal route

Refer to Fig. 2-3 A1-A3 RF CONVERTOR LEVEL DIAGRAM and Fig. 2-12 IF BPF Level Diagram.

When the signal route operates normally, the gain of the RF route and IF route are 8 dB and 3 dB respectively. Set the MS2602A as follows, and check the gain. (At first preset, then set as follows)

Center Frequency: Input Signal Frequency

Span: 0 Hz (or Time)

Reference Level: −10 dBm

Input Attenuator: 0 dB

RBW: 3 MHz

VBW: 3 MHz

When A3 IF LOG/DET operates normally A3 IF LOG/DET output +4 V DC at J 4 with 21.4 MHz, +5 dBm input at W1 .

3.2.3 Local block

(1) Sweep control circuits check

Please notice that start point in the X-axis is decided by the synthesizer and other points are decided by sweep signal.

So if the signal (image) at start frequency is normal and the signal at center or at stop frequency is abnormal, the sweep signal is faulty. In this case, check the sweep signal at ☒ on rear panel. The normal signal is shown in Fig 3-4.

If this signal is abnormal, then A5 SCAN/AD or A6 SCAN CONT/WM is faulty.

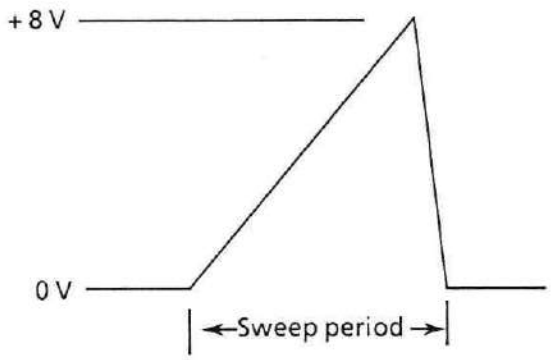

Fig. 3-4

If this signal is normal, then the sweep control circuits on A1-A4-A2 is faulty. Replace this.

(2) Synthesizer Check

The start point of X-axis is decided by the synthesizer.

The synthesizer is composed of three synthesizers of 1 MHz synthesizer, 10 kHz synthesizer, and 1 Hz synthesizer.

The pages 2-13 to 2-18 show the relationship among the start frequency and these synthesizers.

The 1 MHz synthesizer frequency can be checked at A1-A4-A1 LOCAL BOARD 1 J10.

The 10 kHz synthesizer frequency can be checked at A1-A4-A2 LOCAL BOARD 2 J5.

The 1 Hz synthesizer frequency can be checked at A1-A4-A2 LOCAL BOARD 2 J4.

Detailed troubleshooting of each blocks are explained in Part 2.

SECTION 4
OVERALL ADJUSTMENT AND CALIBRATION OF COMPENSATION DATA

4.1 Precautions

There are two overall adjustments as shown below - other adjustments are made at each units. Adjustment procedure of each units is described in Part 2.

- YTO Tuning Adjustment
- YTF Tuning Adjustment

It is necessary to execute both the YTO Tuning Adjustment and YTF Tuning Adjustment when YTO or YTF is changed.

These adjustments are performed at A1-A2-A1 RF CONT1.

Refer to Fig.

4.2 YTO Tuning Adjustment

(1) Adjusting YTO

1. Connect the LOCAL O/P (J4) to a frequency counter.
2. Set the MS2602A to BAND 1−.
3. Set TIME SPAN.
4. Connect the J7 to the GND side.

Center Freq in GHz	Local O/P Freq in MHz	Tuning Resistor	Remarks
1. 7	2221.4 ±1	R163	
4. 4786	5000 ±1	R153	
7. 4786	8000 ±1	R159	

Note: The frequency must be adjusted repeatedly three or four times →R163 →R153 →R159

After adjustment, connect the J7 to the loop side.

(2) Adjusting SWEEP SPAN

Note: Match the frequency reference of the signal generator and the MS2602A with using BUFF OUT of the MS2602A.

(a) Adjusting 1.01 to 10 MHz FREQ SPAN

1. Initialize the MS2602A.
2. Set CENTER 100 MHz and SPAN 2 MHz.
3. Input a 100 MHz from the signal generator.
4. Adjust R181 so that the image come to the center line on the MS2602A screen (use MARKER so as to minimize the error).

(b) Adjusting >10 MHz FREQ SPAN

1. Set the MS2602A to BAND 0 (0 to 2 GHz).
2. Input a 1 GHz from the signal generator.
3. Adjust R176 so that the image come to the center line on the MS2602A screen (use MARKER so as to minimize the error).

4.3 YTF Tuning Adjustment

(1) Adjusting YTF

1. Set the MS2602A to BAND 1- (1.7 to 7.5 GHz)
2. Set TIME SPAN.
3. Set CENTER 1.7 GHz.
4. Set the MS2602A PRESEL value (Shift + Cal) to +10.
5. Input 1.7 GHz from the signal generator.
6. Adjust R98 so that the received signal level on the MS2602A screen doesn't change, when shifting the PRESEL value between +10 and −10.
7. Initialize the MS2602A.
8. Set TIME SPAN.
9. Set CENTER 8.5 GHz
10. Input 8.5 GHz from the signal generator.
11. Adjust R84 so that the received signal level on the MS2602A screen doesn't change, when shifting the PRESEL value between +10 and −10.

(2) Adjusting YTF SWEEP

1. Set the MS2602A to BAND 1- (1.7 to 7.5 GHz).
2. Set the MS2602A PRESEL value (Shift + Cal) to 0.
3. Input 7.5 GHz from the signal generator.
4. Adjust R63 so that the received signal level on the MS2602A screen becomes maximum. (Evaluate at log scale 1 dB/div.)
5. Fine-adjust with R52. (Evaluate at log scale 1 dB/div.)
6. Initialize the MS2602A.
7. Set CENTER 4595 MHz.
8. Set FREQ SPAN 10 MHz.
9. Input 4.6 GHz from the signal generator.
10. Set the MS2602A PRESEL value (Shift + Cal) to 0.
11. Adjust R59 so that the received signal level on the MS2602A screen becomes maximum. (Evaluate at log scale 1 dB/div. The change is 1 dB.)

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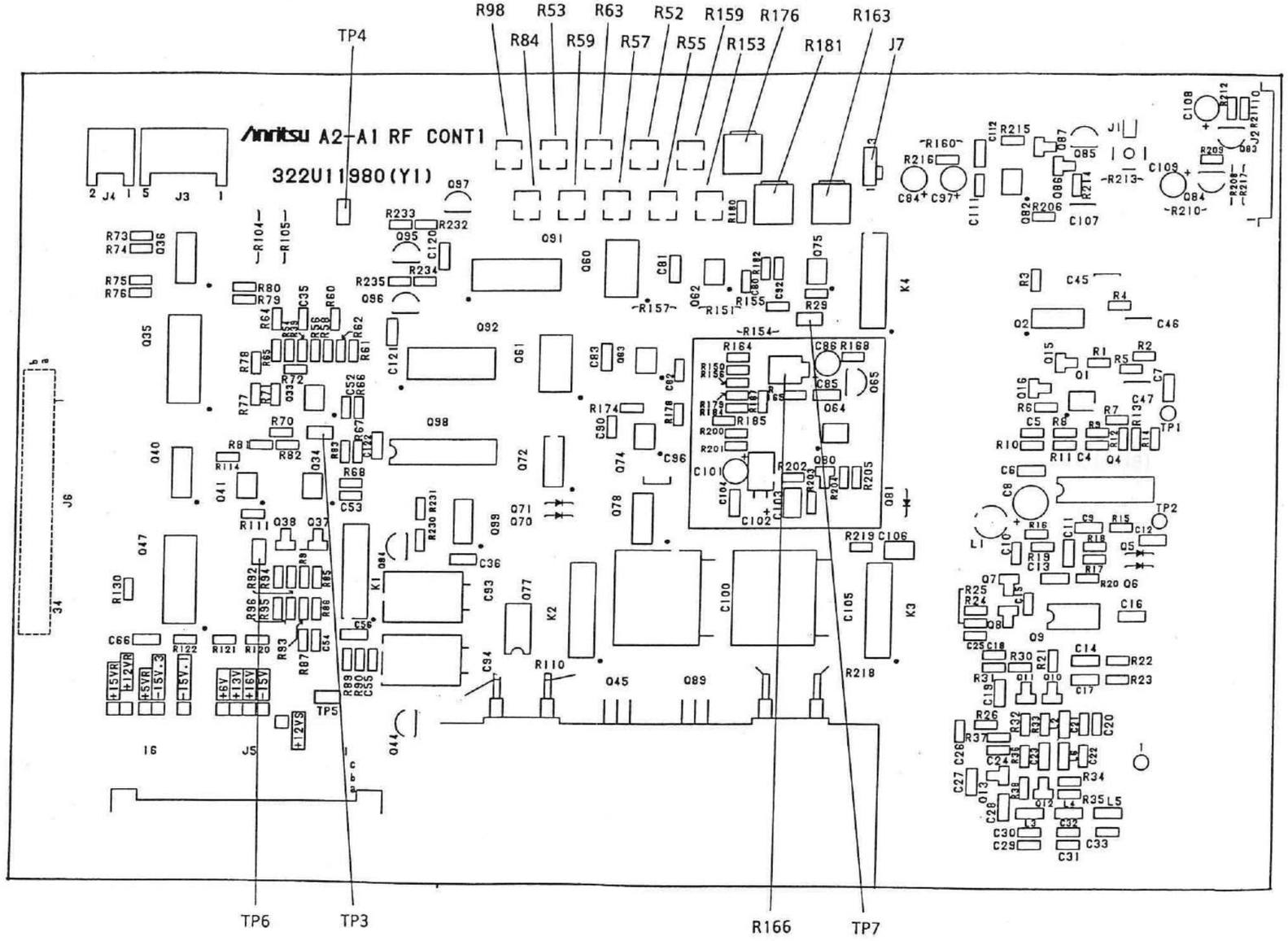

A1-A2-A1 RF CONT 1

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SECTION 5
MECHANICAL CONFIGURATION

5.1 Introduction

This section describes the mechanical structure, the position of the internal units, and the procedures for removing these units to disassemble/reassemble the MS2602A.

The numbers in Figs. 5-1 to 5-8 indicate the mechanical parts. Table 5-1 to 5-7 lists the parts with the corresponding numbers.

CAUTION

When disassembling/reassembling the MS2602A, turn off the POWER switch on the front panel and unplug the power supply cord from the ac outlet.

5.2 Cabinet Assembly

(1) Removing top cover ⑨ (Fig. 5-1)

Step	Procedure
1	Remove the two screws ⑮ and two screws ⑰. Then remove the two rear foot holders ⑦.
2	Remove one screw ⑳, and then pull out the top cover ⑨ in the rear direction by lift it rear side.

(2) Removing bottom cover ⑭ (Fig. 5-1)

Step	Procedure
1	Remove the two screws ⑮ and ⑰. Then remove the two rear foot holders ⑦.
2	Remove one screw ⑳, and then pull out the bottom cover ⑭ in the rear direction by lift it rear side.

(3) Removing side cover ⑧ (Fig. 5-1)

Step	Procedure
1	Remove the four screws ⑮, one screw ⑯, and two screws ⑰.Then remove the front foot ④, front foot holder ⑤, rear foot ⑥, and rear foot holder ⑦.
2	Remove the two screws ⑲, and then remove the side handle ③ and side cover ⑧.

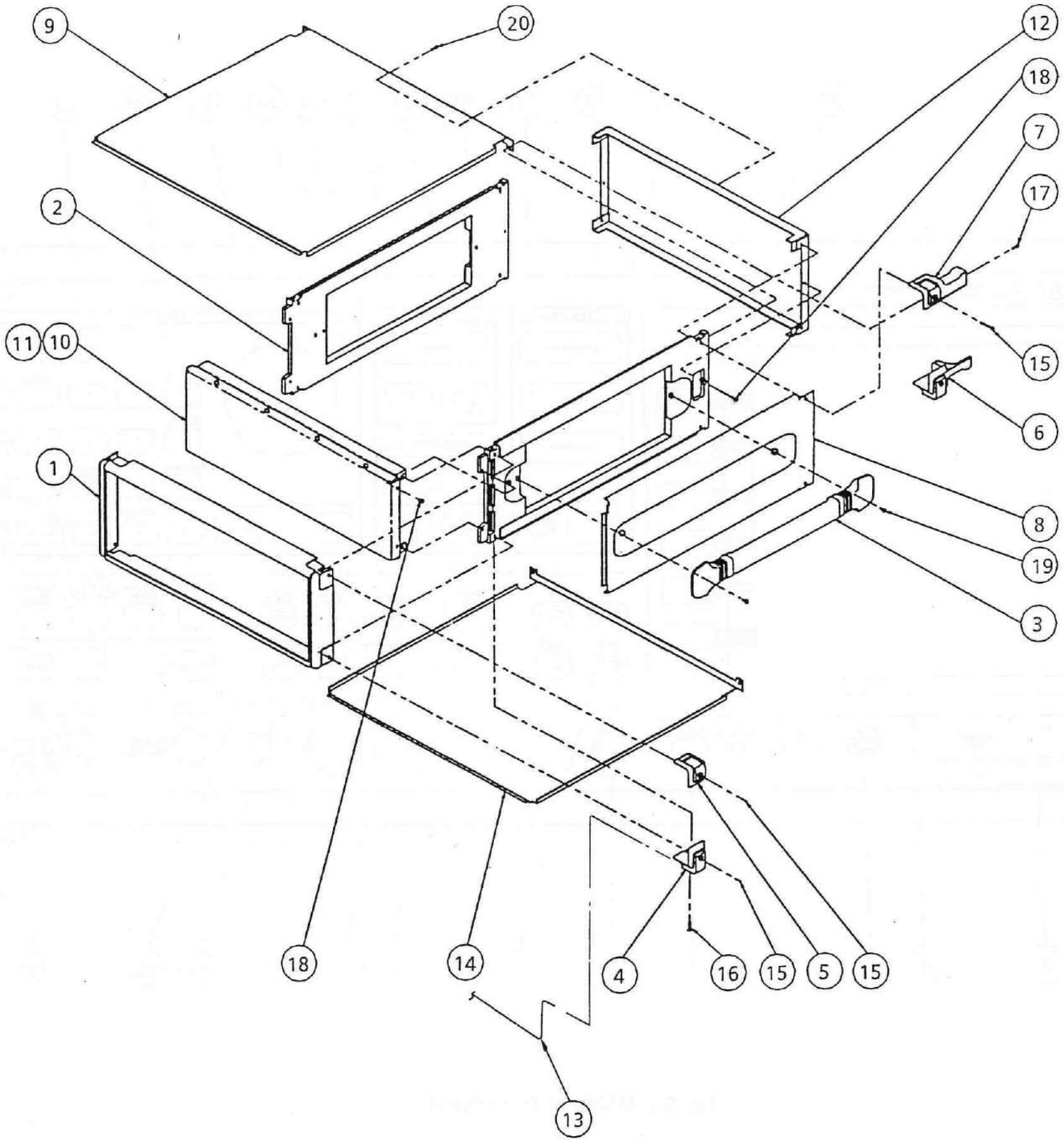

Fig. 5-1 Cabinet Assembly

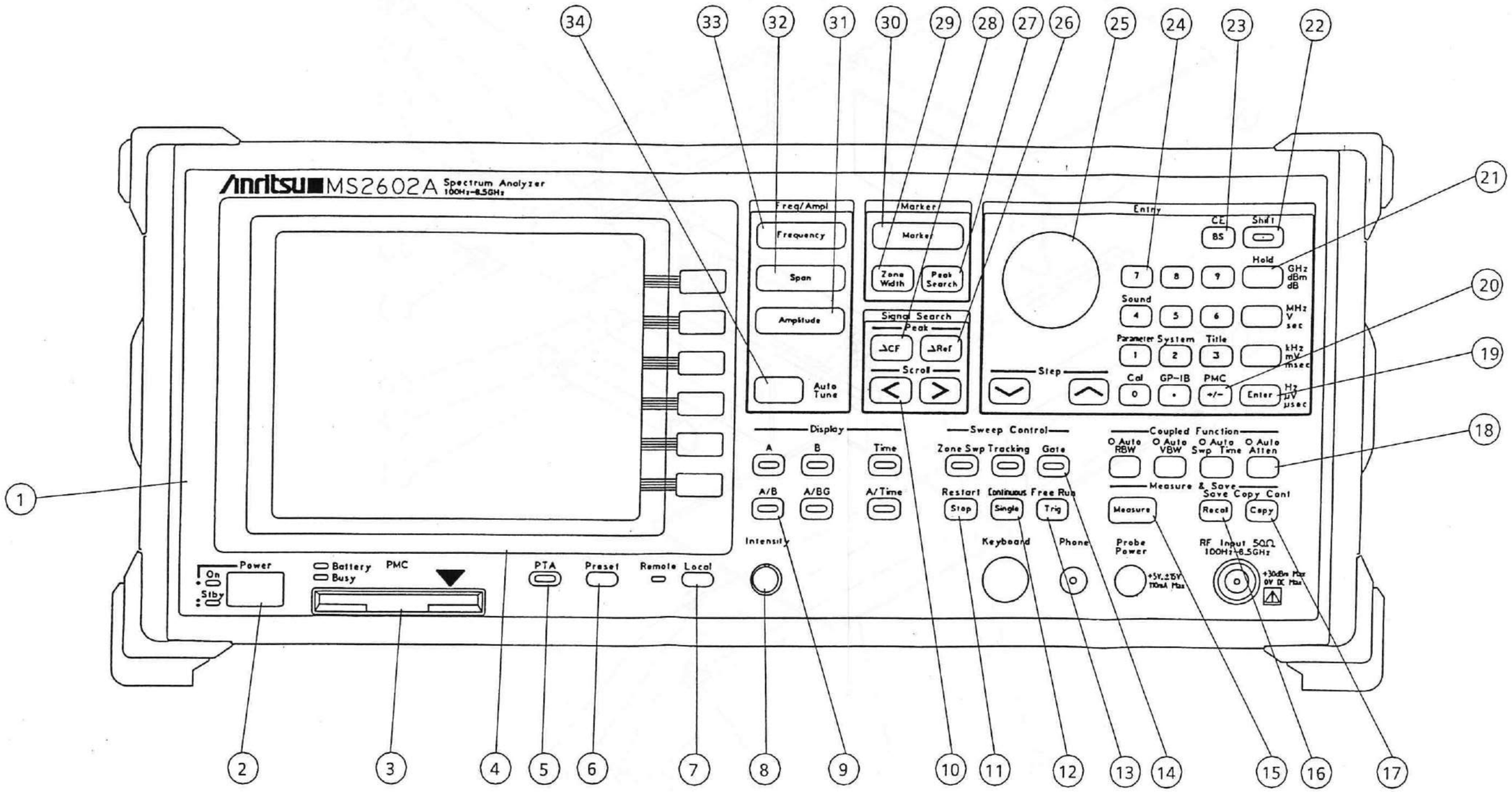

Fig. 5-2 MS2602A Front Panel

5.3 Main Unit Removal

(1) RF block/RF chassis

(2) A3: IF LOG/DET

(3) A4: IF/BPF

(4) A5, A6: SCAN block

(5) A1-A2: RF CONT

(6) A1-A3: RF CONVERTER

(7) A1-A4: LOCAL block

(8) A1-A6: 10 MHz REF

(9) Z1: P-ATTN

(10) Z2, Z3: SW, 8.5G YTF

(11) Z4: 2-8.5 GHz YTO

(12) Z8: CRYSTAL

To remove the above-mentioned units, remove the top cover, bottom cover, and side cover as described in paragraph 5.2 and follow the procedures described in the following paragraphs.

5.3.1 Removing RF block/RF chassis ① (Fig. 5-3)

Step	Procedure
1	Disconnect the W5, W6, W7, W10, W11, W23, and W29 connectors, and J2 semi-rigid cable.
2	Remove the four screws [S1] , three screws [S1] and two screws [S2] (See Fig. 5-4).
3	Lift-up the RF block together with RF chassis ①.

5.3.2 Removing A3: IF LOG/DET unit ② (Fig. 5-3)

Step	Procedure
1	Remove the six screws [S2] and plate 5 ⑤.
2	Disconnect the W1 connector from the A4 IF/BPF unit, and disconnect the W10, W13, W14, and W15 connectors .
3	Remove the two screws [S3] (See Fig. 5-4), then lift out the A3 unit ②.

5.3.3 Removing A4: IF BPF unit ③ (Fig. 5-3)

Step	Procedure
1	Follow step 1 in paragraph 5.3.2.
2	Disconnect the W1 and W11 connectors .
3	Remove one screw [S3], [S4] and [S5], and the plate 3 ⑥ and plate 4 ⑦.
4	Remove the two screws [S4] (See Fig. 5-4).
5	Loose the decorative screw ⑧ in front and in the rear with the minus screwdriver, and lift out the A4 unit ③.

5.3.4 Removing A5/A6: SCAN unit ④ (Fig. 5-3)

Step	Procedure
1	Follow step 1 in paragraph 5.3.2.
2	Disconnect the W15, W16, and W24 connectors.
3	Remove the two screws [S5] (See Fig. 5-4) and lift out the A5/A6 unit ④.

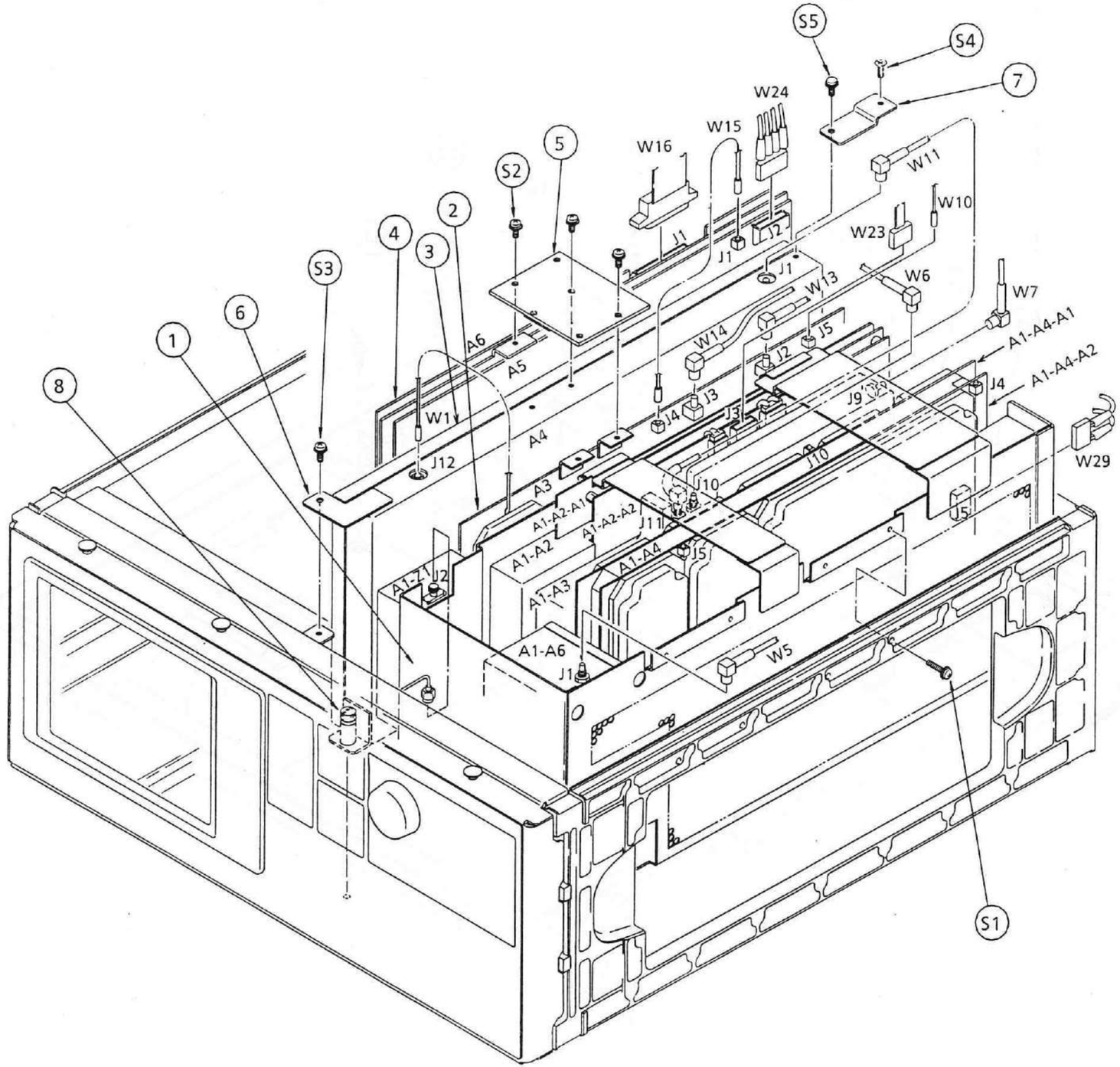

Fig. 5-3 Main Unit Removal

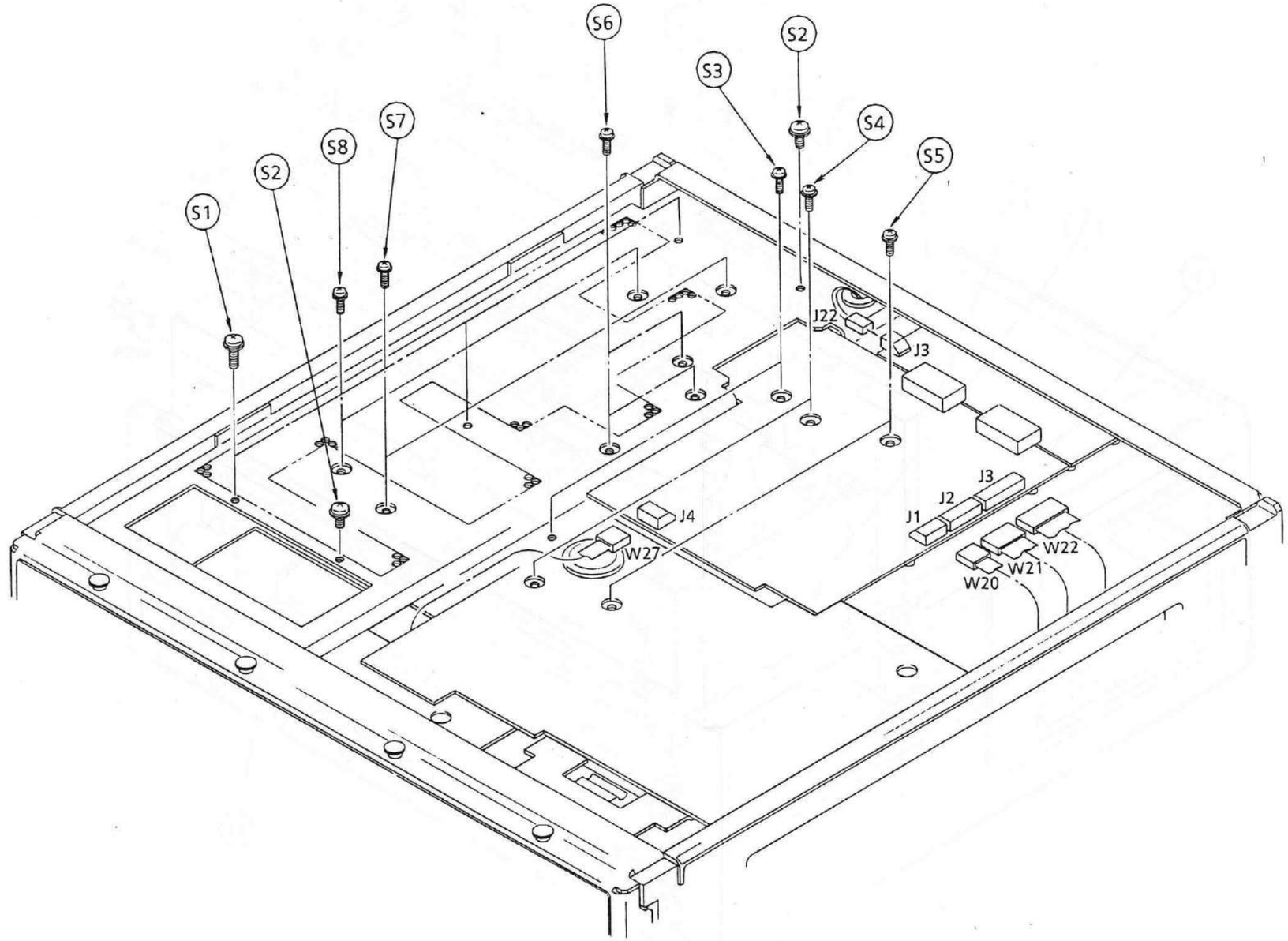

Fig. 5-4 Bottom View

5.3.5 Removing A1-A2: RF CONT unit ① (Fig. 5-5)

Step	Procedure
1	Remove the two screws [S1] and two screws [S2], and lift up the plate ⑪ and ⑫ in the above direction .
2	Disconnect the W1, W2, W3, W5, W6, and W9 connectors, and J6 semi-rigid cable .
3	Remove the three screws [S6] (See Fig. 5-4), and lift out the A1-A2 unit ①.

5.3.6 Removing A1-A3: RF CONVERTER unit ② (Fig. 5-5)

Step	Procedure
1	Follow step 1 in paragraph 5.3.5.
2	Disconnect the W5 connector, J4 and J6 semi-rigid cables.
3	Remove the two screws [S7] (See Fig. 5-4), and lift out the A1-A3 unit ② in the above direction.

5.3.7 Removing A1-A4: LOCAL unit ③ (Fig. 5-5)

Step	Procedure
1	Follow step 1 in paragraph 5.3.5.
2	Disconnect the W9, W21 and W22 connectors.
3	Remove the two screws [S8] (See Fig. 5-4), and lift out the A1-A4 unit ③ in the above direction.

5.3.8 Removing A1-A6: 10 MHz REF ④ (Fig. 5-5)

Step	Procedure
1	Perform procedures described in paragraph 5.3.1 to remove the RF chassis.
2	Disconnect the W1 connector.
3	Remove the four screws [S3] , and lift out the A1-A6 unit ④.

5.3.9 Removing Z1: P-ATT unit ⑤ (Fig. 5-5)

Step	Procedure
1	Perform procedures described in paragraph 5.3.1 to remove the RF chassis.
2	Disconnect the W2 connector and W15 semi-rigid cable.
3	Remove the four screws [S4], and lift out the Z1 unit ⑤.

5.3.10 Removing Z2, Z3: SW, 8.5G YTF ⑥, ⑦ (Fig. 5-5)

Step	Procedure
1	Perform procedures described in paragraph 5.3.1 to remove the RF chassis.
2	Disconnect the W13, W14 and W15 semi-rigid cables.
3	Remove the two screws [S5] and two screws [S6], and lift out the Z2 ⑥, Z3 ⑦, and cover ⑯.

5.3.11 Removing Z4: 2 to 8.6 GHz YTO unit ⑧ (Fig. 5-5)

Step	Procedure
1	Perform procedures described in paragraph 5.3.1 to remove the RF chassis.
2	Disconnect the W5 and W14 connectors.
3	Remove the three screws [S7], and lift out the Z4 unit ⑧.

5.3.12 Removing Z8: crystal unit ⑨ (Fig. 5-5)

Step	Procedure
1	Perform procedures described in paragraph 5.3.1 to remove the RF chassis.
2	Disconnect the W21 and W22 connectors.
3	Remove the two screws [S8], and lift out the Z8 unit ⑨ and angle ⑰.

Note: The ① to ③ units (Fig. 5-5) are removable with mounting the RF chassis at the main frame. However, it is necessary to remove the RF chassis from the main frame, when removing the ④ to ⑨ units (Fig. 5-5).

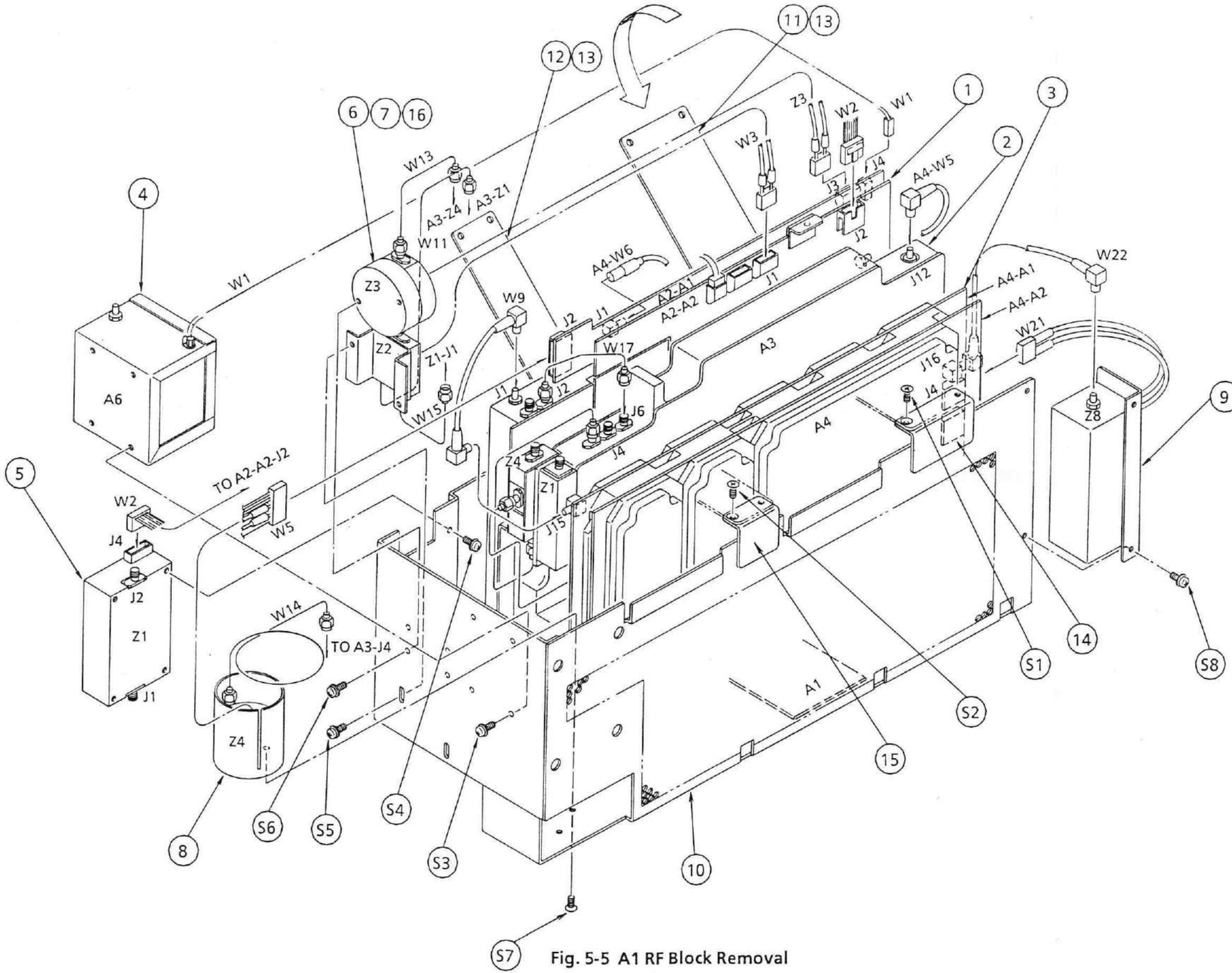

Fig. 5-5 A1 RF Block Removal

(Blank)

5.3.13 Removing front panel unit ① (Fig. 5-6)

Step	Procedure
1	Remove the four screws [S1], two screws [S2], five screws [S3] and one screw [S4] .
2	Disconnect the W1 semi-rigid cable from the J2, and pull out the front panel ① at the range of the W19, W23 and W27 length (Fig. 5-7).
3	Disconnect the W19 (Fig. 5-7), and place the front panel ① face down.
4	Remove the thirteen screws [S5] (Fig. 5-7), and remove the A15 front panel unit ①.

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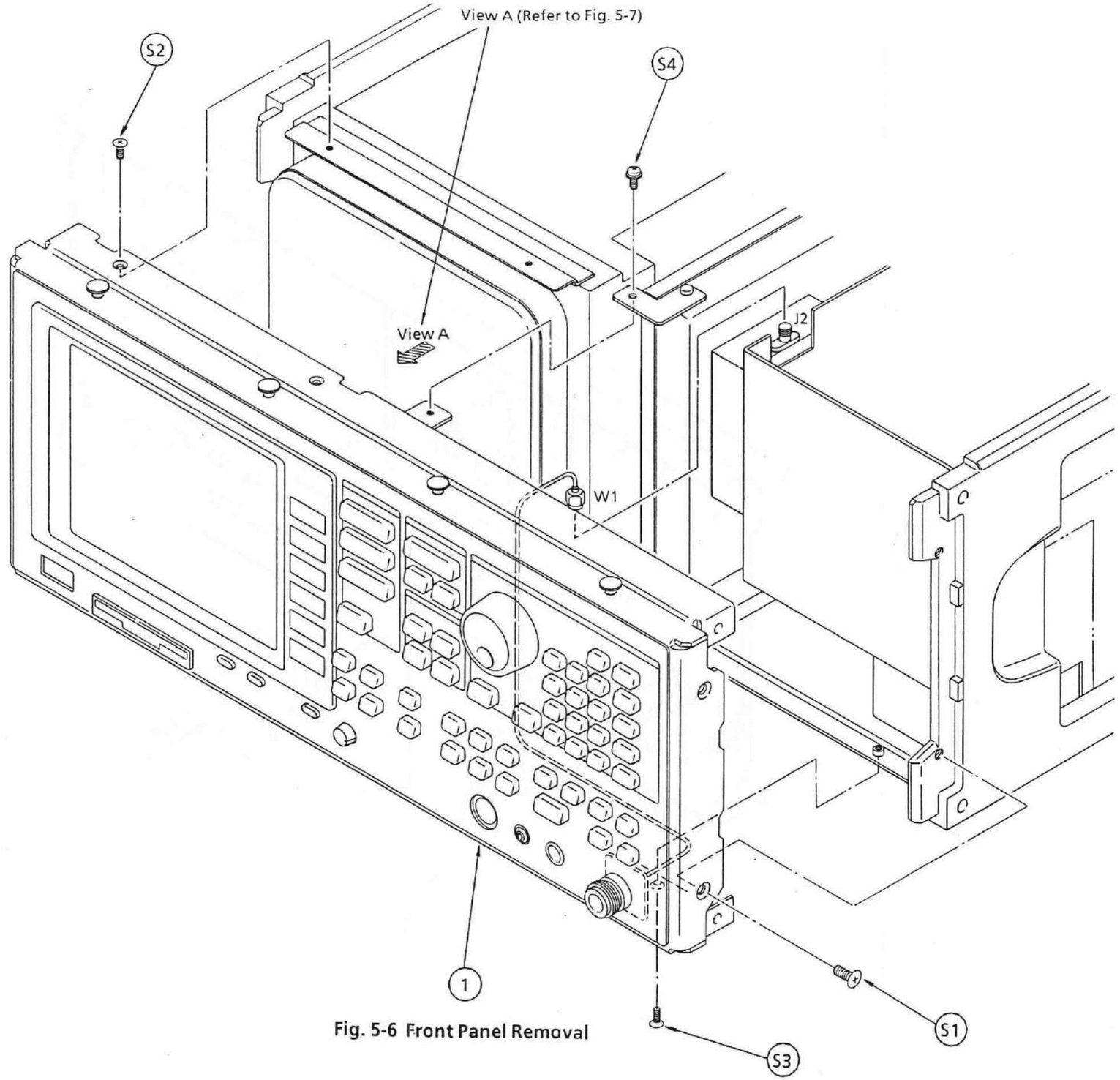

Fig. 5-6 Front Panel Removal

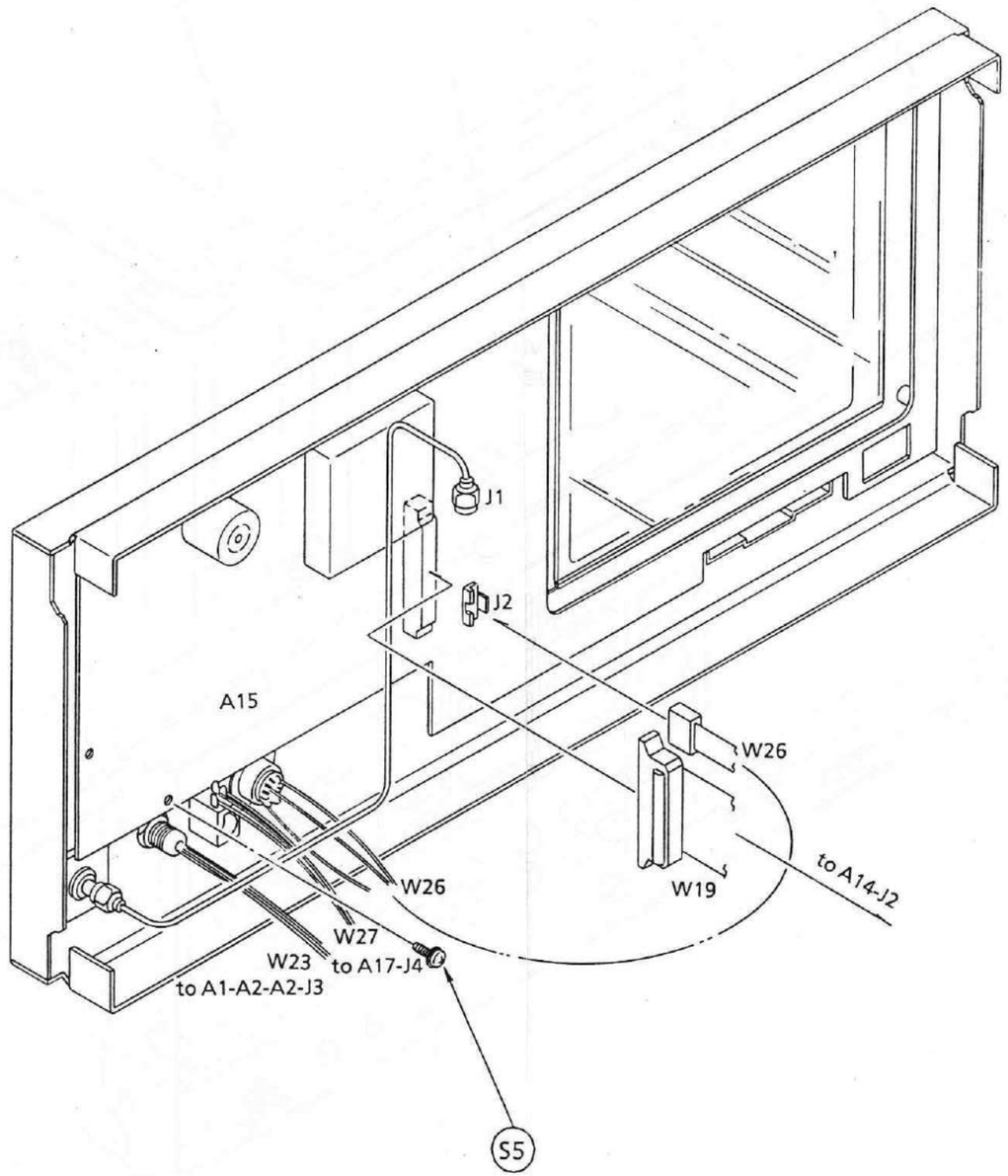

Fig. 5-7 View A

5.3.14 Removing rear decorative panel ① (Fig. 5-8)

Step	Procedure
1	Remove the five screws [S1], three screws [S2] and two screws [S3], then remove the rear decorative panel ①.

5.3.15 Removing rear panel ② (Fig. 5-8)

Step	Procedure
1	Follow step 1 in paragraph 5.3.14.
2	Remove the two screws [S4], three screws [S5] and seven screws [S6], and pull out the rear panel ② in the rear direction.

5.3.16 Removing Z2: power supply unit ③ (Fig. 5-8)

Step	Procedure
1	Follow step 1 in paragraph 5.3.14.
2	Remove the two screws [S7] and four screws [S8].
3	Disconnect the W20, W21 and W22 connector.
4	Pull out the power supply unit ③ in the rear direction.

5.3.17 Removing A10: MAIN CPU unit ④ (Fig. 5-8)

Step	Procedure
1	Follow step 1 in paragraph 5.3.14.
2	Pull out the A10 MAIN CPU ④ with holding the ejectors at the unit top and bottom.

5.3.18 Removing A9: DISP CPU unit ⑤ (Fig. 5-8)

Step	Procedure
1	Follow step 1 in paragraph 5.3.14.
2	Disconnect the W25 connector, and then disconnect the W20, W21 and W22 connectors.
3	Pull out the A9 DISP CPU ⑤ with holding the ejectors at the unit top and bottom.

5.3.19 Removing A8: MEAS CPU unit ⑥ (Fig. 5-8)

Step	Procedure
1	Disconnect the W25 connector at the A9 DISP CPU ⑤.
2	Follow step 1 in paragraph 5.3.14.
3	Pull out the A8 MEAS CPU unit ⑥with holding the ejectors at the unit top and bottom.

5.3.20 Removing A7: INTERFACE 1 unit ⑦(Fig. 5-8)

Step	Procedure
1	Disconnect the W25 connector at the A9 DISP CPU ⑤.
2	Follow step 1 in paragraph 5.3.14.
3	Disconnect the W1 connector.
4	Pull out the A7 INTERFACE 1 ⑦ with holding the ejectors at the unit top and bottom.

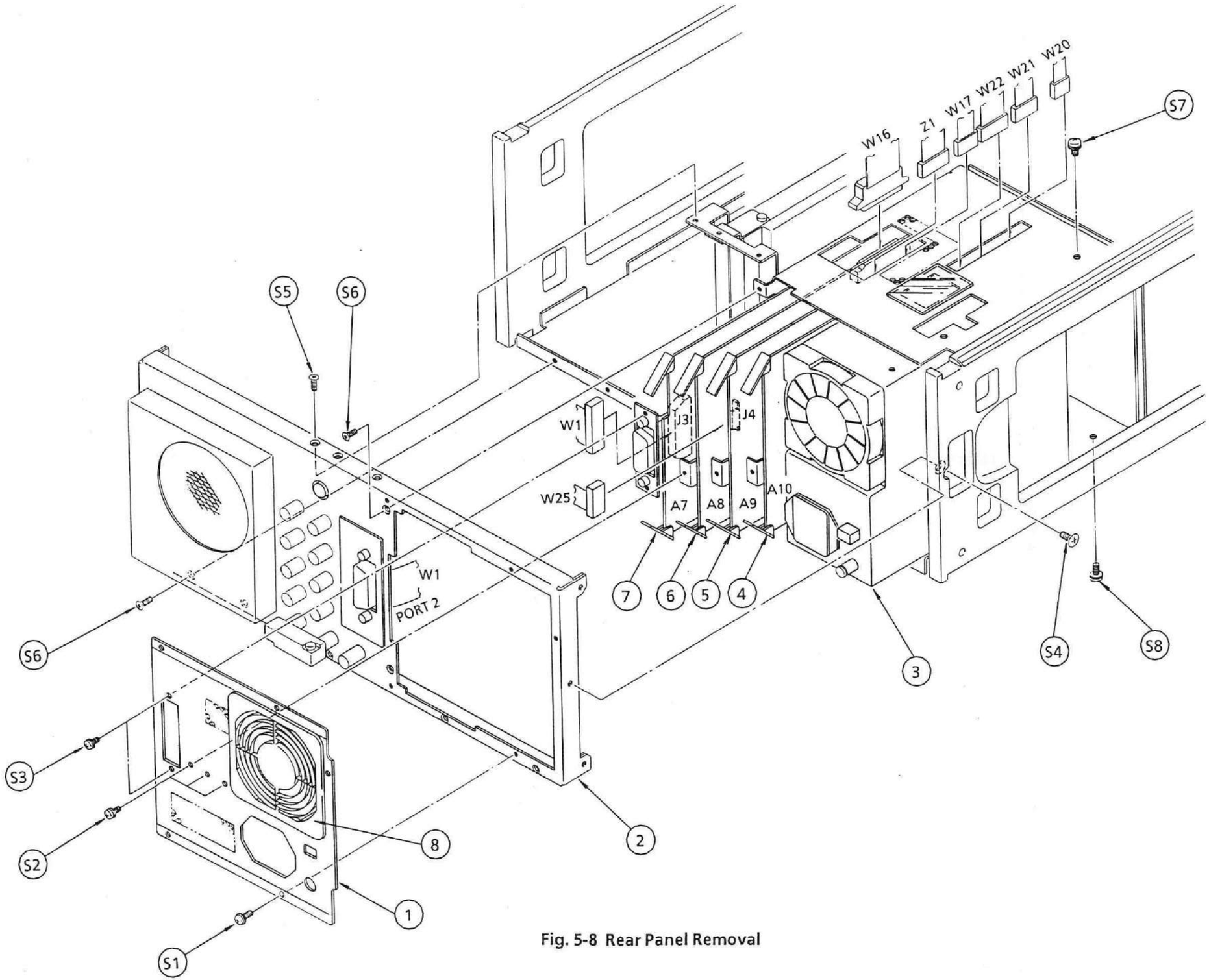

Fig. 5-8 Rear Panel Removal

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Table 5-1 Mechanical Parts List for Fig. 5-1

No.	Parts No.	Description	Qty.	Remarks
(1)	32E11762	Front Bezel	1	1MW4U
(2)	32B11788	Side Frame	2	4U450D
(3)	339E32669	Side Handle	2	450D
(4)	32E11801/32E11801B	Front Foot	1 each	L: 32E11801 R: 32E11801B
(5)	32E11802/32E11802B	Front Foot Holder	1 each	L: 32E11802B R: 32E11802
(6)	32E11803/32E11803B	Rear Foot	1 each	L: 32E11803B R: 32E11803
(7)	32E11804/32E11804B	Rear Foot Holder	1 each	L: 32E11804 R: 32E11804B
(8)	33B32684	Side Cover	2	4U450
(9)	33B33477	Top Cover	1	1MW450
(10)	322B12089	Front Panel	1	Be united with front panel sheet
(11)	32E12122	Front Panel Sheet	1	Be united with front panel
(12)	323B12061	Rear Panel	1	
(13)	34B101778	Tilt Stand	1	
(14)	33B33478	Bottom Panel	1	1MW450
(15)	5NPS24S	Decorative Screw	8	
(16)	4NPS20S7+SW+WBS	Screw	2	
(17)	4NPS10S7+SW	Screw	4	
(18)	4FPS10S7	Screw	6	
(19)	5FPS12S7	Screw	4	
(20)	4BPS10+SW	Screw	4	

Table 5-2 Mechanical Parts List for Fig. 5-2 (1/2)

No.	Parts No.	Description	Qty.	Remarks
(1)	32E12122	Front Panel Sheet	1	Be united with front panel
(2)	34E100224	Key Top	1	Power SW
(3)	33E32668	PMC Bezel	1	
(4)	332E32175	CRT Frame	1	
(5)	342E99985B	Key Top 21-ML	1	
(6)	34E99984F	Key Top 21-M	1	
(7)	34E99984B	Key Top 21-M	1	
(8)	342E73701	Knob	1	ϕ10.5
(9)	332E32851B	Key Top M8-SL	8	
(10)	332E33073B	Key Top 8×13	1 set	∧ ∨ < >
(11)	332E33445G	Key Top 6.5×10	1	Stop
(12)	332E33445H	Key Top 6.5×10	1	Single
(13)	332E33446H	Key Top 6.5×10	1	Trig
(14)	332E32851C	Key Top M8-SL	1	
(15)	342E101390A	Key Top 8×16	1	Measure
(16)	332E33447G	Key Top 6.5×10	1	Recall
(17)	332E33447F	Key Top 6.5×10	1	Copy
(18)	33E32850B	Key Top M8-S	4	
(19)	332E33449	Key Top 6.5×13	1	Enter
(20)	332E33445E	Key Top 6.5×10	1	+/−

Table 5-2 Mechanical Parts List for Fig. 5-2 (2/2)

No.	Parts No.	Description	Qty.	Remarks
(21)	33E32847C	Key Top M8-NS	3	
(22)	332E32848E	Key Top M8-NSL	1	
(23)	332E33445F	Key Top 6.5×10	1	BS
(24)	332E33445A	Key Top 6.5×10	1 set	0 to 9, ·
(25)	33E32858	Encoder Knob	1	
(26)	332E33073V	Key Top 8×13	1	↘Ref
(27)	332E33073T	Key Top 8×13	1	Peak Search
(28)	332E33073U	Key Top 8×13	1	↘Cf
(29)	332E33073S	Key Top 8×13	1	Zone Width
(30)	332E33450D	Key Top 8×30	1	Marker
(31)	332E33450C	Key Top 8×30	1	Amplitude
(32)	332E33450B	Key Top 8×30	1	Span
(33)	332E33450A	Key Top 8×30	1	Frequency
(34)	33E32846B	Key Top M8-L	1	

Table 5-3 Mechanical Parts List for Fig. 5-3

No.	Parts No.	Description	Qty.	Remarks
(1)		RF Block	1	
(2)		A3: IF LOG/DET	1	
(3)		A4: IF/BPF	1	
(4)		A5,A6: SCAN	1	
(5)	342B101165	Plate 5	1	
(6)	34B101163	Plate 3	1	
(7)	342B101164	Plate 4	1	
(8)	ES2B-36	Decorative Screw	2	
S1	3NPS14B3+SW	Screw	4	
S2	3NPS8B3+SW	Screw	6	
S3	3NPS8B3+SW	Screw	1	
S4	3NPS10B3+SW	Screw	1	
S5	3NPS8B3+SW	Screw	1	

Table 5-4 Mechanical Parts List for Fig. 5-4

No.	Parts No.	Description	Qty.	Remarks
S1	4NPS10B3+SW	Screw	3	
S2	4NPS6B3+SW	Screw	2	
S3	3NPS8B3+SW	Screw	2	
S4	3NPS8B3+SW	Screw	2	
S5	3NPS8B3+SW	Screw	2	
S6	3NPS8B3+SW	Screw	3	
S7	3NPS8B3+SW	Screw	2	
S8	3NPS8B3+SW	Screw	2	

Table 5-5 Mechanical Parts List for Fig. 5-5 (1/2)

No.	Parts No.	Description	Qty.	Remarks
(1)		A1-A2: RF CONT	1	
(2)		A1-A3: RF CONVERTER	1	
(3)		A1-A4: LOCAL	1	
(4)		A1-A6: 10 MHz REF	1	
(5)		Z1: P-ATT	1	
(6)		Z2: SW	1	
(7)		Z3: 8.5G YTF	1	
(8)		Z4: 2-8.5 GHz YTO	1	
(9)		Z8: Crystal	1	
(10)	333B33338	RF Chassis	1	
(11)	342B101245	Plate 1	1	
(12)	342B101246	Plate 2	1	
(13)	342B101278	Hinge	2	
(14)	342B101247	Angle	1	
(15)	342B101248	Angle	1	
(16)	342B102170	Cover	1	
(17)	34B101776	Angle	1	

Table 5-5 Mechanical Parts List for Fig. 5-5 (2/2)

No.	Parts No.	Description	Qty.	Remarks
S1	3FPS5B3	Screw	2	
S2	3FPS5B3	Screw	2	
S3	3NPS8B3+SW	Screw	4	
S4	3NPS6B3+SW	Screw	4	
S5	2.6NPS8B3+SW+WB	Screw	2	
S6	3NPS5B3+SW	Screw	2	
S7	3FPS5B3	Screw	3	
S8	3NPS8B3+SW	Screw	2	

Table 5-6 Mechanical Parts List for Figs. 5-6 and 5-7

No.	Parts No.	Description	Qty.	Remarks
(1)		Front Panel	1	
S1	4FPS10S7	Screw	4	
S2	3FS8B3	Screw	2	
S3	3FPS8B3	Screw	5	
S4	3NPS8B3+SW	Screw	1	
S5	3NPS6B3+SW	Screw	13	

Table 5-7 Mechanical Parts List for Fig. 5-8

No.	Parts No.	Description	Qty.	Remarks
(1)	333B33341	Rear Decorative Plate	1	
(2)		Rear Panel	1	
(3)		Z2: Power Supply	1	
(4)		A10: MAIN CPU	1	
(5)		A9: DISP CPU	1	
(6)		A8: MEAS CPU	1	
(7)		A7: INTERFACE 1	1	
(8)	34Z98116	Fan Guard	1	FRP-80
S1	4NPS10B3+SW	Screw	5	
S2	3NPS8B3+SW	Screw	3	
S3	3NPS8B3+SW	Screw	2	
S4	4FPS10S7	Screw	2	
S5	3FPS8B3	Screw	3	
S6	3FPS8B3	Screw	7	
S7	4NPS8B3+SW	Screw	2	
S8	4NPS8B3+SW	Screw	4	