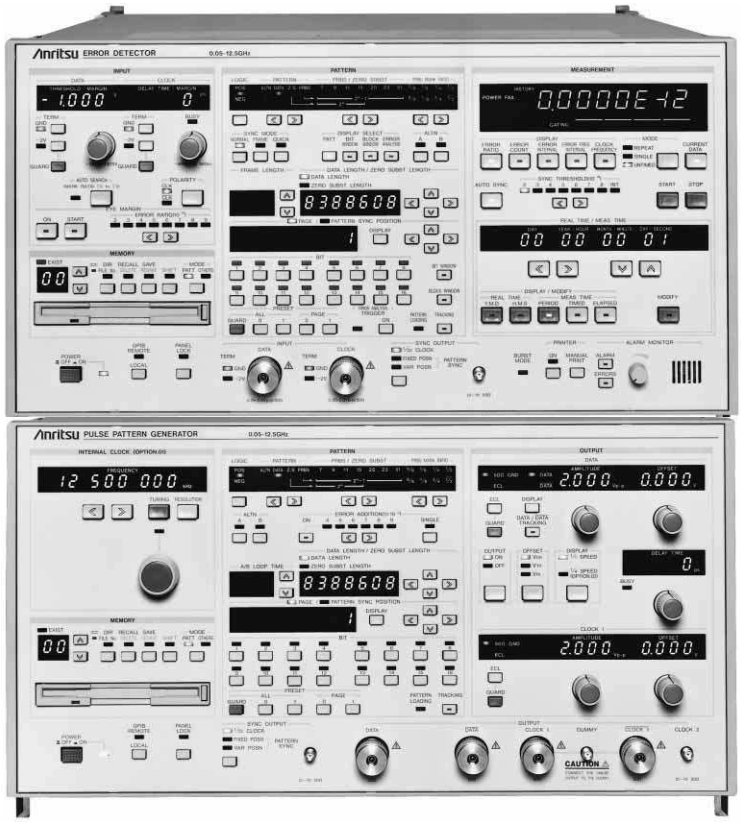
Anritsu

MP1763C/1764C

Pulse Pattern Generator/Error Detector

50 MHz to 12.5 GHz



High-Quality, Low-Jitter, Low-Distortion Waveform Output
12.5 Gbit/s BERTS with Higher Performance and Lower Price

High-Speed/Wide Band, High Quality Waveform and Advanced Functions

High-speed base transmission links are being constructed to transmit the large amount of information which will be required by the future multimedia age. Many countries are carrying out research and development and testing prototype STM-64/OC-192 (9.953 Gbit/s) transmission systems. An 11 Gbit/s optical submarine transmission system is also being tested. The MP1763C Pulse Pattern Generator/MP1764C Error Detector are 12.5 Gbit/s BERTS (Bit Error Rate Test Set) developed for evaluation and inspection of 10 Gbit/s transmission equipment, modules, and devices.

10 Gbit/s Ethernet

- The most suitable for evaluating device of 3.125 Gbit/s x 4 ch and 12.5 Gbit/s x 1 ch (It is necessary for output of 3.125 Gbit/s x 4 ch to install MP1763C-03 1/4 speed output).

High-speed and wide band

One MP1763C/MP1764C can cover the band from STM-0/STS-1 to STM-64/STS-192 and can be used with 11 Gbit/s optical submarine transmission systems.

Many patterns

- 8 Mbit programmable pattern (corresponding to six frames of STM-64/STS192)
- PRBS patterns from $2^7 - 1$ to $2^{31} - 1$
- PRBS pattern with randomness and mark ratio variance for rigorous testing
- Alternating pattern
  The MP1763C alternately sends normal and alarm patterns to a device for response testing.
- Zero substitution pattern
  This feature is effective for testing the clock regeneration of a 3R repeater.

Trigger location of pattern synchronization signal can be changed.

This feature makes it simple to monitor the waveform at any point in a long word pattern.

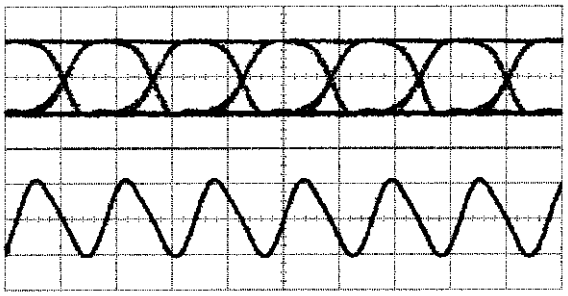
- High Q factor
  A high Q factor can be obtained by back to back connection (typical value at 10 Gb/s, PRBS $2^{23} - 1$: 40 dB).

Pulse Pattern Generator

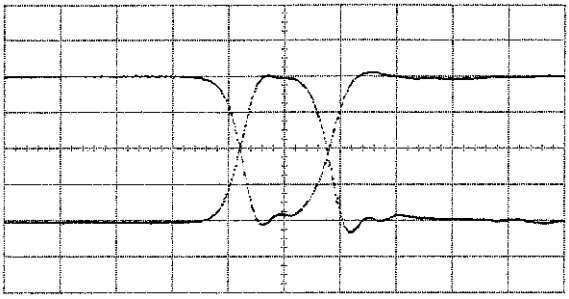
High-quality waveform

- t_r/t_f (10% to 90%): 30 ps (typical)
- Jitter: 10 ps_{p-p} (typical)
- Back termination for low waveform distortion
- A pattern of isolated pulses which do not depend on mark ratios.

MP1763C output waveform



H: 50 ps/div, V: 1 V/div
DATA output of 12.5 GHz (top trace)
CLOCK 1 output (bottom trace)



H: 50 ps/div, V: 0.5 V/div
Isolated pattern (superimposition of 1/64 bits and 63/64 bits)

High resolution clock and data output

- Output amplitude: 0.25 to 2 Vp-p (2 mV steps)
- Output offset: –2 to +2 V (1 mV steps)
- Delay (clock): –500 to +500 ps (1 ps steps)
- DATA/$\overline{\text{DATA}}$ independently variable

Burst signal generation using external gate signal

This feature is effective for optical fiber-loop testing, etc.

1/8 (1/4) speed parallel output interface (standard: 8-bit parallel, option: 4-bit parallel)

This feature is effective for testing 8:1 multiplexer ICs and optical WDM transmission. (However, the 1/8 speed interface and 1/4 speed interface cannot be installed simultaneously.)

Error Detector

High input sensitivity and wide phase margin

- Input sensitivity: 50 mVp-p (typical value at 10 Gb/s, PRBS $2^{23} – 1$)
- Phase margin: 70 ps or more (typical value at 10 Gb/s, PRBS $2^{23} – 1$)

Eye margin measurement

The phase margin and threshold margin can be measured and displayed for any error rate.

Burst measurement possible

- The burst data can be measured even for the PRBS and programmable patterns.
- High-speed synchronization gain is achieved by a quick synchronous method (typical sync. gain time at 10 Gb/s, programmable pattern length of 2048 bits, sync. threshold at E-2: 850 ns).

Selectivity BER measurement in bit units

The bit errors can be measured for any block of 32-bit segments or any bit.

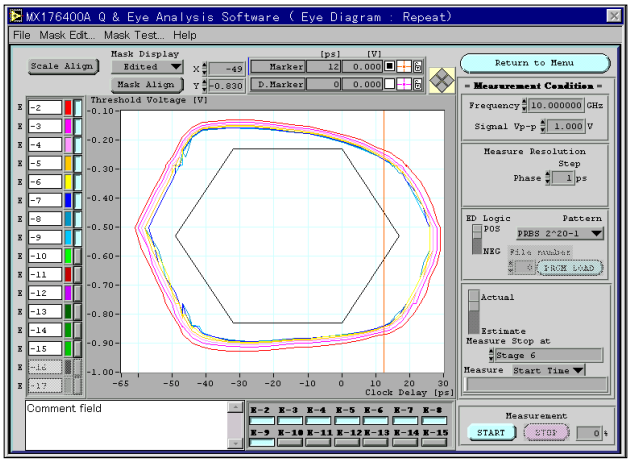
Error analysis function (option)

The pattern (256 bits in total) before and after a bit in which an error occurred can be displayed. Also, insertion and omission errors are displayed using different LED colors.

Application Software

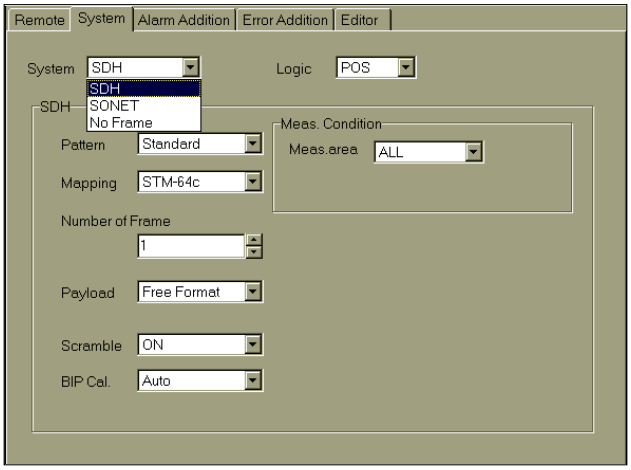
MX176400A Q/Eye Analysis software

- Eye diagram and eye margin automatic measurement
- Displays a mask figure for the evaluation on the screen
- Q-factor (ITU-T G.976) automatic measurement

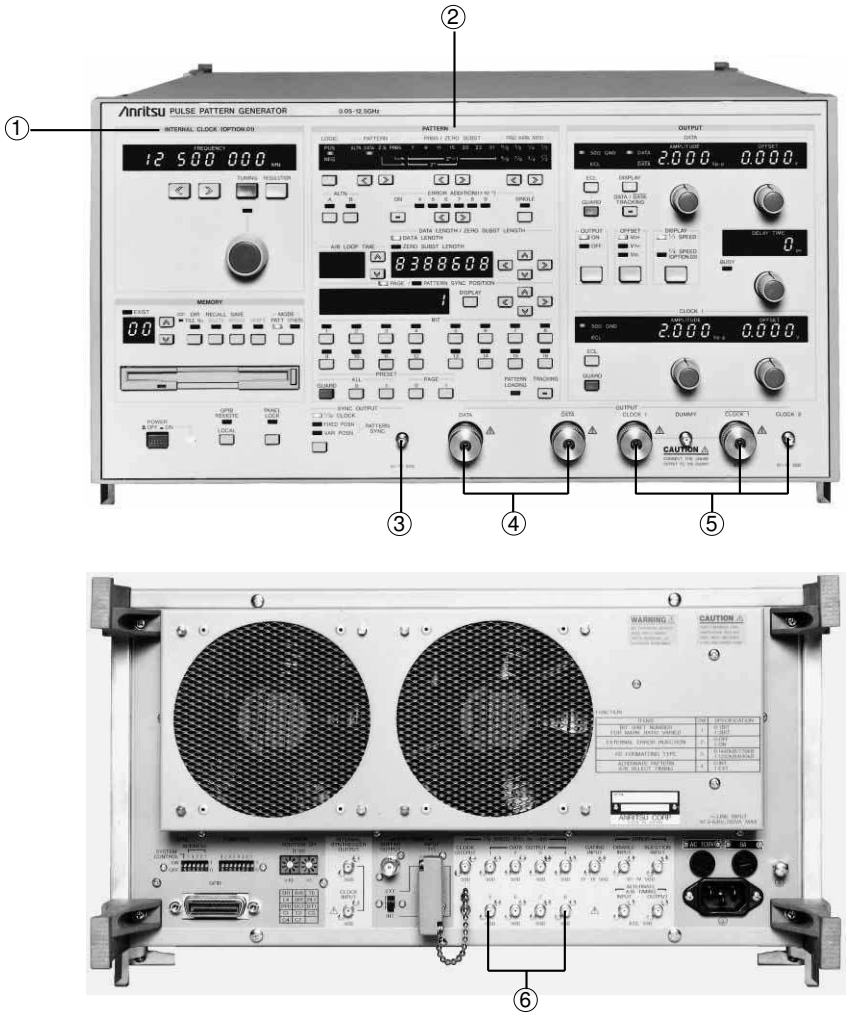


MX176401A SDH/SONET Pattern Editor

- Support OC-1 (STM-0) to OC-192c (STM-64c) mapping
- Alarm addition (OOF, LOF, MS-AIS, REI, RDI)
- BIP error addition (B1, B2, B3)
- Support “No frame” pattern



MP1763C Pulse Pattern Generator



① **Internal clock (Option 01)**
Can be set in units of 1 kHz or 1 MHz over the range from 50 MHz to 12.5 GHz

② **Programmable patterns**
- 8-Mbit programmable pattern (can set six STM-64 frames)
- 4-Mbit alternate pattern
- Zero substitution pattern
- PRBS pattern from $2^7 - 1$ to $2^{31} - 1$ selectable and its mark ratio can be varied.

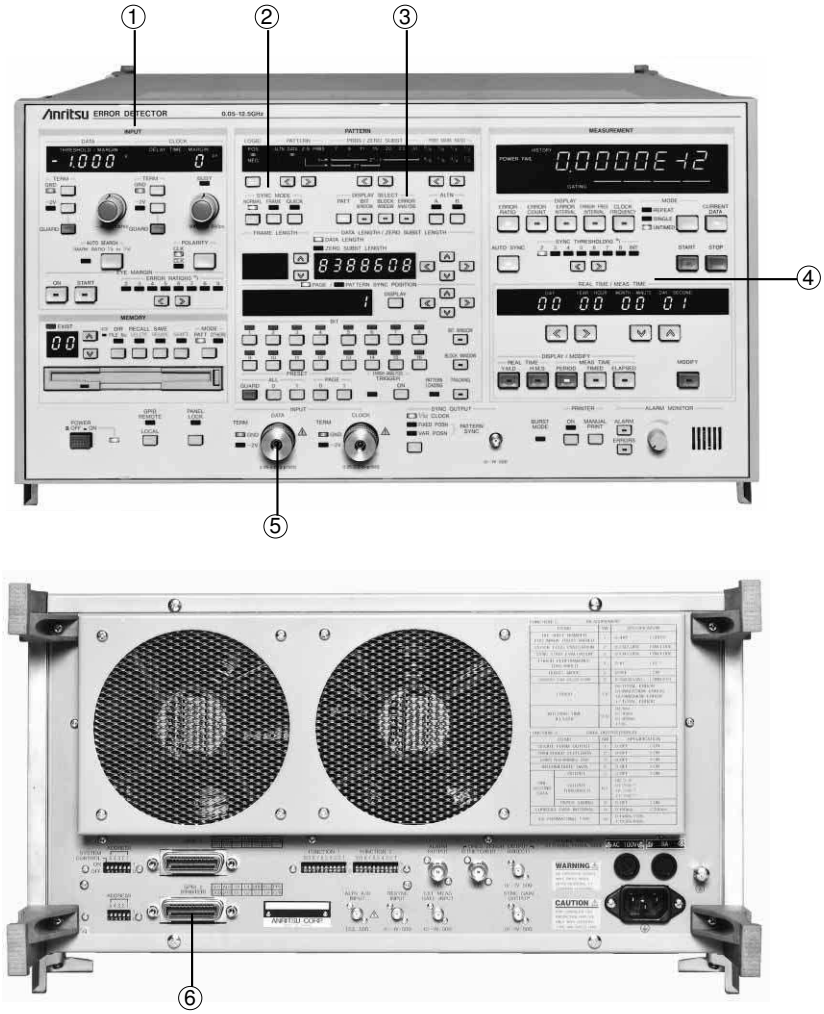
③ **Synchronous output**
The 1/64 clock or pattern SYNC selectable
The trigger position variable for the pattern SYNC

④ **DATA output**
DATA/$\overline{\text{DATA}}$ complementary output with back termination

⑤ **Clock output**
CLOCK 1/$\overline{\text{CLOCK 1}}$, CLOCK 2 (3 systems)
CLOCK 1/$\overline{\text{CLOCK 1}}$ with back termination

⑥ **1/8 speed output**
Useful for testing an 8:1 MUX
(changeable to 1/4 speed output with option)

MP1764C Error Detector



① **Eye margin measurement**
Displays the phase margin and threshold margin

② **Synchronous mode**
High-speed sync. gain is achieved in frame and quick synchronous modes.

③ **Error analysis (Option 01)**
The input pattern before and after a bit in which an error occurred can be checked.

④ **Synchronous threshold**
The sync. gain and sync. loss conditions can be set.

⑤ **DATA input**
Has a high input sensitivity

⑥ **Two GPIB connectors**
One is used for an external printer.

Specifications

MP1763C Pulse Pattern Generator

Operation frequency		0.05 to 12.5 GHz
Internal clock (option 01)	Frequency range	0.05 to 12.5 GHz
	SSB phase noise (at 10 kHz offset, 1 Hz bandwidth)	≤–85 dBc/Hz (0.05 to 4 GHz), ≤–80 dBc/Hz (4 to 8 GHz), ≤–75 dBc/Hz (8 to 10 GHz), ≤–70 dBc/Hz (10 to 12.5 GHz)
External clock input level		0.4 to 2.5 Vp-p
Pattern	Pseudorandom binary sequence pattern (PRBS)	Pattern: $2^n - 1$ (n: 7, 9, 11, 15, 20, 23, 31) Mark ratio: 1/2, 1/4, 1/8, 0/8 ($\overline{1/2}$, 3/4, 7/8, 8/8 are possible with logic inversion) Bit shifts number for mark ratio varied: 1, 3 bits selectable
	Data pattern	Data length: 2 to 8388608 bits
	Alternate pattern	A/B pattern data length: 128 to 4194304 bits (128 bit steps); Loop time: A, B pattern (1 to 127, 1 steps)
	Zero substitution pattern	Zero bit length: 1 to (pattern length – 1) bits; Pattern: 2^n (n: 7, 9, 11, 15)
	Error addition	Error rate: 10^{-n} (n: 4, 5, 6, 7, 8, 9), and single error External error injection: Provided
Data output	Number of outputs	2 (DATA/$\overline{\text{DATA}}$ independently)
	Amplitude	0.25 to 2 Vp-p, 2 mV steps
	Offset voltage	V_{OH}: –2 to +2 V, 1 mV steps Display: V_{OH}, V_{TH} or V_{OL} selectable
	Rise/fall time	Typical 30 ps (10% to 90% of amplitude)
	Pattern jitter	≤20 psp-p, typical 10 psp-p
	Waveform distortion (0-peak)	≤15% or ≤150 mV whichever is greater
	Gating input	Provided
	Load impedance	50 Ω (with back termination)
	Connector	APC-3.5
	DATA/$\overline{\text{DATA}}$ tracking	$\overline{\text{DATA}}$ amplitude and offset voltage can be set to the same values as for DATA.
	Cross point adjustment function	The cross point of DATA and $\overline{\text{DATA}}$ outputs can be adjusted at semifixed resistor of side.
Clock output	Number of outputs	3 (CLOCK 1/$\overline{\text{CLOCK 1}}$, CLOCK 2)
	Amplitude	CLOCK 1/$\overline{\text{CLOCK 1}}$: 0.25 to 2 Vp-p (2 mV steps) CLOCK 2: 1 Vp-p
	Offset voltage	CLOCK 1/$\overline{\text{CLOCK 1}}$: V_{OH} –2 to +2 V (1 mV steps) CLOCK 2: V_{OH} 0 V fixed
	Rise/fall time	Typical 30 ps (10% to 90% of amplitude)
	Load impedance	50 Ω (CLOCK 1/$\overline{\text{CLOCK 1}}$: with back termination)
	Connector	CLOCK 1/$\overline{\text{CLOCK 1}}$: APC-3.5, CLOCK 2: SMA
	Delay	±500 ps (1 ps steps)
1/8 data and clock output		Number of outputs: DATA 8, CLOCK 1 Output level: ECL Connector: SMA
1/4 data and clock output (option 03)*1	Number of outputs	DATA: 4, CLOCK: 1
	Amplitude	0.5 to 2 Vp-p (2 mV steps)
	Offset voltage	V_{OH}: –1.5 to +1.5 V (1 mV steps)
	Connector	SMA
Sync. signal output	Number of outputs	1 (1/64 clock, fixed position pattern, or variable position pattern selectable)
	Output level	0/–1 V
	Connector	SMA
Parameter memory		Media: 3.5 inch FD (2HD, 2DD) Format: MS-DOS (Rev. 3.1)*2 Content: Pattern or other parameters
Operating temperature range		0˚ to +50˚C
Dimensions and mass		426 (W) x 221 (H) x 450 (D) mm, ≤33 kg
Power		≤400 VA
EMC		EN61326: 1997/A1: 1998 (Class A) EN61000-3-2: 1995/A2: 1998 (Class A) EN61326: 1997/A1: 1998 (Annex A)
LVD		EN61010-1: 1993/A2: 1995 (Installation Category Ⅱ, Pollution Degree 2)

*1: When the Option 03 (1/4 speed output) is added, the 1/8 speed output is not available.
*2: MS-DOS is a registered trademark of Microsoft Corporation.

MP1764C Error Detector

Operation frequency		0.05 to 12.5 GHz
Data input	Input waveform	NRZ
	Input amplitude	0.25 to 2.0 Vp-p
	Threshold voltage variable range	–3.000 to +1.875 Vp-p (1 mV steps)
	Phase margin	≥70 ps (typical value at 10 Gb/s, PRBS 2^{23} – 1, and an input amplitude of 1 Vp-p)
	Input sensitivity	50 mVp-p (typical value at 10 Gb/s and PRBS 2^{23} – 1
	Termination	Connected to GND or –2 V via a 50 Ω termination
	Connector	APC-3.5
Clock input	Input waveform	Rectangular wave (<0.5 GHz), rectangular or sine wave (≥0.5 GHz), duty factor: 50%
	Input voltage	0.25 to 2.0 Vp-p
	Input delay variable range	±500 ps (1 ps steps)
	Polarity inversion	CLOCK/$\overline{\text{CLOCK}}$ inversion possible
	Termination	Connected to GND or –2 V via a 50 Ω termination
	Connector	APC-3.5
Auto search function		Provided
Receive pattern	Pseudorandom binary sequence pattern (PRBS)	Pattern: 2^n – 1 (n: 7, 9, 11, 15, 20, 23, 31) Mark ratio: 1/2, 1/4, 1/8, 0/8 ($\overline{1/2}$, 3/4, 7/8, 8/8 are possible with logic inversion.) Number of AND bit shift at mark ratio setting: 1, 3 bits (selectable by using DIP switch on rear panel)
	Data pattern	Data length: 2 to 8388608 bits
	Alternate pattern	A/B pattern word length: 128 to 4194304 bits (128 bits steps), Number of loops: Controlled using external signal
	Zero substitution pattern	Zero bit length: 1 to (pattern length –1) bits, Pattern length: 2^n (n: 7, 9, 11, 15)
Synchronous mode		Normal, frame, quick
Synchronous threshold		Preset value or 10^{-n} (n: 2, 3, 4, 5, 6, 7, 8)
Error detection mode		Omission insertion, total (selectable with DIP switch on rear panel)
Measure-ment item	Error rate	0.0000 x 10^{-16} to 1.0000 x 10^{-0}
	Number of errors	0 to 9.9999 x 10^{16}
	Error interval (asynchronous)	0 to 9999999 (interval: 1 ms, 10 ms, 100 ms, 1 s)
	Error free interval (EFI)	0.0000% to 100.0000%
	Clock frequency	0.05 to 12.5 GHz, (resolution: 1 kHz, accuracy: 10 ppm ±1 kHz)
Eye margin measurement function		Provided
Error performance data calculation function		Provided
Measurement CH mask		1 to 32 ch (settable independently)
Block window		Error for any block of 32-bit segments can be measured.
Error analysis (option 01)		Pattern (256 bits in total) before and after bit in which error occurred is stored.
Auxiliary output	Error output (direct)	1/128 OR error, Output level: 0/–1 V, Connector: SMA
	Error output (stretched)	Pulse width: 350 ns (typical), Output level: TTL, Connector: BNC
	Alarm output (clock loss, sync. loss)	Output level: TTL Connector: BNC
	Sync. gain output	Output level: 0/–1 V; Connector: SMA
Auxiliary input	External mask input	Input level: 0/–1 V; Connector: SMA
	Resync. input	Input level: 0/–1 V; Connector: SMA
	Alternate A/B switching input	Input level: ECL; Connector: SMA
Sync. signal output	Number of outputs	1 (1/32 clock, fixed position pattern, or variable position pattern selectable)
	Output level	0/–1 V
	Connector	SMA
Parameter memory		Media: 3.5 inch FD (2HD, 2DD) Format: MS-DOS (Rev. 3.1)*1 Content: Pattern or other parameters
Operating temperature range		0˚ to +50˚C
Dimensions and mass		426 (W) x 221.5 (H) x 450 (D) mm, ≤30 kg
Power		≤300 VA
EMC		EN61326: 1997/A1: 1998 (Class A) EN61000-3-2: 1995/A2: 1998 (Class A) EN61326: 1997/A1: 1998 (Annex A)
LVD		EN61010-1: 1993/A2: 1995 (Installation Category Ⅱ, Pollution Degree 2)

*1: MS-DOS is a registered trade mark of Microsoft Corporation.

Ordering Information

Please specify model/order number, name and quantity when ordering.

Model/Order No.	Name	
	Main frame	
MP1763C	Pulse Pattern Generator (50 MHz to 12.5 GHz)	
	Standard accessories	
J0500A	Semi-rigid cable (SMA-P • SX-36 • SMA-P), 0.5 m:	2 pcs
J0672D	Semi-rigid cable, 7 cm:	1 pc
J0672F	Semi-rigid cable, 10 cm:	1 pc
J0693A	SMA cable (HRM202B-3D2W-HRM202B), 1 m:	1 pc
J0496	APC-3.5 J-J connector:	4 pcs
J0008	GPIB cable, 2 m:	1 pc
J0491	Power cord:	1 pc
Z0168	3.5-inch floppy disk (MF2HD-3.5MF):	2 pcs
Z0481	12.5G/3.2G BERTS application software demo:	1 pc
Z0306A	Wrist strap:	1 pc
F0014	Fuse, 6.3 A (T6.3A250V):	1 pc
B0021	Protective cover (for 1MW • 5U):	1 pc
W1848AE	MP1763C operation manual:	1 copy
W1849AE	MP1763C GPIB operation manual:	1 copy
	Option	
MP1763C-01	12.5 GHz Synthesizer (50 MHz to 12.5 GHz)	
MP1763C-03	1/4 speed output	
	Main frame	
MP1764C	Error Detector (50 MHz to 12.5 GHz)	
	Standard accessories	
J0500A	Semi-rigid cable (SMA-P • SX-36 • SMA-P), 0.5 m:	2 pcs
J0693A	SMA cable (HRM202B-3D2W-HRM202B), 1 m:	3 pcs
J0496	APC-3.5 J-J connector:	2 pcs
J0008	GPIB cable, 2 m:	2 pcs
J0491	Power cord:	1 pc
Z0168	3.5-inch floppy disk (MF2HD-3.5MF):	2 pcs
Z0481	12.5G/3.2G BERTS application software demo:	1 pc
F0014	Fuse, 6.3 A (T6.3A250V):	1 pc
Z0306A	Wrist strap:	1 pc
B0021	Protective cover (for 1MW • 5U):	1 pc
W1850AE	MP1764C operation manual:	1 copy
W1851AE	MP1764C GPIB operation manual:	1 copy
	Option	
MP1764C-01	Error analysis	
	Optional accessories	
MX176400A	Q/Eye Analysis Software	
MX176401A	SDH/SONET Pattern Editor	
J0500B	Semi-rigid cable (SMA-P • SX-36 • SMA-P), 1 m	
J0322A	Coaxial cable (11SMA • SUCOFLEX104 • 11SMA), 0.5 m	
J0322B	Coaxial cable (11SMA • SUCOFLEX104 • 11SMA), 1 m	
J0007	GPIB cable, 1 m	
Z0054	3.5-inch floppy disk (MF2DD-3.5MF)	
MB24B	Portable Test Rack (rating current of power cord and plug: 20 A)	
B0413A	Carrying case	
B0163	Soft carrying case	
B0044	Rack mount kit (for 1MW • 5U panel)	
Z0416	3.5 inch head cleaning disk	

Anritsu

Specifications are subject to change without notice.

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