

**PULSE PATTERN GENERATOR**  
**MP1763B**  
 12.5 GHz



The MP1763B is used in combination with the MP1764A Error Detector. The amplitude of the clock and data signals can be varied from 0.25 to 2 Vp-p while the offset can be adjusted to within  $\pm 2$  V so that the amplitude and the offset margin can be measured. The clock has a variable delay function so that time-dependent characteristics or phase margins of the input clock and data can be measured. An M series pseudorandom pattern representative of actual conditions or a programmable pattern can be selected as cell data.

In addition, a 3.5 inch floppy disk drive is built in for storing preset data, enabling rapid measurements to be performed by simply pressing a key. A GPIB function is provided, enabling automatic or remote measurement via an external controller.

The MP1763B is a pulse pattern generator ideal for research and development of high-speed logic, ICs, and digital systems.

**Features**

- High quality waveform
- Low FM/PM-noise clock generator
- 8 Mbit programmable pattern corresponding to six frames of STM-64/STS-192
- Generates PRBS patterns with bit length from  $2^7-1$  to  $2^{31}-1$  bits
- Complementary outputs of both data and clock
- The amplitudes and offsets of all 8 data outputs that have 1/8 speed of fundamental clock signal can be set

**Specifications**

Operation frequency	Internal clock	0.05 to 12.5 GHz (option)
	External clock	0.05 to 12.5 GHz
External clock	Input level	0.4 to 2.5 Vp-p
	Input waveform	Square wave with rise/fall time of less than 1 ns, duty factor 50% (0.05 to 0.5 GHz); Sinusoidal wave or square wave with rise/fall time of less than 1 ns, duty factor 50% (>0.5 GHz)
	Input connector	APC-3.5
Internal clock	Frequency range	0.05 to 12.5 GHz (option)
	Frequency setting resolution	1 kHz, 1 MHz
	Stability	$\pm 1$ ppm
	SSB phase noise (at 10 kHz offset, 1 Hz bandwidth)	-85 dBc/Hz (0.05 to 4 GHz), -80 dBc/Hz (4 to 8 GHz), -75 dBc/Hz (8 to 10 GHz), -70 dBc/Hz (10 to 12.5 GHz)
	Reference signal	10 MHz (internal/external, selectable)
Pattern	Pseudorandom binary sequence pattern (PRBS)	Pattern: $2^n - 1$ (n: 7, 9, 11, 15, 20, 23, 31) Mark ratio: 1/2, 1/4, 1/8, 0/8 ( $\sqrt{2}$ , 3/4, 7/8, 8/8 are possible with logic inversion) Number of AND bit shifts when setting mark ratio: 1, 3 bit (selectable by using DIP switch on rear panel)
	Data pattern*1	Data length: 2 to 8388608 bits; Pattern reset/preset: ALL/PAGE selectable
	Logic inversion	Provided
	Alternate pattern	A/B pattern data length: 128 to 4194304 (128 bit steps); Loop time: A, B pattern (1 to 127, 1 steps)
	Zero substitution pattern	Zero bit length: 1 to (pattern length - 1) bits; Pattern: $2^n$ (n: 7, 9, 11, 15)
	Error addition	Error rate: $10^{-n}$ (n: 4, 5, 6, 7, 8, 9), and single error Addition position (selectable with rear panel DIP switch): Possible to insert into any 1 CH of 32 CH

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Data output	Output waveform	NRZ
	Number of outputs	2 (DATA/DATA)
	DATA/DATA tracking mode	ON/OFF selectable
	Amplitude	0.25 to 2 Vp-p, 2 mV steps (setting error: $\pm 15\%$ or $\pm 100$ mV, whichever is greater)
	Offset voltage	Voltage: $-2$ to $\pm 2$ V ( $V_{OH}$ ), 1 mV steps (setting error: $\pm 15\%$ of offset voltage, $\pm 100$ mV or $\pm 15\%$ of amplitude whichever is the greatest) Display: $V_{OH}$ , $V_{TH}$ or $V_{OL}$ selectable
	Rise/fall time	Typical 30 ps (10% to 90% of amplitude)
	Pattern jitter	$\leq 20$ psp-p (typical 10 psp-p)
	Waveform distortion	$\leq 15\%$ or $\leq 150$ mV whichever is greater
	Load impedance	50 $\Omega$ (with back termination)
Connector	APC-3.5	
Clock output	Number of outputs	3 (CLOCK 1, $\overline{\text{CLOCK 1}}$ , CLOCK 2)
	CLOCK delay	$\pm 500$ ps (1 ps steps)
	Amplitude (CLOCK 1, $\overline{\text{CLOCK 1}}$ )	0.25 to 2 Vp-p (2 mV steps) Setting error: $\pm 15\%$ (1.5 to 2 Vp-p), $\pm 25\%$ (0.5 to 1.5 Vp-p), $\pm 100$ mV (0.25 to 0.5 Vp-p)
	Amplitude (CLOCK 2)	1 Vp-p $\pm 35\%$
	Offset voltage (CLOCK 1, $\overline{\text{CLOCK 1}}$ )	Voltage: $-2$ to $\pm 2$ V ( $V_{OH}$ ), 1 mV steps (setting error: $\pm 15\%$ of offset voltage, $\pm 100$ mV or $\pm 15\%$ of amplitude whichever is the greatest) Display: $V_{OH}$ , $V_{TH}$ or $V_{OL}$ selectable
	Offset voltage (CLOCK 2)	0 V $\pm 200$ mV ( $V_{OH}$ )
	Rise/fall time	Typical 30 ps (10% to 90% of amplitude)
	Waveform distortion	$\leq 15\%$ or $\leq 150$ mV whichever is greater
Duty factor adjust function	CLOCK 1, $\overline{\text{CLOCK 1}}$ adjustable	
Clock output	Load impedance	50 $\Omega$ (CLOCK 1, $\overline{\text{CLOCK 1}}$ : with back termination)
	Connector	APC-3.5 (CLOCK 1, $\overline{\text{CLOCK 1}}$ ), SMA (CLOCK 2)
1/4 data and clock output*2	Number of outputs	DATA: 4, CLOCK: 1
	Output level	0.5 to 2 Vp-p, 2 mV steps (setting error: $\pm 15\%$ or $\pm 100$ mV, whichever is greater)
	Offset voltage	Voltage: $-1.5$ to $+1.5$ V ( $V_{OH}$ ), 1 mV steps (setting error: $\pm 15\%$ of offset voltage or $\pm 15\%$ of amplitude or $\pm 100$ mV whichever is the greatest) Display: $V_{OH}$ , $V_{TH}$ or $V_{OL}$ selectable
	Rise/fall time	$\leq 150$ ps (20% to 80% of amplitude)
	Data output jitter	$\leq 100$ psp-p
	Waveform distortion	$\leq 15\%$
	Skew (DATA/DATA, DATA/CLOCK)	$\leq 100$ ps
	Connector	SMA
1/8 data, clock output*3		Number of outputs: DATA 8, CLOCK 1 Output level: ECL Connector: SMA
Sync. signal output	Number of outputs	1 (1/32 clock, fixed position pattern, or variable position pattern selectable)
	Output level	Amplitude: 1 Vp-p $\pm 20\%$ , offset voltage: 0 V $\pm 200$ mV ( $V_{OH}$ )
External control		GPIB, IEEE 488.2
Operating temperature range		0° to +50°C
Parameter memory		Media: 3.5 inch FD (2HD, 2DD) Format: MS-DOS (Rev. 3.1)**4 Content: Programmable pattern and other parameters
Power		*5Vac $\pm 10\%$ , 50/60 Hz, $\leq 700$ VA
Dimensions and mass		426 (W) x 221 (H) x 451 (D) mm, $\leq 33$ kg
EMC		EN55011: 1991, Group 1, Class A EN50082-1: 1992 Harmonic current emissions: EN61000-3-2 (1995)
Safety		EN61010-1: 1993 (Installation Category II, Pollution Degree II)

\*1: Relationship between number of pages and items of word length, number of words, and data length

### • Numerical relation between data length and step width

Data length	Step width
2 to 65536	1 step
65536 to 131072	2 step
131072 to 262144	4 step
262144 to 524288	8 step
524288 to 1048576	16 step
1048576 to 2097152	32 step
2097152 to 4194304	64 step
4194304 to 8388608	128 step

### • Relationship between pages of WORD mode and DATA mode

Output pattern/mode	Variable page range
WORD	1 word to the number of words that have been set, 1 step width
DATA	1 to $< \text{data length}/16$ , 1 step width (up to quotient value when the remainder is 0, up to quotient value +1, 1 step width)
	Data length    Number of pages
	2 to 16                    1
	17 to 32                2
33 to 48                3	
$\geq 49$ $\geq 4$	

- \*2: Option 03
- \*3: When the Option 03 (1/4 speed output) is added, the 1/8 speed output is not available.
- \*4: MS-DOS is a registered trademark of Microsoft Corporation.

• **Floppy disk format**

Media type	Memory capacity	Sector length	Sector number	Track number	Recording surface
2HD	1440 KB	512 bytes	18	80	Double-sided
2DD	720 KB	512 bytes	9	80	Double-sided
2HD	1232 KB	1024 bytes	8	77	Double-sided
2DD	640 KB	512 bytes	8	80	Double-sided

- \*5: Specify one nominal line voltage between 100 and 240 V when ordering. Maximum operating voltage is 250 V.

## Ordering information

Please specify model/order number, name, and quantity when ordering.

Model/Order No.	Name
MP1763B	<p><b>Main frame</b> Pulse Pattern Generator</p> <p><b>Standard accessories</b> Semi-rigid cable (SMA-P • SX-36 • SMA-P), 0.5 m: 2 pcs Semi-rigid cable, 7 cm: 1 pc Semi-rigid cable, 10 cm: 1 pc Coaxial cable (SMA-P • RG58A/U • SMA-P), 1 m: 1 pc APC-3.5 J-J connector: 4 pcs GPIB cable, 2 m: 1 pc Power cord: 1 pc 3.5 inch floppy disk (MF2HD-3.5MF): 2 pcs Wrist strap: 1 pc Fuse, 8 A (for 100 V mains): 2 pcs Fuse, 6.3 A (for 200 V mains): 2 pcs MP1763B operation manual: 1 copy MP1763B GPIB operation manual: 1 copy</p> <p><b>Options</b> 12.5 GHz synthesizer (50 MHz to 12.5 GHz) 1/4 speed output</p> <p><b>Application equipment</b> Synthesized Sweep Generator (10 MHz to 20 GHz)</p> <p><b>Optional accessories</b> Semi-rigid cable (SMA-P • SX-36 • SMA-P), 1 m Coaxial cable (11SMA • SUCOFLEX104 • 11SMA), 0.5 m Coaxial cable (11SMA • SUCOFLEX104 • 11SMA), 1 m Coaxial cable (APC3.5 • – • APC3.5), 0.5 m (double shielded) Coaxial cable (APC3.5 • – • APC3.5), 1 m (double shielded) GPIB cable, 1 m 3.5 inch floppy disk (MF2DD-3.5MF) Portable Test Rack (rating current of power cord and plug: 20 A) Carrying case Soft carrying case Rack mount (for 1MW • 5U panel) Stacking rack (for sweep synthesizer) MP1763B service manual</p>
MP1763B-01 MP1763B-03	
68347B	
J0500B J0322A J0322B J0498	
J0499	
J0007 Z0054 MB24B	
B0413A B0163 B0044 Z0292A W1040BE	