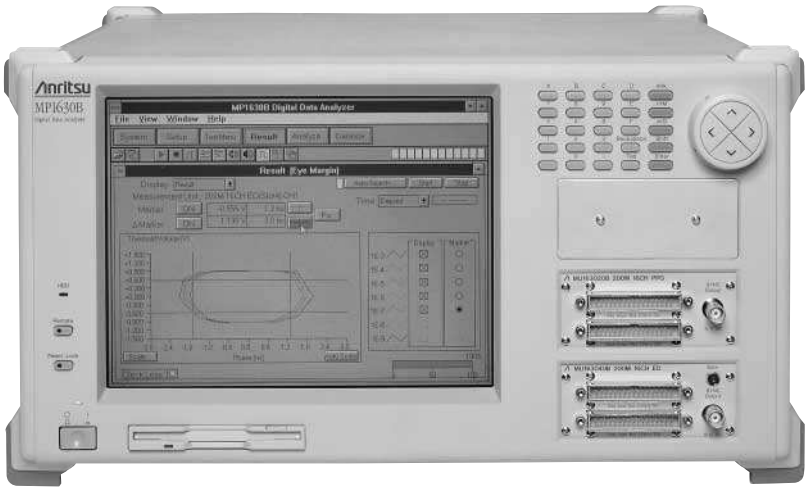
DIGITAL DATA ANALYZER
MP1630B
10 kHz to 200 MHz

GPIB OPTION

For R&D and Manufacturing of Digital Devices and Equipment



Custom-made product

The MP1630B is a general-purpose bit error measuring instrument that can provide simultaneous measurements of multi-channel signals and burst signal measurements up to 200 MHz.
The MP1630B is not only for continuous signals – it can measure burst-signal bit error rates as well. Consequently, it is easily able to handle burst signals used by TDMA (Time Domain Multiplex Access) methods and packet/cell transmissions, etc. Both a pulse pattern generator unit and an error detector unit can be installed in the MP1630B to measure simultaneously parallel data for 16 channels using just one unit.

Features
- 16 channel PPG and ED in one cabinet
- Eye diagram measurement based on BER

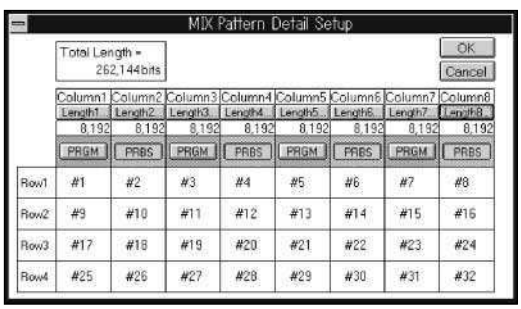
Applications
- Testing multi-channel modules for optical interconnection
- E/O, O/E evaluation for optical networks (PON/PDS)
- Testing SDH/ATM equipment and modules
- Testing cable modems for digital CATV
- R&D on TDMA
- R&D on wireless LAN peripherals
- Evaluating next-generation PC interfaces (fiber channel, IEEE 1394, SSA, ATM-25)
- Evaluating digital demodulators including QPSK/QAM, etc.
- Evaluating IrDA communications equipment
- Evaluating communications LSIs, ASICs/FPGAs, and CCDs, etc.

Performance and functions

• Simultaneous bit error measurement of 16 channels
The MP1630B has 16-channel Pulse Pattern Generator and Error Detector units and can measure bit errors in parallel and simultaneously. Using the MP1630B shortens the time required to measure each device to 1/N, thereby greatly improving production efficiency.

• For both continuous and burst data
Continuous data is used in the PDH/SDH transmission system; burst data is used in the PON (Passive Optical Network) subscriber TDMA transmission system, as well as in the burst cell unit ATM-PON transmission system. The MP1630B can handle bit error measurement of both continuous and burst data. It can output burst data for up to 16 channels, and the burst cycle, guard time, preamble length, and data length can all be varied.

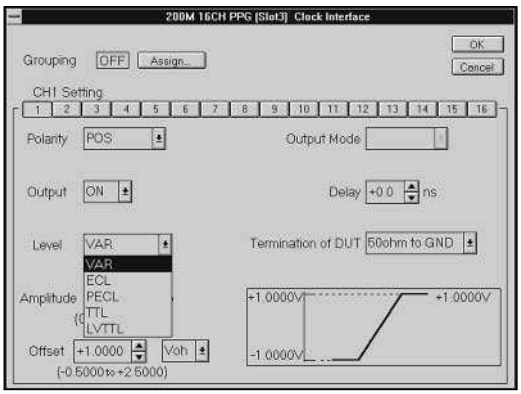
• Mixed pattern generation, selective BER measurement
With the MP1630B, a test pattern can be selected and set for each channel. Not only can both PRGM and PRBS patterns be used, but a mixed pattern composed of both PRGM and PRBS patterns can be generated, too. The packet type and cell type data can be configured smoothly from the overhead and payload parts. Moreover, the pattern field can split in two to 32 blocks, and a PRGM or PRBS pattern can be allocated to each column individually. As a result, it is possible to create pseudo-test signals for SDH/ATM, etc., as well as signals for evaluating complex communication protocols.



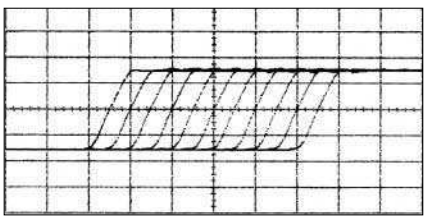
32 block mixed pattern setting screen

• Superior basic functions
A high-performance frequency synthesizer is built into the MP1630B. It generates stable, accurate signals with high resolution in the 10 kHz to 200 MHz band. In addition, when the optional digital modulator function is used, the jitter tolerance of communications equipment and devices can also be measured.
In addition to TTL, LVTTL, ECL, and PECL, the pulse pattern generator clock and data output levels can be set to any output (0.25 to 2.5 V at 50 Ω termination; 0.5 to 5.0 V at high) for a variety of interfaces. The data and clock output delay can be varied at high resolution for each channel, and there is no need to adjust the cable length for each signal.

For product ordering information, see pages 5 – 12



Pulse pattern generator clock interface screen

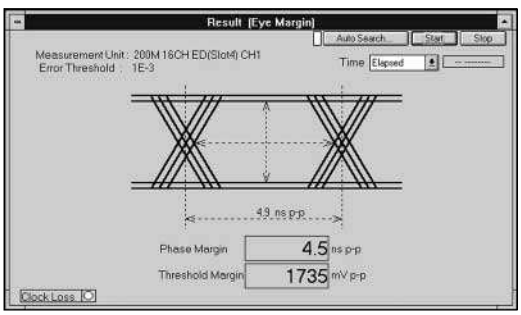


10 MHz (V: 800 mV/div, H: 2 ns/div)
Clock delay: –5 to +5 ns/1 ns steps (averaged waveform)

Variable delay characteristics

• Evaluating error correction function using burst error insertion
In addition to having the earlier cyclic and single error-mode insertion functions, the MP1630B has burst-mode insertion functions, making it ideal for evaluating the efficiency of error-correction codes used by each type of communication protocol. In particular, it is especially effective for testing digital transmission methods used by broadcast satellites and mobile phones, etc.

• Evaluating data waveform quality using eye margin measurement
The MP1630B eye margin measurement function can automatically measure the threshold voltage and phase range below the specified error rate. It has two measurement modes: the Margin mode and the Diagram mode. These modes can be selected according to the application.



Margin mode

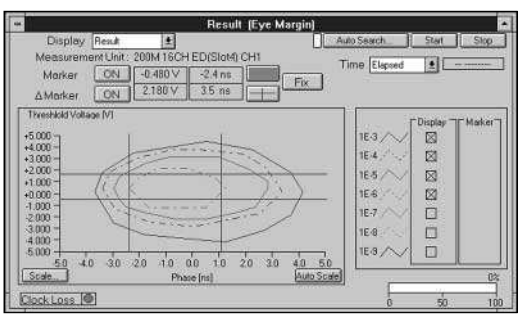
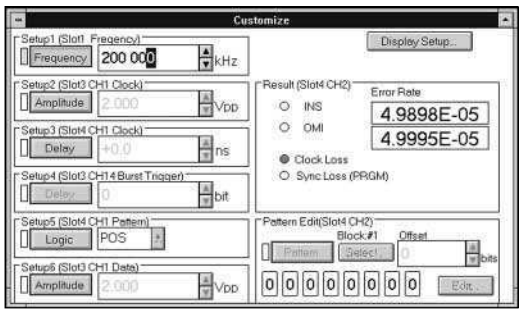


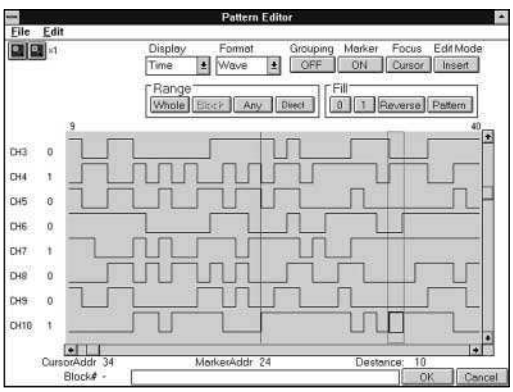
Diagram mode

• One-key/one-parameter operation using customized screens
Measurement of general multi-channel data requires complex operations to manage the large number of measurement parameters. To make measurement settings simpler, the MP1630B has convenient customized screens based on the one-key/one parameter operation used previously in the Anritsu BERTS. It also has a Grouping function which groups together the same measurement items used for each channel. Common settings (all or pattern-only) are saved as files on the large internal hard disk.



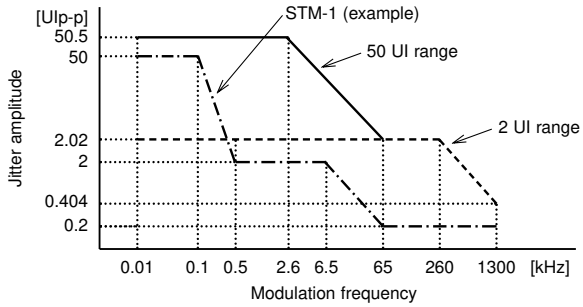
Customized screen

• Powerful pattern editor function
The MP1630B pulse pattern generator and error detector PRGM patterns can be edited easily using the keyboard, mouse, or cursor keys. There are three editing modes matching the various applications: Time, State, and Dump. The Time mode puts time on the horizontal axis and displays the pattern for each channel as a horizontal line. The State mode displays the data of channel 1 as the MSB and parallel 16 bits (corrected 1 bit from each channel at a time) as one data item. The Dump mode displays the pattern for the specified channel as a memory dump image using either binary or hexadecimal code.



Pattern editor (time mode, input waveform)

Specifications

Clock	Internal Operating frequency: 10 kHz to 200 MHz (accuracy: ±2 ppm) Resolution: 1 kHz steps (>1 to 200 MHz), 100 Hz steps (10 kHz to 1 MHz) External Input frequency range: 10 kHz to 200 MHz Input level: AC, 0.5 to 2.0 Vp-p (50 Ω), BNC connector External (at locked) Input frequency range: 10 MHz ±100 ppm, 64 kHz ±100 ppm Input level: AC, 0.5 to 2.0 Vp-p (50 Ω), BNC connector
Jitter modulation function (option)	External modulation input Modulation frequency range: 10 Hz to 1.3 MHz Input level range (sine wave): –1 to +1 V (75 Ω), BNC connector Reference output (jitter-free output): AC, 1 Vp-p (50 Ω), SMA Jitter: 0 to 50.5 UIp-p (clock frequency: >100 to 200 MHz) ∗Switchable to 50 UI/2 UI range 
Test pattern (pulse pattern generator, error detector)	PRBS Pattern: $2^n - 1$ (n: 7, 9, 11, 15, 20, 23, 31), variable mark ratio, logic selectable Zero substitution pattern: 2^n (n: 7, 9, 11, 15); pattern length: n to $2^n - 1$, logic selectable PRGM pattern: 2 to 65,536 bits/channel bit length, logic selectable Mixed pattern: Mixed PRGM and PRBS pattern, logic selectable ∗Block numbers: 2 to 32 [PRGM bit length/block: 8 to 8,912 bits; PRBS bit length/block: 8 to 131,072 bits (depend on block numbers)] PON pattern [TDMA test patterns with preamble inserted in ahead of Mixed patterns (PRGM and PRBS)] Preamble (1010...): 0 to 64 bits; guard time: –2,097,083 to 2,097,067 bits (1 bit resolution) Burst mode: Internal (burst cycle: 0.1 to 10 ms), external (enable length: 8 to 2,097,144 bits) Pattern edit function Edit mode: Dump, timing diagram, state table Edit results storage: Internal HDD or FDD
Error insertion	Each channel, simultaneous or independently Error type: Normal, burst Normal mode (internal: cyclic or single, external) Error rate: 10^{-n} (n: 3 to 9) Insert area: Entire area, selected blocks (in Mixed pattern or PON pattern) Burst mode (internal/external) Error rate: 10^{-n} (n: 2 to 9) Internal enable length: 20 to 140 ms (resolution: 20 ms) Internal cycle: 1 to 10 s (resolution: 1 s) External mode: Error of specified rate inserted in external signal enable period
Data/clock output	Output No.: 16 (multipin connector), output on/off and logic selectable Output waveform: NRZ (data), RZ (clock) Output level: ECL, PECL, TTL, LVTTL, VAR VAR range Amplitude: 0.5 to 5 V (10 mV steps, high impedance), 0.25 to 2.5 V (5 mV steps, 50 Ω) Offset: –4.5 to + 5 V (5 mV steps, high impedance), –2.25 to + 2.5 V (2.5 mV steps, 50 Ω) Rise/fall times (typ.): 1.3 ns (1 Vp-p, 50 Ω termination) Clock delay: –5 to +5 ns (100 ps steps) Data skew: –5 to +5 ns (100 ps steps)
Data/clock input	Input No.: 16, logic selectable, multipin connector Input waveform: NRZ (data), RZ (clock) Input level: ECL, PECL, TTL, LVTTL, VAR VAR input range Amplitude: 0.5 to 5 V (50 Ω) Threshold level: –5 to + 5 V (5 mV steps, in 50 Ω to GND termination) Clock delay: –5 to +5 ns (100 ps steps)
Measurement data	Channel No.: 16 channels simultaneous measurement (selectable measurement channels) Signal format: Continuous or burst (internal/external)
Bit error measurement	Error detection: All, insertion, omission Measurement region: All, PRGM, PRBS selectable, and each block selectable with block configuration Display Error rate: 0×10^{-16} to 1.0000×10^{0} Error count: 0 to 9999999, 1.0000×10^{7} to 9.9999×10^{16} Error interval: 0 to 9999999, 1.0000×10^{7} to 9.9999×10^{16} Error free interval: 0.0000 to 100.0000% Error performance: ITU-T Rec. G.821 Measurement mode: Single, repeat, untimed (1 second to 99 days 23 hours 59 minutes 59 seconds) Auto sync: ON/OFF switchable [threshold value: 1×10^{-n} (n: 2 to 8)], with autosearch function
Alarm measurement	Detected items: Power loss, clock loss, pattern sync loss (PRGM, PRBS)

Continued on next page

For product ordering information, see pages 5 – 12

Frequency measurement		Measurement range: 10 kHz to 200 MHz Effective digits: 6 digits Resolution: 100 Hz Accuracy: ± (1 count ±10 ppm)
Eye margin measurement (based on BER)		Measures eye margin or eye diagram of specified data (1 channel) Eye margin: Displays threshold margin and phase margin as numeric values Eye diagram: Displays width of eye aperture as two-dimensional graph using bit-error measurement
Delay measurement		Mode: Single/repeat Unit: Time/bit numbers Range Time: 0 to 999 µs (1 µs steps), 1 to 999 ms (1 ms steps), 1 to 10 s (1 s steps) Bits: 2^{31} bits (max.) Time out: 0.5, 1, 2, 5, 10 s
I/O signal for burst BER measurement	Pulse pattern generator	External burst input Level: TTL (H: Enable, L: Disable), BNC connector Burst trigger output (index signal for each burst data) Output No.: 16 (for each data output), bit delay function Level: ECL, –2 V (50 Ω), multipin connector Auxiliary output (PON system envelope, or AGC reset signal; usable as normal control signal) Output No.: 8 (selectable channel), 1 (OR output for each channel), bit delay function, logic selectable Level: ECL or TTL (≤100 Mb/s), multipin connector
	Error detector	Burst trigger input Input No.: 16 (for each data input) Level: ECL, –2 V (50 Ω), multipin connector
Other I/O signals		Sync signal output (pulse pattern generator, error detector) Sync source: 1/1 clock, 1/8 clock, PRGM pattern, PRBS pattern Level: 0/–1 V (50 Ω), BNC connector External error input (pulse pattern generator) Error mode: Normal, burst Level: TTL, BNC connector Trigger output (pulse pattern generator) Trigger source: Unique pattern index for delay measurement or pattern block index in MIX/PON pattern Level: 0/–1 V (50 Ω), multipin connector Trigger input (error detector) Trigger source: For delay measurement Level: 0/–1 V (50 Ω), multipin connector
System environment		Platform: Microsoft Windows operating system version 3.1 Display: Color LCD, touch screen, 640 x 480 dots, 256 colors Printer: Parallel port for printer, D-sub 25-pin connector Keyboard: 101 keys (English), PS2 mini-DIN 6-pin connector Mouse: Serial, PS2 mini-DIN 6-pin connector FDD: 2 mode (1.44 MB, 740 KB) HDD C drive: ≥1,380 MB (for measurement data, patterns) D drive: 30 MB (not released to user, interface: IDE)
Remote control		RS-232C (standard), GPIB (option): IEEE488.2, Ethernet (option): 10 Base-T
Other functions		Sound: When error or alarm detected, panel lock function, self check function
Power		100 to 120/200 to 240 Vac, 47.5 to 63 Hz, ≤1,000 VA
Dimensions and mass		426 (W) x 221.5 (H) x 451 (D) mm, ≤29 kg
Operating temperature		+5˚ to +40˚C

The specifications are with the MU163000A (200M Clock Generator Unit), MU163020B (200M 16CH Pulse Pattern Generator Unit), and MU163040B (200M 16CH Error Detector Unit) installed in the MP1630B main frame.

Ordering information

Please specify model/order number, name, and quantity when ordering.

Model/Order No.	Name	
	Main frame	
MP1630B	Digital Data Analyzer	
	Standard accessories	
J0491	Power cord (shielded):	1 pc
F0087	Fuse, 10 A:	2 pcs
Z0319A	PS/2 mouse:	1 pc
Z0320	Input pen:	1 pc
Z0388	MP1630B recovery disk (only for MP1630B customer):	11 pc
Z0389	MP1630B application disk (only for MP1630B customer):	7 pc
Z0390	MP1630B remote sample disk (only for MP1630B customer):	1 pc
Z0396A	Pen holder:	1 pc
W1442AE	MP1630B operation manual:	1 copy
W1443AE	MP1630B remote control operation manual:	1 copy
W1450AE	MP1630B auto adjust operation manual:	1 copy
	Options	
MP1630B-01*1	GPIB (GPIB interface board)	
MP1630B-02*1	Ethernet (Ethernet interface board)	
	Peripherals	
Z0321A	Keyboard (PS/2)	
J0008	GPIB cable	
MB24B	Portable Test Rack (specified current: 10 A)	
B0348	Soft case	
B0329D	Front cover	
B0333D	Rack mount kit	
	Plug-in unit	
MU163000A*1	200M Clock Generator Unit	
	Standard accessories	
W1187AE	MU163000A operation manual:	1 copy
	Option	
MU163000A-01*1	Jitter addition	
	Peripherals	
J0776D	Coaxial cord (BNC-P-3W · 3D-2W · BNC-P-3W), 2 m (double shield)	
	Plug-in unit	
MU163020B*1, *2	200M 16CH Pulse Pattern Generator Unit	
	Standard accessories	
J0693B	SMA cable, 0.27 m:	2 pcs
W1444AE	MU163020B/163040B operation manual:	1 copy
	Peripherals	
J0776D	Coaxial cord (BNC-P-3W · 3D-2W · BNC-P-3W), 2 m (double shield)	
J0824	BNC multi-core cable, (16 pins), 1 m	
J0825	BNC multi-core cable, (9 pins), 1 m	
J0826	SMA multi-core cable, (16 pins), 1 m	
J0827	SMA multi-core cable, (9 pins), 1 m	
J0858	SMA multi-core cable, (16 pins), 2 m	
J0859	SMA multi-core cable, (9 pins), 2 m	
J0860	BNC multi-core cable, (16 pins), 2 m	
J0861	BNC multi-core cable, (9 pins), 2 m	

Model/Order No.	Name	
	Plug-in unit	
MU163040B*1, *2	200M 16CH Error Detector Unit	
	Standard accessories	
J0828	Multi-core cable, (16 pins), 0.5 m:	2 pcs
J0829	Multi-core cable, (17 pins), 0.5 m:	1 pc
J0693D	SMA cable, 0.27 m:	1 pc
W1444AE	MU163020B/163040B operation manual (not supplied when Pulse Pattern Generator Unit purchased at same time):	1 copy
	Peripherals	
J0776D	Coaxial cord (BNC-P-3W · 3D-2W · BNC-P-3W), 2 m (double shield)	
J0824	BNC multi-core cable (16 pins), 1 m	
J0825	BNC multi-core cable (9 pins), 1 m	
J0826	SMA multi-core cable (16 pins), 1 m	
J0827	SMA multi-core cable (9 pins), 1 m	
J0858	SMA multi-core cable (16 pins), 2 m	
J0859	SMA multi-core cable (9 pins), 2 m	
J0860	BNC multi-core cable (16 pins), 2 m	
J0861	BNC multi-core cable (9 pins), 2 m	

∗1: Factory option
∗2: Requires multi-core cable shown in peripherals (sold separately) for measurements

For product ordering information, see pages 5 – 12