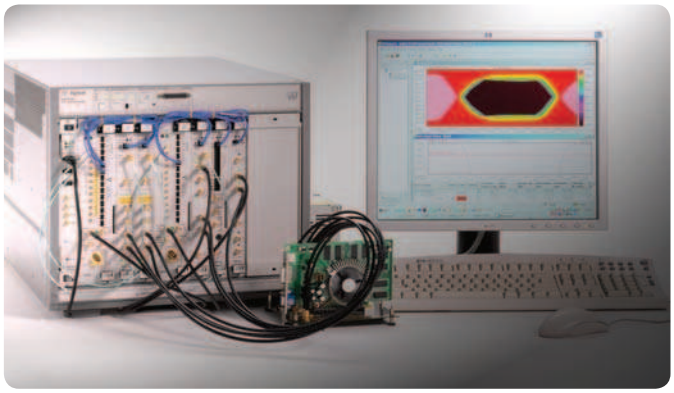
Agilent ParBERT 81250
Parallel Bit Error Ratio Tester

Product Overview
Version 6.0



The only modular parallel bit error ratio test solution with

- different modules covering a range of data rates from 333 kHz to 13.5 GHz
- up to 66 synchronous input and output channels
- powerful pattern sequencer providing looping and branching on events enabling control of complex tests and devices
- PRBS/PRWS and memory based patterns up to 64Mb
- delay control input for jitter generation
- error detector modules featuring individual CDR
- measurement suite

Agilent Technologies

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The ParBERT 81250 is the flexible and scalable physical layer test solution that, based on its modular BERT engine, enables characterization of high-speed multi-port devices in the computer, communications and feeding semiconductor industry.

The **modular** ParBERT 81250 can be tailored to individual test needs with **up to 132**[1] **synchronous channels**. Different modules are available for the ParBERT 81250 System that cover data generation and analysis **from 333 kb/s up to 13.5 Gb/s**. Once purchased in a certain configuration ParBERT 81250 **can easily be extended** to fit future needs protecting your investment.

Broad spectrum of applications

Originally designed to test and characterize synchronous devices such as a **Mux/Demux** typical for the communications industry ParBERT 81250 is equally suited for **clock synchronous multi-port** and **multiple serial** applications such as can be found in the computer industry**.**

Powerful Pattern sequencer for uninterrupted testing

Running complex tests with a variety of test patterns in one shot without stopping the instrument for pattern download is enabled through the powerful ParBERT 81250 pattern sequencer with its up to five nested loop levels and branching on external and internal events or upon SW command.

In-depth insight into designs and devices

The **measurement suite** automates the parameter variation of ParBERT's BER-measurements to achieve and visualize insight into the DUT's parametric performance, e.g. producing eye diagrams, or doing timing margin analysis with BER-scan bathtub-plots with RJ-DJ jitter decomposition. **Jitter injection** via the delay control input of the 13.5 / 7 / 3.35 Gb/s Data Generator Modules allows in depth receiver margining including jitter tolerance tests.

Application support

ParBERT's software package contains setup and processing tools for 10GbE and SONET/SDH. The **N5990A Test Automation Platform** enables simple compliance test with ParBERT for different standards such as **PCI Express®, MIPI™, display port (DP) and HDMI**.

Application and product notes describing a variety of test applications with ParBERT are available for download from **www.agilent.com/find/ParBERT**.

ParBERT 81250 key characteristics:

- Modular BERT platform for physical layer test and characterization
- Modules of various speed classes up to 13.5 Gb/s
- Up to 66 synchronous generator and analyzer channels
- Powerful pattern sequencer to control complex devices PRBS/PRWS[2] and memory based patterns
- Delay control input to apply external jitter sources[3]
- Integrated clock data recovery to test clock-less interfaces[4]
- Comprehensive measurement suite

Note:

1) 66 or 30 channels max with 3.35Gb/s or 13.5Gb/s modules

2) PRWS, Pseudo Random Word Sequence, is a special hardware generated pattern, based on PRBS, to test Mux/DeMux

3) 3.35 Gb/s, 7Gb/s and 13.5 Gb/s generator modules only

4) 7 Gb/s and 13.5 Gb/s analyzer modules only

ParBERT 81250 is designed as a flexible data generator/ analyzer platform for physical layer test and characterization. It can be used for a large variety of applications and by this meets your individual needs.

A module based system

The ParBERT 81250 consists of the user SW and the ParBERT modules. These can be categorized by their maximum data rate (675Mb/s, 3.35Gb/s and 7/13.5Gb/s) and their functionality (clock or data). A minimum system consists of one clock module and one data module forming a so-called clock group which is installed in the ParBERT VXI-mainframe. The mainframe can hold multiple clock groups; each is operated through its own graphical user interface (GUI).

Three main speed classes

The high-speed modules for 13.5 Gb/s and 7 Gb/s are dedicated generator or analyzer modules with one data channel each. The generators provide differential data and full rate clock output. They are equipped with an externally voltage controllable delay line to generate data streams with up to 200ps of peak-to-peak jitter. The analyzer modules feature an integrated clock data recovery CDR.

The 3.35 Gb/s data modules can carry up to two generator or analyzer front-ends of any combination. Equivalent to the high speed modules the generator front-ends feature a voltage controlled delay for jitter generation but, according to the lower data rate, with a wider range of 500ps.

The 675 Mb/s data module back-ends can hold up to four generator or analyzer front ends and combinations thereof. A special capability of these back-end modules is the internal digital and analog channel-add function which e.g. allows generation of multi-level signals.

Up to 132 channels

ParBERT 81250 uses the standard VXI mainframe with its 13 slots, where the leftmost slot is always reserved for the so-called slot-0 controller so that 12 slots are available for ParBERT-modules, i.e. clock and data. A maximum of three mainframes can be combined to form a clock synchronous system, which for the 675Mb/s speed class and its 1-slot-wide clock module per frame yields up to 132 data channels (3 x 11 x 4).

Table 1, a selection guide, lists the maximum number of channels per speed class together with some features or key specifications such as user memory depth or input / output voltage level ranges.

Multiple users at the same time

The ParBERT 81250 Hardware is controlled by the ParBERT user SW via an IEEE 1394 firewire link. The SW is running on an external PC. It consists of three parts:
A firmware server and two clients, the graphical user interface (GUI) which allows instrument setup and basic (BER-) measurements and the measurement user interface (MUI) which provides a variety of parametric physical layer measurements based on BER-measurements. GUI and MUI can either run on the PC which hosts the firmware server and controls the HW or on any other PC which is connected (e.g. via LAN) to that PC mentioned above. They control measurements on any of the installed clock groups. Each clock group can be controlled by a different user. Plug&Play drivers simplify controlling ParBERT 81250 through Agilent VEE, C/C++ or Visual Basic programs or by SCPI based language via GPIB.

Table 1. Brief selection guide for ParBERT 81250

Selection Guide for ParBERT 81250				
target Data rate range	333.334 kb/s to 675 Mb/s	20.834 Mb/s to 3.35 Gb/s	620 Mb/s to 7 Gb/s,	620 Mb/s to 13.5 Gb/s
Data module back-ends	E4832A	E4861A	N/A	N/A
Generator front ends	E4838A	E4862A	N/A	N/A
Analyzer front ends	E4835A	E4863A	N/A	N/A
Generator modules	N/A	N/A	N4874A	N4872A
Analyzer modules	N/A	N/A	N4875A	N4873A
Compatible clock modules	E4805B/E4808A/ E4809A	E4808A/E4809A	E4809A	E4809A
Max. number of channels[1], 1 frame / 3 frames	44 / 132	22 / 66	10 / 30	10 / 30
adressed I/O technology	LVDS, PECL, ECL, TTL, 3.3V CMOS	LVDS, CML, PECL, ECL, low voltage CMOS	LVDS, CML, PECL, ECL, low voltage CMOS	LVDS, CML, PECL, ECL, low voltage CMOS
Data capability	PRWS/PRBS	PRWS/PRBS	PRWS/PRBS	PRWS/PRBS
user memory	2 Mb	16 Mb	64 Mb	64 Mb
Input / Output	differential & single ended	differential & single ended	differential & single ended	differential & single ended
Data format	RZ, R1, NRZ, DNRZ	RZ, R1, NRZ, DNRZ	NRZ, DNRZ	NRZ, DNRZ
transition times 20%-80%	0.5-4.5ns, var (10-90%)	<75ps	<20ps	<20ps
amplitude resolution	0.1-3.5V, 10mV	0.05V-1.8V, 10mV	0.1 1.8V, 5mV	0.1 1.8V, 5mV
window	-2.2 to 4V	-2 to 3.5V	-2 to 3V	-2 to 3V
input voltage ranges	0 to 5V -2 to 3V	-2 to 1V, -1 to 2V, 0 to 3V	-2 to 3V, 2Vpp	-2 to 3V, 2Vpp
sensitivity	50mV typ., diff.	<50mV	<50mV	<50mV
sample delay resolution	2ps	1ps	100fs	100fs

1. ParBERT 81250 controlled via IEEE 1394 link and external PC

Parallel BER measurements up to 13.5 Gb/s

For characterization of parallel or multi-lane interfaces ParBERT 81250 can generate and analyze data clock-synchronously. However, generator skew and analyzer sample point timing can be programmed independently per channel as well as generator levels or analyzer thresholds. The BER is reported per lane and port (see figure 2).

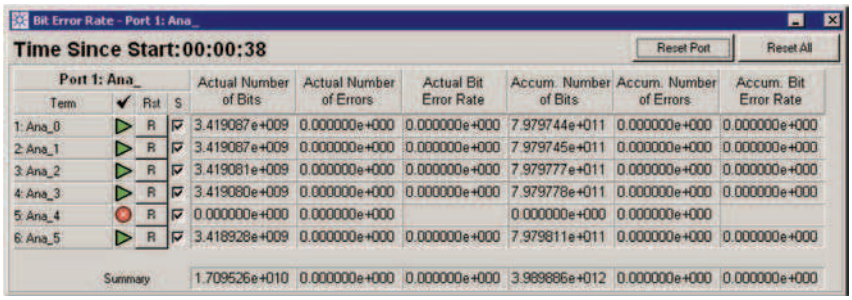

Figure 2. BER results screen

PRBS/PRWS and user defined patterns

A common test pattern for serial (communication) links is a Pseudo Random Binary Sequence PRBS. To simplify Mux/DeMux testing ParBERT provides the so-called Pseudo-Random-Word Sequences (PRWS) for generation and as expected data for analysis. A PRWS consists of a PRBS per lane with a lane-to-lane delay chosen such that, when muxed together, the same PRBS-polynomial as on each lane of the parallel side is generated on the serial side.

The appropriate lane-to-lane delay is determined by the number of lanes (see figure 3). In addition, ParBERT's pattern memory enables user defined test patterns as well.

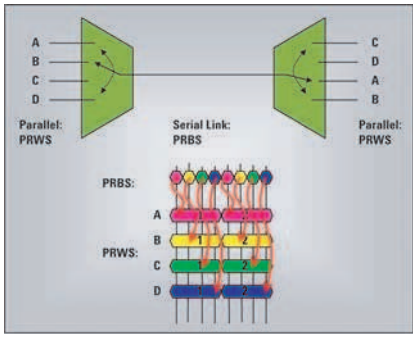

Figure 3. MUX/DEMUX application: relationship between PRBS and PRWS

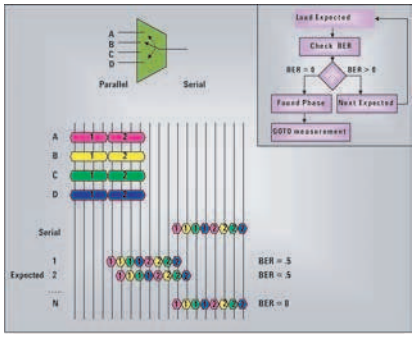

Figure 4. Mechanism of auto-phase and auto-delay assignment

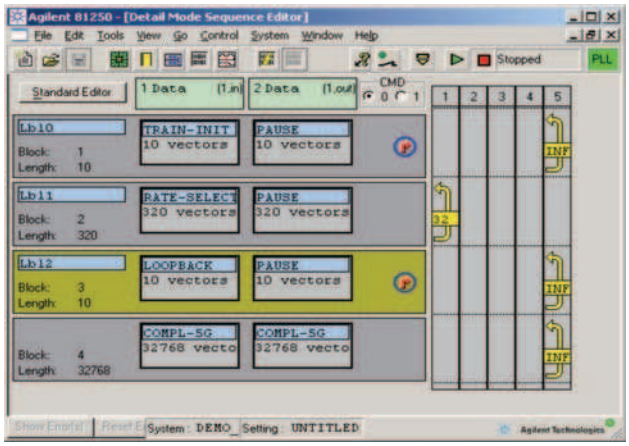

Figure 5. ParBERT detail mode sequence editor screen

Pattern sequencer

Physical layer testing includes the establishment or termination of a connection or the set-up of a DUT into a specific test mode, e.g. a loop-back of received data. Furthermore, specific device parameters often correlate with suitable test patterns. To perform such complex tests in one shot without interruption to download different test patterns, the ParBERT 81250 is equipped with a powerful pattern sequencer allowing up to five nested loops and branching on internal and external events or upon SW command.

Set-up is made easy through the powerful ParBERT 81250 graphical sequence editor, which also aids you maneuvering around HW restrictions when setting up user patterns not directly matching selected block lengths. Debugging of the test sequence is supported e.g. by highlighting the currently executed block within the sequence (see figure 5). Combining sequencing and precise timing with internal or external generator channel-add allows realization of e.g. user defined multi-level or de-emphasized signals.

Automatic data synchronization

The latency between DUT input and output is often not exactly known or not even deterministic. Having to set ParBERT's sample point for analysis manually would be tedious.

Therefore ParBERT 81250 analyzers provide three modes to automatically synchronize and align upon expected data with BER below a user defined threshold as a criteria (figure 5).

- **Auto Bit Sync**
  Finds the proper bit position in a data stream. For memory based patterns a unique detect word is required. Automated phase alignment is optional.
- **Fast Bit Sync**
  Possible for PRBS/PRWS only. Especially useful for burst-mode applications, e.g. optical re-circulating loops.
- **Auto Delay Align**
  Only the sample point timing of the analyzers is adjusted. The latency between input and output must be within the delay range of the analyzers used.

For applications w/o expected data with ParBERT running in data acquisition mode, e.g. for A/D test, proper sample point adjustment can automatically be achieved with the CDR / lane mode (7 and 13Gb/s analyzer modules only)

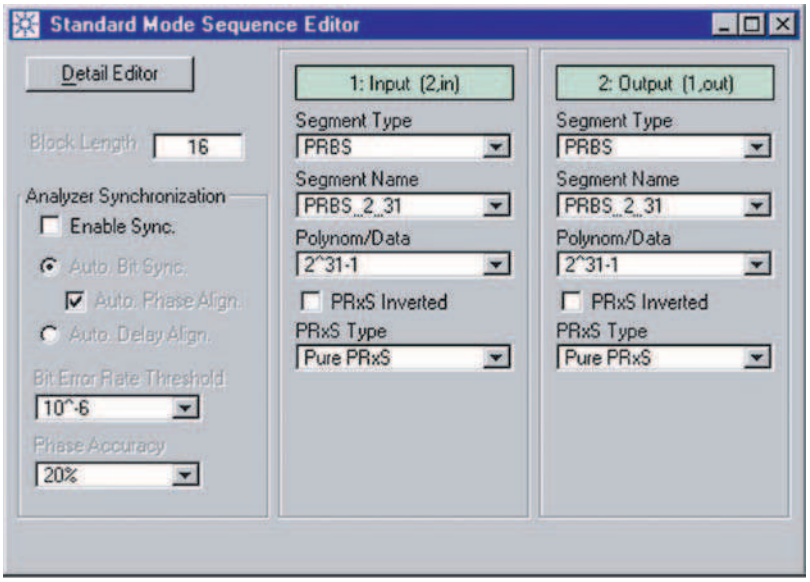

Figure 6. ParBERT standard mode sequence editor with PRBS/PRWS patterns and data synchronization mode chosen

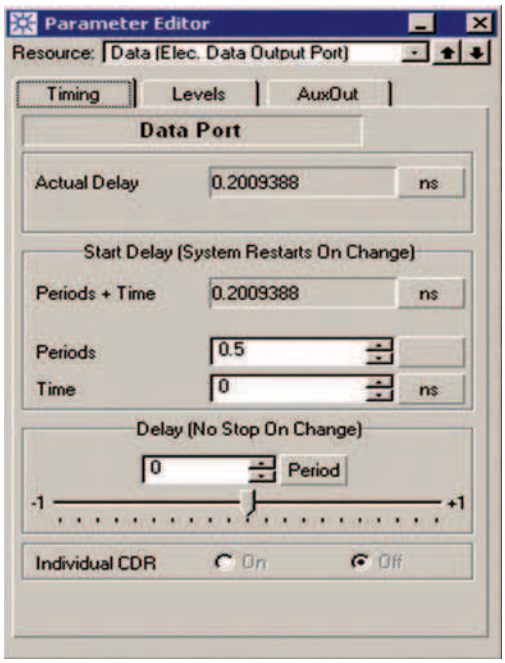

Figure 7. Analyzer delay can be changed without stopping the system, CDR/lane can be enabled

Interrupt-free change of analyzer and generator delay

The analyzer sample timing can be adjusted ±1 period while the instrument keeps running w/o interrupting the measurement (see figure 7).

For the 13.5 Gb/s, 7 Gb/s and 3.35 Gb/s the delay of the generator modules can be adjusted ±1 period while running as well.

Different data rates

The architecture of ParBERT 81250 allows using data modules of different speed classes in one clock group. Choosing the right combination of system data rate and binary frequency multipliers (..., 1/16, 1/8, 1/4, 1/2, 1 , 2 ,4 ,8 , 16, ...) enables each module to operate within its valid data rate range. Furthermore even channels within one module can operate at different data rates of binary ratio (see figure 8).

ParBERT can be configured with one or more clock groups each controlled via an independent instance of the GUI. The clock groups can either run completely independent from each other or can be locked to each other in a frequency ratio of m/n, with m, n=1...256 and m x n<1024. In chapter "ParBERT 81250 application examples" on page 17 some configurations with two clock groups are shown.

Jitter injection and spread spectrum clocking SSC

Receiver margining is a measurement that is very demanding in terms of signal conditioning capabilities of the stimulating pattern generator, because it shall emulate worst case conditions as they may appear in mission mode of the DUT or as they are specified in relevant standards. For this purpose not only voltage levels and cross point of differential signals shall be adjustable. Jitter shall be injected as well. For this purpose the higher data rate modules of ParBERT, i.e. the 3.35 Gb/s, 7Gb/s and 13.5 Gb/s generator modules are equipped with a delay control input, that allows phase modulation of the data output signals equivalent to the applied voltage signal.

Modern computer standards use spread spectrum clocking (SSC) techniques to decrease the power density of radiated emissions per frequency. The 13.5 GHz clock module allows direct feed-through of such a multi-UI low frequency modulated external clock enabling the data modules to generate and analyze such data patterns with SSC. Agilent's signal generators can be used to generate such a modulated clock.

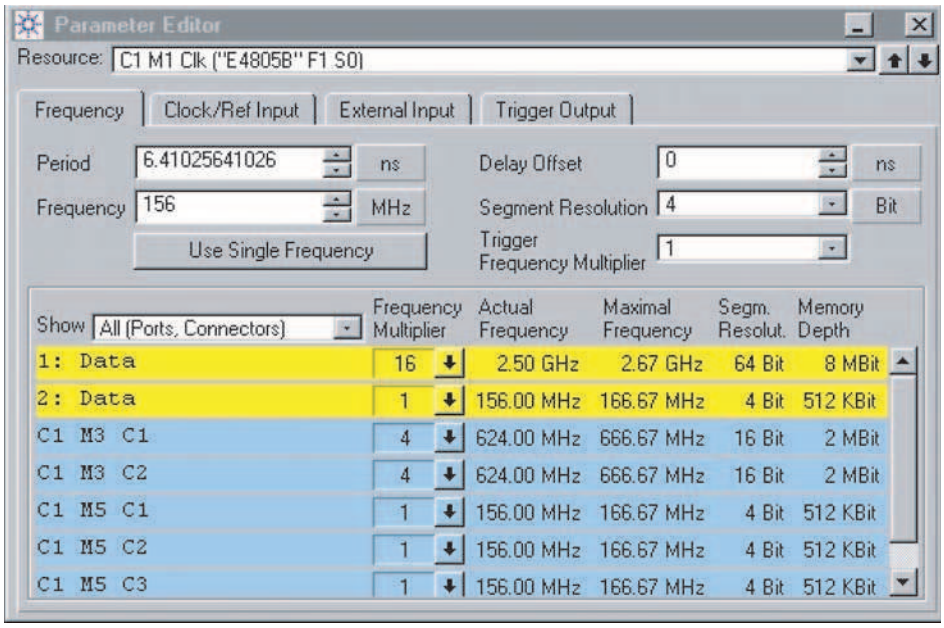

Figure 8. Parameter editor for setting multiple frequencies in one system

ParBERT Measurement software consists of six different measurements that deliver graphical and numerical results allowing in-depth characterization for use in R&D and Device Verification (DV). Fast pass/fail tests against user definable limits for manufacturing purposes are provided as well.

ParBERT, as any other BERT, physically can only do one measurement: it digitizes the input signal with respect to a predefined **threshold voltage** and, at a predefined portion of the bit width (the **sample point**), compares this to its expected data and counts an error if it doesn't match the expected binary value.

ParBERT Measurement Software

automates the variation of these mentioned parameters (sample point timing and threshold voltage) and the repetition of this measurement for a number of subsequent bits and by this allows performing a variety of measurements:

1. **BER measurement,** targeting the error performance of a complete system under test
2. **DUT output level measurement**
3. **Eye opening**
4. **DUT output timing measurement**
5. **Spectral decomposition of jitter**

allowing in depth pin- and port-wise characterization of the output performance of a transmitter (TX) under test as it is typically required in **R&D** or during **DV**. Graphical representation(s) of the test result (e.g., pseudo color plot and contour plots) are available as well as a multitude of extracted or extrapolated numerical values. Pass/fail criteria can be defined for every numerical result, simplifying a fast test against limits making it well suited for **manufacturing** as well.

Reduction of test time as it is usually desired in manufacturing is possible using the

6. **Fast eye mask measurement** that requires a much smaller number of measured bits.

Each of the six measurements is an active-X component, which simplifies its integration into any test executive written with Agilent VEE Pro, National Instruments' LabVIEW, Excel, Agilent TestExec, C/C++, C# and Microsoft® VisualBasic.

The MUI comprises a Windows (2000, XP or Vista) based GUI that simplifies test set-up and execution. Measurement results can be exported and printed.

The measurement software is included in the standard ParBERT 81250 software package. It works as a client to the ParBERT firmware server and can run on that PC that hosts the firmware server and is connected to the HW through the slot -0 controller, or on any other PC that is connected (e.g. via LAN) to this mentioned PC.

BER measurement

During the bit error ratio (BER) measurement sample point timing and threshold voltage are kept constant, usually at the optimum values in the middle of the TX's output eye. ParBERT performs its standard BER-measurement as described above.

Compared to the BER-measurement of the regular GUI which reports the number of received bits and errors and their ratio, the BER, as actual and accumulated values (for last measurement timeframe and since start of measurement), the BER measurement of the MUI delivers additional information and measurement control:

Errors for expected ones and zeroes are counted and reported separately.

Repetitive and single shot measurements can be set-up along with error counting, run-mode options and stop criteria such as logging, automatic resynchronization or stop after a specified number of errors, bits or seconds.

These features enable R&D usage for root cause failure analysis (e. g. BER log during a temp cycle), as well as manufacturing with minimum sample sizes and short measurement times.

Table 2. BER measurement

Measurement parameters	
	Compared bits Errors from expected 0s Errors from expected 1s Total errors Parameters from last measurement period Accumulated parameters
Measurement mode	
	Single or repetitive Repetition rate is programmable in seconds (In this mode resynchronization can be enabled)
Pass/fail	
	For actual and accumulated parameters
Log file	
	Logs all measured parameters

Output level measurement

This measurement performs an automated sweep of the analyzer threshold voltage at constant, usually optimum, sample timing, while it continuously measures the BER. The result is displayed in an unusual but intuitive way, i.e. the threshold voltage (the input parameter) is plotted on the vertical axis and the BER (the result), on the horizontal axis (Figure 12a). A histogram of BER versus threshold is derived (Figure 12b) and is used to calculate mean value and standard deviation for one- and zero-levels. Furthermore the Q-factor can be derived from the tail fitting operations of the innermost (highest low-level and lowest high-level) Gaussian distributions of the BER histograms (Figure 12c).

Table 3. Output Level Measurements

Numerical Measurement Results	
	High/low level
	Mean level
	Amplitude
	Threshold margin
	High/low level standard deviation
	Peak to peak noise
	Signal/noise ratio (rms & peak-to-peak)
	Q-factor
	Q-factor optimum threshold
	Q-factor residual BER
Pass/fail	
	For all numerical results
	Each one can be enabled individually
Graphical Result Displays	
	BER versus threshold
	BER histogram versus threshold
	Q-factor from BER versus threshold

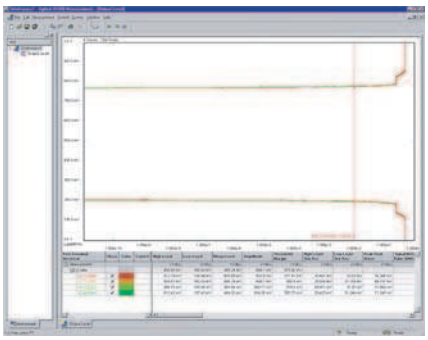

Figure 12a. BER versus threshold

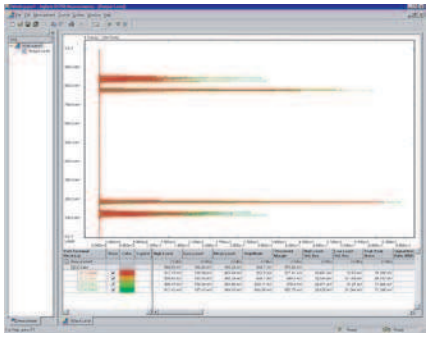

Figure 12b. BER histogram versus threshold

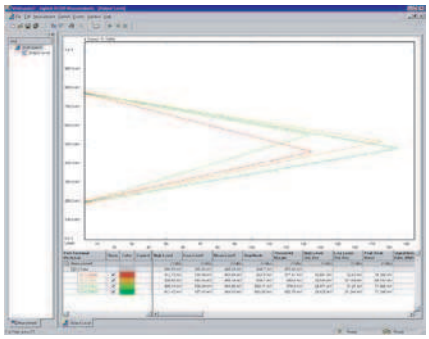

Figure 12c. Q from BER versus threshold

Eye opening

During this measurement both sampling point timing and analyzer threshold voltage are automatically swept, while BER is recorded and plotted either as a pseudo-color- or a contour-plot (see figure 9 a,b,c), giving the user intuitive and in-depth information of the pulse- or eye-performance of the RX under test.

Range and resolution for the measurement parameters and pass/fail values are user definable.

Table 4: Eye opening

Numerical Measurement Results	
	Optimum sample Point delay Optimum threshold Eye opening (Volt)Phase margin
Pass/fail	
	For all parameters Each parameter can be individually enabled
Graphical Result Displays	
	pseudo color plot BER-contour Two markers: voltage, delay, BER

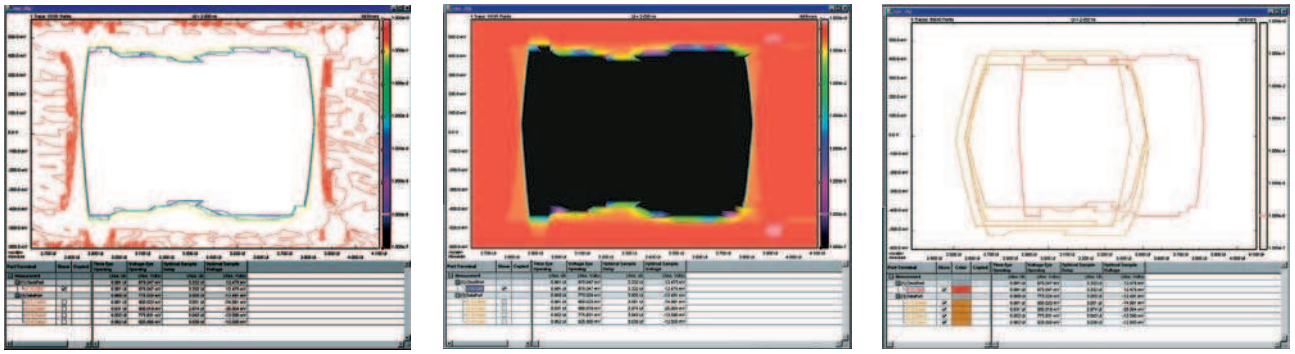

Figure 9a/b/c. View the BER for one terminal as a pseudo color plot or contour plot or equal BER at BER threshold

Fast eye mask

The eye opening measurement as above reveals a lot of detailed information but can be time consuming, especially when a fine resolution has been chosen, which maybe required and tolerable during the R&D phase, but probably not during manufacturing. For this purpose the fast eye mask measurement was developed. From one up to 32 measurement points can de defined where the BER shall be measured. A measurement point is defined as a pair of sample point timing and threshold voltage. Both can be defined in absolute values or relative to the automatically determined eye opening / optimum sampling point and threshold.

Very often six measurement points are sufficient (see figure 11) to guarantee a certain pulse/eye performance. For reasonable BER values the whole measurement usually only takes a few seconds.

Measurement results provided:

- BER at pre-defined sample point and threshold voltage
- pass/fail results

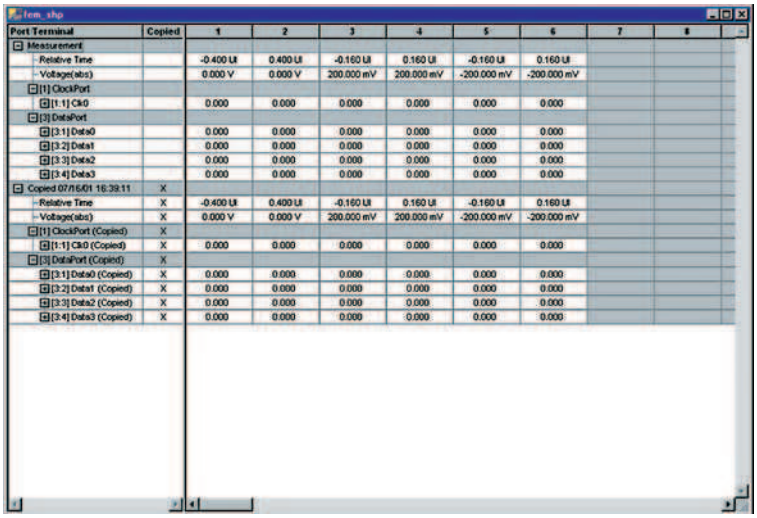

Figure 10. The fast eye mask setup and results window

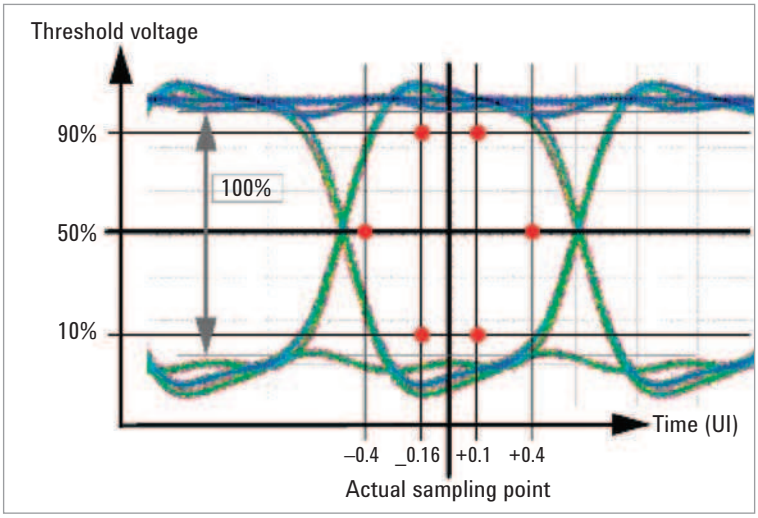

Figure 11. The fast eye mask setup and results window

DUT output timing measurement

Probably the most important routine as it enables a real measurement of Total Jitter (TJ) in contradiction to just an extrapolation. In addition it performs jitter decomposition and delivers numerical results for Random (RJ) and Deterministic Jitter (DJ) according to the dual-dirac model.

During this measurement the sample point timing is automatically swept with constant, usually optimum analyzer threshold voltage while BER is continuously measured.

The result display of this so-called BER-scan measurement, i.e. the BER vs the sample point delay, is because of its shape, often called the “bath tub” curve.

All measured curves are centered around the optimum sampling point delay of the port allowing to determine edge to edge skew between the data lanes of a data port. Clock to data delay per channel equivalent to set-up and hold-time condition of a RX driven by the TX under test, can be measured. When (depending on the synch mode) absolute timing is available , the delay value at optimum sample point is provided as well.

There is also a numerical view that shows the “numerical return values” for the selected BER threshold only.

Another flavor of the BER-scan is the fast total jitter (FTJ) measurement, which by measuring for each delay point only as many bits as required to determine if the BER is above or below the target BER, delivers the horizontal eye opening, i.e. the TJ in much shorter time.

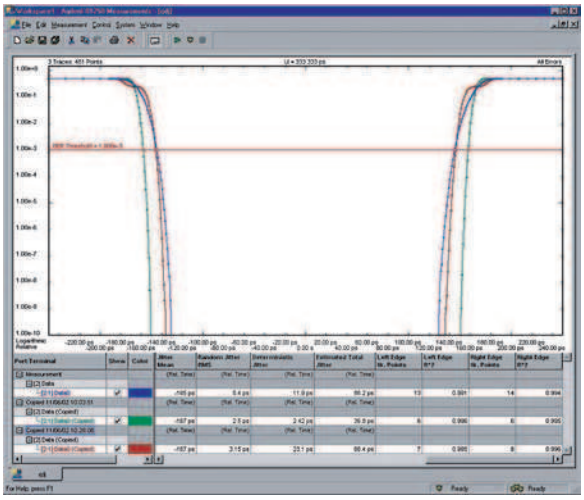

Figure 10a. View the DUT output measurement results as a bathtub curve

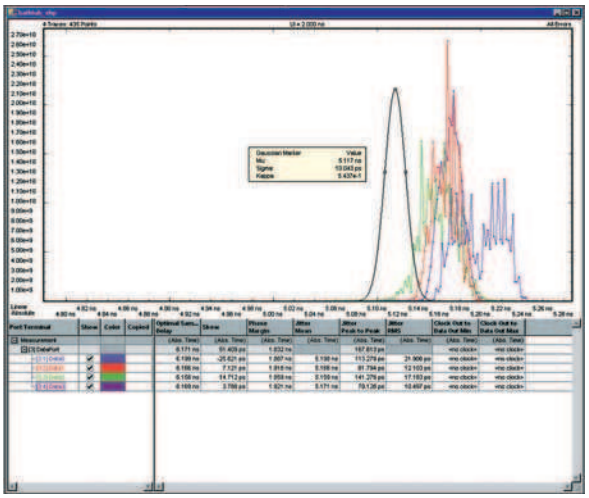

Figure 10b. View the DUT output measurement results as a histogram

Table 6. DUT output timing measurement

Timing parameters	
	Optimum sample point delay Phase margin Clock to data out minimum Clock to data out maximum Skew between channels
Jitter parameters	
	RMS jitter Mean value Peak peak jitter for specific BER
Pass/fail	
	For all timing and jitter parameters Each parameter can be individually enabled
Graph	
	View of BER versus sample delay 2 Markers: delay, BER

Spectral Jitter decomposition

This measurement is different from all the above because the sample point is unusually set exactly to the crossing point of the eye and because it is post-processing the captured error data utilizing FFT, to extract the desired result, i.e. the embedded jitter spectrum. This is extremely helpful for R&D to separate deterministic components from the Random Jitter (RJ) "noise"-floor and by this pinpointing e.g. sources of undesired crosstalk. Using this measurement with pass/fail limits applied during manufacturing test it ensures that certain known contributory jitter frequencies do not increase above a safe limit. You can also measure the frequency response of a CDR or a PLL's in one shot, by applying white random jitter RJ on the ref clock or the incoming data stream (see figure 11b).

Table 7. Spectral decomposition of jitter

Measurement parameters	
	Data segment length FFT windowing
Numerical results	
	BER, total power, noise power, frequency and power of n highest power jitter frequencies
Pass/fail	
	Power factor
Graphical result displays	
	Spectrum graph (power vs. frequency)

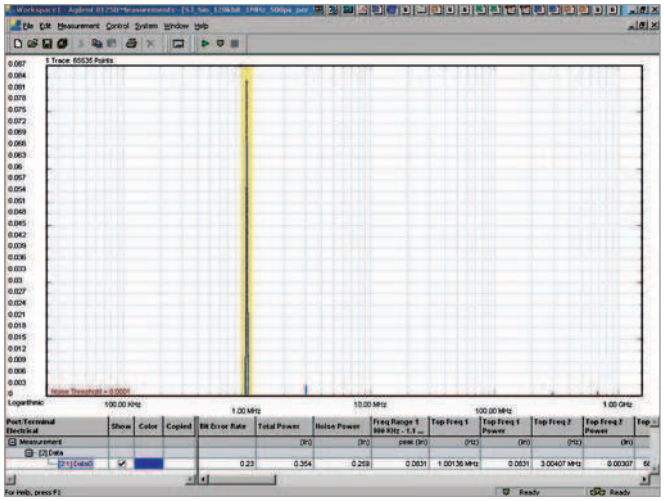

Figure 11a. Spectral decomposition of Jitter with a large peak at 1MHz

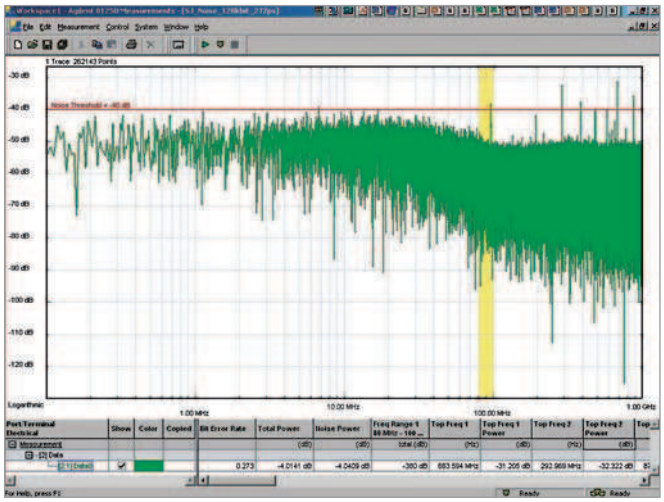

Figure 11b. Jitter transfer of a CDR with a corner frequency of approximately 40 MHz

10Gb Ethernet

Frame Generator and Post processing tool for 10GbE applications

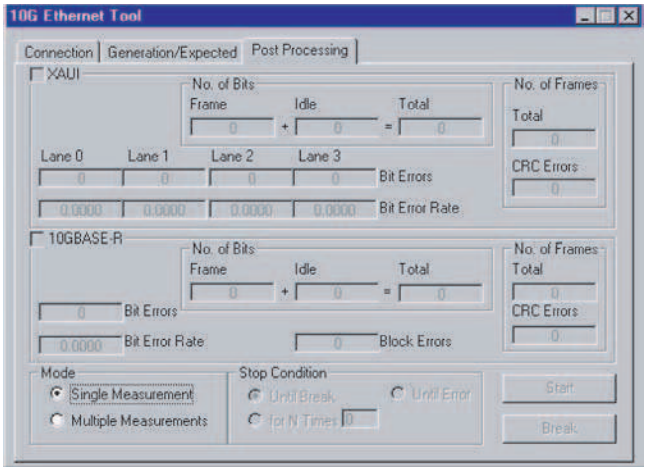

Figure12a. 10 GbE processing tool

SONET/SDH

Frame Generator for SONET/ SDH for serial (e.g. OC192, segment width = 1) or parallel applications (e.g. OC768, segment width = 4, or 16 depending on serializer (mux) in use)

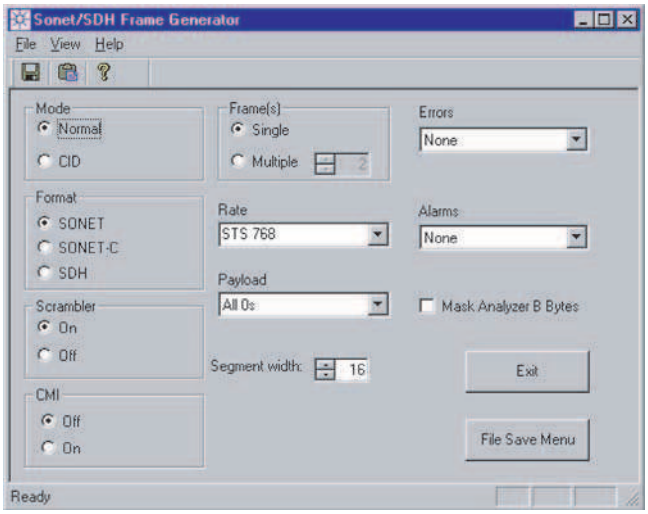

Figure 12b. SONET/SDH editor

SFI5

Post processing tool for analysis of 16 data lanes and 17th deskew (DSC) bit, which ensures that

- the 16 data channels are valid (valid PRBS 2^7 - 1 or 2^{11} - 1) streams
- the 16 data channels are within skew specification
- the DSC (17th) bit is valid
  - correct header
  - match to the 16 data channels

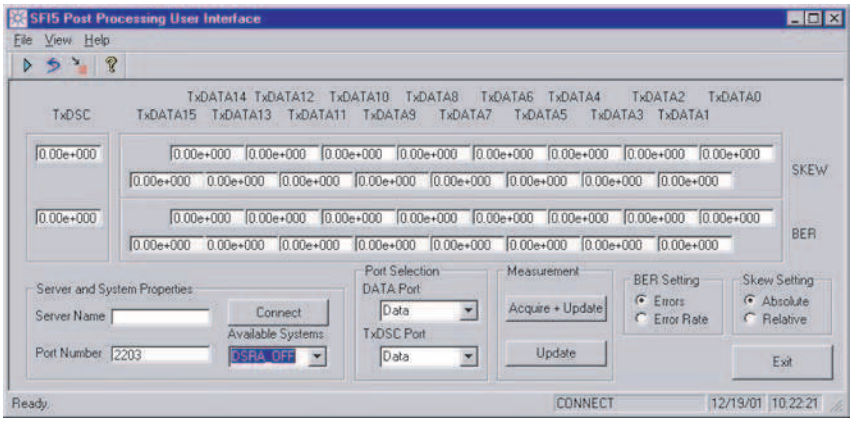

Figure 12c. SF15 post processing

ParBERT is a very versatile instrument usable in a variety of different applications across the industries. Some examples are briefly introduced below. In the context of this brochure the description is focused more on relevant ParBERT capabilities utilized for that specific application than on imparting in-depth knowledge on how to perform the related measurement task. For this purpose please refer to the related application notes which along with some other applications not mentioned here can be found under **www.agilent.com/find/ParBERT.**

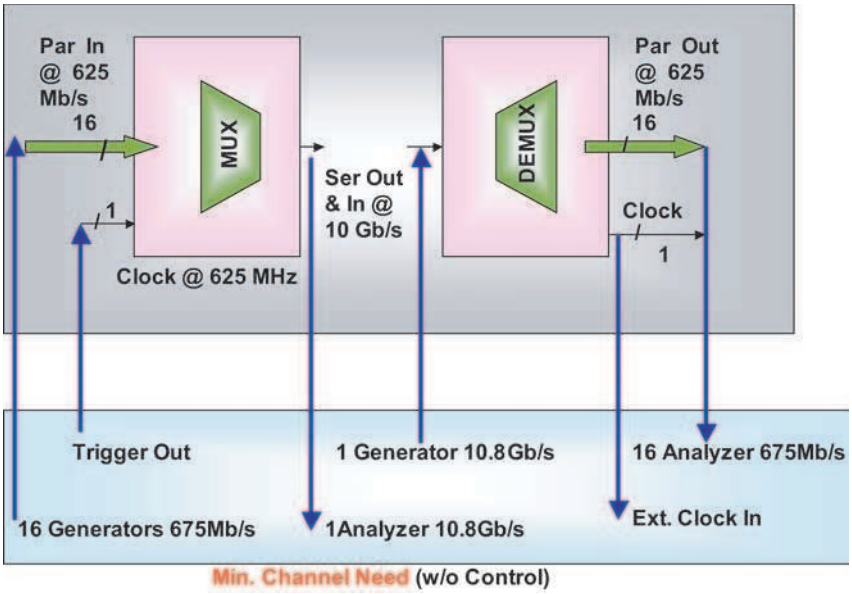

Figure 13. OC 192 example

OC 192

Probably the most basic and instructive application for ParBERT's capabilities is a clock synchronous mux/de-mux test e.g. found in the SONET/ OC 192 telecom arena. ParBERT masters the requirements resulting from the different data-rates at the parallel and serial side easily and cost efficient utilizing modules of different speed classes and running them at (binary weighted) data rates as depicted in figure 8.

For the different tests ParBERT can be connected at either interface for signal generation and/or analysis so that both parts (mux and de-mux) can be tested simultaneously creating an environment similar to mission mode of the DUT and furthermore saving test time.

Depending on the desired test result and the test patterns used it can however be advantageous to use more than one central clock module and combine generators and analyzers in separate clock groups eliminating limitations in synchronization.

10GbE-XAUI

This example depicted in figure 14, seems similar to the one above as the DUT again is some sort of mux/demux. However, in this 10GbE LAN application the data rates between parallel (XAUI: 4 x 3.125 Gb/s) and serial side 10GbE: 1 x 10.3125Gb/s) have a ratio of 3.3 (= 4 x 8/10 x 66/64), which stems from the different codings on each side (8B/10B and 66B/64B). ParBERT can either be used as the clock master with e.g. one clock module running at 10.3125Gb/s and the other at a rate of 10/33 or with both clock modules tied to the DUT-internal reference clock multiplying this by 66 or 20 respectively.

When the DUT is a complete XENpac module with its electrical XAUI-I/Os on the parallel side and optical I/Os on the serial side ParBERT can be complemented w/ optical E/O and O/E converter modules to completely address this application. Again, it maybe advantageous to separate generators and analyzers in different clock groups so that the optimum ParBERT configuration may consist of four clock modules and 6 data modules (2 x 13.5Gb/s and 4 x 3.35Gb/s with two generator or analyzer channels each).

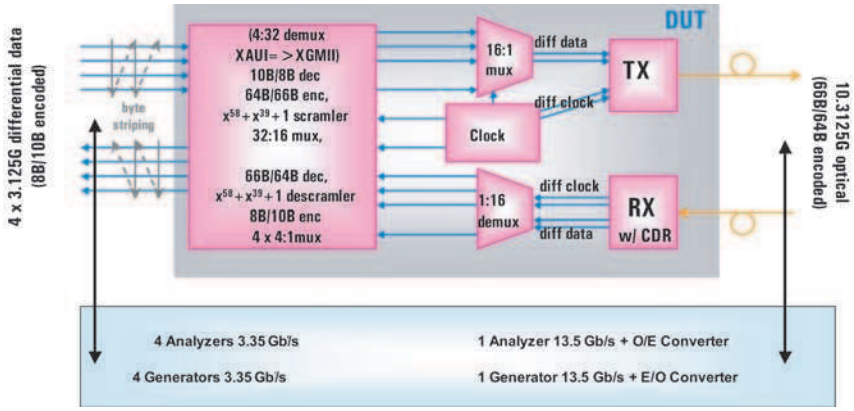

Figure 14. 10 GbE XAUI module

PON

The last example from the optical communication domain is about passive optical networks (PON) based on time division multiple access (TDMA) as used by GPON and BPON.

The most critical sub-module in this system is the receiver RX of the optical line terminal (OLT) in the central office which has to deal with the upstream signal bursts arriving from the optical network units (ONU) as depicted in figure 15. The spacing between them is very short and the amplitude maybe very different, such that the RX in the OLT must settle to the appropriate threshold and synchronize its internal PLL in a very short time.

A test set-up consisting of ParBERT 81250, Agilent's Lightwave Measurement System (LMS) 8163B/8164B and a Digital Communication Analyzer (DCA) 81600C emulating the important portions of a PON is depicted in figure 16. ParBERT's exact timing capability for the two data burst and the related laser control signals is essential for standard compliant testing and characterization of the OLT's RX. The pattern sequencer allows the set-up and generation of the burst-packages with desired content.

The SW controlling ParBERT and the other instruments can be written in a language of your choice. It can run on the same PC that the ParBERT SW resides on. Using e.g. visual Basic or C allows utilization of the Plug & Play libraries provided with ParBERT (and many other instruments), which simplifies programming a lot.

For more information:
www.agilent.com/find/PON

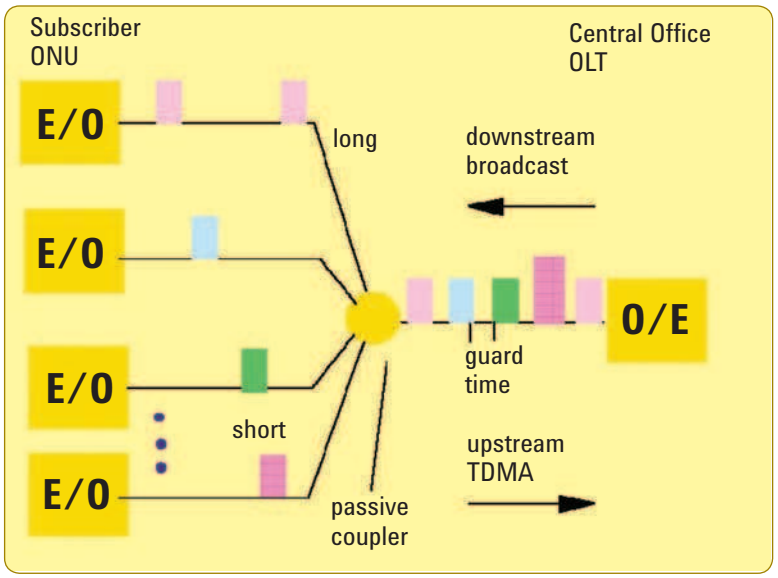

Figure 15. TDMA bursts travelling upstream on a passive optical network Figure 41: TDMA bursts travelling upstream on a passive optical network

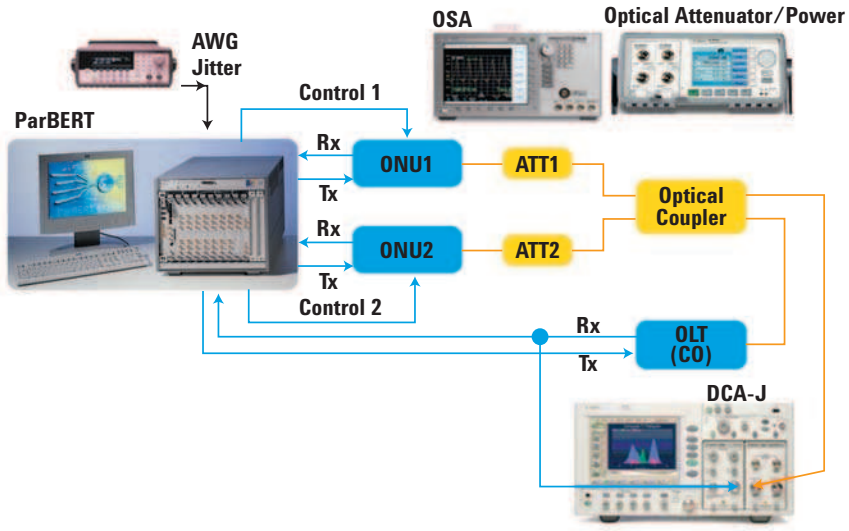

Figure 16. ParBERT based test set-up for characterization of OLT

HDMI

The High-Definition Multimedia Interface (HDMI) is an industry-supported, uncompressed, all-digital audio/video interface. HDMI provides a connection between any compatible digital audio/video source, such as a set-top box, DVD player, or A/V receiver and a compatible digital audio and/or video monitor, such as a digital television (DTV). For this application Agilent provides a complete test solution, i.e. the Agilent TMDS Signal Generator. Its hardware is based on ParBERT and the test SW is based on the N5990A Test Automation Software Platform.

ParBERT provides the data channels D0, D1 and D2 to cover the three colors green, red and blue. The fourth channel D- is used as intra-pair skew channel to provide additional skew testing capability between normal and complementary data as defined in the HDMI standard.

A clock signal is also provided. The SW guides the user through the test set-up (figure 17), allows the definition of ParBERT data packets in user terms with its "HDMI Frame generator" and performs automated measurement of the full HDMI jitter tolerance curve.

For more information:
www.agilent.com/find/hdmi_sink_test

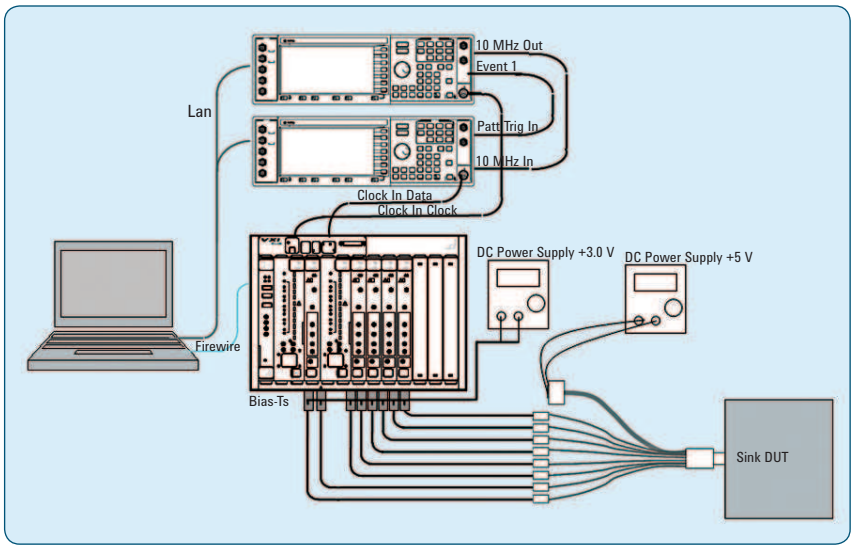

Figure 17. Sink test connection setup example

MIPI

The mobile industry processor interface (MIPI) is a standard used throughout the field of mobile communication. Several versions addressing different speed classes are already defined or under definition.

MIPI D-PHY is the standard for a serial bus used in battery operated equipment (e.g. a cell phone) to connect high data capacity devices like the camera module. Battery life is always a key issue of portable electronics. MIPI D-PHY therefore operates in two modes, low power/low data rate (max 20 Mbit), and high data rate mode.

The low power mode works single ended on standard CMOS levels while signaling and high data rate use LVDS. The transition between modes happens dynamically and is therefore one of the critical areas that require testing. Using ParBERT modules of different speed classes and adding their output signals passively allows generation of the depicted waveform (figure 18) with the ParBERT-typical freedom to define all levels timing and data content enabling tailored receiver stress tests for R&D and manufacturing.

For more information:
www.agilent.com/find/mipi_dphy

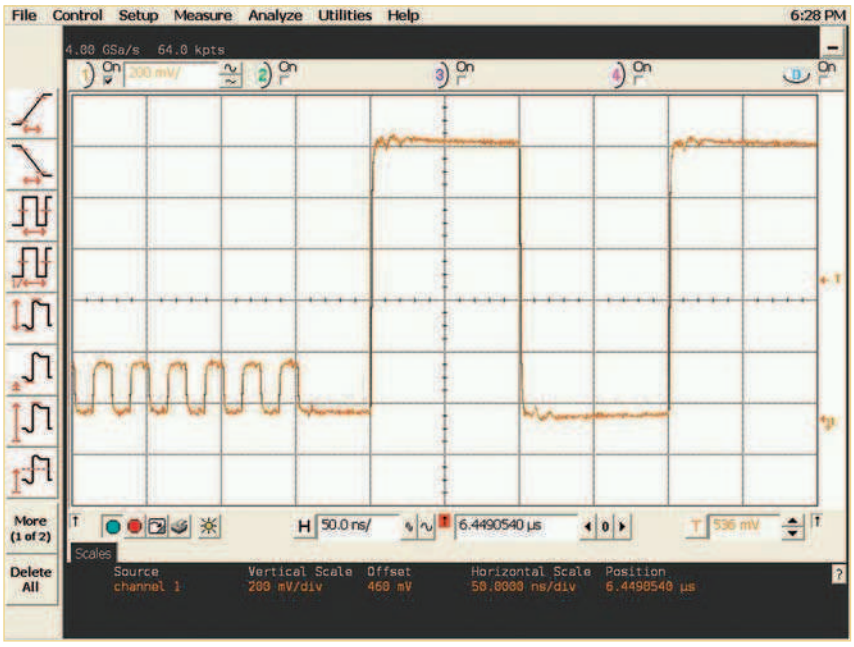

Figure 18. Zoom into the bit level of the D-PHY stimulus signal switching between HS and LP mode

PCI Express

PCIe shall be used as an application example from the computer industry. This bus consists of up to 16 differential point to point connections, so called lanes. Architectural it is not a traditional synchronous, parallel bus instead a multiple serial bus. Symbol rates are 2.5Gb/s, 5Gb/s and 8Gb/s for the three generations of the standard already defined or in process. Generation 1 and 2 use 8B/10B coding with a relatively high overhead of 25%. For the third generation this coding scheme was dropped because of its data rate penalty.

For the first generation with its moderate symbol rate of 2.5Gb/s an RX test was not defined. This has changed since the second generation, where for RX jitter tolerance test, a quite complicated cocktail was defined. While a single lane can be tested with a serial BERT such as the Agilent N4903 J-BERT, an extensive and more realistic simultaneous test of more than one lane can only be achieved with a ParBERT. In order to generate test patterns with the required jitter cocktail ParBERT makes use of its jitter modulation capability via the external delay control input. Figure 19 shows a setup with Agilent 33220 and 81150A acting as jitter modulation sources. The whole setup is structured into three clock groups. The first with the 33250 being connected "only" generates a modulated clock that the second ParBERT system runs from. With the help of the 81150A and an accessory filter the random jitter RJ with the required spectral distribution is created. The third clock group holds ParBERT analyzers that by measuring BER check if the RX under test tolerated the amount of jitter applied at its input and extracted the data content correctly, i.e. with a BER below the specified limit.

Specified test patterns can be created utilizing ParBERT's custom pattern memory and its sequencer. External control SW takes care of proper calibration and test automation.

For more information:
www.agilent.com/find/pcie_receiver_test

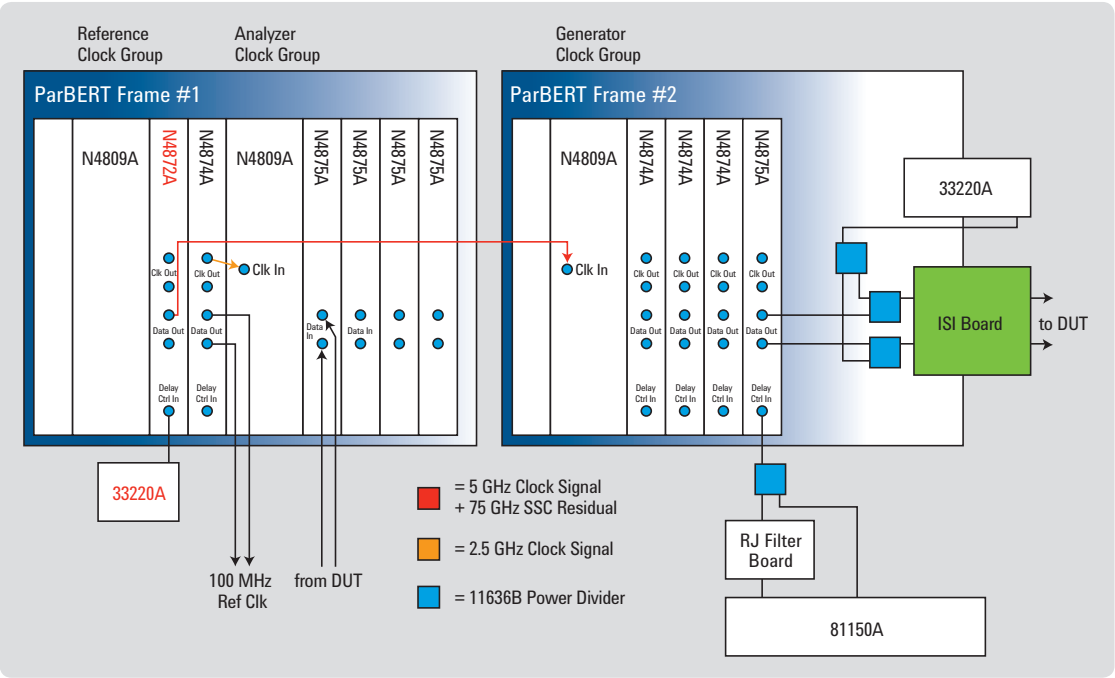

Figure 19. Example measurement set-up for a PCIe™ RX test with 4 data lanes

A/D converter test

This last example, basically a semiconductor test application, is very interesting in such that a parallel bit error tester, i.e. the ParBERT is used although literally a BER cannot be measured at all.

The DUT is an A/D converter such as it is used in satellite communications. The problem that an A/D converter as a DUT presents to a BERT lies in the nature of A/D conversion. Even if the A/D converter works within its specification, quantization may have an inaccuracy of at least a bit, probably a few. This means, that when applying an analog input signal at the A/D's input, its output value can not be predicted bit-wise. So the only way of testing the performance of the A/D converter is capturing its output data, and doing an appropriate post processing on the uploaded data.

The analog input signal for the A/D test may come from a signal generator or, in a back-to-back configuration, from an appropriate D/A converter driven by ParBERT generators. Analyzers with their deep capture memory are used to record the A/D's output data and make it available for later post processing.

Although this set-up sounds simple, details such as setting a correct sample delay maybe tricky, as the overall propagation delay of the A/D converter or an individual lane maybe unknown. All the nice BERT-typical autosynchronization features that ParBERT offers do not work, as they need expected data. However, ParBERT solves this problem in a very user friendly way: its built-in CDR with its CDR/channel feature enables automated sampling at optimum sample point for each channel.

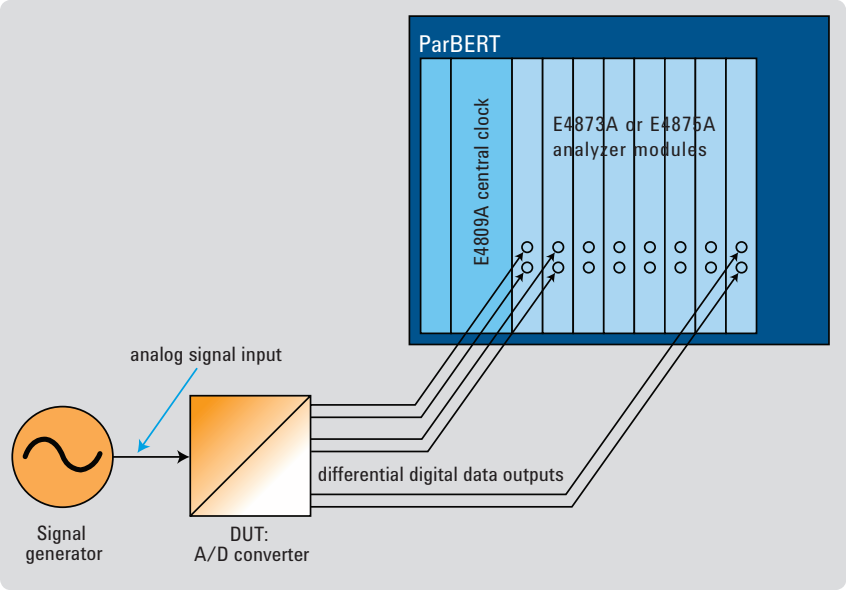

Figure 20. Example measurement set-up for an 8bit A/D converter utilizing ParBERT's CDR/channel feature for automated optimization of sampling point

Agilent N4872A ParBERT 13.5 Gb/s Generator
Agilent N4873A ParBERT 13.5 Gb/s Analyzer

Technical Specifications
Version 1.0

General

The N4872A generator and N4873A analyzer modules are each one VXI slot wide and operate in a range from 620 Mb/s up to 13.5 Gb/s. The ParBERT 13.5 Gb/s modules require the E4809A 13.5 GHz central clock module, which is two VXI slots wide. All specifications, if not otherwise stated, are valid at the end of the recommended N4910A cable set (24" matched pair 2.4 mm).

The N4872A generator module generates hardware-based PRBS up to 2^{31}- 1, PRWS and user-defined patterns and provides a memory depth of 64 Mbit. The N4873A can synchronize on a 48 bit detect word, or on a pure PRBS pattern without detect word.

Timing specifications

The ParBERT 13.5 Gb/s modules are able to work with three different clock modes.

- *Internal clock mode:* The common clock mode is provided by the E4809A 13.5 GHz central clock module, which generates clock frequencies up to 13.5 GHz.
- *External clock mode:* The system also works synchronously with an external clock, which is connected to the E4809A clock module.
- *CDR mode:* To use the N4873A 13.5 Gb/s analyzer CDR capabilities, connect the analyzer's CDR out to the E4809A clock module's clock in.

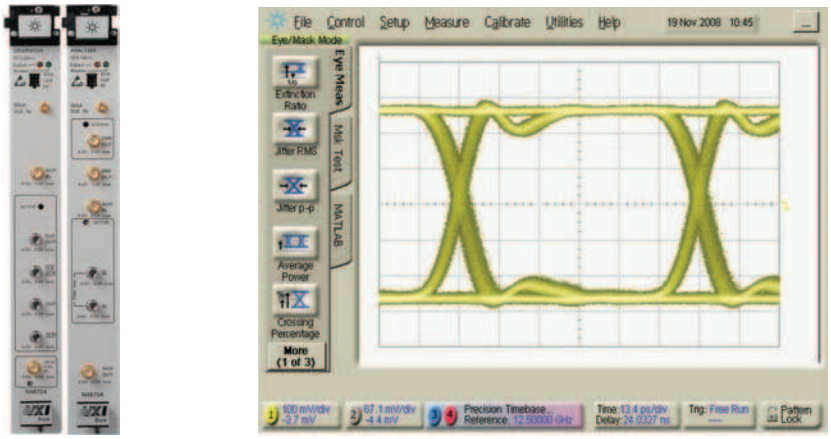

Figure 21. N4872A & N4873A and waveform

Table 10. N4872A data generator timing specifications (@ 50% of amplitude, 50 Ω to GND)

Frequency range	620 Mb/s to 13.5 Gb/s
Delay = start delay + fine delay	Can be specified as leading edge delay in fraction of bits in each channel
Start delay range	0 to 100 ns
Fine delay range	± 1 period (can be changed without stopping)
Delay resolution	100 fs
Delay accuracy	±10 ps ± 20 ppm relative to the zero-delay placement. (@ 25 °C - 40 °C ambient temp.)
Relative delay accuracy	±2 ps ± 2% typ. (@ 25 °C - 40 °C ambient temp.)
Skew between modules of same type	20 ps after cable deskewing at customer levels and unchanged system frequency. (@ 25 °C - 40 °C ambient temp.)

Sequencing

The sequencer receives instructions from the central sequencer and generates a sequence. The channel sequencer can generate a sequence with up to 60 segments.

An analyzer channel generates feedback signals that can control the channel sequencer and/or the central sequencer. With parallel analyzer channels, the feedback is routed to the central sequencer to allow a common response of all parallel channels. With a single receive channel, the channel sequencer itself handles the feedback signals.

Pattern generation

The data stream is composed of segments. A segment can be made up of a memory-based pattern, memory-based PRBS or hardware generated PRBS. A total of 64 Mbit (at segment length resolution 512 bits) are available for memory-based pattern and PRBS.

Memory-based PRBS is limited to 2^{15} - 1 or shorter. Memory-based PRBS allows special PRBS modes like zero substitution (also known as extended zero run) and variable mark ratio

A zero substitution pattern extends the longest zero series by a user selectable number of additional zeroes. The next bit following these zero series will be forced to 1. Mark ratio is the ratio of 1 s and 0 s in a PRBS stream, which is 1/2 in a normal PRBS. Variable mark ratio allows values of 1/8, 1/4, 1/2, 3/4 and 7/8.

Due to granularity reasons a PRBS has to be written to RAM several times, at a multiplexing factor of 512 the number of repetitions is also 512. That means that a 2^{15} - 1 PRBS uses up to 16 Mbit of the memory. Hardware-based PRBS can be a polynomial up to 2^{31} - 1. No memory is used for hardware-based pattern generation. Error insertion allows inserting single or multiple errors into a data stream. So instead of a 0 a 1 is generated and vice versa.

Table 11. N4872A pattern and sequencing

Patterns:	
Memory based	Up to 64 Mbit
PRBS/PRWS	2^n - 1, n = 7, 10, 11, 15, 23, 31
Mark density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n - 1, n = 7, 9, 10, 11, 15
Errored PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15
Extended ones or zeros	2^n - 1, n = 7, 9, 10, 11, 15
PRWS port width	1, 2 , 4, 8, 16

Table 12. Data rate range, segment length resolution, available memory for synchronization and fine delay operation

Data rate range, Mb/s	Segment length resolution	Maximum memory depth, bits
620 ... 1.350,000	32 bits	4,194,304
620 ... 2.700,000	64 bits	8,388,608
620 ... 5.400,000	128 bits	16,777,216
620 ... 10.800,000	256 bits	33,554,432
620 ... 13.500,000	512 bits	67,108,864

N4872A generator module

The N4872A generates differential or single-ended data and clock signals operating from 620 Mb/s up to 13.5 Gb/s. The output levels are able to drive high-speed devices with interfaces like LVDS, ECL, PECL, CML and low voltage CMOS. The nominal output impedance is 50 Ω typical. The delay control IN has a single-ended input with 50 Ω impedance. The input voltage allows modulation of a delay element up to 1 GHz (200 ps) within the generator's differential output.

The AUX IN has a single-ended input with a 50 Ω impedance. The AUX IN allows injecting gating signals.

An active (TTL high) signal at the auxiliary input forces (gates) the data to a logic zero.

Data OUT

Table 17. Parameters for N4872A ParBERT 13.5 Gb/s generator

Data output	1, differential or single ended, 2.4 mm(f)	(1)
Range of operation	620 Mb/s - 13.5 Gb/s	
Impedance	50 Ω typ.	
Output amplitude/resolution	0.1 Vpp – 1.8 Vpp / 5 mV	
Output voltage window	–2.00 to +3.00 V	
Short circuit current	72 mA max.	
External termination voltage	–2 V to +3 V	(2)
Data formats	Data: NRZ, DNRZ	
Addressable technologies	LVDS, CML PECL; ECL (terminated to 1.3 V/0 V/-2 V) low voltage CMOS	
Transition times (20% - 80%)	< 20 ps	(3)
Jitter	9 ps peak-peak typ.	(4)
Cross-point adjustment (Duty cycle distortion)	20%...80% typ.	

(1) In single-ended mode, the unused output must be terminated with 50 Ω to GND.
(2) For positive termination voltage or termination to GND, external termination voltage must be less than 3 V below VOH. For negative termination voltage, external termination voltage must be less than 2 V below VOH. External termination voltage must be less than 3 V above VOL.
(3) At ECL levels
(4) Clock out to data out

Clock OUT

Table 18. Parameters for N4872A ParBERT 13.5 Gb/s generator

Clock output	1, differential or single-ended, 2.4 mm(f)	(1)
Frequency	620 MHz - 13.5 GHz	
Impedance	50 Ω typ.	
Output amplitude/resolution	0.1 Vpp – 1.8 Vpp / 5 mV	
Output voltage window	–2.00 to +2.80 V	
Short circuit current	72 mA max.	
External termination voltage	–2 V to +3 V	(2)
Addressable technologies	LVDS, CML PECL; ECL (terminated to 1.3 V/0 V/-2 V) low voltage CMOS	
Transition times (10% - 90%)	< 25 ps	(3)
Jitter	1 ps RMS typ.	
SSB phase noise (10 GHz @ 10 kHz offset, 1 Hz bandwidth)	< –75dBc with clock module E4809A typ.	

(1) In single-ended mode, the unused output must be terminated with 50 Ω to GND.
(2) For positive termination voltage or termination to GND, external termination voltage must be less than 3 V below VOH. For negative termination voltage, external termination voltage must be less than 2 V below VOH. External termination voltage must be less than 3 V above VOL.
(3) At ECL levels

Delay control IN

Table 19. Parameters for N4872A ParBERT 13.5 Gb/s generator

Delay control input	Single-ended; DC-coupled; SMA(f)
Input voltage window	–250 mV ... +250 mV (DC-coupled)
Input impedance	50 Ω typ.
Data rate Delay range Modulation bandwidth	 –100 ps ... +100 ps DC ... 1 GHz @ < 10.5 Gb/s

AUX IN

Table 20. Parameters for N4872A ParBERT 13.5 Gb/s generator

Interface	DC coupled, 50 Ω nominal
Levels	TTL levels
Minimum pulse width	100 ns
Connector	SMA female

N4873A analyzer module

The analyzer features are:

- Acquire data from start
- Compare and acquire data around error
- Compare and count erroneous ones and zeros to calculate the bit error rate

Receive memory for acquired data is up to 64 Mbit deep, depending on segment length resolution. The stimulus portion of the channel generates expected data and mask data. Mask data is also available at the maximum segment resolution (32, 64, 128, 256, 512).

The analyzer is able to synchronize on a received data stream by means of a user selectable synchronization word. The sync. word has a length of 48 bits and is composed of zeros, ones and Xs ("don't cares"). The detect word must be unique within the data stream. Synchronization on a pure PRBS data-stream is done without a detect-word, instead by simply loading a number of the incoming bits into the internal PRBS generator. A pre-condition for this is that the polynomial of the received PRBS is known.

The input comparator has differential inputs with 50 Ω impedance. The sensitivity of 50 mV and the common mode range of the comparator allow the testing of all common differential high-speed devices. The user has the choice of using the differential input with or without a termination voltage or as single-ended input (with a termination voltage). The differential mode does not need a threshold voltage, whereas the single-ended mode does. But also in differential mode the user can select one of the two inputs and compare the signal to a threshold voltage.

Table 21. N4875A analyzer timing: all timing parameters are measured at ECL levels, terminated with 50 Ω to GND

Sampling rate	620 MHz to 13.5 GHz	
Sample delay	Can be specified as leading edge delay in fraction of bits in each channel	
Start delay range	0 to 100 ns	
Fine delay range	± 1 period (can be changed without stopping)	
Delay resolution	100 fs	
Delay accuracy	±10 ps ± 20 ppm relative to the zero-delay placement	(1)
Relative delay accuracy	±2 ps ± 2% typ.	(1)
Skew between modules of same type	20 ps after cable deskewing at customer levels and unchanged system frequency.	(1)

(1) 25 °C - 40 °C ambient temperature

Table 22. N4873A pattern and sequencing

Analyzer auto-synchronization	On PRBS or memory-based data Manual or automatic by: Bit synchronization(2) with or without automatic phase alignment Automatic delay alignment around a start sample delay (range: ± 10 ns) BER Threshold: 10^{-4} to 10^{-9}

(2) With PRBS data, analyzers can autosyncronize on incoming PRBS data bits. When using memory-based data, this data must contain a unique 48 bit detect Word at the beginning of the segment, and the generators must be on a separate system clock. Don't cares within detect word are possible. If several inputs synchronize, the delay diffference between terminals must be smaller than ±5 segment length resolution.

Table 23. Parameters for N4873A ParBERT 13.5 Gb/s analyzer

Number of channels	1, differential or single ended, 2.4 mm (f)
Range of operation	620 Mb/s - 13.5 Gb/s
Max input amplitude	2 Vpp
Input sensitivity	50 mVpp typical @ 10 Gb/s, PRBS 2^{31} - 1, and BER 10^{-12}
Input voltage range	–2V ... +3 (selectable 2V window)
Internal termination voltage (can be switched off)	-2.0 to +3.0 V (must be within selected 2 V window)
Threshold voltage range	–2.0 to + 3.0 V (must be within selected 2 V window)
Threshold resolution	1 mV
Minimum detectable pulse width	25 ps typ.
Phase margin (source: N4872A)	1 UI - 12 ps typ.
Impedance	50 Ω typ. (100 Ω differential, if termination voltage is switched off)

Clock data recovery

The analyzer module has integrated CDR capabilities, which allow the recovery of either clock or data. Before the CDR can lock onto the incoming data stream, the data rate must be defined within the user interface; common data rates are pre-defined. In CDR mode, phase alignment to the center of the eye is done automatically during synchronization. For correct operation, the CDR output must be connected to the clock input of the E4809A central clock module. In addition the generator clock source and the analyzer clock source must be independent.

AUX OUT

The AUX OUT provides data or recovered clock signals.

AUX IN

Gating functionality: if a high level is applied at AUX IN, comparison is disabled and internal counters are stopped. After resuming a low level at AUX IN, comparison is enabled and internal counters continue. The internal sequencing is not stopped.

ERROR OUT

Whenever one or more bit errors are detected, the error out signal is high for one segment resolution. A high period is always followed by a low period (RZ-format) in order to ensure trigger possibility on continuous errors.

Table 24. Parameters for N4873A ParBERT 13.5 Gb/s analyzer - clock data recovery

Common data rates		
	OC-192:	9.953 Gb/s
	10GbE:	10.3125 Gb/s
	Fiber channel:	10.51875 Gb/s
	G.709/G.975:	10.664 Gb/s/10.709 Gb/s
	S-ATA:	1.5/3.0/6.0 Gb/s
	PCI-Express:	2.5/5.0/8.0 Gb/ss
	OC-48:	2.488 Gbit/s
	10GbE (XAUI):	3.125 Gbit/s
	SAN:	3.187 Gbit/s
Frequency ranges		
	9.9 GHz ...10.90 GHz	
	4.23 GHz ... 6.4 GHz	
	2.115 GHz ... 3.2 GHz	
	1.058 GHz....1.6 GHz	(1)
The CDR works with specified PRBS patterns up to 2^{31} - 1, The CDR expects a DC balanced pattern, The CDR expects an average transition density of one transition for every second bit.		

(1) Available for hardware S/N DE43A00401 and software rev. 5.62 and above

Table 25. Parameters for N4873A 13.5 Gb/s analyzer - AUX OUT

Interface	AC Coupled, 50 Ω nominal
Amplitude	600 mV nominal
Output jitter (clock @ AUX OUT)	0.01 UI rms typical
Connector	SMA female

Technical specifications

All specifications describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications are valid from 10 to 40 °C ambient temperature after a 30 minute warm-up phase, with outputs and inputs terminated with 50 Ω to ground at ECL levels if not specified otherwise.

Table 26. Parameters for N4873A 13.5 Gb/s analyzer - AUX IN

Resolution	Segment resolution
TTL compatible	Internal 500 Ω termination to GND;
Threshold	@ 1.5 V
Connector	SMA female
Low (0...1 V)	Internal counters are enabled
High (2 V...4 V)	Internal counters are stopped
Open	Same as low

Table 27. Parameters for N4873A 13.5 Gb/s analyzer - ERROR OUT

Format	RZ; active high
Output high level	0 V ± 100 mV
Output low level	+1 V ± 100 mV
Connector	SMA female

Agilent N4874A ParBERT 7 Gb/s Generator
Agilent N4875A ParBERT 7 Gb/s Analyzer

Technical Specifications

General

The N4874A generator and N4875A analyzer modules are each one VXI slot wide and operate in a range from 620 Mb/s up to 7 Gb/s. The ParBERT 7 Gb/s modules require the E4809A 13.5 GHz central clock module. All specifications, if not otherwise stated, are valid at the end of the recommended N4910A cable set (24" matched pair 2.4 mm).

The N4874A generator module generates hardware-based PRBS up to 2^{31} - 1, PRWS and user-defined patterns and provides a memory depth of 64 Mbit. The N4875A can synchronize on a 48bit detect word, or on a pure PRBS pattern without detect word.

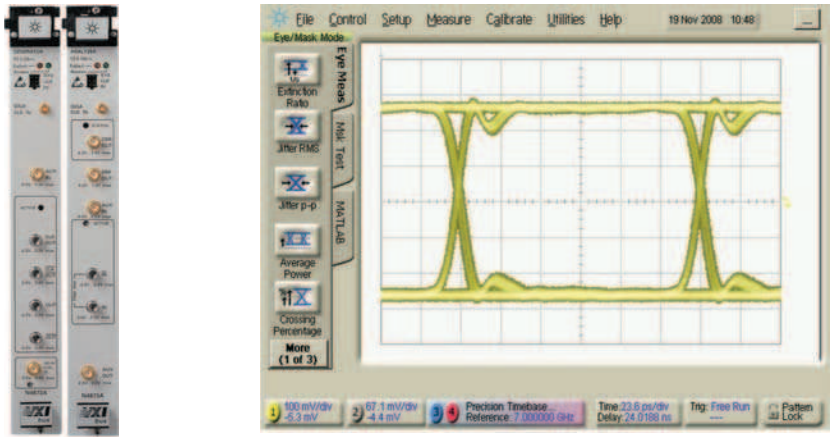

Figure 22. N4874A & N4875A and waveform

Timing specifications

The ParBERT 13.5 Gb/s modules are able to work with three different clock modes.

- *Internal clock mode:* The common clock mode is provided by the E4809A 13.5 GHz central clock module, which generates clock frequencies up to 13.5 GHz.
- *External clock mode:* The system also works synchronously with an external clock, which is connected to the E4809A clock module.
- *CDR mode:* To use the N4875A 7 Gb/s analyzer CDR capabilities, connect the analyzer's CDR out to the E4809A clock module's clock in.

Table 28. N4874A data generator timing specifications (@ 50% of amplitude, 50 ž to GND)

Frequency range	620 MHz to 7 GHz
Delay = start delay + fine delay	Can be specified as leading edge delay in fraction of bits in each channel
Start delay range	0 to 100 ns
Fine delay range	± 1 period (can be changed without stopping)
Delay resolution	100 fs
Delay accuracy	±10 ps ± 20 ppm relative to the zero-delay placement. (@ 25 °C - 40 °C ambient temp.)
Relative delay accuracy	±2 ps ± 2% typ. (@ 25 °C - 40 °C ambient temp.)
Skew between modules of same type	20 ps after cable deskewing at customer levels and unchanged system frequency. (@ 25 °C - 40 °C ambient temp.)

Sequencing

The sequencer receives instructions from the central sequencer and generates a sequence. The channel sequencer can generate a sequence with up to 60 segments.

An analyzer channel generates feedback signals that can control the channel sequencer and/or the central sequencer. With parallel analyzer channels, the feedback is routed to the central sequencer to allow a common response of all parallel channels. With single receive channel, the channel sequencer itself handles the feedback signals.

Pattern generation

The data stream is composed of segments. A segment can be made up of a memory-based pattern, memory-based PRBS or hardware generated PRBS. A total of 64 Mbit (at segment length resolution 512 bits) are available for memory-based pattern and PRBS.

Memory-based PRBS is limited to 2^{15} - 1 or shorter. Memory-based PRBS allows special PRBS modes like zero substitution (also known as extended zero run) and variable mark ratio.

A zero substitution pattern extends the longest zero series by a user selectable number of additional zeroes. The next bit following these zero series will be forced to 1. Mark ratio is the ratio of 1 s and 0 s in a PRBS stream, which is 1/2 in a normal PRBS. Variable mark ratio allows values of 1/8, 1/4, 1/2, 3/4 and 7/8.

Due to granularity reasons a PRBS has to be written to RAM several times, at a multiplexing factor of 512 the number of repetitions is also 512. That means that a 2^{15} - 1 PRBS uses up to 16 Mbit of the memory. Hardware-based PRBS can be a polynomial up to 2^{31} - 1. No memory is used for hardware-based pattern generation. Error insertion allows inserting single or multiple errors into a data stream. So instead of a 0 a 1 is generated and vice versa.

Table 29. N4874A pattern and sequencing

Segment length resolution	**512 bit**
Patterns:	
Memory based	up to 64 Mbit
PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15, 23, 31
Mark density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n - 1, n = 7, 9, 10, 11, 15
Errored PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15
Extended ones or zeros	2^n - 1, n = 7, 9, 10, 11, 15
Clock patterns	Divide or multiply by 1, 2, 4
PRWS port width	1, 2 , 4, 8, 16

Table 30. Data rate range, segment length resolution, available memory for synchronization and fine delay operation

Data rate range (Mbit/s)	Segment length resolution	Maximum memory depth (bits)
620 ... 1.350,000	32 bits	4,194,304
620 ... 2.700,000	64 bits	8,388,608
620 ... 5.400,000	128 bits	16,777.216
620 ... 7.000,000	256 bits	33,554.432
620 ... 7.000,000	512 bits	67,108.864

N4874A generator module

The N4874A generates differential or single-ended data and clock signals operating from 620 Mb/s up to 7 Gb/s. The output levels are able to drive high-speed devices with interfaces like LVDS, ECL, PECL, CML and low voltage CMOS. The nominal output impedance is 50 Ω typical. The delay control IN has a single-ended input with 50 Ω impedance. The input voltage allows modulation of a delay element up to 1 GHz (200 ps) within the generator's differential output.

The AUX IN has a single-ended input with a 50 Ω impedance. The AUX IN allows injecting gating signals. An active (TTL high) signal at the auxiliary input forces (gates) the data to a logic zero.

Data OUT

Table 31. Parameters for N4874A ParBERT 7 Gb/s generator

Data output	1, differential or single ended, 2.4 mm(f)	(1)
Range of operation	620 Mb/s - 7 Gb/s	
Impedance	50 Ω typ.	
Output amplitude/resolution	0.1 Vpp – 1.8 Vpp / 5 mV	
Output voltage window	–2.00 to +3.00 V	
Short circuit current	72 mA max.	
External termination voltage	–2 V to +3 V	(2)
Data formats	Data: NRZ, DNRZ	
Addressable technologies	LVDS, CML PECL - 3.3 V; ECL (terminated to 1.3 V/0 V/-2 V) low voltage CMOS, LVDS, CML	
Transition times (20% - 80%)	< 20 ps	(3)
Jitter	9 ps peak-peak typ.	(4)
Cross-point adjustment	20%...80% typ.	

(1) In single-ended mode, the unused output must be terminated with 50 Ω to GND.
(2) For positive termination voltage or termination to GND, external termination voltage must be less than 3 V below VOH. For negative termination voltage, external termination voltage must be less than 2 V below VOH. External termination voltage must be less than 3 V above VOL.
(3) At ECL levels.
(4) Clock out to data out.

Clock OUT

Table 32. Parameters for N4874A ParBERT 7 Gb/s generator

Clock output	1, differential or single-ended, 2.4 mm(f)	(5)
Frequency	620 MHz - 7 GHz	
Impedance	50 Ω typ.	
Output amplitude/resolution	0.1 Vpp – 1.8 Vpp / 5 mV	
Output voltage window	-2.00 to +2.80 V	
Short circuit current	72 mA max.	
External termination voltage	–2 V to +3 V	(6)
Addressable technologies	LVDS, CML PECL; ECL (terminated to 1.3V/0 V/-2 V) low voltage CMOS	
Transition times (10% - 90%)	< 25 ps	(7)
Jitter	1 ps RMS typ.	
SSB phase noise (10 GHz @ 10 kHz offset, 1 Hz bandwidth)	< - 75 dBc with clock module E4809A typ.	

(5) In single-ended mode, the unused output must be terminated with 50 Ω to GND.
(6) For positive termination voltage or termination to GND, external termination voltage must be less than 3 V below VOH. For negative termination voltage, external termination voltage must be less than 2 V below VOH. External termination voltage must be less than 3 V above VOL.
(7) At ECL levels.

Delay control IN

Table 33. Parameters for N4874A ParBERT 7 Gb/s generator

Delay control input	Single-ended; DC-coupled; SMA(f)
Input voltage window	–250 mV ... +250 mV (DC-coupled)
Input impedance	50 Ω typ.
Delay range	–100 ps ... +100 ps
Modulation bandwidth	DC ... 1 GHz @ data rate < 10.5 Gb/s

AUX IN

Table 34. Parameters for N4874A ParBERT 7 Gb/s generator

Interface	DC coupled, 50 Ω nominal
Levels	TTL levels
Minimum pulse width	100 ns
Connector	SMA female

N4875A analyzer module

The analyzer features are:

- Acquire data from start
- Compare and acquire data around error
- Compare and count erroneous ones and zeros to calculate the bit error rate

Receive memory for acquired data is up to 64 Mbit deep, depending on segment length resolution. The stimulus portion of the channel generates expected data and mask data. Mask data is also available at the maximum segment resolution (32, 64, 128, 256, 512).

The analyzer is able to synchronize on a received data stream by means of a user selectable synchronization word. The sync. word has a length of 48 bits and is composed of zeros, ones and Xs ("don't cares"). The detect word must be unique within the data stream. Synchronization on a pure PRBS data-stream is done without a detect-word, instead by simply loading a number of the incoming bits into the internal PRBS generator. A pre-condition for this is that the polynomial of the received PRBS is known.

The input comparator has differential inputs with 50 Ω impedance. The sensitivity of 50 mV and the common mode range of the comparator allow the testing of all common differential high-speed devices. The user has the choice of using the differential input with or without a termination voltage or as single-ended input (with a termination voltage). The differential mode does not need a threshold voltage, whereas the single-ended mode does. But also in differential mode the user can select one of the two inputs and compare the signal to a threshold voltage.

Table 35. N4875A analyzer timing: all timing parameters are measured at ECL levels, terminated with 50 Ω to GND

Sampling rate	620 MHz to 7 GHz	
Sample delay	Can be specified as leading edge delay in fraction of bits in each channel	
Start delay range	0 to 100 ns	
Fine delay range	± 1 period (can be changed without stopping)	
Delay resolution	100 fs	
Delay accuracy	±10 ps ± 20 ppm relative to the zero-delay placement	(1)
Relative delay accuracy	±2 ps ± 2% typ.	(1)
Skew between modules of same type	20 ps after cable deskewing at customer levels and unchanged system frequency.	(1)

(1) 25 °C - 40 °C ambient temperature

Table 36. N4875A pattern and sequencing

Analyzer auto-synchronization	On PRBS or memory-based data Manual or automatic by: Bit synchronization(2) with or without automatic phase alignment Automatic delay alignment around a start sample delay (range: ± 10 ns) BER Threshold: 10^{-4} to 10^{-9}

(2) With PRBS data, analyzers can autosyncronize on incoming PRBS data bits. When using memory-based data, this data must contain a unique 48 bit detect Word at the beginning of the segment, and the generators must be on a separate system clock. Don't cares within detect word are possible. If several inputs synchronize, the delay diffference between terminals must be smaller than ±5 segment length resolution.

Data IN

Table 37. Parameters for N4875A ParBERT 7 Gb/s analyzer

Number of channels	1, differential or single ended, 2.4 mm (f)
Range of operation	620 Mb/s - 7 Gb/s
Max input amplitude	2 Vpp
Input sensitivity	50 mVpp typical @ 7 Gb/s, PRBS 2^{31} - 1, and BER 10^{-12}
Input voltage range	–2V ... +3 (selectable 2V window)
Internal termination voltage (can be switched off)	–2.0 to +3.0 V (must be within selected 2 V window)
Threshold voltage range	–2.0 to + 3.0 V (must be within selected 2 V window)
Threshold resolution	1 mV
Minimum detectable pulse width	25 ps typ.
Phase margin (source: N4874A)	1 UI - 12 ps typ.
Impedance	50 Ω typ. (100 Ω differential, if termination voltage is switched off)
Sampling delay resolution	100 fs

Table 38. Parameters for N4875A ParBERT 7 Gb/s analyzer - clock data recovery

Common data rates		
	S-ATA:	1.5/3.0/6.0 Gb/s
	PCI-Express:	2.5/5.0 Gb/s
	OC-48:	2.488 Gbit/s
	10GbE:	3.125 Gbit/s
	SAN:	3.187 Gbit/s
Frequency ranges		
	4.23 GHz ... 6.4 GHz	
	2.115 GHz ... 3.2 GHz	
	1.058 GHz....1.6 GHz	(1)
The CDR works with specified PRBS patterns up to 2^{31} - 1, The CDR expects a DC balanced pattern, The CDR expects an average transition density of one transition for every second bit.		

(1) Available for hardware S/N: DE43A00401 and software rev. 5.62

Clock data recovery

The analyzer module has integrated CDR capabilities, which allow the recovery of either clock or data. Before the CDR can lock onto the incoming data stream, the data rate must be defined within the user interface; common data rates are pre-defined. In CDR mode, phase alignment to the center of the eye is done automatically during synchronization. For correct operation, the CDR output must be connected to the clock input of the E4809A central clock module. In addition the generator clock source and the analyzer clock source must be independent.

AUX OUT

The AUX OUT provides data or recovered clock signals.

AUX IN

Gating functionality: if a high level is applied at AUX IN, comparison is disabled and internal counters are stopped. After resuming a low level at AUX IN, comparison is enabled and internal counters continue. The internal sequencing is not stopped.

ERROR OUT

Whenever one or more bit errors are detected, the error out signal is high for one segment resolution. A high period is always followed by a low period (RZ-format) in order to ensure trigger possibility on continuous errors.

Table 39. Parameters for N4875A 7 Gb/s analyzer - AUX OUT

Interface	AC Coupled, 50 Ω nominal
Amplitude	600 mV nominal
Output jitter (clock @ AUX OUT)	0.01 UI rms typical
Connector	SMA female

Table 40. Upgrades 7 Gb/s - 13 Gb/s

Module number	Upgrade to 13.5 Gb/s
E4874A	Available on request
E4875A	Available on request

Table 41. Parameters for N4875A 13.5 Gb/s analyzer - AUX IN

Resolution	Segment resolution
TTL compatible	Internal 500 Ω termination to GND
Threshold	@ 1.5 V
Connector	SMA female
Low (0...1 V)	Internal counters are enabled
High (2 V...4 V)	Internal counters are stopped
Open	Same as low

Table 42. Parameters for N4875A 13.5 Gb/s analyzer - ERROR OUT

Format	RZ; active high
Output high level	0 V ± 100 mV
Output low level	+1 V ± 100 mV
Connector	SMA female

Technical specifications

All specifications describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications are valid from 10 to 40 °C ambient temperature after a 30 minute warm-up phase, with outputs and inputs terminated with 50 Ω to ground at ECL levels if not specified otherwise.

Agilent E4861B ParBERT 3.35 Gb/s Data Module
Agilent E4862B ParBERT 3.35 Gb/s Generator Front-End
Agilent E4863B ParBERT 3.35 Gb/s Analyzer Front-End

Technical Specifications

General

A ParBERT 3.35 Gb/s module can house up to two front-ends, either two generators or analyzers or any mix. ParBERT 3.35 Gb/s modules work with the E4808A or E4890A clock modules. The key specifications of ParBERT 3.35 Gb/s modules are:

- 21 MHz ... 3.350 GHz clock/data rate
- 16 Mbit memory depth at each channel
- HW-based PRBS generation up to the polynomial of $2^{31}-1$
- Analyzer can synchronize on a 48 bit detect word (memory-based data)
- Analyzer can synchronize on a pure PRBS pattern without detect word

Timing capabilities

The frequency range of the modules is 21 MHz ... 3.350 GHz. The ParBERT 3.35 Gb/s front-ends use a multiplying PLL that multiplies system master clock by 4 or 8. Through the clock module, an external clock source can be used. This external clock must run continuously. If the clock signal is interrupted, the multiplying PLLs typically needs 100 milliseconds to lock onto the clock again.

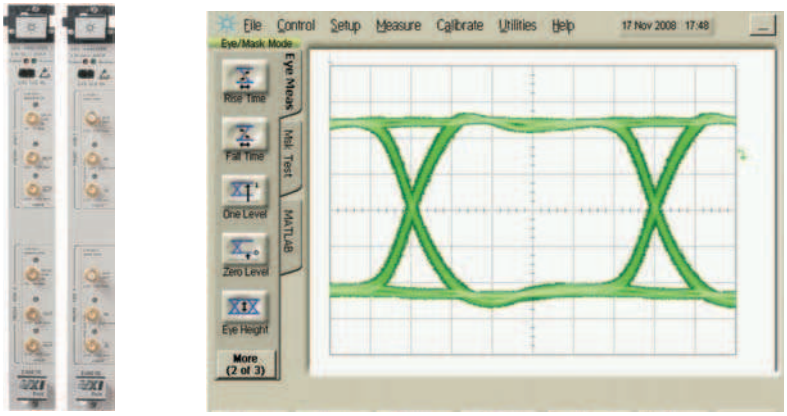

Figure 23. E4861B and E4862B with waveform of E4861B generator

Table 43. E4861B data generator timing specification (@ 50% of amplitude, 50 Ω to GND)

Frequency range	20.834 MHz to 3.350 GHz
Delay = start delay + fine delay	Can be specified as leading edge delay in fraction of bits in each channel
Start delay range	0 to 200 ns (not limited by period)
Fine delay range	±1 period (can be changed without stopping)
Delay resolution	1 ps
Accuracy data mode	±25 ps ±50 ppm relative to the zero-delay and temperature change within ±10 °C after autocalibration
Clock mode	±50 ps ±50 ppm relative to the zero-delay
Skew between modules of same type (data mode)	50 ps typ. after deskewing at customer levels and unchanged system frequency

The variable delay is available in data mode and pulse mode. In clock mode the timing is fixed.

Sequencing

The sequencer receives instructions from the clock module. The channel sequencer can generate a sequence with up to 60 segments. An analyzer channel can generate feedback signals which are combined in the clock module for a common response of all parallel channels. With a single receiver channel the channel sequencer itself handles the feedback signals.

Table 44. E4861B analyzer timing all timing parameters are measured at ECL levels, terminated with 50 Ω to GND

Sampling rate	20.834 MHz to 3.350 GHz
Sample delay	Same as delay = start delay + fine delay
	Can be specified as leading edge delay in fraction of bits in each channel
Start delay range	0 to 200 ns (not limited by period)
Fine delay range	±1 period (can be changed without stopping)
Resolution	1 ps
Accuracy	±25 ps ±50 ppm relative to the zero-delay and temperature change within ±10 °C after autocalibration
Skew	50 ps typ. after deskewing at customer levels and unchanged system frequency

Table 45. E4861B pattern and sequencing

Patterns	
Memory based	Up to 16 Mbit
PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15, 23, 31
Mark density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n - 1, n = 7, 9, 10, 11, 15
Errored PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15
Extended ones or zeros	2^n - 1, n = 7, 9, 10, 11, 15
Clock patterns	Divide or multiply by 1, 2, 4
Analyzer auto-synchronization	On PRBS or memory-based data Manual or automatic by: Bit synchronization(1) with or without automatic phase alignment. Automatic delay alignment around a start sample delay (range: ± 10 ns) BER threshold: 10^{-4} to 10^{-9}

(1) With PRBS data, analyzers can autosyncronize on incoming PRBS data bits. When using memory-based data, this data must contain a unique 48 bit detect word at the beginning of the segment, and the generators must be on a separate system clock. “Don’t cares” within detect word are possible. If several inputs synchromize, the delay diffference between terminals must be smaller than ±5 segment length resolution.

Table 46. Data rate range, segment length resolution, available memory for synchronization and fine delay operation

Data rate range Mb/s	Segment length	Maximum memory resolution depth, bits
20.834 ... 41.666	1 bit	131,072
20.834 ... 82.333	2 bits	262,144
20.834 ... 166.666	4 bits	524,288
20.834 ... 333.333	8 bits	1,048,576
20.834 ... 666.666	16 bits	2,097,152
20.834 ... 1,333.333	32 bits	4,194,304
20.834 ... 2,700.000	64 bits	8,388,608
20.834 ... 3,350.000	128 bits	16,777,216

Table 47. Dependancy of PRWS generation and port width.

Almost all the combinations are possible except the following:	
PRWS	Port width
2^7 - 1	No restriction
2^9- 1	7
2^{10}- 1	3, 11, 31, 33
2^{11}- 1	23
2^{15}- 1	7, 31
2^{23}- 1	47
2^{31}- 1	No restriction

Pattern generation

The data stream is composed of segments. A segment can be a memory-based pattern, memory-based PRBS or hardware generated PRBS. A total of 16 Mbit (at segment length resolution 128 bits) are available for memory-based pattern and PRBS.

Memory-based PRBS is limited to 2^{15}- 1 or shorter. Memory-based PRBS allows special PRBS modes like zero substitution (also known as extended zero run) and variable mark ratio. A zero substitution pattern extends the longest zero series by a user-selectable number of additional zeros. The next bit following these zero-series will be forced to 1. Mark ratio is the ratio of ones and zeros in a PRBS stream, which is 1/2 in a normal PRBS. Variable mark ratio allows values of 1/8, 1/4, 1/2, 3/4, 7/8. Due to granularity reasons a PRBS has to be written to RAM several times, at a multiplexing factor of 128 the number of repetitions is also 128. That means that a 2^{15}- 1 PRBS uses up to 4 Mbit of the memory. Hardware-based PRBS can be any polynomial up to 2^{31}- 1. No memory is used, so the total memory is free for memory-based pattern generation. Error insertion allows inserting single or multiple errors into a data stream. So instead of a ‘0’ a ‘1’ is generated and vice versa. Single errors can be inserted by pod or via instruction from the central sequencer. The user can trigger an error with a signal supplied to the qualifier pod of the central module. An error insertion with a fixed rate and a fixed distribution is supported. The user software allows the selection of errored and error-free segments.

Generator front end (E4862B)

The amplifier generates a differential output signal. Each output can be individually switched on and off. The output levels are sufficient to drive typical high-speed devices with interfaces like ECL, PECL, LVDS and DVI levels. The nominal output impedance is 50 Ω. The delay control has a single-ended input with 50 Ω impedance. The input voltage modulates a delay element within the generator's differential output. The user has the option of turning the delay control in feature on or off. Additionally the user can select between two delay ranges.

Table 48. Parameters for generator front-ends E4862B 3.35 Gb/s

Outputs	1, differential or single-ended	
Impedance	50 Ω typ.	
Data formats	Data: NRZ, DNRZ, RZ, R1	
Pulse mode Range Sampling delay resolution Width accuracy	 150 ps to (1UI - 150 ps) 1 ps 40 ps typ.	
Output voltage window	–2.00 to +3.5 V	(1)
Ext. term. voltage	–2.00 to +3.5 V	(2)
Absolute maximum external voltage	–2.2 V to +3.2 V	
Addressable technologies	LVDS, CML, PECL, ECL low voltage CMOS	
Amplitude/resolution	0.05 Vpp ... 1.8 Vpp/10 mV	
Accuracy hi level/amplitude	±2% ±10 mV	
Short circuit current	72 mA max.	
Transition times (20% - 80%)	< 75 ps; 60 ps typ.	
Overshoot/ringing	5% +10 mV typ.	
Jitter, NRZ data mode Clock mode Pulse, RZ, R1 mode	< 30 ps peak-peak < 2 ps rms 30ps peak-peak typ.	(3) (3 & 4) (3 & 4)
Cross-point adjustment (Duty cycle distortion)	30% ... 70% (in NRZ mode only)	

(1) For output voltages > 3 V the termination voltage ≥ 3 V needs to be applied.
(2) External termination voltage must be less than 3 V below VOH. and less than 3 V above VOL. Termination into AC is possible.
(3) Measured with E4808A clock module.
(4) Specified as intra channel jitter.

Table 49. Delay control in

Input voltage window	–500 mV to +500 mV (DC-coupled)
Delay range 1	–250 ps to +250 ps
Delay range 2	–25 ps to +25 ps
Modulation bandwidth	DC to 200 MHz
Input impedance	50 Ω (typ.)

Typical waveform pictures

Eye Plots

The 3.35 Gb/s generator output is designed for clean and fast output signals. It offers a swing of 50 mV to 1.8 V within the voltage window suited for testing LVDS, CML, (P)ECL and SSTL 0 - 3.3 V technologies.

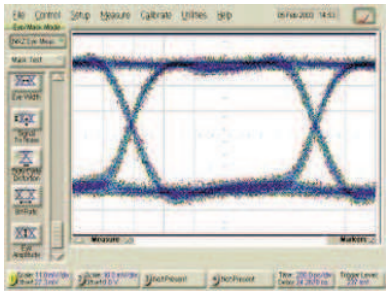

Figure 24a. 3.35 Gb/s Generator: 50 mVpp

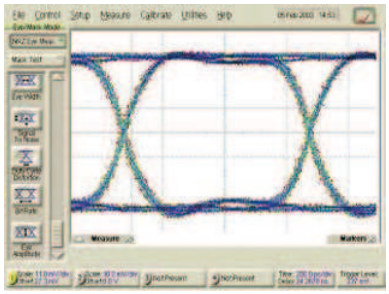

Figure 24b. 3.35 Gb/s Generator: 1.8 V pp

Crossing Point

The 3.35 Gb/s generator allows a variable cross-over for differential signals. The cross-over can be programmed by the user interface or remote program between 30 and 70%.

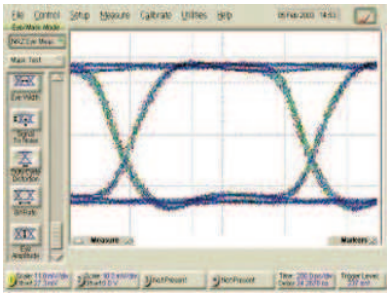

Figure 24c. 3.35 Gb/s Generator @30%

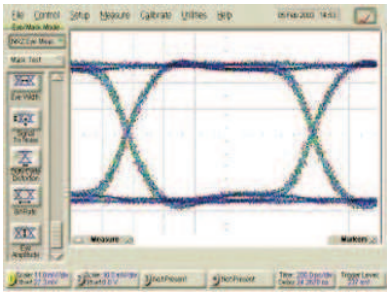

Figure 24d. 3.35 Gb/s Generator @50%

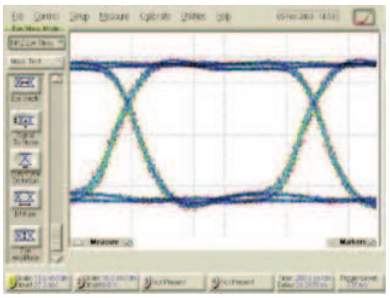

Figure 24e. 3.35 Gb/s Generator @70%

Jitter Modulation Examples

A Receiver's jitter tolerance can be tested applying a voltage at the external delay control input and by this generating jittered output signals as depicted in figure 26 a-d.

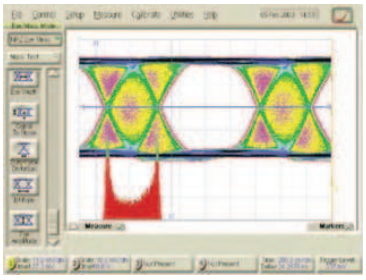

Figure 25a. Jitter modulated with sine wave

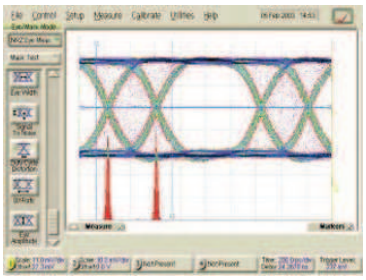

Figure 25b. Jitter modulated with rectangle wave

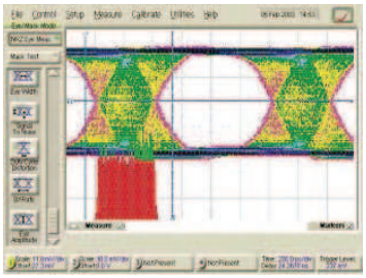

Figure 25c. Jitter modulated with triangle wave

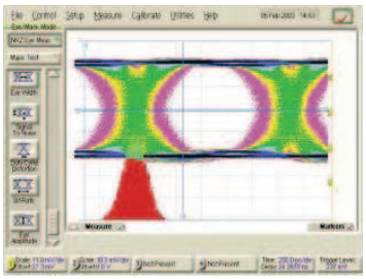

Figure 25d. Jitter modulated with noise generator

Analyzer front end (E4863B)

The analyzer features are:

- Acquire data from start
- Compare and acquire data around error
- Compare and count erro neous ones and zeros to calculate the bit error rate

The receive memory for acquired data is up to 16 Mbit deep, depending on the segment length resolution. The stimulus portion of the channel generates expected data and mask data. Mask data is also available at the maximum granularity.

The analyzer is able to synchronize on a received data stream by means of a user-defined detect word. The detect word is defined by the first bits within the expected segment, it has a length of 48 bits and is composed of zeros, ones and Xs (“don’t cares”). The detect word must be unique within the data stream. Synchronization on a pure-PRBS data-stream is done without a detect-word, by simply loading a number of the incoming bits into the internal PRBS generator. A pre-condition for this is that the polynomial of the received PRBS is known.

The input comparator has differential inputs with 50 Ω impedance. The sensitivity is down to 50 mV and the common mode range of the comparator allows the testing of all common differential high-speed devices.The user has the option of using the differential input with or without a termination voltage or as single-ended input (with a termination voltage). The differential mode does not need a threshold voltage, whereas the single-ended mode does. But also in differential mode the user can select one of the two inputs and compare the signal to a threshold voltage.

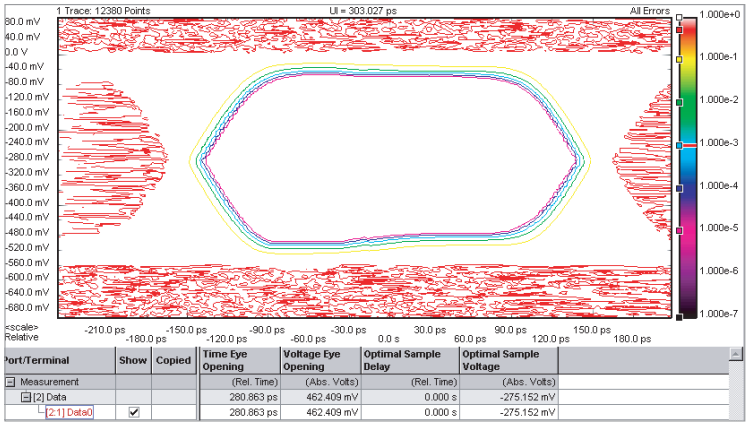

Figure 26. Eye diagram of E4863B analyzer

Table 50. Parameters for analyzer front-ends E4863B 3.35 Gb/s

Number of channels	1, differential or single-ended	
Impedance	50 Ω typ. (100 Ω differential if termination voltage is switched off)	
Internal termination voltage (can be switched off)	-2.0 to +3.0 V	
Threshold voltage range	-2.0 to +3.0 V	
Threshold resolution	1 mV	
Threshold accuracy	±20 mV ±1%	
Input sensitivity (single-ended and differential)	< 50 mV	
Minimum detectable pulse width	< 150 ps	
Maximum input voltage range	Three ranges selectable: -2 V to +1 V -1 V to +2 V 0 V to 3 V	
Maximum differential voltage	1.8 V	
Phase margin with ideal input signal	> 1 UI - 30 ps	(1)
Phase margin with E4862B generator	> 1 UI - 50 ps	(1)
Auxilary out	V out: 350 mV pp typ., AC coupled	(2)
Sampling delay resolution	1 ps	

(1) Measured with E4808A central module

(2) Terminate with 50 Ω to GND, if not used

Protection

Input and output relays switch off automatically, if the absolute maximum voltage window is exceeded.

Agilent E4832A ParBERT 675 Mb/s Data Module
Agilent E4838A ParBERT 675 Mb/s Generator Front-End
Agilent E4835A ParBERT 675 Mb/s Analyzer Front-End

Technical Specifications

E4832A 675 Mb/s generator/analyzer module

This module holds any combination of up to two analyzer front-end pairs (E4835A) and four generator front-ends (E4838A).

Clock module/data mode

The generator can operate in clock mode or data mode. Clock mode is achieved when the generator is assigned as a pulse port. Data mode is achieved with assigning it to a data port. In clock mode it is a fixed duty cycle of 50%. In data mode it is NRZ format with variable delay. The analyzer only works as a data port whenever used with variable sampling delay. The sampling delay consists of two elements: the start delay and the fine delay. The fine delay can be varied within ±1 period without stopping.

Data capabilities

PRBS/PRWS and memory-based data are defined by segments. Segments are assigned to a generator, and for stimulating a pattern. On an analyzer, it defines the expected pattern which the incoming data are compared to. The expected pattern can contain mask bits.

The segment length resolution is the resolution to which the length of a pattern segment can be set. The maximum memory per channel of the E4832A can be set in steps of 16 bits up to a length of 2048 Kbit. If the 16-bit segment length resolution is too coarse, memory depth and frequency can be traded.

Sub-frequencies

For applications requiring different frequencies at a fraction of the system clock, the ratio can be divided or multiplied by 2, 4, 8, or 16. This influences the dependency between segment length resolution and maximum memory depth.

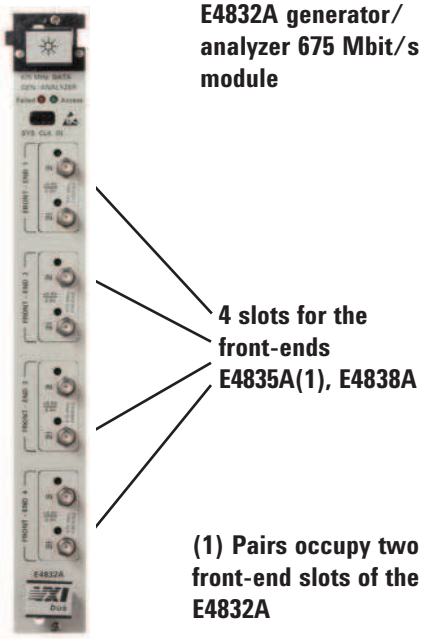

Figure 27. E4832A module

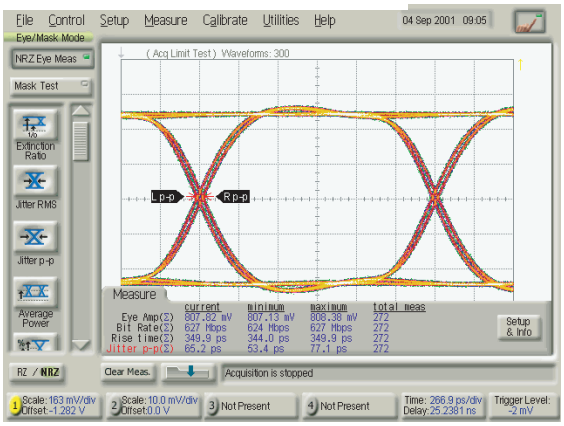

Fig 28. Wave diagram of E4832A generator

Synchronization

Synchronization is the method of automatically adjusting the proper bit phase for data comparison on the incoming bit stream. The sychronization can be performed on PRBS/PRWS and memory-based data but it is not possible on a mix of PRxs and memory based data.

There are two types of synchronization:

- Bit synchronization
- Auto delay alignment

Bit synchronization is possible to cover a bit alignment for a totally unknown number of cycles. Using memory-based data, the first 48 bits within the expected data segment will work as a detect word which the incoming data are compared to. When the incoming data match with this detect word, analysis will begin.

Auto delay alignment is performed by using the analyzer sampling delay. The sampling delay range is ±50 ns while this is possible.

Using auto delay alignment provides synchronization with an absolute timing relation between a group of analyzer channels. This makes skew measurements are possible.

Table 51. E4832A data generator timing specifications (@ 50% of amplitude, 50 Ω to GND and fastest transition times)

Frequency range	333,334 kHz to 675 MHz
Delay range	0 to 3.0 µs (not limited by period)
Sampling delay resolution	2 ps
Accuracy	±50 ps ±50 ppm relative to the zero-delay placement (1)
Skew	50 ps typ. after deskewing at customer levels
Pulse width	Can be specified as width or % of duty cycle
Range	750 ps to (period -750 ps)
Resolution	2 ps
Accuracy	±200 ps ±0.1%
Duty cycle	1% to 99%, subject to width limits

(1) Valid at 15 to 35 °C room temperature

Table 52. E4832A analyzer timing; all timing parameters are measured at ECL levels terminated with 50 Ω to GND

Sample delay = start delay + fine delay	
Fine delay can be changed without stopping (2)	
Sampling rate (3)	333,334 Kb/s to 675 Mb/s
Sampling delay	(= start delay + fine delay)
range	0 to 3.0 µs (not limited by period)
Fine delay range	±1 period
Accuracy	±50 ps ±50 ppm relative to the zero-delay placement (3)
Resolution	2 ps
Skew	50 ps typ. after deskewing at customer levels

(2) Conditions: frequency > 20.8 MHz and by using the finest segment length resolution.
(3) See tables for front-end deratings

Table 53. Pattern and sequencing features of E4832A

Patterns:	
Memory based	Up to 2 Mbit
PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15, 23, 31
Mark density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n - 1, n = 7, 9, 10, 11, 15
Errored PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15
Extended ones or zeros	2^n - 1, n = 7, 9, 10, 11, 15
Clock patterns	Divide or multiply by 1, 2, 4
User patterns	Data editor, file import
Analyzer auto-synchronization (2):	On PRBS or memory-based data manual or automatic by: Bit synchronization (1) with or without automatic phase alignment Automatic delay alignment around start sample delay (range: ±50 ns) BER threshold: 10^{-4} to 10^{-9}

(1) Bit synchronization on data is achieved by detecting a 48 bit unique word at the beginning of the segment. "Don't cares" within the detect word are possible. In this mode no memory-based data can be sent within the same system. If several inputs synchronize, the delay difference between the terminals must be ±5 segment length resolution.
(2) Condition: frequency > 20.8 MHz and by using the finest segment length resolution.

Table 54. Data rate range, segment length resolution, available memory for synchronization and fine delay operation

Data rate range Mb/s	Segment length	Maximum memory resolution depth, bits
20.834 ... 41.666	1 bit	131,008
41.667 ... 83.333	2 bits	262,016
83.334 ... 166.666	4 bits	524,032
166.667 ... 333.333	8 bits	1,048,064
333.334 ... 666.667	16 bits	2,097,152

In general, it is possible to set higher values for the segment length resolution and also at lower frequencies than are indicated in the table. In this case the fine delay function and the auto-synchronization function are unavailable.

Table 55. between the capability of generating PRWS and port width, almost all the combinations are possible except the following:

PRWS	Port width
2^7 - 1	No restriction
2^9 - 1	7
2^{10} - 1	3, 11, 31, 33
2^{11} - 1	23
2^{15} - 1	7, 31
2^{23} - 1	47
2^{31} - 1	No restriction

Addressable technologies
LVDS, (P)ECL, TTL, 3.3 V CMOS
Analyzer input

The analyzer channel can be operated:

- Single-ended normal
- Single-ended compliment
- Differential

For termination there is always 50 Ω connected to a programmable termination voltage. In differential mode there is an additional, selectable 100 Ω differential termination. Independent of the selected termination, there is the choice of whether the anaylsis of the incoming signal is performed on the input or true differential.

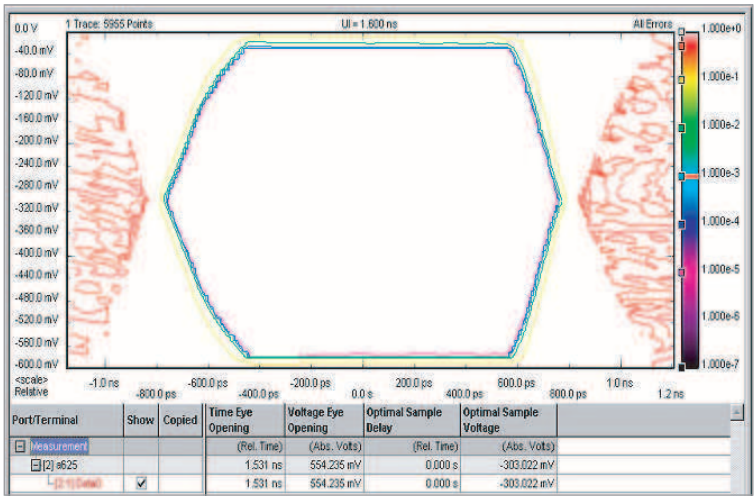

Figure 29. Eye diagram of E4835A analyzer

Table 56. Level parameters for differential generator front-end E4838A 675 Mb/s

Number of channels	1, differential
Impedance	50 Ω typ.
Data formats	RZ, R1, NRZ, DNRZ
Output voltage window	–2.2 to +4.4 V (doubles into open up to max. 5 Vpp)
Amplitude/resolution	0.1 V to 3.50 V / 10 mV
Level accuracy	±3% ± 25 mV typ. after 5 ns settling time
@ LVDS/(P)ECL	±1% ±25 mV typ. after 5 ns settling time
Variable transition time range (10 - 90% of amplitude)	0.5 to 4.5 ns
Accuracy	±5% ±100 ps
@ LVDS/(P)ECL (20 - 80% of amplitude)	0.35 ns typ
Overshoot/ringing	< 7% (< 5% typ).
Jitter Data mode Clock mode	 < 100 ps peak to peak (80 ps typ) 8 ps rms typ.
Channel addition	XOR and analog

Table 57. Two differential analyzer front-ends E4835A (1), 667 MSa/s

Number of channels	2, differential or single-ended (switchable)
Impedance	50 Ω typ. 100 Ω differential if termination voltage is switched off
Termination voltage (can be switched off)	–2.0 to +3.0 V
Threshold voltage range/ threshold accuracy	–2.00 to +4.50 V/±1% ±20 mV
Threshold resolution	2 mV
Input sensitivity	Differential 50 mV typ Single-ended 100 mV typ
Minimum detectable pulsewidth	400 ps typ. at ECL levels
Input voltage range	Two ranges selectable: 0 to +5 V and -2 to +3 V
Phase margin with ideal input signal with E4838A generator	> 1 UI - 100 ps > 1 UI - 180 ps

(1) Occupy two front-end slots of the E4832A. The E4835A contains two front-ends (E4835AZ) and one common data back end. In this document one front-end is referred to as E4835A.

Agilent E4809A 13.5 GHz Central Clock Module
Agilent E4808A High Performance Central Clock Module
Agilent E4805B 675 MHz Central Clock Module

Technical Specifications

Each ParBERT 81250 system consists of at least one clock module, which generates the system clock for at least one generator or analyzer or any mix. Please see the table to the right for a complete compatibility overview.

Sequencing
The sequencing can be used to specify the data flow:

- Single
- Looped
- Infinite loop
- Event handling (branch)
- Synchronization

Event handling
With event handling, the flow of data generation and analysis can be controlled with external signals at run time.

Usage of events

- Start and stop of data
- Match loop
- Integration with other equipment (ATE)
- Trigger on error

Table 58.

Modules/central clock	E4805B	E4808A	E4809A
E4832A - ParBERT 675 Mb/s	●	●	●
E4861A - ParBERT 2.7/1.6 Gb/s	●	●	
E4861B - ParBERT 3.35 Gb/s		●	●
E4810A/11A - ParBERT 3.3.5 Gb/s optical (1)		●	
E4866A/67A - ParBERT 10.8 Gb/s (1)		●	
N4872A/73A - ParBERT 13.5 Gb/s			●
E4868B/69B - ParBERT 45 Gb/s (1)		●	
E4874A/75A - ParBERT 7 Gb/s			●

(1) Modules discontinued.

Table 59. E4809A, E4808A and E4805B sequencing features

Number of segms ents	1 to 30 (every segment looped once) 1 to 60 (no segment looped)
Looping levels	Up to 4 nested loops plus one optional infinite loop Loops can be set independently from 1 to 2^{20} repetitions
Start/stop	External input, manual, programmed (stop with E4832A only)
Event handling	React on internal and external events.

Table 60. E4809A, E4808A and E4805B event handling

Event trigger sources
Events can be defined as any combination of the following sources. A maximum of 10 events can be defined.
○ 8-line trigger input pod for TTL signals
○ VXI trigger lines TO and T1
○ Any capture error/or no error detected by one of the analyzer channels
○ Software command control: an event trigger command issued locally or remotely
Reactions to an event can be set per data segment immediately or deferred and can be any combination of:
○ Data segment jump
○ Launch trigger pulse at trigger output of the clock module
○ VXI trigger lines TO and T1 can be set to 01, 10, or 11

Master slave, multi-mainframe, different clock groups

Up to 3 clock modules can be combined to run in one clock grouping by connecting the master slave cable. This is used to combine channels which do not fit into one frame into one clock group. Omitting the master-slave connection will run the channels as separate clock groups. A system can be a combination of multiple clock groups made up of multiple channels. The frequencies used can be totally asynchronous or m/n ratio (see clock input multiplier/divider). For separated clock groups the master slave is not used. Within one master-slave system the modules must be the same type.

Table 61. E4809A, E4808A and E4805B trigger pod characteristics

Input lines	8, single-ended	
Input levels	TTL compatible	
Input threshold	1.5 V	
Input termination	5 kΩ pullup to +5 V	
Absolute max ratings for input voltages	–1.2 V to + 7.0 V	
Cable delay	11 ns typical	
sampling clock frequency	system frequency/segment length resolution	
	TRIGGER OUTPUT	CLOCK/REF INPUT
Setup time (1)	2.5 ns	–12.5 ns
Hold time (1)	5 ns	20 ns

(1) Includes the cable delay

Table 62. E4809A clock module specifications

Frequency range	20.834 MHz...13,5 GHz	
Resolution	1 Hz	
SSB phase noise (at 10 kHz offset)	< -75 dBc at 10 GHz	
Latency external start input		
• Start IN to Trig OUT with 7/13.5 Gb/s	16 ns + (2 * system clock * segment resolution) ± 1 clock	(1)
• Start IN to Data OUT with 7/13.5 Gb/s	416 ns + (2 * system clock * segment resolution) ± 1 clock	(1)
• IN to Trig OUT without 7/13.5 Gb/s	16 ns ± 1 clock	(1)
• IN to Data OUT without 7/13.5 Gb/s	48 ns ± 1 clock	**(1)**

(1) Add 3 ns if expander frame is used

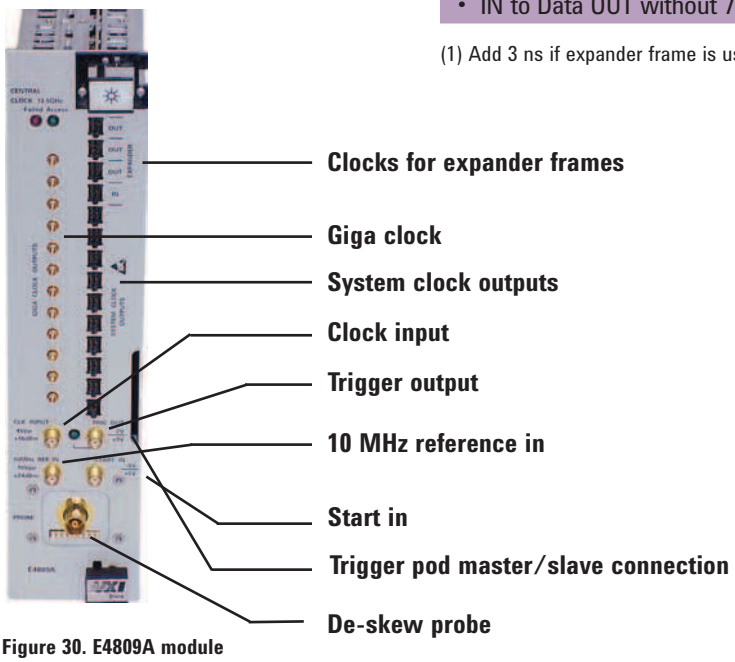

Figure 30. E4809A module

E4809A 13.5 GHz central clock module

General

E4809A is a 2-slot central clock module with 13GHz clock distribution. ParBERT 81250 13.5 Gb/s modules are designed to run with the E4809A 13.5 GHz central clock module.

Timing capabilities

The E4809A supports three different operation modes.

E4809A as system clock
The E4809A distributes clock signals to connected modules in the range from 20.834 MHz up to 13.5 GHz. The E4809A provides Giga-clock signals in a range from 500 MHz up to 13.5 GHz to the ParBERT 81250 13.5 Gb/s modules (N4872A, N4873A). All other supported modules work using the E4809A master clock.

External clock mode
The system will run synchronously to an external clock, which is connected to the clock module's clock input. There are two different sub-modes available. In the **direct** clock mode, the PLL (phase locked loop) is bypassed and an external clock signal can be distributed to all Giga-clock connected modules. This direct external clock mode operates in a range from 500 MHz to 13.5 GHz. In this mode the external clock may be FM or PM modulated. In the **indirect** external clock mode, the clock modules' internal PLL is used to generate flexible master clock and Giga-clock signals.

Clock data recovery (CDR) mode
If the CDR is used, the CDR out of the analyzer must be connected to the clock input of the clock module.

Start input

A sequence of generated data can be started by an external signal.

Table 63. Start input

Start input	DC coupled; 3.5 mm (f)
Threshold range	–1.40 V to +3,70 V
Zin/termination voltage	50 Ω typ./-2 V to +3 V
Sensitivity/max. levels	200 mVpp / -3 V...+6 V

Reference input

The reference input allows ParBERT to run synchronously with an external 10 MHz clock. A continuous clock is necessary. A burst clock can not be used as an external clock.

TTable 64. Reference input

Reference input	AC coupled; 3.5 mm(f)
Frequency	10 MHz
Input transition time	< 20 ns
Required duty cycle	50% ±10
Imput impedence	50 Ω
Sensitivity	200 mVpp
Required input phase noise	<–137 dBc @ 10 MHz offset

Clock input

This input runs ParBERT synchronously with an external clock. Usage of a continuous clock is necessary. A burst clock can not be used as an external clock. Two modes are selectable: Indirect external clock mode (clock module PLL is used) and Direct external clock mode (clock module is bypassed).

Trigger output

The trigger output is used to deliver a trigger signal to a DUT, a digital communication analyzer (Agilent 86100A/B/C Series) or as a stimulus for the analyzer de-skew.

Table 65. Clock input

Clock input	AC coupled; 3.5 mm (f)
Frequency range Indirect mode Direct mode	 20.834 MHz...13.5 GHz 620 MHz...13.5 GHz
Clock input (indirect mode only) Multiplier(m)/divider(n)	m = 1...256; n = 1...256 m x n < = 1024; clock > = 5 MHz
Input transition/slope	30 ps typ.
Zin	50 Ω
Sensitivity	< 150 mV
Required input phase noise	< 75 - 20 log (13.5 GHz / input frequency) dBc / Hz

Table 66. Trigger input

Trigger output	DC coupled, SMA (f)
Frequency	Up to 675 MHz
Output transition/slope	70 ps typ. 10/90
Zout/termination voltage	50 Ω /-2 to +3 V
Output voltage window	–2 V to +3 V
Output level	0.1 to 1.8 Vpp

E4805B and E4808A central clock modules

The central clock module includes a PLL (phase-locked loop) frequency generator to provide a system clock. Depending on the frequency chosen, the data modules can be clocked at a ratio of 1, 2, 4, 8, 16, 32, 64 or 256 times higher or lower than the system clock.

External start/stop: The data can be started by an external signal applied to the external input. When using the E4832A module, a stop mode and a gate mode is also available.

Ext. clock/ext. reference: This input runs ParBERT 81250 synchronously with an ext. clock, or when a more accurate reference is needed than the internal oscillator. A continuous clock is necessary. A burst clock cannot be used as an external clock. Maximum external clock is 2.7 GHz for the E4805B and 10.8 Gb/s for the E4808A. (Note: no improvement of jitter specifications will be achieved with an external clock).

Guided de-skew: Individual semi-automatic deskew per channel is available. The 15447A de-skew probe 15447A allows de-skew on the DUT's (device under test) fixture.

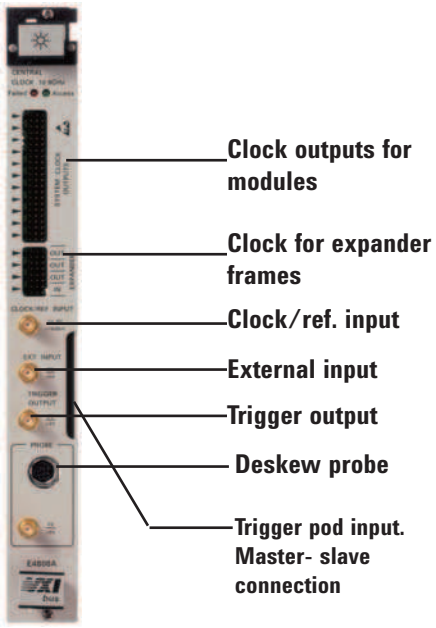

Figure 33: Clock module

Table 67. E4805B and E4808A clock module specifications

	E4805B	E4808B
Frequency range (1) (can be entered as period or frequency)	1 kHz to 675 MHz	170 kHz to 675 MHz
will run with	• E4861A (2) in range of 334 MHz to 2.7GHz • E4832A in range of 334 KHZ to 675 MHz	• E4866A/E4867A (2) in range of 9.5 GHz to 10.8 GHz • E4861B in range of 20.834 MHz to 3.35 GHz • E4861A (2) in range of 334 MHz to 2.7 GHz • E4832A in range of 334 KHZ to 675 MHz
Resolution	1 Hz	1 Hz
Accuracy	±50 ppm with internal PLL reference	±50 ppm with internal PLL reference

(1) May be limited or enhanced by modules or frontends
(2) Modules discontinued

Table 68. External input and ext. clock/ext. ref. input

	E4805B		E4808A	
Zin/termination voltage	50 Ω /-2.10 V to 3.30 V		50 Ω /-2.10 V to 3.30 V	
Sensitivity/max levels	400 mVpp/-3 V to + 6 V		200 mVpp/-3 V to + 6V for < 9.5 Gbit/s 300 mVpp/-3 V to+ 6 V for > 9.5 Gb/s	
Coupling	dc		dc	
Ext. input:	Threshold range: –1.40 V to +3.70 V		–1.40 V to +3.70 V	
Ext. clock/ext. ref:	ac		ac	
Input transitions/slope	< 20 ns. ext. input active edge is selectable		< 20 ns. ext. input active edge is selectable	
Clock input multiplier(m)/divider (n)	m = 1...256; n = 1...256 m*n < = 1024 m/n * input frequency must fit data range input frequency/n > = 1.3 MHz			
PLL lock time	100 ms		100 ms	
Input frequency/period Ext. clock	170 kHz - 2.7 GHz		170 kHz - 10.8 GHz	
Ext. ref	1(1), 2(1), 5, or 10 MHz		1(1), 2(1), 5, or 10 MHz	
Required duty cycle	50 ±10 %		50 ±10 %	
Latency (typical):	to trigger output	to channel output	to trigger output	to trigger output
Ext. input	16ns ±1 clock	46ns ±1 clock	16 ns ±1 clock	46 ns ±1 clock(2)
Ext. clock	15 ns	45 ns	15 ns	45 ns
	Add 3 ns if an expander frame is used		Add 3 ns if an expander frame is used	

(1) Jitter performance may be degraded

(2) If frequency = 667 MHz

Trigger ouput

Can be used in:

- Clock mode
- Sequence mode

In sequence mode a pulse will be set to mark the start of any segment.

In clock mode, the trigger output can supply a clock output of up to 675 MHz. If a higher speed performance clock is needed:

- A 2.7 Gb/s generator can be used to supply a clock output up to 2.7 GHz
- A 10.8 Gb/s generator can be used to supply a clock output up to 10.8 GHz.

Table 69. Trigger output characteristics E4805B and E4808A

Trigger output signals	• Clock mode (up to 675 MHz). • Sequence mode
Output impedance	50 Ω typ.
Output level	TTL (frequency < 180 MHz), 50 Ω to GND
	ECL 50 Ω to GND/-2 V, PECL 50 Ω +3 V
Trigger advance	30 ns typ. between trigger output and data output /sampling point (delay set to zero in both cases)
Maximum ext voltage	–2 V to +3.3 V
Jitter (int. reference/int. clock)	< 10 ps rms (5 ps typ.)

Technical specifications
All specifications describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications are valid from 10 ° to 40 ° ambient temperature after a 30 minute warm-up phase, with outputs and inputs terminated with 50 Ohms to ground at ECL levels unless specified otherwise.

Mainframes: See table 72 on page 56.

Save/recall: Pattern segments, settings and complete settings plus segments can be saved and recalled. The number of settings that can be stored is limited only by disk space.

Vector import/export: File format is ASCII using a STIL subset. Import/export to/from ParBERT internal data-base for regular file transfer via USB memory stick, CD or LAN is handled by ParBERT user SW. Direct programming of data segments is possible via GPIB (IEEE 488.2) and SCPI.

Programming interface: GP-IB (IEEE 488.2) and LAN. The interface to applications such as C, Visual Basic, or VEE must be installed. Use the Agilent 81200 *Plug&Play* drivers for easy programming.

Programming language:
SCPI 1992.0, active X for MUI

Programming times: Vector transfer from memory to hardware depends on the amount of data. See Table 70 for examples.

On-line help: Context-sensitive.

Print-on-demand: Getting started and programming guides can be printed from .pdf files included in the ParBERT 81250 software.

Self-test: Module and system selftests can be initiated.

Modules

Module size:
VXI C-size, 1 slot.

Module type:
Register-based; requires ParBERT 81250 user software E4875A supplied with the mainframes.

Weight:
(including front-ends) Net: 2kg.

Shipping: 2.5 kg.

Warranty:
1 year return to Agilent

Re-calibration period: 1 year.

Agilent Technologies quality standards
The ParBERT 81250 is produced in accordance to the ISO 9001 international quality system standard as part of Agilent Technologies' commitment to continually increasing customer satisfaction through improved quality control.

Table 70. Programming times

Parameter	Programming time For one E4805B with one E4832A. Increases with the number of modules.
Change of levels	6 ms typ.
Change of delay	16 ms typ. Not applicable in run mode
Change of period (1)	60 ms typ. Not applicable in run mode.
Stop & start	32 ms typ.
Synchronization (1)	50 ms typ. (without phase alignment) 110 ms typ. with 20% phase accuracy @ 660 MHz 650 ms typ. with 1% phase accuracy @ 660 MHz
Download values	
System with 4 channels	< 1.5 s typ. 1000,000 bit each
System with 120 channels	< 20 s typ. 1 Mbit each
System with 40 channels	< 10 s typ. 1 Mbit each

(1) valid for a system consisting of one E4805A and one E4832A.

Table 71. Cooling requirements for modules with front-ends installed

Modules	ΔP mm H20	Air flow liter/s	Max Δtemp
E4805B	0.25	3.6	10 °C
E4808A	0.25	3.6	10 °C
E4809A	1.08	3.7	12 °C
E4832A	0.30	4.7	15 °C
E4861B	0.40	6.6	15 °C
N4872A/74A	1.20	7.5	13 °C
N4873A/75A	0.85	5.4	12 °C

Table 72. Power Requirements of Modules and Front-Ends

	DC Volts	+24V	+12V	+5V	–2V	–5.2V	–12V	–24V
Modules (These specifications are valid for the module with the front-ends installed)								
E4805B Central Clock module	DC Current Dynamic current	0.15A 0.015A	0.2A 0.02A	1.8A 0.18A	1.4A 0.14A	3.8A 0.38A	0.2A 0.02A	– –
E4808A	DC Current Dynamic current	0.2A 0.02A	0.3 A. 0.03A	1.8A 0.18A	1.9A 0.19A	3.9A 0.39A	0.2A 0.02A	– –
E4809A	DC Current Dynamic current	0.35A 0.05A	1.25 A 0.15A	2.0A 0.2A	2.4A 0.3A	6.8A 0.7A	0.5A 0.05A	0.55A 0.06A
N4872A/74A	DC Current Dynamic current	0.5A 0.05A	0.75A 0.08A	3.8A 0.38A	0.6A 0.06A	2.6A 0.26A	1.2A 0.12A	0.8A 0.08A
N4873A/75A	DC Current Dynamic current	0.2A 0.02A	0.5A 0.05A	4.6A 0.46A	0.7A 0.07A	2.3A 0.23A	0.3A 0.03A	0.7A 0.07A
E4861B	DC Current Dynamic current	0.02A 0.01A	0.03A 0.01A	2.2A 0.2A	0.4A 0.04A	0.4A 0.04A	– –	– –
E4862B Generator	DC Current Dynamic Current	0.2A 0.02A	0.2A 0.02A	1.0A 0.07A	0.2A 0.02A	0.5A 0.05A	0.21A 0.2A	0.48A 0.05A
E4863B Analyzer	DC Current Dynamic Current	0.2A 0.02A	0.2A 0.02A	2.0A 0.02A	0.2A 0.02A	0.45A 0.05A	0.21A 0.2A	0.48A 0.05A
E4832A 675 Mb/s Gen./An. Module	DC Current Dynamic Current	0.10A 0.01A	0.10A 0.01A	2.60A 0.26A	0.60A 0.06A	3.60A 0.36A	0.10A 0.01A	0.1A 0.01A
Remark: For the module E4832A, the power specifications of the chosen front-ends (E4835A, E4838A or E4843A) have to be added to the power specifications of the E4832A module to get the overall value of the power specifications								
E4838A Differential Generator 675 Mb/s	Dynamic Current DC Current		0.45A 0.045A	0.18A 0.018A	0.07A 0.007A	0.38A 0.038A	0.41A 0.041A	– –
Front-ends								
E4835A two differential Analyzer 675 Mb/s	DC Current Dynamic Current		0.2A 0.02A	1.2A 0.12A	0.2A 0.02A	0.3 A 0.03A	0.3A 0.03A	– –

Table 73. General mainframe characteristics

	81250A mainframe
Description	E8403A 13 slot VXI C-size frame
Order description	81250A-149 (entry frame) 81250A-152 (expander frame) 81250A-148
Number of slots available for ParBERT 81250 data/ clock modules	12
Operating temperature	10 °C to 40 °C
Storage temperature	-20 °C to +60 °C
Humidity	80% rel. humidity at 40 °C
Power requirements	90 - 264 Vac 47 - 66 Hz 90 - 264 Vac 300 - 440 Hz (not recommended: leakage current may exceed safety limits @ > 132 Vac)
Power available for modules	950 W for 90 - 110 Vac supplies 1000 W for 110 - 264 Vac supplies
Electromagnetic compatibility	EN 55011/CISPR 11 group 1, class A + 26 dB
Acoustic noise	48 (56) dBA sound pressure at low (high fan speed)
Safety	IEC 348, UL 1244, CSA 22.2 #231, CE-mark
Physical dimensions	W: 424.5 mm, 16.71 inches H: 352 mm, 13.85 inches D: 631 mm, 24.84 inches
Weight (net)	26.8 kg (25.3 kg)
Weight (shipping) (max.)	72 kg (67 kg)

The ParBERT 81250 is a modular instrument, which can be tailored to your specific needs. It consists of the user SW and modules. These can be categorized by their functionality (clock or data) and their maximum data rate (675Mb/s, 3.35Gb/s and 7/13.5Gb/s).

The 675Mb/s data modules can hold up to four generator or analyzer Front-Ends allowing either four generator- or analyzer- channels or two channels of each kind. The 3.35Gb/s modules can hold two Front-Ends of any combination, resulting in two channels. The 7Gb/s and 13Gb/s modules are dedicated generator or analyzer modules delivering one data channel.

Entry system

A minimum system consists of one clock module and one data module forming a so-called clock group which gets installed in the ParBERT VXI-mainframe.

The connection between the PC (81250 #015, a laptop), which runs the user SW, and the VXI-frame, which holds the the ParBERT hardware, is achieved by the so called slot-0 controller, in this case an IEEE1394 FireWire interface, 81250 #013, which consumes 1 of the 13 slots of the VXI-frame.

The mainframe can hold multiple clock groups. Each is operated by its own instance of the graphical user interface (GUI).

Assuming the use of the Firewire interface and one clock module in place, the entry system can hold up to:

- 10 channels at 13.5 Gb/s and 7 Gb/s
- 22 channels at 3.35 Gb/s
- 44 channels at 675 Mb/s.

In some circumstances these maximum numbers cannot be achieved due to power restrictions. Before finalizing a configuration, it is necessary to calculate the power budget. The 675 Mb/s Analyzer E4835A always comes as a pair and need to be configured side by side, providing two fully independent analyzer channels.

Table 74. Ordering guide

Data module/front-ends		Generator	Analyzer	Clock module
13.5 Gb/s data module		N4872B	N4873	E4809A
7 Gb/s data module		N4874A	N4875A	E4809A
3.35 Gb/s data module	(1)	E4861B	E4861B	E4808A
3.35 Gb/s front-end		E4862B	E4863B	or E4809A
675 MHz data module	(2)	E4832A	E4832A	E4805B
675 MHz front-end	(3)	E4838A	E4835A	or E4808A
				or E4809A

(1) Houses 2 front-ends
(2) Houses 4 front-ends
(3) E4835A provides a pair of analyzers

Table 75. Entry system

Max # of channels FireWire	675 Mbits	3.35 Gb/s	7 or 13.5 Gb/s
1 frame	44	22	10
2 frames	88	44	20
3 frames	132	66	30
4 frames	176	88	40

More than 3 frames require more than one clock group.

Multi-mainframe/master-slave

If the number of desired channels exceeds the number of available slots in the “entry” frame, it is possible to add expander frames. To add channels within one clock group, there is the limit of a maximum of two expander frames. If data modules are housed in an expander frame they need an additional clock module. This clock module must be connected to the clock module in the entry frame (master frame) with the help of the master-slave connection. This connection carries the clock and data flow synchronization between the frames. The master-slave connection hardware is delivered with the expander frames. The master-slave connection is only possible between clock modules of the same type.

Aside from the master-slave connection between the clock modules, the controller interface also needs an extension into the expander frames:

The FireWire interface, can be “daisy-chained” from frame to frame. This would allow the configuration of a ParBERT 81250 system with a virtually unlimited number of channels. However, as mentioned above, a clock group can only be constructed of up to three VXI-frames, such that ParBERT systems larger than three frames must consist of more than one-clock group.

Different clock groups

A clock group consists of a clock module and one or more data modules. It is possible to have data modules from different speed classes combined in one clock group. The configuration of more than one clock group is possible. Several clock groups may be housed in one frame. Using expander frames is also possible. Each clock group will be operated from an independent instance of the graphical user interface, which will actually be assigned to this set of hardware defined as a clock group. In such a case the different GUIs may run from separate PCs, connected via LAN. A configuration of more than one clock group is recommended for the following purposes:

- To run different speeds (non binary ratio) between generators and/or analyzers
- To make flexible use of data rate range when combining different speed classes
- To use custom (memory) based data and use of bit synchronization for the analyzer(s).

The additional clock modules necessary for the different clock groups reduce the maximum number of possible channels listed in table 85 on the previous page. A master-slave connection must not be installed between the clock modules if different clock groups are desired.

Order information entry system	
1 x 81250A 1 x 81250-149 1 x E4805B-ATO/E4808A-ATO/ E4809A-ATO	System reference Mainframe 1st clock module
Decide on controller:	
1 x 81250A-013 1 x 81250A-014 or 1 x 81250A-015	FireWire (IEEE 1394) PC Link to VXI Ext. PC Laptop including PCMCIA IEEE 1394 card
Decide on controller accessories:	
1 x 15444A 1 x 15445A	Monitor Ext. CD-ROM
Order information multi mainframe:	
1 x 81250-152 1 x E4805B/E4808A/	FireWire (IEEE 1394) expander frame Clock module
Order information master-slave/different clock groups	
E4805B-ATO:	Clock module (usable with 675Mb/s and 2.7 Gb/s module)
E4808A-ATO:	Clock module (usable with 675 Mb/s, 1.65 Gb/s, 2.7 Gb/s, 3.35 Gb/s, 10.8 Gb/s and 45 Gb/s modules)
E4809A-ATO:	Clock module (usable with 675 Mb/s, 3.35 Gb/s, 7 Gb/s and 13.5 Gb/s modules)
Specific rules:	Do not mix E4809A, E4808A and E4805B: • Slave connection is possible only between clock modules of the same type • One system must be configured with one type of clock module

Add data modules/front-ends

Table 76. Cable kit accessories

P/N	Cable kit description	No. of cables	Connectors	To be used with	Bandwidth	Matching	Length	Addl. parts included
15441A	SMA to SCI	10	SMA (m) - SCI (f)	675 Mb/s	tt ≥ 500 ps	No	1.5 m	4 SCI adapters
15442A	SMA	4	SMA (m) - SMA (m)	675 Mb/s/ (3.35*) Gb/s	tt ≥ 100 ps	No	1 m	–
15443	SMA matched pair	2	SMA (m) - SMA (m)	675 Mb/s/ (3.35*) Gb/s	tt ≥ 100 ps	Yes	1 m	–
N4869A	SMA & phase shifter	3	SMA (m) - SMA (m)	E4866A out to N4868A in	tt ≥ 50 ps	Adjustable	0.4 m	Mech. phase Shifter ± 50 ps
N4870A	1.85 mm matched	2	1.85/2.4 mm 1.85/2.4 mm	N4868A out E4868A/B out E4869A/B in	tt ≥ 15 ps	± 1.5 ps	0.63 m	–
N4871A	SMA matched	2	SMA (m) - SMA (m)	3.35 Gb/s front-ends	tt ≥ 50 ps	± 1.5 ps	1 m	–
N4910A	2.4 mm matched pair	2	2.4 mm - 2.4 mm	7 Gb/s,	13.5 Gb/s	0.60 m		–

Product structure - ParBERT 81250

Part #/Option	Description
81250A	ParBERT 81250
81250A-013	IEEE 1394 PC link to VXI
81250A-015	Laptop including PCMCIA IEEE 1394 card
81250A-148	13-slot VXI Mainframe
81250A-149	Mainframe
81250A-152	IEEE 1394 'FireWire' expander frame
81250A-0B0	Do not include tutorial CD ROM
81250A-AX4	Rack flange kit
Software	
E4875A-ATO	One licence and software CD ROM for ParBERT 81250
Clock modules	
E4805B	675 MHz central clock module
E4808A	High performance central clock module
E4809A	13.5 GHz central clock module
Data modules & front ends	
E4832A-ATO	675 Mb/s generator/analyzer module
E4835A-FG	Two differential analyzer front-ends, 675 Mb/s
E4838A-FG	Differential generator front-end, 675 Mb/s
E4861B-ATO	3.35 Gb/s generator/analyzer module
E4862B-ATO	Generator front-end 3.35 Gb/s
E4863B-ATO	Analyzer front-end 3.35 Gb/s
N4874A-ATO	Generator module 7 Gb/s
N4875A-ATO	Analyzer module 7 Gb/s
N4872A-ATO	Generator module 13.5 Gb/s
N4873A-ATO	Analyzer module 13.5 Gb/s
HDMI bundles and accessories	
E4887A-003	Economic HDMI Signal Generator up to 3.4 Gb/s
E4887A-007	HDMI TMDS Signal Generator up to 7 Gb/s
E4887A-037	HDMI TMDS Signal Generator up to 3.4 Gb/s
E4887A-101	CTS 1.3 compliant low-speed cable emulator (< 75MHz)
E4887A-102	CTS 1.3 compliant high-speed cable emulator (> 75MHz)
E4887A-104	CTS 1.3 compliant passive EQ type cable emulator (set of 8 units)
E4887A-207	HDMI Frame Generator Software for E4887A platform
E4887A-303	Accessory and Cable Kit for E4887A-003 HDMI Signal Generator
E4887A-307	Accessory and Cable Kit for E4887A-007 TMDS Signal Generator 7 Gb/s
E4887A-308	Accessory and Cable Kit for E4887A-007 HDMI TMDS Signal Generator
E4887A-310	Accessory and Cable Kit for E4887A-037 HDMI TMDS Signal Generator
E4887A-S01	CTS 1.3 compliant passice EQ type cable emulator prototype (5mm chip)

Accessories	
15440A	Adapter kit: 4* SMA (M) I/O adapters
15442A	Cable kit: 4*SMA (m) to SMA (m)
15443A	Matched cable pair
15446A	8-line trigger input pod
15447A	Deskew probe
N4871A	Cable kit: SMA matched pair, 50 ps
N4910A	Cable kit: matched cable pair for 13.5 G
N4911A-002	Adapter 3.5 mm female to 2.4 mm male
N4912A	2.4 mm 50Ω termination, male connector
N4913A	4 GHz deskew probe

Test automation software platform N5990 (Excerpt)	
N5990A-010	Test automation software platform, required for all other options
N5990A-001	Interfaces to databases (Microsoft SQL and MySQL) and web browsers
N5990A-500	User programming (API including templates)
	For test interfaces pls see **www.agilent.com/find/automation**

Warranty & services

All systems and modules have 1 year on-site warranty.

Start up assistance for first time users is included.

Storage of Customer Specific Data in ParBERT 81250 Modules and Front Ends

This statement is to certify that none of Agilent Technologies' ParBERT 81250 clock modules, data generator/analyzer modules or front ends store customer specific data in any non-volatile memory. As a general rule it can be said that after electrical power has been turned off, the modules will not store any data or settings.

Data storage across power down/power up cycles will only appear in the ParBERT's PC Controller where access to the data can be controlled via generic Microsoft ® Windows ® security mechanisms.

Related literature

- *Agilent ParBERT 81250, Mux/Demux Application, Application Note,* Literature Number 5968-9695E
- *Advanced Memory Buffer, Product Note,* Literature Number 5989-3481EN
- *Jitter Fundamentals: Jitter Tolerance Testing with Agilent 81250 ParBERT, Application Note,* Literature Number 5989-0223EN
- *HDMI Compliant Jitter Tolerance Test Solution for cable and RX Test with ParBERT 81250, Application Note,* Literature Number 5989-4959EN
- *How to characterize the Physical Layer of the Mobile Industry Processor Interface (MIPI D-PHY), Application Note* Literature Number, 5989-7184EN
- *Next Generation I/O Bus PCI-Express BER Test Solution Application Note,* Literature Number 5989-2690EN
- *Automated PCI Express Receiver Compliance Test and Characterization with the Agilent N5990A Software Platform, Application Note,* Literature Number 5989-5500EN
- *Agilent N5990A Test Automation Software Platform (Version 1.0), Product Overview,* Literature Number 5989-3797EN
- *Test Automation Software Platform N5990A, Data Sheet,* Literature Number 5989-5483EN
- *Total Jitter Measurement at Low Probability Levels Using Optimized BERT Scan Method, White Paper,* Literature Number 5989-2933EN
- *Fast Total Jitter Test Solution, Application Note,* Literature Number 5989-3151EN
- *BERT Family brochure - applications focused, Brochure,* Literature Number 5988-9514EN
- *Physical Layer Testing of Passive Optical Network (PON) Modules, Application note,* Literature number 5989-3298EN

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