Agilent N4850A DigRF v3 Digital Acquisition Probe

User's Guide

Agilent Technologies

Notices

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Agilent Technologies, Inc.
1900 Garden of the Gods Road
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Contents

1 Introduction

About this Manual

This manual will help you connect an Agilent N4850A acquisition probe to your board and set up the logic analysis system to make measurements.

Additional Information Sources

This manual is intended to be used with these other documents:

- See the *Agilent N4850A/N4860A Digital Probes Design Guide* for information on how to design the necessary connectors into your board. This document is available by searching for "N4850A" at www.agilent.com.
- See the *Agilent N4860A Stimulus Probe User's Guide* for information on how to use the N4850A acquisition probe and the N4860A stimulus probe together.
- See the N4850A/N4860A product data sheet for a description of the product and its characteristics.
- See the online help in the logic analysis system for more information on using the software tools.
- Detailed information on Agilent probes (such as the Agilent E5381A differential flying lead probe) is available by searching for the product number at www.agilent.com.

- Information on how to visualize captured IQ data using the DVSA software is available in Agilent Application Note 1593: *Making RF Measurements on Digital Serial Data with Agilent's Signal Extractor and the 89601A Vector Signal Analyzer*, available by searching for "signal extractor" at www.agilent.com.
- Additional application notes or white papers may be available from your Agilent representative.

Product Overview

The Agilent N4850A acquisition probe connects an Agilent Technologies logic analyzer between the baseband and RF components on a device under test, to allow decoding and display of DigRF v3 signals. The acquisition probe may be connected to a production board, as long as it incorporates the necessary connectors, or the probe may be connected to a test platform.

The Agilent N4860A stimulus probe allows you to generate the digital signals, emulating either a baseband IC or an RF IC. The stimulus probe is usually connected to a test platform which contains only one of the two chips.

Connection to the device under test

The 90-pin cable on the Agilent N4850A acquisition probe is the same as the ones which are used on Agilent 1695x-series logic analyzer cards. This allows you to choose from a variety of probes to make the physical connection. See *Probing Solutions for Logic Analyzers*, available from www.agilent.com/find/logic.

The Agilent N4860A stimulus probe is connected using three SMA cables.

The parts of a measurement system

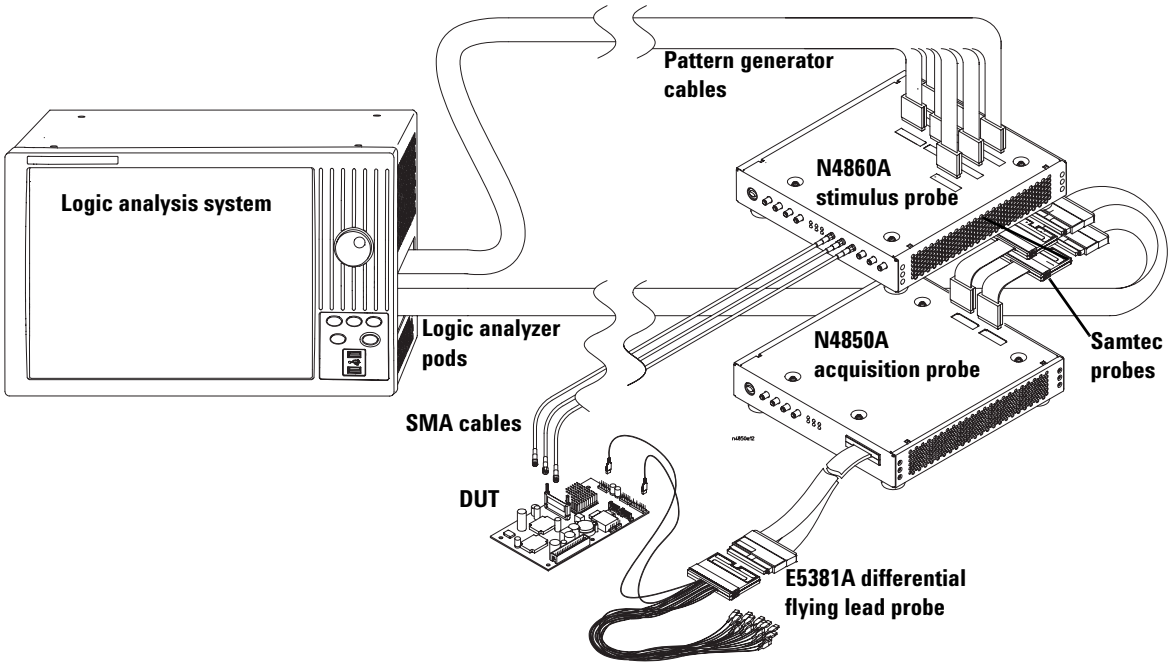


Figure 1 A complete measurement system

The device under test (**DUT**) is your board, which might include an RF IC, a baseband IC, or both.

The Agilent N4850A digital **acquisition probe** captures the digital signal between the two ICs. A **differential flying lead probe** (or another kind of probe, if needed) connects the DUT to the cable on the acquisition probe.

The Agilent N4860A **stimulus probe** can emulate an RF IC or baseband IC by supplying the missing digital signals. The stimulus probe connects to the DUT via 50-ohm coaxial cables using SMA connectors.

The acquisition probe and stimulus probe are connected to one another through a short **option cable**.

A **logic analysis system** collects data from the acquisition probe and controls the stimulus probe. The logic analysis system must contain at least one **logic analyzer** card. If you are using the N4860A stimulus probe, the logic analysis system must also contain a **pattern generator** card.

Each of the cables coming out of the logic analyzer card is called a **pod**. These pods require adapter cables, called **Samtec probes**, to mate with the connectors on the acquisition probe and stimulus probe.

For some logic analyzers, the logic analyzer card and pattern generator are built in, rather than being separate cards.

Software installed on the logic analysis system decodes the digital RF data and displays it as digital waveforms, as decoded packets, or as IQ data. The software also extracts the IQ data for analysis with other products such as the Agilent 89601 digitial vector signal analysis (DVSA) software.

Equipment Supplied

The Agilent N4850A includes:

- The Agilent N4850A acquisition probe.
- A power supply.
- A power cord appropriate for your country.
- This *User's Guide*.
- Regulatory compliance documents.
- A software license certificate.

Additional Equipment and Software Required

You *must* have the following additional equipment to use the N4850A acquisition probe:

- An Agilent 16800-series or 16900-series logic analysis system.
- An Agilent probe adapter to connect the pods of the logic analyzer to the Samtec connectors on the acquisition probe, such as the Agilent E5385A probe. These are sometimes called “Y adapter cables.”
- An Agilent probe to connect the acquisition probe to the device under test. Probing options are described in the the *Agilent N4850A/N4860A Digital Probes Design Guide*.
- The Agilent N4850A DigRF v3 Digital Acquisition Probe software. See “Installing the Software” on page 16 for information on obtaining and installing the software.

The following equipment and software *may* be required, depending on the kinds of measurements you plan to make:

- An Agilent N4860A stimulus probe and associated equipment and software.
- SMA cables, if you will be using the SMA outputs with another instrument.
- A torque wrench for the SMA connectors. The wrench should provide 0.8 to 0.9 N • m (7 to 8 inch-pounds) of torque. An Agilent 3.5mm torque wrench (part number 8710-1765) will provide the appropriate amount of torque.
- The Agilent 89601A digital vector signal analyzer (DVSA) for viewing IQ data.
- The Agilent B4641A protocol development kit for customizing the protocol.

Overview of Installation and Setup

1. Check that you received all of the necessary equipment. See "Equipment Supplied" on page 12 and "Additional Equipment and Software Required" on page 13.
2. Check that the device under test has the necessary connectors. Make sure you know (or can find out) the name and voltage level of the signal at each connector. See the *Agilent N4850A/N4860A Digital Probes Design Guide*.
3. Set up the logic analysis system, if necessary.
4. Turn on the logic analysis system.
5. Install the software on the logic analysis system. See "Installing and Configuring the Software" on page 15.
6. Make the physical connections. This includes:
   - connecting the acquisition probe to the logic analyzer
   - connecting the acquisition probe to the device under test
   - connecting power to the acquisition probe
   - connecting other instruments, such as the N4860A stimulus probe or an oscilloscope
7. Turn on the acquisition probe, then the device under test. See "Connecting the Probe to a Power Source" on page 37.
8. Load a configuration file. See "Loading a Configuration File" on page 19.
9. Set up a logic analyzer trigger. See "Capturing Data" on page 39.
10. Begin making measurements.

2
Installing and Configuring the Software

Installing the Software

Where to find the software

Your Agilent logic analyzer is shipped with the latest application software installed on the instrument, including any licensed optional products you may have purchased.

The latest version of logic analyzer instrument and application software can be downloaded from the web or by ordering a copy of the logic analyzer application CD.

To download the latest logic analyzer application software

The latest logic analyzer product software can be downloaded from the web at:

http://www.agilent.com/find/LA-SW-Download

NOTE While you are visiting the Web site, be sure to download the most recent version of the manuals. You can find the manuals by searching for "Agilent N4850A" at www.agilent.com.

To obtain an application software CD

Logic analyzer product CDs can be ordered from this web- site:

http://software.cos.agilent.com/LogicAnalyzerSW

To sign up for software update notification

To be notified when software upgrades are available for downloading from the web, please sign up for e- mail notification at:

http://www.agilent.com/find/emailupdates

Installing the logic analysis system software

The N4850A acquisition probe requires version 03.67.3xxx or higher of the logic analysis system core software.

- If you downloaded the software, double-click **SetupLAxxxxxxxx.exe** then follow the instructions which are displayed.
- If you have a CD, insert the product CD and select **Install Products>Install Agilent Logic Analyzer**, then follow the instructions which are displayed.

Note that newer versions of the Logic Analyzer software will automatically uninstall the previous version as a step in the upgrade. (User files in the "Documents and Settings" folder are not affected.)

To install the logic analyzer software onto your PC for offline processing, insert the product CD into your PC drive, click INSTALL PRODUCTS>Install Logic Analyzer.

Installing the probe software

The Agilent B4602 signal extractor and DigRF v3 packet decoder and packet viewer are included with the N4850A acquisition probe. The signal extractor software requires a license before it can be used.

- If you downloaded the software, double-click **SetupProbeDigRFxxxxxxxx.exe** then follow the instructions which are displayed.
- If you have a CD, insert the product CD and select **Install Products>Install an Optional Probe>Install Agilent N4850A Analysis Probe for DigRF 03.xx.xxxx**, then follow the instructions which are displayed.
- If you will be using the signal extractor software, follow the instructions on the Entitlement Certificate to install the license. For more information, go to the Index tab in the online help and click “license.”

Installing additional software

The probe is normally used with other software such as the Agilent 89600 digital vector signal analyzer (DVSA) and Signal Studio, all of which are licensed. If you want to customize the protocol files, you will need the Agilent B4641A protocol development kit, which is also licensed. If you want to use these additional tools then you will need to purchase the proper licenses.

1. Insert the product CD and select **Install Products**, then install the additional software you need.
2. Follow the instructions on the Entitlement certificate to install the license for the software. For more information, go to the Index tab in the online help and click “license.”

Loading a Configuration File

You configure the logic analyzer by loading a configuration file. The information in the configuration file includes:

- Signal/bus names and channel assignments for the logic analyzer.
- Tool configuration including logic analyzers, probes, filters, and Listing displays.

Several configuration files are provided with the N4850A acquisition probe. In most cases, the logic analyzer configuration will be modified to work with your particular DUT, then saved as a custom configuration file.

To choose which provided configuration file to load

Several configuration files are provided. Choose the appropriate configuration for the measurement that you will be making.

Table 1 Supplied configuration files

Shortcut name	File name	Description
Load Analysis Only Default Config	AnalysisOnly_DefaultConfig.xml	1-Card Analyzer; for use when N4860A is not used; uses the Signal Extractor to extract IQ data which can be send to an anaysis program
Load Stimulus to BBIC Default Config	StimulusToBBIC_DefaultConfig.xml	1-Card Analyzer with pattern generator; used when both analysis and stimulus to a baseband IC will be used
Load Stimulus to RFIC Default Config	StimulusToRFIC_DefaultConfig.xml	1-Card Analyzer with pattern generator; used when both analysis and stimulusto an RF IC will be used

To load a provided configuration file

1. Check that the N4850A acquisition probe is connected to the logic analysis system and that it is turned on. See "Connecting to Your Board" on page 29.

   If you load a configuration file with the probe powered off, or not connected or incorrectly connected to the analyzer pods, the communication with the probe will fail and you will see an error message.
2. Close the logic analyzer window, if it is open.
3. Select **Start>All Programs>Agilent Logic Analyzer>Agilent N4850_60A DigRFv3 Default Configs** or open the shortcut on the desktop.
4. Click on the configuration you want.

   When you click on a configuration file, the logic analyzer software will start and configure itself.

To load a provided configuration file without restarting the logic analyzer software

1. Check that the N4850A acquisition probe is connected to the logic analysis system and that it is turned on. See "Connecting to Your Board" on page 29.

   If you load a configuration file with the probe powered off, or not connected or incorrectly connected to the analyzer pods, the communication with the probe will fail and you will see an error message.
2. Select **File>Open...**.
3. Navigate to the configuration file.

   The default location is:

```
C:\Documents and Settings\All Users\Documents\Agilent
Technologies\Logic Analyzer\Default Configs\Agilent\
N4850_60A Default Configs
```

4. Select the file and click Open.

To save a configuration file

The provided configuration files are read-only. If you modify the configuration and want to save your work, select **File>Save As...** and save the configuration as an ALA format file.

ALA format configuration files are more complete and efficient than XML format configuration files. See the logic analyzer online help for more information on these formats.

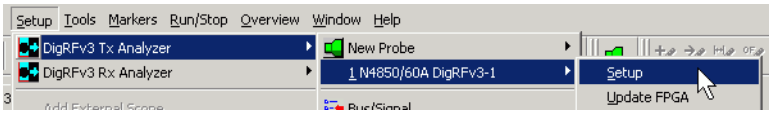
Setting up the Probe for Your Device Under Test

To open the probe setup dialog

Before you can make any measurements, you need to configure the acquisition probe for the type of DigRF v3 link you are probing.

1 Make sure the acquisition probe is connected and turned on. See "Connecting to Your Board" on page 29.

2 Open the Properties dialog.



3 Set the acquisition probe mode.

4 Configure the N4850A speed and voltage settings.

5 Configure the N4850A payload and miscellaneous settings.

6 Configure the N4850A outputs to the logic analyzer.

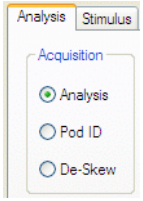
7 Configure the N4850A SMA inputs and outputs.

8 Configure the N4860A stimulus probe settings, as described in the *Agilent N4860A Stimulus Probe User's Guide* and in the online help.

Once you have configured the acquisition probe, remember to select **File>Save As...** and save the logic analyzer configuration.

To set the acquisition probe mode

The probe has four modes of operation. These modes include Analysis, Pod ID, and De-Skew.



Analysis mode is used to analyze the device under test. Analysis is the "normal" mode for acquiring activity from the link under test. Most of the graphical elements on the Setup tab which control the probe configuration are available only in Analysis mode.

Pod ID mode outputs Pod ID values on the analyzer channels and can be used to validate proper connection to the analyzer card. See the online help for instructions on how to do this.

De-Skew mode toggles all bits to the analyzer and can be used to validate that the cables are all connected properly and that the proper setup and hold values in the analyzer cards are set. Use the logic analyzer's eye finder with the De-Skew mode to validate that the proper setup and hold values are set. This should not be necessary during normal use. Use De-Skew mode only when instructed to do so by Agilent.

Configuring the clock speed

SysClk Speed

Set the speed you expect to be used by your device under test (DUT).

SysClk should be either 19.2 MHz, 26.0 MHz, or 38.4 MHz, as specified by the DigRF V3 specification. You must enter the correct frequency here so that data sent at SysClk/4 or SysClk speeds can be captured correctly. Once the correct frequency is entered, the N4850A acquisition probe will automatically detect the data transmission speed and capture the data (even if the speed change protocol is violated).

Voltages

Set the voltage levels used by your device under test.

SysClk VHigh (Voltage Threshold) is the threshold, or center voltage of the signal swing. If SysClk is AC coupled at the source, and a DC blocking capacitor was used, set SysClk VHigh to 750 mV.

SysClkEn VHigh is the threshold or voltage of the signal swing.

The Tx and Rx signals will be considered to be differential inputs. Specify the appropriate Vcm (common mode or center voltage) for each of these signals. Please be sure to enter Vcm accurately as this will allow the probe to properly detect the Tx or Rx sleep mode.

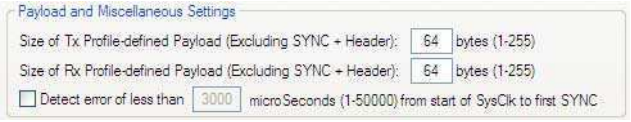
When using Agilent's demonstration board, use 26MHz and 1500 mV for all voltages.

For Target VDD VHigh, enter a value for Vsense which indicates that the DUT has power. This information is sent to the N4860A stimulus probe, which will not drive the stimulus signals until the DUT is active. Target VDD VHigh can be anywhere between 0.5V and 2.5V. Note that this will be a voltage that is used to detect the "power up" state, so you can use 2.5V even if the voltage is +5V. This setting is not required if you are only using the N4850A acquisition probe.

NOTE

Do not change the voltage thresholds in the logic analysis system's Bus/Signal Setup dialog. The voltage levels of the signals from the N4850A acquisition probe to the logic analyzer are always the same and never need to be adjusted. To adjust for the voltage levels on your DUT, use the probe setup dialog.

To configure payload and miscellaneous settings



Set the payload sizes which are used for the "profile-defined" payload size. The payload size must be an integer number of bytes. If you do not use a profile-defined frame, then you can leave these set to the default value of 64.

Set the minimum time between the start of SysClk and the first Sync. This is the minimum time between SysClkEn going true and the time when the RF IC is ready to receive SysClk. This value is used only to flag errors and allows the you to observe if the DUT is violating the needed time for the RF IC to power up.

When using Agilent's demonstration board, use the default values of 64 bytes and 3000 microseconds.

To configure Tx and Rx outputs to the logic analyzer

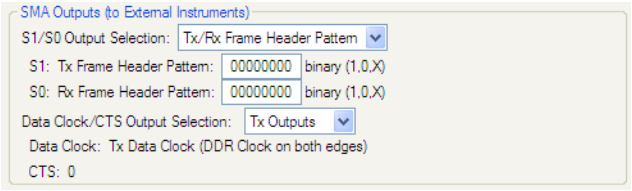
These selections allow you to filter out frames of particular types before they are sent to the logic analyzer.

For example, you may only want to see Data Channel A on the Rx output. To do this, unselect all Rx Output frames except the Data Channel A box.

You can filter out frames which you don't need to see either here or by using a filter tool in the logic analysis system. By filtering them here, you can conserve logic analyzer memory. By filtering with a filter tool, all of the frames will be saved in logic analyzer memory, and you can choose which of those frames to display.

In most cases, leave every box checked, so that all frames will be captured.

To configure the N4850A SMA inputs and outputs



You can control what information is sent through the SMA connectors on the probe. The most common use for these signals is to trigger an oscilloscope to capture certain events.

A large variety of signals can be output on the SMA connectors. The output selections include a wide variety of Tx outputs on S0, and a wide variety of Rx outputs on S1. The outputs include either a Level or Pulse designation to indicate what type of signal will be output when the condition is found. These signals are intended to drive other instruments as trigger events. The voltage range of the SMA connectors is 0V low and 3.3V high.

The CTS SMA can also output a variety of error conditions in addition to the ability to receive a SysClk signal. Use the Input Reference SysClk only if you are using N4860A stimulus probe for stimulus and you are trying to stimulate a baseband IC. This input allows you the ability to vary the SysClk frequency that will be driven out of the N4860A stimulus probe. Care must be taken to not violate the specification which may then cause the analysis phased lock loops to fail.

The Clock SMA outputs a variety of reconstructed clock signals. Be aware that the clocks are output in a DDR mode meaning that each edge of the output clock represents the rising edge of the internal clocks. This causes the clocks to be output at one-half of the rate of the internal clocks.

Tx/Rx Eye Closure

A brief 3.3V pulse will be issued when signal quality is poor and the size of the "data valid" eye does not meet DigRF v3 requirements (S1 for TxData, S0 for RxData).

Tx/Rx Out of Frame Data

A brief 3.3V pulse will be issued when data is detected outside of a packet frame (S1 for TxData, S0 for RxData).

Tx/Rx Frame Header Pattern

You can enter a binary pattern. When a frame header matches the pattern you entered, a brief 3.3V pulse will be issued from the SMA.

Data Clock/CTS

Choose whether to output a clock for TxData or RxData.

Note that the clocks are output in a DDR mode. Each edge of the output clock represents the rising edge of the internal clocks. This causes the clocks to be output at one-half of the rate of the internal clocks.

3 Connecting to Your Board

To connect the N4850A acquisition probe to the device under test (DUT), follow these steps:

1. Check that the device under test has the necessary connectors, as specified in the *Agilent N4850A/N4860A Digital Probes Design Guide*.
2. Make sure you know the name and voltage level of the signal at each connector.
3. Check the signal quality at each connector with an oscilloscope. See "Checking signal integrity" on page 30.
4. Position the N4850A acquisition probe for easy access and good ventilation. See "Positioning the Probe" on page 31.
5. Connect the logic analyzer cables to the N4850A acquisition probe. See "Connecting to the Logic Analysis System" on page 32.
6. Connect the acquisition probe to each of the required signals, listed in Table 2 on page 34.
7. Turn on the logic analysis system, then the N4850A acquisition probe, then the DUT. See "Connecting the Probe to a Power Source" on page 37.
8. Perform initial checks to confirm that the acquisition probe is ready to capture valid data:
   a. Check the LEDs on the front of the acquisition probe. See "Understanding the LEDs" on page 75.

Checking signal integrity

The N4850A acquisition probe is designed to be used with signals that meet the DigRF v3 electrical requirements. Before you connect the N4850A acquisition probe to your signals, use an oscilloscope to check the signals.

Positioning the Probe

Take care to allow space for the probe be placed near the device under test and the logic analysis system. You will also need plenty of space near the probe for the logic analysis system.

See "Mechanical Characteristics" on page 80 for probe dimensions.

Position the probe and power supply so that it is not difficult to unplug the power cord.

Allow at sufficient clearance above the probe for the logic analyzer cables. You may stack the N4860A stimulus probe on top of the N4850A acquisition probe.

Allow at least 5 cm (2 in) clearance on both sides of the probe for proper cooling.

CAUTION Do not block the airflow holes on the sides of the probe box. Blocked airflow may cause overheating and equipment damage

Connecting to the Logic Analysis System

The N4850A acquisition probe has two slots along the top edge labeled "Pod 1/Pod 2" and "Pod 3/ Pod 4". These slots are where the analyzer pods connect to the probe. Use the appropriate Samtec probe adapter to connect the probes to your logic analyzer card.

Logic analyzers with 90-pin connectors

Many logic analyzer cards, such as those in the 1695x family, have 90-pin connectors at the end of the pod cables. Use two E5378A 90-pin to Samtec probe adapters to connect the logic analyzer card to the probe.

- Connect Pod 1 to the Odd side of Pod 1 / Pod2.
- Connect Pod 2 to the Even side of Pod 1 / Pod 2.
- Connect Pod 3 to the Odd side of Pod 3 / Pod 4.
- Connect Pod 4 to the Even side of Pod 3 / Pod 4.

Logic analyzers with 40-pin connectors

If you are using a 40-pin connector based logic analyzer card then you will need to use two E5385A 40-pin to Samtec probe adapters. Connect them as listed above.

To verify the logic analyzer connections

If you are unsure whether you have connected the logic analyzer pods to the correct connectors on the N4850A acquisition probe, use the probe's Pod ID mode.

1. Turn on the logic analysis system and the N4850A acquisition probe.
2. Display the DigRF v3 probe tool.
3. In the Setup tab, select Pod ID mode.
4. Open the logic analyzer's Bus/Signal Setup window.
5. Find the signal activity indicators next to the bus/signal names.
6. Examine the activity indicators to determine if the pod is connected to the right place on the acquisition probe. At each connector on the acquisition probe, the "activity" pattern of bits will be a binary value that corresponds to the pod number.

Pod ID mode requires that at least one of the pods has been connected correctly.

Connecting to the Device Under Test

The probe uses the same 90-pin probe cable as the Agilent 1695x-series logic analyzer. That allows you to choose from a variety of probes to make the physical connection.

CAUTION

Caution: input connector

Connect the probe cable only to an Agilent Technologies probe, following the design recommendations in the *Agilent N4850A/N4860A Digital Probes Design Guide*.

Do not connect the signals or grounds to high voltages. Use ESD precautions to avoid static discharge. The grounds are not isolated from earth ground. Applying voltages which are above 5 V could damage the N4850A acquisition probe.

The exact details of the physical connection depend on which probe you use. See the *Agilent N4850A/N4860A Digital Probes Design Guide* and the manual for the probe you are using.

Signal-to-channel mapping

The following table shows the default mapping of signal names to logic analyzer channel numbers. This mapping works well if you are using Agilent E5381A flying leads.

Table 2 Connections for E5381A flying leads

Signal	Lead to connect	Comments
SysClk	Ch 3, positive	
SysClkEn	Ch 4, positive	
Vsense	Ch 6, positive	Required if using the N4860A stimulus probe. Optional if using the N4850A acquisition probe alone.
TxDataP	Ch 8, positive	

Table 2 Connections for E5381A flying leads

Signal	Lead to connect	Comments
TxDataN	Ch 9, positive	
RxDataP	Ch 15, positive	
RxDataN	CLOCK, positive	

The TxData and RxData lines are probed both as single ended and differential, even though the your physical connection is only single ended. This is done so that the "sleep" state, where positive and negative signals go to almost the same voltage, can be unambiguously detected.

The negative sides of all of these connections *must* be connected to ground.

Connecting the SMA cables

Threaded SMA connectors are provided in case you want to view the signals with another instrument, such as an oscilloscope.

CAUTION

Caution: SMA connectors

The SMA outputs are 3.3V only. Do not connect short these connectors to ground or to other low-impedance sources.

Do not connect the grounds to a high voltage—the grounds are not isolated from earth ground. When working near the SMA connectors, use ESD precautions to avoid static discharge.

Failure to follow these precautions could damage the N4850A acquisition probe.

Use a torque wrench to tighten the SMA connector.

Apply 0.8 to 0.9 N • m (7 to 8 inch-pounds) of torque. An Agilent 3.5mm torque wrench (part number 8710-1765) will provide the appropriate amount of torque.

Some torque wrenches, such as the Agilent SMA torque wrench (part number 8710-1582) provide only 5 in-lbs of torque. If you apply too little torque, the electrical connection may not be reliable.

CAUTION Apply no more than 0.9 N•m (8 inch-pounds) of torque. If you apply too much torque, the N4850A acquisition probe may be damaged.

Connecting the Probe to a Power Source

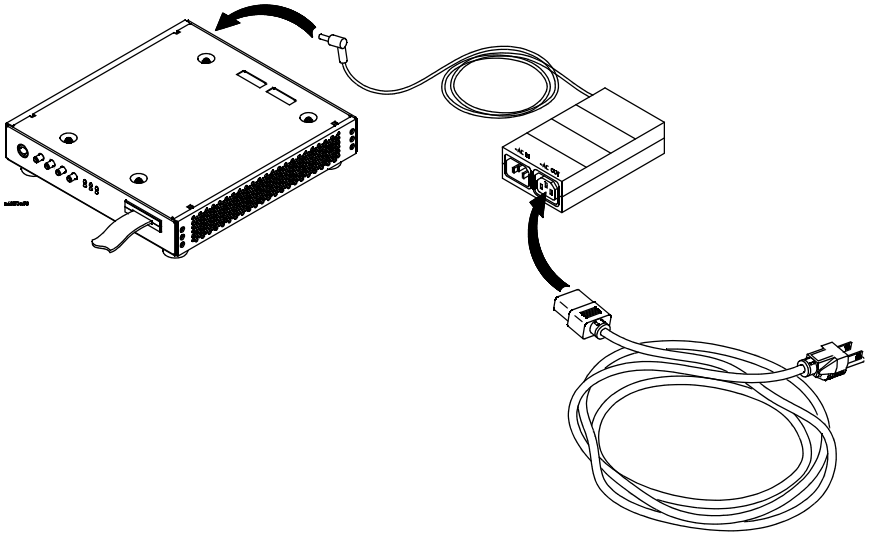
The probe is shipped from the factory with a power supply and cord appropriate for your country. If the cord you received is not appropriate for your electrical power outlet type, contact your Agilent Technologies sales and service office.

Position the probe and power supply so that it is not difficult to unplug the power cord.

WARNING **Maintain ground to avoid electrical shock.** Use only the power supply and power cord supplied with the probe. Connect the power cord only to a properly grounded electrical power outlet.

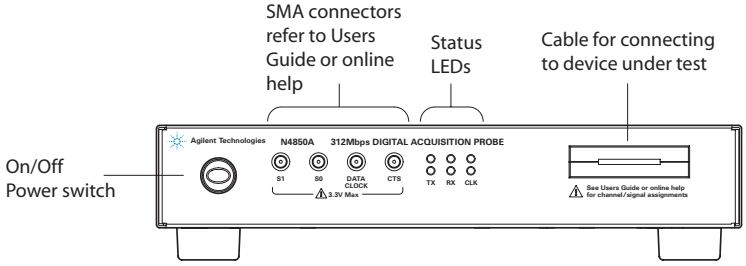
1. Connect the power cord to the power supply and to a socket outlet.
2. Connect the 12V power cord to the back of the probe.

   Ensure the power supply plug is completely seated in the power input receptacle.



To turn power ON

- Press the power button on the front of the probe.



The power button is lighted when the switch is ON.

It is best to power on the probe *before* loading a configuration file into the logic analysis system.

You may turn the probe on before or after the logic analysis system is turned on. You may connect and disconnect the cables and the logic analyzer pods while the probe and logic analyzer are powered on.

When you turn on the probe, self-test and loading of calibration factors can take up to 45 seconds.

To turn power OFF

- Press the power button on the front of the probe.

4 Capturing Data

This chapter shows you how to set up logic analyzer triggers to capture just the data you want.

The normal steps in using the logic analyzer are:

1. Configure the logic analyzer.
2. Configure the probe for the measurement.
3. Set up the trigger, and run the measurement.
4. Display the captured data.

The logic analyzer is configured, and buses (sometimes known as "labels") are created for the logic analysis signals when configuration files are loaded (see "Loading a Configuration File" on page 19).

Is the data captured in real time?

The logic analyzer captures data in real time as it is running. The trigger stops the measurement, after which you can use various tools to view the data which has been stored in the logic analyzer's memory.

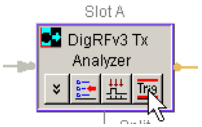
This chapter describes setting up logic analyzer triggers. See "Viewing the Captured Data" on page 49 for information on displaying the captured data.

Triggering on a Packet

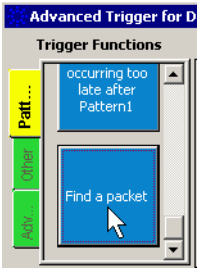
You can set up the logic analyzer to trigger when a certain event happens. For example, you can set the logic analyzer to trigger:

- When a certain kind of packet is detected.
- When a field in the header of a packet has a particular value.
- When the first few bytes of the payload has a particular value.

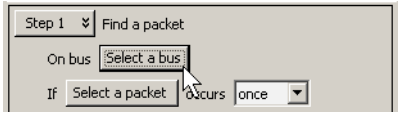
1 Open the Advanced Trigger dialog for the appropriate analyzer. Note that there is a separate Trigger dialog for Tx and Rx.

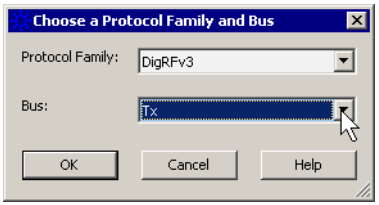


2 In the Advanced Trigger dialog, scroll down the list of trigger functions and drag **Find a packet** into the trigger sequence.

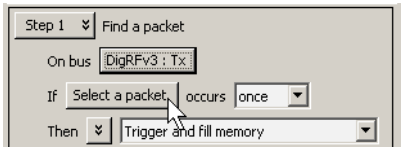


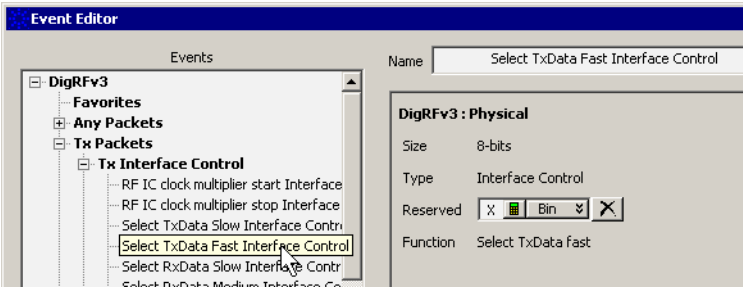
3 Select the bus.





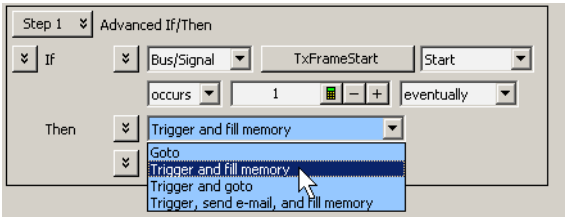
4 Select the packet which the logic analyzer should watch for.





5 If you want the logic analyzer to trigger only when the value of a field in the packet header has a certain value, or when the packet payload begins with a certain value, enter the value. Leave the value as “X” to trigger on any value.

6 Select what the logic analyzer should do when it encounters the packet. Usually you will want to “Trigger and fill memory.”



7 If you want to capture activity which happened before the trigger, or if you want to reduce the amount of information which is captured, see “To adjust sample position and memory depth” on page 45.

8 Click **OK**.

9 Run the logic analyzer.

To add new events

You cannot *modify* the events and packet types which are supplied in the configuration files, but you can *add* events using the Event Editor.

Triggering On Specific Events

To trigger on a speed change

A good test trigger is to trigger when there is a speed change on the DigRF link. On many DUTs, a speed change will occur as the link is initialized.

1. In the Listing display, find the Speed bus.
2. Set the base to Symbols.
3. Set a trigger for when the value becomes “312 MHz.”
4. Open the Sampling setup dialog.
5. Set the sampling position to about 80% prestore.
6. Uncheck Force Prestore.
7. Click Run.

To trigger on data capture problems: jitter

Use the EyeClose signal to find packets where there was excessive jitter or other signal quality problems. EyeClose=1 indicates that the time when the data is stable is getting small; the data may or may not have been read correctly.

A single EyeClose=1 within a packet indicates an eye width between 0.624 and 0.375.

EyeClose=1 on several states, until the end of the packet, can indicate that there was too much drift from the Sync word.

1. Trigger on EyeClose = 1.
2. Look for where the EyeClose occurred relative to FrameStart. Patterns can point you toward the cause:
   - Is the problem always at the start of a packet?
   - Is it always at the end of a long packet?
   - Does it occur at random?

To trigger on data capture problems: noise

Here is one way to look for out-of-frame signals.

1. Trigger on StatusOnly=1 to see if any bits are on.
2. Look at the individual status signals:

Status Only: the “status only” meanings of bits are valid (reused data bits)

Sleep: (Advisory) entered sleep state

NoStartSync: There was transition on differential data, but not between SYNC and end-of-frame

InvalidSysClk: SYSCLK frequency does not match the frequency which was set when the probe was configured

SysClkStopped: (Advisory)

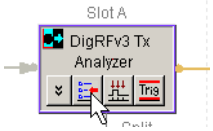
DataEarly: After SYSCLK started, got SYNC before GUI’s time

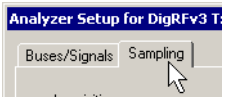
DidNotStop: Data toggling after end-of-frame

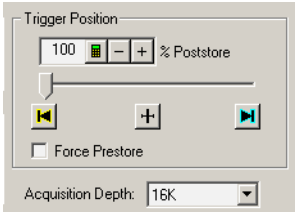
Customizing a Trigger

To adjust sample position and memory depth

If you want to capture activity which happened before the trigger, or if you want to reduce the amount of information which is captured, use the logic analyzer's Sampling tab.







If you move the trigger position, make sure that Force Prestore is not enabled.

To choose which data to store

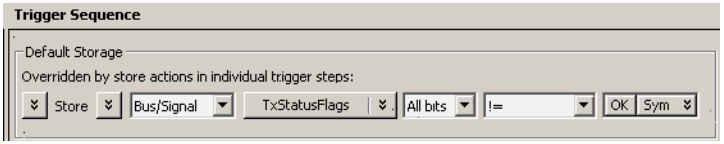
You can configure the N4850A acquisition probe to output only certain kinds of data to the logic analyzer. See "To configure Tx and Rx outputs to the logic analyzer" on page 25.

You can also control how much data is captured by the analyzer by using storage qualification to store only selected kinds of states.

Storage qualification acts as a real-time filter which allow you to selectively remove states from the captured data.

To store only error states

Use storage qualification and the StatusFlags bus to set up the logic analyzer to store only those states in which the N4850A acquisition probe detected an error.



When to Use the Sampling Tab

You may safely use the logic analyzer's Analyzer Setup window to change:

- Trigger position (start/center/end)
- Sampling positions (after running eye finder, to "fine-tune" the results if necessary)
- Acquisition depth

Many of the settings are set by the configuration files and should not be modified. *Do not* use the Analyzer Setup window to change:

- Analyzer mode (state/timing/eye scan)
- Clock setup
- Acquisition speed

5
Viewing the Captured Data

Understanding the Displays in the Logic Analysis System

To display an overview of tools in the logic analysis system

1 At the bottom of the logic analyzer window, click the **Overview** tab.

The Overview window lets you view how the data is sent from the logic analyzer data acquisition module to post-processing tools and display windows. Each icon represents a hardware or software tool you can use. The arrows represent the flow of data between tools.

The **Probes** column shows the probes which physically acquire the data.

The **Modules** column shows the logic analyzer cards which capture the data.

The **Tools** column shows post-processing tools which manipulate the captured data before it is displayed.

The **Windows** column shows the different display windows which you can use to display the captured data.

Tools may be accessed by clicking on their icon, by clicking on the tab at the bottom of the screen, or through the menus at the top of the screen.

See the online help in the logic analysis system for more information on how to add more tools and display windows. The online help also explains how to control the data flow between tools and windows, and how to control the appearance of the data within each window.

Overview window example: Rx and TX, no Signal Extractor

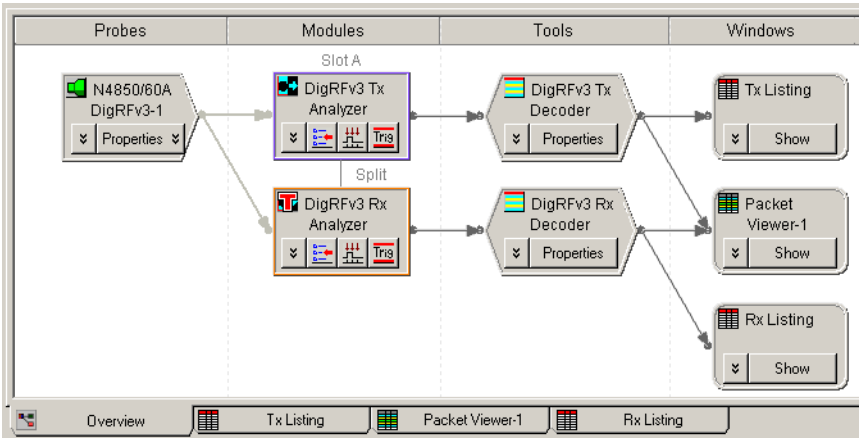


Figure 2 Overview display show Rx and Tx data, without a Signal Extractor tool

Figure 2 on page 51 shows a basic setup for the N4850A acquisition probe. The N4850A acquisition probe sends Tx data to one logic analyzer (which is probably one-half of a logic analyzer card, set up as a “module”). The Tx data is decoded by the DigRF3 Tx Decoder tool.

The decoded Tx data is then displayed as a series of logic analyzer states in the Tx Listing window. The Tx data is also displayed in packet form in the Packet Viewer window.

The Rx data is displayed in the same way. Note that both the Tx and Rx data are displayed in the same Packet Viewer.

Overview window example: Rx and TX, with Signal Extractor

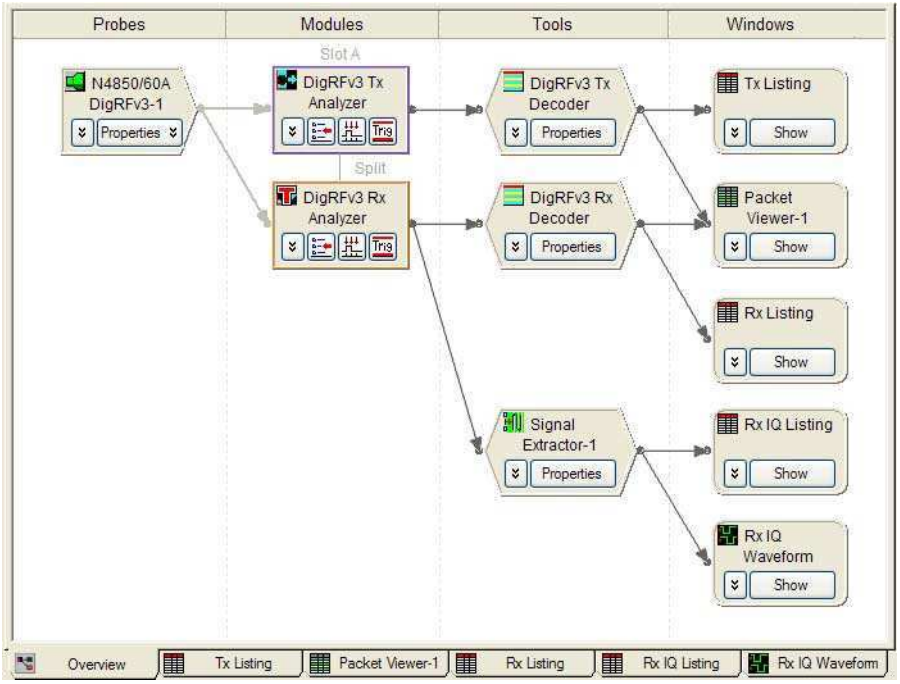


Figure 3 Overview display show Rx and Tx data, with a Signal Extractor tool

Figure 3 on page 52 shows a setup for the N4850A acquisition probe which includes the Signal Extractor tool. The N4850A acquisition probe sends Rx data to one logic analyzer (which is probably one-half of a logic analyzer card, set up as a “module”). The Rx data is sent to the Signal Extractor tool, which extracts the IQ data.

The IQ data can be displayed as a listing or plotted as a waveform. The IQ data can also be used as the input to the Agilent 89601A vector signal analyzer software.

Using the Listing Display

Predefined buses and signals

The configuration files define the following buses and signals. Each bus or signal corresponds to a column in the Listing display.

Table 3 Tx buses and signals

Tx signal/bus name	Size in bits	Description
TxData	24	The capture of the TxData without the Sync pattern.
TxStartFrame	1	Indicates the start of a frame. The Header byte is always placed in bits 23-16 of this label when TxStartFrame is true.
TxEndFrame	1	Indicates the end of a frame. One to three bytes of the TxData will be valid data. Invalid data will be set to zero.
TxSpeed	2	Indicates the speed that the frame was captured at.
TxCTS	1	Indicates the CTS condition on the Tx path (Duplicate of RxCTS)
TxEyeClosure	1	Indicates if the data capture eye had excessive jitter.
TxSpeedErr	1	Indicates if the specified speed does not match the speed that data was captured at.
TxStatusFlags	10	Indicates that a Status cycle has been introduced into the TxData. This status cycle is used to indicated addition information and possible error conditions.
TxExtractor	32	Grouping of all of the signals for the Signal Extractor tool.

Table 4 Rx buses and signals

Rx signal/bus name	Size in bits	Description
RxData	24	The capture of the RxData without the Sync pattern.
RxStartFrame	1	Indicates the start of a frame. The Header byte is always placed in bits 23-16 of this label when RxStartFrame is true.
RxEndFrame	1	Indicates the end of a frame. One to three bytes of the RxData will be valid data. Invalid data will be set to zero.
RxSpeed	2	Indicates the speed that the frame was captured at.
RxCTS	1	Indicates the CTS condition on the Rx path.
RxEyeClosure	1	Indicates if the data capture eye had excessive jitter.
RxSpeedErr	1	Indicates if the specified speed does not match the speed that data was captured at.
RxStatusFlags	10	Indicates that a Status cycle has been introduced into the RxData. This status cycle is used to indicated addition information and possible error conditions.
RxExtractor	32	Grouping of all of the signals for the Signal Extractor tool.

Predefined symbols

Status flags

The Tx and Rx buses and signals are basically duplicates of each other. The TxStatusFlags and RxStatusFlags deserve special attention.

When RxStatusFlags bit 10 is set to one then the RxData is now used to send additional status.

Symbols are defined for each combination of status flag bits. The additional status messages and their meanings are shown in Table 5.

Table 5 Status flag symbols

Status flag symbol	Description
InvalidSysClk	SYSCLK toggling while SYSCLKEN false
SysClkStopped	SysClk has stopped. This may have happened in the middle of a frame. If it does then Mocha will terminate the frame early by setting EOF. Then a Status Only cycle will be generated and SysClockStopped will be set to 1. The fact that the frame is too small will be caught by the protocol analyzer. If SysClk stops not in a frame then a status only cycle can be generated with SysClockStopped=1.
BadSysClkFreq	SysClk frequency is out of specification. Probe cannot maintain phase lock.
NoStartSync	Data is toggling, but start of frame Sync field was not found. This can happen if the eye for the Sync field is too small.
DataEarly	Too little time from when SYSCLK starts toggling to when DATA starts toggling ("too little" defined by user—see page 25).
DataNoSysClkEn	SysClkEn went false but the Data line is still active.
IllegalSleep	Data lines entered sleep, but the bit after frame did not request sleep.
Sleep	Line has been directed to enter sleep mode. (First bit of data is '1' after a frame.)

Table 5 Status flag symbols

Status flag symbol	Description
DidNotSleep	Bus did not enter low voltage sleep mode. When a '1' occurs after a packet we will generate a Status Only cycle with Sleep=1. If after a specified time the comparators do not indicate Sleep then we will output a Status Only cycle with Sleep=1 and DidNotSleep=1.
OK	Bit 10 is 0. There is no additional status message.

Speeds

Table 6 TxSpeed and RxSpeed symbols

Symbol	Description
SysClk/4	Indicates that the current packet was captured at a speed of SysClk/4.
SysClk	Indicates that the current packet was captured at a speed of SysClk.
312MHz	Indicates that the current packet was captured at a speed of 312 Mbps.

Frame start/end

Table 7 Tx and Rx Frame Start and End symbols

Symbol	Description
Start is High	Indicates start of a frame.
End is High	Indicates end of a frame.

EyeClose

Table 8 Tx and Rx EyeClose symbols

Symbol	Description
PossibleDataError is High	Indicates that the data capture eye had excessive jitter. Some data might not have been valid at the moment it was captured.
OK is Low	StatusFlags bit 10 is 0. There is no additional status message.

SpeedErr

Table 9 Tx and Rx SpeedErr symbols

Symbol	Description
SpeedMistake is High	The contents of a packet are being sent at a speed which is different from the speed indicated in the packet header.
OK is Low	StatusFlags bit 10 is 0. There is no additional status message.

Sync words

The N4850A acquisition probe strips off the 16-bit Sync word from each packet before the data is sent to the logic analyzer. This conserves logic analyzer memory, so you can capture more states.

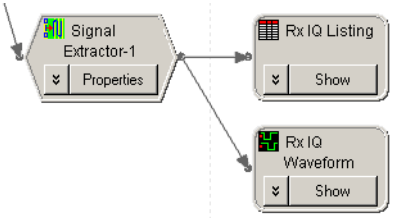
Each time a Sync word occurs, at least one state is captured by the logic analyzer. The state(s) will include the full packet, as defined by the size bits in the header.

If a Sync word is invalid, several things will happen:

- The top TX or RX LED will be red.
- The N4850A acquisition probe will set the corresponding StatusFlag to NoStartSync. You can trigger on this value, or search for it in the Listing display.
- A message will be displayed in the Listing display.
- No message will be displayed in the Packet Viewer display.

Extracting IQ data

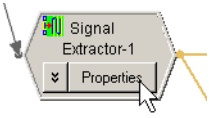
Use the Agilent B4602 signal extractor tool to extract I and Q values from the packet payload. The signal extractor tool is automatically added when you load one of the provided configuration files.



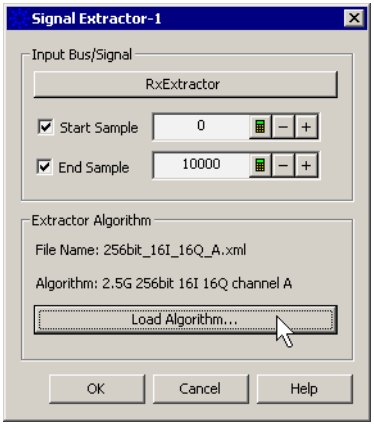
To choose an algorithm for extracting IQ data

DigRF v3 allows many different algorithms for encoding I and Q data in the payload.

1 Open the signal extractor Properties dialog.



2 Click Load Algorithm.



3 Choose the algorithm which is used by your DUT. All the DigRF v3 algorithms will be located in the DigRFv3 directory.

If you need a different algorithm then it can be created by modifying one of the existing algorithms. See "Customizing How IQ Data is Encoded" on page 67.

What you need to know about the Agilent B4602 signal extractor

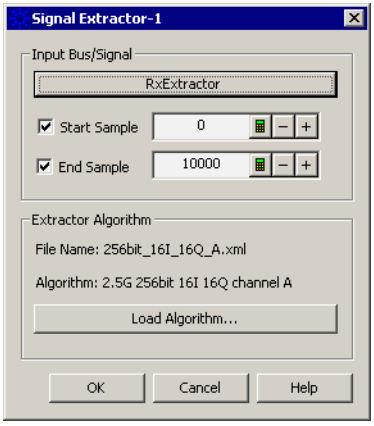


Figure 4 Signal extractor properties dialog

Licensing

The Agilent B4602 signal extractor is a licensed tool. It is included with the probe software, but you will need to purchase additional licenses if you want to run it on an additional logic analysis system or on a PC.

Improving performance

By default, the signal extractor processes the entire trace. It is possible to restrict the processing to a range of samples (the supplied configuration files limit the signal extractor to the first

10000 samples). This is different from most logic analysis tools, which can process just those samples required by the downstream display tool.

If it takes a long time to process the whole trace, you can improve performance in one of two ways:

- In the logic analyzer's Sampling dialog, reduce the acquisition depth.
- In the signal extractor properties dialog, set the start and end samples.

Logic analyzer buses

The signal extractor tool takes its input from one logic analyzer bus and places the extracted data on one or more buses. In the case of the N4850A acquisition probe, the buses are:

Table 10 Signal extractor input and output buses for DigRF v3

Bus name	Description
RxExtractor	All of the bits captured by the Rx analyzer. This bus is defined by the configuration file.
TxExtractor	All of the bits captured by the Tx analyzer. This bus is defined by the configuration file.
I	I data from the packet. This bus is defined by the signal extractor algorithm file.
Q	Q data from the packet. This bus is defined by the signal extractor algorithm file.
Signal Extractor: Sample Number	Each "sample" output from the signal extractor tool is assigned a sample number, beginning with 0. Not every logic analyzer sample is a packet containing IQ data, therefore there is not a one-to-one mapping between logic analyzer sample numbers and signal extractor sample numbers.

Algorithm files

DigRF v3 defines several data formats for packing I and Q values into a packet payload. XML algorithm files are provided for each of these formats.

If your DUT uses one of these defined formats, you can use one of the provided algorithm files.

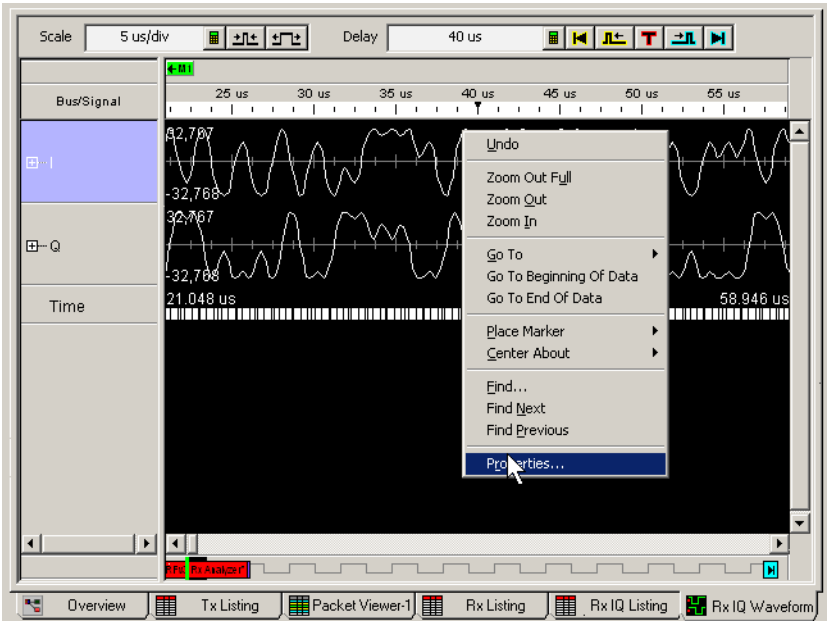
If your DUT uses a different format–for example, if it uses a profile-defined payload size–then you will need to modify one of the provided algorithms. See "Customizing How IQ Data is Encoded" on page 67.

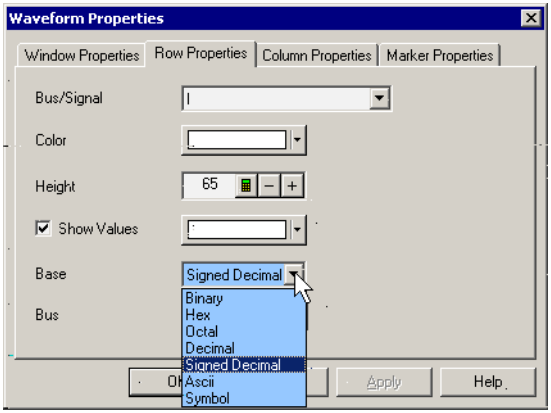
Using the Waveform display

The Waveform display can be used to view the I and Q data as seqarate waveforms.

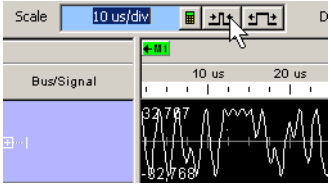
Tips for using the Waveform display

- Set the base to signed decimal.





- In most cases, it is necessary to scale the waveform to see it clearly.



Viewing IQ data with the Digital Vector Signal Analyzer

Information on how to visualize captured IQ data using the DVSA software is available in Agilent Application Note 1593: *Making RF Measurements on Digital Serial Data with Agilent's Signal Extractor and the 89601A Vector Signal Analyzer*, available by searching for "signal extractor" at www.agilent.com.

Here is a summary of the steps:

1. In the logic analysis system, connect a Signal Extractor tool to the Tx or Rx analyzer.
2. On the logic analysis system, start the VSA software.

   Now, in the VSA software:
3. Set the digital input properties.
4. Set the module name to be the Signal Extractor tool
5. Set up the demodulation.
6. Set up the displays.

Note that the data is captured in real time, then passed to the VSA software. The logic analyzer is not running while the data is being passed to the VSA, or while the VSA analyzes the data. After the VSA is done analyzing the data, the logic analyzer is ready to run again. You can shorten this cycle by reducing the memory depth of the logic analyzer trace (see "To adjust sample position and memory depth" on page 45).

6 Customizing the Protocol

Customizing How IQ Data is Encoded

The Agilent B4602 signal extractor tool uses XML files to define how the I and Q data is encoded in the packet payload.

If the algorithm used by your DUT is not covered by one of the provided algorithm files, you can create a new algorithm file.

Begin by choosing one of the provided algorithm files, then edit it with an XML editor or text editor.

Click the Help button in the signal extractor Properties dialog for detailed information on the syntax of the XML files.

Overview of the algorithm

An algorithm file consists of patterns and commands.

The signal extractor processes each logic analyzer sample, beginning with the Start Sample in the signal extractor Properties dialog.

If the signal extractor finds a matching pattern, then it will execute the corresponding command.

The signal extractor then shifts the pattern by the width of the input bus, and begins the pattern matching process again.

Patterns

Here is the Buses/Signals Setup dialog for the Tx analyzer:

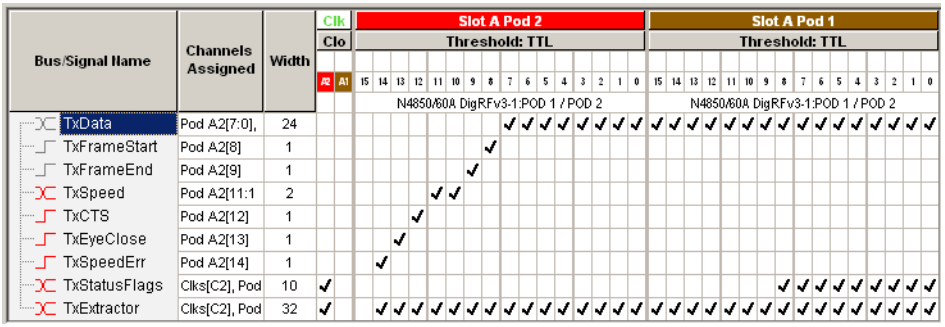


Figure 5 Tx buses and signals

The first 8 bits are status bits. When a sample is the beginning of a frame, the first 8 bits are 0xxxxxx1, and the next eight bits are the header. The rest is payload data.T he signal extractor algorithm uses this pattern to indentify the beginning of each frame:

```
<ExtractorPattern Value='b0XXXXXX1 1010111X XXXXXXXX
   XXXXXXXX' Width='32' Enabled='T' />
```

Commands

The I and Q data can appear in different positions on the logic analyzer's input bus. For example, profiles with a 16I_16Q format look like this:

<status bits>	<header>	I	I
<status bits>	Q	Q	I
<status bits>	I	Q	Q

For DigRF v3, the frame size is known. Therefore, a sequential set of commands can extract the I and Q values in the right order.

Timestamps

Each set of values output by the signal extractor has a sample number and a timestamp. The algorithm must calculate and write a *unique* timestamp for *every* set of output values. The signal extractor is able to interpolate the time of each input bit, based on the timestamps of successive logic analyzer samples.

The following lines from the 16I_16Q algorithm extract two bytes of I from the payload, and write it to the I bus. The time is set to the time of the last bit:

```
<ExtractorCmd Cmd="LoadRange" BitStart="56" BitEnd="63" />
<ExtractorCmd Cmd="LoadRange" BitStart="72" BitEnd="79" />
<ExtractorCmd Cmd="WriteLabelTime" Name="I" BitTime="79" />
```

Where to find the algorithm files

The provided algorithm files may be found at:

```
C:\Documents and Settings\All Users\Documents\Agilent
   Technologies\Logic Analyzer\Extractor Algorithms\DigRFv3
```

You may store your algorithm files wherever you wish.

Customizing frame structure and command encoding

It is possible to customize the protocol used by the Packet Decoder tool. For example, if your DUT defines additional interface control commands, you could customize the protocol so that those commands will be properly displayed in the Packet Viewer.

Tools required

To customize the protocol, you must have licenses for both the protocol (supplied with theN4850A acquisition probe) and the Agilent B4641A protocol development kit (purchased separately).

Protocol description files

The protocol is defined in a set of protocol description files.

Protocol description files are loaded when the Agilent Logic Analyzer application starts or when "refreshed" in the Packet Decoder tool.

Protocol description files have the .aex (Agilent Encrypted XML) file extension.

The Agilent B4641A protocol development kit (PDK) allows you to edit these files. The PDK editor provides standard text editing and XML syntax highlighting features.

See the logic analysis system’s online help for step-by-step information on how to edit protocol descriptions.

7 Troubleshooting

If you see an error message while loading a configuration file

If you load a configuration filewith the probe powered off, or not connected or incorrectly connected to the analyzer pods, the communication with the probe will fail and you will see an error message.

- ✔ Check that the probe is powered on.
- ✔ Check that the probe is connected to the logic analysis system.

If the last packet in the Packet Viewer has an error

The logic analyzer stops storing information when its memory is filled or when the analyzer halts. This will often result in the last packet being cut off before it has been completely captured. This in turn causes the Packet Viewer to display the message, "Unexpected End Of Packet" at the end of the trace.

If triggers are sometimes missed

If you are sure that the condition you want to trigger on is occuring, but the logic analyzer fails to trigger:

- ✔ Check that the trigger has been set up correctly.
- ✔ If the sample position is not “100% prestore”, check that Force Prestore is not enabled.

To run the built-in self test

1. In the logic analysis system, open the N4850A acquisition probe’s Self Test dialog.
2. Select the appropriate test.
3. Follow the directions listed for the test.
4. Click Run Self Test. The results of the test will be displayed.

If an error occurs during Self Test, select "Enable Log to File" and choose a file name, then run the test again.

If SysClk is not being acquired correctly

If SysClk is AC coupled at the source, you must also place a DC blocking capacitor after the point where the acquisition probe is connecting to the signal. See the *Agilent N4850A/N4860A Digital Probes Design Guide* for more information.

If you see “SpeedMismatch” errors

If you see “SpeedMismatch” in the SpeedErr column of the listing, it means that the N4850A acquisition probe is receiving data at a different rate than what the probe expects (see “Configuring the clock speed” on page 23).

When the SpeedErr column (for either RX or TX) shows “SpeedMismatch,” it is possible that other errors will also show up.

For example, if the protocol set the speed to 312 Mbps, but the data was sent out at SYSCLK/4 speed, the analyzer will capture the data correctly, but also generate a "OutOfFrameData" line. This is because the Sync word, at SYSCLK/4 speed, takes so long to be recognized as a Sync word compared to how fast it should be recongized as a Sync word at 312 Mbps, that the error status is generated before the system recognizes the Sync word at the incorrect frequency.

If no data is being acquired by the logic analyzer

- ✔ Check that the probe is connected to the correct signals.
- ✔ Check that the logic analyzer is set to trigger on something which you are certain will occur.
- ✔ Use an oscilloscope to check all of the signals while the probe is connected. Check the signal quality. Also check that the probe is not pulling up the center voltage for the differential signals.

If packet payloads contain incorrect data

Check that you have correctly configured the size of the user-defined payloads ("To configure payload and miscellaneous settings" on page 25). If a user-defined payload on the DUT is longer than what the probe is configured for, the Sync of the next payload will be captured as part of the payload for the preceding packet.

If no packets are shown in the Packet Viewer

If the DUT has link or signalling problems, no packets will be displayed. Instead, the Packet Viewer will continue searching the captured data for a packet to display.

Use the Listing display to confirm that this is the case. In the Listing display:

- ✔ Is any data being captured? If not, see "If no data is being acquired by the logic analyzer" on page 73.
- ✔ Do you see any packet headers? Remember, the Sync fields are not captured by the logic analyzer.

If you see packets in the Listing display but not in the Packet Viewer display:

- ✔ If the packets are different in any way from standard DigRF v3 packets, you may need to customize the protocol definition file which is used by the Packet Viewer. See "Customizing the Protocol" on page 67.
- ✔ In the Overview display, check that the Packet Viewer is connected to the correct logic analyzer.

Understanding the LEDs

Each of the six LEDs on the front of the N4850A acquisition probe can be green, amber, or red.

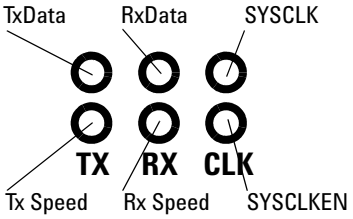


Figure 6 Names of the status LEDs

Table 11 What the colors of the LEDs mean

	TxData	**RxData**	**SYSCLK**
Green	Toggling, synced	Toggling, synced	Toggling, synced
Flashing green			
Amber			Toggling, no SysClkEn
Red	Toggling, not synced	Toggling, not synced	Bad input frequency
Flashing red	Illegal sleep condition	Illegal sleep condition	
Off	Data idle, no activity	Data idle, no activity	No SysClk and no SysClkEn
	Tx Speed	**Rx Speed**	**SYSCLKEN**
Green	312 Mbps	312 Mbps	Enabled (high)
Flashing green		SysClk	
Amber	SysClk/4	SysClk/4	
Red	SysClk (illegal speed)		
Flashing red			
Off	Unknown speed	Unknown speed	Disabled (low)

What to look for

When you connect the acquisition probe to the DUT, check the following things:

- ✔ Check SYSCLK and SYSCLKEN first (the two CLK LEDs). Both of these LEDs should be steady green.
- ✔ Check TxData and RxData (the top TX and RX LEDs). Both of these LEDs should be steady green, flashing green, or off.
- ✔ Look for red or “hints of red.”

  Red is always “bad.”

  Amber is combination of red and green. It can be difficult to see a difference difference between amber and intermittent red. But if everything is connected properly, you should not see amber for TxData and RxData.

Updating the Firmware

You can update the FPGAs in the probe by sending new configurations over the analyzer cables. It takes up to 60 minutes (the FLASH memory erase time is variable) to update the FPGAs. This should only be done when requested by Agilent.

1. Copy the new firmware to the logic analysis system. Save the files in the following directory:

```
C:\Program Files\Agilent Technologies\Logic Analyzer\AddIns\
   Agilent\N4850A\FPGA
```

2. Check that the N4850A acquisition probe is turned on and connected to the logic analysis system.
3. Open the N4850/60A DigRFv3 probe Properties dialog.
4. Select the **Update FPGA** tab.
5. Select the module you wish to update and then which FPGA version you want to use.
6. Click **Update FPGA**.

8 Characteristics — N4850A

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics.

Table 1 N4850A Connectors

Connector	Characteristics
Input	Connectors for use only with an Agilent probe. Maximum data rate: 312 Mbps Minimum voltage swing: Complies with DigRF v3 requirements Installation category: CAT I (Mains isolated)
Logic Analyzer Pod Outputs	Two 38-pin Samtec connectors
SMA S0, S1	SMA connector. (Input/output function configured as output-only in firmware). Min: 0.8V, Max: 3.3V, Max current 24mA DC-50 MHz. CAT I (Mains isolated)
DATA CLOCK	SMA Output. Min: 0.8V, Max:3.3V, Max current 24mA 10-160 MHz.
CTS	SMA Output. Min: 0.8V, Max: 3.3V, Max current 24mA DC-50 MHz.

Table 1 N4850A Connectors

Connector	Characteristics
Option Connector	Reserved for use with compatible Agilent products.

Table 2 Electrical Characteristics

Electrical Characteristics	
Power Requirements (Power Supply)	Input: 100-240 V, 1.5 A, 50/60 Hz, IEC 320 connector Output: 12 V, 5 A
Power Requirements (N4850A Probe)	Input: 12 V DC, 5 A. Use only with the provided power supply.
Load Model	See the documentation for the probe you are using.

Table 3 Mechanical Characteristics

Mechanical Characteristics	
Analysis Probe Dimensions	See "Positioning the Probe" on page 31 for ventilation requirements.

Table 3 Mechanical Characteristics

Mechanical Characteristics

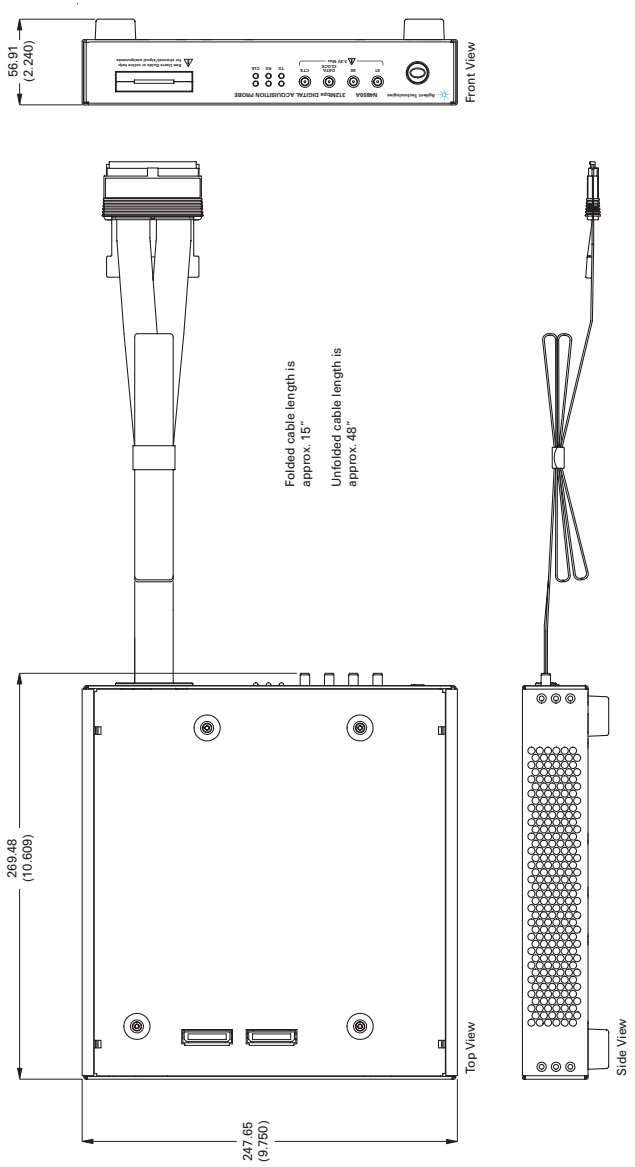


Table 3 Mechanical Characteristics

Mechanical Characteristics	
Weight	Probe: 2.0 kg (4.4 lb), not including power supply

Table 4 Environmental Characteristics (Operating)

Environmental Characteristics (Operating)	
Temperature	Operating/non-operating: +0° to +55° C (+32° to +131° F)
Altitude	Operating/nonoperating 3000 m (10,000 ft)
Humidity	8 to 80% relative humidity at 40° C (104° F).
	Avoid sudden, extreme temperature changes which could cause condensation on the circuit board. For indoor use only.
	Pollution degree 2: Normally only dry non-conductive pollution occurs. Occasionally a temporary conductivity caused by pollution may occur.

9 Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 61010-1, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.
- If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.
- Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.

- Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not use the instrument in a manner not specified by the manufacturer.

To clean the instrument

If the analysis probe requires cleaning: (1) Remove power from the instrument. (2) Clean the external surfaces of the instrument with a soft cloth dampened with a mixture of mild detergent and water. (3) Make sure that the instrument is completely dry before reconnecting it to a power source.

Do not clean the cables.

Safety symbols

"Caution" or "Warning" risk of danger marked on product. See "Safety Notices" on page 2 and refer to this manual for a description of the specific danger.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

10 Glossary

For more terms, see the glossary in the logic analysis system's online help.

Bus A bus is a group of associated signals within the logic analysis system.

Card A logic analyzer, oscilloscope, or pattern generator that can be inserted into a slot in logic analysis system frame. Cards can be combined with others to increase the channel count available in a single time domain.

Deskew To cancel or nullify the effects of differences between two different internal delay paths for a signal. Deskewing is normally done by running eye finder.

DUT Device Under Test—the board containing the RF IC or baseband IC which you are testing.

Eye Finder A logic analyzer feature which trains the logic analyzer to sample each signal at the moment that it is most likely to be stable.

Intermodule Bus The intermodule bus (IMB) is a bus in the frame that allows the measurement modules to communicate with each other. Using the IMB, you can set up one instrument to *arm* another. Data acquired by instruments using the IMB is time-correlated.

Intermodule Intermodule is a term used when multiple instrument tools are connected together for the purpose of one instrument arming another. In such a configuration, an arming tree is developed and the group run function is

designated to start all instrument tools. Multiple instrument configurations are done in the Intermodule window.

Label See *Bus*.

Markers Markers are the green and yellow lines in the display that are labeled *x*, *o*, *G1*, and *G2*. Use them to measure time intervals or sample intervals. Markers are assigned to patterns in order to find patterns or track sequences of states in the data. The x and o markers are local to the immediate display, while G1 and G2 are global between time correlated displays.

Master Card In a module, the master card controls the data acquisition or output. The logic analysis system references the module by the slot in which the master card is plugged. For example, a 5-card Agilent Technologies 16555D would be referred to as Slot C: machine because the master card is in slot C of the mainframe. The other cards of the module are called expansion cards.

Module A logical collection of logic analyzer cards that are connected together. This gives you the flexibility to increase channel count by using more than one card. A module can be a single card or several cards, and a single card or several card module can be split into two modules. By definition, a module consists of a single time domain. While a module can consist of a single card, a module is not a physical entity. When a module has more than one card, one card is set up as the *master card*.

Pod Each of the cables coming out of the logic analyzer card is called a **pod**.

Probe A device to connect the various instruments of the logic analysis system to the device under test.

The word “probe” is used in three ways in this manual:

- The Agilent N4850A digital acquisition probe and N4860A digitial stimulus probe are always referred to as “acquisition probe” and “stimulus probe,” respectively.
- An Agilent probe connects the cables from the logic analyzer to the Samtec connectors on the N4850A acquisition probe. This probe is referred to as a “probe adapter.”
- An Agilent probe connects the N4850A acquisition probe to your DUT. This is referred to as a “probe.”

Probe Adapter See *probe*.

Sample Position The position of the logic analyzer’s setup/hold window for a particular channel, relative to the bus clock.

Skew Skew is the difference in channel delays between measurement channels. Typically, skew between modules is caused by differences in designs of measurement channels, and differences in characteristics of the electronic components within those channels. You should adjust measurement modules to eliminate as much skew as possible so that it does not affect the accuracy of your measurements.

State Measurement In a state measurement, the logic analyzer is clocked by a signal from the system under test. Each time the clock signal becomes valid, the analyzer samples data from the system under test. Since the analyzer is clocked by the system, state measurements are synchronous with the test system.

Storage Qualification Storage qualification is only available in a state measurement, not timing measurements. Store qualification allows you to specify the type of information (all samples, no samples, or selected states) to be stored in memory. Use store qualification to prevent memory from being filled with unwanted activity such as no-ops or wait-loops. To set up storage qualification, use “Trigger

and fill memory with Default Storage" in a logic analyzer trigger sequence. In contrast, filters can hide data after it has been collected.

Symbol Symbols represent patterns and ranges of values found on logic analyzer buses. Symbols come from several sources:
1) Object file symbols — Symbols from your source code, and symbols generated by your compiler. Object file symbols may represent global variables, functions, labels, and source line numbers.
2) User-defined symbols — Symbols you create.
3) Predefined symbols — Symbols defined in a supplied configuration file.

Target System The device under test.

Timing Measurement In a timing measurement, the logic analyzer samples data at regular intervals according to a clock signal internal to the timing analyzer. Since the analyzer is clocked by a signal that is not related to the system under test, timing measurements capture traces of electrical activity over time. These measurements are *asynchronous* with the test system.

Trace All of the data captured by a run of the logic analyzer. Also called an "acquisition."

Trigger Trigger is an event that occurs immediately after the instrument recognizes a match between the incoming data and the trigger specification. Once trigger occurs, the instrument completes its *acquisition*, including any store qualification that may be specified.

Trigger Sequence A trigger sequence is a sequence of events that you specify. The logic analyzer compares this sequence with the samples it is collecting to determine when to *trigger*.

Trigger Specification A set of conditions that must be true before the instrument triggers. See the printed or online documentation of your logic analyzer for details.

Y Adapter Cable See *probe*.

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