

Service Guide

Agilent Technologies 8719D/20D/22D Network Analyzers



Agilent Technologies

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Hewlett-Packard to Agilent Technologies Transition

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Service Guide
HP 8719D/20D/22D
Network Analyzer



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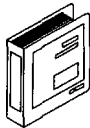
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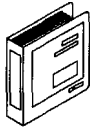
The **Installation** and Quick Start Guide **familiarizes** you with the network analyzer's front and rear panels, electrical and environmental operating **requirements**, as well as **procedures** for **installing, configuring, and verifying** the operation of the **analyzer**.



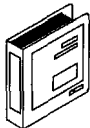
The **User's Guide** shows how to make **measurements**, explains commonly-used features, and **tells** you how to get the most **performance** from your **analyzer**.



The Quick Reference Guide **provides** a summary of all available user features.



The **Programmer's** Guide **provides programming information** including an HP-IB **command** reference, an HP-IB **programming reference**, as well as **programming** examples.



The **Service Guide** provides information **to adjust**, troubleshoot, **repair, and verify conformance** to published specifications. Available **with** Option OBW.

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Service Equipment and Analyzer Options

This chapter contains information on the following topics:

- Service **Tools**
- Service **Test** Equipment
- Principles of Microwave Connector Care
- Analyzer Options
- Service and Support Options

Table of Service **Test** Equipment

Table 1-1. Required Tools

<p>T-8, T-10, T-15 and T-25 TORX screwdrivers</p> <p>Flat-blade screwdrivers-small, medium, and large</p> <p>5/16-inch open-end torque wrench (for SMA nuts)</p> <p>3/16, 5/16, and 9/16-inch hex nut drivers</p> <p>5/16-inch open-end torque wrench (set to 10 in-lb)</p> <p>2.5-mm hex-key driver</p> <p>Soldering iron</p> <p>Non-conductive and non-ferrous adjustment tool</p> <p>Needle-nose pliers</p> <p>Tweezers</p> <p>Antistatic work mat with wrist-strap</p>
--

Table 1-2. Service Test Equipment (1 of 2)

Required Equipment	Critical Specifications	Recommended Model	Use
Frequency Counter	Freq:0.050 to 20 GHz Accuracy:3 ppm	HP 5843A, 5850B, 5851B	P,A,T
Frequency Counter (HP 8722D Only)	Freq:0.050 to 26.6 GHz Accuracy:3 ppm	HP 5851B	P,A,T
Spectrum Analyzer	Freq: 100 Hz to 22 GHz	HP 8566B, 8568E	P,A,T
Power Meter	Range:-30 to +15 dBm Accuracy:±0.05 dB	HP 436A, 438A, 437B*	P,A,T
Power Sensor (HP 8719D/20D Only)	Freq:0.050 to 20 GHz Range:-30 to +20 dBm	HP 8485A	P,A,T
Power Sensor (HP 8722D Only)	Freq:0.050 to 40 GHz Range:-30 to +20 dBm	HP 8487A	P,A,T
Digital Voltmeter	Resolution:10 mV	Any	T
Oscilloscope	Bandwidth:100 MHz	Any	T
Printer	Rastergraphics capability	HP 660	P
Photometer	Elektronix J16	T	
Photometer Probe	Elektronix J6503	T	
Light Occluder	Elektronix 016-0805-00	T	
External Keyboard	PC-AT-compatible with standard DIN connector ¹	HP C1405A (Option ABA)	A
Keyboard Adaptor		C1405-60015	A
Adapter (HP 8719D/20D Only)	3.5 mm to Type-N (f) connectors	HP 11525A	A
Adapter (HP 8722D Only)	2.4 mm to 7 mm connectors	HP 85180E	A
Adapter (HP 8722D Only)	Type-N (f) to 7 mm connectors	HP 11524A	A

¹ HP 437A can also be used for the HP 8722D. HP 437B or 438A is required for power meter calibration.

P - Performance Tests

A - Adjustment

T - Troubleshooting

1 Keyboards with a mini-DIN connector are compatible with the HP P/N C1405-60015 adaptor.

Table 1-2. Service Test Equipment (2 of 2)

Required Equipment	Critical Specifications	Recommended Model	Use
ExtensionCables	SMB (m) to SMB (f)	HP P/N 8120-5040	A , T
Extension Cables	SMB(f) to BNC (m)	HP P/N 8120-5048	A , T
Coax Cable	BNC (m) to BNC (m), 50Ω	HP 10503A	A
BP-IB Cables		HP 10833A/B/C/D	P,A
BP Cable	Type-N connectors, 50ohm, 24-inch	HP P/N 8120-4781	A
RF Cable Set	3.5mm connectors	HP 85181C/D/E/F	P,A,T
RF Cable Set	7mm connectors	HP 85182D/F	P,A
BP Cable Set	Type-N connectors	HP 85182D/F	P,A
RF Cable Set (HP 8722D Only)	2.4mm connectors	HP 85183D/E/F	P,A,T
Tbol Kit	No substitute	08722-60018	A,T
2.4mm Calibration Kit (HP 8722D Only)	No substitute	HP 85056A/D	P,A,T
2.4mm Verification Kit (HP 8722D Only)	No substitute	HP 85057B	P
3.5mm Calibration Kit	No substitute	HP 85052B/D	P,A,T
3.5mm Verification Kit¹	No substitute	HP 85053B	P
7 mm Calibration Kit	No substitute	HP 85050B/D	P,A,T
7 mm Verification Kit (HP 8719D/20D Only)	No substitute	HP 85051B	P
Type-N Calibration Kit	No substitute	HP 85054B/D	P,A,T
Type-N Verification Kit (HP 8719D/20D Only)	No substitute	HP 85055A	P
Floppy Disks	3.5-inch	HP 92192A (box of 10)	A
Tbol Kit		08722-60018	A
P - Performance Tests A - Adjustment T - Troubleshooting			

¹ Verification can only be done up to 26.5 GHz on the HP 8722D while using the 3.5 mm Verification Kit.

Principles of Microwave Connector Care

Proper connector care and connection techniques are critical for accurate, repeatable measurements

Refer to the calibration kit documentation for connector care information. Prior to making connections to the network analyzer, carefully review the information about inspecting, cleaning and gaging connectors

Having good connector care and connection techniques extends the life of these devices. In addition, you obtain the most accurate measurements

This type of information is **typically** located in Chapter 3 of the calibration kit **manuals**.

For additional connector care instruction, contact your local Hewlett-Packard Sales and Service **Office** about course numbers HP **85050A + 24A** and HP **85050A + 24D**.

See the following table for quick reference tips about connector care.

Table 1-3. Connector Care Quick Reference

Handling and Storage	
Do	Do Not
Keep connectors clean Extend sleeve or connector nut Use plastic end-caps during storage	Touch mating-plane surfaces Set connectors contact-end down
Visual Inspection	
Do	Do Not
Inspect all connectors carefully Look for metal particles, scratches, and dents	Use a damaged connector-ever
Connector Cleaning	
Do	Do Not
Try compressed air first use isopropyl alcohol Clean connector threads	Use any abrasives Get liquid into plastic support beads
Gaging Connectors	
Do	Do Not
clean and zero the gage before use Use the correct gage type Use correct end of calibration block Gage all connectors before first use	Use an out-of-spec connector
Making Connections	
Do	Do Not
Align connectors carefully Make preliminary connection lightly Turn only the connector nut Use a torque wrench for final connect	Apply bending force to annexion Over tighten preliminary connection Twist or screw any connection Tighten pest torque wrench "break" point

Analyzer Options Available

Option **1D5**, High Stability Frequency Reference

Option **1D5** offers ± 0.05 ppm temperature stability from 0 to 56 °C (referenced to 25 °C).

Option 007, Mechanical Transfer Switch

This option replaces the solid state transfer switch with a mechanical switch in the test set, providing the instrument with greater power handling capability. Because the mechanical transfer switch has less loss than the standard switch, the output power of Option 007 instruments is 5 dB higher.

Option **085**, High Power System

This option is designed to permit the measurement of high power devices. With an external power amplifier, this **configuration will** allow up to 20 Watts (+43 dBm) of output at the test **ports**. The maximum test port input power is 1 Watt (+30 dBm) CW, but jumpers on the front panel allow the insertion of high power attenuators or isolators. This allows test device output levels up to the power limits of the inserted components. Additionally, there is an external reference input that allows the external **amplifier's** frequency response and drift to be **ratiored** out, and there are internally controlled step attenuators between the couplers and samplers to prevent overload. A network analyzer with this option can be **configured** to operate as a normal instrument (with slightly degraded output power level and accuracy) or as an instrument capable of making **single** connection multiple measurements. Because of high output power, option **085** is only available with a mechanical **transfer** switch similar to Option 007.

Option 089, Frequency **Offset** Mode

This option adds the ability to offset the source and receiver frequencies for frequency translated measurements. **This** provides the instrument with mixer measurement capability. It also provides a graphical setup that allows easy **configuration** of your mixer measurement.

Option 012, Direct Access Receiver Configuration

This option provides front panel access to the A and B samplers. This allows direct access to the sampler inputs for improved sensitivity in applications such as antenna tests, or for the insertion of attenuators between the couplers and samplers to allow measurements of up to 1 Watt (+ 30 **dBm**) at the input of the test **ports**. Direct access to the B sampler provides a test configuration for the HP **8722D** that gives increased dynamic range in the forward direction.

Option 400, Four-Sampler **Test Set**

This option reconfigures the instrument's test set to ratio out the characteristics of the test port transfer switch, and to include a second reference channel that allows full accuracy with a **TRL** measurement calibration.

Option 010, Time Domain

This option allows the analyzer to display the time domain response of a network by computing the inverse **Fourier** transform of the frequency domain response. The analyzer shows the response of a test device as a function of time or distance. Displaying the reflection **coefficient** of a network versus time determines the magnitude and location of each discontinuity. Displaying the **transmission coefficient** of a network versus time determines the characteristics of individual **transmission** paths. Time domain operation retains all accuracy inherent with the active error correction.

Option **1CM**, Rack Mount Flange Kit Without Handles

Option **1CM** is a rack mount kit containing a pair of **flanges** and the necessary hardware to mount the instrument, with handles detached, in an equipment rack with 482.6 mm (19 inches) horizontal spacing.

Option **1CP**, Rack Mount Flange Kit With Handles

Option **1CP** is a rack mount kit containing a pair of flanges and the necessary hardware to mount the instrument with handles attached **in** an equipment rack with 482.6 mm (19 inches) spacing.

Service and Support Options

The analyzer automatically includes a one-year on-site service warranty, where available. If on-site service is not available in your local area, you can purchase the analyzer with a **W08** option instead, which converts the one year on-site warranty to a three year return to HP warranty. Consult your local Hewlett-Packard sales engineer for availability of on-site service.

The following service and support options are available at the time you purchase an HP **8719D/20D/22D** network analyzer.

Option **W08**

This option converts the one year on-site warranty, that was automatically included with your analyzer, **to** a three year return to HP warranty. This option does not include calibration.

Option **W31**

This option adds two years of on-site repair to the product warranty, providing three years of repair coverage. This option does not include calibration.

Option **W51**

This option adds four years of on-site repair to the product warranty, providing five years of repair coverage. This option does not include calibration.

Option **W32**

This option provides three years of return to HP calibration service. The calibration provided is traceable to national standards

Option **W52**

This option provides **five** years of return to HP calibration service. **The** calibration provided is traceable to national standards

Option **W34**

This option provides three years of return to HP Standards Compliant Calibration. This type of calibration meets the **ANSI/NCSL Z540-1-1994** standard.

Option **W54**

This option provides five years of return to HP Standards Compliant Calibration. This type of calibration meets the **ANSI/NCSL Z540-1-1994** standard.

If support was not purchased along with the analyzer, there are many repair and calibration options available from Hewlett-Packard's support organization. These options cover a range of on-site services and agreements with varying response times as well as return to HP agreements and per-incident pricing. Contact your local Hewlett-Packard customer engineer for details.

System Verification and Performance Tests

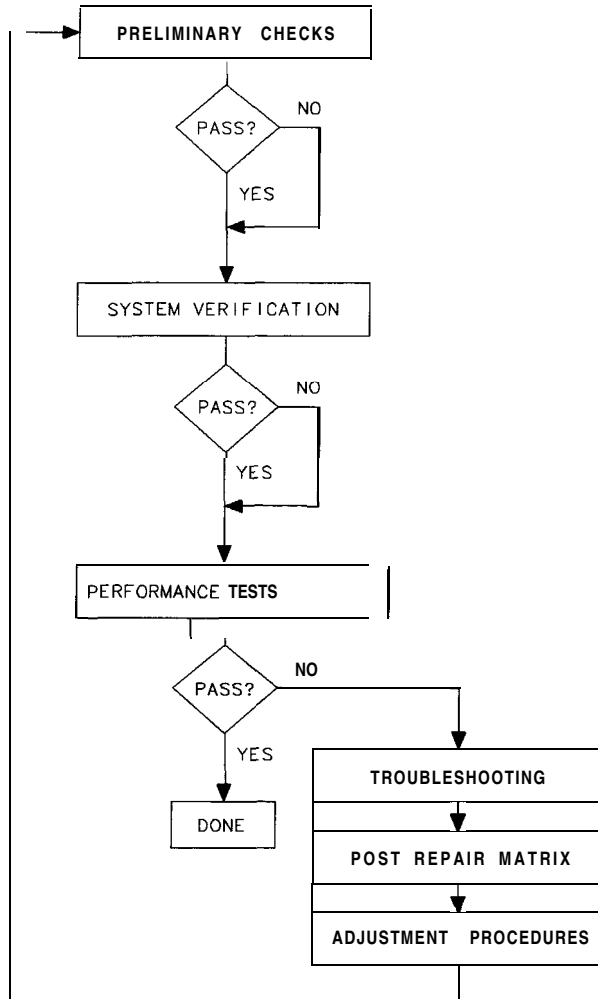
How to **Test** the Performance of Your Analyzer

There are two different ways to verify the performance of your analyzer. One method meets **ANSI/NCSL Z540-1-1994** standards, and the other method does not. To determine which type of verification you wish to perform, refer to the following descriptions and flow **charts**.

- **ANSI/NCSL Z540-1-1994 verification** consists of conducting the **preliminary** checks, system verification, and the performance tests without stopping to troubleshoot along the way. Exceptions will only be made in case of catastrophic **failure** or cable connector damage. In order to obtain data of how the analyzer was performing at the **time of verification**, these tests must be done even if you are aware that the instrument will not **pass**. Obtaining the data (system verification printout and performance test record) at this point is necessary so that customers will understand that their measurements may not have been accurate. A technician must wait until after the **ANSI/NCSL Z540-1-1994** verification is complete before troubleshooting and repairing any problems. After troubleshooting, the “Post-Repair Procedures” matrix in Chapter 3 will direct the technician to perform the necessary adjustment procedures. Then the technician will repeat the system verification and performance tests, generating a new set of data.
- **Non-ANSI/NCSL Z540-1-1994** verification consists of conducting the **preliminary** checks, system verification, and performance tests, but stopping at any point if the analyzer fails a test. The technician will troubleshoot and repair the first problem encountered without continuing to other tests. After troubleshooting, the “Post-Repair Procedures” matrix in Chapter 3 will direct the **technician** to perform the necessary adjustment procedures. Then the technician will repeat the system verification and performance tests. As the analyzer passes the system **verification** and all the tests, the **technician** will print out the system verification results and **fill** out the performance test record.

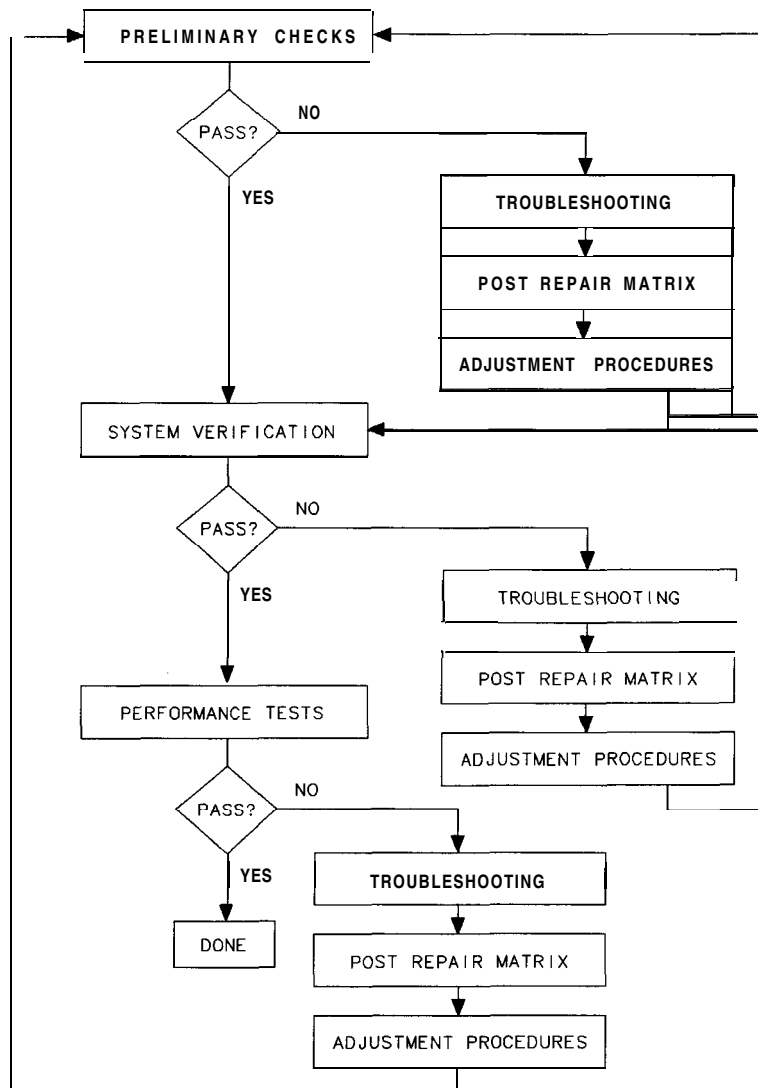
Instrument Verification Cycle

The performance of the network analyzer should be **verified** at least once per year.



sb636d

Figure 2-1. ANSI/NCSL Z540-1-1994 Verification Flowchart



sb637d

Figure 2-2. Non-ANSI/NCSL Z540-1-1994 Verification Flowchart

Sections in this Chapter

- **Preliminary Checks**
 - Check the Temperature and Humidity
 - Check the Analyzer Internal **Tests**
 - Run the Operation Check
 - Clean and Gage **all** Connectors
 - Check the **Test** Port Cables
- **System Verification**
 - Equipment Initialization
 - Measurement Calibration
 - Verification Device Measurements
 - Interpreting the **Verification** Results
- Performance **Tests**
 1. **Frequency Accuracy Test**
 2. Power Flatness **Test**
 3. Power Linearity **Test**
 4. Dynamic Range **Test**
- Performance **Test** Record

Preliminary Checks

Check the **Temperature** and Humidity

Required Equipment and Tools (HP 8719D/20D Only)

Calibration Kit	HP85052B/D
RF Cable Set	HP85131C/D
Verification Kit	HP 85053B

Required Equipment and Tools (HP 8722D Only)

Calibration Kit	HP85056A/D
RF Cable Set	HP 85133C/D
Verification Kit	HP85057B

Caution Use an antistatic work surface and wrist strap to lessen the chance of electrostatic discharge.

1. Measure the temperature and humidity of the environment and write the values on the "Performance **Test** Record." The performance is specified at an ambient temperature of **+23°C ±3°**. Therefore, the environmental **TEMPERATURE MUST** remain in the range of **+20°C to +26°C**. Once the measurement calibration has been done, the ambient temperature must be held to **±1°C**.
2. **Open** the calibration and verification kits and place all the devices on top of the foam so they will reach room temperature. **TEMPERATURE OF TEE DEVICES IS IMPORTANT** because device dimensions (electrical characteristics) change with temperature.
3. Switch on the power to the instrument.

Note **To achieve the** maximum system stability, allow the instrument to warm up for at least 1 hour

Check the Analyzer Internal **Tests**

This test is recommended to be done before the **performance** tests, but is not required.

To run the analyzer internal tests, press **[Preset] PRESET: FACTORY [Preset] [System] SERVICE MENU TESTS INTERNAL TESTS EXECUTE TEST**.

These quick, automated internal checks may save time by indicating an instrument fault before time is invested doing performance tests. Internal tests are described in the “Service Key Menus and Error Messages” chapter of this manual.

Run the Operation Check

1. Connect a short to port 1.
2. To run the first part of the operation check, press the following keys:

[Preset] PRESET: FACTORY [Preset] [System] SERVICE MENU TESTS [21] [x1] EXECUTE TEST CONTINUE

- If the **CONTINUE** softkey label appears on the display, that particular attenuator setting check has failed. Press **CONTINUE** to check the other attenuator settings
 - If the message FAIL appears on the analyzer display, the analyzer failed the **first** part of the operation check.
 - If the message DONE appears on the analyzer display, the analyzer passed the **first** part of the check.
3. Connect the short to port 2.
 4. To run the second part of the operation check, press the following keys:

[↑] EXECUTE TEST CONTINUE

- If the **CONTINUE** softkey label appears on the display, that particular attenuator setting check has failed. Press **CONTINUE** to check the other attenuator settings
- If the message FAIL appears on the analyzer display, the analyzer failed the first part of the operation check.

- If the message DONE appears on the analyzer display, the analyzer passed the **first** part of the check.

Clean and Gage All Connectors

Caution If connectors are damaged, *they must be repaired or replaced NOW* in order to prevent damage to the calibration and **verification** kit devices Always use adapters when verifying a system with SMA connectors

1. Visually inspect all the connectors for any burrs, gold flakes, or places where the gold is worn.

Clean all the connectors with alcohol and foam-tipped swabs Dry the connectors with dry foam-tipped swabs

2. Visually inspect the calibration block and the end of the connector gage before any measurements of the connectors are made.
3. Gage all devices, cables, and test port connectors.

Note **The** procedures for correct use of gages are in the calibration kit **manuals.**

Check the Test **Port** Cables

The following series of cable tests (return loss, insertion loss, magnitude stability, phase stability, and connector repeatability) can be done to check the stability of a test port cable. These checks are not required, but are recommended to avoid spending a considerable amount of time on the **verification** only to have a failure caused by the cables.

Return Loss of Cables

1. Press **Preset** **Menu** **SWEEP TIME MENU** **STEP SWP ON** to activate step sweep.
2. Perform an **S₁₁** 1-port measurement calibration at test port 1. Use a **lowband** and sliding load combination, or a broadband load for the loads portion of the calibration. If necessary, refer to the operating manual for a detailed measurement calibration procedure.

Note	If the fixed load in your calibration kit is labeled BROADBAND, you can use this load in the lowband portion of the measurement calibration.
------	--

3. Connect the test port cable to port 1 and tighten to the specified torque for the connector type.
4. Connect a broadband termination to the end of the cable.
5. **To** measure the return loss over the entire specified band, press **Marker Fctn** **MR SEARCH** **TRACKING ON** **MAX** to activate the marker search tracking and find the worst case **S₁₁** measurement.

See **Figure 2-3** for an example of a return loss measurement. Refer to the cable manual to see if the cable meets the return loss specification. If it doesn't, the cable should be either repaired or replaced.

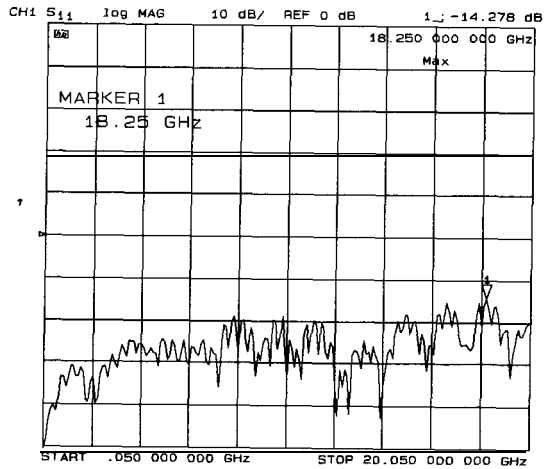


Figure 2-3. Return Loss Measurement of Cables

Insertion Loss of Cables

1. Replace the load with a short.
2. To measure the insertion loss of the cable over the entire **specified** band, press **TRACKING OFF** **Marker**, and turn the front panel knob, to switch off tracking and look for the worst case measurement. Rower holes **>0.5 dB** indicate a bad cable See **Figure 2-4** for example insertion loss measurements of a good cable. Refer to the cable manual to see if the cable you are measuring meets its insertion loss **specification**. If it doesn't, the cable should be either repaired or replaced.

In this S_{11} measurement, the displayed trace results from energy being propagated down the cable and reflected back from the short. Therefore, the correct insertion loss is approximately the measured value divided by 2 (one-way path loss of the cable).

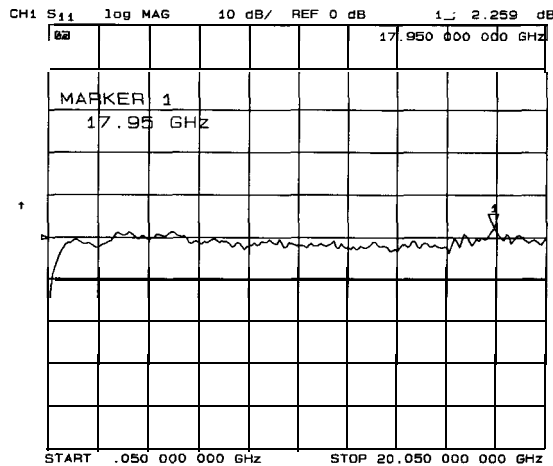


Figure 2-4. Insertion Loss Measurements of Cables

Magnitude and Phase Stability of Cables

1. To measure magnitude and phase stability, press the following keys on the analyzer:

Display **DUAL CHANNEL**
Avg **AVERAGING FACTOR** **64** **x1** **AVERAGING**
Chan 2 **Meas** **Ref1: P4D S11 (A/R)** **Format** **PHASE**
Avg **AVERAGING FACTOR** **64** **x1** **AVERAGING**

2. Connect a short at the end of the cable and then wait for the analyzer to average the measurement 64 times
3. Hold the cable in a straight line, and press the following keys to normalize the displayed traces:

Chan 1 **Display** **DATA → MEMORY** **DATA / MEM**
Chan 2 **Display** **DATA → MEMORY** **DATA / MEM**

4. Make a gradual 90° bend in the middle of the cable and restart the measurement averaging by pressing **Avg** **AVERAGING RESTART**.

5. To change the scale of the displayed traces, press:

Chan 1 **Scale Ref** **SCALE/DIV** **↓** (repeat arrow key)
Chan 2 **Scale Ref** **SCALE/DIV** **↓** (repeat arrow key)

6. To mark the end of the cable's specified range, place a marker on the highest **specified** frequency of the cable. Press: **Marker** (enter the **specified** frequency) **G/n**.

- Place a marker on the largest deflection that goes above and below the reference line and is within the **specified** frequency range. See **Figure 2-5** for example plots of this measurement.

In this S_{11} measurement, the displayed trace results from energy being propagated down the cable and reflected back from the short. Therefore, the measured deflection value must be divided in half to reach the correct value. If the cable does not meet the **specifications** in the cable manual, it should be either repaired or replaced.

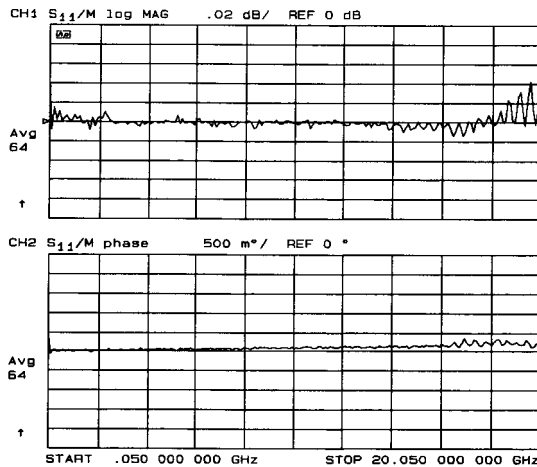


Figure 2-5. Cable Magnitude and Phase Stability

Cable Connector Repeatability

- To measure the cable connector repeatability, connect a broadband termination at the end of the cable.
- Press the following keys on the analyzer:

Chan 1 Display DUAL CHANNEL DISPLAY DATA
Avg AVERAGING FACTOR 128 x1

Wait until the analyzer has averaged the measurement 128 times

3. To normalize the data trace press:

Display **DATA → MEMORY** **DATA → MEM**

Scale Ref **REFERENCE VALUE** **−50** **x1**

SCALE/DIV **20** **x1**

4. Disconnect and then reconnect the cable to the test port. Tighten the connection to the **specified** torque for the connector type. Look at trace for spikes or modes

5. To re-normalize the data trace of the reconnected cable press: **Display**

DATA → MEMORY

- Repeat steps 4 and 5 at least 3 times to look for modes. Modes appear when a harmonic of the source fundamental frequency is able to propagate through the cable or connector. It is helpful to be able to plot the trace each time to compare several connections. If any mode appears each time the cable is connected and reconnected, measurement integrity will be affected. The cable connector and/or cable should be repaired or replaced. Refer to the example plot in Figure 2-6.

Note The connector repeatability measurement should be done at the test port as well as at the end of the test port cable.

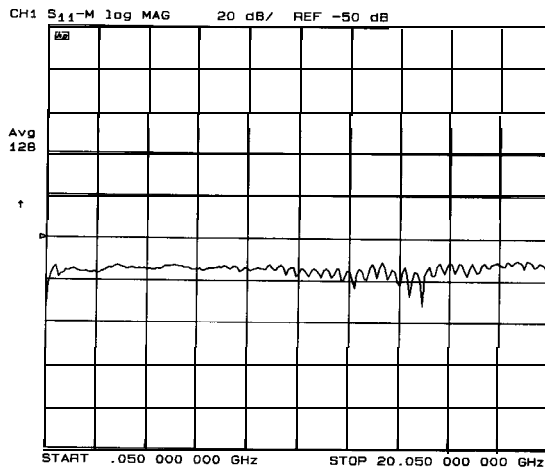


Figure 2-6. Connector Repeatability Example

System **Verification**

This system **verification** consists of four separate procedures:

1. Equipment Initialization
2. Measurement Calibration
3. **Verification** Device Measurement
4. Interpreting the **Verification** Results

The procedures consist of equipment initialization, calibrating the analyzer with a calibration kit, measuring a set of characterized devices, and comparing the resultant measured data to the data and uncertainty **limits** supplied with the verification kit.

The device data provided with the **verification** kit has a traceable path to a national standard. The difference between the supplied traceable data and the measured data must fall within the total uncertainty limits at all frequencies for the system verification to pass

The total measurement uncertainty limits for the system **verification** are the sum of the factory measurement uncertainties for the verification devices and the uncertainties associated with the system being **verified**. **You** can determine what your system measurement uncertainty limits are by referring to ‘Determining System Measurement Uncertainties’ located in Appendix A, at the end of this manual.

When an HP **8719D/20D/22D** system passes this test, it does not ensure that the system meets all of the performance **specifications**. However, it does show that the system being **verified** measures the same devices with the same results as a factory system which has had all its **specifications verified** and its total measurement uncertainty has been **minimized** to the smallest extent possible.

Verification Kit

A **verification** kit is used **in** the following procedure, The kit consists of two attenuators, a **25 Ω** mismatch **airline**, a **50 Ω** **airline**, a data disk containing the

factory measured verification data, uncertainty limits of an HP 8719D/20D/22D system, and a printout of the factory uncertainties for the devices in the kit.

Measurement Uncertainty

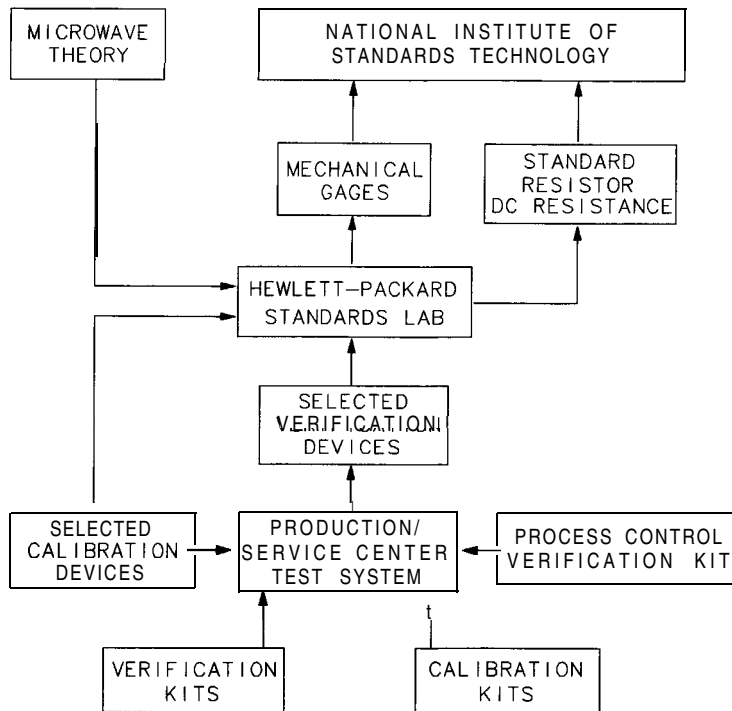
Measurement uncertainty is defined as the sum of the residual systematic (repeatable) and random (non-repeatable) errors in the measurement system after accuracy enhancement. The systematic errors are directivity, source match, load match, reflection and **transmission** frequency tracking, and isolation (crosstalk). Random errors include errors due to noise, drift, connector repeatability, and test cable stability. A complete description of system errors and how they affect measurements is provided under the “What is Measurement Calibration?” section of Chapter 6 in the HP *8719D/20D/22D Network Analyzer User’s Guide*.

Any measurement result is the vector sum of the actual test device response **plus** all error terms. The precise effect of each error term depends on its magnitude and phase relationship to the actual test device response. When the phase of an error response is not known, phase is assumed to be worst case (-180 to + 180 °). Random errors such as noise and connector repeatability are generally combined **in** a root-sum-of-the-squares (**RSS**) manner. **For** more information on determining measurement uncertainties, refer to Appendix A, “Determining System Measurement Uncertainties ”

Measurement Traceability

To establish a measurement traceability path to a national standard for a network analyzer system, the overall system performance is **verified** through the measurement of device characteristics that have a **traceability** path. This is accomplished by electrically measuring devices in an HP **verification** kit.

The measurement of the **verification** kit device characteristics has a traceable path because the factory system that characterizes the devices is calibrated and verified by measuring standards that have a traceable path to the National Institute of Standards and **Technology (NIST)**, see **Figure 2-7**. This chain of measurements **defines** how the verification process brings traceability to the HP **8719D/20D/22D** system measurements. Therefore, when your analyzer system is **verified** through the performance of the “System **Verification**” procedure, a measurement traceability path is established.



sb66d

Figure 2-7.
National Institute of Standards and Technology Traceability Path for
HP 8719D/20D/22D System Calibration and Verification Standards

What the System Verification Verifies

The system **verification** procedure **verifies** the minimum HP 8719D/20D/22D system, which **includes** the following:

- network analyzer
- calibration kit
- test port return cables

Note Additional equipment or accessories used with the above system are not **verified** by system verification.

Required Equipment and Accessories

The following equipment and accessories are required to verify the network analyzer system (for information on compatible printers, refer to the “Printing, Plotting, and Saving Measurement Results” chapter in the *HP 8719D/20D/22D Network Analyzer User’s Guide*.)

- HP 660 Printer (or other compatible printer)
- Centronics Interface cable (1)
- Verification Kit
- Calibration Kit
- RF Cable Set

Analyzer warm-up time: 1 hour

Table 2-1.
Supported System Configurations (HP 8719D/20D Only)

Description	3.5 mm	7 mm	Type-N
Calibration Kit	85052B/D	85050B/D	85054B/D
Verification Kit	85053A/B	85051A/B	85055A
Cables	85131D/F	85132D/F	85132D/F

Table 2-2.
Supported System Configurations (HP 8722D Only)

Description	2.4 mm	3.5 mm
Calibration Kit	85056B/D	85052B/D
Verification Kit	85057B	85053A/B
Cables	85133D/F	85131D/F

Cable Substitution. The test port cables specified for an HP 8719D/20D/22D system have been characterized for connector repeatability, magnitude and phase stability with flexing, return loss, insertion loss, and aging rate. Since the performance of test port cables is a very **significant** contributor to the system performance, substituting specified cables with cables of lower performance will increase the uncertainty of your measurement verification. Refer to the

plots in the cable checks (earlier in this chapter) that show the performance of good cables. It is highly recommended to periodically check test port cables to determine if they are good.

If the system **verification** is performed with non-HP cables and fails but is then repeated with HP cables and passes, the non-HP cables are at fault. (It must be documented in the comments area of the performance verification printout that non-HP cables were used in the system.) The effects of the non-specified cables cannot be taken into account in the performance **verification** procedure.

See supported system **configurations** in **Table 2-1** and **Table 2-2**.

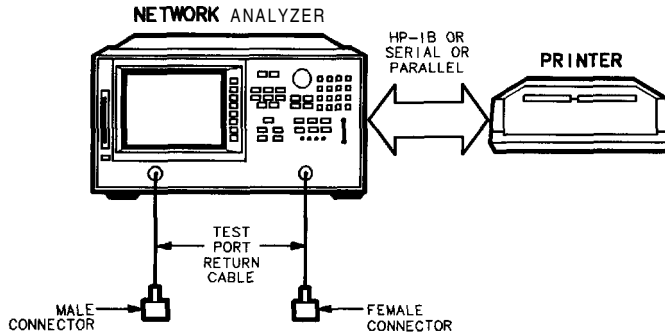
Calibration Kit Substitution. The accuracy of the analyzer when it is used with any calibration kit is dependent on how well the kit standards are **defined**.

The measurement **specifications** for the system assume a measurement calibration with an HP calibration kit. Measurement calibrations made with user defined or modified calibration hits are not subject to the performance specifications, although a procedure similar to the standard **verification** procedure may be used.

See supported system **configurations** in **Table 2-1** and **Table 2-2**.

Equipment Initialization

1. Connect the equipment as shown in **Figure 2-8**. Let the **analyzer** warm up for one hour.



sb67d

Figure 2-8. System **Verification Test** Setup

2. While the equipment is warming up, review the “Connector Care Quick Reference” information in the “Service Equipment and Analyzer Options” chapter. Good connections and clean, undamaged connectors are critical for accurate measurement **results**.
3. Insert the **verification** kit disk into the **analyzer** disk drive.
4. Press **(Preset)** **PRESET, FACTORY** **(Save/Recall)** **SELECT DISK** **INTERNAL DISK**.
5. If you want a printout of the verification data for all the devices, press **(System)** **SERVICE MENU** **TEST OPTIONS** **RECORD ON**. Also press **DUMP GRAPHICS ON** if graphs are also desired on test results print outs.

Note If you switch on the record function at this point, you **CANNOT** **switch** it off later during the verification procedure.

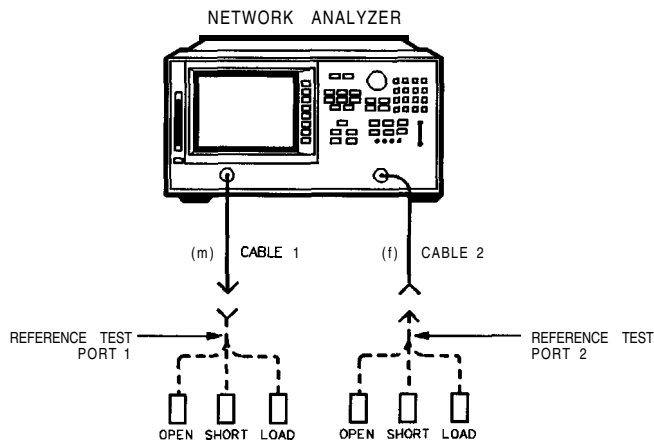
6. Position the paper in the printer so that printing starts at the top of the Page.
7. If you have **difficulty** with the printer:

- If the interface on your printer is **HP-IB**, verify that the printer address is set to 1 (or change the setting in the analyzer to match the printer).
 - If the interface on your **printer** is serial or parallel, be sure that you selected the printer port and the printer type correctly (refer to the *HP 8719D/20D/22D Network Analyzer User's Guide* for more information on how to perform these tasks).
8. Press **Cal** **CAL KIT** **SELECT CAL KIT** and select the type of calibration kit used.
 9. Press **System** **SERVICE MENU** **TESTS** **SYS VER TESTS** **EXECUTE TEST**.
 10. The analyzer displays Sys **Ver Init** DONE when the initialization procedure is complete

Caution At this point, **DO NOT** press **Preset** **PRESET: FACTORY** or recall another instrument state. You must use the instrument state that you loaded during the initialization procedure for the next step.

Measurement Calibration

11. Press **Cal** **CALIBRATE MENU** **FULL 2-PORT** **RETENTION**.
12. Connect the open that is supplied in the calibration kit to reference test port 1.



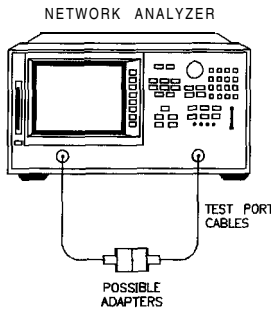
sb68d

Figure 2-9. Connections for Measurement Calibration Standards

13. Press **FORWARD OPEN**.
14. When the analyzer **finishes** measuring the standard, connect the short that is supplied in the calibration kit to reference test port 1.
15. Press **FORWARD SHORT**.
16. When the analyzer **Wishes** measuring the standard, connect the **50 ohm** termination that is supplied in the calibration kit to reference test port 1.
17. Press **FORWARD LOAD**.

Note **For** broadband measurements, use either a broadband load or a combination of **lowband** (or broadband) and sliding loads Use the same loads used during normal calibrations

18. Press either **BROADBAND** or **SLIDING**, depending on which device is used. If you select **SLIDING**, you must also measure a lowband load to complete the loads calibration.
19. When the measurement is complete, press **DONE LOADS**. Leave the load connected to the reference test port 1 cable.
20. When the analyzer finishes measuring the standard, connect the open that is supplied in the calibration kit to reference test port 2.
21. Press **REVERSE OPEN**.
22. When the analyzer finishes measuring the standard, connect the short that is supplied in the calibration kit to reference test port 2.
23. Press **REVERSE SHORT**.
24. When the analyzer finishes measuring the standard, connect the 50 ohm termination to reference test port 2.
25. Press **REVERSE LOAD**.
26. Press either **BROADBAND** or **SLIDING**, depending on which device is used. If you select **SLIDING**, you must also measure a lowband load to complete the loads calibration.
27. When the measurement is complete, press **DONE LOADS STANDARDS DONE**. Leave the load connected to the reference test port 2 cable.
28. The analyzer briefly displays **COMPUTING CAL COEFFICIENTS**.
29. Press **ISOLATION DO BOTH FWD + REV**.
30. Connect the two test port return cables together to form a "thru" configuration, as shown in Figure 2-10.



pb626d

Figure 2-10. Thru Connections

31. Press **TRANSMISSION DO BOTH FWD + REV.**
32. Press **DONE 2-PORT CAL.**
33. Press **(Save/Recall) SELECT DISK INTERNAL MEMORY RETURN SAVE STATE** to save the calibration into the analyzer **internal** memory.

Note Step 33 is crucial to the correct recall of the calibration during **subsequent measurements**. The calibration **MUST** be stored in **INTERNAL MEMORY** to be properly recalled.

34. When the analyzer **finishes** saving the instrument **state**, press **SELECT DISK INTERNAL DISK**.

Verification Device Measurements

The following **verification** procedure is automated by the analyzer firmware. For each **verification** device, the analyzer reads a **file** from the **verification** disk and sequentially measures the **magnitude** and phase for all four S-parameters.

The device number and test number for each verification device are as follows:

Verification Device	Test Number	Device Description
1	27	20 dB attenuator
2	28	40/50 dB attenuator
3	29	50Ω airline
4	30	25Ω mismatch airline

35. Press **(System)** **SERVICE MENU** **TESTS** **(27)** **(x1)** .

36. In the **active** entry area on the display, the following will be displayed:

TEST 27 **Ver** Dev 1

37. If the record function was switched on **in** step 5, or if a printout is not desired, go to step 38.

If a printout of the data for this device is desired, press **(System)**

SERVICE MENU **TEST OPTIONS** **RECORD ON** **(System)** **SERVICE MENU** **TESTS** .

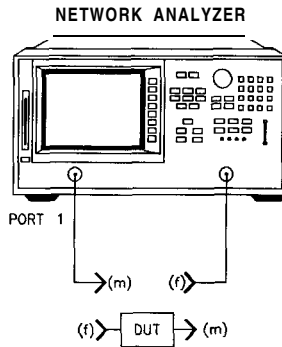
Make sure the paper in the printer is set up so that printing starts at the top of the page.

38. Press **PAUSE TESTS** .

Note When printing the test results, press **FORM FEED** on the printer to create page breaks in appropriate places

Connecting a Device

39. When prompted, **insert** the 20 **dB** attenuator as shown in the following **figure**.



sb638d

Figure 2-11. Verification Device Connections

40. Press **CONTINUE**. The tests **will** begin.
41. If the record function is off (**printout** is not required), the program will **pause after** each S-parameter measurement and you will need to press **CONTINUE** after each measurement. (There are eight measurements: magnitude and phase for each of the four S-parameters)

Note

Although the **verification** limits for all four **S-parameters** are calculated, only the uncertainties **associated** with the items indicated in the following chart will be used for the system verification. The other characteristics are less **significant** for verifying system performance; therefore, they will not appear on the printout. If a measurement fails, note which device and S-parameter failed, and continue on with the remaining **tests**.

Also note that both the measured data and the factory data are displayed as **DATA** and **MEMORY**, respectively.

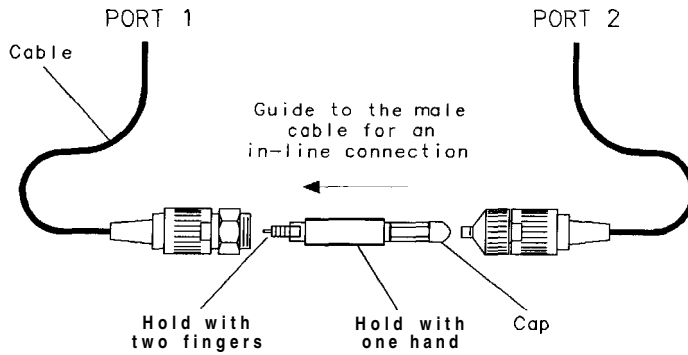
Verification Device	S11/S22 Magnitude	S11/S22 Phase	S21/S12 Magnitude	S21/S12 Phase
20 dB attenuator	x		x	x
40 dB attenuator	x		x	x
Airline	x	x	x	x
Stepped impedance airline (rho = 0.6 std)	x	x	x	x

42. When all measurements are complete, the **TESTS** softkey menu will appear. Disconnect the verification device.
43. Enter **Test 28** (using step keys, entry keys, or front panel knob). Repeat steps 38 through 42 with the 40 or 50 dB attenuator.
44. Enter **Test 29** (using step keys, entry keys, or front panel knob). Repeat steps 38 through 42 with the 500 airline. For an example of how to perform proper airline connections, refer to the following figures.

Caution

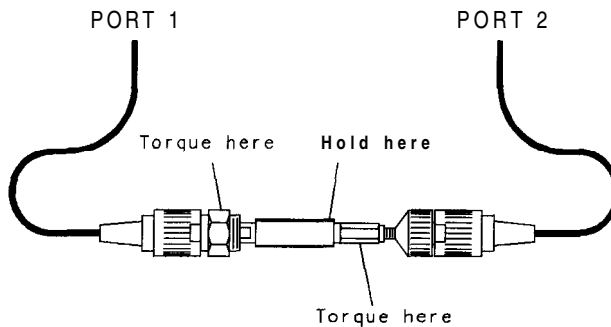
Be **especially** careful not to drop either the center conductor or the outer conductor when handling these airlines. Irreparable damage will result if these devices are dropped.

During this procedure, you will be touching the exposed center conductor of the test port with the center conductor of the airline. Ground yourself to prevent electrostatic discharge (ESD).



sb610d

Figure 2-12. Aligning the Center Conductor



sb611d

Figure 2-13. Torquing the Connection

46. Enter **Test** 30 (using step keys, entry keys, or front panel knob). Repeat steps 38 through 42 with the **25Ω** mismatch airline. See the above figures
46. The printout of the measurements shows both a plot of the measurement, when **TOP GRAPHICS** is active, and a list of the measured frequencies with corresponding data. The plot includes both the measured data trace and the supplied factory data trace. The listing includes only the measured data. If there is a **failure** at any frequency, an asterisk **will** be next to the measured data and the **out-of-specification** measured data on the plot **will** be blanked out.

In Case of **Difficulty**

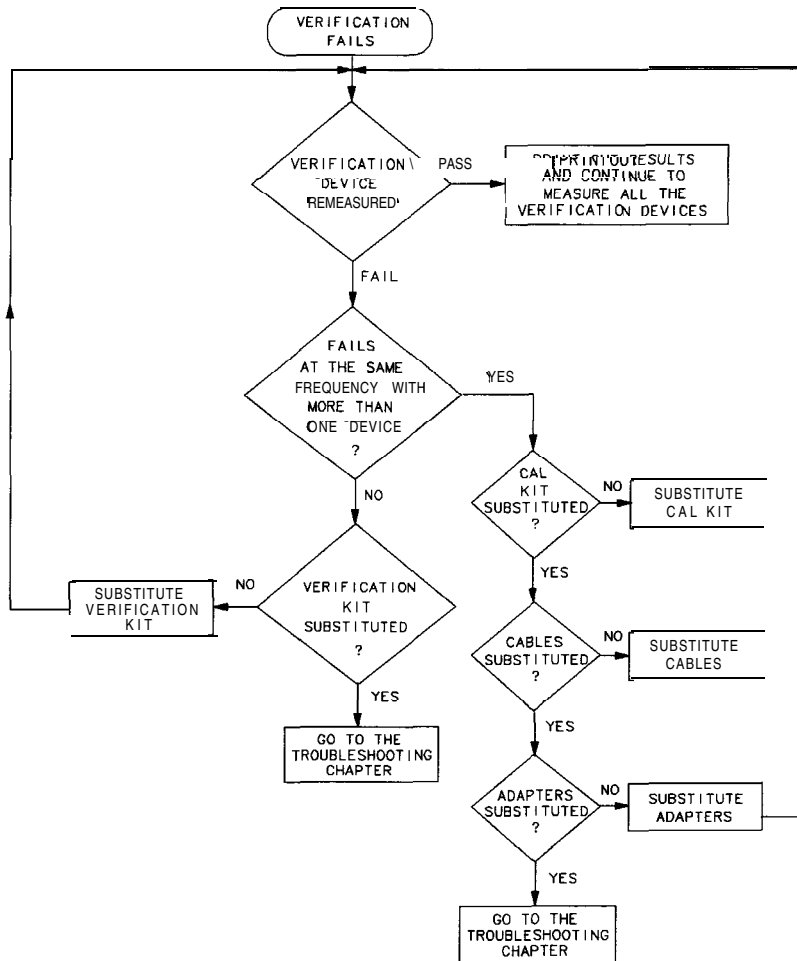
1. Inspect all connections. **DO NOT disconnect** the cables from the analyzer test ports. Doing so **WILL INVALIDATE** the calibration that you have done earlier.
2. Repeat the “Device Verification” procedure. **Be** sure to make good connections for each **verification** device measurement.
3. If the analyzer still fails the test, check the measurement calibration as follows:
 - a. Press - **PRESET: FACTORY**.
 - b. **Recall the calibration by pressing** **(Save/Recall)** **SELECT DISK** **INTERNAL MEMORY** **RETURN**.
 - c. Use the **front panel knob** to **highlight** the calibration you want to recall and press **RECALL STATE**.
 - d. Connect the short to reference test port 1.
 - e. Press **(Meas)** **Ref1: FWD S11 (A/R)** **(Menu)** **TRIGGER MENU** **CONTINUOUS**.
 - f. Press **(SCALE/REF)** **SCALE/DIV** **.05** **(x1)**.
 - g. Check that the trace response is 0.00 ± 0.05 dB.
 - h. Disconnect the short and connect it reference test port 2.
 - i. Press **(Meas)** **Ref1: REV S22 (B/R)**.
 - j. Check that the trace response is 0.00 ± 0.05 dB.
 - k. If any of the trace responses are out of the specified limits, repeat the “Measurement Calibration” and “Device Verification” procedures.
4. Refer to the “Start Troubleshooting Here” chapter for more troubleshooting information.

If the System **Fails** the **Verification Test**

- **Disconnect** and reconnect the device that failed the **verification**. Then remeasure the device.

If the performance verification still fails:

- Continue to measure the rest of the verification devices and print out the results of **all** four measurement parameters
- Print the error terms and examine them for anomalies near the failure frequencies (Refer **to** the “Error **Terms**” chapter in this manual.)
- Make another measurement calibration and follow the flow chart on the following page.



sb69d

Figure 2-14. Verification Fails Flowchart

Interpreting the Verification Results

The following **figures** show typical **verification** results, with dump graphics activated, that could appear on a system verification printout. These printouts compare the data from your measurement results with the traceable data and corresponding uncertainty specifications. Use these printouts to determine whether your measured data falls within the total uncertainty **limits** at **all** frequencies.

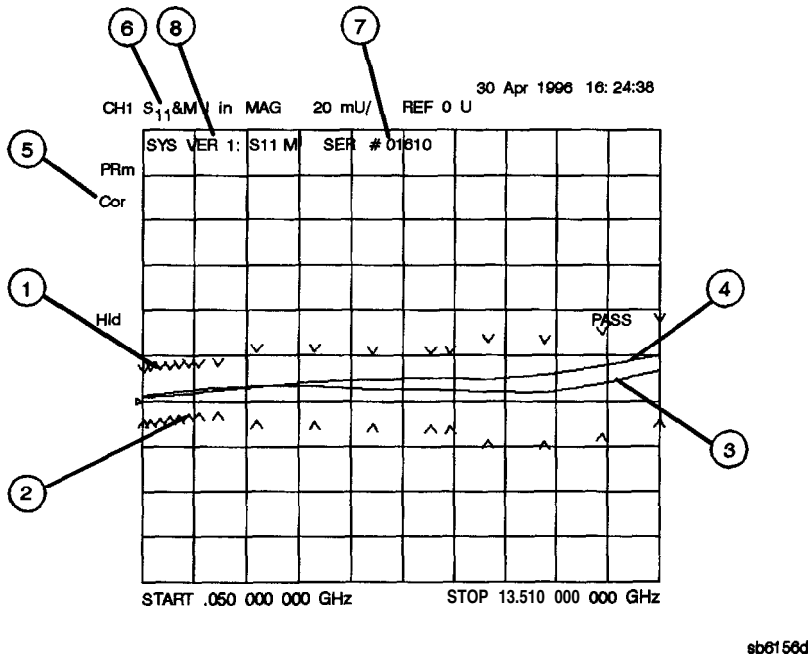


Figure 2-15. Graphic Print Out of Verification Results

1. Upper limit points as defined by the total system uncertainty **specifications**.
2. Lower **limit** points as **defined** by the total system uncertainty **specifications**.
3. Data measured at the factory.
4. Results of magnitude measurement as measured in performance **verification**.
5. Correction is turned on.
6. Measurement parameter **S₁₁** linear magnitude
7. Serial number of device
8. Device being measured : sys ver 1 = 20 **dB** attenuator.

STIMULUS	CH1 S12	Margin	Upper lim	Lower Lim
	MHz			
.050 000 000	-20.04 dB	.063	-19.976 dB	-20.197 a
.250 000 000	-20.105 dB	.103	-19.985 dB	-20.208 dB
.500 000 000	-20.113 dB	.101	-19.987 dB	-20.214 dB
.750 000 000	-20.12 dB	.103	-19.983 dB	-20.224 dB
1.000 000 000	-20.126 dB	.104	-19.984 dB	-20.23 dB
1.250 000 000	-20.136 dB	.098	-19.989 dB	-20.234 dB
1.500 000 000	-20.155 dB	.082	-19.992 dB	-20.237 dB
2.000 000 000	-20.197 dB	.048	-19.999 dB	-20.246 dB
3.000 000 000	-20.19 dB	.125	-19.957 dB	-20.315 dB
4.500 000 000	-20.192 dB	.149	-19.976 dB	-20.342 dB
6.000 000 000	-20.212 dB	.152	-19.993 dB	-20.365 dB
7.500 000 000	-20.206 dB	.181	-20.016 dB	-20.388 dB
8.000 000 000	-20.22 dB	.180	-20.025 dB	-20.4 dB
9.000 000 000	-20.235 dB	.262	-19.961 dB	-20.498 dB
10.500 000 000	-20.257 dB	.261	-19.966 dB	-20.518 dB
12.000 000 000	-20.295 dB	.254	-20.017 dB	-20.55 dB
13.500 000 000	-20.307 dB	.265	-20.041 dB	-20.574 dB
15.000 000 000	-20.317 dB	.280	-20.036 dB	-20.622 dB
16.500 000 000	-20.412 dB	.238	-20.061 dB	-20.65 dB
18.000 000 000	-20.46 dB	.205	-20.076 dB	-20.666 dB
19.500 000 000	-20.345 dB	.257	-20.087 dB	-20.675 dB
20.000 000 000	-20.346 dB	.259	-20.087 dB	-20.675 dB

sb6157d

Figure 2-16. Tabular Print Out of Verification Results

1. Frequency of the data points
2. Results of magnitude measurement as measured in the performance verification.
3. Upper hit line as defined by the total system uncertainty **specification**.
4. Lower limit line as **defined** by the total system uncertainty **specification**.
6. Difference between the measured results **and** the **limit** line A positive number indicates a pass An asterisk (*) indicates a fail.

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1. Frequency Accuracy Performance **Test**

This test checks the frequency accuracy of the analyzer at its maximum frequency.

Required Equipment and Tools (HP 8719D/20D Only)

Frequency Counter HP 5350B
RF Cable..... HP 85131C/D

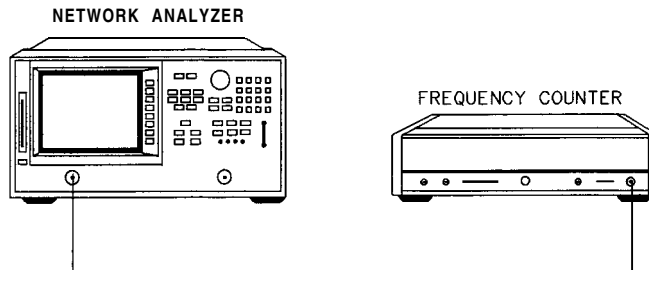
Required Equipment and Tools (HP 8722D Only)

Frequency Counter HP 5351B
RF Cable..... HP 85133C/D

Analyzer warm-up time: 1 hour.

1. Connect the equipment as shown in **Figure 2-17** and press **Preset**

PRESET: FACTORY **Preset** **Menu** **CV FREQ.**



sb65d

Figure 2-17. Frequency **Range** and Accuracy **Test** Setup

2. Select the analyzer CW frequency:
 - a. **For** the HP 8719D, press (13.5) **(G/n)**.
 - b. **For** the HP 8720D, press **(20) (G/n)**.
 - c **For** the HP 8722D, press **(26) (G/n)**.
3. Write the frequency counter reading on the “Performance **Test** Record.”

If the Instrument **Fails** This **Test**

1. If the frequency measured is close to **specification** limits (either in or out of **specification**), check the time base accuracy of the counter used.
2. If the analyzer **fails** by a **significant** margin, the master time base probably needs **adjustment**. In this case, refer to the “Frequency Accuracy Adjustment” in Chapter 3.
3. See the “Source Troubleshooting” chapter for related troubleshooting information.

2. Power Flatness Performance **Test**

The source power level is tested at 201 frequencies across the frequency range of the analyzer.

Required Equipment and Tools (HP 8719D/20D Only)

Power Meter HP 437B, HP 436A, or HP 438A
Power Sensor HP8485A
Adapter 3.5-mm (f) to 3.5-mm (f) .. HP P/N 85052-60012 (part of HP 85052B/D)

Required Equipment and Tools (HP 8722D Only)

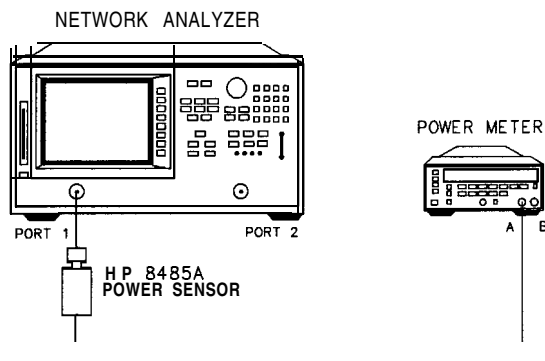
Power Meter HP 437B, HP 436A, or HP 438A
Power Sensor HP8487A
Adapter 2.4-mm (f) to 2.4-mm (f) HP P/N 11900B (part of HP 85056B/D)

Analyzer warm-up time: 1 hour.

1. Zero and calibrate the power meter.
2. Set the calibration factor on the power meter to the average value of the power sensor between 0.050 and 20 GHz (40 GHz for HP 8722D).

For example, if the power sensor calibration factor is 100% at 0.050 GHz and 92% at 20 GHz (40 GHz for HP 8722D), set the calibration factor to 96%.

3. Connect the equipment as shown in **Figure 2-18**.



sb64d

Figure 2-18. Power Test Setup

4. On the analyzer, press **(Preset) PRESET: FACTORY (Preset)**.
5. Press **(Menu) POWER** enter the power value listed in **Table 2-3** and then press **(x1)**.

Table 2-3. Power Values for Flatness Test

Model/Option	Test Power Setting
HP 8719D/20D	0 dBm
HP 8719D/20D Option 007	5 dBm
HP 8722D	-15 dBm
HP 8722D Option 007	-10 dBm

6. Press **(Menu) SWEEP TIME (300) (x1)** to set a 300 second sweep.
7. Press **(Menu) SINGLE** to initiate a single sweep.
8. **During** the sweep, notice the maximum and minimum power level readings, and write these on the “Performance **Test** Record.”
 The analyzer remains at each frequency point for 1.5 seconds to allow the power meter **sufficient time to** settle.
9. Connect the power sensor to port 2 and press **(Meas) Ref1: REF 322 (B/R)**.
10. Repeat steps 5 through 8.

If the Instrument **Fails This** Test

1. Ensure that the power meter and power sensor are operating to **specification**.
2. **Inspect** the analyzer port connectors, the adapter and the power sensor connector for damage. Poor match at these connections can generate power reflections and cause the analyzer to appear to be out of **limits**.
3. **Marginal** failures (especially at the high or low end) may be due to the power sensor calibration factor approximation method. A calibration factor approximation of **±4%**, as in the above example, induces an error of about

0.15 dB. To eliminate the calibration factor approximation as the cause of failure, do the following:

- a. Press **(Menu)** **CF FREQ** and rotate the knob to the frequency in question.
 - b. Set the calibration factor on the power meter to the value indicated by the power sensor.
 - c. The corrected power level reading should be between the limits shown in the “Performance **Test** Record.”
4. The source relies on the power adjustment for proper performance. Refer to “Adjustments” for additional information.
 5. In case of a repeated failure, after you have made the power adjustments, refer to “Source Troubleshooting.”

3. Power Linearity Performance Test

1. Press **(Preset)** **PRESET: FACTORY** **(Preset)**.
2. Press **(Meas)** **INPUT PORTS** **R** to measure R channel.
3. Press **(Marker Fctn)** **MARKER MODE MENU** **MARKERS: DISCRETE**.
4. Press **(Avg)** **IF BW** **(10)** **(x1)** to set the IF bandwidth to 10 Hz.
5. Press **(Menu)** **POWER** **PRR RANGE MAN** **POWER RANGES** **RANGE 0**.

Table 2-4. Power Value Settings for Testing Linearity

Power Settings	HP 8719D/20D Option 007	HP 8719D/20D Option 007	HP 8722D	HP 8722D Option 007
	$P_{Ref} - 5 \text{ dBm}$	$P_{Ref} - 0 \text{ dBm}$	$P_{Ref} - 10 \text{ dBm}$	$P_{Ref} - 5 \text{ dBm}$
$P_1 (P_{Ref} - 5 \text{ dB})$	-10 dBm	-5 dBm	-15 dBm	-10 dBm
$P_2 (P_{Ref} - 10 \text{ dB})$	-15 dBm	-10 dBm	-20 dBm	-15 dBm
$P_3 (P_{Ref} + 5 \text{ dB})$	0 dBm	+5 dBm	-5 dBm	0 dBm
$P_4 (P_{Ref} + 10 \text{ dB})$	+5 dBm	+10 dBm	NA	NA

For 8719D/20D Only

6. Refer to Table 2-4 and enter the power value for P_{Ref} for the particular analyzer under test. After you enter the value, press **(x1)**.
7. Wait for the analyzer to complete a full sweep.
8. Press **(Display)** **DATA: MEN** **DATA/MEN**.
9. Press **(Marker)** **A NODE MENU** **FIXED MKR POSITION** **FIXED MKR VALUE** **(0)** **(x1)**.
10. Press **(Menu)** **POWER**.
11. Enter the power value that is listed in the P_1 row of Table 2-4 for the particular analyzer under test. After you enter the value, press **(x1)**.
12. Wait for the analyzer to complete a full sweep.

13. Press **(Marker Fctn)** **MR SEARCH** **SEARCH: MAX**.
14. Read the marker value from the **analyzer** display and add 5 **dB**. Write the **calculated** value on the test record.
15. Press **SEARCH: MIN**.
16. Read the marker value from the analyzer display and add 5 **dB**. Write the calculated value on the test record.
17. Repeat steps 10 through 16 but enter the power value listed in row **P₂** and add 10 **dB** to arrive at the calculated **value**.
18. Repeat steps 10 through 16 but enter the power value listed in row **P₃** and subtract 5 **dB** to arrive at the calculated value.
19. Repeat steps 10 through 16 but enter the power value listed in row **P₄** and subtract 10 **dB** to arrive at the calculated value.

For 8722D Only

20. Press **(Stop)** **20** **(G/n)**.
21. Press **(Menu)** **POWER**.
22. Refer to **Table 2-4** and enter the power value for **P_{Ref}** for the particular analyzer under test. After you enter the value, press **(x1)**.
23. Wait for the analyzer to complete a full sweep.
24. Press **(Display)** **DATA-MEM** **DATA/MEM**.
25. Press **(Marker)** **A MODE MENU** **FIXED MKR POSITION** **FIXED MKR VALUE** **(0)** **(x1)**.
26. Press **(Menu)** **POWER**.
27. Enter the power value that is listed in the **P₁** row of **Table 2-4** for the particular analyzer under test. **After** you enter the value, press **(x1)**.
28. Wait for the analyzer to complete a full sweep.
29. Press **(Marker Fctn)** **MR SEARCH** **SEARCH: MAX**.
30. Read the marker value from the analyzer display and add 5 **dB**. Write the calculated value on the test record.

31. Press **SEARCH: MIN**.
32. Read the marker value from the analyzer display and add 5 **dB**. Write the calculated value on the test record.
33. Press **Start** **20** **G/n**.
34. Press **Stop** **40** **G/n**.
35. Repeat steps 21 through 32.
36. Press **Start** **50** **M/u**.
37. Repeat steps 21 through 26.
38. Enter the power value that is listed in the **P₂** row of **Table 2-4** for the particular analyzer under test. After you enter the value, press **x1**.
39. Wait for the analyzer to complete a full sweep.
40. Press **Marker Fctn** **MARK SEARCH** **SEARCH: MAX**.
41. Read the marker value from the analyzer display and add 10 **dB**. Write the **calculated value on the** test record.
42. Press **SEARCH: MIN**.
43. Read the marker value from the analyzer display and add 10 **dB**. Write the calculated value on the test record.
44. Press **Stop** **20** **G/n**.
45. Repeat steps 21 through 26.
46. **Enter** the power value that is listed in the **P₃** row for the particular analyzer under test. After you enter the value, press **x1**.
47. Wait for the analyzer to complete a full sweep.
48. Press **Marker Fctn** **MARK SEARCH** **SEARCH: MAX**.
49. Read the marker value from the analyzer display and subtract 5 **dB**. Record the calculated value on the test record.
50. Press **SEARCH: MIN**.
51. Read the marker value from the analyzer display and subtract 5 **dB**. Record the calculated value on **the** test record.

If the Instrument Fails This Test

1. Ensure that the power meter and power sensor are operating to specification.
2. The source relies on the power linearity adjustment for correct performance. Refer to “Power Linearity Adjustment” and perform the procedure. Then repeat this test.
3. If the analyzer repeatedly fails this test, refer to “Source Troubleshooting” located later in this manual.

4. Dynamic Range Performance **Test**

Dynamic range is checked by comparing the noise floor to the test port output power level.

Required Equipment and Tools (HP 8719D/20D Only)

Calibration Kit.....HP 85052B/D
RF Cable Set.....HP 85131C/D

Required Equipment and Tools (HP 8722D Only)

Calibration Kit.....HP 85056B/D
RF Cable Set.....HP 85133C/D

Note Other calibration kits may be used if you are working in a different connector type.

Analyzer warm-up time: 1 hour.

1. To preset the analyzer, press **Presets** **PRESET: FACTORY** **Presets**.
2. To enter the values for the first frequency segment:
 - a. For analyzers without new CPU and with **firmware** upgrade **6.xx** and below, press:

Menu **SWEEP TYPE MENU**
EDIT LIST **ADD**
START **50** **M/μ**
STOP **50.000101** **M/μ**
NUMBER OF POINTS **101** **x1**
DONE

- b. For analyzers with new CPU and with **firmware** upgrade **7.xx** and greater, press:

Menu **SWEEP TYPE MENU**
EDIT LIST **ADD** **MORE** **LIST POWER ON** **LIST IF BW ON** **RETURN**
Menu **SWEEP TYPE MENU**
EDIT LIST **ADD**

START (50) (M/μ)
STOP (50.000101) (M/μ)
NUMBER of POINTS (101) (x1)
SEGMENT POWER (FROM TABLE) **SEGMENT BW** (FROM TABLE) (x1)
DONE

- Repeat the previous procedure (beginning with **ADD**) to enter the values for the remaining frequency segments of your analyzer. (Refer to **Table 2-5**.)

Note If your analyzer has the new, faster CPU **Firmware** Revision **7.xx** or greater, refer to **Table 2-6**.

Table 2-5. Frequency Segment Values

Segment	Start	Stop	Number of Points
1	50 MHz	50.000101 MHz	101
2	839.999899 MHz	840 MHz	101
3	0.84 GHz	2 GHz	101
4	2 GHz	8 GHz	101
5 (HP 8719D)	8 GHz	13.5 GHz	101
5(HP 8720D/22D)	8 GHz	20 GHz	151
6 (HP 8722D)	20 GHz	40 GHz	201

Table 2-6.
Frequency Segment Values for HP 8722D
with new CPU and firmware 7.xx and above

Segment	Start	Stop	Number of Points	Power at Test Port	Power at Test Port Opt.007	IF Bandwidth
1	50 MHz	50.000101 MHz	101	-5 dBm	0 dBm	10 Hz
2	889.999899 MHz	840 MHz	101	-5 dBm	0 dBm	10 Hz
3	.840 GHz	2 GHz	101	-5 dBm	0 dBm	10 Hz
4	2 GHz	8 GHz	101	-5 dBm	0 dBm	10 Hz
5	8 GHz	20 GHz	151	-5 dBm	0 dBm	10 Hz
6	20.000001 GHz	40 GHz	201	-10 dBm	-5 dBm	10 Hz

4. When all of the frequency segments have been entered, press **DONE**

LIST FREQ ALL SEGS SWEEP.

5. To set up the port 1 measurement, press:

Meas **Trans. FWD S21 (B/R)**

Format **LIN MAG**

Avg **IF BW** **10** **x1**

Scale Ref **2** **x1**

Cal **NONE** **ALTERNATE A and B**

All 8722D

Menu **POWER** **PWR RANGE HAT** **POWER RANGES** **RANGE 0**

8722D without new CPU and **firmware 6.14** and below:

I-lo] **x1** (for Option 007 -5 dBm)

6. Connect a **thru** (RF cable) between ports 1 and 2.

7. To start the measurement calibration, press **Cal** **CALIBRATE MENU**

RESPONSE & TSDL F **RESPONSE** **THRU**.

8. Remove the **thru** and connect 50 ohm terminations to ports 1 and 2.

9. To continue the measurement calibration, press **(Avg) AVERAGING FACTOR (8)**
(x1) AVERAGING ON (Cal) RESUME CAL SEQUENCE ISOL'N STD.

This measurement takes several minutes.

10. When the analyzer beeps, press **DONE-RESP ISOL'N CAL.**

11. Press **(Avg) AVERAGING OFF.**

12. Press **(Menu) TRIGGER MENU SINGLE.**

13. When the single sweep has been taken, press the following keys:

(Scale Ref) AUTOSCALE
(Marker Fctn) ALL OFF MARKER MODE MENU MARKERS: DISCRETE
(Marker) MARKER 1 (50) (M/μ)
(MARKER 2) (50.000101) (M/μ)
(Marker Fctn) MKR MODE MENU STATS ON
(Marker) ANODE MENU AREF=1

14. Read the mean value and standard deviation from the analyzer display.
 Calculate the dynamic range value, using the following equation.

$$20 \times \log [(3 \times \text{Standard Deviation}) + \text{Mean Value}]$$

Write the calculated value on the "Performance Test Record."

15. Repeat the previous two steps (beginning with **(Marker) MARKER 1**), placing marker 1 and marker 2 at the start and stop of the remaining frequency ranges that are listed on the "Performance Test Record."

HP 8722D without new CPU board and with revision 6.14 and below, proceed as follows:

(MENU) SWEEP TYPE MENU LIN FREQ SWEEP (START) (20 GHz) (STOP) (40 GHz)
(MENU) POWER (-10 dBm)

Repeat steps 6 through 15.

16. Press **(Meas) Trans: REF S12 (A/R)** and repeat steps 6 through 15 to measure port 2.

If the Instrument **Fails** This **Test**

1. **First** suspect the connections, the calibration standards and the cable. Visually inspect all of the connectors and repeat the test.
2. In case of repeat failure, gage the connectors, see ‘Principles of Microwave Connector Care’ in Chapter 1 of this manual, and substitute the calibration standards and the cable.
3. Recheck the output power of the source
4. Refer to the “Start Troubleshooting Here” chapter for additional help.

Performance **Test** Record

The complete system performance verification record includes the printout from the total system uncertainty test, these test records, and a **certificate** of calibration.

Use the following sheets to record the results of the performance tests You may wish to copy the sheets to retain them as masters

Performance Test Record for HP 8719D/20D/22D

Test Facility _____		Report Number _____	
_____		Date _____	
_____		Date of Last System Calibration _____	
_____		_____	
Tested by _____		Customer _____	
Model _____		Calibration Kit S/N _____ Verification Kit Model _____	
Serial Number _____		Test Port cables _____ Verification Kit S/N _____	
Calibration Kit _____		Measurement Calibration Technique _____	
Ambient temperature _____ °C		Relative Humidity _____	
Ambient temperature at measurement calibration _____ °C		Ambient temperature at performance verification _____ °C	
Test Equipment Used			
Model Number	Trace Number	Cal Due Date	
1. Frequency Counter _____	_____	_____	
2. Power Meter _____	_____	_____	
3. Power Sensor _____	_____	_____	
4. Spectrum Analyzer _____	_____	_____	
Special Notes: This system verification applies to total measurement uncertainty and frequency accuracy specifications . _____			

Test Description	Minimum Specifications	Results	Maximum Specifications	Measurement Uncertainty*
1. Frequency Accuracy				
13.5 (HP 8719D)	13.499865 GHz		13.600135 GHz	40.5 kHz
20.0 (HP 8720D)	19.999800 GHz		20.000200 GHz	60 kHz
26.0 (HP 8722D)	25.999740 GHz		26.000260 GHz	78 kHz

*The measurement uncertainty is based on equipment specified in Table 1-2 in the ‘Service Equipment and Analyzer Options’ chapter.

Test Description	Minimum Spec	Results Test Port 1		Results Test Port 2		Maximum Spec	Measurement Uncertainty
		Min.	Max.	Min.	Max.		
2. Power Flatness							
HP 8719D	-2.0 dBm					+2.0 dBm	0.3 dB
HP 8719D (Opt. 007)	+ 3.0 dBm					+7.0 dBm	0.3 dB
HP 8720D	-2.0 dBm					+2.0 dBm	0.3 dB
HP 8720D (Opt. 007)	+ 3.0 dBm					+7.0 dBm	0.3 dB
HP 8722D	-18.0 dBm					-12.0 dBm	0.3 dB
HP 8722D (Opt. 007)	- 13.0 dBm					-7.0 dBm	0.3 dB

Test Description	Minimum Specification	Results		Maximum Specification
		Min.	Max.	
1. Power Linearity				
Power Settings				
P₁				
BP 8719D/20D	-0.356			0.35 dB
HP 8722D (0.05–20 GHz)	-0.35 dB			0.35 dB
HP 8722D (20–40 GHz)	-0.6	0.6		0.60 dB
P₂				
HP 8719D/20D	-0.6 dB			0.6 dB
HP 8722D	-0.6 dB			0.6 dB
P₃				
HP 8719D/20D	-0.35 dB			0.35 dB
HP 8722D (0.05–20 GHz)	-0.35 dB			0.35 dB
P₄				
HP 8719D/20D	-1.0 dB			1.0 dB
HP 8722D	NA	NA	NA	NA

Power Value Settings for Testing Linearity

Power Settings	HP 8719D/20D	HP 8719D/20D Option 007	HP 8722D	HP 8722D option 007
	P _{Ref} = -5 dBm	P _{Ref} = 0 dBm	P _{Ref} = -10 dBm	P _{Ref} = -5 dBm
P₁ (P_{Ref} - 5 dB)	-10 dBm	-5 dBm	-15 dBm	-10 dBm
P₂ (P_{Ref} - 10 dB)	-15 dBm	-10 dBm	-20 dBm	-15 dBm
P₃ (P_{Ref} + 5 dB)	0 dBm	+5 dBm	-5 dBm	0 dBm
P₄ (P_{Ref} + 10 dB)	+5 dBm	+10 dBm	NA	NA

Test Description	Specification		Results	
	NOT Option 00 ¹	Option 007	Port 1	Port 2
4. Dynamic Range				
HP 8719D/20D				
0.05 to 0.050000101 GHz	77 dB	82 dB		
0.839999899 to 0.84 GHz	77 dB	82 dB		
0.84 to 2 GHz	100 dB	105 dB		
2 to 8 GHz	100 dB	105 dB		
8 to 20 GHz	100 dB	105 dB		
HP 8722D				
0.05 to 0.050000101 GHz	67 dB	72 dB		
0.839999899 to 0.84 GHz	67 dB	72 dB		
0.84 to 2 GHz	93 dB	98 dB		
2 to 8 GHz	93 dB	98 dB		
8 to 20 GHz	91 dB	96 dB		
20 to 40 GHz	80 dB*	85 dB*		
* 3 dB less for Option 085 or Option 012.				

Adjustments and Correction Constants

The accuracy of the analyzer is achieved and maintained through mechanical adjustments, electrical **adjustments**, and correction constants. The correction constants are empirically derived data that are stored in memory and then recalled to **refine** the instrument's measurements and to determine its proper operation.

Any **time** the **A7** CPU assembly is replaced, all of the correction constants must be regenerated and stored on the new assembly. Alternatively, the data can be retrieved from disk. Hewlett-Packard recommends that you store the correction constant data to disk by referring to the "EEPROM Backup Disk Procedure" in this chapter.

Additionally, there are adjustments and correction constants that must be performed following the replacement of an assembly. Refer to the following "Post Repair Procedures" tables in order to determine which adjustments and correction constants procedures to perform.

This chapter contains the following adjustment procedures:

- **A7** Jumper/Switch Positions
- Source **Pretune** Correction Constants (Test 43)
- Analog Bus Correction Constants (~~Test~~ 44)
- **IF Amplifier** Correction Constants (~~Test~~ 47)
- **ADC** Offset Correction Constants (Test 48)
- **Serial** Number Correction Constants (~~Test~~ 49)
- Protected Option Numbers Correction Constants (~~Test~~ 50)
- Unprotected Hardware Option Numbers Correction **Constants**
- Output Power Adjustments
- Power Linearity Adjustment
- **Blanking** Adjustment (~~Test~~ 54)
- **Initialize EEPROMs** (~~Test~~ 53)
- EEPROM Backup Disk Procedure
- Correction Constants Retrieval Procedure
- ㊦㊧㊨㊩㊪ **Firmware**
- Reference Assembly VCO Tune Adjustment
- Frequency Accuracy Adjustment
- Fractional-N Spur Avoidance and **FM** Sideband Adjustment

Post-Repair Procedures

The following tables list the additional service procedures which you must perform to ensure that the instrument is working correctly, following the replacement of an assembly. These procedures can be located in either Chapter 2 or Chapter 3.

Perform the procedures in the order that they are listed in the table.

Table 3-1. Related Service Procedures (1 of 4)

Replaced Assembly	Adjustments/ Correction Constants (Ch. 8)	Verification (Ch. 2)
A1 Front Panel Keyboard	None	Internal Test 0 Internal Test 12 Internal Test 23 Internal Test 24
A2 Front Panel Processor	None	Internal Test 0 Internal Test 12 Internal Test 23
A4/A5/A6 Second Converter	None	System Verification
A52 Pulse Generator	Output Power Adjustments	System Verification
A8 Post Regulator	None	Internal Test 0 Check A8 test point voltages
A7 CPU¹	A7 Jumper/Switch Positions Load Firmware² CC Retrieval Serial Number CC (Test 40) Option Number CC (Test 60) Display Intensity CC (Test 45) Analog Bus CC (Test 44) Source Pretune CC (Test 43) IF Amplifier CC (Test 47) EEPROM Backup Disk	Power Level Test Dynamic Range Test <i>or</i> System Verification

1 If you have an EEPROM backup disk available, you only need to perform the first five tests listed.

2 Only for instruments with firmware revisions 7.xx and above.

Table 3-1. Related Service Procedures (2 of 4)

Replaced Assembly	Correction Constants (Ch. 3)	Verification (Ch. 2)
A9 Source Control	None	System Verification
A10 Digital IF	A7 Jumper/Switch Positions Analog Bus CC (Test 44) IF Amplifier CC (Test 47)	Dynamic Range Test System Verification Internal Test 17 Internal Test 18 Internal Test 19 or System Verification
A11 Phase Lock	A7 Jumper/Switch Positions Analog Bus CC (Test 44) Source Pretune CC (Test 43)	Frequency Range and Accuracy or System Verification
A12 Reference	A7 Jumper/Switch Positions Reference Assembly VCO Tune Frequency Accuracy	Frequency Range and Accuracy
A13 Fractional-N Analog)	A7 Jumper/Switch Positions Analog Bus CC (Test 44) Fractional-N Spur Avoidance and FM Sideband Adjustment	Internal Test 20 Frequency Range and Accuracy
A14 Fractional-N Digital)	A7 Jumper/Switch Positions Analog Bus CC (Test 44)	Frequency Range and Accuracy Internal Test 20 or System Verification
A15 Preregulator	None	Self-Test†
A16 Rear Panel Interface	None	Internal Test 13, Rear Panel
A17 Motherboard	None	Self-Test†
These tests are located in Chapter 4, "Start Troubleshooting Here."		

Table 3-1. Related Service Procedures (3 of 4)

Replaced Assembly	Adjustments/ Correction Constants (Ch. 3)	Verification (Ch. 2)
A18 Display	None	None
A19 Graphics System Processor	None	Observation of Display Tests 59–76*
A51 Test set Interface	None	Operation Check [†]
A53 Low Band Assembly	Output Power Adjustments	Power Level Test Frequency Range and Accuracy
A54 YIG2 20–40 GHz (HP 8722D Only)	Source Pretune	Power Level Test Frequency Range and Accuracy
A55 YIG1 2.4-20 GHz	Source Pretune	Power Level Test Frequency Range and Accuracy
A56 Lower Front Panel Assembly	None	Observation (watch LEDs when switching from S11 to S22)
A57 Fixed Oscillator	Output Power Adjustments	Power Level Test Frequency Range and Accuracy
A58 M/A/D/S	Output Power Adjustments	Power Level Test
A59 Source Interface	Output Power Adjustments	Power Level Test
A60/61 DC Bias Tees	None	System Verification

* **These tests** are located in Chapter 6, “**Digital** Control Troubleshooting.”

† **These checks** are located in Chapter 4, ‘Start **Troubleshooting** Here.’”

Table 3-1. Related Service Procedures (4 of 4)

Replaced Assembly	Adjustments/ Correction Constants (Ch. 3)	Verification (Ch. 2)
A62/A63 Directional Couplers	None	System Verification
A64 R1 Sampler	Sampler Check[†] Power Adjustment	System Verification Power Level Test
A64 R2 Sampler (Option 400 Only)	Sampler Check[†] Power Adjustment	System Verification Power Level Test
A65 A Sampler	Sampler Check[†]	System Verification
A66 B Sampler	Sampler Check[†]	System Verification
A68 6 dB Attenuator	None	Operation Check[†]
A69 Step Attenuator	None	Operation Check[†]
S1 Switch (HP 8722D Only)	None	Operation Check[†]
S2/S3 Switches	None	Operation Check[†]
S4 Transfer Switch	None	Operation Check[†]
† These checks are located in Chapter 4, ‘Start Troubleshooting Here.’		

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A7 Jumper/Switch Positions

1. Remove the power line cord from the analyzer.
2. Set the analyzer on its side.
3. Remove the two corner standoffs from the bottom of the instrument with the **T-10** TORX screwdriver.
4. Loosen the captive screw on the bottom cover's back edge, with the **T-15 TORX** screwdriver.
5. Slide the cover toward the rear of the instrument.

Caution Proper ESD procedures must be used when performing the following step.

6. Move the jumper or switch as shown in F'igure **3-1** or F'igure 3-2.
 - Move the **A7** jumper/switch to the Alter position (**ALT**) before you **run** any of the correction constant adjustment routines. This is the position for **altering** the analyzer's correction constants
 - Move the **A7** jumper/switch to the Normal position (**NRM**) after you have run correction constant adjustment routines This is the position for normal operating conditions
7. Reconnect the power **line** cord and switch on the instrument.

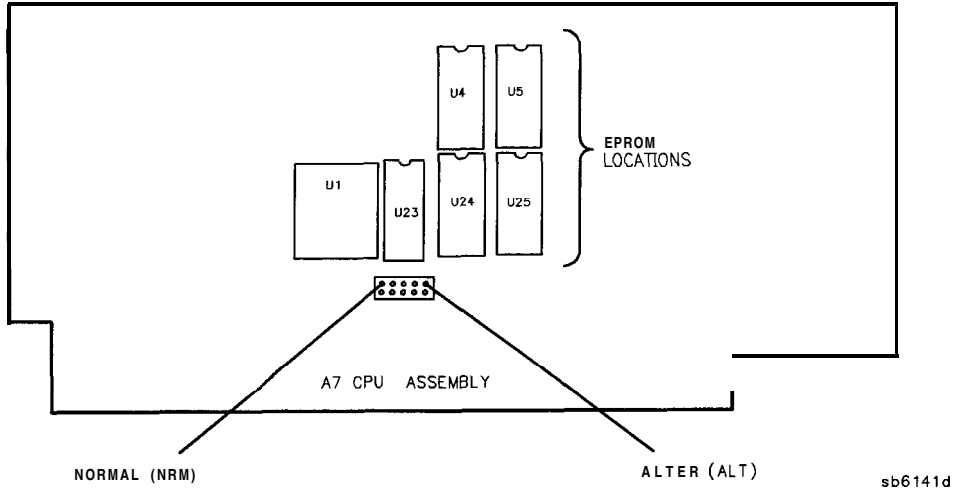


Figure 3-1. A7 Jumper Positions (Firmware revisions 6.xx and below.)

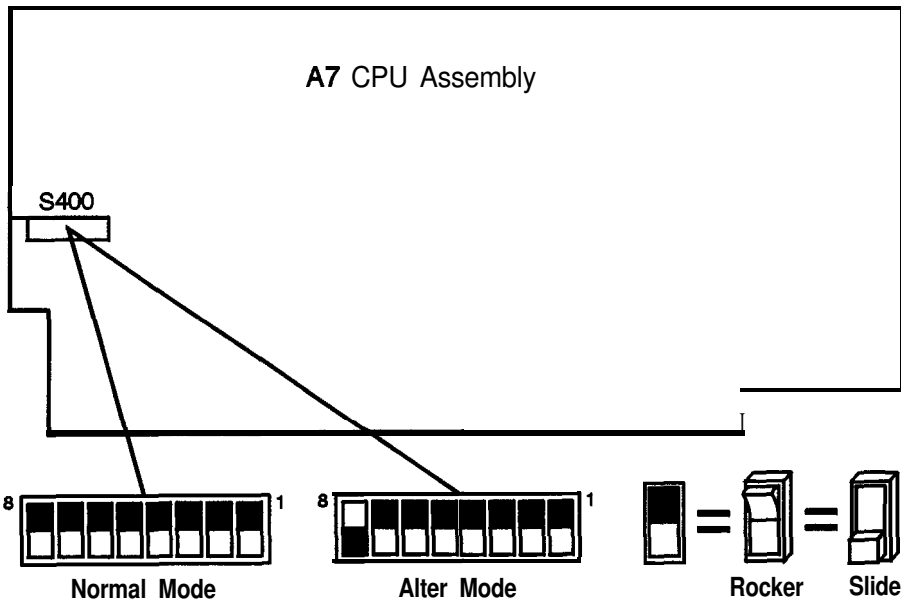


Figure 3-2. A7 Switch Positions (Firmware revisions 7.xx and above.)

Source Pretune Correction Constants (Test 43)

Required Equipment and Tools (HP 8719D/20D Only)

Frequency counter HP 5350B*
RF cable HP 85131C/D/E/F

*The frequency accuracy of the HP 8566B/63E spectrum analyzer is sufficient for this procedure.

Required Equipment and Tools (HP 8722D Only)

Frequency counter HI5351B*
RF cable HP 85133C/D/E/F

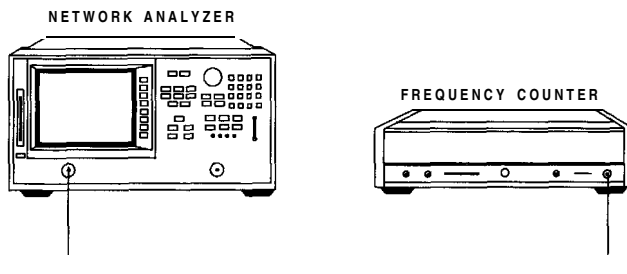
*The frequency accuracy of the HP 8566B/63E spectrum analyzer is sufficient for this procedure.

Analyzer warm-up time: 30 minutes.

This procedure generates pretune values for correct phase-locked loop operation.

1. Make sure the **A7** jumper/switch is in the Alter position (**ALT**).
2. Connect the equipment as shown in Figure 3-2 and then press **(Preset)**
PRESET **FACTORY** **(System)** **SERVICE MENU** **TESTS** **ADJUSTMENT TESTS**.

When P-pretune Adj is displayed, press **ALC/OUT TEST**. Press **YES** at the query to alter the correction constants



sb65d

Figure 3-3. Source Pretune Correction Constants Setup

3. When the prompt, Set source to 2.345 **GHz**, then `continue` appears, use the front panel knob to adjust the **frequency** of the analyzer source to within 5 MHz of 2.345 **GHz**. Press **CONTINUE** when the frequency is set.
4. For the HP **8722D**, when the prompt, Set source to 19.550 **GHz**, then `continue` appears, use the front panel knob to adjust **the frequency of the** analyzer source to within 5 MHz of 19.550 **GHz**. Press **CONTINUE** when the frequency is set.
5. When **Pretune Adj DONE** is displayed, press **(Preset) PRESET: FACTORY** .
6. If no more correction constant routines are going to be performed, return the **A7** jumper/switch to the Normal position (**NRM**) .
7. Perform the “EEPROM **Backup** Disk Procedure’ located on page 3-34.

In Case of **Difficulty**

If any error messages appear, refer to “Source Troubleshooting.”

Analog Bus Correction Constants (Test 44)

Analyzer warm-up time: 30 minutes.

This procedure calibrates the analog bus by using three reference voltages (ground, +0.37 and +2.5 volts), then stores the calibration data as correction constants in EEPROMs.

1. Make sure the A7 jumper/switch is in the Alter position (ALT).
2. Press **(Preset)** **PRESET: FACTORY** **(System)** **SERVICE MENU** **TESTS** **(44)** **(x1)**
EXECUTE TEST **YES**.
3. Observe the analyzer for the results of the adjustment routine:
 - If the analyzer displays ABUS Cor DONE, you have completed this procedure.
 - If the analyzer displays ABUS Cor FAIL, refer to the “Digital Control Troubleshooting” chapter.
4. If no more correction constant routines are going to be performed, return the A7 jumper/switch to the Normal position (NRM) .
5. Perform the “EEPROM Backup Disk Procedure” located on page 3-34.

IF **Amplifier** Correction Constants (**Test 47**)

Required Equipment and Tools

RF Cable (HP 8719D/20D Only)	HP 85131C/D/E/F
RF Cable (HP 8722D Only)	HP 85133C/D/E/F
Antistatic Wrist Strap	9300-1367
Antistatic Wrist Strap Cord	9300-0980
Static-control Table Mat and Earth Ground Wire	9300-0797

Analyzer warm-up Time: 30 minutes.

These correction constants compensate for IF amplifier linearity difference between gain stages

1. Make sure the **A7** jumper/switch is in the Alter position (ATT).
2. Connect the RF cable from Port 1 to Port 2 of the analyzer.
3. Press **(Preset)** **PRESET: FACTORY** **(System)** **SERVICE MENU** **TESTS** **(47)** **(x1)**
EXECUTE TEST **YES** **CONTINUE**.
4. Observe the analyzer for the results of the adjustment routine:
If IF Step Cor **DONE** is displayed, you have completed this procedure.
5. If no more correction **constant** routines are going to be performed, return the **A7** jumper/switch to the Normal position (**NRM**) .
6. Perform the “EEPROM Backup Disk Procedure” located on page 3-34.

In **Case** of **Difficulty**

1. If FAIL is displayed, check that the RF’ cable is connected from Port 1 to Port 2. Then repeat this adjustment routine
2. If the analyzer continues to fail the adjustment routine, refer to the “Digital Control Troubleshooting” chapter.

ADC Offset Correction Constants (**Test 48**)

Analyzer warm-up time: 30 minutes.

These correction constants improve the dynamic accuracy by shifting small **signals** to the most linear part of the ADC **quantizing** curve

1. Make sure the **A7** jumper/switch is in the Alter position (**ALT**).

2. Press **(Preset)** **PRESET: FACTORY** **(System)** **SERVICE MENU** **TESTS** **(48)** **(x1)**
EXECUTE TEST **YES**.

Note **This** routine takes about three minutes

3. Observe the analyzer for the results of the adjustment routine:

If the analyzer displays **ADC Ofs Cor DONE**, you have completed this procedure

4. If no more correction constant routines are going to be performed, return the **A7** jumper/switch **to** the Normal position (**NRM**).

5. Perform the “EEPROM Backup Disk Procedure” located on page 3-34.

In Case of **Difficulty**

If the analyzer displays **ADC Ofs Cor FAIL**, refer to the “**Digital** Control Troubleshooting” chapter.

Serial Number Correction Constants (Test 49)

Analyzer warm-up time: None.

This procedure stores the analyzer serial number in the **A7** CPU assembly EEPROMs.

Caution Perform this procedure **ONLY** if the **A7** CPU assembly has been replaced.

1. Make sure the **A7** jumper/switch is in the Alter position (**ALT**).
2. Record the ten character serial number that is on the analyzer rear panel **identification** label.
3. Press **Preset** **PRESET: FACTORY** **Display** **MORE** **TITLE** **ERASE TITLE** to erase the HP logo.
4. Enter the serial number by rotating the front panel knob to position the arrow below each **character** of the instrument serial number, and then **pressing** **SELECT LETTER** to enter each character. Enter a total of ten characters: two letters and eight **digits**.

Press **←** if you made a mistake.

Note The serial number may also be entered using the optional external keyboard.

5. Press **DONE** when you have finished entering the title. Double check that the correct serial number appears in the title area. If you made a mistake at this point, return to step 3.

Caution **You CANNOT** correct mistakes after you perform step 6, **unless** you contact the factory for a clear serial number keyword. Then you must perform the “Options Correction Constants” procedure and repeat this procedure.

6. Press **(System)** **SERVICE MENU** **TESTS** **(49)** **(x1)** **EXECUTE TEST** **YES**.
7. Observe the analyzer for the results of the routine:
If the analyzer displays the message Serial Cor **DONE**, you have completed this procedure
8. If no more correction constant routines are going to be performed, return the **A7** jumper/switch to the Normal position (**NRM**).

In Case of Difficulty

1. If the analyzer does not display **DONE**, then either the serial number that you entered in steps 3 and 4 did not match the required format or a serial number was already stored. Check the serial number recognized by the analyzer:
 - a. Press **(Preset)** **PRESET: FACTORY** **(System)** **SERVICE MENU** **FIRMWARE REVISION**.
 - b. Look for the serial number displayed on the analyzer screen.
 - c. **Rerun** this adjustment test if the serial number is not displayed.
2. If the analyzer continues to fail this adjustment routine, contact your nearest Hewlett-Packard sales and service **office**.

Protected Option Numbers Correction Constants (Test 50)

Analyzer warm-up time: None.

This procedure stores the instrument's protected option(s) information in **A7** CPU assembly **EEPROMs**. You can also use this procedure to remove a serial number, with the unique keyword, as referred to in "Serial Number Correction constant."

Caution Perform this procedure **ONLY** if the **A7** CPU assembly has been replaced and the "Serial Number Correction Constants" procedure has been performed.

1. Remove the instrument bottom cover and record the keyword label(s) that are located on the exposed sheet metal next to the **A7** CPU assembly. Note that each keyword is for EACH option installed in the instrument.
2. Make sure the **A7** jumper/switch is in the Alter position (**ALT**).
 - If the instrument does not have a label, then contact your nearest Hewlett-Packard Sales and Service **Office**. **Be** sure to include the full serial number of the instrument.
3. Press **Presets** **PRESET: FACTORY** **Display** **MORE** **TITLE** **ERASE TITLE** to erase the HP logo.
4. Enter the keyword by rotating the front panel knob to position the arrow below each character of the keyword, and then pressing **SELECT LETTER** to enter each letter.

Press **←** if you made a mistake.

Note The keyword may also be entered using the optional external keyboard.

5. Press **DONE** when you have finished entering the title.

Caution Do not confuse **"I"** with **"1"** (one) or **"O"** with **"0"** (zero).

6. Press **(System) SERVICE MENU TESTS (50) (x1) EXECUTE TEST YES.**
7. Observe the analyzer for the results of the adjustment routine:
 - If the analyzer **displays** Option Cor **DONE**, you have completed this procedure.
 - If the analyzer has more than one option, repeat steps 3 through 6 to **install** the remainhg options
8. If no more correction constant routines are **going** to be performed, return the **A7 jumper/switch** to the Normal position (**NRM**).

In Case of Difficulty

1. If the analyzer displays Option Cor FAIL, check the keyword used **in** step 2 and make sure it **is** correct. Pay **special** attention to the letters **“I”** or **“O”**, the numbers **“1”** or **“0”** (zero). Repeat **this** entire adjustment test.
2. If the analyzer continues to fail the **adjustment** routine, refer to the **“Digital Control Troubleshooting”** chapter.

Unprotected Hardware Option Numbers Correction Constants

Analyzer warm-up time: None

This procedure stores the instrument's unprotected option(s) information in **A7** CPU assembly **EEPROMs**.

1. Make sure the **A7** jumper/switch is in the Alter position (**ALT**).
2. Record the installed options that are printed on the rear panel of the analyzer.
3. Press **System** **SERVICE MENU** **PEEK/POKE** **PEEK/POKE ADDRESS**.
4. Refer to **Table 3-2** for the address of each unprotected hardware option. Enter the address for the **specific** installed **hardware option that needs to be** enabled or disabled. **Follow** the address entry by **POKE** **[-1]** **[x1]**.
 - Pressing **POKE** **[-1]** **[x1]** after an address entry enables the option.
 - Pressing **POKE** **[0]** **[x1]** after an address entry disables the option.

Table 3-2.
PEEK/POKE Addresses for Unprotected Hardware Options

Hardware Option	PEEK/POKE Address	
	Firmware Revisions 6.xx and Below	Firmware Revisions 7.xx and Above
1D5	5243250	1619001529
8722	5243258	1619001533
085	6243260	1619001534
007	5243262	1619001535
089	5243264	1619001536
400	5243266	1619001537
012	5243268	1619001538

5. Repeat steps 3 and 4 for all of the unprotected options that you want to enable

6. After you have entered **all** of the instrument's hardware options, press the following keys:

System **SERVICE MENU** **FIRMWARE REVISION**

7. View the analyzer display for the listed options
8. When you have entered all of the hardware options, return the **A7** jumper/switch to the Normal position (**NRM**).
9. Perform the 'EEPROM Backup Disk Procedure' located on page 3-34.

In Case of **Difficulty**

If any of the installed options are missing from the list, return to step 2 and reenter the missing option(s).

Output Power Adjustments

Required Equipment and Tools (HP 8719D/20D Only)

Power meter	HP 436A, 437B/438A
Power sensor	HP 8485A
3.5-mm (f) to 3.5-mm (f) Adapter	85052-60012 (part of 85052B/D)
Cable 3.5 mm (f) to 3.5 mm (f)	85131-60013

Required Equipment and Tools (HP 8722D Only)

Power meter	HP 436A, 437B/438A
Power sensor	HP 8487A
2.4-mm (f) to 2.4-mm (f) Adapter	HP 11900B (part of 85056B/D)
Cable 2.4 mm (f) to 2.4 mm (f)	85133-60016

Analyzer warm-up time: 30 minutes.

1. Prepare the power meter for use. Refer to “Power Meter Measurement Calibration” in Chapter 5 of your **analyzer’s User’s Guide**.
2. Make sure the write protect jumper/switch on the CPU board is in the Alter position (**ALT**).

Set main power DAC to preset values.

3. For each PEEK/POKE location listed in **Table 3-3** do the following:

- a. Press **(System)** **SERVICE MENU** **PEEK/POKE** **PEEK POKE ADDRESS**.
- b. Enter the peek/poke address from **Table 3-3** and then press **(x1)** **POKE**.
- c. Enter the poke value from **Table 3-3** and then press **(x1)**.

Table 3-3. Main Power DAC Peek/Poke Location Table

Hardware Option	PEEK/POKE Location		Poke Value 8719/8720	Poke Value 8722
	Firmware Revisions 6.xx and Below	Firmware Revisions 7.xx and Above		
Low power	5243076	1619001442	1	1
Low power	5243078	1619001443	0	200
Mid power	5243080	1619001444	3	5
Mid power	5243082	1619001445	49	172
High Power	5243084	1619001446	10	10
High Power	5243086	1619001447	12	12

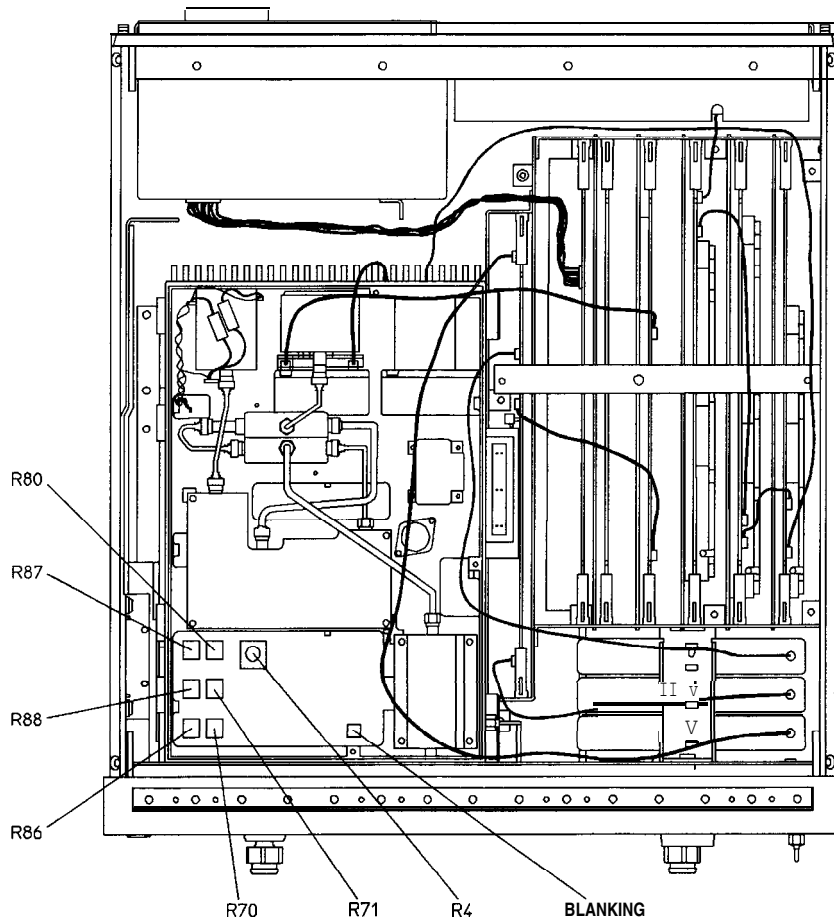
Note The analyzer may display the message CAUTION TEST PORT
OVERLOAD, REDUCE POWER. Ignore this message and continue
with the procedure.

Set the potentiometers to the minimum levels.

4. **Set** the low band power potentiometer (**A59 R4**), full counter-clockwise.
5. Set the offset potentiometers (**A59 R70, R71, R80**), to their full counter-clockwise position.

The end stops on **10-turn** potentiometers are indicated by a clicking sound.

6. Set the slope potentiometers (**A59 R86, R87, R88**), to their full clockwise position.



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Figure 3-4. Location of Output Power Adjustments

Start the Adjustment

7. Connect the power sensor to Test Port 1.

8. Press **Preset** **PRESET FACTORY** **Preset**.

9. Press **System** **SERVICE MENU** **SERVICE MODES** **SRC ADJUST MENU** **ALC OFF**.

Adjustments and Correction Constants **3-23**

10. Press **Start** **50** **M/μ** **Stop** **2.549** **G/n**.
11. Press **MEAS** **INPUT PORTS** **R**.
12. If the analyzer is not phase locked, adjust Low Band Power Adjust, **A59 R4**, clockwise until the instrument phaselocks across the frequency range 50 MHz to 2.549 GHz.
13. Press **Marker Fctn** **MR SEARCH "OFF"** **SEARCH MIN** **Seq**
SPECIAL FUNCTIONS **MARKER → CH**. Press **Menu** **CH FREQ**.
14. Adjust the low band power resistor (**A59 R4**) for a power meter reading that is equal to the **value** listed under “Power A” in **Table 3-4**.

Table 3-4. Output Power Adjustment Values

Model/Option	Power A (dBm)	Power B (dBm)	Power C (dBm)
HP 8719/20D ¹	+7	-3	-5
HP 8719/20D Option 007	+12	+2	0
HP 8722D ¹	-3	-13	-10
HP 8722D Option 007	+2	-8	-5

¹ All options *except* Option 007

Note The analyzer may display the message **CAUTION TEST PORT OVERLOAD, REDUCE POWER**. Ignore this message and continue with the procedure.

15. Press **Preset** **FACTORY PRESET** **Preset**.
16. Press **Menu** **POWER** **PWR RANGE MAN** **POWER RANGES** **RANGE 0**.

Adjust Mid Band **Power**

17. Press **Menu** **CH FREQ** **2.566** **G/n**.
18. To switch the power DAC on, press the following keys:
System **SERVICE MENU** **SERVICE MODES** **SRC ADJUST MENU**
POWER DAC [ON] **1000** **x1**

19. **Adjust** the mid band power offset resistor (**A59 R71**) for a power meter reading that is equal to the value (± 0.2 dB) listed under “Power B” in **Table 3-4**.
20. Press **(Menu)** **CW FREQ** **(20)** **(G/n)**.
21. **Adjust** the mid band power slope resistor (**A59 R88**) for a power meter reading that is equal to the value (± 2 dB) listed under “Power B” in **Table 3-4**.

Adjust Low Band Power

22. Press **(Menu)** **CW FREQ** **(50)** **(M/μ)**.
23. Adjust the low band power offset resistor (**A59 R70**) for a power meter reading that is equal to the value listed under “Power B” in **Table 3-4**.
24. Press **(Menu)** **CW FREQ** **(2.54)** **(G/n)**
25. Adjust the low band power slope resistor (**A59 R86**) for a power meter reading that is equal to the value listed under “Power B” in **Table 3-4**.

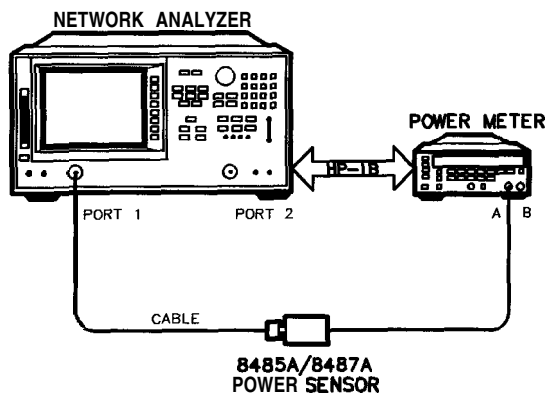
Adjust High Band Power (8722D ONLY)

26. Press **(Menu)** **CW FREQ** **(20.06)** **(G/n)**
27. Adjust the high band power offset resistor (**A59 R80**) for a power meter reading that is equal to the value listed under “Power B” in **Table 3.4**.
28. Press **(Menu)** **CW FREQ** **(40)** **(G/n)**
29. Adjust the **high** band power slope resistor (**A59 R87**) for a power meter reading that is equal to the value listed under “Power B” (± 4 dB) in **Table 3-4**.

Fine Tune the Flatness

30. Press **(Preset)** **FACTORY: PRESET** **(Preset)**.
31. Press **(Menu)** **POWER** **PWR RANGE MAX** **POWER RANGES** **RANGE 0**.
32. Enter the power value from the “Power C” column in **Table 3.4** for the particular analyzer that you are adjusting.

33. Press **Menu** **SWEEP TYPE MENU** **STEP SWEEP ON**.
34. Press **Menu** **NUMBER of POINTS** **101** **x1**.
35. Press **Avg** **IF BW** **300** **x1**.
36. Press **MEAS** **INPUT PORTS** **B**.
37. Press **Scale Ref** **.5** **x1**.
38. Press **Local** **SYSTEM CONTROLLER** **Cal** **PWR MTR CAL**. Set the calibration power to the power level from the “Power C” column in **Table 3-4**.
39. Press **NUMBER of READINGS** **2** **x1**.
40. Connect the power sensor to the port 1 through cable and press **ONE SWEEP** **MAX CAL SWEEP**. See **Figure 3-5**.



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Figure 3-5. Output Power Adjustments

Wait for the analyzer to **finish** the power meter calibration.

Note **The** analyzer may display the message CAUTION TEST PORT OVERLOAD, **REDUCE** POWER. Ignore this message and continue with the procedure

41. Connect Port 1 to Port 2.
42. Press **(Save/Recall)** **SAVE STATE** **FILE UTILITIES** **RENAME FILE** **ERASE TITLE** rename file "PWRCAL" and press **DONE**.
43. Press **(Cal)** **RECEIVER CAL**.
44. Enter the power value in "Power C" column of **Table 3-4** and then press **TAKE RCVR CAL SWEEP**.
45. Switch off the power meter calibration by pressing **(Cal)** **PWR MTR CAL [DNE SWEEP]** **PWR MTR CAL OFF**.

The analyzer's trace now represents power flatness

46. Adjust the slope and offset of **all** the bands for a flatness of ± 1 dB to 20 GHz (± 2.5 to 40 GHz). Refer to the column "Power C (dBm)" in **Table 3-4**.

This sets the mid band power level.

In Case of Difficulty

1. Check for available power and modulator functionality by **adjusting** the power DAC from 0 to 4005.

The power should vary from approximately -33 **dB** to +4 **dB** from the maximum **specified** power.

- If the analyzer is not operating correctly, as indicated from the results of the previous step, refer to “Source Troubleshooting” located later in this **manual**.

Power Linearity Adjustment

Before you perform this procedure, you must perform the previous procedure, “Output Power Adjustment.” This procedure is a continuation of the “Output Power Adjustments” procedure.

Preparatory Steps

1. If you haven’t already done so, perform the “Output Power Adjustment” procedure.
2. Connect a cable between port 1 and port 2.
3. Press **(Save/Recall)** select the “PWRCAL” file and press **RECALL STATE**.
4. To switch off the power meter calibration, press **(Cal)** **PWR MTR CAL [DONE SWEEP] PWR MTR CAL OFF**.

The analyzer’s trace now represents power flatness

5. Press **(Cal)** **RECEIVER CAL** and enter the power value listed as “P2” in **Table 3-6**, and then press **(x1)** **TAKE RCVR CAL SWEEP**.
6. Press **(Menu)** **POWER** and enter the power value listed as “P3” in **Table 3-5**, and then press **(x1)**.

Table 3-5. Power Linearity Adjustment Values

Power Settings	HP 8719D/20D	HP 8719D/20D Option 007	HP 8722D	HP 8722D Option 007
P1 1	5 dBm	10 dBm	-5 dBm	0 dBm
P2	-5 dBm	0 dBm	-10 dBm	-5 dBm
P3	-15 dBm	-10 dBm	-20 dBm	-15 dBm

1 P1 only applies to 20 GHz for HP 8722D.

7. Press **(Scale Ref)** **(.5)** **(x1)** **REFERENCE VALUE** enter the power value listed as P3 in **Table 3-5** and then press **(x1)**.

The displayed trace should be centered on the reference (± 0.5 dB).

- If the trace is not centered on the reference, continue with the next step.
- If the trace is centered on the reference, continue with step 17.

8. To switch on the power DAC, press **(System)** **SERVICE MENU** **SERVICE MODES** **SRC ADJUST MENU** **PHR DAC**.
 For the HP 8719D or 8720D, press **(258)** **(x1)**.
 For the HP 8722D, press **(459)** **(x1)**.
9. Adjust the front panel knob until the measurement trace is centered around **the** reference **line**. Record the "MAIN POWER DAC" number.
10. To switch off the power DAC, press **PHR DAC ON OFF**.
11. Press **(Save/Recall)** **SAVE STATE**.
12. Divide the previously recorded DAC number by 256.
13. Store the quotient by pressing **(System)** **SERVICE MENU** **PEEK/POKE** **PEEK/POKE ADDRESS** **(5243076)** **(x1)** **POKE** enter the quotient and then press **(x1)**.
14. Store the remainder by pressing **(System)** **SERVICE MENU** **PEEK/POKE** **PEEK/POKE ADDRESS** **(5243078)** **(x1)** **POKE** enter the remainder and then press **(x1)**.
15. Press **(Preset)** **PRESET FACTORY** **(Preset)**.
16. Press **(Save/Recall)** **RECALL STATE**.

For 8722D Analyzers Only

17. Press **(MARKER)** **(20)** **(G/n)** and disregard response beyond 20 GHz.

For All Analyzers

18. Press **Menu** **POWER** and enter the power level that is listed as “P1” in Table 3-5 and then press **x1**.
19. Press **Scale Ref** **.5** **x1** **REFERENCE VALUE** enter the value listed as P1 in Table 3-5 and then press **x1**.

The displayed trace should be centered on the reference (± 0.5 dB).

- If the trace is not centered on the reference, continue with the next step.
- If the trace is centered on the reference, continue with step 27.

20. lb switch on the power DAC, press **System** **SERVICE MENU** **SERVICE MODES** **SRC ADJUST MENU** **PWR DAC** **2580** **x1**.
21. Adjust the front panel knob until the measurement trace is centered around the reference **line**. Record the “MAIN POWER DAC” number.
22. To switch off the power DAC, press **PWR DAC**.
23. Press **Save/Recall** **SAVE STATE**.
24. Divide the previously recorded DAC number by 256.
25. Store the quotient by pressing **System** **SERVICE MENU** **PEEK/POKE** **PEEK/POKE ADDRESS** **5243084** **x1** **POKE** enter the quotient and then press **x1**.
26. Store the remainder by pressing **System** **SERVICE MENU** **PEEK/POKE** **PEEK/POKE ADDRESS** **5243086** **x1** **POKE** enter the remainder and then press **x1**.
27. Press **Preset** **PRESET: FACTORY** **Preset**.
28. Press **Save/Recall** **RECALL STATE**.
29. Perform **the** EEPROM Backup Procedure, located on page 3-34.
30. Perform the ‘Power Linearity performance **Test**’ procedure that is located behind the “2c. Performance **Tests**” tab of this manual.

In Case of **Difficulty**

1. If the analyzer fails the “Power Linearity Performance **Test,**” do the following:
 - If the analyzer fails the performance test for the power levels listed as **P2,** **P3,** and **P4,** repeat the ‘Power Linearity Adjustment.’”
 - If the analyzer fails the performance test for the power level listed as **P1,** repeat the “Output Power Adjustment” and the “Power Linearity Adjustment. ”
2. If the analyzer is still not passing the “Power Linearity Performance Test,” check for available power and modulator functionality by adjusting the power DAC from 0 to **4095** (refer to the “Output Power **Adjustments**” procedure).

The power should vary from -20 **dB** to +4 **dB** from the maximum specified power.

- If the analyzer is operating correctly, as indicated from the results of the previous step, repeat the “Output Power Adjustments” procedure.
- If the analyzer is not operating correctly, as indicated from the results of the previous step, refer to “Source Troubleshooting” located later in this manual.

Blanking Adjustment (Test 54)

Required Equipment and Tools (HP8719D/20D Only)

Power Meter	HP 436A, 437B, 438A
Power Sensor	HP 8485A
3.5-mm (f) to 3.5-mm (f) Adapter	85052-60012 (part of 85052B/D)

Required Equipment and Tools (HP8722D Only)

Power Meter	HP 436A, 437B, 438A
Power Sensor	HP 8487A
2.4-mm (f) to 2.4-mm (f) Adapter	HP 11900B (part of 85056B/D)

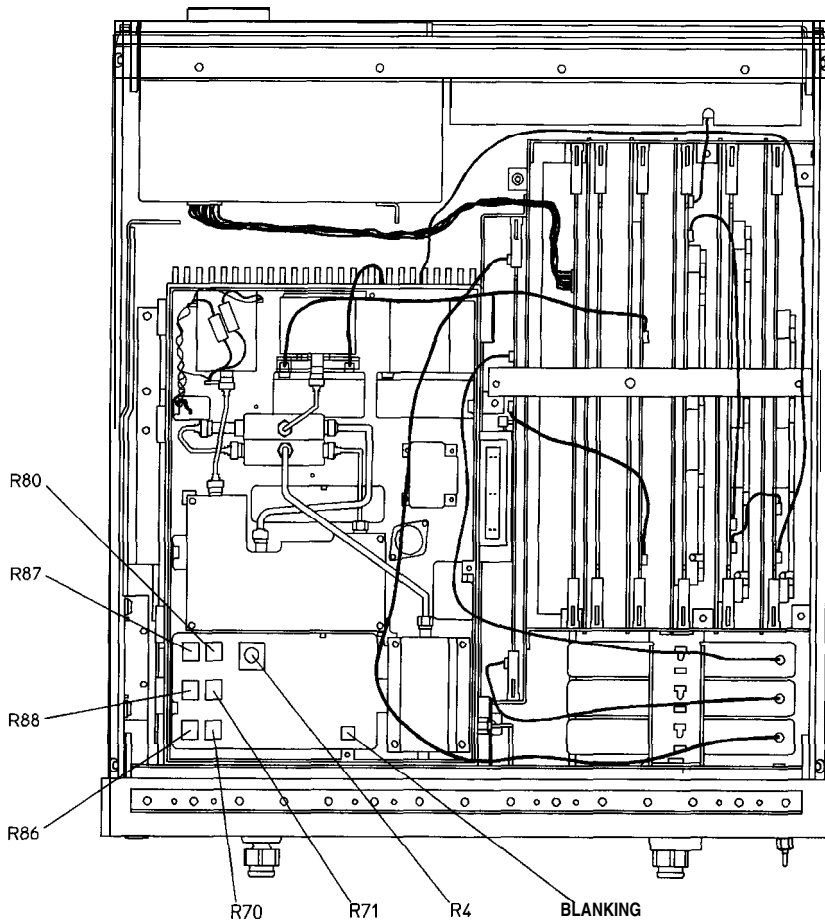
Analyzer warm-up time: 30 minutes.

This adjustment sets the output power level during retrace. If incorrectly adjusted, the first data points in a sweep may not be stable.

1. Remove the instrument top cover and source assembly cover.
2. Press **Preset** **PRESET: FACTORY** **Menu** **CH FREQ** **50.5** **(M/μ)**.
3. Press **System** **SERVICE MENU** **TESTS** **54** **(x1)**.

When the display reads **BLANKING ADJ**, press **EXECUTE TEST**.

4. Calibrate the power meter and connect it to port 1.
5. Refer to **Figure 3-6** and use the blanking **adjustment** to obtain the **value** indicated on the **analyzer display**.
6. **When** the adjustment is complete, press **CONTINUE**.



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Figure 3-6. Location of Blanking Adjustment

In Case of **Difficulty**

If you are unable to perform this adjustment, refer to the “Source Troubleshooting” chapter in this manual.

Initialize **EEPROMs (Test 53)**

This **internal** service test performs the following functions:

- **destroys** all correction constants and all un-protected options
- initializes certain EEPROM address locations to zeroes
- replaces the display intensity correction constants with default values

Note This routine **will not** alter the serial number or option number correction constants (**Tests** 49 and 50, respectively).

1. Press **(Preset)** **PRESET: FACTORY** **(System)** **SERVICE MENU** **TESTS** **(53)** **(x1)**
EXECUTE TEST **YES**.

2. Restore the **analyzer** correction constants in the **EEPROMs** by referring to “Correction Constants Retrieval Procedure,” located later in this chapter.
3. If you don’t have the correction constants backed up on a disk, run all the internal service routines in the following order:
 - Analog Bus Correction Constants (**Test** 44)
 - Source **Pretune** Correction Constants (**Test** 43)
 - ADC Offset Correction Constants (**Test** 48)
 - IF **Amplifier** Correction Constants (**Test** 47)

EEPROM Backup Disk Procedure

Required Equipment and Tools

3.5-inch Floppy Disk HP **92192A** (box of 10)

The correction constants, that are unique to your instrument, are stored in EEPROM on the **A7** controller assembly. By creating an EEPROM backup disk, you will have a copy of all the correction constant data should you need to replace or repair the **A7** assembly.

1. Insert a **3.5-inch** disk into the analyzer disk drive.

2. If the disk is not formatted, follow these steps:

a. Press **(Save/Recall)** **FILE UTILITIES** **FORMAT DISK**.

b. Select the format type:

■ lb format a **LIF** disk, select **FORMAT LIF**.

■ lb format a DOS disk, select **FORMAT DOS**.

c. Press **FORMAT INT DISK** and answer **YES** at the query.

3. Press **(System)** **SERVICE MENU** **SERVICE MODES** **MORE** **STORE EEPROM**
(Save/Recall) **SELECT DISK** **INTERNAL DISK** **RETURN** **SAVE STATE**.

Note The analyzer creates a default file "**FILE0**". The **filename** appears in the upper-left corner of the display. The **file** type "**ISTATE(E)**" indicates that the **file** is an instrument-state with EEPROM backup.

4. Press **FILE UTILITIES** **RENAME FILE** **ERASE FILE**. Use the front panel knob and the **SELECT LETTER** softkey (or an external keyboard) to rename the file "**FILE0**" TO "**N12345**" where **12345** represents the last 5 digits of the instrument's serial number. (The **first** character in the **filename** must be a letter.) When you are finished renaming the **file**, press **DONE**.

5. Write the following information on the disk label:

- analyzer serial number
- today's date
- "EEPROM Backup Disk"

Correction Constants Retrieval Procedure

Required Equipment and Tools

EEPROM Backup Disk

By using the current EEPROM backup disk, you can download the correction constants data into the instrument **EEPROMs**.

1. Insert the 'EEPROM Backup Disk' into the HP 8753E disk drive.
2. Make sure the **A7** jumper/switch is in the Alter position.
3. Press **(Save/Recall)** **SELECT DISK** **INTERNAL DISK**. Use the front panel knob to **highlight the file "N12345"** where **N12345** represents the **file** name of the EEPROM data for the analyzer. On the factory shipped EEPROM backup disk, the **filename** is **FILE1**.
4. Press **RETURN** **RECALL STATE** to download the correction constants data into the instrument **EEPROMs**.
5. Perform "Option Numbers Correction Constant (**Test 56**)."
6. Press **(Preset)** and verify that good data was transferred to EEPROM by performing a simple measurement.
7. Move the **A7** jumper/switch back to its Normal position when you are done working with the instrument.

Loading Firmware

Required Equipment and Tools

- **Firmware** disk for the HP 8719D/20D/22D

Analyzer warmup Time: None required.

The following procedures will load firmware for new or existing CPU boards in an HP 8719D/20D/22D network analyzer having firmware revision **7.xx** or above.

Loading Firmware into an Existing CPU

Use this procedure for upgrading **firmware** in an operational instrument whose CPU board has not been changed.

1. **Turn** off the network analyzer.
2. Insert the firmware disk into the instrument's disk drive.
3. Turn the instrument on. The llrmware will be loaded automatically **during** power-on. **The** front panel **LEDs** should step through a sequence as firmware is loaded. The display will be blank during this time.

At the end of a successful loading, the **LEDs** for Channel 1 and **Testport 1** **will** remain on and the display will turn on indicating the version of **firmware** that was loaded.

In Case of Difficulty

If the firmware did not load successfully, LED patterns on the front panel can help you isolate the problem.

- If the following LED pattern is present, the firmware disk is not for use with your instrument model. Check that the firmware disk used was for the HP 8719D/20D/22D.

LED Pattern					
CH1	CH2	R	L	T	S
•	•				

- If any of the following LED patterns are present, the firmware disk may be defective.

LED Pattern					
CH1	CH2	R	L	T	S
		•			
	•	•			
•		•			
•	•	•			
	•			•	
•				•	
•	•			•	
		•		•	
•	•	•		•	
		•		•	
	•	•			•
		•			•

- If any other LED pattern is present, the CPU board is defective.

Loading Firmware Into a New CPU

Use this procedure to load flrmware for an instrument whose CPU board has been replaced.

1. Turn off the network analyzer.
2. Insert the **firmware** disk into the instrument's disk drive.
3. Turn the instrument on. The **firmware** will be loaded automatically during power-on. The front panel **LEDs** should step through a sequence as **firmware** is loaded. The display will be blank during this time.

At the end of a successful loading, the **LEDs** for Channel 1 and **Testport 1** **will** remain on and the display will turn on indicating the version of **firmware** that was loaded.

Note Any time the **A7** CPU assembly is replaced, all of the correction constants must be regenerated or recalled, and stored on the new CPU assembly. Hewlett-Packard recommends that you store the correction constant data to a **3.5"** disk. Refer to the "**EEPROM Backup Disk Procedure**" in this chapter to do this.

In Case of Difficulty

- If the firmware did not load successfully, LED patterns on the front panel can help you isolate the problem.
 - If the following LED pattern is present, an acceptable **firmware filename** was not found on the disk. (The desired format for flrmware **filenames** is **8720D_07._02.**) Check that the firmware disk used was for the HP 8719D/20D/22D.

LED Pattern					
CH1	CH2	R	L	T	S

- If any of the following LED patterns are present, the firmware disk may be defective.

LED Pattern					
CH1	CH2	R	L	T	S
		•			
	•	•			
•		•			
•	•	•			
				•	
	•			•	
•				•	
•	•			•	
		•		•	
•		•		•	
		•		•	
	•	•			
					•
	•	•			•

- If any other LED pattern is present, the CPU board is defective.

Note If firmware did not load, a red LED on the CPU board will be flashing.

- If the following LED pattern is present on the CPU board, suspect the disk drive or associated cabling:

• • • ○ • • ○ ○

(front of instrument ↓)

Reference Assembly VCO Tune Adjustment

Required Equipment and Tools

Extender board, large part of tool kit 08720-60004
SMB (m) to SMB (f) Extension Cables **8120-5040**

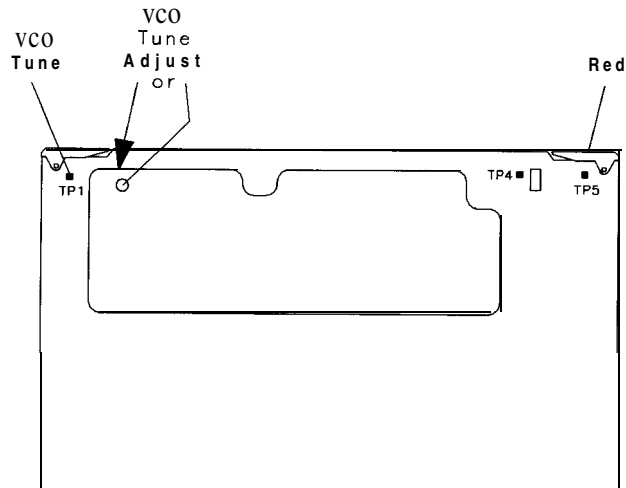
Analyzer warm-up time: 30 minutes.

This **adjustment** centers the reference assembly VCO (voltage controlled oscillator) in its tuning range.

1. Switch off the analyzer.
2. Remove the instrument top cover.
3. If the VCO TUNE adjustment screw is not accessible from the top of the **A12** assembly, perform the following step. If the screw is accessible, continue with step 4.
 - In order to access the VCO **TUNE** adjustment screw on the **A12** assembly, install the **A12** assembly onto the extender board. Use SMB extension cables as required (the **EXT REF** cable need not be reconnected now).

4. Press **[Preset]** **PRESET: FACTORY** **[Menu]** **CR PRG** **SWEEP TIME [AUTO]**
[2] **[x1]** **[System]** **SERVICE MENU** **ANALOG BUS ON** **[MEAS]**
ANALOG IN Aux Input **ANALOG BUS** **[15]** **[x1]** to display VCO
Tulle.

5. Press **[MARKER]** and **[Scale Ref]** **SCALE / DIV** **[.5]** **[x1]**.



sb6168d

Figure 3-7. VCO Tune Adjustment Location

6. Adjust VCO TUNE with a **non-metallic** adjustment tool to 0.0 V ± 500 mV (within one division of the reference line).

The adjustment is sensitive, and if out of adjustment may display an **irregular** waveform. If so, slowly tune through the entire adjustment **range** to obtain a flat trace, then carefully tune for O.OV. Once the adjustment is done, it should be rechecked with the reference board **reinstalled** in the instrument, and at operating temperature

In Case of Difficulty

If VCO TUNE cannot be adjusted as **specified**, and the instrument passes the Analog Bus Correction Constants (**Test 44**) adjustment, the **A12** assembly must be replaced.

Frequency Accuracy Adjustment

Required Equipment and Tools (HP 8719D/20D Only)

Frequency Counter	HP 5350B
RF Cable	HP 85131C/D
Non-metallic Adjustment Tool8830-0024
Antistatic Wrist Strap9300-1367
Antistatic Wrist Strap Cord9300-0980
Static-control Table Mat and Earth Ground Wire9300-0797

Required Equipment and Tools (HP 8722D Only)

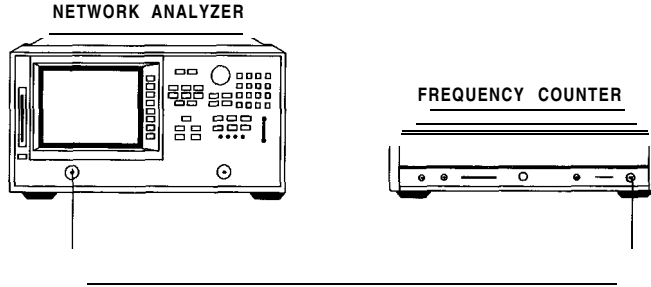
Frequency Counter (HP 8722D Only)	HP 5351B
RF Cable (HP 8722D Only)	HP 85133C/D
2.4-mm (f) to 3.5-mm (m) adapter (HP 8722D Only)	HP 11901D
Non-metallic Adjustment Tool8830-0024
Antistatic Wrist Strap9300-1367
Antistatic Wrist Strap Cord	9300-0980
Static-control Table Mat and Earth Ground Wire9300-0797

Network Analyzer warm-up time: 30 minutes.

Spectrum Analyzer warm-up time: 30 minu tes.

This adjustment sets the VCXO (voltage controlled crystal oscillator) frequency to maintain the instrument's frequency accuracy.

1. Remove the upper-rear standoffs **and** analyzer top cover.
2. Connect the equipment as shown in Figure 3-8.



sb65d

Figure 3-8. Frequency Accuracy Adjustment Setup

Note Make sure that the frequency counter and network analyzer references are NOT connected.

3. For Option 1D5 Instruments Only: Remove the rear panel BNC to BNC jumper that is connected between the “EXT REF” and the “10 MHz Precision Reference,” as shown in Figure 3-10.

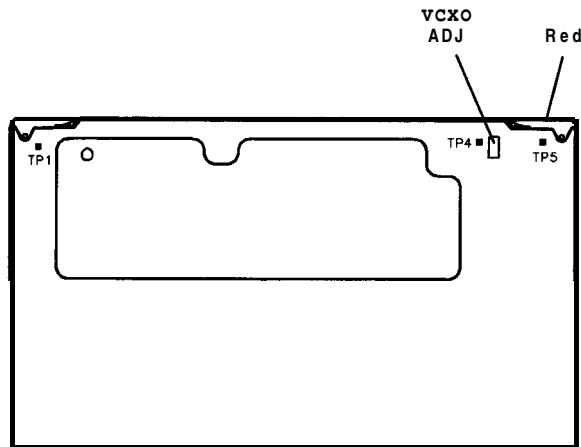
4. Press **[Preset]** **PRESET: FACTORY** **[Menu]** **CH FREQ** and select the frequency:

- For the HP 8719D, press **[13.5]** **[G/n]**.
- For the HP 8720D, press **[20]** **[G/n]**.
- For the HP 8722D, press **[26]** **[G/n]**.

5. No **adjustment** is required when the frequency counter measurement results are within specification:

- ± 135 kHz for HP 8719D
- ± 200 kHz for HP 8720D
- ± 260 kHz for HP 8722D

Otherwise, locate the **A12** assembly (red extractors) and adjust the VCXO ADJ (see **Figure 3-9**) for a frequency measurement within **specifications**.



sb616d

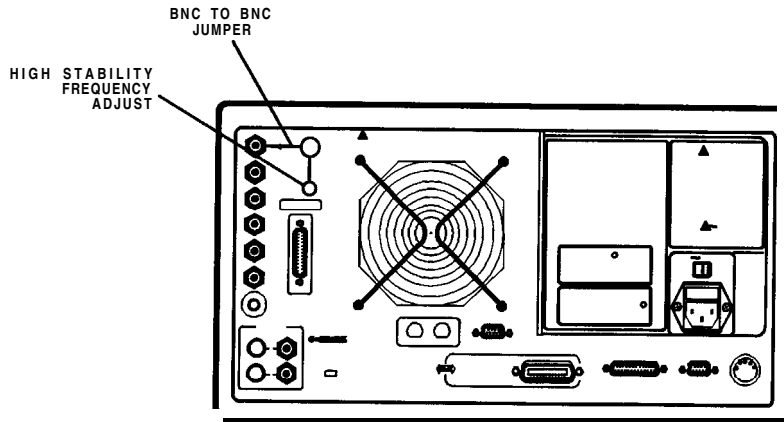
Figure 3-9. Location of the VCXO ADJ Adjustment

Note To increase the accuracy of this adjustment, the following steps are recommended.

6. Replace the instrument covers and wait 10 to 16 minutes **in** order to allow the analyzer to reach its precise operating temperature.
7. Recheck the CW frequency and adjust if necessary.

Instruments with Option **1D5** Only

8. Reconnect the BNC to BNC jumper between the “**EXT REF**” and the “10 MHz Precision Reference” as shown in **Figure 3-10**.



sb629d

Figure 3-10. High Stability Frequency Adjustment Location

9. Insert a narrow screwdriver and **adjust** the high-stability frequency reference potentiometer for a CW frequency measurement **within specification**.

In Case of Difficulty

Replace the **A26** assembly if you cannot adjust the CW frequency within **specification**.

Fractional-N Spur Avoidance and FM Sideband Adjustment

Required Equipment and Tools

Spectrum Analyzer	HP 8563E
RF Cable 50Ω , Type-N, 24-inch	8120-4781
Cable, 50Ω Coax , BNC (m) to BNC (m)	HP 10503A
Non-metallic Adjustment Tool	8830-0024
Antistatic Wrist Strap	9300-1367
Antistatic Wrist Strap Cord	9300-0980
Static-control Table Mat and Earth Ground Wire	9300-0797
(HP 8719D/20D) Adapter 3.5-mm to Type-N (f)	HP 1152545
(HP 8722D) Adapter 2.4-mm to 7-mm	HP 851303
(HP 8722D) Adapter Type-N (f) to 7-mm	HP 11524A

Analyzer warm-up time: 30 minutes.

This adjustment **minimizes** the spurs caused by the API (analog phase interpolator, on the fractional-N assembly) circuits. It also improves the sideband **characteristics**.

1. Connect the equipment as shown in **Figure 3-1**.
2. Make sure the **instruments** are set to their default HP-IB addresses:
HP **8719D/20D/22D** = 16, Spectrum Analyzer = 18.

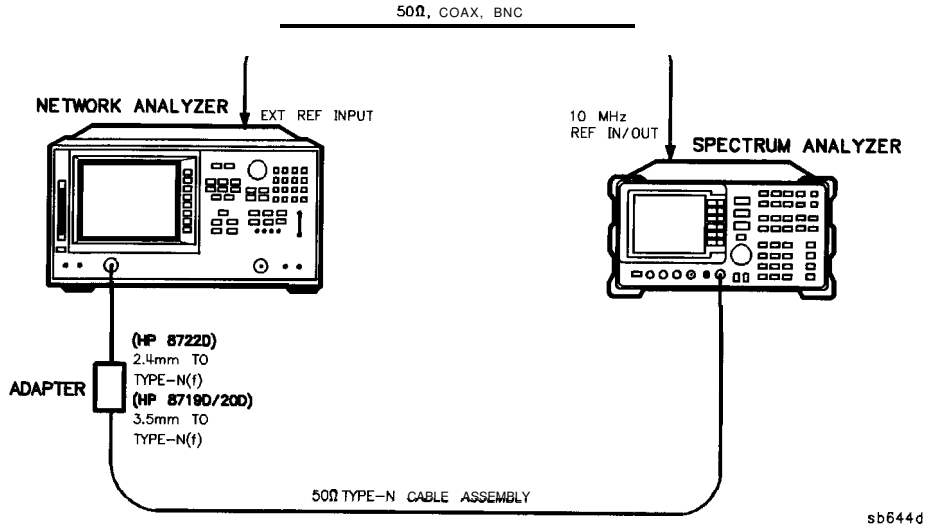
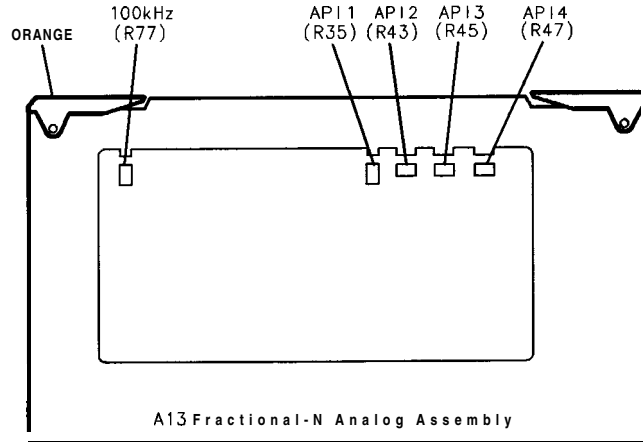


Figure 3-11.
Fractional N Spur Avoidance and FM Sideband Adjustment Setup

3. **Set** the spectrum analyzer measurement parameters as follows:

Reference Level	0 dBm
Resolution Bandwidth	100 Hz
Center Frequency	2.3451 GHz
Span	2.5 GHz

4. On the network analyzer, press **Preset** **Menu** **CW FREQ** **2.345** **G/μ**.
5. Adjust the 100 kHz (R77) for a null (minimum amplitude) on the spectrum analyzer. The minimum signal may, or may not, drop down into the noise floor.



sg69d

Figure 3-12. **Location of API and 100 kHz Adjustments**

6. On the spectrum **analyzer**, set the center frequency for 530.039 MHz.
7. On the network analyzer, press **CW FREQ** **530.036** **M/μ**.
8. Adjust the **API1 (R35)** for a null (**minimum** amplitude) on the spectrum analyzer.
9. On the spectrum analyzer, set the center frequency for 530.0066 MHz.
10. On the network analyzer, press **CW FREQ** **530.0036** **M/μ**.
11. Adjust the **API2 (R43)** for a null (minimum amplitude) on the spectrum analyzer.
12. On the spectrum analyzer, set the center frequency for 530.00336 MHz.
13. On the network analyzer, press **CW FREQ** **530.00036** **M/μ**.
14. Adjust the **API3 (R45)** for a null (minimum amplitude) on the spectrum analyzer.
15. On the spectrum analyzer, set the center frequency for 530.003036 MHz.

16. On the network analyzer, press **CW FREQ** **530.000036** **M/μ**.
17. Adjust the **API4 (R47)** for a null (**minimum** amplitude) on the spectrum analyzer.

In Case of Difficulty

1. If this adjustment can not be performed satisfactorily, repeat the entire procedure.
2. If the analyzer repeatedly fails this adjustment, replace the **A13** board assembly.

Start Troubleshooting Here

The information in this chapter helps you:

- Identify the portion of the analyzer that is at fault.
- Locate the **specific** troubleshooting procedures to identify the assembly or peripheral at fault.

To identify the portion of the analyzer at fault, follow these procedures:

- Step 1. Initial Observations
- Step 2. Operator's Check
- Step 3. **HP-IB** Systems Check
- Step 4. **Faulty** Group Isolation

Assembly Replacement Sequence

The following steps show the sequence to replace an assembly in the network analyzer.

1. Identify the faulty group. Refer to Chapter 4, “Start Troubleshooting Here.” Follow up with the appropriate troubleshooting chapter that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, “Replaceable Parts”
3. Replace the faulty assembly and determine what adjustments are necessary Refer to Chapter 14, “Assembly Replacement and Post-Repair Procedures.”
4. Perform the necessary adjustments Refer to Chapter 3, “Adjustments and Correction Constants ”
5. Perform the necessary performance **tests**. Refer to Chapter 2, “System **Verification** and Performance **Tests**.”

Having **Your** Analyzer Serviced

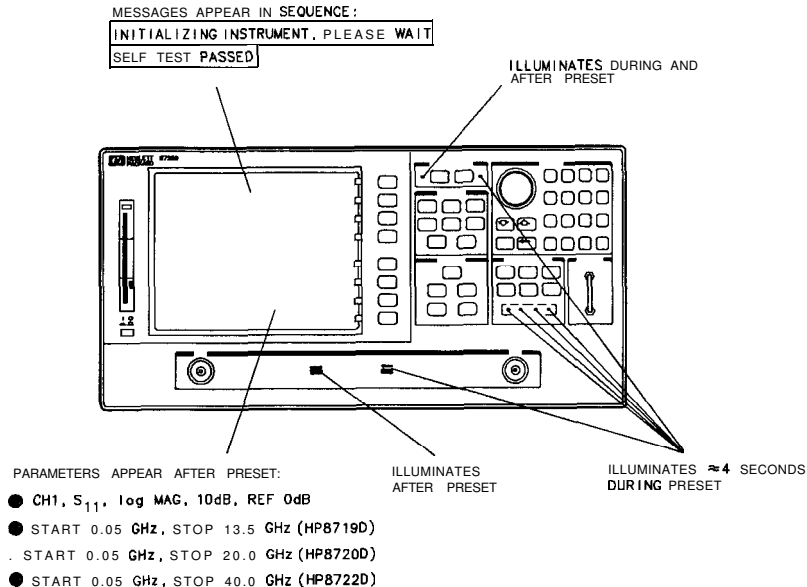
The analyzer has a one year on-site warranty, where available. If the analyzer should fail any of the following checks, call your local HP Sales and Service **office**. A customer engineer will be dispatched to service your analyzer on-site. If a customer engineer is not available in your area, follow the steps below to send your analyzer back to HP for repair.

1. Choose the nearest HP service center. (A table listing of Hewlett-Packard Sales and Service **offices** is provided at the end of this guide)
2. Include a detailed description of any failed test and any error message.
3. Ship the **analyzer**, using the original or comparable anti-static packaging **materials**.

Step 1. Initial Observations

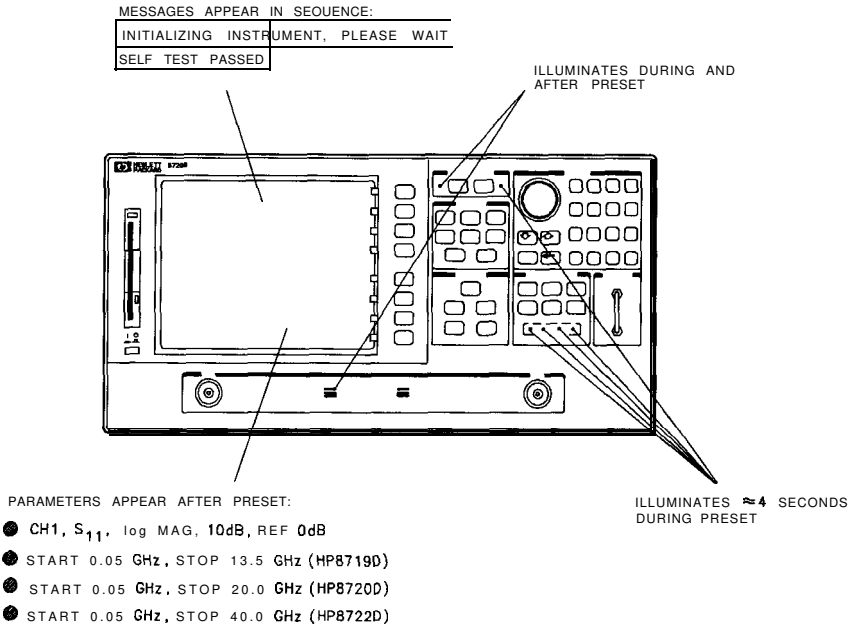
Initiate the Analyzer **Self-Test**

1. Disconnect **all** devices and peripherals from the analyzer.
2. Switch on the **analyzer** and press **PRESET** **PRESET** **FACTORY**.
3. Watch for the indications shown in **Figure 41** or **Figure 42** to determine if the analyzer is operating correctly.



sb626d

Figure 4-1. Preset Sequence for Firmware Revisions 6.xx and below



sb6167d

Figure 4-2. Preset Sequence for Firmware Revisions 7.xx and above

- If the self-test failed, refer to **“Step 4. Faulty Group Isolation”**.

Step 2. Operator's Check

Description

The operator's check consists of two **softkey** initiated tests: Op Ck Port 1 and Op Ck Port 2.

A short is connected to port 1 (port 2) to reflect all the source energy back into the **analyzer** for an **S₁₁ (S₂₂)** measurement.

The first part of OP CK PORT **1** checks the repeatability of the transfer switch. An **S₁₁** measurement is stored in memory and the switch is toggled to port 2 and then back to port 1 where another **S₁₁** measurement is made. The difference between the memory trace and the second trace is switch repeatability.

The remaining parts of both tests exercise the internal attenuator in **5 dB** steps over a **55 dB** range.

The resulting measurements must fall within a limit testing window to pass the test. The window **size** is based on both source and receiver **specifications**.

The operator's check determines that:

1. The source is phase-locked across the entire frequency range
2. All three samplers are functioning properly.
3. The transfer switch is operational.
4. The attenuator steps **5 dB** at a **time**.

Required Equipment and Poles

Short 3.5 mm (**f**) HP P/N 85052-60007
(p/o calibration kit HP 85052B)
Short 2.4 mm (**f**) (HP 8722D Only) (p/o calibration kit HP 85056B/D)

Analyzer warm-up time: 30 minutes.

Procedure

1. To run the test for port 1, press **PRESET** **PRESET - FACTORY** **SYSTEM** **SERVICE MENU** **TESTS** **EXTERNAL TESTS**.
2. The display should show TEST 21 Op Ck Port 1 in the active entry area.
3. Press **EXECUTE TEST** to begin the test.
4. At the prompt, connect the short to the port indicated. Make sure the connection is tight.
5. Press **CONTINUE**.
6. The test is a sequence of **subtests**. At the end of the subtests, the test title and result will be displayed. If all tests pass successfully, the overall test status will be PASS. If any test fails, the overall test status will be FAIL.
7. To run the test for port 2, press the step **⏮** key. The display should show **TEST 22 Op Ck** Port 2 in the active entry area.
8. Repeat steps 3 through 7.
9. If both tests pass, the analyzer is about 80% verified. If either test fails, refer to “Step 4. Faulty Group Isolation” in this section, or:
 - a. Make sure that the connection is tight. Repeat the test.
 - b. Visually inspect the connector interfaces and clean if necessary (refer to “Principles of Microwave Connector Care” located in Chapter 1).
 - c. Verify that the short meets published specifications
 - d. Substitute another short, and repeat the test.
 - e. **Finally**, refer to the detailed tests located in this section, or fault isolation procedures located in the troubleshooting **sections**.

Step 3. HP-IB Systems Check

Check the analyzer's **HP-IB** functions with a *known working* passive peripheral (such as a plotter, printer, or disk drive).

1. Connect the peripheral to the **analyzer** using a *known good* HP-IB cable.
2. Press **LOCAL SYSTEM CONTROLLER** to enable the analyzer to control the peripheral.
3. Then press **SET ADDRESSES** and the appropriate **softkeys** to verify that the device addresses will be recognized by the analyzer. The factory default addresses are:

Device	HP-IB Address
HP 8719D/20D/22D	16
Plotter port	5
Printer port	1
Disk (external)	0
Controller	21
Power meter	13

Note

You may use other addresses with two provisions:

- Each device must have its own address
- The address set on each device must match the one recognized by the analyzer (and displayed).

Peripheral addresses are often set with a rear panel switch. Refer to the manual of the peripheral to read or change its address

If Using 8 Plotter or Printer

1. Ensure that the plotter or **printer** is set up correctly:
 - power is on
 - pens and paper loaded
 - pinch wheels are down
 - some plotters need to have **P1** and **P2** positions set
2. Press **COPY** and then **PLOT** or **PRINT MONOCHROME**.
 - If the result is a copy of the analyzer display, the printing/plotting features are functional in the analyzer. Continue with “Troubleshooting Systems with Multiple Peripherals,” “Troubleshooting Systems with Controllers,” or the “Step 4. **Faulty** Group Isolation” section in this chapter.
 - If the result is not a copy of the analyzer display, refer to Chapter 6, “Digital Control Troubleshooting.”

If Using an External Disk Drive

1. Select the external disk drive. Press **SAVE/RECALL** **SELECT DISK** **EXTERNAL DISK**.
2. Verify that the address is set correctly. Press **LOCAL** **SET ADDRESSES** **ADDRESS DISK**.
3. Ensure that the disk drive is set up correctly:
 - power is on
 - an initialized disk in the correct drive
 - correct disk unit number and volume number (press **LOCAL** to access the **softkeys** that display the numbers; default is 0 for both)
 - with hard disk (Winchester) drives, make sure the configuration switch is properly set (see drive manual)

4. Press **START** **1** **M/μ** **SAVE/RECALL** **SAVE STATE**. Then press **PRESET** **PRESET: FACTORY** **SAVE/RECALL** **RECALL STATE**.
- If the resultant trace starts at 1 MHz, HP-IB is functional in the analyzer. Continue with “Troubleshooting Systems with Multiple Peripherals,” “Troubleshooting Systems with Controllers,” or the “Step 4. Faulty Group Isolation” section in this chapter.
 - If the resultant trace does not start at 1 MHz, suspect the HP-IB function of the analyzer: refer to Chapter 6, “Digital Control Troubleshooting.”

Troubleshooting Systems with Multiple Peripherals

Connect any other system peripherals (but not a controller) to the analyzer one at a time and check their functionality. Any problems observed are in the peripherals, cables, or are address problems (see above).

Troubleshooting Systems with Controllers

Passing the preceding checks indicates that the analyzer’s peripheral functions are normal. Therefore, if the analyzer has not been operating properly with an external controller, check the following:

- The HP-IB interface hardware is incorrectly **installed** or not operational. (See ‘HP-IB Requirements’ in the HP *8719D/20D/22D Network Analyzer User’s Guide*.)
- The programming syntax is incorrect. (Refer to the *HP 8719D/20D/22D Network Analyzer Programmer’s Guide*.)

If the analyzer appears to be operating unexpectedly but has not completely failed, go to “Step 4. Faulty Group Isolation.”

Step 4. Faulty Group Isolation

Use the following procedures only if you have read the previous sections in this chapter and you think the problem is in the analyzer. These are **simple** procedures to verify the five functional groups in sequence, and determine which group is faulty.

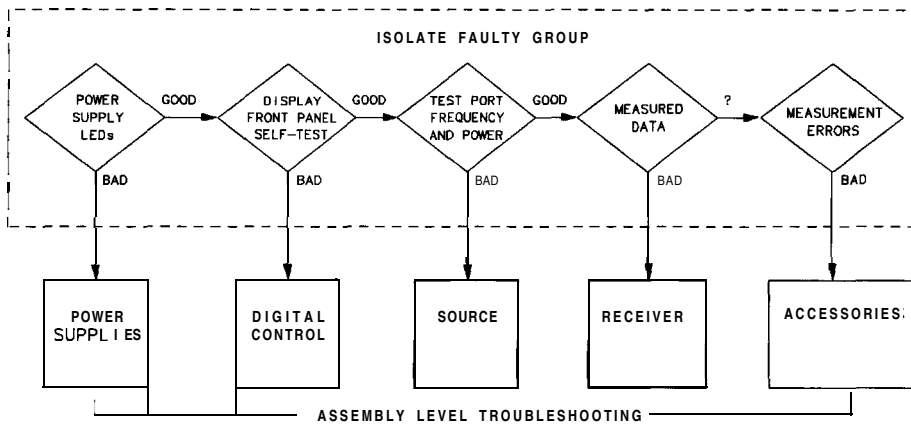
The **five** functional groups are:

- power supplies
- digital control
- source
- receiver
- accessories

Descriptions of these groups are provided in Chapter 12, “Theory of Operation.”

The checks in the following pages must be performed in the order presented. If one of the procedures fails, it is an indication that the problem is in the functional group checked. Go to the troubleshooting information for the indicated group, to isolate the problem to the defective assembly.

Figure 4-3 illustrates the troubleshooting organization.



sg645d

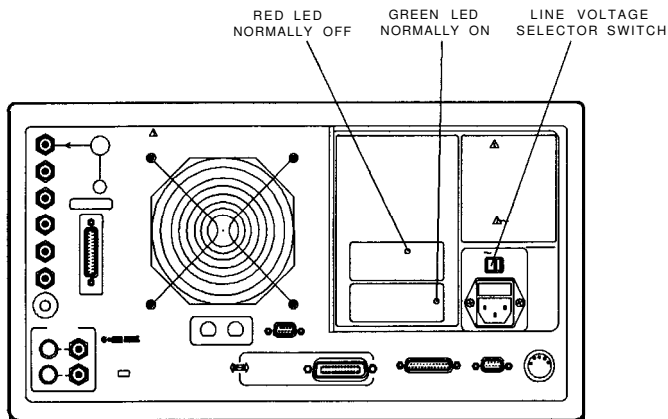
Figure 4-3. Troubleshooting Organization

Power Supply

Check the Rear **Panel LEDs**

Switch on the analyzer and look directly at the rear panel. Notice the condition of the two **LEDs** on the **A15** preregulator. (See **Figure 4-4**.)

- ❑ The upper (red) LED should be off.
- ❑ The lower (green) LED should be on.



sb618d

Figure 4-4. **A15 Preregulator LEDs**

Check the **A8** Post Regulator **LEDs**

Remove the analyzer's top cover. Switch on the power. Inspect the green **LEDs** along the top edge of the **A8** post-regulator assembly.

- ❑ All green **LEDs** should be on.
- ❑ **The** fan should be audible.

In case of **difficulty**, refer to Chapter 5, “Power Supply Troubleshooting.”

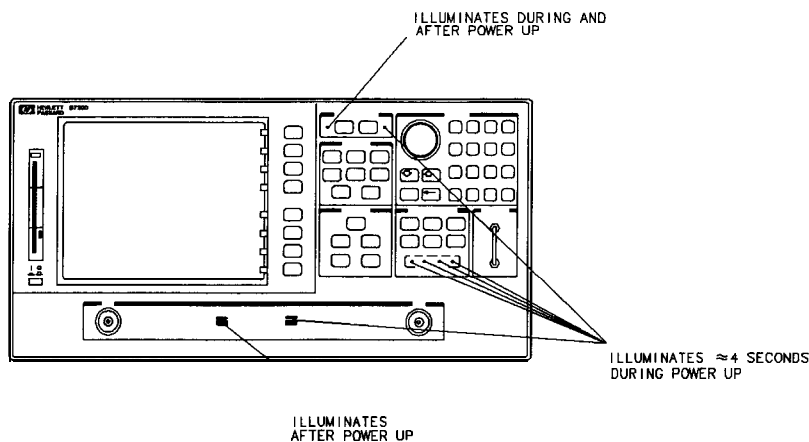
Digital Control

Observe the **Power** Up Sequence (**firmware** revisions **6.xx** and below)

Switch the analyzer power off, then on. The following should take place **within** a few seconds:

- On the front panel observe the following:
 1. All six amber **LEDs illuminate**.
 2. The port 2 LED **illuminates**.
 3. The amber **LEDs** go off after a few seconds, except the CH 1 LED. At the same moment, the port 2 LED goes off and the port 1 LED **illuminates**.
(See Figure 4-5.)
- The display should come up bright with no irregularity in colors
- **Four** red **LEDs** on the **A9** CPU board should **illuminate**. They can be observed through a small opening in the rear panel.

If the power up sequence does not occur as described, or if there are problems **using** the front panel keyboard, refer to Chapter 6, “Digital Control Troubleshooting. ”



sb625d

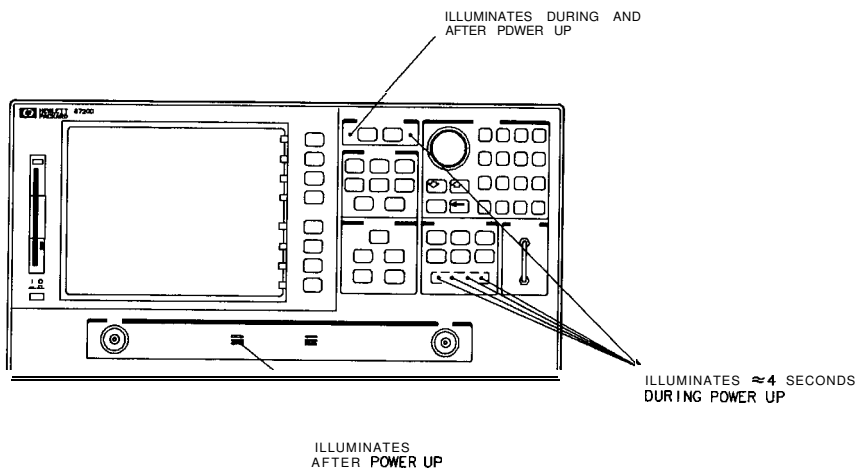
Figure 45. Front Panel Power Up Sequence

Observe the **Power Up Sequence** (**firmware** revisions **7.xx** and above)

Switch the analyzer power **off**, then on. The following should take place within a few seconds:

- On the front panel observe the following:
 1. All six amber **LEDs** illuminate.
 2. **The port 2 LED illuminates.**
 3. **The amber LEDs** go off after a few seconds, except the CH 1 LED. At the same moment, the port 2 LED goes off and the port 1 **LED** illuminates (See **Figure 46.**)
- The display should come up bright with no irregularity in colors.
- After an initial pattern, five red **LEDs** on the **A9** CPU board should remain off. They can be observed through a small opening in the rear panel.

If the power up sequence does not occur as described, or if there are problems using the front panel keyboard, refer to Chapter 6, “Digital Control Troubleshooting.”



sb6166d

Figure 4-6. Front Panel Power Up Sequence

Verify Internal **Tests** Passed

1. Press **PRESET** **PRESET: FACTORY** **SYSTEM** **SERVICE MENU** **TESTS** **INTERNAL TESTS** **EXECUTE TEST**. The display should indicate:

TEST

0 ALL **INT** PASS

- ❑ If your display shows the above message, go to step 2. Otherwise, continue with this step.
 - ❑ If phase lock error messages are present, this test may stop without passing or failing. In this case, continue with the next procedure to check the **source**.
 - ❑ If you have unexpected results, or if the analyzer indicates a specific test **failure**, refer to Chapter 6, “Digital Control Troubleshooting.” The analyzer reports the **first failure** detected.
 - ❑ If the analyzer indicates **failure** but does not identify the test, press **⇧** to search for the **failed** test. Then refer to Chapter 6, “Digital Control Troubleshooting.” Likewise, if the response to front panel or HP-IB commands is unexpected, troubleshoot the digital control group.
2. Press **19** **x1** **0300-0100 1050** to perform the Analog Bus test.
 - ❑ If this test **fails**, refer to Chapter 6, “Digital Control Troubleshooting.”
 - ❑ If this test passes, continue with the next procedure to check the source.

Source

Phase Lock Error Messages

The following list contains all phase lock error messages and their descriptions.

- **NO IF FOUND: CHECK R INPUT LEVEL**

The **first IF** was not detected **during** the pretune stage of phase lock.

- **NO PHASE LOCK: CHECK R INPUT LEVEL**

The **first IF** was detected at the **pretune** stage but phase lock could not be acquired thereafter.

- **PHASE LOCK LOST**

Phase-lock was acquired but then lost.

- **PHASE LOCK CAL FAILED**

An internal phase lock calibration routine is automatically executed at power-on, when pretune values drift, or when phase lock problems are detected. A problem aborted a calibration attempt.

- **POSSIBLE FALSE LOCK**

The **analyzer** is achieving phase lock but possibly on the wrong harmonic comb tooth.

- **SWEEP TIME TOO FAST**

The fractional-N and the digital **IF** circuits have lost synchronization.

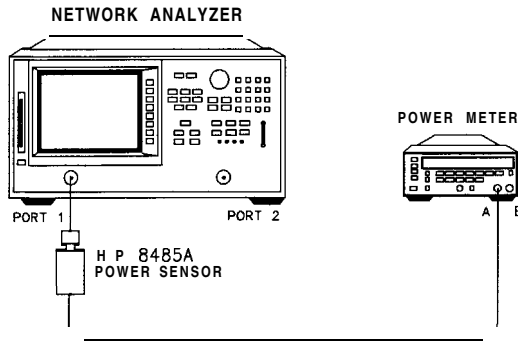
The error messages listed above are usually indicative of a source **failure** or improper **instrument configuration**. As a **preliminary** step, ensure that all option jumper cables are properly **connected**. To ensure that the R channel input is receiving at least -35 **dBm** power, perform the following steps:

1. Perform steps 1 and 2 of the “Source **Pretune** Correction Constants” procedure located in Chapter 3. Make note of the DAC number that is displayed and then abort the procedure
2. Press **(SYSTEM)** **SERVICE MENU** **SERVICE MODES** **SRC ADJUST MENU** **DAC FOR HIGH BAND**.
3. Enter the DAC number determined from step 1 and press **(x1)**.

4. Disconnect the front panel **R** CHANNEL jumper.
5. Zero and calibrate a power meter. Measure the power at R CHANNEL OUT .

Check Source Output Power

1. Zero and calibrate the power meter.
2. Connect the equipment as shown in **Figure 4-7**.



sb64d

Figure 4-7. Equipment Setup for Source Power Check

3. Press **PRESET** **PRESET: FACTORY** on the analyzer to initialize the instrument.
4. For the HP 8719D/20D, press **MENU** **POWER** **5** **(10)**, Option **007** [x1] **RETURN** **CV 0120** to check power at 1 GHz.
5. For the HP 8722D, press **MENU** **POWER** **-10** **(-5)**, Option **007** **x1** **RETURN** **CV 0120** to check power at 1 GHz.
6. On the power meter, set the calibration factor for the value on the power sensor that corresponds to 1 GHz.
7. For the HP 8719D, press **(1)** repeatedly to check power at **2, 5, 10, and 13.5 GHz**, setting the power meter to the corresponding calibration factors for each frequency.

The power should be within **±2 dBm** of the set **value**.

8. For the HP 8720D, press **(F)** repeatedly to check power at 2, 5, 10, and 20.0 GHz.

The power **should** be within **± 2 dBm** of the set value.

9. For the HP 8722D, press **(F)** repeatedly to check power at 2, 5, 10, 20, and 40.0 GHz.

The power should be within **± 2 dBm** of the set value.

10. Press **(MEAS)** **Box 1: REV S22 (B/R)** and connect the power sensor to port 2. Repeat the measurement from port 2. If the power is not within **specification** at either port, go to the “Source Troubleshooting” chapter to continue troubleshooting.

No Oscilloscope or Power Meter? **Try** the **ABUS**

Monitor **ABUS** node 9.

1. Press **PRESET** **PRESET: FACTORY** **START** **50** **M/μ** **STOP** **20** **G/n** **SYSTEM**
SERVICE MENU **ANALOG BUS ON**.
2. **MEAS** **ANALOG IN Aux Input** **9** **X1**.
3. **FORMAT** **MORE** **REAL** **SCALE REF** **AUTOSCALE**.

The display should resemble **Figure 4-8**. If any of the above procedures provide unexpected results, or if error messages are present, refer to Chapter 7, “Source Troubleshooting.”

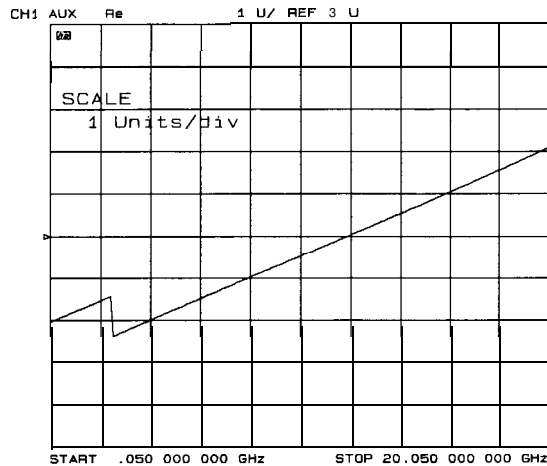


Figure 4-8. 0.25V/GHz Waveform at Abus Node 9

Receiver

If any input shows unexpected results, go to the “Receiver Troubleshooting” section. Otherwise, proceed to Accessories.

1. For the HP 8719D/20D, perform the following steps:

- a. Press **PRESET** **PRESET: FACTORY** **MEAS** **INPUT PORTS** **1**. The trace should show a **relatively flat line at about +5 ±2 dB (+10 dB, Option 007)**.
- b. Connect an open or short calibration standard to port 1. Press **1** to look at input A (port 1). The trace should resemble Figure 49 **below, with a minimum of about -35 dB at 50 MHz and a value around +5 ±2 dB (+10 dB, Option 007) over the flat section**.
- c. To check input B (**port 2**), **connect** an open or short calibration standard to port 2, then press **5** **TESTPORT 2** to drive port 2. Again, the trace should resemble Figure 4-9 below.

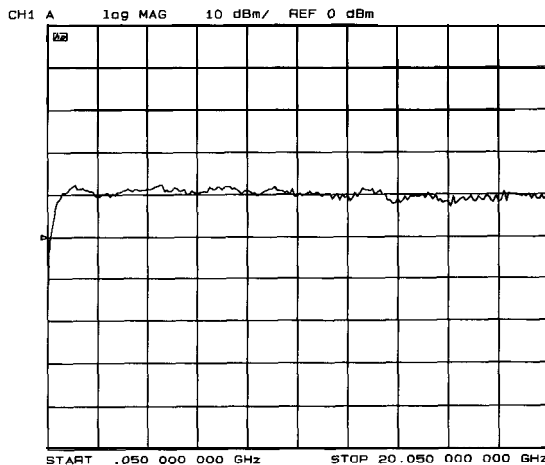


Figure 4-9. Typical Trace

2. For the HP 8722D, perform the following steps:
 - a. Press **PRESET** **PRESET: FACTORY** **MEAS** **INPUT PORTS** **R**. The trace should show a relatively **flat** line at about $-10 \pm 2 \text{ dB}$ (-5 dB , Option 007).
 - b. Connect an open or short calibration standard to port 1. Press **A** to look at input A (port 1). The trace should be **similar** to Figure 47, with the exception of having a minimum of about -50 dB at 50 MHz and a value around $-10 \pm 2 \text{ dB}$ (-5 dB , Option 007) over the flat section.
 - c. To check input B (port 2), connect an open or short calibration standard to **port 2**, then press **B** **TESTPORT 2** to drive port 2. Again, the trace should have the same characteristics as described in the preceding step.

Switch Repeatability

Calibration does not compensate for the repeatability of the transfer switch in instruments. As a result, the switch can be a source of error. To check the switch, use the following procedure:

1. Press **Preset** **PRESET: FACTORY** **Avg** **IF BW** **100** **x1**, **AVERAGING FACTOR** **4** **x1** **AVERAGING ON** to set the bandwidth to 100 Hz and take 4 averages
2. Press **Cal** **CALIBRATE MENU** **RESPONSE** to access the response calibration menu.
3. Connect a short to test port 1 and press **SHORT**.
4. Press **Display** **DATA → MEM** **DATA/MEM** **Scale Ref** **.01** **x1** to display data/memory and scale the trace.
5. Press **Meas** and then repeatedly (6 to 12 times) press **Ref1: REV S22 (B/R)** **Ref1: FWD S11 (A/R)** to switch back and forth between S_{22} and S_{11} 6 to 12 times Return to the S_{11} measurement condition.
After 4 averages, the trace should look **similar** to Figure 410.
6. Press **Meas** **Ref1: REV S22 (B/R)**.
7. Repeat steps 2, 3 and 4, only this time connect a short to port 2 and monitor the **S22** trace.

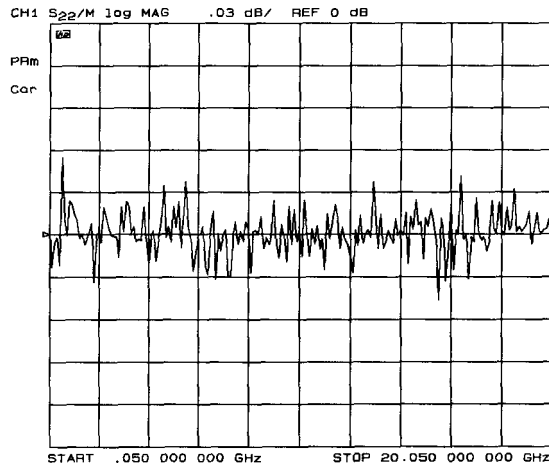


Figure 4-10. Typical Switch Repeatability Trace

Accessories

If the analyzer has passed all of the above checks but is still making incorrect measurements, suspect the system accessories Accessories such as RF or interconnect cables, calibration or **verification** kit devices, and adapters can all induce system problems

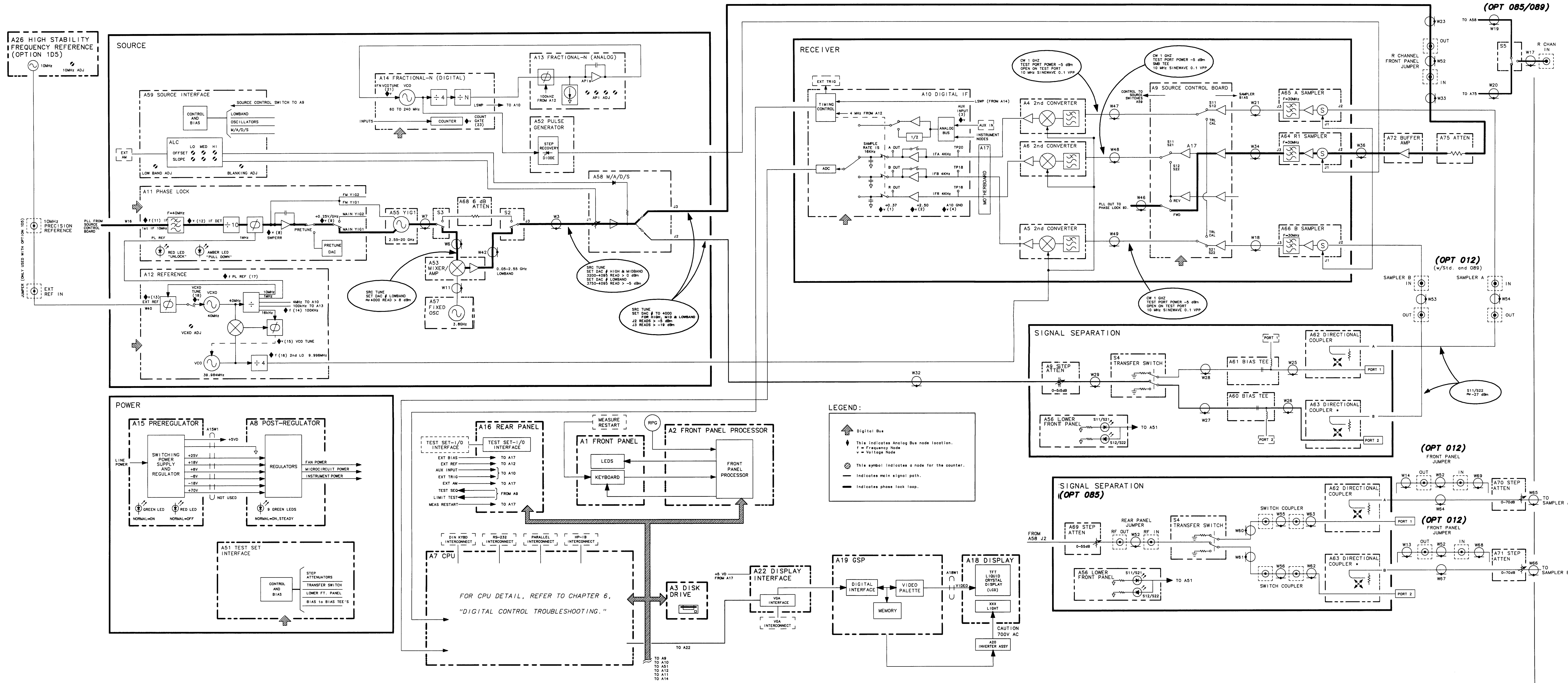
Reconfigure the system as it is normally used and reconfirm the problem. Continue with Chapter 9, "Accessories Troubleshooting. "

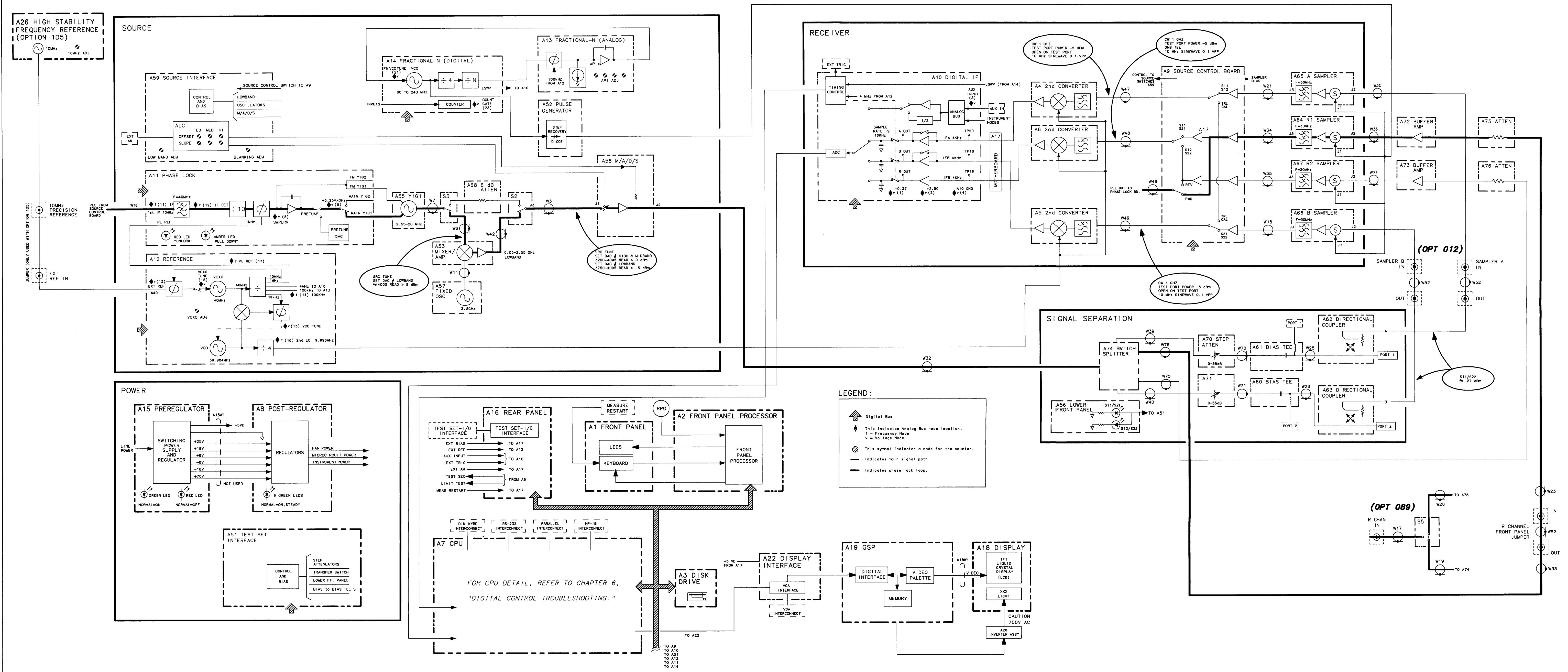
(oversized art) /08720/90292/art/sb6122d.hpg

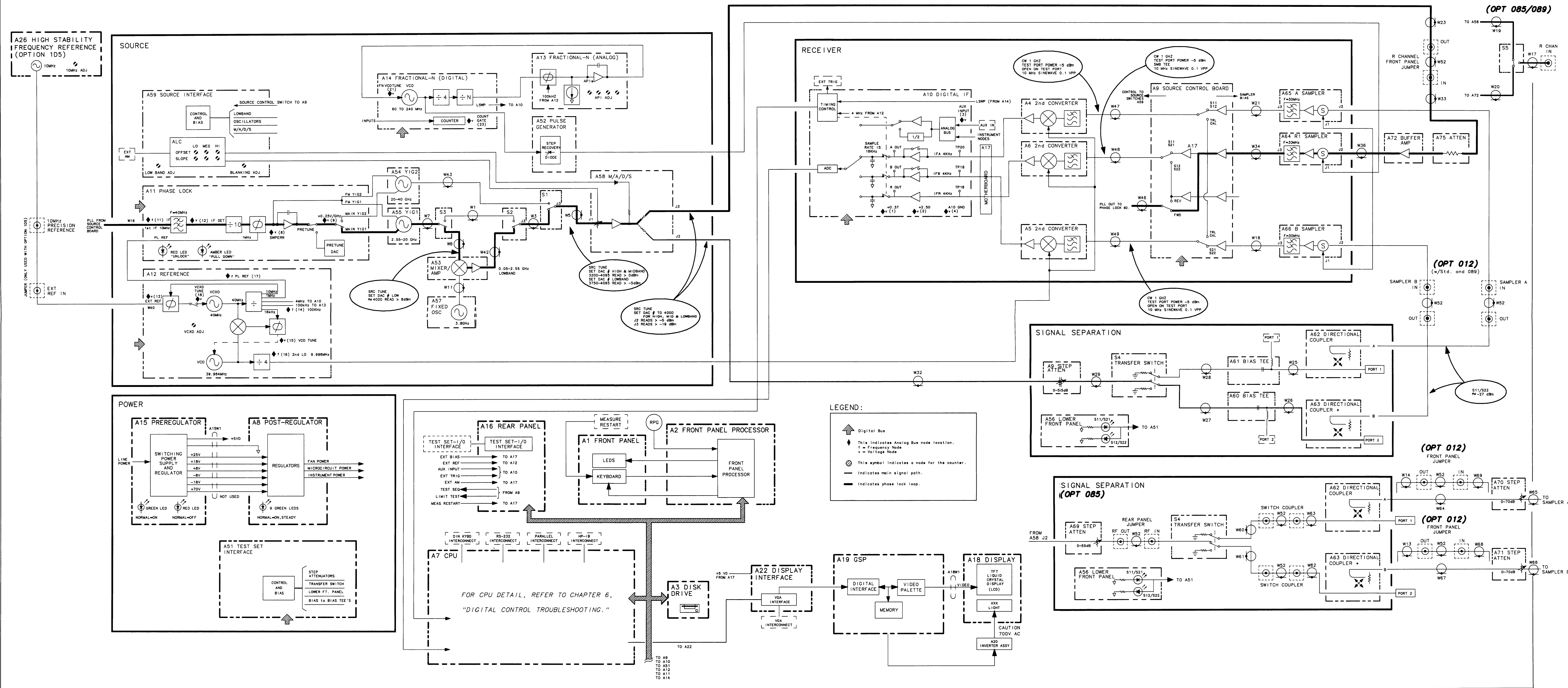
Figure 411. HP 8719D/20D/22D Overall Block Diagram

Start **Troubleshooting** Hen **4-23**









Power Supply Troubleshooting

Use this procedure only if you have read Chapter 4, “Start Troubleshooting Here.” Follow the procedures in the order given, unless:

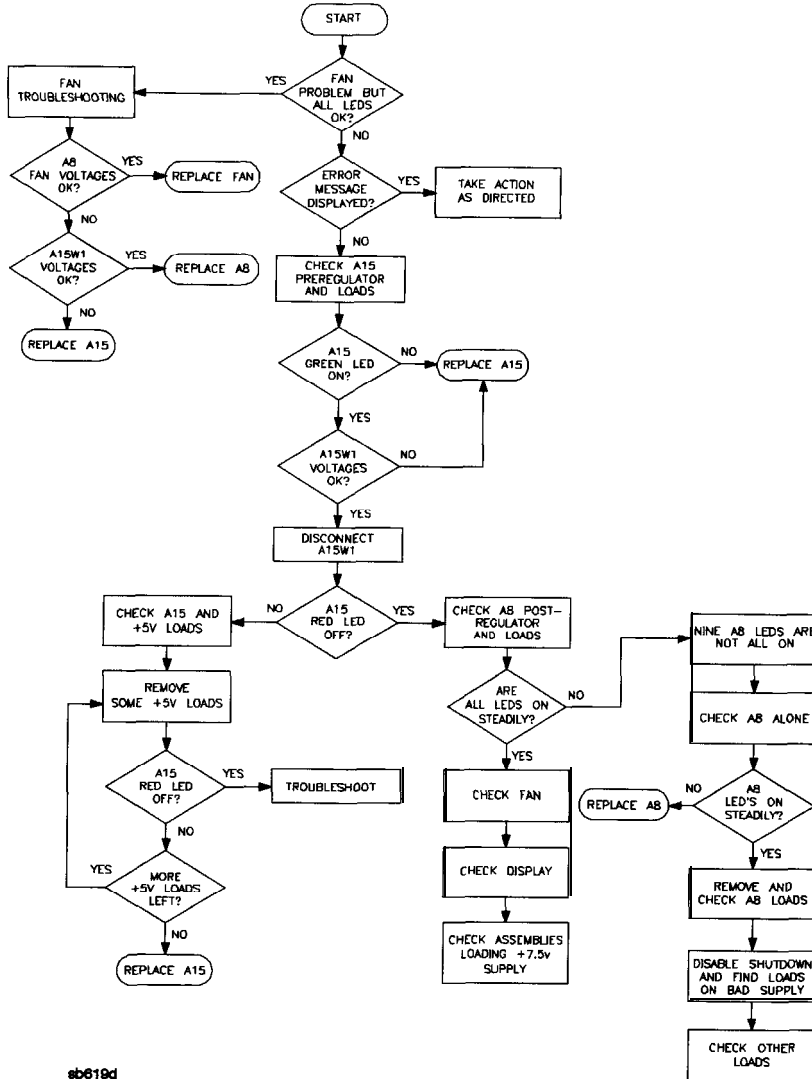
- an error message appears on the display, refer to “Error Messages” near the end of this chapter.
- the fan is not working, refer to “**Fan** Troubleshooting” in this chapter.

The power supply group assemblies consist of the following:

- **A8** post regulator
- **A15** preregulator

All assemblies, however, are related to the power supply group because power is supplied to each assembly.

Power Supply Troubleshooting Flowchart



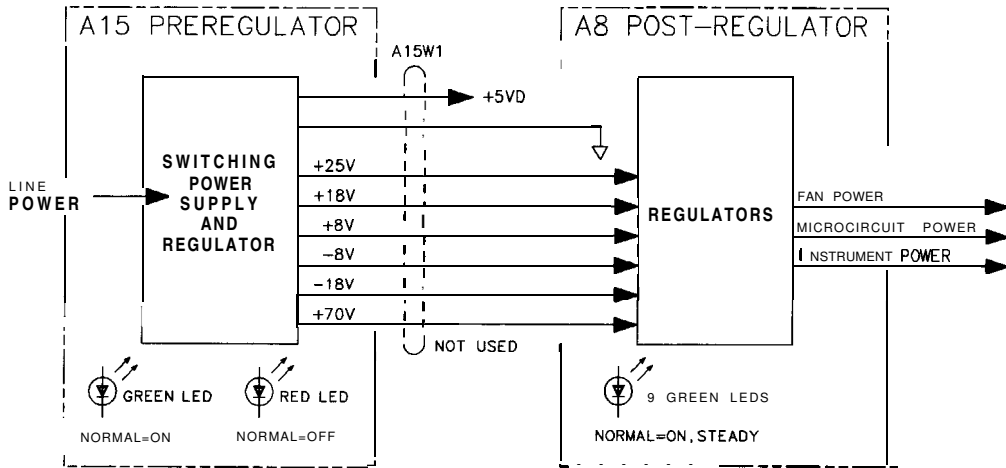
Assembly Replacement Sequence

The following steps show the sequence to replace an assembly in the network analyzer.

1. Identify the faulty group. Refer to Chapter 4, “Start Troubleshooting Here.” Follow up with the *appropriate troubleshooting chapter* that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, “Replaceable Parts.”
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, “Assembly Replacement and Post-Repair Procedures”
4. Perform the necessary adjustments Refer to Chapter 3, “Adjustments and Correction Constants”
5. Perform the necessary performance **tests**. Refer to Chapter 2, “System **Verification** and Performance **Tests**.”

Simplified Block Diagram

Figure 5-1 shows the power supply group in **simplified** block diagram form. Refer to the detailed block diagram of the power supply (Figure 5-7) located at the end of this chapter to see voltage lines and **specific** connector pin numbers.



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Figure 5-1. Power Supply Group Simplified Block Diagram

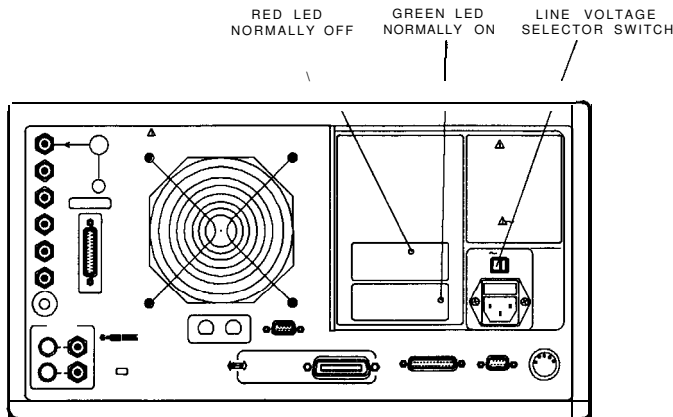
Start Here

Check the Green LED and Red LED on **A15**

Switch on the analyzer and look at the rear panel of the analyzer. Check the two power supply diagnostic **LEDs** on the **A15** preregulator casting by looking through the holes located to the left of the line voltage selector switch. (See **Figure 5-2**.)

During normal operation, the bottom (green) LED is on and the top (red) LED is off. If these **LEDs** are normal, then **A15** is 95% verified. Continue to “Check the Green **LEDs** on **A8**.”

- If the green LED is not on steadily, refer to “If the Green LED of the **A15** is Off or Blinking” in this procedure.
- If the red LED is on or **flashing**, refer to “If the Red LED of the **A15** is On” in this procedure.



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Figure 5-2. Location of A15 Diagnostic LEDs

Check the Green LEDs on A8

Remove the top cover of the analyzer and locate the **A8** post regulator; use the location diagram under the top cover if necessary. Check to see if the green **LEDs** on the top edge of **A8** are all on. There are nine green **LEDs** (one is not visible without removing the PC board stabilizer).

- If all of the green **LEDs** on the top edge of **A8** are on, there is a 95% **confidence** level that the power supply is verified. **To confirm** the last 5% uncertainty of the power supply, refer to "Measure the Post Regulator Voltages" (next).
- If any LED on the **A8** post regulator is off or flashing, refer to "If the Green **LEDs** of the **A8** are not All ON" in this procedure.

Measure the Post Regulator Voltages

Measure the DC voltages on the test points of **A8** with a voltmeter. Refer to **Figure 5-3** for test point locations and **Table 5-1** for supply voltages and limits

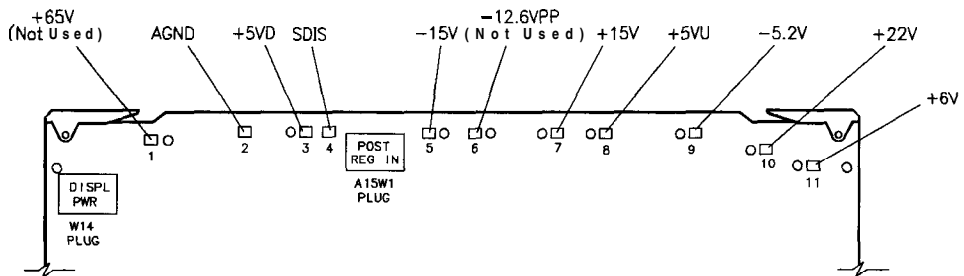


Figure 5-3. A8 Post Regulator Test Point Locations

Table 5-1. AS Post Regulator Test Point Voltages

TP	Supply	Range
1	+ 65 V (Not Used)	+ 64.6 to + 65.4
2	AGND	n/a
3	+ 5 VD	+ 4.9 to + 5.3
4	SDIS	n/a
5	- 15 V	-14.4 to -15.6
6	-12.6 PP (Not Used)	-12.1 to -12.8
7	+ 15 V	+ 14.5 to + 15.5
8	+ 5 VU	+ 5.05 to + 5.35
0	-5.2 V	-5.0 to -5.4
10	+ 22 V	+ 21.3 to + 22.7
11	+ 6 V	+ 5.8 to + 6.2

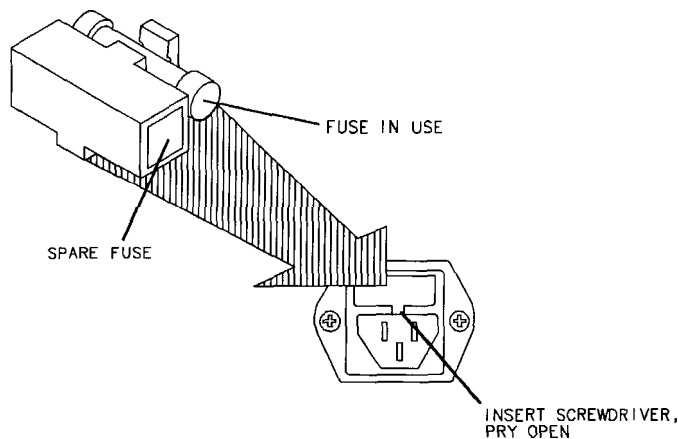
If the Green LED of the **A15** is Off or Blinking

If the green LED is not on steadily, the line voltage is not enough to power the analyzer.

Check the Line Voltage, Selector Switch, and Fuse

Check the main power line cord, line fuse, line selector switch setting, and actual line voltage to see that they are **all** correct. **Figure 5-4** shows how to remove the line fuse, using a small flat-blade screwdriver to pry out the fuse holder. **Figure 5-2** shows the location of the line voltage selector switch. Use a small flat-blade screwdriver to select the correct switch position.

If the **A15** green LED is still not on steadily, replace **A15**.



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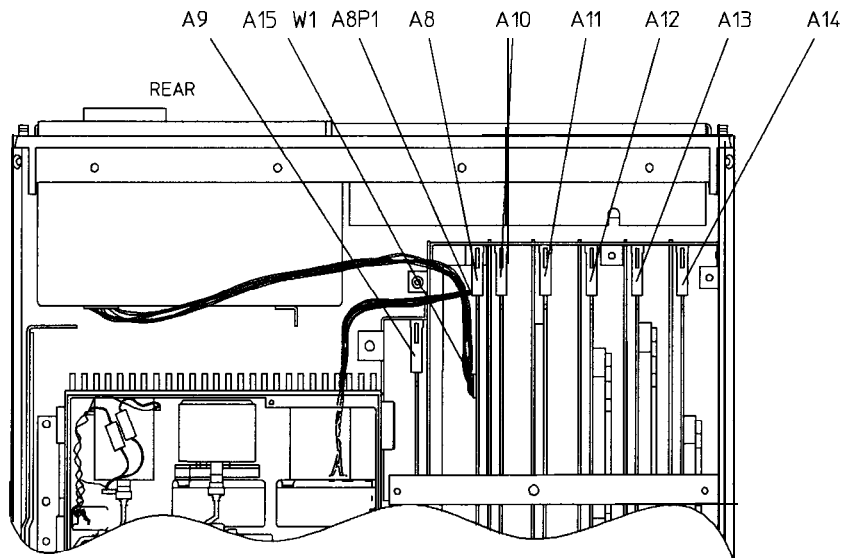
Figure 5-4. Removing the **Line Fuse**

If the Red LED of the **A15** is On

If the red LED is on or **flashing**, the power supply is shutting down. Use the following procedures to determine which assembly is causing the problem.

Check the **A8** Post Regulator

1. Switch off the analyzer.
2. Disconnect the cable **A15W1** from the **A8** post regulator. (See **Figure 5-5**.)
3. Switch on the analyzer and observe the red LED on **A15**.
 - ❑ If the red LED goes out, the problem is probably the **A8** post regulator. Continue to “Verify the **A15** Preregulator” to **first** verify that the inputs to **A8** are correct.
 - ❑ If the red LED is still on, the problem is probably the **A15** preregulator, or one of the assemblies obtaining power from it. Continue with “Check for a Faulty Assembly.”



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Figure 5-5. Power Supply **Cable** Locations

Verify the **A15** Preregulator

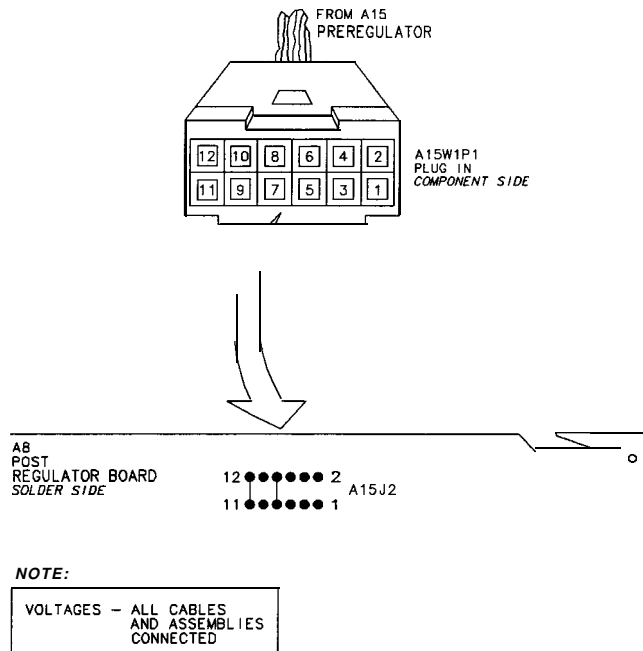
Verify that the **A15** preregulator is supplying the correct voltages to the **A8** post regulator. Use a voltmeter with a small probe to measure the output voltages of **A15W1**'s plug. Refer to **Table 5-2** and **Figure 5-6**.

- If the voltages are not within tolerance, replace **A15**.
- If the voltages are within tolerance, **A15** is verified. Continue to “Check for a Faulty Assembly.”

Table 5-2. Output Voltages

Pin	A15W1P1 (Disconnected) Voltages	A8J2 (connected) Voltages	A15 Preregulator Mnemonic
1	+100 to +125	+68 to +75.9	+70 V (not used)
2	N/C	N/C	N/C
3,4	+22.4 to +33.6	+17.0 to +18.4	+18 V
5,6	-22.4 to -33.6	-17.0 to -18.4	-18 V
7	N/C	+7.4 to +8.0	N/C
8	+9.4 to +14	+7.4 to +8.0	+8 V
9,10	-9.4 to -14	-6.7 to -7.3	-8 V
11	+32 to +48	+24.6 to +26.6	+25 V
12	N/C	+24.6 to +26.6	N/C

NOTE: The +5 VD supply must be loaded by one or more assemblies at all times, or the other voltages will not be correct. It connects to the motherboard connector **A17J3** Pin 4.



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Figure 5-6. A15W1 Plug Detail

Check for a Faulty Assembly

This procedure checks for a **faulty** assembly that might be shutting down the **A15 preregulator** via one of the following lines (also refer to Figure 5-1):

- **A15W1** connecting to the **A8** post regulator
- the **+5VCPU** line through the motherboard
- the **+5VDIG** line through the motherboard

Do the following:

1. **Switch off the analyzer.**
2. Ensure that **A15W1** is reconnected to **A8**. (Refer to Figure 5-5.)
3. Remove or disconnect the assemblies listed in Table 5-3 one at a time and in the order shown. The assemblies are sorted from most to least accessible. Table 5-3 **also lists** any associated assemblies that receive power from

the assembly that is being removed. After each assembly is removed or disconnected, switch on the analyzer and observe the red LED on A15.

Note

- *Always switch off the analyzer before removing or disconnecting assemblies.*
- When extensive disassembly is required, refer to Chapter 14, “Assembly Replacement and Post-Repair Procedures ”
- Refer to Chapter 13, “Replaceable Parts,” to identify specific cables and assemblies that are not shown in this chapter.

- If the red LED goes out, the particular assembly removed, or one receiving power from it, is faulty.
- If the red LED is still on after you have checked all of the assemblies listed in Table 6-3, continue to “Check the Operating Temperature.”

Table 5-3.

Recommended Order for Removal/Disconnection for Troubleshooting **the A15** Assembly

Assembly To Remove	Removal or Disconnection Method	other Assemblies that Receive Power from the Removed Assembly
1. A14 Frac N Digital	Remove from Card Cage	None
2. A51 Test Set Interface	Disconnect wso	S4 Transfer Switch A56 LED Front Panel
3. A7 CPU	Disconnect W91 from A7	A3 Disk Drive
4. A22 Display Interface	Disconnect W37	A18 Display
5. A2 Front Panel Interface	Disconnect W83 from A2	A1 Front Panel Keyboard

Check the Operating **Temperature**

The temperature sensing circuitry inside the A15 preregulator may be shutting down the supply. Make sure the temperature of the open air operating environment does not exceed 55 °C (131 °F), and that the analyzer fan is operating.

- If the fan does not seem to be operating correctly, refer to “**Fan Troubleshooting**” at the end of this chapter.
- If there does not appear to be a temperature problem, it is likely that A15 is faulty.

Inspect the Motherboard

If the red LED is still on after replacement or repair of A15, switch off the analyzer **and** inspect the motherboard for solder bridges, and other noticeable defects. Use an ohmmeter to check for shorts. The +5VD, +5VCPU, or +5VDSENSE lines may be bad. Refer to the block diagram (Figure 5-7) at the end of this chapter and troubleshoot these suspected power supply lines on the A17 motherboard.

If the Green **LEDs** of the A8 are not All ON

The green LEDs along the top edge of the A8 post regulator are normally on.

Flashing LEDs on A8 indicate that the shutdown circuitry on the A8 post regulator is protecting power supplies from overcurrent conditions by repeatedly shutting them down. This may be caused by supply loading on A8 or on any other assembly in the analyzer.

Remove A8, **Maintain A15W1** Cable Connection

1. Switch off the analyzer.
2. Remove A8 from its motherboard connector, but keep the A15W1 cable connected to A8.
3. Short A8TP2 (AGND) (see Figure 5-3) to chassis ground with a clip lead.
4. Switch on the analyzer and observe the green LEDs on A8.
 - ❑ If any green LEDs other than +5VD are still off or flashing, continue to “Check the A8 Fuses and Voltages”
 - ❑ If all LEDs are now on steadily except for the +5VD LED, the A15 preregulator and A8 post regulator are working properly and the trouble is excessive loading somewhere after the motherboard connections at A8. Continue to “Remove the Assemblies”

Check the A8 Fuses and Voltages

Check the fuses along the top edge of A8. If any A8 fuse has burned out, replace it. If it burns out again when power is applied to the analyzer, A8 or A15 is faulty. Determine which assembly has failed as follows

1. Remove the A15W1 cable at A8. (See Figure 5-5.)
2. Measure the voltages at A15W1P1 (see Figure 5-6) with a voltmeter having a small probe.
3. Compare the measured voltages with those in Table 5-2.
 - ❑ If the voltages are within tolerance, replace A8.
 - ❑ If the voltages are not within tolerance, replace A15.

If the green LEDs are now on, the A15 preregulator and A8 post regulator are working properly and the trouble is excessive loading somewhere after the motherboard connections at A8. Continue to “Remove the Assemblies”

Remove the Assemblies

1. Switch off the analyzer.
2. **Install A8.** Remove the jumper from A8TP2 (AGND) to chassis ground.
3. Remove or disconnect **all** the assemblies listed below. (See Figure 5-5.)
Always switch off the analyzer before removing or disconnecting an assembly.
 - A10 digital IF
 - All phase lock
 - A12 reference
 - A13 fractional-N analog
 - A14 fractional-N digital
 - A22 Display Interface (disconnect A8P1)
4. Switch on the **analyzer** and observe the green LEDs on A8.
 - If any of the green LEDs are off or **flashing**, it is not likely that any of the assemblies listed above are causing the problem. Continue to “Briefly Disable the Shutdown Circuitry.”
 - If **all** green LEDs are now on, one or more of the above assemblies may be faulty. Continue to next step.
5. **Switch off the analyzer.**
6. Reconnect cable A8P1.
7. **Switch on the analyzer** and observe the LEDs.
 - If the LEDs are off or **blinking**, replace the A19 assembly.
 - If the LEDs are **still** on, continue to next step.
8. **Switch off the analyzer.**
9. **Switch on the analyzer** and observe the LEDs.
 - If the LEDs are off, replace the A18 display.
 - If the LEDs are **still** on, continue with the next step.
10. **Switch off the analyzer.**

11. Reinstall each assembly one at a time. Switch on the analyzer after each assembly is installed. The assembly that causes the green LEDs to go off or flash could be faulty.

Note It is possible, however, that this condition is caused by the A8 post regulator not supplying enough current. To check this, reinstall the assemblies in a different order to change the loading. If the same assembly appears to be faulty, replace that assembly. If a different assembly appears faulty, A8 is most likely faulty (unless both of the other assemblies are faulty).

Briefly Disable the Shutdown Circuitry

In this step, you shutdown and disable the protective circuitry for a short time, forcing on the supplies (including shorted supplies) with a 100% duty cycle.

Caution Damage to components or to circuit traces may occur if A8TP4 (SDIS) is shorted to chassis ground for more than a few seconds while supplies are shorted.

1. Connect A8TP4 (SDIS) to chassis ground with a jumper wire.
2. Switch on the analyzer and note the test points of any LEDs that are off.
Immediately remove the jumper wire.
3. Refer to the block diagram (Figure 5-7) at the end of this chapter and do the following:
 - Note the mnemonics of any additional signals that may connect to any A8 test point that showed a fault in the previous step.
 - Cross reference all assemblies that use the power supplies whose A8 LEDs went out when A8TP4 (SDIS) was connected to chassis ground.

- Make a list of these assemblies
- Delete the following assemblies from your list as they have already been verified earlier in this section.

A10 digital IF

All phase lock

A12 reference

A13 fractional-N analog

A14 fractional-N digital

A18 display

A22 *display interface*

4. *Switch off the analyzer.*

5. Of those assemblies that are left on the list, remove or disconnect them from the analyzer one at a time. **Table 5-4** shows the best order in which to remove them, sorting them from most to least accessible. **Table 5-4** also lists any associated assemblies that are supplied by the assembly that is being removed. After each assembly is removed or disconnected, switch on the analyzer and observe the **LEDs**.

Note

- *Always switch off the analyzer before removing or disconnecting assemblies*
- When extensive disassembly is required, refer to Chapter 14, “Assembly Replacement and Post-Repair Procedures ”
- Refer to Chapter 13, “Replaceable Parts,” to identify specific cables and assemblies that are not shown in this chapter.

-
- If all the **LEDs** light, the assembly removed (or one receiving power from it) is faulty.
 - If the **LEDs** are still not on steadily, continue to “Inspect the Motherboard.”

Table 5-4.
Recommended Order for **Removal/Disconnection** for
Troubleshooting the **A8 Board**

Assembly To Remove	Removal or Disconnection Method	Other Assemblies that Receive Power from the Removed Assembly
1. A7 CPU Board	Disconnect W87	None
2. A4 R Sampler	Unplug from A17 and Remove	None
3. A5 A Sampler	Unplug from A17 and Remove	None
4. A6 B Sampler	Unplug from A17 and Remove	None
5. A9 Source Control	Disconnect W91	None
6. A2 Front Panel Interface	Disconnect W84	A1 Front Panel Keyboard
7. A51 Test Set Interface	Disconnect W89	S4 Transfer Switch A56 LED Front Panel

Inspect the Motherboard

Inspect the A17 motherboard for solder bridges and shorted traces. In particular, inspect the traces that carry the supplies whose LEDs faulted when A8TP4 (SDIS) was grounded earlier.

Error Messages

Three error messages are associated with the power supplies functional group. They are shown here.

- **POWER SUPPLY SHUT DOWN!**

One or more supplies on the A8 post regulator assembly is shut down due to one of the following conditions: overcurrent, overvoltage, or undervoltage. Refer to “If the Red LED of the A15 is On” earlier in this procedure.

- **POWER SUPPLY HOT!**

The temperature sensors on the A8 post regulator assembly detect an overtemperature condition. The regulated power supplies on A8 have been shut down.

Check the temperature of the operating environment; it should not be greater than +55 °C (131 °F). The fan should be operating and there should be at least 15 cm (6 in) spacing behind and all around the analyzer to allow for proper ventilation.

Check the Fuses and Isolate **A8**

Check the fuses associated with each of these supplies near the A8 test points. If these fuses keep burning out, a short exists. Try isolating A8 by removing it from the motherboard connector, but keeping the cable A15W1 connected to A8J2. Connect a jumper wire from A8TP2 to chassis ground. If either the + 15 V or -12.6 V fuse blows, or the associated green LEDs do not light, replace A8.

If the + 15 V and -12.6 V green LEDs light, troubleshoot for a short between the motherboard connector pins XA8P2 pins 6 and 36 (-12.6 V) and the front panel probe power connectors. Also check between motherboard connector pins XA8P2 pins 4 and 34 (+ 15 V) and the front panel probe power connectors.

Fan Troubleshooting

Fan Speeds

The fan speed varies depending upon temperature. It is **normal** for the fan to be at high speed when the **analyzer** is just switched on, and then change to low speed when the **analyzer** is cooled.

Check the Fan Voltages

If the fan is dead, refer to the **A8** post regulator block diagram (Figure 5-7) at the end of this chapter. The fan is driven by the + 18 V and -18 V supplies coming from the **A15** preregulator. Neither of these supplies is fused.

The -18 V supply is **regulated** on **A8** in the fan drive block, and remains constant at approximately -14 volts. It connects to the **A17** motherboard via pin 32 of the **A8P1** connector.

The + 18 V supply is regulated on **A8** but changes the voltage to the fan, depending on **airflow** and temperature information. Its voltage ranges from approximately -1.0 volts to + 14.7 volts, and connects to the **A17** motherboard via pin 31 of the **A8P1** connector.

Measure the voltages of these supplies **while** using an extender board to **allow** access to the **PC** board connector, **A8P1**.

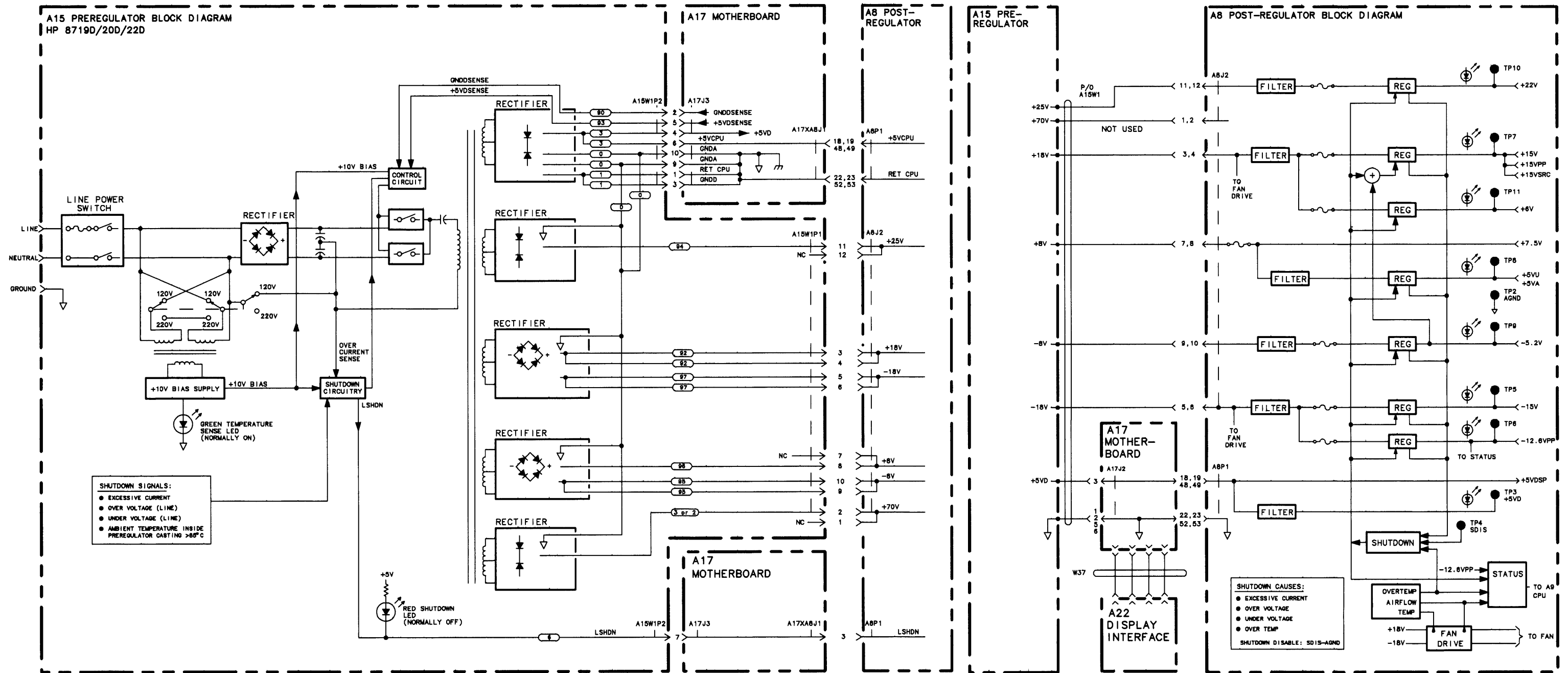
Short **A8TP3** to Ground

If there is no voltage at **A8P1** pins 31 and 32, switch **off** the **analyzer**. Remove **A8** from its motherboard connector (or extender board) but keep the cable **A15W1** connected to **A8**. (See Figure 5-5.) Connect a jumper wire between **A8TP3** and chassis ground. Switch on the analyzer.

- If **all** the green LEDs on the top edge of **A8** **light** (except +5VD), replace the fan.
- If other green LEDs on **A8** do not **light**, refer to “If the Green LEDs of the **A8** are not **All ON**” earlier in this procedure

Intermittent Problems

PRESET states that appear spontaneously (without pressing **PRESET** **PRESET: FACTORY**) typically signal a power supply or A7 CPU problem. Since the A7 CPU assembly is the easiest to substitute, do so. If the problem ceases, replace the A7. If the problem continues, replace the A15 preregulator assembly.



sb6170d

Figure 5-7
POWER SUPPLY BLOCK DIAGRAM

Digital Control Troubleshooting

Use this procedure only if you have read Chapter 4, “Start Troubleshooting Here.”

The digital control group assemblies consist of the following:

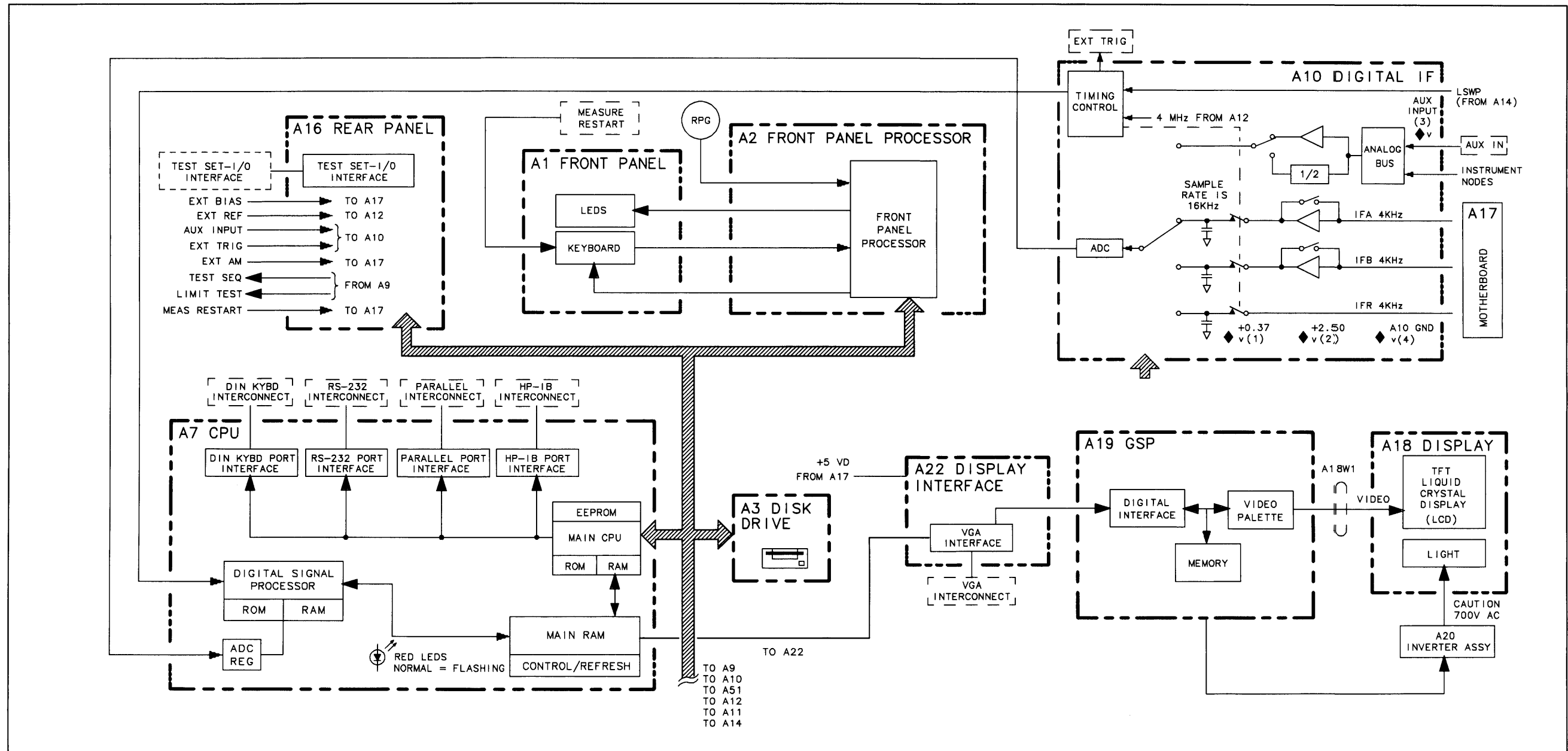
- A1 front panel keyboard
- A2 front panel interface
- A7 CPU
- A10 digital IF
- A16 rear panel
- A18 display
- A19 GSP

Begin with “CPU Troubleshooting, ” then proceed to the assembly that you suspect has a problem. If you suspect an HP-IB interface problem, refer to “HP-IB Failures,” at the end of this chapter.

Assembly Replacement Sequence

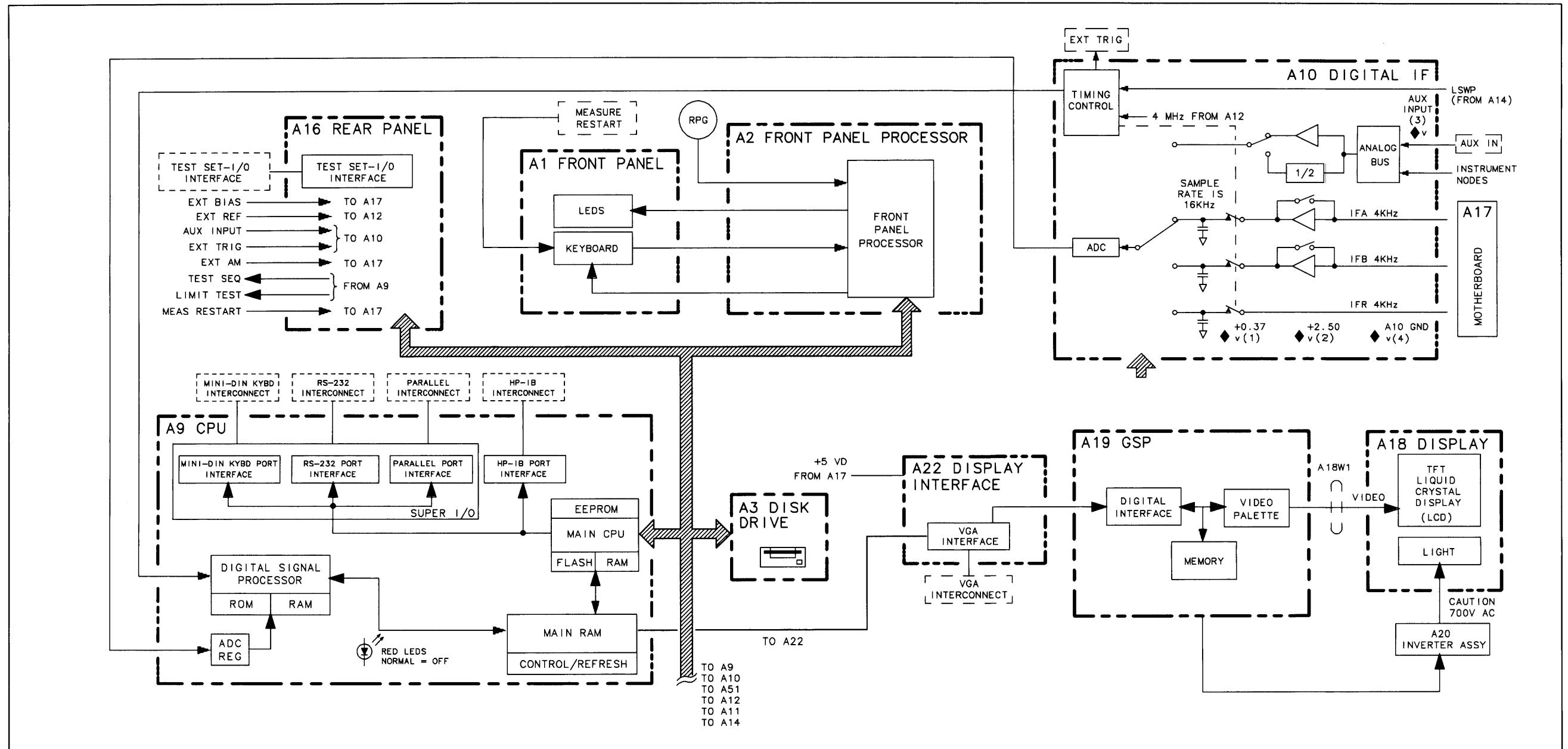
The following steps show the sequence to replace an assembly in the network analyzer.

1. **Identify the faulty group. Refer to Chapter 4, “Start Troubleshooting Here.”**
Follow up with the *appropriate troubleshooting chapter* that identifies the faulty assembly.
2. **Order a replacement assembly. Refer to Chapter 13, “Replaceable Parts.”**
3. **Replace the faulty assembly and determine what adjustments are necessary.**
Refer to Chapter 14, “Assembly Replacement and Post-Repair Procedures. ”
4. **Perform the necessary adjustments. Refer to Chapter 3, “Adjustments and Correction Constants.”**
5. **Perform the necessary performance tests. Refer to Chapter 2, “System Verification and Performance Tests. ”**



sb6125d

Figure 6-1
DIGITAL CONTROL GROUP BLOCK DIAGRAM
FOR FIRMWARE REVISIONS 6.XX AND BELOW



sb6164d

Figure 6-2
DIGITAL CONTROL GROUP BLOCK DIAGRAM
FOR FIRMWARE REVISIONS 7.XX AND ABOVE

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CPU Troubleshooting (A7)

A7 Jumper/Switch Positions

The A7 jumper/switch must be in the Normal position (NRM) for these procedures. This is the position for normal operating conditions. To move the jumper/switch to the Normal position (NRM), do the following:

1. Remove the power line cord from the analyzer.
2. Set the analyzer on its side.
3. Remove the two comer bumpers from the bottom of the instrument with a T-15 TORX screwdriver.
4. Loosen the captive screw on the bottom cover's back edge.
5. Slide the cover toward the rear of the instrument.

Caution Be sure to observe proper ESD procedures and precautions when performing the following step.

6. Move the jumper/switch to the Normal position (NRM) as shown in Figure 6-3.
7. Replace the bottom cover, comer bumpers, and power cord.

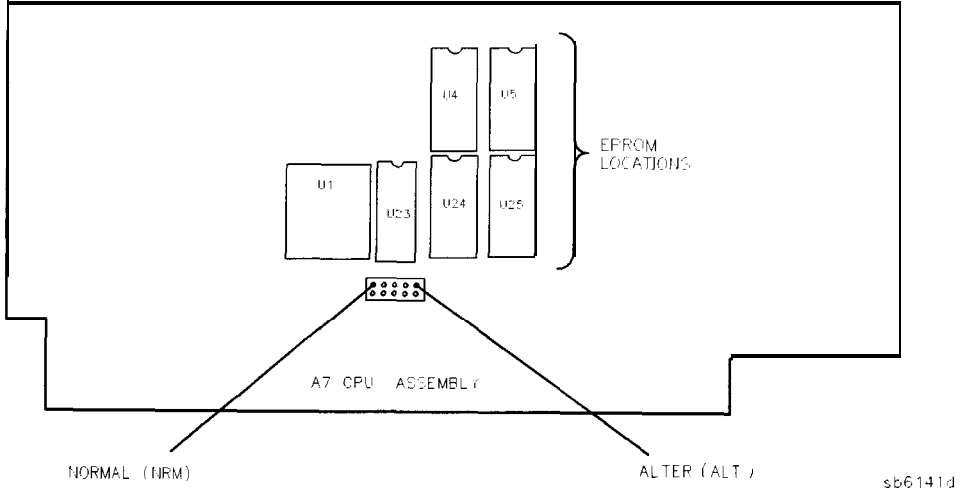
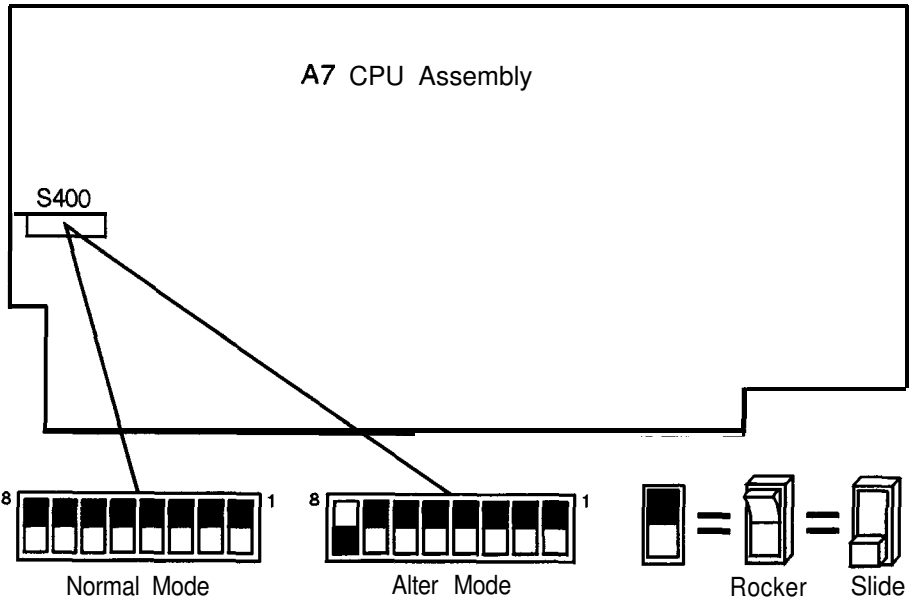


Figure 6-3. **A7** Jumper Positions (Firmware revisions **6.xx** and below.)



sb6165d

Figure 6-4. **A7** Switch Positions (Firmware revisions **7.xx** and above.)

Checking **A7** CPU Red LED Patterns

(For instruments with **firmware revisions **6.xx** and below.)**

The A7 CPU has four red LEDs that can be viewed through a small opening in the rear panel of the analyzer. (See Figure 6-5.)

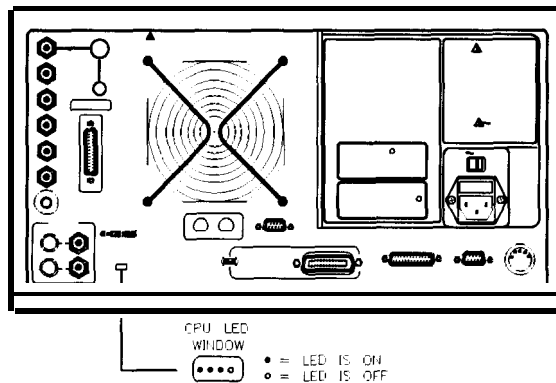
1. Cycle the power

Cycle the power on the analyzer and observe the four red LEDs. All four LEDs should be on momentarily after power up.

If the four LEDs did not turn on, replace the A7 CPU after verifying the power supply.

2. Hold in the **(PRESET)** key

Press and hold down the **(PRESET)** key while observing the four LEDs on A7. The far right LED should be off. (See Figure 6-5.)



sb6 td

Figure 6-5. CPU LED Window on Rear Panel

3. Release the **PRESET** key

Release the **PRESET** key and watch for the rapid sequence shown below. Note that the far right LED always remains on.

- • • ○ **PRESET** still held down
- • ○ • **PRESET** released – Pattern 1
- • ○ • Pattern 2
- • • • Pattern 3
- ○ ○ • Pattern 4
- • • • Pattern 5 – two left LEDs flicker

4. Observe and evaluate results

- If the above sequence is observed, and the far right LED remained on, go to “Display Troubleshooting (A19, A18).”
- If the right LED does not remain on, replace the A7 CPU assembly and repeat the three LED pattern checks.
- If the LEDs are held in any one of the patterns shown in Table 6-1, and have the corresponding error message, replace the A7 firmware ICs. (Firmware ICs are not separately replaceable. Replacement kits are listed in Chapter 13, “Replaceable Parts.”)

Table 6-1. LED Code and Pattern Versus Test Failed

LED Code Sum	Message Displayed	Faulty Component
. . • ○	ROM 1L FAIL	U24
. . . .	ROM 1M FAIL	U4
○ . . .	ROM 2L FAIL	U25
○ . . .	ROM 2M FAIL	U5

Checking **A7** CPU Red LED Patterns

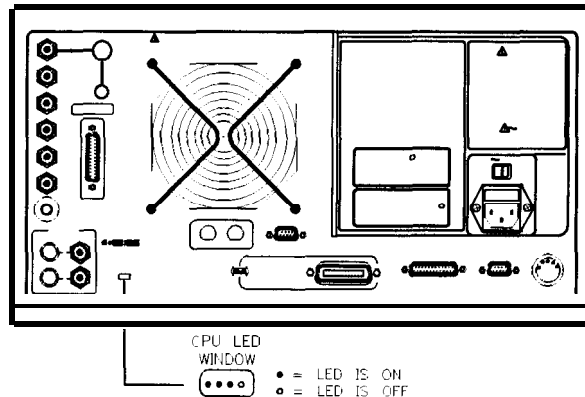
(For instruments with firmware revisions **7.xx** and above.)

The **A7** CPU has five red LEDs that can be viewed through a small opening in the rear panel of the analyzer. (See Figure 6-6.) Four LEDs are easily viewable. The fifth LED must be viewed by looking to the left at an angle.

1. Cycle the power while observing five red **LEDs**

Cycle the power on the analyzer and observe the five red LEDs. After an initial pattern, the five red LEDs on the **A7** CPU board should remain off.

- If the LEDs remained off, then proceed to the assembly that you suspect has a problem.
- If the LEDs did not remain off, switch off the power and remove the bottom cover for further troubleshooting.



5b6-1d

Figure 6-6. CPU LED Window on Rear **Panel**

2. Cycle the power while observing all eight red **LEDs**

With the analyzer positioned bottom up, cycle the power and observe the eight red LEDs while looking from the front of the instrument.

Note **If firmware did not load, a red LED on the CPU board will be flashing. Refer to “Loading Firmware” in Chapter 3.**

3. Evaluate results

- **If either of the following LED patterns remain, go to “Display Troubleshooting.”**



(front of instrument ↓)

- **If any other LED patterns remain, replace the A7 CPU after verifying the power supply.**

Display Troubleshooting (A18, A19)

This section contains the following information:

- Evaluating your Display
- A19 GSP and A18 Display Troubleshooting

Evaluating your Display

There are four criteria against which your display is measured:

- Background Lamp Intensity
- Green, Red or Blue Stuck Pixels
- Dark Stuck Pixels
- Newton's Rings

Evaluate the display as follows:

- If either the A19 GSP, A7 CPU or A20 assemblies are replaced, perform a visual inspection of the display.
- If it appears that there is a problem with the display, refer to the troubleshooting information that follows.
- If the new display appears dim or doesn't light see "Backlight Intensity Check," next.

Backlight Intensity Check

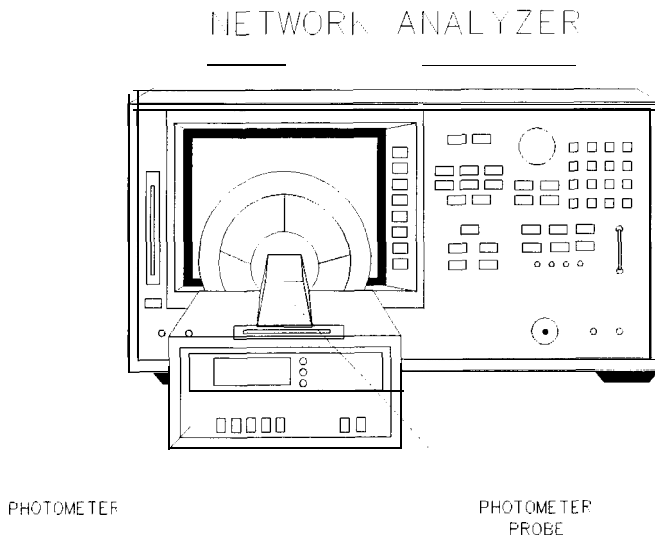
Required Equipment and **Tools**

Photometer	Tektronix J16
Probe	Tektronix J6503
Light Occluder	Tektronix 016-0305-00
Antistatic Wrist Strap	HP P/N 9300-1367
Antistatic Wrist Strap Cord	HP P/N 9300-0980
Static-control Table Mat and Earth Ground Wire	HP P/N 9300-0797

Analyzer warm-up *time*: 30 minutes. *Photometer* warmup time: 30 minutes.

Note This procedure should be performed with a photometer and only by qualified personnel.

1. Press **(Display)** **MORE ADJUST DISPLAY INTENSITY** **(100)** **(x1)**, to set the display intensity at 100%.
2. Press **(System)** **SERVICE MENU TESTS** **(62)** **(x1)** **EXECUTE TEST CONTINUE**, to set a white screen test pattern on the display.
3. Set the photometer probe to **NORMAL**. Press **(POWER)** on the photometer to switch it on and allow 30 minutes of warm-up time. Zero the photometer according to the manufacturer's instructions.
4. Center the photometer on the analyzer display as shown in Figure 6-7.



sb6142d

Figure 6-7. Backlight Intensity Check Setup

Note **The intensity levels are read with a display bezel installed.**

5. If the photometer registers less than 50 Nits, the display backlight lamp is bad. Refer to the “Replacement Procedures” chapter in the service manual for information on display lamp replacement.

Red, Green, or Blue Pixels Specifications

Red, green, or blue “stuck on” pixels may appear against a black background.

To test for these dots, press **(System)** **SERVICE MENU TESTS** **(70)** **(x1)**

EXECUTE TEST CONTINUE.

In a properly working display, the following will not occur:

- complete rows or columns of stuck pixels
- more than 5 stuck pixels (not to exceed a maximum of 2 red or blue, and 3 green)
- 2 or more consecutive stuck pixels
- stuck pixels less than 6.5 mm apart

Dark Pixels Specifications

Dark “stuck on” pixels may appear against a white background. To test for

these dots, press **(System)** **SERVICE MENU TESTS** **(66)** **(x1)** **EXECUTE TEST**

CONTINUE.

In a properly working display, the following will not occur:

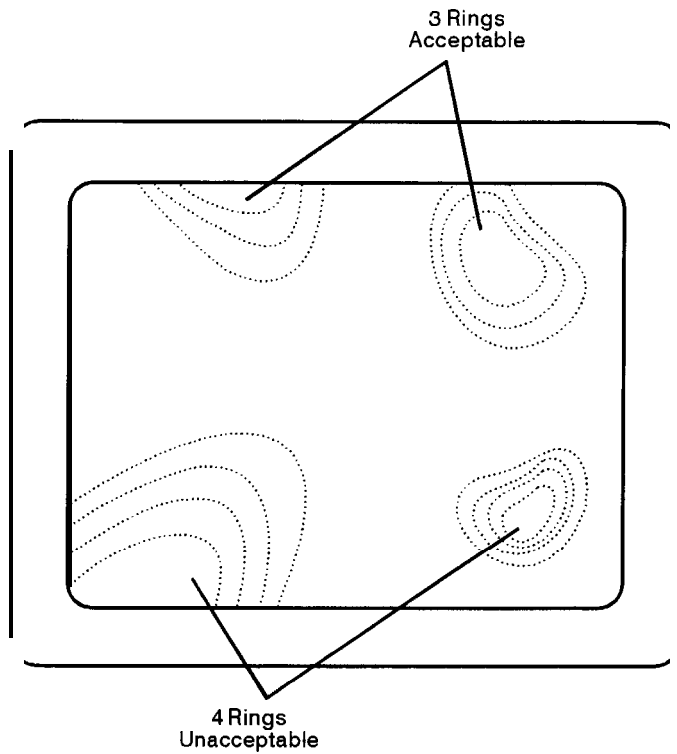
- more than 12 stuck pixels (not to exceed a maximum of 7 red, green, or blue)
- more than one occurrence of 2 consecutive stuck pixels
- stuck pixels less than 6.5 mm apart

Newton’s Rings

To check for the patterns known as Newton’s Rings, change the display to white by pressing the following keys:

(System) **SERVICE MENU TESTS** **(62)** **(x1)** **EXECUTE TEST CONTINUE**

Figure 6-8 illustrates acceptable and non-acceptable examples of Newton’s Rings.



sb6123d

Figure 6-8. Newtons Rings

A19 GSP and A18 Display Troubleshooting

Measure Display Power Supply Voltages Entering A19

Measure the power supply voltages entering the A19 assembly coming from the A18 assembly. Unplug the wire harness (W14) from the back of the GSP interface. Check pins 2 and 3 for +5.16 fO.l V. (See Figure 6-9.)

- If the voltages are incorrect, refer to Chapter 5, “Power Supply Troubleshooting.”
- If the voltages are correct entering, but incorrect leaving the GSP assembly, replace the A19 GSP assembly.

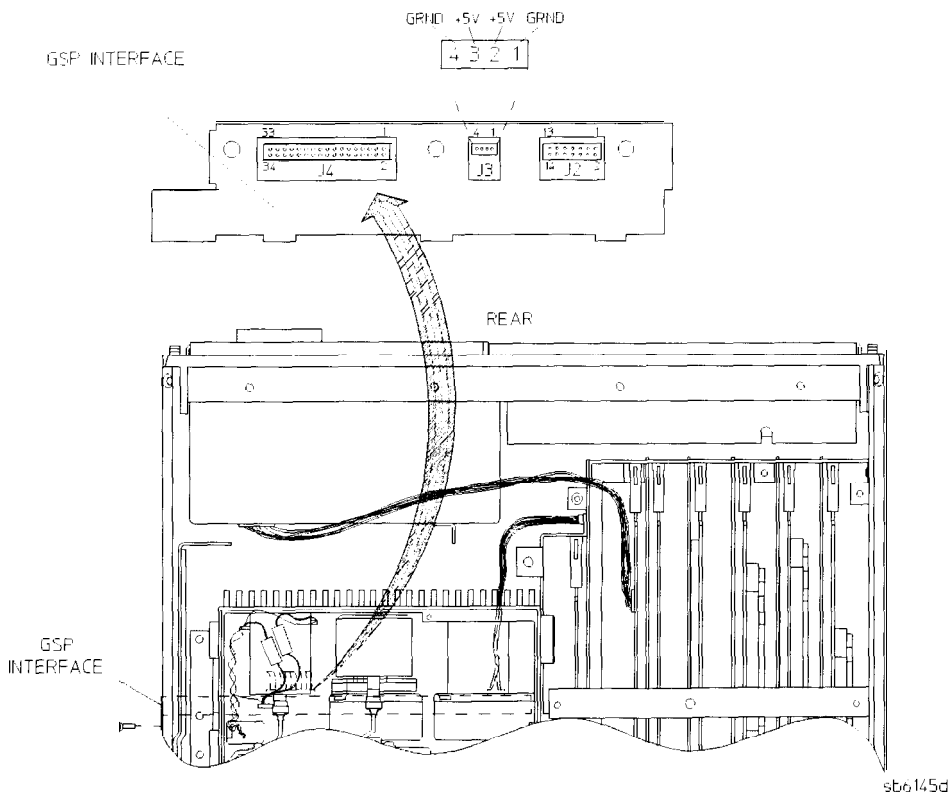


Figure 6-9. A19 GSP Voltages

Run Display Test 55

1. On the analyzer, press **PRESET** **PRESET: FACTORY** **SYSTEM** **SERVICE MENU** (softkey 8) **TESTS** (softkey 1) **DISPLAY TESTS** (softkey 7). The analyzer will display:

55 Disp/cpu com -ND-

2. Press **EXECUTE TEST** (softkey 1).
 - If the analyzer passes the test, the message TEST RESULT DISPLAYED ON LEDS IF FAILED will be displayed. Press **CONTINUE** and the analyzer will display 55 DISP/CPU COM PASS. Press **PRESET** **PRESET: FACTORY** and go to “Run Display Tests 59-76 ”.
 - If the analyzer fails the test, the display will appear blank and the front panel LEDs will stay on. Continue with the next check.

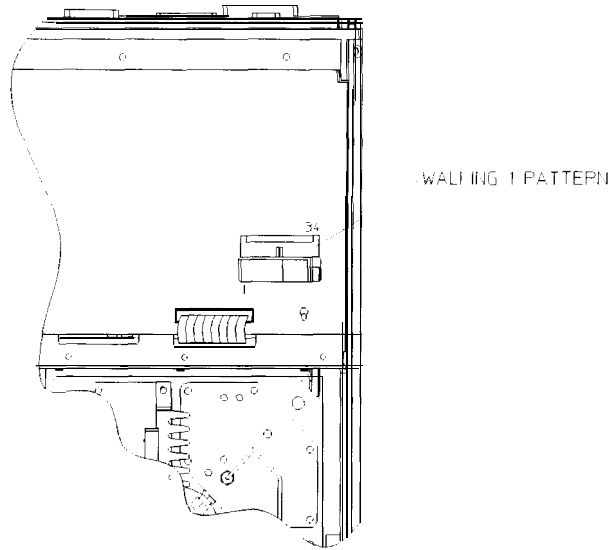
Inspect Ribbon Cable Repeat Display Test 55

Inspect the W20 (A7-A19) ribbon cable for a loose connection. Repeat “Run Display Test 55.” If the analyzer fails the test, a walking one pattern will be continuously transferred from the CPU, through the cable, to the GSF. Immediately go to the next check.

Perform Walking One Pattern

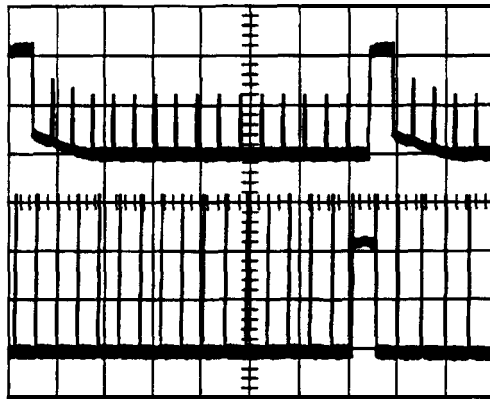
Use an oscilloscope probe to verify that a walking one pattern is transferring from the A7 CPU. The walking one pattern similar to the one shown in Figure 6-11 and is found on pins 3 through 10, and 13 through 20. (See Figure 6-10.)

- If the signal is present at the A7 connector of the ribbon cable, verify that it is present at the other end of the cable.
- If the signal is still not present, replace the cable.



sb6146d

Figure 6-10. Pin Locations on **A19**



sg601s

Figure 6-11. **A7 CPU Walking One** Pattern

Run Display Tests 59-76

1. Press **PRESET** **PRESET: FACTORY** **SYSTEM** **SERVICE MENU** (softkey 8) **TESTS** (softkey 1) **DISPLAY TESTS** (softkey 7) **59** **X1**.
2. Press **EXECUTE TEST** (softkey 1). The display and the front panel LEDs will flash once. If the analyzer passes the test, the message **PASS** is displayed.
3. Press **PRESET** **PRESET: FACTORY** and perform display tests 59 through 76 (substitute the next test number where **59** was used). Watch for the analyzer display and front panel LEDs to flash.
 - If the analyzer fails any of the tests (59 through 61), replace the A19 assembly.
 - If all of the following is true, replace the A18 display assembly.
 - CPU passes the LED test.
 - GSP passes all of the internal display tests (59 through 61).
 - Power supply checks out.

Front Panel Troubleshooting (A1/A2)

Check Front Panel **LEDs** After Preset

1. Press **PRESET** on the analyzer.
2. Observe that all front panel LEDs turn on and, within five seconds after releasing **PRESET**, all but the CH1 LED turns off.
 - If all the front panel LEDs either stay on or off, there is a control problem between A7 and A1/A2. See “Inspect Cables,” located later in this chapter.
 - If, at the end of the turn on sequence, the channel 1 LED is not on and all HP-IB status LEDs are not off, continue with “Identify the Stuck Key.”
 - If you suspect that one or more LEDs have burned out, replace the A1 keypad assembly.

Note Port 1 and port 2 LED problems may be caused by the malfunction of the LED board or the transfer switch.



















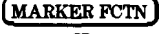



Identify the Stuck Key

Match the LED pattern with the patterns in Table 6-2. The LED pattern identifies the stuck key. Free the stuck key or replace the front panel part causing the problem.

Table 6-2. Front Panel Key Codes (1 of 2)

Decimal Number	LBD Pattern						Key	Front Panel Block
	CH1	CH2	R	L	T	S		
0							CAL	Response
1						•	3	Entry
2					•		k/m	Entry
3					•	•	DISPLAY	Response
4				•			AVG	Response
5				•		•	2	Entry
6				•	•		1	Entry
7				•	•	•	softkey 3	Softkey
8		•					softkey 5	Softkey
9		•				•	9	Entry
10		•			•		G/n	Entry
11		•			•	•	CH 1	Active Channel
12		•	•				CH 2	Active Channel
13		•	•			•	8	Entry
14		•	•	•			7	Entry
15		•	•	•		•	softkey 1	Softkey
16	•						STOP	Stimulus
17	•					•	SAVE/RECALL	Instrument State
18	•				•		SEQ	Instrument State
19	•				•	•	MENU	Stimulus
20	•		•				START	Stimulus
21	•		•			•	COPY	Instrument state
22	•		•	•			SYSTEM	Instrument State
23	•			•	•	•	softkey 6	Softkey
24	•	•					SCALE REF	Response
25	•	•				•	6	Entry

Front **Panel** Key Codes (2 of 2)

Decimal Number	LED Pattern						Key	Front Panel Block
	CH1	CH2	R	L	T	S		
26		Entry
27		Response
28		Response
29		Entry
30		Entry
31	.	.	.	•	.	.		Softkey
32		Stimulus
33	•		Entry
34		Entry
35		Stimulus
36		Softkey
37		Entry
38		Instrument State
39		Softkey
40-47	Not used							
48		Entry
49		Entry
50		Entry
51		Response
52	•		Response
53	•	•	•	•	•	•		Entry
54	•	•	•	•	•	•		Entry
55		Softkey

Inspect Cables

Remove the front panel assembly and visually inspect the ribbon cable that connects the front panel to the motherboard. Also, inspect the interconnecting ribbon cable between A1 and A2. Make sure the cables are properly connected. Replace any bad cables.

Test Using a Controller

If a controller is available, write a simple command to the analyzer. If the analyzer successfully executes the command, the problem is either the A2 front panel interface or W17 (A2 to motherboard ribbon cable) is faulty.

Run the Internal Diagnostic **Tests**

The analyzer incorporates 20 internal diagnostic tests. Most tests can be run as part of one or both major test sequences: all internal (test 0) and preset (test 1).

1. Press **SYSTEM** **SERVICE MENU TESTS** **0** **(x1)** **EXECUTE TEST** to perform all internal tests.
2. Then press **1** **(x1)** to see the results of the preset test. If either sequence fails, press the **↑** **↓** keys to find the first occurrence of a FAIL message for tests 2 through 20. See Table 6-3 for further troubleshooting information.

Table 6-3. Internal Diagnostic Test with Commentary

Failed Test	Sequence*	Probable Failed Assemblies† ; Comments and Troubleshooting Hints
0 All Int	---	--: Executes tests 3-11, 13-16, 20.
1 Preset	---	--: Executes tests 2-11, 14-16. Runs at power-on or preset.
2 ROM	P,AI	A7 : Repeats on fail; refer to 'CPU Troubleshooting (A7)' in this chapter to replace ROM or A7 .
3 CMOS RAM	P,AI	A7 : Replace A7 .
4 Main DRAM	P,AI	A7 : Repeats on fail; replace A7 .
5 DSP Wr/Rd	P,AI	A7 : Replace A7 .
6 DSP RAM	P,AI	A7 : Replace A7 .
7 DSP ALU	P,AI	A7 : Replace A7 .
8 DSP Intrpt	P,AI	A7/A10 : Remove A10 , rerun test. If fail, replace A7 . If pass , replace A1 .
9 DIF Control	P,AI	A7/A10 : Most likely A7 assembly.
LO DIP Counter	P,AI	A10/A7/A12 : Check analog bus node 17 for 1 MHz. If correct, A12 is verified ; suspect A10 .
11 DSP Control	P,AI	A10/A7 : Most likely A10 .
12 Fr Pan Wr/Rd	---	A2/A1/A7 : Run test 23. If fail, replace A2 . If pass, problem is on bus between A7 and A2 or on A7 assembly.
13 Rear Panel	AI	A16/A7 : Disconnect A16 , and check A7J2 pin 48 for 4 MHz clock signal. If OK, replace A16 . If not, replace A7 .
14 Post-reg	P,AI	A15/A8/Destination assembly: See Chapter 6, " Power Supply Troubleshooting."
15 Frac-N Cont	P,AI	A14 : Replace A14 .
16 Sweep Trig	P,AI	A14,A10 : Most likely A14 .
17 ADC Lin	---	A10 : Replace A10 .
18 ADC Ofs	---	A10 : Replace A10 .
19 ABUS Test	---	A10 : Replace A10 .
20 FN count	AI	A14/A13/A10 : Most likely A14 or A13 , as previous tests check A10 . See Chapter 7, "Source Troubleshooting."

* P - part of PRESET sequence; AI -part of ALL JINTERNAL sequence.

† in decreasing order of **probability**.

If the Fault is Intermittent

Repeat Test Function

If the failure is intermittent, do the following:

1. Press **(SYSTEM) SERVICE MENU TEST OPTIONS REPEAT ON** to switch on the repeat function.
2. Then press **RETURN TESTS**.
3. Select the test desired and press **EXECUTE TEST**.
4. Press **(PRESET)** to stop the function. The test repeat function is explained in Chapter 10, “Service Key Menus and Error Messages.”

HP-IB Failures

If you have performed “Step 3. Troubleshooting HP-IB Systems” in Chapter 4, “Start Troubleshooting Here,” and you suspect there is an HP-IB problem in the analyzer, perform the following test. It checks the internal communication path between the A7 CPU and the A16 rear panel. It does not check the HP-IB paths external to the instrument.

Press **(SYSTEM) SERVICE MENU TESTS (13) (X1) EXECUTE TEST**.

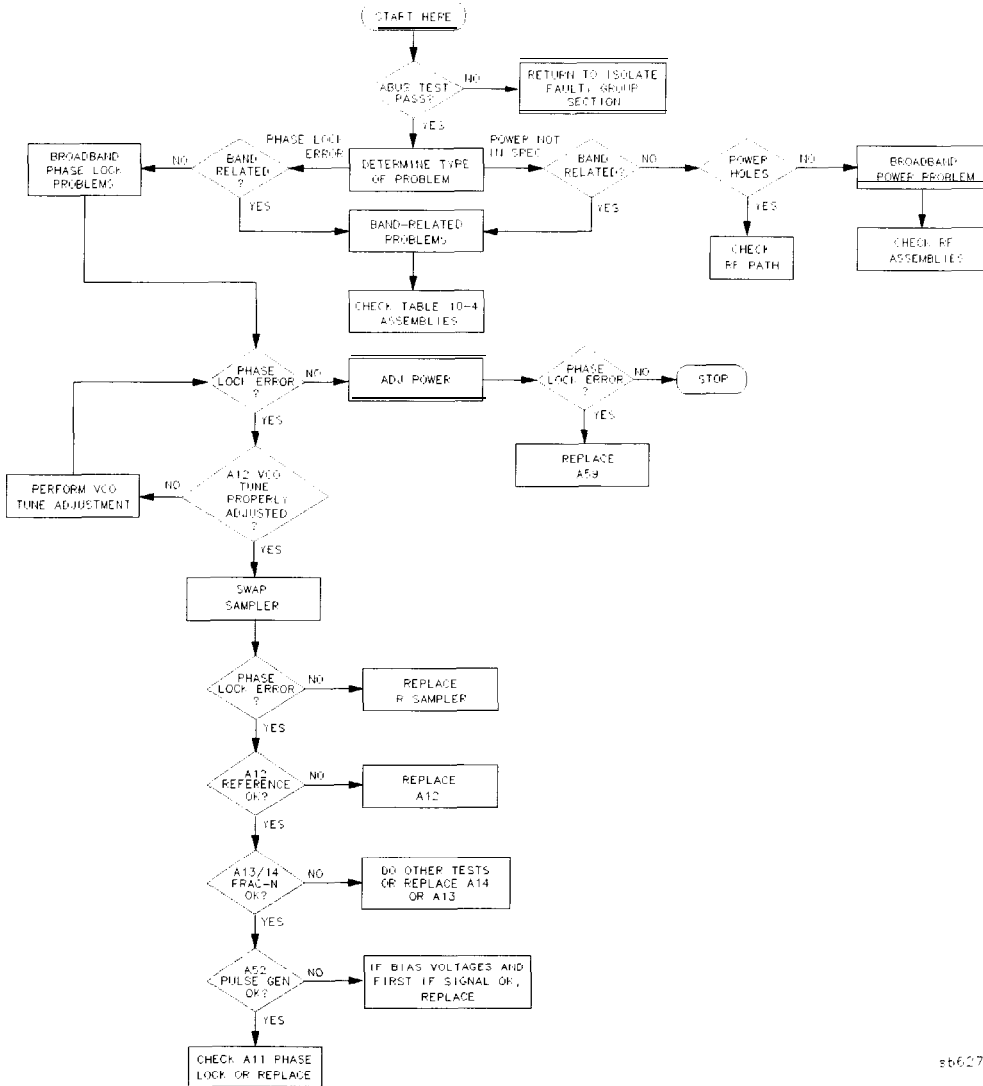
- If the analyzer fails the test, the problem is likely to be the A16 rear panel.
- If the analyzer passes the test, it indicates that the A7 CPU can communicate with the A16 rear panel with a 50% confidence level. There is a good chance that the A16 rear panel is working. This is because internal bus lines have been tested between the A7 CPU and A16, and HP-IB signal paths are not checked external to the analyzer.

Source Troubleshooting

Use this procedure only if you have read Chapter 4, “Start Troubleshooting Here.” This chapter is divided into two troubleshooting procedures for the following problems:

- **Incorrect power levels:** Perform the “Broadband Power Problems” troubleshooting checks.
- **Phase lock error:** Perform the “Phase Lock Error” troubleshooting checks.

Source Troubleshooting Flowchart



sb627d

Assembly Replacement Sequence

The following steps show the sequence to replace an assembly in the network analyzer.

1. Identify the faulty group. Refer to Chapter 4, “Start Troubleshooting Here.” Follow up with the appropriate troubleshooting chapter that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, “Replaceable Parts.”
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, “Assembly Replacement and Post-Repair Procedures.”
4. Perform the necessary adjustments. Refer to Chapter 3, “Adjustments and Correction Constants, ”
5. Perform the necessary performance tests. Refer to Chapter 2, “System Verification and Performance Tests. ”

Before You Start Troubleshooting

1. Make sure all of the assemblies are firmly seated.
2. Make sure that input R has a signal of at least -35 dBm (about 0.01 Vp-p into 50 ohms) at all times to maintain phase lock. To make this measurement, perform the following steps:
 - a. Perform steps 1 and 2 of the “Source Pretune Correction Constants” procedure located in Chapter 3. Make note of the DAC number that is displayed and then abort the procedure.
 - b. Press **(SYSTEM) SERVICE MENU SERVICE MODES SRC ADJUST MENU DAC NUM HIGH BAND**.
 - c. Enter the DAC number determined from step a and press **(x1)**.
 - d. Disconnect the front panel R CHANNEL jumper.
 - e. Zero and calibrate a power meter. Measure the power at R CHANNEL OUT.

Start Here

The use of this section is based on several assumptions:

- The analog bus has passed test #19. (If not, press **(System)** **SERVICE MENU** **TESTS** **(19)** **(x1)** **EXECUTE** **TEST**.
 - If the analyzer falls the test, return to “Step 4. Faulty Group Isolation” section of the “Start Troubleshooting Here” chapter in this manual.
 - If the test passes, continue with this procedure.
- If you observed a phase lock error message, in “Step 4. Faulty Group Isolation” section of the “Start Troubleshooting Here” chapter in this manual
- If incorrect power levels were observed in “Step 4. Faulty Group Isolation” section of the “Start Troubleshooting Here” chapter in this manual.
- A performance test or adjustment failed.

Phase Lock Error Message Displayed

1. Press the following keys to view the 0.25V/GHz signal to the YIG oscillator drives.

(Preset) **PRESET: FACTORY** **(Preset)**

(System) **SERVICE MENU** **ANALOG BUS**

(Meas) **ANALOG IN AUX INPUT** **COUNTER: ANALOG BUS** **(9)** **(x1)**

(Scale Ref) **(2)** **(x1)**

Notice that for each band, the waveform should start and stop exactly as shown in Figure 7-1 and Figure 7-2, with only one ramp in each band. A problem in one band should not affect the appearance of the waveform in other bands.

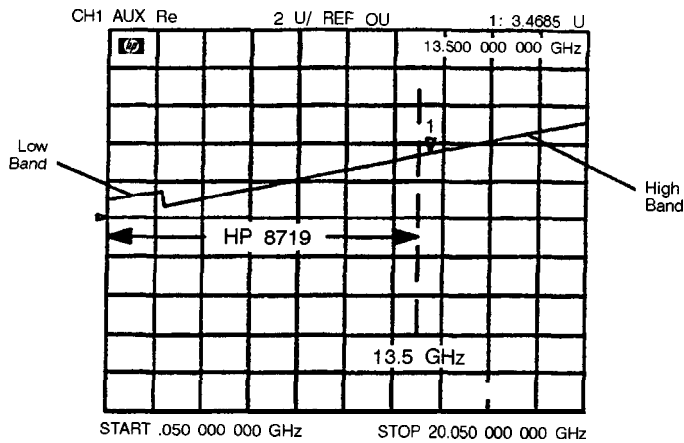


Figure 7-1. **HP 8719D/20D 0.25V/GHz** Waveform at **Abus** Node 9

sb6154d

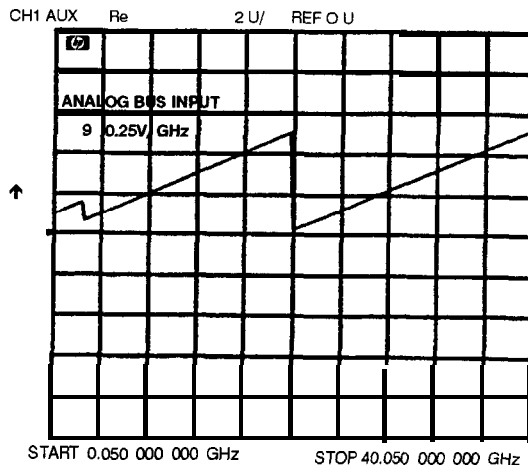


Figure 7-2. **HP 8722D 0.25V/GHz** Waveform at **Abus** Node 9

sb6153d

- If the waveform appears normal in one but not all frequency bands, go to “Band-Related Problems” located later in this chapter.
- If the waveform appears abnormal in all frequency bands, refer to “Broadband phase Lock Problems,” below.

Power Not Within Specifications

Perform these power adjustments:

1. output power adjustments
 2. blanking adjustments
- If power holes exist, use the block diagram (located in “Start Troubleshooting Here”) and the location diagrams (in “Replaceable Parts”) to check the cables and connections in the RF path.
 - If power levels are incorrect (are not ± 3 dBm of setting) in only one or two bands, go to “Band-Related Problems” located later in this chapter.
 - If power levels are incorrect in all bands, go to “Broadband Power Problems.”

Broadband Phase Lock Problems

Phase lock problems can be caused by incorrect pretune correction constants.

1. Perform the source pretune correction constant procedure (service test 43, see Chapter 3, “Adjustments and Correction Constants”) to fix this potential problem.
2. Then press (**PRESET**) **PRESET: FACTORY** to see if the phase lock problem persists.
3. If the phase lock problem persists, continue. It could be caused by a fault in one of these source assemblies:

All phase lock

A14 fractional-N digital

A58 M/A/D/S

A54 YIG 2 (HP 8722D Only)

S1 PIN switch
(HP 8722D Only)

A9 source control board

A12 reference

A51 test set interface

A64 R sampler

A55 YIG 1

A74 switch splitter
Option 400 only)

S5 R channel remote input switch
(Options 085,089 only)

A13 fractional-N analog

A52 pulse generator

S2, S3 PIN switches

A59 source interface board

A72 R channel buffer amp

A75 R channel attenuator

Swap Samplers to Check **A64 R** Sampler

1. At A66J3 (the B sampler, see location diagram or the “Replacement Procedures” chapter of this manual), replace the IF OUT cable with the IF OUT cable removed from A64J3 (the R sampler).
2. Press **(MEAS) Ref1: REV S22** (B/R) (Ignore the trace) .
3. If the phase lock problem persists, the R sampler was not the problem. Continue with “Check Open Loop Power.”
4. If the phase lock error message disappears, either the control voltage, bias voltage, RF signal or the R sampler itself is faulty.
5. Check for about + 0.02 V on the green sampler control wire: if it is bad, replace A5 1.
6. Check the + 15 V and -15 V bias voltages (see “A51 Interface Power Supplies”). If they are bad, replace A51.

Note

For the HP 8722D, if 2.4 mm flexible cables and 2.4 mm power sensors are not available, troubleshooting is possible using 3.5 mm equipment and 3.5 mm to 2.4 mm adapters, such as HP 11901D 2.4 mm (f) to 3.5 mm (m) and HP 11901B 2.4 mm to 3.5 mm (f).

7. If the control and bias voltages are good, use a power meter and the flexible cable from the tool kit to troubleshoot the RF signal path.
8. Press **(SYSTEM) SERVICE MENU SERVICE MODES SRC ADJUST MENU DAC NUM HIGH BAND (4000) (x1)** to enter the service mode.
9. Measure the M/A/D/S output power at the R CHANNEL OUT port on the front panel.
 - For the HP 8719D/20D, the power should be at least -18 dBm (-13 dBm, Option 007).
 - For the HP 8722D, the power should be at least -27 dBm (-22 dBm, Option 007).
10. If the power level is correct, replace the R sampler. If the power level is not correct, replace A58.

Check Open Loop Power (HP **8719D/20D** Only)

1. Use a power meter to measure power at the R CHANNEL OUT port on the front panel.
2. Press **(SYSTEM) SERVICE MENU SERVICE MODES SRC ADJUST MENU DAC NUM LOW BAND (4000) (x1)**.
The power should be at least -23 dBm (-18 dBm, Option 007).
3. Press **DAC NUM HIGH BAND (4000) (x1)**.
The power should be at least -18 dBm (-13 dBm, Option 007).
4. You may have to change the DAC number slightly to achieve a good power reading. If power is correct, proceed with “Check A12 Reference.”
5. If the high band power level is lower than -18 dBm, check A55 YIG 1 power at S2J3.
6. Connect a power meter to S2J3 and measure the DAC num high band values from about 3200 to 4095.
 - If the power at S2J3 is greater than 0 dBm, replace the A58 M/A/D/S.
 - If the power is less than 0 dBm, check YIG 1 output power at the A53 end of W6.
7. Power greater than 10 dBm indicates proper power out of YIG at about 4.5 GHz. If the analyzer is not phase locking at this frequency in normal operation, the problem is with the RF cabling, S2 or S3.
8. If no power is present, refer to “A51 Test Set Interface Power Supplies” at the end of this section, to check the bias voltages to YIG1. If the voltages are correct, replace the YIG.

Check Open Loop Power (HP **8722D** Only)

1. Use a power meter to measure power at the R CHANNEL OUT port on the front panel.
2. Press **(SYSTEM) SERVICE MENU SERVICE MODES SRC ADJUST MENU DAC NUM LOW BAND (4000) (x1)**.
The power should be at least -32 dBm (-27 dBm, Option 007).

3. Press **DAC NUM MID BAND** **(4000)** **(x1)**.
The power should be at least -32 dBm (-27 dBm, Option 007).
4. Press **DAC NUM HIGH BAND** **(4000)** **(x1)**.
The power should be at least -27 dBm (-22 dBm, Option 007).
5. You may have to change the DAC number slightly to achieve a good power reading. If power is correct, proceed with “Check A12 Reference.”
6. If the power level is not correct, connect a power meter to the output of SI leading to the A58 M/A/D/S, and check the power of the YIG oscillator.
 - High band power should be greater than + 3 dBm for DAC numbers from 2400 to 4095.
 - Mid band power should be greater than + 5 dBm for DAC numbers from 3300 to 4095.
 - Low band power should be greater than -2 dBm for DAC numbers from 3700 to 4095.
7. Low power in high or mid band indicates a problem with the associated YIG or switches. Trace back along the signal path to find where the power is lost. Activate the signal path under test by selecting the proper **DAC NUM XXX BAND**.
8. If no power is present, refer to “A51 Test Set Interface Power Supplies” at the end of this section, to check the bias voltages to the YIGs. If the voltages are correct, replace the YIG.

Check **A12** Reference

1. Press **(PRESET)** **PRESET: FACTORY** **(SYSTEM)** **SERVICE MENU** **ANALOG BUS ON** **(MEAS)** **ANALOG IN Aux Input** **ANALOG BUS** **(14)** **(x1)** **COUNTER: ON** to check the 100 kHz signal from A12.
2. The analyzer should display **ANALOG BUS INPUT 14 100kHz cnt : .100 MHz**
3. Press **(17)** **(x1)** to check the 1 MHz signal.
The analyzer should display **17 PL Ref cnt : 1.000 MHz**
4. If either counter reading is incorrect, the A12 reference assembly is probably faulty and should be replaced. However, it is also possible that there is a faulty counter, A14 fractional-N digital, or A10 digital IF assembly.

Check **A14** Fractional-N Checks With **ABUS**

1. Press **PRESET** **PRESET: FACTORY** **MENU** **SWEEP TYPE MENU LOG FREQ** **(SYSTEM)** **SERVICE MENU ANALOG BUS ON** **(MEAS)** **ANALOG IN Aux Input** **ANALOG BUS** **(21)** **(x1)** and compare the fractional-N tuning voltage to Figure 7-3.

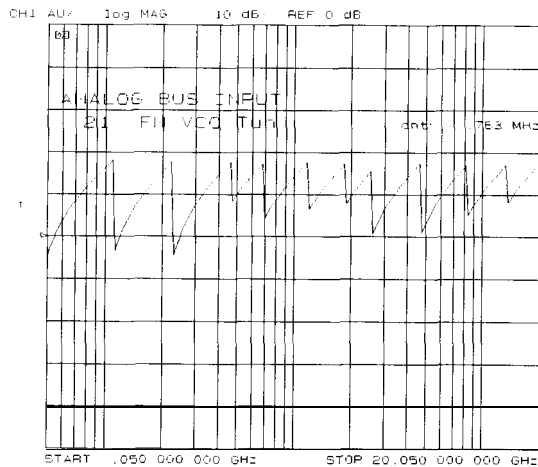


Figure 7-3. Fractional-N Tuning Voltage Waveform at **Abus** Node 21

2. Press **COUNTER: FRAC N** **(MENU)** **CW FREQ** and set the instrument to the frequencies of column one in Table 7-1.

Table 7-1. VCO Range Check Frequencies

Front Panel	Displayed Counter Value
50 MHz	119.988 to 120.012MHz
109.999 MHz	239.975 to 240.024 MHz

- If the voltage waveform resembles Figure 7-3 but the counter values do not match Table 7-1, A14 or the pulse generator may be at fault.
- If the voltage waveform and the counter values are bad, continue with “A14 VCO Exercise.”

- If the instrument passes both checks, the probability is greater than 90% that A13 and A14 are functional: go to “Check Pulse Generator” or continue with “A14 VCO Range Check with Oscilloscope” to confirm.

A13 Fractional-N Analog and **A14** Fractional-N Digital Check with Spectrum

Analyzer

1. Press **PRESET** **PRESET: FACTORY** **SYSTEM** **SERVICE MENU** **SERVICE MODES** **FRACN TUNE ON** .

2. Set the parameters on the spectrum analyzer:

start frequency = 50 MHz
stop frequency = 250 MHz
bandwidth = 300 kHz

3. Remove the instrument bottom cover and disconnect the A52J1 cable from the A52 Pulse Generator.
4. Connect the spectrum analyzer to the output of A14 via the A52J1 cable.
5. Slowly turn the network analyzer front panel knob to tune the signal across the entire frequency range.

You should see a signal that is about 0 dBm at 120 MHz and below. You should see the signal drop approximately 2.5 dB above 120 MHz.

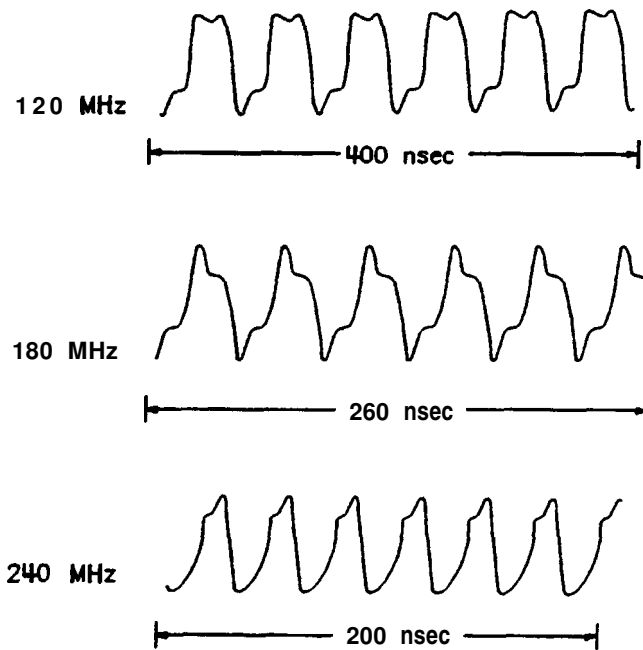
6. Look for sidebands on the signal.

The signal should appear very clean without any sidebands present, however, you will observe source harmonics

- If any sidebands do appear on the signal, there could be a faulty A13 fractional-N analog assembly.
- If you see pieces of the signal dropping out (possibly in steps) when you are tuning the signal across the frequency range, there could be a faulty A14 fractional-N digital assembly.
- If a clean signal appears across the entire frequency range, you can assume that the A13 (fractional-N analog) and the A14 (fractional-N digital) assemblies are working correctly.

A14 VCO Range Check with Oscilloscope

1. Connect an oscilloscope to A14TP1 (labeled VCO/2).
2. Press **PRESET** **PRESET: FACTORY** **SYSTEM** **SERVICE MENU** **SERVICE MODES** **FRACN** **TUNE ON**.
3. Vary the fractional-N VCO frequency with the front panel knob.
4. If the waveforms do not resemble Figure 7-4 at the frequencies indicated, replace A14. (The amplitude of the waveforms will vary from 3 V to 10 V P-P.)



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Figure 7-4. **VCO/2 Waveforms** at **A14TP1**

A14 VCO Exercise

The tuning voltage range of the VCO is approximately + 1 to + 14 volts. This procedure substitutes power supplies for the normal voltages from A13 to check the frequency range of the A14 VCO.

1. Remove the A13 assembly.
2. Put the A14 assembly on an extender board. It is not necessary to connect the cables while the A14 is on the extender board.
3. Press **(SYSTEM) SERVICE MENU ANALOG BUS ON (MEAS) ANALOG IN Aux Input FRAC-N** to set the internal counter to the frac-N node.
4. In turn, jumper each of the three supply voltages to A14TP14 and observe the frequency as shown in Table 7-2.

Table 7-2. VCO Exercise Matrix

supply Test Point	Voltage Mnemonic	A14 Test Point	Counter Frequency
A8TP7	+ 15 V	A14TP14	≈ 240 MHz
A8TP8	+5VU	A14TP14	≈ 155 MHz
A8TP2	AGND	A14TP14	≈ 105 MHz

5. If the frequency changes are not correct, replace A14.
6. If the frequency changes are correct, continue with “A14 Divide-by-N Circuit Check.”

A14 Divide-by-N Circuit Check

Note The A13 assembly should still be out of the instrument and the A14 assembly on an extender board.

1. Jumper A14TP14 to the +5VU supply.
2. Connect an oscilloscope to A14J3 (labeled VCO/N OUT).
3. Press **(SYSTEM) SERVICE MENU SERVICE MODES FRACN TUNE ON** .

4. Vary the fractional-N frequency from 120 MHz to 242 MHz.
 - If the period of the signal does not vary from 7.5 μ sec to 15.5 μ sec, replace A14.
 - If the period does vary as prescribed, remove the jumper and reinsert A14.

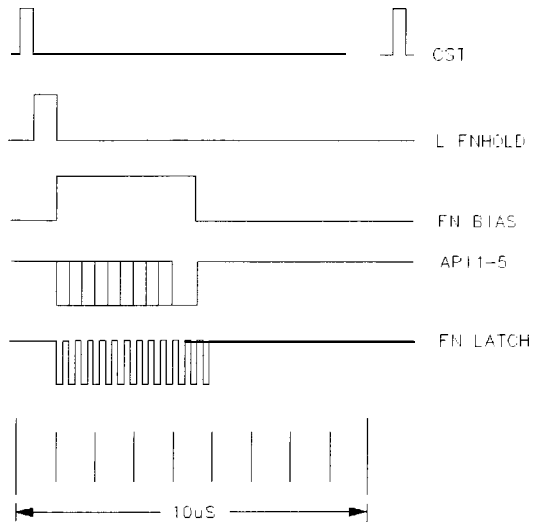
A14-to-A13 Digital Control Signals Check

1. Place A13 on the extender board and reconnect all of the flexible cables (the one to A14J1 is optional).
2. The A14 assembly generates a TTL cycle start (CST) signal every 10 microseconds when the VCO is oscillating.
3. Connect an oscilloscope to A14TP3 (CST). (Suggested vertical scale: 2.0V/div).
4. Press **(MENU) TRIGGER MENU HOLD** to stop the sweep. This will make triggering on these waveforms easier.
5. If there is no signal, replace A14.
6. Use the CST signal as an external trigger for the oscilloscope and observe the signals listed in Figure 7-5. Since these TTL signals are generated by A14 to control A13, check them at A13 first.

The signals should look similar to the waveforms in Figure 7-5.

Table 7-3. A14-to-A13 Digital Control Signal Locations

Mnemonic	A13 Location	A14 Location
CST	none	TP3
L FNHOLD	P2-2	P2-2
FNBIAS	P2-5	P2-5
API1	P2-32	P2-32
API2	P2-3	P2-3
API3	P2-34	P2-34
API4	P2-4	P2-4
API5	P2-35	P2-35
NLATCH	P1-28	P1-58



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Figure 7-5. A14 TTL Signals at A14TP3

- If these signals are bad, replace A14.
- If they are good, replace A13.

A52 Pulse Generator Check With Oscilloscope

1. Monitor the 1st IF signal at the output of A65 A sampler: disconnect the SMB cable from A65 and connect an oscilloscope to the sampler IF output. Connect a frequency counter to port 1. Then perform these steps:

- a. Press **PRESET** **PRESET: FACTORY** **SYSTEM** **SERVICE MENU**
SERVICE MODES FRACN TUNE ON **180** **M/U** to set the fractional-N VCO to 180 MHz.
- b. Press **SRC ADJUST MENU DAC NUM LOW BAND** and rotate the front panel knob to change the DAC number to about 4013. Readjust the DAC number as required to measure an output frequency of about 0.91 GHz.

Note The frequency counter may have to be removed from port 1 to provide enough of a reflection to see on the scope.

2. Now the oscilloscope should display the IF signal as a sine wave of about 10 MHz. The actual frequency can be expressed as this equation:

$$\text{Oscilloscope frequency} = (\text{counter frequency}) - (180 \text{ MHz}) \times (\text{harmonic})$$

3. Repeat steps 1b and 2 using the information in the second through fourth rows of Table 7-4. Substitute **DAC NUM LOW BAND** with the appropriate band.

Table 7-4. First IF Settings

DAC Number Band	Approximate DAC Number Displayed	Approximate Source Frequency On Counter	Harmonic	Oscilloscope Frequency
Low	4013	0.910 GHz	5	10 MHz
Mid (HP 8722D Only)	3541	3.610 GHz	26	10 MHz
High	4004	4.690 GHz	26	10 MHz
High (HP 8722D Only)	2529	20.17 GHz	112	10 MHz

- If the IF signals are correct, replace the A11.

- If the IF signals are incorrect, check the pulse generator bias voltages (see “A51 Interface Power Supplies”). If the voltages are correct, replace the A52 pulse generator.

A52 Pulse Generator Check With Spectrum Analyzer

1. Connect the spectrum analyzer to the network analyzer A65, A sampler (J3) IF output.

2. Set the parameters on the spectrum analyzer:

center frequency = 10 MHz

span = 20 MHz

marker = 10 MHz

3. Press the following keys on the network analyzer to set the fractional-N

vco to 180 MHz: **PRESET** **PRESET: FACTORY** **SYSTEM** **SERVICE MENU**

SERVICE MODES **FRACN TUNE ON** **180** **M/u** **SRC ADJUST MENU**

DAC NUM **LOW BAND** **4000** **x1**.

4. Slowly turn the network analyzer front panel knob until the spectrum analyzer measures an output frequency of 10 MHz.

If the 10 MHz signal appeared, disregard the rest of this step and continue with the next step.

If the 10 MHz signal didn't appear, connect the R sampler (J3) to the spectrum analyzer input and change the center frequency to 10 MHz.

- If the 10 MHz signal appears on the R sampler but not on the A sampler, the A sampler is faulty.

- If the 10 MHz signal didn't appear at either the A sampler or the R sampler, connect the network analyzer's PORT 1 to the spectrum analyzer input.

Press the following keys on the network analyzer: **PRESET**

PRESET: FACTORY **SYSTEM** **SERVICE MENU** **SERVICE MODES**

FRACN TUNE ON **180** **M/u** **SRC ADJUST MENU** **DAC NUM** **LOW BAND** **4000**

x1.

Set the parameters on the spectrum analyzer:

center frequency = 0.9 GHz

span = 200 MHz

You should see a signal near the center frequency.

If a signal is present, the A52 pulse generator is probably faulty.

5. Connect the network analyzer's PORT 1 to the spectrum analyzer input,

6. Set the parameters on the spectrum analyzer:

center frequency = 0.9 GHz

span = 200 MHz

You should see a signal at approximately 910 MHz.

7. Reconnect the spectrum analyzer to the A sampler (53).

8. Set the parameters on the spectrum analyzer:

start frequency = 0 Hz

stop frequency = 200 MHz

marker = 10 MHz

9. Press **DAC NUM HIGH BAND** **(4000)** **(x1)** on the network analyzer, and slowly turn the front panel knob to get a 10 MHz signal displayed on the spectrum analyzer.

10. Reconnect the network analyzer's PORT 1 to spectrum analyzer input.

11. Set the parameters on the spectrum analyzer:

center frequency = 4.69 GHz

span = 200 MHz

You should see a signal at approximately 4.69 GHz.

- If the signals appeared for both the low band and high band, you can assume that all the assemblies are working correctly, with the exception of the All phase-lock assembly.
- If the high band signal didn't appear, there could be a faulty A68 Attenuator, S1 switch (HP 8722D Only), S2 switch, S3 switch, or associated cabling.
- If the low band signal didn't appear, there could be a faulty A57 fixed oscillator, A53 mixer/amp, S1 switch (HP 8722D Only), S2 switch, S3 switch or associated cabling.
- If neither low band or high band signal appears, there could be a faulty A54 YIG oscillator (HP 8722D Only), A55 YIG oscillator, All phase-lock, A58 M/A/D/S, or associated cabling.

Band-Related Problems

Table 7-5 lists assemblies potentially responsible for band-related problems.

Table 7-5.
Assemblies Potentially Responsible for Band-Related Problems

Low Band	Mid Band (HP 8722D Only)	High Band
A57	A55	A59
A53	S2	S2
S2	S3	S3
S3	A59	S1 (HP 8722D Only)
A59		A54 (HP 8722D Only)

Note Problems in RF components, crimped RF cables, and improper connections which generally cause power holes in an RF signal may cause symptoms that indicate a band-related problem.

Start by measuring power from S2 (S1, HP 8722D Only). If the power here is good, then all of the components are verified. Continue troubleshooting with “Broadband Power Problems” to check other components. Also keep the following points in mind.

- Remove the instrument covers.
- Cables having improper connections can be the problem in all cases.
- Use the flexible RF cable from the tool kit to measure power at otherwise inaccessible connections.
- Before replacing suspect assemblies, refer to “A15 Interface Power Supplies” to check bias voltages.

Low Band Problems:

1. Calibrate and zero a power meter and connect it to S2J3.

2. Press **(SYSTEM) SERVICE MENU SERVICE MODES SRC ADJUST MENU**
DAC NUM LOW BAND (4000) (x1) to measure power at S2J3.

Note While adjusting the DAC numbers in the following step, monitor port 1 with a spectrum analyzer to be sure that the frequency remains between 50 MHz and 1.1 GHz. DAC numbers that set the analyzer below 50 MHz should not be used.

- If greater than -5 dBm for DAC numbers from 50 MHz (DAC # \approx 3650) to about 1.1 GHz (DAC # = 4095), troubleshoot the cabling from S2J3 to the R sampler A64J2 (refer to the overall block diagram).
 - If less than -5 dBm at S2J3, the problem is in the A53 mixer/amp, A57 fixed oscillator, S2, or S3.
3. Measure power at the A53 end of cable W6.
 - If power is greater than + 8 dBm, S3 is good.
 - If power is not good, replace S3.
 4. Measure power on the S2 end of W36.
 - If the power is greater than -5 dBm, replace S2.
 - If the power is less than -5 dBm, the problem is the A53 mixer amp or the A57 fixed oscillator. Replace the A53 first and if the problem persists, replace the A57.

Mid Band Problems: (HP **8722D** Only)

1. Press **(SYSTEM) SERVICE MENU SERVICE MODES SRC ADJUST MENU**
DAC NUM MID BAND (4000) (x1). (SRC tune in the mid band is capable of tuning the instrument from about 2.4 to 5 GHz). Loss of lock in mid band only may likely be due to a bad cable or connection.
2. Referring to the overall block diagram, the following components may be at fault:
 - S2
 - S3
 - A58 M/A/D/S
 - A55 YIG 1

3. Since the analyzer phase locked in lowband, all of the phase lock circuitry is working Look for low power as a cause of phase lock errors.
4. Check power at S2J3.
 - If the power at S2J3 is less than 0 dBm, check the insertion loss of S3, S4 and the associated cabling.
 - If the power at S2J3 is greater than 0 dBm, the problem is probably above 5 GHz.

Proceed with the next steps.
5. Check all RF cabling and connections.
 - If any of the cables or connectors are bad, have them repaired or replaced.
 - If the cables and connectors are good, replace the A55 YIG 1. If mid band problems still persist, then replace the A58 M/A/D/S.

High Band Problems: (HP **8719D/20D** Only)

1. Press **(SYSTEM) SERVICE MENU SERVICE MODES SRC ADJUST MENU DAC NUM HIGH BAND (4000) (x1)**. (SRC tune in the high band is capable of tuning the instrument from about 2.4 to 5 GHz). Loss of lock in high band only may likely be due to a bad cable or connection.
2. Referring to the overall block diagram, the following components may be at fault:
 - S2
 - S3
 - A58 M/A/D/S
 - A55 YIG 1
3. Since the analyzer phase locked in lowband, all of the phase lock circuitry is working Look for low power as a cause of phase lock errors.
4. Check power at S2J3.
 - If the power at S2J3 is less than 0 dBm, check the insertion loss of S3, S4 and the associated cabling.
 - If the power at S2J3 is greater than 0 dBm, the problem is probably above 5 GHz. Proceed with the next steps.

5. Check all RF cabling and connections.
 - If any of the cables or connectors are bad, have them repaired or replaced.
 - If the cables and connectors are good, replace the A55 YIG 1. If mid band problems still persist, then replace the A58 M/A/D/S.

High Band Problems: (HP 8722D Only)

1. Press **(SYSTEM) SERVICE MENU SERVICE MODES SRC ADJUST MENU**
DAC NUM HIGH BAND (4000) [x1]. (SRC tune in the high band is capable of tuning the instrument from about 19.5 to 24 GHz). Loss of lock in high band only may likely be due to a bad cable or connection.
2. Referring to the overall block diagram, the following components may be at fault:
 - S1
 - A58 M/A/D/S
 - A54 YIG 2
3. Since the analyzer phase locked in low and/or mid band, all of the phase lock circuitry is working, so look for low power as a cause of phase lock errors,
4. Check power at the output of S1.
 - If the power is less than +5 dBm, check the insertion loss of S1 and the associated cabling.
 - If the power out of S1 is greater than + 5 dBm, the problem is probably above 24 GHz. Proceed with the next steps.
5. Check all RF cabling and connections.
 - If any of the cables or connectors are bad, have them repaired or replaced.
 - If the cables and connectors are good, replace the A54 YIG 2. If high band problems still persist, then replace the A58 M/A/D/S.

Broadband Power Problems

This section assumes that a power problem exists across the full frequency range, and that no error message is displayed. The problem may affect port 1, port 2 or both. Suspect assemblies include:

A69 step attenuator	A59 source interface board	S2
S4 transfer switch	A58 M/A/D/S	A61 bias tee
A62 directional coupler	A60 bias tee	S8
A55 YIG1	A63 directional coupler	S1 (HP 8722D Only)
A54 YIG2 (HP 8722D Only)	A74 switch splitter (Option 400 Only)	

To also troubleshoot port 2 problems, press **MEAS** Refl: **REV S22 (B/R)**.

ALC/Signal Separation Check

1. Press **MENU** **CW FREQ** **3** **G/n**.
2. Choose which port to begin troubleshooting by pressing **MEAS** and **Refl: FWD S11 (A/R)** or **Refl: REV S22 (B/R)**.
3. To Disable the ALC eliminate modulator control, press **SYSTEM** **SERVICE MENU SERVICE MODES** **SRC ADJUST MENU ALC OFF** to . Use a power meter to measure the power at the faulty port:
4. For the HP 8719D/20D:
 - If you measure at least + 5 dBm (+ 10 dBm, Option 007) at the port: replace the A59 source interface board assembly.
 - If you measure less than + 5 dBm (+ 10 dBm, Option 007) at the port: press **MEAS** and **Refl: REV S22 (B/R)** or **Refl: FWD S11 (A/R)** and measure power at the other port:
 - If you measure less than + 5 dBm (+ 10 dBm, Option 007) at the other port: continue with “A69 Step Attenuator Check” next.
 - If you measure at least + 5 dBm (+ 10 dBm, Option 007) at the other port either the directional coupler or the bias tee or the transfer switch (S4) is faulty. The power loss through each of these components should be negligible.

5. For the HP 8722D:

- If you measure at least -8 dBm (-3 dBm, Option 007) at the port: replace the A59 source interface board assembly.
- If you measure less than -8 dBm (-3 dBm, Option 007) at the port: press **MEAS** and **Ref1: REV 522 (B/R)** or **Ref1: FWD S11 (A/R)** and measure power at the other port:
- If you measure less than -8 dBm (-3 dBm, Option 007) at the other port: continue with “A69 Step Attenuator Check” next.
- If you measure at least -8 dBm (-3 dBm, Option 007) at the other port either the directional coupler or the bias tee or the transfer switch (S4) is faulty. The power loss through each of these components should be negligible.

A69 Step Attenuator Check

1. Measure the input and output power of the step attenuator; the loss should be negligible if the attenuator is set to 0 dB.
2. If the 5 dB attenuation steps seem inconsistent, the “Operator’s Check” procedure in Chapter 4, “Start Troubleshooting Here,” can be performed again.

Receiver Troubleshooting

Use this procedure only if you have read Chapter 4, “Start Troubleshooting Here.” Follow the procedures in the order given, unless instructed otherwise.

This section can be used to determine which receiver assembly of the instrument is faulty. The two receiver assemblies that affect all three signal paths are the A10 digital IF and A12 reference assemblies. The receiver assemblies that are associated with specific signal paths are listed in Table 8-1.

Table 8-1. Receiver Assemblies and Associated **Paths**

Signal Path	Port	Directional Coupler	Sampler	2nd Converter
R1	internal	NA	A64	A6
R2 (Option 400)	internal	NA	A67	A6
A	1	A62	A65	A4
B	2	A63	A66	A5

Assembly Replacement Sequence

The following steps show the sequence to replace an assembly in the network analyzer.

1. Identify the faulty group. Refer to Chapter 4, “Start Troubleshooting Here.” Follow up with the *appropriate* troubleshooting *chapter* that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, “Replaceable Parts.”
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, “Assembly Replacement and Post-Repair Procedures.”
4. Perform the necessary adjustments. Refer to Chapter 3, “Adjustments and Correction Constants.”
5. Perform the necessary performance tests. Refer to Chapter 2, “System Verification and Performance Tests.”

All Signal Paths Look Abnormal

For the receiver to operate properly, the A10 digital IF and 2nd converter assemblies must receive signals from the A12 assembly. Those signals are the 2nd LO and the 4 MHz signal.

2nd LO Check

Press **Preset** **PRESET: FACTORY** **SYSTEM** **SERVICE MENU** **ANALOG BUS ON** **Meas** **ANALOG IN: Aux Input** **ANALOG BUS** **(16)** **(x1)** to check the 2nd LO signal with the analog bus counter.

- If the counter reads 9.996 MHz, continue with “4 MHz Check.”
- If the counter does not read 9.996 MHz, perform the “A12 VCO Tune Adjustment.”
 - If the adjustment is successful and the problem is cured, perform the “Frequency Accuracy Performance Test” for verification.
 - If the adjustment is unsuccessful or the problem persists, replace the A12 assembly.

4 MHz Check

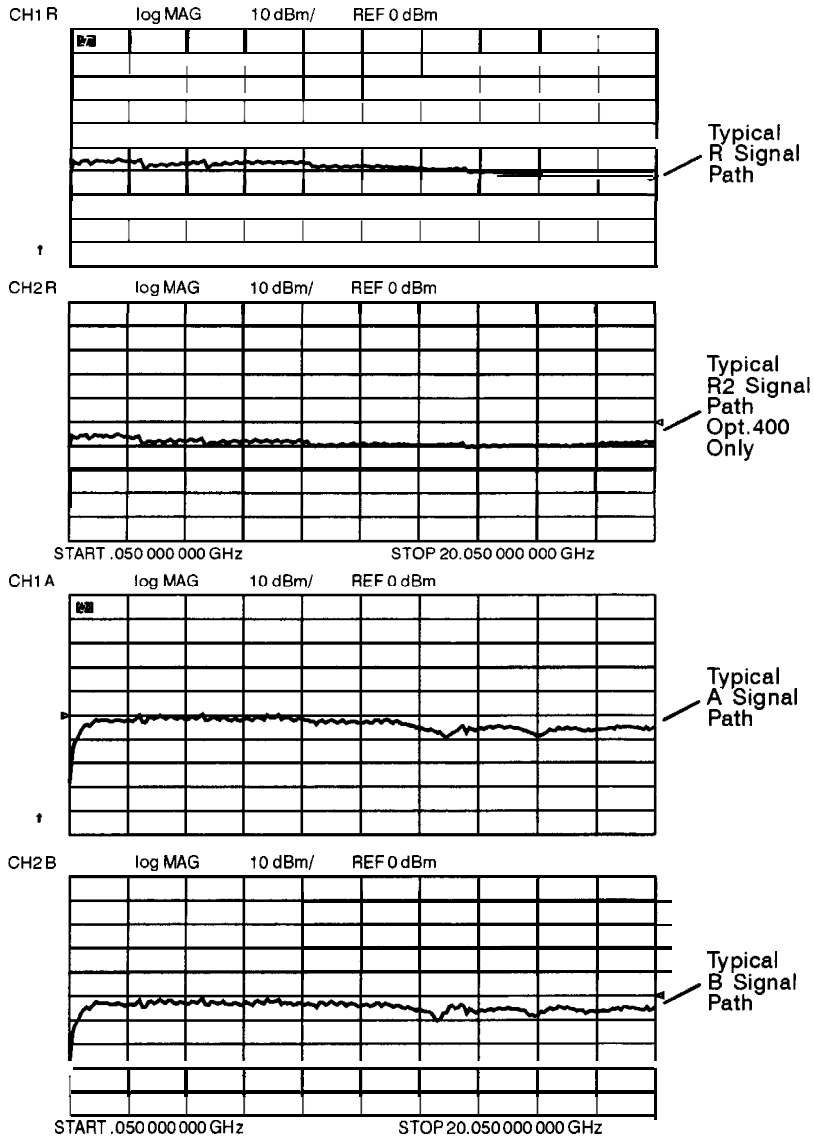
1. Switch off the analyzer.
2. Remove the A10 board and install it onto the extender board.
3. Use an oscilloscope to observe the 4 MHz signal at A10P2 pin 6.
 - If the 4 MHz sine wave signal is present at A10P2 pin 6, replace A10.
 - If the 4 MHz sine wave signal is not present at A10P2 pin 6, check signal at A12P2 pin 36.
 - If the 4 MHz signal is not present at A12P2 pin 36, replace A12.
 - If the 4 MHz signal is present at A12 (but not A10), check the motherboard trace.

At Least One Signal Path Looks Normal

One normal signal path indicates that at least one sampler, one 2nd converter, A12 and much of A10 are functional. Thus substitution is a convenient troubleshooting approach. If two signal paths are abnormal, repeat the steps of this section for each suspect signal path.

1. To see the traces of signal path A or R, connect a short to port 1.
2. Press **[Preset] PRESET: FACTORY [Meas] INPUT PORTS and R** or **4 TESTPORT 1**.
3. To see the traces of signal path B or R2 (if the instrument is an option 400), connect a short to port 2. Then press **[Preset] PRESET: FACTORY [Meas] INPUT PORTS and R**, or **B TESTPORT 2**.
4. Refer to Figure 8-1 to determine if the signal path trace is normal for the HP 8719D/20D. For the HP 8722D, the normal power levels of the traces would appear to be reduced by approximately 15 dBm. Further increase in power (5 dBm) would also be expected for instruments equipped with Option 007.
 - Even if the R signal path trace is abnormal, the R sampler is nonetheless good (or there would be a phase lock problem). Go directly to “2nd Converter Check.”

- **If the A or B signal path is very low and the R signal path is normal, go to “A and B Sampler Check by Substitution.”**
- **If the A or B signal path appears slightly low the problem is possibly a faulty directional coupler or, more probably, a lossy sampler. To isolate the fault, continue with “Directional Coupler Check.”**



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Figure 8-1. **Typical R1, R2, A, and B** Traces

Directional Coupler Check

1. For the HP 8719D/20D, set the output power to -10 dBm by pressing **Menu**
POWER POWER RANGE NAN POWER RANGES RANGE 3 -30 to -10.
2. For the HP 8722D, set the output power to -15 dBm by pressing **Menu**
POWER POWER RANGE NAN POWER RANGES RANGE 3 -25 to -15.
3. Connect a 3.5-mm (f) to 2.4-mm (m) adaptor to one end of the RF flexible cable that is supplied with the tool kit.
4. Connect the RF flexible cable from the output of the A69 step attenuator (3.5-mm) directly to the J2 RF INPUT (2.4 mm) of the suspect sampler.

Note To disconnect the rigid cable of the A69 step attenuator, it may be necessary to disconnect addition rigid cables and loosen the transfer switch.

5. Press **Meas** **INPUT PORTS A TESTPORT 1** to bypass the port 1 coupler and measure the signal at the A sampler or press **Meas** **INPUT PORTS B TESTPORT 2** to bypass the port 2 coupler and measure the signal at the B sampler. Compare the trace to Figure 8-2 for the HP 8719D/20D. For the HP 8722D, the normal power level of the trace would appear to be reduced by approximately 15 dBm. Further increase in power (5 dBm) would also be expected for instruments equipped with Option 007.

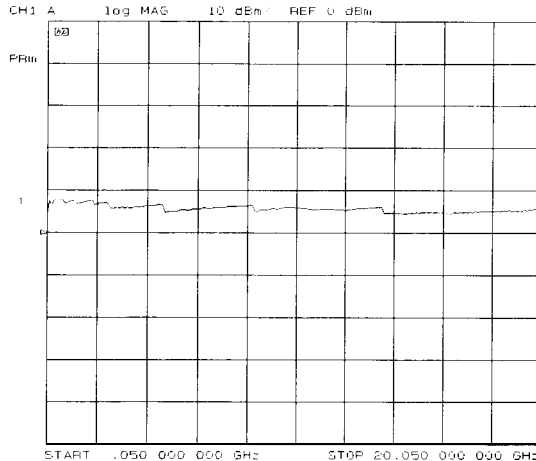


Figure 8-2. Directional Coupler Bypassed

- If the trace is similar to Figure 8-2, the sampler is good. Therefore, the coupler is lossy and should be replaced. Minor power variations are probably due to the flexible cable and are of no concern.
- If the trace is abnormally low, the coupler is good and the sampler is at fault. Troubleshoot the associated sampler by referring to “Sampler Voltage Check.”

A and B Sampler Check by Substitution

1. For the HP 8719D/20D, set the, output power to -10 dBm by pressing (Menu) **POWER POWER RANGE MAN POWER RANGES RANGE 4 -30 to -10**.
2. For the HP 8722D, set the output power to -15 dBm by pressing (Menu) **POWER POWER RANGE MAN POWER RANGES RANGE 2 -25 to -15**.
3. Connect a 3.5-mm (f) to 2.4-mm (m) adaptor to one end of the RF flexible cable that is supplied with the tool kit.
4. Connect the RF flexible cable from the output of the A69 step attenuator (3.5-mm) directly to the J2 RF INPUT (2.4-mm) of the suspect sampler.

Note To disconnect the rigid cable of the A69 step attenuator, it may be necessary to disconnect addition rigid cables and loosen the transer switch.

5. Connect the IF cable from the output of the R sampler, to the IF Output of the suspect sampler.
6. Press (Preset) ~~PRESET~~ FACTORY and see whether the instrument phase locks. Disregard the trace.
 - If the instrument phase locks and no error message is displayed, the sampler under test is normal. Go to “2nd Converter Check.”
 - If the instrument displays the PHASE LOCK CAL FAIL error message, either the sampler or its control and bias voltages are faulty. Continue with “ Sampler Voltage Check. ”

Sampler Voltage Check

Note The BIAS CONTROL line is not used.

1. Measure the SAMPLER CONTROL voltage (green wire) at the suspect sampler. The voltage should be about +0.2 V when the sampler is on.
 - If the sampler control voltage is wrong, replace A51, the interface assembly. (Do NOT replace the sampler: the problem is in the control signals.)
 - If the sampler control voltage is correct, proceed to the next step.
2. Check the + 15 V and -15 V supply voltages.
 - If the supply voltages are within 5% of nominal, replace the sampler.
 - If the supply voltages are incorrect, refer to “A51 Interface Power Supply” at the end of the Source troubleshooting section.

2nd Converter Check

Note Repair signal path R before troubleshooting signal path A or B.

Faulty R Signal Path:

1. If R is the bad signal path, substitute A6 (R 2nd converter) with a 2nd converter from the working signal path.
2. Press **(Meas) INPUT PORTS R** and compare the trace to the signal path R trace of Figure 8-1.
 - If the trace appears normal, replace the faulty 2nd converter.
 - If the trace appears abnormal, replace A10.

Faulty A or B Signal Path:

1. If A is the bad signal path, remove A6 (the working R signal path 2nd converter) and install A4 (the suspect A signal path 2nd converter) in its place.
2. If B is the bad signal path, substitute A6 with A5.
3. Press **(Meas) INPUT PORTS R** and compare the trace to the signal path R trace of Figure 8-1.
 - If the trace appears normal, the substitute 2nd converter is good. Replace A10.
 - If the trace appears abnormal, the substitute 2nd converter is faulty. Replace A4 (or A5).

Accessories Troubleshooting

Use this procedure only if you have read Chapter 4, “Start Troubleshooting Here.” Follow the procedures in the order given, unless instructed otherwise.

Measurement failures can be divided into two categories:

- Failures which don’t affect the normal functioning of the analyzer but render incorrect measurement data.
- Failures which impede the normal functioning of the analyzer or prohibit the use of a feature.

This chapter addresses the first category of failures which are usually caused by the following:

- operator errors
- faulty calibration devices or connectors
- bad cables or adapters
- improper calibration techniques
- RF cabling problems within the analyzer

These failures are checked using the following procedures:

- “Inspect and Gage Connectors”
- “Inspect the Error Terms”

Inspect and Gage Connectors

1. Check for damage to the mating contacts of the test port center conductors and loose connector bulkheads. If the center pin recession is incorrect, replace the entire connector assembly (see Chapter 14, “Assembly Replacement and Post-Repair Procedures.”)
2. Inspect the calibration kit devices for bent or broken center conductors and other physical damage. Refer to the calibration kit operating and service manual for information on gauging and inspecting the device connectors.

If any calibration device is obviously damaged or out of mechanical tolerance, replace the device.

Inspect the Error **Terms**

Error terms are a measure of a “system”: a network analyzer, calibration kit, and any cables used. As required, refer to Chapter 11, “Error Terms,” for the following:

- The specific measurement calibration procedure used to generate the error terms.
- The routines required to extract error terms from the instrument.
- Typical error term data.

Use Table 9-1 to cross-reference error term data to system faults.

Table 9-1. Components Related to Specific Error Terms

Component	Directivity	Source Match	Reflection Tracking	Isolation	Load Match	Transmission Tracking
Calibration Kit						
load	X					
open/short		X	X			
Analyzer						
coupler	X	X	X	X	X	X
bias tee		X	X	X	X	X
transfer switch		X	X	X	X	X
step attenuator		X	X		X	X
sampler			X	X*		X
A10 digital IF				X		
test port connectors	X	X	X	X	X	X
External cables					X	X

* This component is likely to contribute to crosstalk at 4 GHz.

If you detect problems using error term analysis, use the following approach to isolate the fault:

1. Check the cable by examining the load match and transmission tracking terms. If those terms are incorrect, go to “Cable Test”.
2. Verify the calibration kit devices:

Loads: If the directivity error term looks good, the load and the test port are good. If directivity looks bad, connect the same load on the other test port and measure its directivity. If the second port looks bad, as if the problem had shifted with the load, replace the load. If the second port looks good, as if the load had not been the problem, troubleshoot the first port.

Shorts and opens: If the source match and reflection tracking terms look good, the shorts and the opens are good. If these terms look bad while the rest of the terms look good, proceed to “Verify Shorts and Opens”.

Isolate the Fault in the RF Path

Since the calibration devices have been verified, the problem exists in the test port connector, the coupler, or elsewhere in the internal RF path. Table 9-1 shows which assemblies affect each error term. If more than one error term is bad, note which assemblies are common to each of the bad terms. These are the suspects.

The method of fault isolation that must be used is assembly substitution.

Assembly Substitution **Fault** Isolation

At this point, the error term problem has been isolated to a specific port and you should have a list of suspected assemblies.

1. Swap identical assemblies between the port 1 and port 2 signal paths and then regenerate the error terms.
2. If the problem moves from one port to another, you have found the offending assembly.

Note	Before trying this, be sure to inspect the front panel test port connector for obvious damage. Tighten all semi-rigid cable connectors inside the instrument.
------	---

Cable **Test**

The load match error term is a good indicator of cable problems. You can further verify a faulty cable by measuring the reflection of the cable. Perform an S_{11} 1-port calibration directly at port 1 (no cables). Then connect the suspect cable to port 1 and terminate the open end in 50 ohms.

Figure 9-1 shows the return loss trace of a good (left side) and faulty cable.

Note that the important characteristic of a cable trace is its level (the good cable trace is much lower) not its regularity. Refer to the cable manual for return loss specifications.

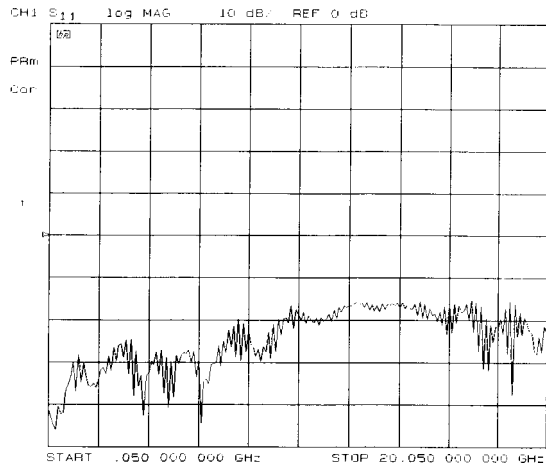


Figure 9-1. Typical Return Loss Trace of a Good Cable

Verify Shorts and Opens

Substitute a known good short and open of the same connector type and sex as the short and open in question. If the devices are not from one of the standard calibration kits, refer to the *HP 8719D/20D/22D Network Analyzer User's Guide* for information on how to use the **MODIFY CAL KIT** function. Set aside the short and open that are causing the problem.

1. Perform an S_{11} 1-port calibration using the good short and open. Then press **Format** **SMITH CHART** to view the devices in Smith chart format.

2. Connect the good short to port 1. Press **Scale Ref** **ELECTRICAL DELAY** and turn the front panel knob to enter enough electrical delay so that the trace appears as a dot at the left side of the circle. (See Figure 9-2a, left.)

Replace the good short with the questionable short at port 1. The trace of the questionable short should appear very similar to the known good short.

3. Connect the good open to port 1. Press **Scale Ref** **ELECTRICAL DELAY** and turn the front panel knob to enter enough electrical delay so that the trace appears as a dot at the right side of the circle. (See Figure 9-2b, right.)

Replace the good open with the questionable open at port 1. The trace of the questionable open should appear very similar to the known good open.

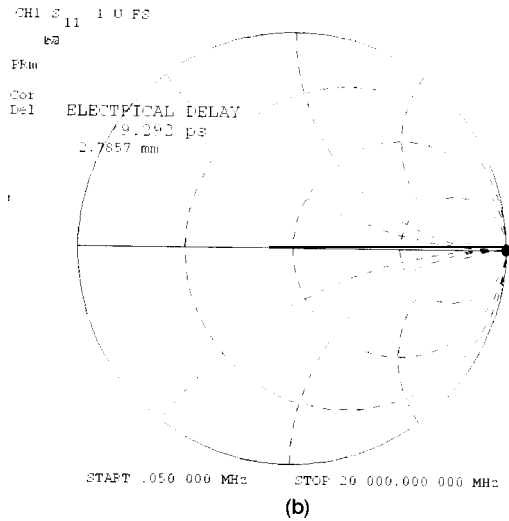
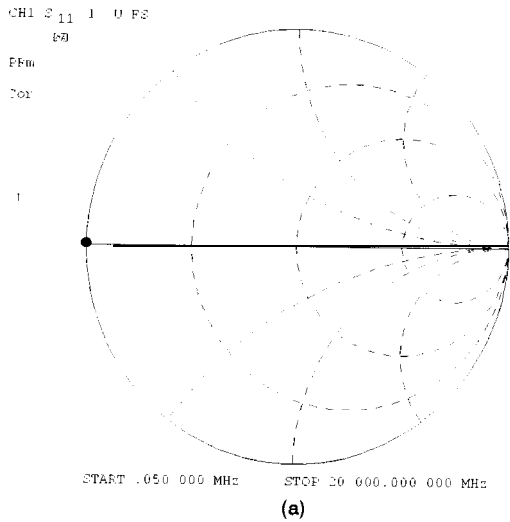


Figure 9-2. Typical Smith Chart Traces of Good Short (a) and Open (b) sb6143d

Service Key Menus and Error Messages

Service Key Menus

These menus allow you to perform the following service functions:

- test
- verify
- adjust
- control
- troubleshoot

The menus are divided into two groups:

1. Internal Diagnostics
2. Service Features

When applicable, the HP-IB mnemonic is written in parentheses following the key. See “HP-IB Service Mnemonic Definitions” at the end of this section.

Note	Throughout this service guide, these conventions are observed: <ul style="list-style-type: none">□ Hardkeys are labeled front panel keys□ SOFTKEYS are display defined keys (in the menus)□ (HP-IB COMMANDS) when applicable, follow the keystrokes in parentheses
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Error Messages

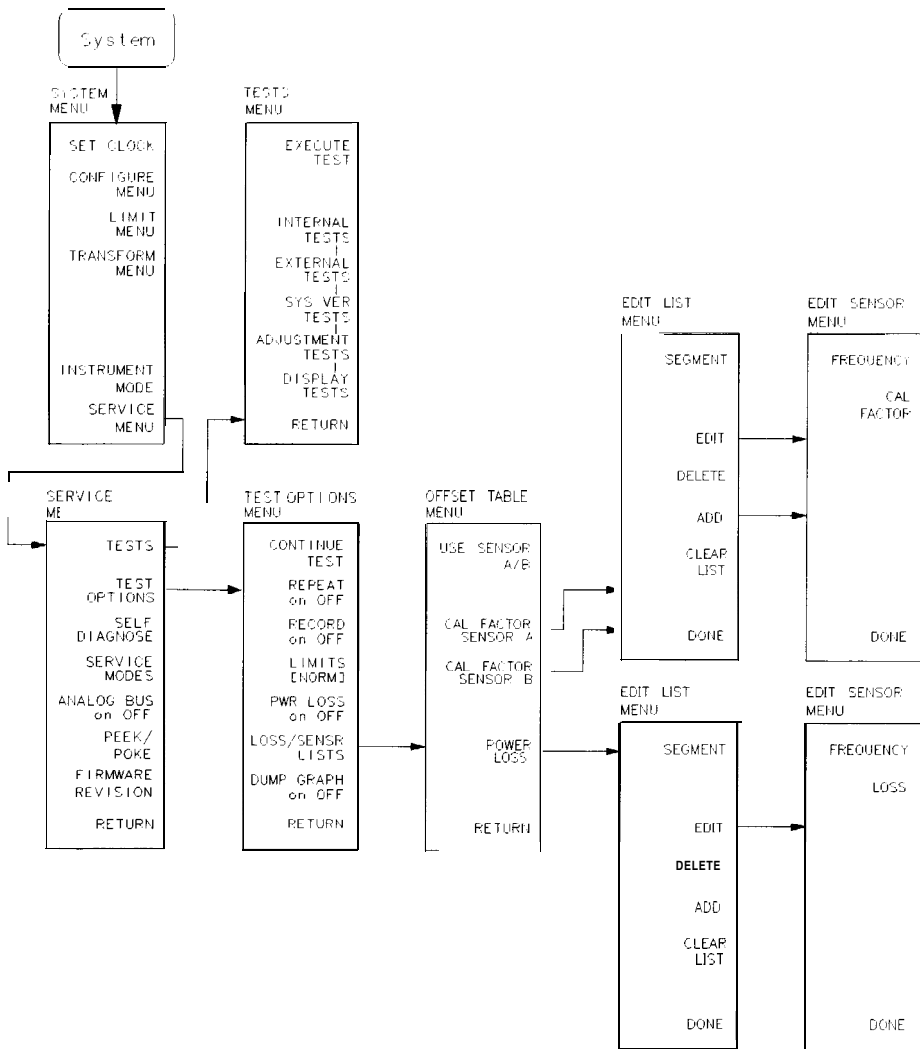
The displayed messages that pertain to service functions are also listed in this chapter to help you:

- Understand the message.
- Solve the problem.

Service Key Menus - Internal Diagnostics

The internal diagnostics menus are shown in Figure 10-1 and described in the following paragraphs. The following keys access the internal diagnostics menus:

- **TESTS**
- **TEST OPTIONS**
- **SELF-DIAGNOSE**



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Figure 10-1. Internal Diagnostics Menus

Tests Menu

To access this menu, press **System** **SERVICE MENU TESTS** .

TESTS (TEST [D]) accesses a menu that allows you to select or execute the service tests. The default is set to internal test 1.

Note Descriptions of tests in each of the categories are given under the heading *Test Descriptions* in the following pages.

The tests are divided by function into the following categories:

- Internal Tests (0–20)
- External Tests (21-25)
- System Verification Tests (26-42)
- Adjustment Tests (43-54)
- Display Tests (55-61)
- Test Patterns (62-76)

To access the first test in each category, press the category softkey. To access the other tests, use the numeric keypad, step keys or front panel knob. The test number, name, and status abbreviation will be displayed in the active entry area of the display.

Table 10-1 shows the test status abbreviation that appears on the display, its definition, and the equivalent HP-IB code. The HP-IB command to output the test status of the most recently executed test is OUTPTESS. For more information, refer to “HP-IB Service Mnemonic Definitions” located at the end of this chapter.

Table 10-1. Test Status Terms

Display Abbreviation	Definition	HP-IB Code
PASS	PASS	0
FAIL	FAIL	1
-IP-	IN PROGRESS	2
(NA)	NOT AVAILABLE	3
-ND-	NOT DONE	4
DONE	DONE	5

EXECUTE TEST (EXET)

runs the selected test and may display these softkeys:

CONTINUE (TESR1) continues the selected test.

YES (TESR2) alters correction constants during adjustment tests.

NEXT (TESR4) displays the next choice.

SELECT (TESR6) chooses the option indicated.

ABORT (TESR8) terminates the test and returns to the tests menu.

INTERNAL TESTS

evaluates the analyzer’s internal operation. These tests are completely internal and do not require external connections or user interaction.

EXTERNAL TESTS

evaluate the analyzer’s external operation. These additional tests require some user interaction (such as keystrokes).

SYS VER TESTS

verifies the analyzer system operation by examining the contents of the measurement calibration arrays. The procedure is in the “System Verification and Performance Tests” chapter. Information about the calibration arrays is provided in the “Error Terms” chapter.

ADJUSTMENT TESTS

generates and stores the correction constants. For more information, refer to the “Adjustments” chapter.

Display Tests

These tests return a PASS/FAIL condition. All six amber front panel LEDs will turn off if the test passes. Press **PRESET** to exit the test. If any of the six LEDs remain on, the test has failed.

- 55 **Disp/cpu** corn. Checks to confirm that the CPU can communicate with the A19 GSP board. The CPU writes all zeros, all ones, and then a walking one pattern to the GSP and reads them back. If the test fails, the CPU repeats the walking 1 pattern until **Preset** is pressed.
- 56 **DRAM cell**. Tests the DRAM on A19 by writing a test pattern to the DRAM and then verifying that it can be read back.
- 57 **Main VRAM**. Tests the VRAM by writing all zeros to one location in each bank and then writing all ones to one location in each bank. Finally a walking one pattern is written to one location in each bank.
- 58 **VRAM bank**. Tests all the cells in each of the 4 VRAM banks.
- 59 **VRAM/video**. Verifies that the GSP is able to successfully perform both write and read shift register transfers. It also checks the video signals LHSYNC, LVSINC, and LBLANK to verify that they are active and toggling.
- 60 **RGB** outputs. Confirms that the analog video signals are correct and it verifies their functionality.
- 61 **Inten** DAC. Verifies that the intensity DAC can be set both low and high.

Test Options Menu

To access this menu, press **(System) SERVICE MENU TEST OPTIONS**.

- TEST OPTIONS** accesses **softkeys** that affect the way tests (routines) run, or supply necessary additional data.
- CONTINUE TEST** (TESRI) resumes the test from where it was stopped.
- REPEAT on OFF** (TO2) toggles the repeat function on and off. When the function is ON, the selected test will run 10,000 times unless you press any key to stop it. The analyzer shows the current number of passes and fails.
- RECORD on OFF** (TO1) toggles the record function on and off. When the function is ON, certain test results are sent to a printer via HP-IB. This is especially useful for correction constants. The instrument must be in system controller mode or pass **control** mode to print (refer to the ‘Printing, Plotting, and Saving Measurement Results’ chapter in the HP *8719D/20D/22D Network Analyzer User’s Guide*).
- LIMITS [NORM/SPCL]** selects either **NORMAL** or **SPeCiaL** (tighter) limits for the Operator’s Check. The SPCL limits are useful for a guard band.
- POWER LOSS** (POWLLIST) accesses the following Edit List menu to allow modification of the external power loss data table.

LOSS/SENSR LISTS

accesses the power loss/sensor lists menu:

USE SENSOR A/B selects the A or B power sensor calibration factor list for use in power meter calibration measurements.

CAL FACTOR SENSOR A (CALFSENA) accesses the Edit List menu to **allow** modification of the calibration data table for power sensor A.

CAL FACTOR SENSOR B (CALFSENB) accesses the Edit List menu to **allow** modification of the calibration data table for power sensor B.

POWER LOSS (POWLLIST) accesses the Edit List menu to allow modification of the external power loss data table that corrects coupled-arm power loss when a directional coupler samples the RF output.

DUMP GRAPH

generates printed graphs of verification results when activated during a system verification.

Edit List Menu To access this menu, press **(System)** **SERVICE MENU**

TEST OPTIONS LOSS/SENSR LISTS and then press one of the following:

CAL FACTOR SENSOR A or **CAL FACTOR SENSOR B** or **POWER LOSS** .

SEGMENT

selects a segment (frequency point) to be edited, deleted from, or added to the current data table. Works with the entry controls.

EDIT (SEDI[D])

allows modification of frequency, **cal** factor and loss values previously entered in the current data table.

DELETE (SDEL)

deletes frequency, **cal** factor and loss values previously entered in the current data table.

ADD (SADD)

adds new frequency, cal factor and loss values to the current data table up to a maximum of 12 segments (frequency points, PTS).

CLEAR LIST (CLEL)

deletes the entire current data table (or list) when **YES** is pressed. Press **NO** to avoid deletion.

DONE (EDITDONE)

returns to the previous menu.

Self Diagnose Softkey

You can access the self diagnosis function by pressing, **(System) SERVICE MENU SELF DIAGNOSE**. This function examines, in order, the pass/fail status of **all internal tests** and displays NO FAILURE FOUND if no tests have failed.

If a failure is detected, the routine displays the assembly or assemblies most probably faulty and assigns a failure probability factor to each assembly.

Test Descriptions

The analyzer has up to 80 routines that test, verify, and adjust the instrument. This section describes those tests.

Internal Tests

This group of tests runs without external connections or operator interaction. All return a PASS or FAIL condition. All of these tests run on power-up and preset except as noted.

- 0 **ALL INT.** Runs only when selected. It consists of internal tests 3-11, 13-16, and 20. Use the front panel knob to scroll through the tests and see which failed. If all pass, the test displays a PASS status. Each test in the subset retains its own test status.
- 1 **PRESET.** Runs the following subset of internal tests: **first**, the ROM/RAM tests 2, 3, and 4; then tests 5 through 11, 14, 15, and 16. If any of these tests fail, this test returns a FAIL status. Use the front panel knob to scroll through the tests and see which failed. If all pass, this test displays a PASS status. Each test in the subset retains its own test status. This same subset is available over HP-IB as "TST?". It is not performed upon remote preset.
- 2 **ROM.** Part of the ROM/RAM tests and cannot be run separately. Refer to the "**Digital** Control Troubleshooting" chapter for more information.

Note The following descriptions of tests 3 and 4 apply to instruments with **firmware** revisions **6.xx** and below.

- 3 CMOS RAM. Verifies the A7 CPU CMOS (long-term) memory with a non-destructive write/read pattern. A destructive version that writes over stored data is shown in **Table 10-2**.
- 4 **Main DRAM**. Verifies the A7 CPU main memory (DRAM) with a non-destructive write/read test pattern. A destructive version is shown in **Table 10-2**. These tests, internal tests 2 through 4, are normally run at preset and power-on. However, a jumper on the A7 CPU assembly, illustrated in **Figure 10-2**, can be set in one of five positions with the following results:

Table 10-2. Descriptions of Jumper Positions

Jumper Position	Position No	Result
ALTER	1	With the jumper in this right position, correction constants can be altered, (updated) during adjustment procedures. The altered correction constants are stored in EEPROM, replacing previously stored correction constants.
CMOS	2	This destructive version of the CMOS RAM test (internal test 3) continuously writes over information stored there.
DRAM	3	This destructive version of the main DRAM test (internal test 4) continuously writes over information stored there.
SKIP	4	For factory use only.
NORMAL	5	The left position is the normal operation position.

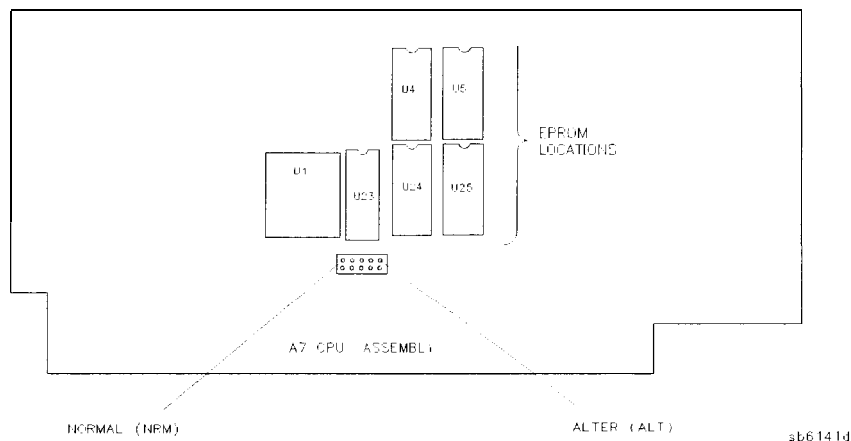


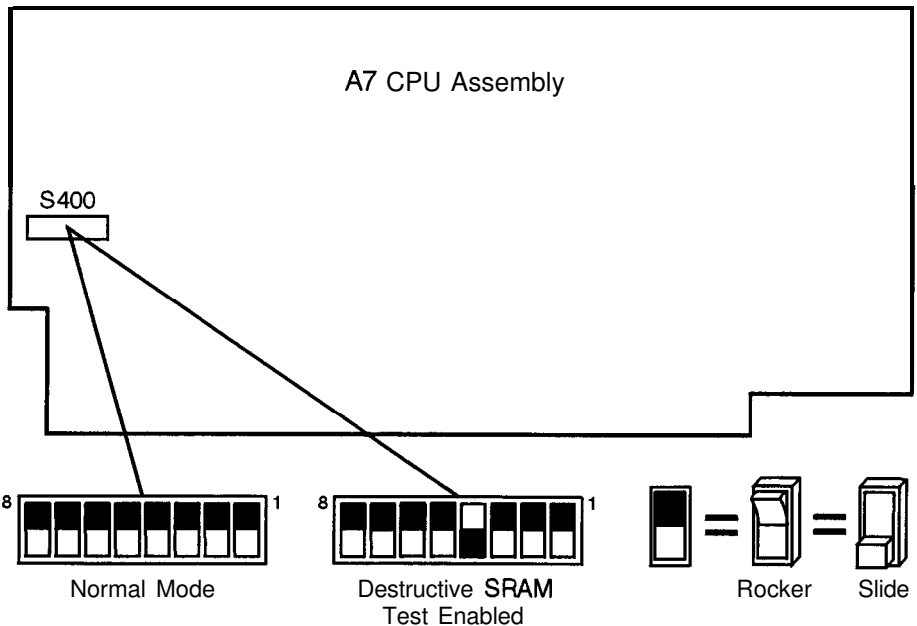
Figure 10-2. Jumper Positions on the A7 CPU

For additional information, see Internal Tests (near the front of this chapter) and the “**Digital** Control Troubleshooting” chapter.

Note

The following descriptions of tests 3 and 4 apply to instruments with firmware revisions **7.xx** and above.

- 3 **SRAM RAM.** Verifies the **A7 CPU SRAM** (long-term) memory with a non-destructive write/read pattern. A destructive version that writes over stored data at power-on can be enabled by changing the **4th** switch position of the **A7 CPU** switch as shown in Figure 10-3.



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Figure 10-3. Switch Positions on the A7 CPU

- 4 **Main DRAM.** Verifies the **A7 CPU** main memory (DRAM) with a non-destructive write/read test pattern. A destructive version of this test is run during power-on.

For additional information, see Internal Tests (near the front of this section) and the “Digital Control Troubleshooting” chapter.

- 5 **DSP Wr/Rd.** Verifies the ability of the main processor and the DSP (digital signal processor), both on the **A7 CPU** assembly, to

communicate with each other through DRAM. This also verifies that programs can be loaded to the **DSP**, and that most of the main RAM access circuits operate correctly.

- 6 **DSP RAM.** Verifies the **A7** CPU RAM associated with the digital signal processor by using a write/read pattern.
- 7 **DSP ALU.** Verifies the **A7** CPU high-speed math processing portions of the digital signal processor.
- 8 **DSP Intrpt.** Tests the ability of the **A7** CPU digital signal processor to respond to interrupts from the **A10** digital IF ADC.
- 9 **DIF Control.** Tests the ability of the **A7** CPU main processor to write/read to the control latches on the **A10** digital IF.
- 10 **DIF Counter.** Tests the ability of the **A7** CPU main processor to write/read to the triple divider on the **A10** CPU. It tests the **A7** CPU data buffers and **A10** digital IF, the 4 MHz clock from the **A12** reference.
- 11 **DSP Control.** Tests the ability of the **A7** CPU digital signal processor to write to the control latches on the **A10** digital IF Feedback is verified by the main processor. It primarily tests the **A10** digital IF, but failures may be caused by the **A7** CPU.
- 12 **Fr Pan Wr/Rd.** Tests the ability of the **A7** CPU main processor to write/read to the front panel processor. It tests the **A2** front panel interface and **processor, and A7** CPU data buffering and address decoding. (See also tests 23 and 24 below.) This runs only when selected.
- 13 **Rear Panel.** Tests the ability of the **A7** CPU main processor to write/read to the rear panel control elements It tests the **A16** rear panel, and **A7** CPU data buffering and address decoding. (It does not test the HP-IB interface; for that see the HP-IB Programming Guide.) This runs only when selected or with ALL INTERNAL.
- 14 **Post Reg.** Polls the status register of the **A8** post-regulator, and flags these conditions: heat sink too hot, inadequate air flow, or post-regulated supply shutdown.

- 15 **Frac N Cont.** Tests the ability of the **A7** CPU main processor to write/read to the control element on the **A14** fractional-N (digital) assembly. The control element must be functioning, and the fractional-N VCO must be oscillating (although not necessarily phase-locked) to pass.
- 16 **Sweep Trig.** **Tests** the sweep trigger (L SWP) line from the **A14** fractional-N to the **A10** digital IF. The receiver with the sweep synchronizes L SWI?
- 17 **ADC Lin.** It tests the linearity of the **A10** digital IF ADC using the built-in ramp generator. The test generates a histogram of the ADC linearity, where each data point represents the relative “width” of a particular ADC code. **Ideally, all** codes have the same width; different widths correspond to non-linearities.
- 18 **ADC Ofs.** **This runs only** when selected. It tests the ability of the offset DAC, on the **A10** digital IF, to apply a bias offset to the IF signals before the ADC input. This runs **only** when selected.
- 19 **ABUS Test.** Tests analog bus accuracy, by measuring several analog bus reference voltages (**all** nodes from the **A10** digital IF). This runs **only** when selected.
- 20 **F’N Count.** Uses the internal counter to count the **A14** fractional-N VCO frequency (120 to 240 MHz) and the divided fractional-N frequency (100 kHz). It requires the 100 kHz signal from **A12** and the counter gate signal from **A10** to pass.

External Tests

These tests require either external equipment and connections or operator interaction of some kind to run. Tests 30 and 60 are comprehensive front panel checks, more complete than test 12, that checks the front panel keys and knob entry.

- 21 **Op Ck Port 1** Part of the “Operator’s Check” procedure, located in Chapter 4, “Start Troubleshooting Here.” The procedure requires the external connection of a short to PORT 1.
- 22 **Op Ck Port 2** Same as 21, but tests PORT 2.
- 23 **Fr Pan Seq.** Tests the front panel knob entry and all A1 front panel keys, as well as the front panel microprocessor on the A2 assembly. It prompts the user to rotate the front panel knob, then press each key in an ordered sequence. It continues to the next prompt only if the current prompt is correctly satisfied.
- 24 **Fr Pan Diag. Similar** to 23 above, but the user rotates the front panel knob or presses the keys in any order. This test displays the command the instrument received.
- 25 **ADC Hist. Factory** use only.

System Verification Tests

These tests apply mainly to system-level, error-corrected verification and troubleshooting. Tests 26 to 30 are associated with the system verification procedure, documented in the “System Verification and Performance Tests” chapter. Tests 31 to 42 facilitate examining the calibration coefficient arrays (error terms) resulting from a measurement calibration; refer to the “Error Terms” chapter for details.

- 26 Sys Ver Init. Recalls the initialization state for system verification from an analyzer verification disk, in preparation for a measurement calibration. It must be done before service internal tests 27, 28, 29 or 30 are performed.
- 27 **Ver Dev 1.** Recalls verification limits from disk for verification device #1 in all applicable S-parameter measurements. It performs pass/fail limit testing of the current measurement.
- 28 **Ver Dev 2. Same as 28 above** for device #2.
- 29 **Ver Dev 3. Same as 28 above** for device #3.
- 30 **Ver Dev 4. Same as 28 above** for device #4.
- 31-42 **Cal Coef 1-12.** Copies error term data from a measurement calibration array to display memory. A measurement calibration must be complete and active. The **definition** of calibration arrays depends on the current calibration type. After execution, the memory is automatically displayed. Refer to the “Error **Term**” chapter for details.

Adjustment **Tests**

The tests without asterisks are used in the procedures located in the “Adjustments” chapter of this manual, except as noted.

- 43 **Pretune Adj** Generates source pretune values for proper phase-locked loop operation. Run test 44 first.
- 44 **ABUS Cor.** Measures three **fixed** voltages on the **ABUS**, and generates new correction constants for **ABUS** amplitude accuracy in both high resolution and low resolution modes. Use this test before running test 43, above.
- 45 **Intensity Cor.** Stores the current values of the intensity adjustments under **(DISPLAY)** for **recall** of display intensity values at power-on.
- 46 **Disp 2 Ex.** Not used in “Adjustments.” Writes the “secondary test pattern” to the display for adjustments. Press **(Preset)** to exit this routine.
- 47 **IF Step Cor.** Measures the gain of the IF amplifiers (A and B only) located on the **A10** digital IF, to determine the correction constants for absolute amplitude accuracy. It provides smooth dynamic accuracy and absolute amplitude accuracy in the **-30 dBm** input power region.
- 48 **ADC Ofs Cor.** Measures the **A10** Digital IF ADC linearity characteristics, using an internal ramp generator, and stores values for the optimal operating region. During measurement, IF signals are centered in the optimal region to improve low-level dynamic accuracy.
- 49 **Serial Cor.** Stores the serial number (input by the user in the Display Title menu) in EEPROM. This routine will not overwrite an existing serial number.
- 50 **Option Cm.** Stores the option keyword (required for Option 007, 010 or any combination).
- 51 ***Cal Kit Def.** Loads the default calibration kit definitions (device model coefficients) into EEPROM.

- 52 Power **Adj** This test measures power linearity at the test port. It **also** generates correction constants to improve power linearity.
- 53 **Init** EEPROM. This test initializes certain EEPROM addresses to zeros and resets the display intensity correction constants to the default values. Also, the test will not alter the serial number and correction constants for Option 007 or 010.
- 54 Blanking **Adj** This test allows adjustment of the output power level during retrace.

Display Tests

These tests do not return a **PASS/FAIL** condition. All six amber front panel **LEDs** will turn off if the test passes. The display will be blank; press **Preset** to exit the test. If any of the six **LEDs** remain on, the test has failed.

- 55 **Disp/cpu corn.** Checks to **confirm** that the CPU can communicate with the **A19** GSP board. The CPU writes all zeros, all ones, and then a **walking** one pattern to the GSP and reads them back. If the test fails, the CPU repeats the walking 1 pattern until **PRESET** is pressed.
- 56 **DRAM cell.** Tests the DRAM on **A19** by writing a test pattern to the DRAM and then verifying that it can be read back.
- 57 **Main VRAM.** Tests the VRAM by writing all zeros to one location in each bank and then writing all ones to one location in each bank. Finally a walking one pattern is written to one location in each bank.
- 58 **VRAM bank.** Tests all the cells in each of the 4 VRAM banks.
- 59 **VRAM/video.** Verifies that the GSP is able to successfully perform both write and read shift register transfers. It also checks the video signals **LHSYNC**, **LVSUNC**, and **LBLANK** to verify that they are active and toggling.
- 60 **RGB** outputs. Confirms that the analog video signals are correct and it verifies their functionality.
- 61 **Inten DAC.** Verifies that the intensity DAC can be set both low and high.

Test Patterns

Test patterns are used in the factory for adjustments, diagnostics, and troubleshooting, but most are not used for field service. Test patterns are **executed** by entering the test number (62 through **76**), then pressing **EXECUTE TEST CONTINUE**. The test pattern will be displayed and the softkey labels blanked. To increment to the next pattern press **softkey** 1, to go back to a previous pattern press **softkey** 2. To exit the test pattern and return the **softkey** labels, press **softkey** 8 (bottom softkey). The following is a description of the test patterns.

- 62 **Test Fat 1.** Displays an all white screen for verifying the light output of the **A18** display and checks for color purity.

- 63-65 **Test Pat 2-4.** Displays a red, green, and blue pattern for verifying the color purity of the display and also the ability to independently control each color.
- 66 **Test Fat 5.** Displays an all black screen. This is used to check for stuck pixels.
- 67 **Test Pat 6.** Displays a **16-step** gray scale for verifying that the **A19** GSP board can produce 16 different amplitudes of color (in this case, white.) The output comes from the RAM on the GSP board, it is then split. The signal goes thru a video DAC and then to an external monitor or thru some buffer amplifiers and then to the internal LCD display. If the external display looks good but the internal display is bad then the problem may be with the display or the cable connecting it to the GSP board. This pattern is also very useful when using an oscilloscope for troubleshooting. The staircase pattern it produces will quickly show missing or stuck data bits.
- 68 **Test Pat 7.** Displays the following seven colors. Red, Yellow, Green, Cyan, Blue, Magenta and White.
- 69 **Test Pat 8.** This pattern is intended for use with an external display. The pattern displays a color rainbow pattern for showing the ability of the **A19** GSP board to display 15 colors plus white. The numbers written below each bar indicate the tint number used to produce that bar (**0 & 100=pure red, 33=pure green, 67=pure blue**).
- 70 **Test Pat 9.** Displays the three primary colors Red, Green, and Blue at four different intensity levels. You should see 16 color bands across the screen. Starting at the left side of the display the pattern is; Black four bands of Red (each band increasing in intensity) Black four bands of Green (each band increasing in intensity) Black four bands of Blue (each band increasing in intensity) Black If any one of the four bits for each color is missing the display will not look as described.

- 71 **Test Pat 10.** Displays a character set for showing the user all the different types and sizes of characters available. Three sets of characters are drawn in each of the three character sizes. 125 characters of each size are displayed. Characters 0 and 3 cannot be drawn and several others are really control characters (such as carriage return and line feed).
- 72 **Test Fat 11.** Displays a bandwidth pattern for verifying the bandwidth of the EXTERNAL display. It consists of multiple alternating white and black vertical stripes. Each stripe should be clearly visible. A limited bandwidth would smear these lines together. This is used to test the quality of the external monitor.
- 73 **Test Pat 12.** Displays a repeating gray scale for troubleshooting, using an oscilloscope. It is similar to the 16 step gray scale but is repeated 32 times across the screen. Each of the 3 outputs of the video palette will then show 32 ramps (instead of one staircase) between each horizontal sync pulse. This pattern is used to troubleshoot the pixel processing circuit of the **A19** GSP board.
- 74 **Test Pat 13.** Displays a convergence pattern for measuring the accuracy of the color convergence of the external monitor.
- 75-76 **Test Pat 14-15.** Displays crosshatch and inverse crosshatch patterns for testing color convergence, linearity, and alignment. This is useful when aligning the LCD display in the bezel.

Service Key Menus - Service Features

The service feature menus are shown in 10-3 and described in the following paragraphs. The following keys access the service feature menus:

- **SERVICE MODES**
- **ANALOG BUS on OFF**
- **PEEK/POKE**
- **FIRMWARE REVISION**

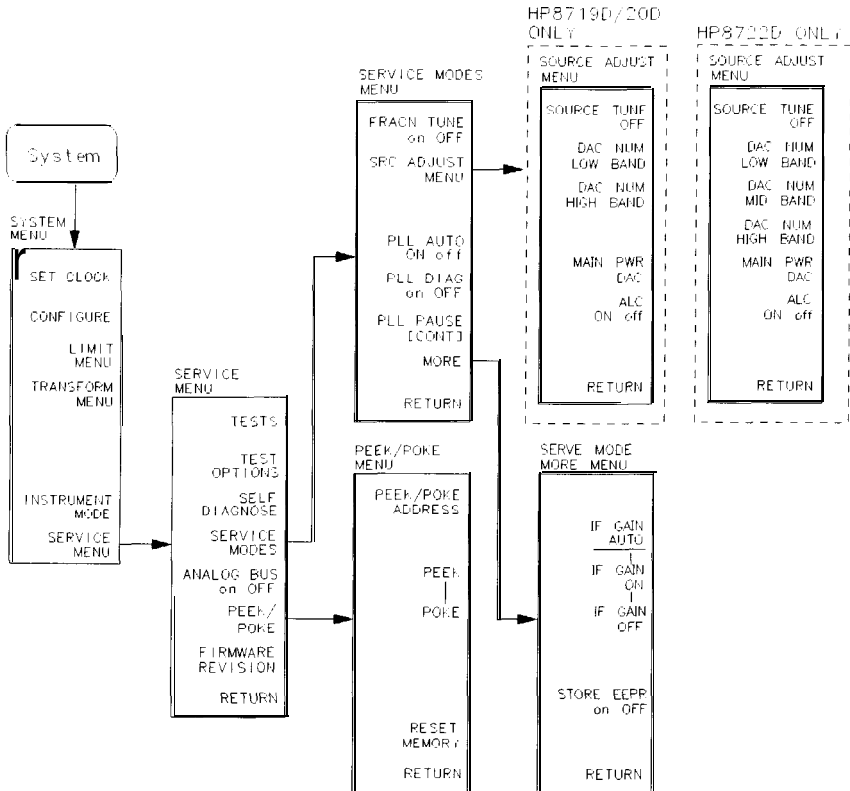


Figure 10-4. Service Feature Menus

Service Modes Menu

To access this menu, press: **System** **SERVICE MENU** **SERVICE MODES**

SERVICE MODES

allows you to control and monitor various circuits for troubleshooting.

FRACN TUNE on OFF (SM1)

tests the **A13** and **A14** fractional-N circuits. It **allows** you to directly control and monitor the output frequency of the fractional-N synthesizer (60 MHz to 240 MHz).

Set the instrument to CW sweep mode and then set FRACN TUNE ON. Change frequencies with the front panel keys or knob. The output of the **A14** assembly can be checked at **A14J1 HI OUT** (in high band) or **A14J2 LO OUT** (in low band) with an oscilloscope, a frequency counter, or a spectrum analyzer. **Signal** jumps and changes in shape at 20 MHz and 30 MHz when tuning up in frequency, and at 29.2 MHz and 15 MHz when tuning down, are due to switching of the digital divider. This mode can be used with the SRC TUNE mode as described in “Source Troubleshooting” chapter.

SRC ADJUST MENU

accesses the functions that allow you to adjust the source:

Note

If the instrument displays the PHASE LOCK CAL FAILED message, use the **DAC NUM XXX BAND** keys below. The relationship between DAC numbers and frequency varies from instrument to instrument. The DAC numbers and frequencies below are guidelines only.

SOURCE TUNE OFF (SM2D) disables the source frequency tune modes.

DAC NUM XXX BAND tests the pretune functions of the phase lock and source assemblies. These keys allow entry of digital data directly into the DAC on the All phase lock assembly. When in this mode:

- Instrument does not attempt to phase lock.
- Residual FM increases.

DAC NUM LOW BAND (SM2L) allows you to enter DAC numbers in the range of 3650 through 4095 to generate test port output frequencies from .050 GHz to 1.1 GHz.

DAC NUM MID BAND (SM2M) (HP 8722D Only) allows you to enter DAC numbers in the range of 2900 through 4095 to generate test port output frequencies from 2.3 GHz to 4.9 GHz.

DAC NUM HIGH BAND (SM2H) (HP 8719D/20D) allows you to enter DAC numbers in the range of 2900 through 4095 to generate test port output frequencies from 2.3 GHz to 4.9 GHz.

DAC NUM HIGH BAND (SM2H) (HP 8722D) allows you to enter DAC numbers in the range of 2020 through 4095 to generate test port output frequencies from 18.2 GHz to 23.2 GHz.

MAIN PWR DAC

ALC ON off toggles the automatic leveling control (ALC) on and off.

PLL AUTO ON off (SM4) automatically attempts to determine new pretune values when the instrument encounters phase lock problems (for example, “harmonic skip”). With **PLL AUTO OFF** the frequencies and voltages do not change, like when they are attempting to determine new **pretune** values, so troubleshooting the phase-locked loop circuits is more convenient. This function may also be turned off to avoid pretune calibration errors in applications where there is a limited frequency response in the R

(reference) channel. For example, in a high power test application, using band limited **filters** for R channel phase locking.

PLL DIAG on OFF (SM5) displays a phase lock sequence at the beginning of each band. This sequence normally occurs very rapidly, making it difficult to troubleshoot phase lock problems. Switching this mode ON slows the process down, allowing you to inspect the steps of the phase lock sequence (pretune, acquire, and track) by pausing at each step. The steps are indicated on the display, along with the channel (C1 or C2) and band number (B1 through B13).

This mode can be used with PLL PAUSE to halt the process at any step. It can **also** be used with the analog bus counter.

PLL PAUSE is used only with PLL DIAG mode. **CONT** indicates that it will continuously cycle through **all** steps of the phase lock sequence. **PAUSE** holds it at any step of interest. This mode is **useful** for troubleshooting phase-locked loop problems.

MORE accesses the service modes more menu listed below.

Service Modes More Menu

To access this menu, press **System** **SERVICE MENU** **SERVICE MODES** **MORE**.

IF GAIN AUTO is used for normal operating conditions and works in conjunction with IF GAIN ON and OFF. The **A10** assembly includes a switchable attenuator section and an amplifier that amplifies low-level **4 kHz** IF signals (for A and B inputs only). This mode allows the **A10** IF section to automatically determine if the attenuator should be switched in or out. The switch occurs when the A or B input signal is approximately **-30 dBm**.

IF GAIN ON locks out the **A10** IF attenuator sections for checking the **A10** IF gain amplifier circuits, regardless of the amplitude of the A or B IF signal.

Turning this ON switches out both the A and B attenuation circuits; they cannot be switched independently. Be aware that input signal levels above -30 dBm at the sampler input will saturate the ADC and cause measurement errors.

IF GAIN OFF

switches in both of the A10 IF attenuators for checking the A10 IF gain amplifier circuits. Small input signals will appear noisy, and raise the apparent noise floor of the instrument.

STORE EEPR on OFF

allows you to store the correction constants that reside in non-volatile memory (EEPROM) onto a disk. Correction constants improve instrument performance by compensating for specific operating variations due to hardware limitations (refer to the “Adjustments” chapter). Having this information on disk is useful as a backup, in case the constants are lost (due to a CPU board failure). Without a disk backup the correction constants can be regenerated manually, although the procedures are more time consuming.

ANALOG BUS on OFF (ANAB)

enables and disables the analog bus, described below. Use it with the analog in menu, (a description of this menu follows).

Analog Bus

To access the analog bus, press **(System) SERVICE MENU ANALOG BUS ON**.

Description of the Analog Bus

The analog bus is a single multiplexed line that networks 23 nodes within the instrument. It can be controlled from the front panel, or through HP-IB, to make voltage and frequency measurements just like a voltmeter, oscilloscope, or frequency counter. The next few paragraphs provide general information about the structure and operation of the analog bus. See “Analog Bus Nodes,” below, for a description of each individual node. Refer to the “Overall Block Diagram,” in the “Start Troubleshooting” chapter, to see where the nodes are located in the instrument.

The analog bus consists of a source section and a receiver section. The source can be the following:

- any one of the 23 nodes described in “Analog Bus Nodes”
- the **A14** fractional-N VCO
- the **A14** fractional-N VCO divided down to 100 kHz

The receiver portion can be the following:

- the main ADC
- the frequency counter

When analog bus traces are displayed, frequency is the x-axis. For a linear x-axis in time, switch to CW time mode (or sweep a single band).

The Main ADC

The **main** ADC is located on the **A10** digital IF assembly and makes voltage measurements in two ranges. See “**RESOLUTION**”, under “Analog In Menu”.

The Frequency Counter

The frequency counter is located on the **A14** assembly and can count one of three sources:

- selected analog bus node
- **A14** fractional-N VCO (FRAC N)
- **A14** fractional-N VCO divided down to 100 kHz (DIV FRAC N) (frequency range is 100 kHz to 16 MHz)

The counts are triggered by the phase lock cycle; one at each pretune, acquire, and track for each bandswitch. The counter works in swept modes or in CW mode. It can be used in conjunction with **SERVICE MODES** for troubleshooting phase lock and source problems

To read the counter over HP-IB, use the command OUTPCNTR.

Notes

- The display and marker units (**U**) correspond to volts.
- About 0.750 MHz is a typical counter reading with no AC signal present.
- Anything occurring during bandswitches is not visible.
- Fast-moving waveforms may be sensitive to sweep time.
- The analog bus input **impedance** is about **50K** ohms.
- Waveforms up to approximately 200 Hz can be reproduced.

Analog In Menu

Select this menu to monitor voltage and frequency nodes, using the analog bus and internal counter, as explained below.

To switch on the analog bus and access the analog in menu, press:

System **SERVICE MENU** **ANALOG BUS ON** **Meas** **ANALOG IN Aux Input**

The **RESOLUTION [LOW]** key toggles between low and high resolution.

Resolution	Maximum Signal	Minimum Signal
LOW	+ 0.5 V	-0.5 V
HIGH	+ 10 V	-10 V

AUX OUT on OFF allows you to monitor the analog bus nodes (except nodes 1, 2, 3, 4, 9, 10, 12) with external equipment (oscilloscope, voltmeter, etc). To do this, connect the equipment to the AUX INPUT BNC connector on the rear panel, and press **AUX OUT**, until **ON** is highlighted.

Caution To prevent damage to the analyzer, **first** connect the signal to the rear panel AUX INPUT, and then switch the function ON.

COUNTER: OFF switches the internal counter off and removes the counter from the display. The counter can be switched on with one of the next three keys. (Note: Using the counter slows the sweep.) The counter bandwidth is 16 **MHz unless** otherwise noted for a specific node.

Note OUTPCNTR is the HP-IB command to output the counter's frequency data.

ANALOG BUS

switches the counter to monitor the analog bus.

FRAC N

switches the counter to monitor the **A14** fractional-N VCO frequency at the node shown on the “Overall Block Diagram, ” in the “Start Troubleshooting” chapter.

DIV FRAC N

switches the counter to monitor the **A14** fractional-N VCO frequency after it has been divided down to 100 **kHz** for phase locking the VCO.

Analog Bus Nodes

The following paragraphs describe the 23 analog bus nodes. They are listed in numerical order and are grouped by assembly. Refer to the “Overall Block Diagram” for node locations.

Press **(USER PRESET)** **(System)** **SERVICE MENU INPUT PORTS ANALOG BUS** and then use the front panel keys or knob to select an analog bus node. Terminate the entry by pressing **(x1)**.

A10 Digital IF

1. + **0.37V** (+ 0.37 V reference)

Check for a flat line at approximately +**0.37V**. This is used as the voltage reference in the Analog Bus Correction Constants adjustment for calibrating out the analog bus **high/low** resolution gain and offset errors. The absolute voltage level is not critical, but it should be the same in high and low resolution.

2. + **2.50V** (+ 2.50 V reference)

Check for a flat line at approximately +**2.5V**. This voltage is used in the Analog Bus Correction Constants adjustment as a reference for calibrating the analog bus low resolution circuitry.

3. **Aux Input** (Rear panel input)

This selects the rear panel AUX INPUT to drive the analog bus for making voltage and frequency measurements. It can be used to look at test points within the instrument on the CRT (using the CRT as an oscilloscope). Connect the test point of interest to the AUX INPUT BNC connector on the rear panel. This feature can be useful if an oscilloscope is not available. Also, it can be used for testing voltage-controlled devices by connecting the driving voltage of the DUT to the AUX IN connector. You can look at the driving voltage on one display channel while displaying the DUT S-parameter response on the other display channel.

With **AUX OUT** turned ON, you can **examine analog** bus nodes with external equipment (see **AUX OUT** on **OFF** under the “Analog Bus Menu” heading). See “**HP-IB Service Mnemonic Definitions**” for HP-IB considerations.

4. **A10 Gnd** (Ground reference)

This is used in the “Analog Bus Correction Constants” adjustment as a reference for calibrating the analog bus low and high resolution circuitry.

All Phase Lock

5. All Gnd (Ground reference)
6. All Gnd (Ground reference)
7. All Gnd (Ground reference)
8. Swp Err (Phase error voltage)

This node measures the voltage at the output of the phase comparator on the All phase lock assembly. This error voltage corresponds to the difference

in frequency between the divided IF and the 1 MHz reference frequency from the **A12** assembly.

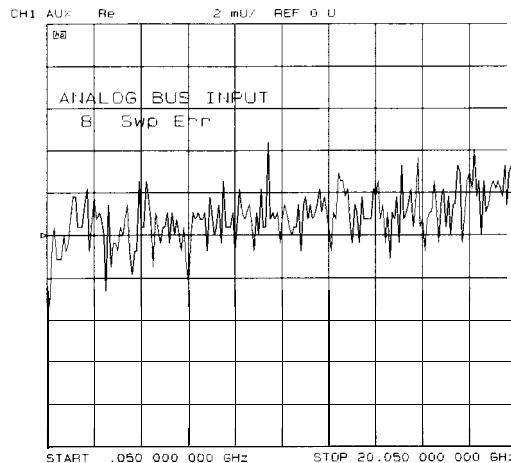


Figure 10-5. Node 8: Swp Err, Phase Error Voltage

9. **0.25V/GHz** (Source oscillator tuning voltage)

This node displays the tuning voltage ramp used to tune the source oscillators. You should see a voltage ramp like the one shown in Figure 10-5. If this waveform is correct, you can be confident that the All phase lock assembly, the source assemblies, the **A13/A14** fractional-N assemblies, and

the **A52** pulse generator are working properly and the instrument is phase locked. If you see anything else, refer to the “Source Troubleshooting” chapter.

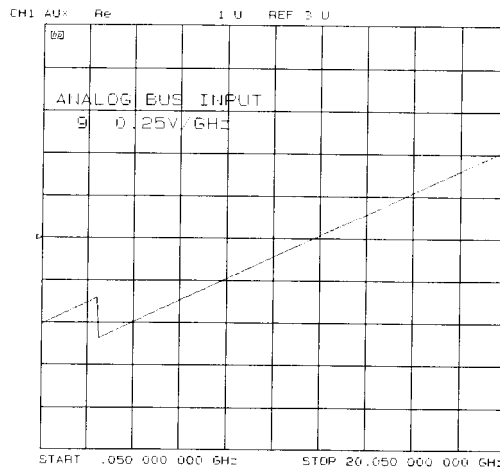


Figure 10-6. Node 9: 0.25V/GHz, Source Tuning Voltage

10. **All Gnd** (Ground reference)

11. **IF** (IF used for phase lock)

Counter ON: analog bus Reading: 10 MHz

This node displays the IF frequency (see Figure 10-6) as it enters the All phase lock assembly via the **A7** ALC assembly. This signal comes from the R sampler output and is used to phase lock the source.

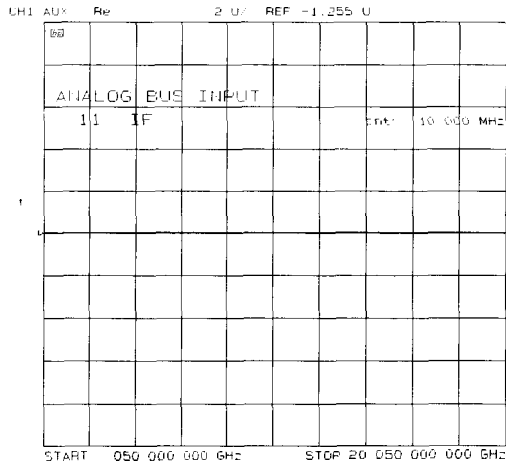


Figure 10-7. Location of Internal Counter Wading on Display

12. IF Det (IF on All phase lock after 40 MHz filter)

This node detects the IF as a voltage at the output of the 40 MHz filter on the All phase lock assembly. The trace should be a flat line at about -1.7 V as shown in Figure 10-7.

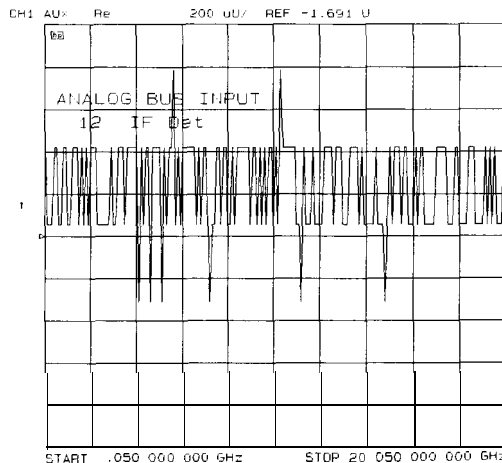


Figure 10-8. Node 12: Typical IF Detector Voltage Trace

A12 Reference

13. Ext Ref (Rear panel external reference input)

This node is used to detect an external reference voltage. If an external reference (timebase) is used, the voltage level should be about -0.6V . If an external reference is not used, the voltage level should be about -0.87V .

14. 100 kHz (100 kHz reference frequency)

Counter ON: analog bus

Reading: .100 MHz

This node counts the **A12 100 kHz** reference signal that is used on **A13** (the fractional-N analog assembly) as a reference frequency for the phase detector.

15. VCO Tune (A12 VCO tuning voltage)

This node displays the tuning voltage for the **A12 VCO**. It is used in the reference assembly VCO tune adjustment.

16. 2nd LO (2nd converter reference)

Counter ON: analog bus

Reading: 9.996 MHz

This node counts the **2nd LO** used by the **2nd** converter assemblies to produce the **2nd IF** of **4 kHz**.

17. PL Ref (Phase lock reference)

Counter ON: analog bus

Reading: 1 MHz

This node counts the reference signal used by the phase comparator circuit on the All phase lock assembly.

18. VCXO Tune (40 MHz VCXO tuning voltage)

This node displays the voltage used to **fine** tune the **A12** reference VCXO to 40 MHz. You should see a flat line at some voltage level (the actual voltage level varies from instrument to instrument). Anything other than a flat line indicates that the VCXO is tuning to different frequencies. Refer to the frequency accuracy adjustment in the “Adjustments and Correction Constants” chapter.

- 19. **A12 Gnd** (Ground reference)
- 20. **A12 Gnd** (Ground reference)

A14 Fractional-N (Digital)

- 21. **FN VCO Tun** (A14 FN VCO tuning voltage)

This node displays the **A14 FN VCO** tuning voltage. **This** voltage comes from the **A13** fractional-N (analog) assembly and is the return path for the fractional-N phase-locked loop. If the **A13** and **A14** assemblies are functioning properly and the VCO is phase locked, the trace should look like the trace shown in **Figure 10-8** when in **Log Freq.** sweep mode. Any other waveform indicates that the **FN VCO** is not phase locked. The vertical lines in the trace indicate the band crossings. (The counter can also be enabled to count the VCO frequency. Use CW mode.)

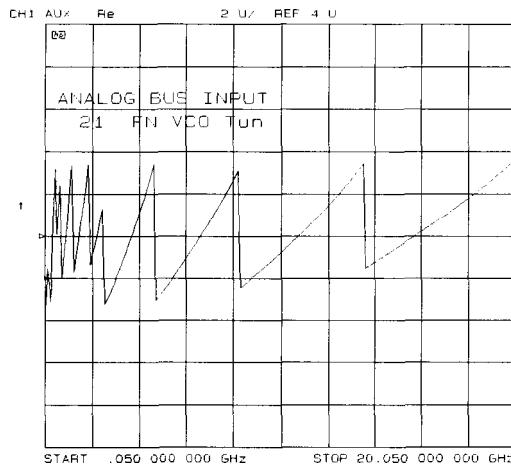


Figure 10-9. Node 21: FN VCO Tun, FN VCO Tuning Voltage

- 22. **A14 Gnd** (Ground reference)
- 23. **Count Gate** (Analog bus counter gate)

This node checks the analog bus counter gate signal. You should see a flat line at **+5V**. The counter gate activity occurs during bandswitches, and therefore is not visible on the analog bus. **To** view the bandswitch

activity, look at this node on an oscilloscope, using **AUX OUT ON** (refer to **AUX OUT on OFF** under the “Analog Bus Menu” heading).

PEEK/POKE Menu

To access this menu, press **(SYSTEM) SERVICE MENU PEEK/POKE**.

PEEK/POKE

Allows you to edit the content of one or more memory addresses. The keys are described below.

Caution The PEEK/POKE **capability** is intended for service use only.

PEEK/POKE ADDRESS (PEEK[D])

accesses any memory address and shows it in the active entry area of the display. Use the front panel knob, entry keys, or step keys to enter the memory address of interest.

PEEK (PEEK)

Displays the data at the accessed memory address.

POKE (POKE[D])

allows you to change **the** data at the memory address accessed by the **PEEK/POKE ADDRESS softkey**. Use the front panel knob, entry keys, or step keys to change the data. The **A7CC** jumper must be in the “**ALT**” position in order to poke.

RESET MEMORY

Resets or clears the memory where instrument states are stored. To do this, press **RESET MEMORY (PRESET)**.

Firmware Revision Softkey

Press **(SYSTEM) SERVICE MENU FIRMWARE REVISION** to display the current **firmware** revision information. The number and implementation date appear in the active entry area of the display as shown in **10-9** below. The analyzer's serial number and installed options are also displayed. Another way to display the **firmware** revision information is to cycle the line power.

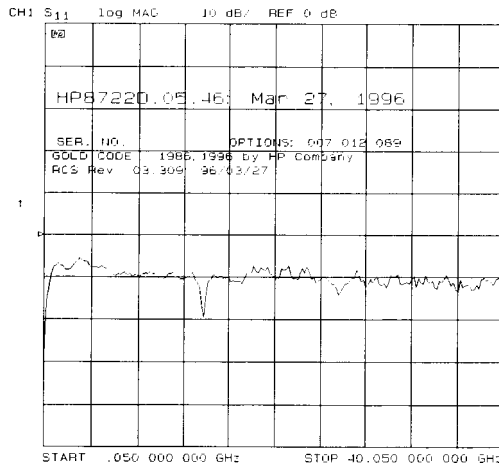


Figure 10-10. Location of Firmware Revision Information on Display

HP-IB Service Mnemonic Definitions

All service routine keystrokes can be made through HP-IB in one of the following approaches:

- sending equivalent remote HP-IB commands (Mnemonics have been documented previously with the corresponding keystroke.)
- invoking the System Menu (**MENUSYST**) and using the analyzer mnemonic (**SOFTn**), where “n” represents the **softkey** number. (Softkeys are numbered 1 to 8 from top to bottom.)

An HP-IB overview is provided in the “Compatible Peripherals” chapter in the *HP 8719D/20D/22D Network Analyzer User’s Guide*. HP-IB programming information is **also** provided in the *HP 8719D/20D/22D Network Analyzer Programmer’s Guide*.

Invoking Tests Remotely

Many tests require a response to the displayed prompts. Since bit 1 of the Event Status Register B is set (bit 1 = service routine waiting) any time a service routine prompts the user for an expected response, you can send an appropriate response using one of the following techniques:

- Read event status register B to reset the bit.
- Enable bit 1 to interrupt (**ESNB[D]**). See “Status Reporting” in the *HP 8719D/20D/22D Network Analyzer Programmer’s Guide*.
- Respond to the prompt with a **TESRn** command (see Tests Menu, at the beginning of this chapter).

Symbol Conventions

- [] An optional operand
- D A numerical operand
- < > A necessary appendage
- | An either/or choice in appendages

Analog Bus Codes

ANAI[D]	Measures and displays the analog input. The preset state input to the analog bus is the rear panel AUX IN. The other 22 nodes may be selected with D only if the ABUS is enabled (ANABon).
OUTPCNTR	Outputs the counter's frequency data.
OUTPERRO	Reads any prompt message sent to the error queue by a service routine.
OUTPTESS	Outputs the integer status of the test most recently executed. Status codes are those listed under "TST?".
TST?	Executes the power-on self test (internal test 1) and outputs an integer test status. Status codes are as follows: 0 = pass 1 = fail 2 = in progress 3 = not available 4 = not done 5 = done

Error Messages

This section contains an alphabetical list of the error messages that pertain to servicing the analyzer. The information in the list includes explanations of the displayed messages and suggestion to help solve the problem.

Note The error messages that pertain to measurement applications are included *in the HP 8719D/20D/22D Network Analyzer User's Guide.*

ADDITIONALSTANDARDSNEEDED

Error Number 68 Error correction for the selected calibration class cannot be computed until you have measured all the necessary standards.

ADDRESSED TO TALK WITH NOTHING TO SAY

Error Number 31 You have sent a read command to the analyzer (such as ENTER 716) without **first** requesting data with an appropriate output command (such as OUTPDATA). The analyzer has no data in the output queue to satisfy the request.

AIR FLOW RESTRICTED: CHECK FAN FILTER

Error Number 20 Something is restricting the air flow into the analyzer. Check for any debris and clean or replace the fan filter.

ANALOG INPUT OVERLOAD

Error Number 60 The power level of the analog input is too high. Reduce the power level of the analog input source.

BATTERY FAILED. STATE MEMORY CLEARED

Error Number 183 The battery protection of the non-volatile CMOS memory has failed. The CMOS memory has been cleared. Refer to the “Assembly Replacement and Post-Repair Procedures” chapter for battery replacement instructions. See the “Preset State and Memory Allocation, ” chapter *in* the **HP 8719D/20D/22D Network Analyzer User’s Guide** for more information about the CMOS memory.

BATTERY LOW! STORE SAVE REGS TO DISK

Error Number 184 The battery protection of the non-volatile CMOS memory is in danger of failing. If this occurs, **all** of the instrument state registers stored in CMOS memory will be lost. Save these states to a disk and refer to the “Assembly Replacement and Post-Repair Procedures” chapter for battery replacement instructions. See the “Preset State and Memory Allocation, ” chapter *in* the **HP 8719D/20D/22D Network Analyzer User’s Guide** for more information about the CMOS memory.

BLOCK INPUT ERROR

Error Number 34 The analyzer did not receive a complete data transmission. This is usually caused by an interruption of the bus transaction. Clear by pressing the **Local** key or aborting the I/O process at the controller.

BLOCK INPUT LENGTH ERROR

Error Number 35 The length of the header received by the analyzer did not agree with the size of the internal array block. Refer to the **HP 8719D/20D/22D Network Analyzer Programmer’s Guide** for instructions on using analyzer input commands.

CALIBRATION ABORTED

Error Number 74 You have changed the active channel during a calibration so the calibration in progress was terminated. Make sure the appropriate channel is active and restart the calibration.

CALIBRATION REQUIRED

Error Number 63 A calibration set could not be found that matched the current stimulus state or measurement parameter. You will have to perform a new calibration.

CANNOT READ/WRITE 1FILESYSTEM

Error Number 203 The disk is being accessed by the analyzer and is found to contain an 1 (hierarchical **file** system) or **files** nested within subdirectories. The analyzer does not support 1. Replace the disk medium with a LIF or DOS formatted disk that does not contain **files** nested within subdirectories.

CAUTION: POWER OUT MAY BE UNLEVELED

Error Number 179 There is either a hardware failure in the source or you have attempted to set the power level too high. The analyzer allows the output power to be set higher or lower than the specified available power range. However, these output powers may be unlevelled or unavailable. Check to see if the power level you set is within specifications. If it is, refer to the *HP 8719D/20D/22D Network Analyzer Service Guide* for troubleshooting.

CORRECTION CONSTANTS NOT STORED

Error Number 3 A store operation to the EEPROM was not successful. You must change the position of the jumper on the **A7** CPU assembly. Refer to the “**A7** CC Jumper Position Procedure” in the “Adjustments and Correction Constants” chapter.

CORRECTION TURNED OFF

Error Number 66 Critical parameters in your current instrument state do not match the parameters for the calibration set, therefore correction has been turned off. The critical instrument state parameters are sweep type, start frequency, frequency span, and number of points

CURRENT PARAMETER NOT IN CAL SET

Error Number 64 Correction is not valid for your selected measurement parameter. Either change the measurement parameters or perform a new calibration.

DEADLOCK

Error Number 111 A fatal firmware error occurred before instrument preset completed.

DEVICE: **not on**, not connect, wrong addr

Error Number 119 The device at the selected address cannot be accessed by the analyzer. Verify that the device is switched on, and check the HP-IB connection between the analyzer and the device. Ensure that the device address recognized by the analyzer matches the HP-IB address set on the device itself.

DISK HARDWARE PROBLEM

Error Number 39 The disk drive is not responding correctly. If using an external disk drive, refer to the disk drive operating manual.

DISK MESSAGE LENGTH ERROR

Error Number 190 The analyzer and the external disk drive aren't communicating properly. Check the HP-IB connection and then try substituting another disk drive to isolate the problem instrument.

DISK: **not on, not connected, wrong addr**

Error Number 38 The disk cannot be accessed by the analyzer. Verify power to the disk drive, and check the HP-IB connection between the analyzer and the disk drive. Ensure that the disk drive address recognized by the analyzer matches the HP-IB address set on the disk drive itself.

DISK READ/WRITE ERROR

Error Number 189 There may be a problem with your disk. Try a new floppy disk. If a new floppy disk does not eliminate the error, suspect hardware problems.

EXT SOURCE NOT READY FOR TRIGGER

Error Number 191 There is a hardware problem with the HP 8625A external source. Verify the connections between the analyzer and the external source. If the connections are correct, refer to the source operating manual.

EXTSRC : NOT ON/CONNECTED OR WRONG ADDR

Error Number 162 The analyzer is unable to communicate with the external source. Check the connections and the HP-IB address on the source.

FILE NOT COMPATIBLE WITH INSTRUMENT

Information Message You cannot recall user graphics that had been saved on an earlier model of analyzer with a monochrome display. These **files** cannot be used with the HP 8719D/20D/22D.

ILLEGAL UNIT OR VOLUME NUMBER

Error Number 46 The disk unit or volume number set in the analyzer is not **valid**. Refer to the disk drive operating manual.

INITIALIZATION FAILED

Error Number 47 The disk initialization failed, probably because the disk is damaged.

INSUFFICIENT MEMORY, PWR MTR CAL OFF

Error Number 154 There is not enough memory space for the power meter calibration array. Increase the available memory by clearing one or more save/recall registers, or by reducing the number of points.

NO CALIBRATION CURRENTLY IN PROGRESS

Error Number 69 The **RESUME CAL SEQUENCE** softkey is not valid unless a calibration is already in progress. Start a new calibration.

NO FAIL FOUND

Service Error Number 114 The self-diagnose function of the instrument operates on an internal test failure. At this time, no failure has been detected.

NOT ENOUGH SPACE ON DISK FOR STORE

Error Number 44 The store operation will overflow the available disk space. Insert a new disk or purge files to create free disk space.

NO FILE(S) FOUND ON DISK

Error Number 45 No **files** of the type created by an analyzer store operation were found on the disk. If you requested a specific file title, that **file** was not found on the disk.

NO IF FOUND: CHECK R INPUT LEVEL

Error Number 5 The **first** IF signal was not detected during pretune. Check the front panel R channel jumper. If there is no visible problem with the jumper, refer to the “Source Troubleshooting” chapter.

PHASE LOCK FAILURE

Error Number 7 The **first** IF signal was detected at pretune, but phase lock could not be acquired. Refer to the “Source Troubleshooting” chapter.

NO SPACE FOR NEW CAL. CLEAR REGISTERS

Error Number 70 You cannot store a calibration set due to insufficient memory. You can free more memory by clearing a saved instrument state from an internal register (which may also delete an associated calibration set, if all the instrument states using the calibration kit have been deleted.) You can store the saved instrument state and calibration set to a disk before clearing them. After deleting the instrument states, press **PRESET** to run the memory packer.

NOT ALLOWED DURING POWER METER CAL

Error Number 198 When the analyzer is performing a power meter calibration, the HP-IB bus is unavailable for other functions such as printing or plotting.

OVERLOAD ON INPUT A, POWER REDUCED

Error Number 58 You have exceeded approximately + 14 **dBm** at one of the test ports. The RF output power is automatically reduced to -85 **dBm**. The annotation **P↓** appears in the left margin of the display to indicate that the power trip function has been activated. When this occurs, reset the power to a lower level, then toggle the **SOURCE PWR on OFF** softkey to switch on the power again.

OVERLOAD ON INPUT B, POWER REDUCED

Error Number 59 You have exceeded approximately + 14 **dBm** at one of the test ports, The RF output power is automatically reduced to -85 **dBm**. The annotation **P↓** appears in the left margin of the display to indicate that the power trip function has been activated. When this occurs, reset the power to a lower level, then toggle the **SOURCE PWR on OFF** softkey to switch on the power again.

OVERLOAD ON INPUT, POWER REDUCED

Error Number 57 You have exceeded approximately + 14 dBm at one of the test ports. The RF output power is automatically reduced to -85 dBm. The annotation P↓ appears in the left margin of the display to indicate that the power trip function has been activated. When this occurs, reset the power to a lower level, then toggle the **SOURCE PWR on OFF** softkey to switch on the power again.

PARALLEL PORT NOT AVAILABLE FOR GPIO

Error Number 165 You have defined the parallel port as COPY for sequencing in the HP-IB menu. To access the parallel port for general purpose I/O (GPIO), set the selection to **PARALLEL [GPIO]**.

PARALLEL PORT NOT AVAILABLE FOR COPY

Error Number 167 You have **defined** the parallel port as general purpose I/O (GPIO) for sequencing. The **definition** was made under the **(LOCAL)** key menus. **To** access the parallel port for copy, set the selection to **PARALLEL [COPY]**.

PHASE LOCK CALFAILED

Error Number 4 An internal phase lock calibration routine is automatically executed at power-on, preset, and any time a loss of phase lock is detected. This message indicates that phase lock calibration was initiated and the **first** IF detected, but a problem prevented the calibration from completing successfully. Refer to Chapter 3, “Adjustments and Correction Constants” and execute pretune correction (test 43). This message may appear if you connect a mixer between the RF output and R input before turning on frequency offset mode. Ignore it: it will go away when you turn on frequency offset. This message may also appear if you turn on frequency offset mode before you **define** the offset.

PHASE LOCK LOST

Error Number 8 Phase lock was acquired but then lost. Refer to the “Source Troubleshooting” chapter.

POSSIBLE FALSE LOCK

Error Number 6 Phase lock has been achieved, but the source may be phase locked to the wrong harmonic of the synthesizer, Perform the source pretune correction routine documented in the “Adjustments and Correction Constants” chapter.

CAUTION: POWER OUT MAY BE UNLEVELED

Error Number 179 There is either a hardware failure in the source or you have attempted to set the power level too high. The analyzer allows the output power to be set higher or lower than the **specified** available power range. However, these output powers may be unlevelled or unavailable. Check to see if the power level you set is within specifications. If it is, refer to the “Source Troubleshooting” chapter.

POWER METER INVALID

Error Number 116 The power meter indicates an out-of-range condition. Check the test setup.

POWER METER NOT SETTLED

Error Number 118 Sequential power meter readings are not consistent. Verify that the equipment is set up correctly. If so, preset the instrument and restart the operation.

PWR MTR : NOT ON/CONNECTED OR WRONG ADDR

Error Number 117 The power meter cannot be accessed by the analyzer. Verify that the power meter address and model number set in the analyzer match the address and model number of the actual power meter.

POWER SUPPLY HOT!

Error Number 21 The temperature sensors on the **A8** post-regulator assembly have detected an over-temperature condition. The power supplies regulated on the post-regulator have been shut down. Refer to the “Power Supply Troubleshooting” chapter.

POWER SUPPLY **SHUT** DOWN!

Error Number 22 One or more supplies on the **A8** post-regulator assembly have been shut down due to an over-current, over-voltage, or under-voltage condition. Refer to the “Power Supply Troubleshooting” chapter.

PRINTER : error

Error Number 175 The parallel port printer is malfunctioning. The analyzer cannot complete the copy function.

PRINTER : not handshaking

Error Number 177 The printer at the parallel port is not responding.

PRINTER:**not on, not connected**, wrong addr

Error Number 24 The printer does not respond to control. Verify power to the printer, and check the HP-IB connection between the analyzer and the printer. Ensure that the printer address recognized by the analyzer matches the HP-IB address set on the printer itself.

SAVE FAILED. INSUFFICIENT MEMORY

Error Number 151 You cannot store an instrument state in an internal register due to insufficient memory. Increase the available memory by clearing one or more save/recall registers and pressing **PRESET**, or by storing files to a disk.

SELF TEST #n FAILED

Service Error Number 112 Internal test #n has failed. Several internal test routines are executed at instrument preset. The analyzer reports the **first** failure detected. Refer to the internal tests and the self-diagnose feature descriptions earlier in this chapter.

SOURCEPOWERTURNEDOFF, RESET UNDER POWER MENU

Information Message You have exceeded the maximum power level at one of the inputs and power has been automatically reduced. The annotation **P↓** indicates that power trip has been activated. When this occurs, reset the power and then press **MENU POWER SOURCE PWR on OFF**, to switch on the power. This message follows error numbers 57, 58, and 59.

SWEEPMODECHANGEDTOCW TIMESWEEP

Error Number 187 If you select external source auto or manual instrument mode and you do not also select CW mode, the analyzer is automatically switched to CW.

SWEEP TIME TOO FAST

Error Number 12 The fractional-N and digital IF circuits have lost synchronization. Refer to the HP *8719D/20D/22D Network Analyzer Service Guide* for troubleshooting information.

TEST ABORTED

Error Number 113 You have prematurely stopped a service test.

TEST PORT OVERLOAD, REDUCE POWER

Error Number 57 You have exceeded approximately + 14 **dBm** at one of the test ports (or 0 **dBm** at the A or B sampler, Option 012 Only). When this occurs, reduce the power to a lower level.

TROUBLE! CHECKSET-UP AND START OVER

Service Error Number 115 Your equipment setup for the adjustment procedure in progress is not correct. Check the setup diagram and instructions in the “Adjustments and Correction Constants” chapter. Start the procedure again.

WRONG DISK FORMAT, INITIALIZE DISK

Error Number 77 You have attempted to store, load, or read **file** titles, but your disk format does not conform to the Logical Interchange Format (**LIF**) or DOS format. You must initialize the disk before reading or writing to it.

Error Terms

The analyzer generates and stores factors in internal arrays when a measurement error-correction (measurement calibration) is performed. These factors are known by the following terms:

- error terms
- E-terms
- measurement calibration coefficients

The analyzer creates error terms by measuring well-defined calibration devices over the frequency range of interest and comparing the measured data with the ideal model for the devices. The differences represent systematic (repeatable) errors of the analyzer system. The resulting calibration coefficients are good representations of the systematic error sources. For details on the various levels of error-correction, refer to the “Optimizing Measurement Results” chapter of the *HP 8719D/20D/22D Network Analyzer User’s Guide*. For details on the theory of error-correction, refer to the “Application and Operation Concepts” chapter of the *HP 8719D/20D/22D Network Analyzer User’s Guide*.

Error Terms Can Also Serve a Diagnostic Purpose

Specific parts of the analyzer and its accessories directly contribute to the magnitude and shape of the error terms. Since we know this correlation and we know what typical error terms look like, we can examine error terms to monitor system performance (preventive maintenance) or to identify faulty components in the system (troubleshooting).

- **Preventive Maintenance:** A stable, repeatable system should generate repeatable error terms over long time intervals, for example, six months. If you make a hardcopy record (print or plot) of the error terms, you can periodically compare current error terms with the record. A sudden shift in error terms reflects a sudden shift in systematic errors, and may indicate the need for further troubleshooting. A long-term trend often reflects drift,

connector and cable wear, or gradual degradation, indicating the need for further investigation and preventive maintenance. Yet, the system may still conform to specifications. The cure is often as simple as cleaning and gaging connectors or inspecting cables.

- **Troubleshooting:** If a subtle failure or mild performance problem is suspected, the magnitude of the error terms should be compared against values generated previously with the same instrument and calibration kit. This comparison will produce the most precise view of the problem.

However, if previously generated values are not available, compare the current values to the typical values listed in **Table 11-2**, and shown graphically on the plots in this chapter. If the magnitude exceeds its limit, inspect the corresponding system component. If the condition causes system verification to fail, replace the component.

Consider the following while troubleshooting:

- All parts of the system, including cables and calibration devices, can contribute to systematic errors and impact the error terms.
- Connectors must be clean, gaged, and within specification for error term analysis to be meaningful.
- Avoid unnecessary **bending** and flexing of the cables following measurement calibration, **minimizing** cable instability errors.
- Use good connection techniques during the measurement calibration. The connector interface must be repeatable. Refer to the “Principles of Microwave Connector Care” section in the “Service Equipment and Analyzer Options” chapter for information on connection techniques and on cleaning and gaging connectors.
- Use error term analysis to troubleshoot minor, subtle performance problems. Refer to the “Start Troubleshooting Here” chapter if a blatant **failure** or gross measurement error is evident.
- It is often worthwhile to perform the procedure twice (using two distinct measurement calibrations) to establish the degree of repeatability. If the results do not seem repeatable, check all connectors and cables.

Measurement Calibration Procedure

1. Refer to the “Measurement Calibration” section in Chapter 2, “System Verification and Performance Tests,” and perform the full **2-port** calibration with the following modifications:
2. For the reflection measurements (short, open, loads), connect the calibration device directly to the test port instead of to a reference test port. Use the female devices for port 1. Adapt the male devices for port 2.
3. For the reflection measurements, use a cable configuration (a single cable or cable pair) that is consistent with the normal use of the system.
4. For the isolation measurement, select from the following two options:
 - If you will be measuring devices with a dynamic range less than 90 dB, press:
OMIT ISOLATION ISOLATION DONE
 - If you will be measuring devices with a dynamic range greater than 90 dB, follow these steps:
 - a. Leave the cables **connected** and connect impedance-matched loads to the test ports (or reference test ports).

Note If you will be measuring highly reflective devices, such as **filters**, use the test device, connected to the reference plane and terminated with a load, for the isolation standard.

- b. Press **(Avg) AVERAGING on AVERAGING FACTOR (16) (x1)** to change the averaging to at least 16.
- c. Press **(Avg) IF BW (10) (x1)** to change the IF bandwidth to 10 Hz.
- d. Press **(Cal) RESUME CAL SEQUENCE ISOLATION DO BOTH FWD + REV .**
- e. Return the averaging to the original state of the measurement, and press **(Cal) RESUME CAL SEQUENCE DONE 2-PORT CAL .**

The following table lists the calibration coefficients along with their corresponding test numbers. You may wish to refer to this table when performing the “Error Term Inspection” procedure.

Table 1 1-1. Calibration Coefficient Terms and Tests

Calibration Coefficient	Calibration Type				Test Number		
	Response	Response and Isolation*	1-port	2-port†			
1	E_R or E_T	E_X (E_D)	E_D	E_{DF}	31		
2				E_T (E_R)	ES	E_{SF}	32
3					E_R	E_{RF}	33
4				E_{XF}	34		
5				E_{LF}	35		
6				E_{TF}	36		
7				E_{DR}	37		
8				E_{SR}	38		
0				E_{RR}	30		
10				E_{XR}	40		
11				E_{LR}	41		
12				E_{TR}	42		
NOTES:							
Meaning of first subscript: D –directivity; S–source match; R–reflection tracking; X –crosstalk; L–load match; T–transmission tracking.							
Meaning of second subscript: F–forward; R–reverse.							
* Response and Isolation cal yields: E_X or E_T if a transmission parameter (S_{21} , S_{12}) or E_D or E_R if a reflection parameter (S_{11} , S_{22})							
† One-path, 2-port cal duplicates arrays 1 to 6 in arrays 7 to 12.							

Error Term Inspection

Note If the correction is not active, press **[Cal] CORRECTION ON**.

1. Press **[System] SERVICE MENU TESTS [31] [x1] EXECUTE TEST**.

The analyzer copies the **first** calibration measurement trace for the selected error term into memory and then displays it. **Table 11-1** lists the test numbers.

2. Press **[Scale Ref]** and adjust the scale and reference to study the error term trace.
3. Press **[Marker Fctn]** and use the marker functions to determine the error term magnitude.
4. Compare the displayed measurement trace to the trace shown in the following “Error Term descriptions” section, and to previously measured data. If data is not available from previous measurements, refer to the typical uncorrected performance specifications listed in **Table 11-2** and **Table 11-3**.
5. Make a hardcopy of the measurement results:
 - a. Connect a printing or plotting peripheral to the analyzer.
 - b. Press **[Local] SYSTEM CONTROLLER SET ADDRESSES** and select the appropriate peripheral to verify that the HP-IB address is set correctly on the analyzer.
 - c. Press **[Save/Recall]** and then **choose** either **PRINT** or **PLOT**.
 - d. Press **[Display] MORE TITLE** and title each data trace so that you can identify it later.

Note For detailed information on creating hardcopies, refer to “Printing, Plotting, and Saving Measurement Results” in the *HP 8719D/20D/22D Network Analyzer User’s Guide*.

6. Repeat steps 1 through 5 for each test number that corresponds to a calibration coefficient (see **Table 11-1**).

If Error Terms Seem Worse than Typical Values

1. Perform a system verification to verify that the system still conforms to specifications.
2. If system verification fails, refer to “Start Troubleshooting Here.”

Uncorrected Performance

The following tables show typical performance without error-correction. RF cables are not used except as noted. Related error terms should be within these values.

Table 11-2.
HP 8719D/8720D Characteristics Without Error-Correction

Parameter & Option	Frequency Range			
	0.05 to 0.5 GHz	0.5 to 2 GHz	2 to 8 GHz	8 to 20 GHz
Directivity ¹	27 dB	27 dB	21 dB	16 dB
Source Match (Standard)	12 dB	12 dB	10 dB	8 dB
Source Match (Option 400)	20 dB	20 dB	12 dB	10 dB
Source Match (Option 007)	16 dB	20 dB	14 dB	11 dB
Source Match (Option 085)	18 dB	18 dB	14 dB	8 dB
Load Match (Standard)	22 dB	20 dB	12 dB	10 dB
Load Match (Option 400)	20 dB	17 dB	12 dB	10 dB
Load Match (Option 007)	26 dB	24 dB	15 dB	12 dB
Load Match (Option 085)	26 dB	24 dB	15 dB	10 dB
Reflection Tracking ²	±3 dB	±3 dB	±3 dB	±3 dB
Transmission Tracking ²	±3 dB	±3 dB	±3 dB	±3 dB
Crosstalk ²	95 dB	95 dB	95 dB	90 dB

¹ Includes effect of HP 85131D cable set on test ports.

² Excludes 0/–5 dB slope, characteristic, in magnitude response from 0.84 to 40 GHz and rolloff below 0.84 GHz, which is characteristically –3 dB at 500 MHz, –15 dB at 100 MHz, and –20 dB at 50 MHz.

Table 11-3.
HP 8722D Characteristics Without Error-Correction

Parameter & option	Frequency Range			
	0.05 to 2 GHz	2 to 8 GHz	8 to 20 GHz	20 to 40 GHz
Directivity	23 dB	21 dB	16 dB	15 dB
Source Match (Standard, Option 400)	17 dB	12 dB	11 dB	7 dB
Source Match (Option 007, Option 085)	20 dB	16 dB	11 dB	8 dB
Load Match ¹ (Standard, Option 400)	18 dB	16 dB	12 dB	10 dB
Load Match (Option 007, Option 085)	21 dB	17 dB	13 dB	10 dB
Reflection Tracking ²	±3 dB	±3 dB	±3 dB	±3 dB
Transmission Tracking ^{1 2}	±3 dB	±3 dB	±3 dB	±3 dB
Crosstalk	95 dB	95 dB	88 dB	85 dB

¹ Measured with RF cables.

² Excludes 0/−5 dB slope, characteristic, in magnitude response from 0.84 to 40 GHz and rolloff below 0.84 GHz, which is characteristically −3 dB at 500 MHz, −15 dB at 100 MHz, and −20 dB at 50 MHz.

Error Term Descriptions

The error term descriptions in this section include the following information:

- significance of each error term
- typical results following a full **2-port** error-correction
- guidelines to interpret each error term

The same description applies to both the forward (**F**) and reverse (**R**) terms. The plots shown with each are typical of a working system following a full **2-port** calibration as performed in “Measurement Calibration Procedure,” above.

It may be helpful to define some of the terms used in the error term descriptions that follow:

- **R signal path:** refers to the reference signal path. It includes the **A58** M/A/D/S, **A64** R sampler, and associated semi-rigid coax cables.
- **A input path:** refers to the port 1 input path and includes the **A58** M/A/D/S, **A69** step attenuator, **S4** transfer switch, **A61** bias tee, **A62** directional coupler, **A65** A sampler, and associated semi-rigid coax cables.
- **B input path:** refers to the port 2 input path and includes the **A58** M/A/D/S, **A69** step attenuator, **S4** transfer switch, **A60** bias tee, **A63** directional coupler, **A66** B sampler, and associated semi-rigid coax cables.

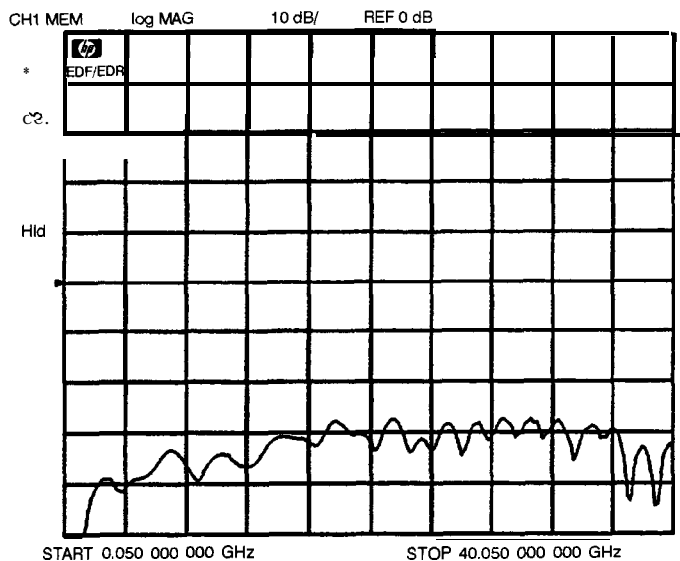
Directivity (EDF and EDR)

These are the uncorrected forward and reverse directivity error terms of the system. The directivity error of the test port is determined by measuring the **S11** and **S22** reflection of the calibration kit load. The load has a much better return loss specification than does the uncorrected test port, therefore any power detected from this measurement is assumed to be due to directivity error.

Significant System Components. The load used in the calibration is the most important component. The test port connector, the cable, and the coupler also greatly affect the measured directivity error.

Affected Measurements. The measurements most affected by directivity errors are measurements of low reflection devices; highly reflective device measurements

will appear normal.



sb6147d

Figure 11-1. Typical **EDF/EDR** Without Cables

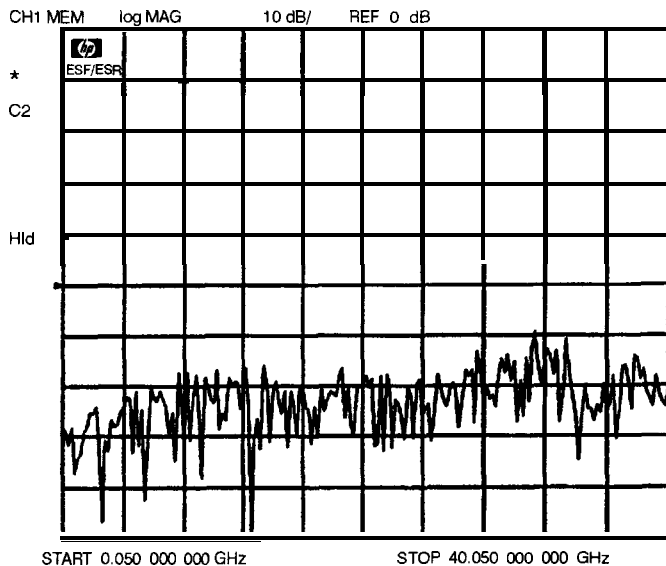
Source Match (ESF and ESR)

Description

These are the forward and reverse uncorrected source match terms of the driven port. They are obtained by measuring the reflection (S_{11} , S_{22}) of an open and then a short connected directly to the ports. Source match is a measure of the match between the coupler and test set connector, as well as the match between all components from the source to the output port.

Significant System Components. The open and short calibration devices are important, as are the coupler and test port connectors. The power splitter, bias tees, step attenuator, and transfer switch may also contribute to source match errors.

Affected Measurements. The measurements most affected by source match errors are reflection and transmission measurements of highly reflective **DUTs**.



sb6148d

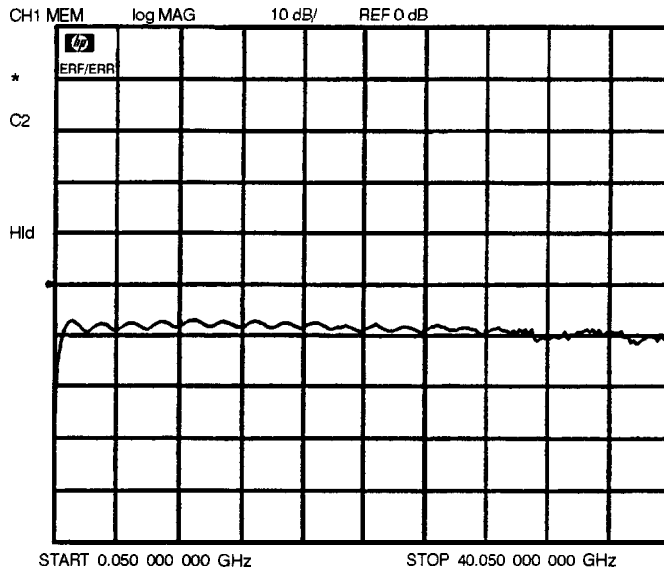
Figure 11-2. Typical ESF/ESR Without Cables

Reflection Tracking (ERF and ERR)

Reflection tracking is the difference between the frequency response of the reference path (R path) and the frequency response of the reflection test path (A or B input path). These error terms are characterized by measuring the reflection (S_{11} , S_{22}) of the open and the short during the measurement calibration. Note that coupler response is included in this error term. Typically this appears as a slope of 0/-5 dB from 0.84 GHz to 40 GHz and a roll-off below 0.84 GHz, which is typically -3 dB at 500 MHz, -15 at 100 MHz, and -20 at 50 MHz.

Significant System Components. The open and short calibration devices have an effect on reflection tracking. But large variations in this error term may indicate a problem in one of the signal paths. Suspect the R signal path if the problem appears in both ERF and ERR. Troubleshoot the A or B input paths **first** if only one reflection tracking term is affected.

Affected Measurements. All reflection measurements (high or low return loss) are affected by the reflection tracking errors.



OPTION 003 ERR APPROXIMATELY 6 dB LOWER

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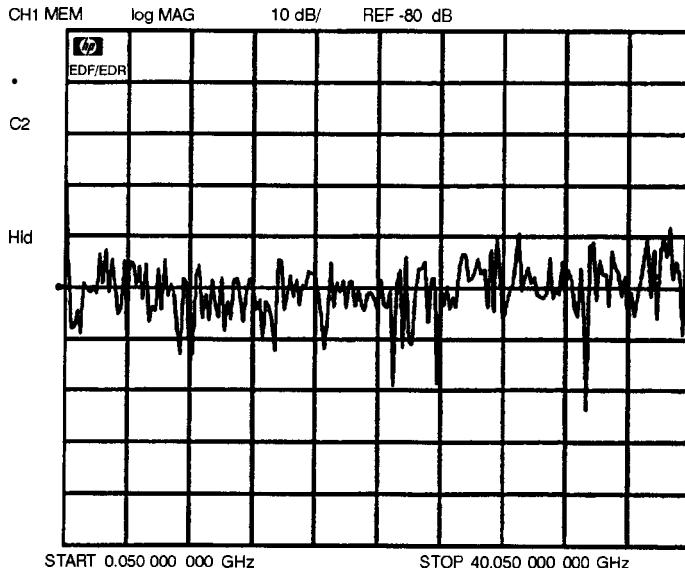
Figure 11-3. Typical **ERF/ERR**

Isolation (Crosstalk, EXF and EXR)

These are the uncorrected forward and reverse isolation error terms that represent leakage between the test ports and the signal paths. The isolation error terms are characterized by measuring transmission (S_{21} , S_{12}) with loads attached to both ports during the measurement calibration. Since these terms are low in magnitude, they are usually noisy (not very repeatable). The error term magnitude changes dramatically with IF bandwidth: a 10 Hz IF bandwidth must be used in order to lower the noise floor beyond the crosstalk specification. Using averaging will also reduce the peak-to-peak noise in this error term.

Significant System Components. Loose cable connections or leakage between components in the lower box are the most likely cause of isolation problems. The transfer switch, bias tees, couplers, and samplers are the most susceptible components.

Affected Measurements. Isolation errors affect both reflection and transmission measurements, primarily where the measured signal level is very low. Examples include reflection measurements of a well-matched DUT, and transmission measurements where the insertion loss of the DUT is large.



sb6150d

Figure 11-4. Typical **EXF/EXR** with 3 kHz Bandwidth

Load Match (ELF and ELR)

Load match is a measure of the impedance match of the test port that terminates the output of a Z-port device. The match of test port cables is included. Load match error terms are characterized by measuring the **S11** and **S22** responses of a “thru” configuration during the calibration procedure.

Significant System Components. Large variations in the forward or reverse load match error terms may indicate a bad “thru” cable or a poor connection of the cable to the test port.

Affected Measurements. The measurements most affected by load match errors are all transmission measurements, and reflection measurements of a low insertion

loss two-port device, such as an airline.

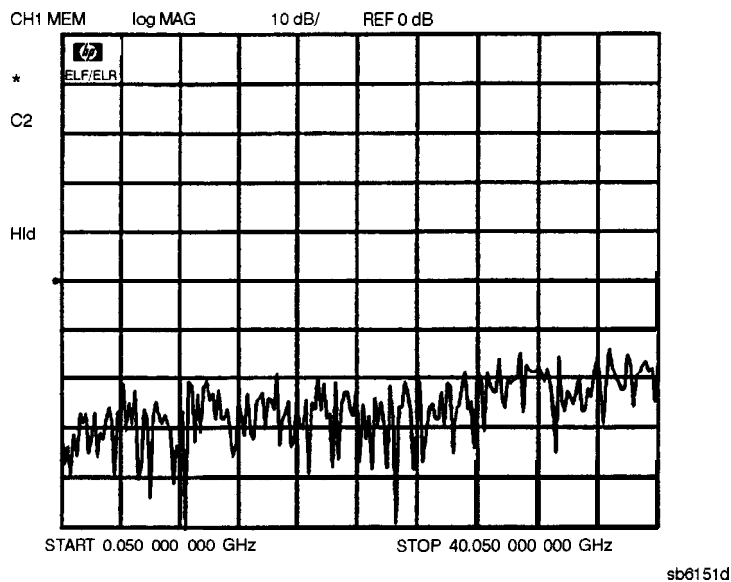


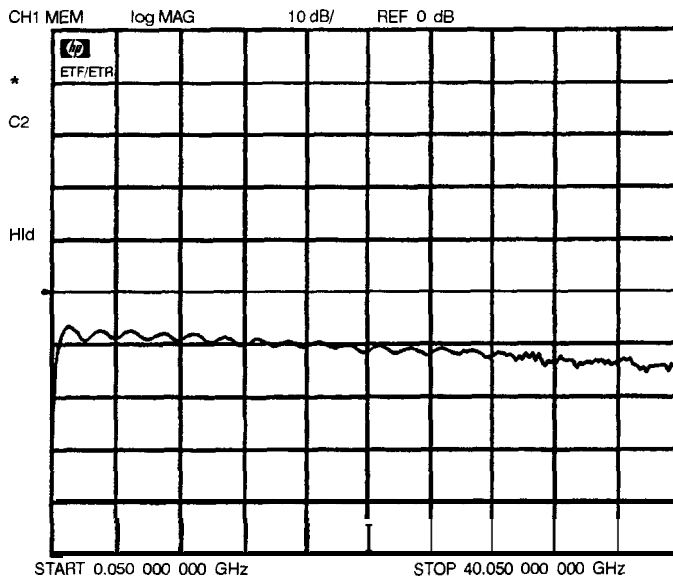
Figure 11-5. Typical **ELF/ELR**

Transmission Tracking (ETF and ETR)

Transmission tracking is the difference between the frequency response of the reference path (including R input) and the frequency response of the transmission test path (including A or B input) while measuring transmission. The response of the test port cables is included. These terms are characterized by measuring the transmission (S_{21} , S_{12}) of the ‘thru’ configuration during the measurement calibration. Note that coupler response is included in this error term. Typically transmission tracking appears as a slope of $0/-5$ dB from 0.84 GHz to 40 GHz and a roll-off below 0.84 GHz, which is typically -3 dB at 500 MHz, -15 at 100 MHz, and -20 at 50 MHz.

Significant System Components. Large variations in this error term probably indicate a problem in the reference signal path (if both ETF and ETR are bad) or in the A or B input path. The ‘thru’ cable also has an effect on transmission tracking.

Affected Measurements. All transmission measurements are affected by transmission tracking errors.



sb6152d

Figure 11-6. Typical ETF/ETR

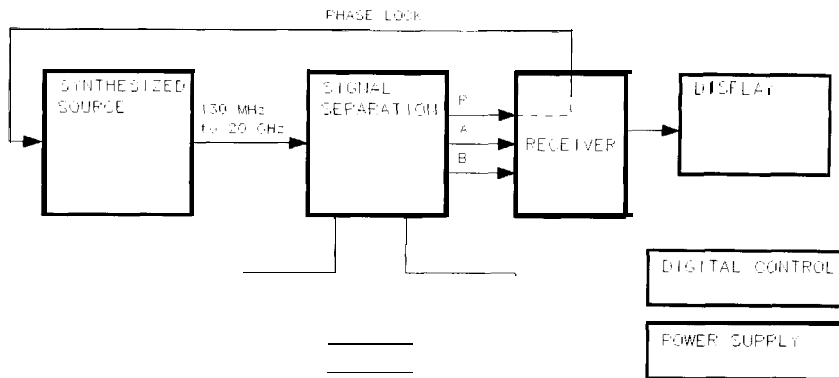
Theory of Operation

Introduction

Theory of Operation provides a general description of the system, and operating theory of the network analyzer functional groups. Operation is explained to the assembly level only: component-level circuit theory is not provided. Simplified block diagrams illustrate the operation of each functional group. An overall block diagram is provided at the end of the section.

System Operation

The HP 8719D/20D/22D microwave network analyzers integrate a synthesized source, signal separation devices, a three-channel receiver for measurement of test device characteristics, and a large-screen display. Figure 12-1 is a simplified block diagram of the network analyzer system.



sb629d

Figure 12-1. Simplified System Block Diagram

The built-in synthesized source of the analyzer generates a swept or CW (continuous wave) signal in the following ranges:

HP 8719D	HP 8720D	HP 8722D
50 MHz to 13.5 GHz	50 MHz to 20 GHz	50 MHz to 40 GHz

The source output power is leveled by an internal ALC (automatic leveling control) circuit, to a maximum level of **+5 dBm** (-10 dBm, HP 8722D) at the front panel measurement ports. A portion of the source signal is routed to the R sampler in the receiver, and fed back to the source for phase lock.

The signal separation devices separate the source signal into a reference path and a test path. They provide attenuation for the source signal, RF path switching to allow forward and reverse measurements, and external connections for the DUT (device under test). The signal transmitted through or reflected from the DUT goes to the receiver for comparison with the reference signal.

The receiver converts the source signal to a 4 **kHz** IF (intermediate frequency) for signal processing, **retaining** both magnitude and phase characteristics. The IF is converted to digital signals, which are processed into magnitude and phase information. The processed and formatted data is finally routed to the display, and to the HP-IB for remote operation.

In addition to the analyzer, the system includes cables for interconnections, and calibration standards for accuracy enhanced measurements.

Functional Groups of the Analyzer

The operation of the analyzer is most logically described in five functional groups. Each group consists of several major assemblies, and performs a distinct function in the instrument. Some assemblies are related to more than one group, and in fact all the groups are to some extent interrelated and affect each other's performance.

Power Supply. The power supply functional group provides power for the other assemblies in the instrument.

Digital Control. The digital control group, which includes the front and rear panels and the display, as well as the CPU, provides control to all assemblies in the network analyzer. The graphics signal processor (GSP) provides an interface between the CPU and the display.

Source. The source group supplies a phase-locked and leveled microwave signal to the device under test.

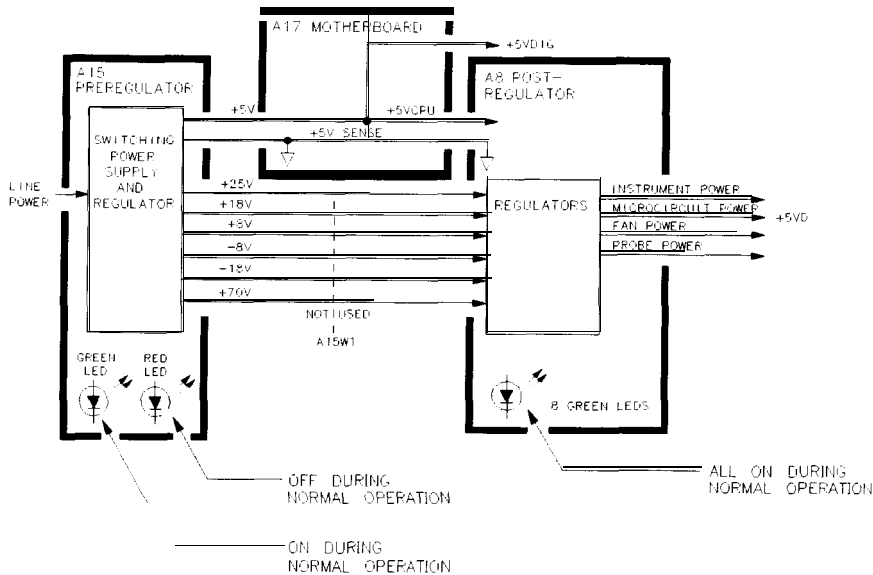
Signal Separation. The signal separation group performs the function of an S-parameter test set, dividing the source signal into a reference path and a test path, and providing connections to the device under test.

Receiver. The receiver group measures and processes the input signals for display.

The following pages describe the operation of the assemblies within each of the functional groups.

Power Supply Theory

The power supply functional group consists of the **A15** preregulator and the **A8** post regulator. These two assemblies comprise a switching power supply that provides regulated DC voltages to power all assemblies in the analyzer. The **A15** preregulator is enclosed in a casting at the rear of the instrument behind the display. It is connected to the **A8** post regulator by a wire bus **A15W1**. Figure 12-2 is a simplified block diagram of the power supply group.



sg6105e

Figure 12-2. Power Supply Functional Group, Simplified Block Diagram

A15 Preregulator

The **A15** preregulator steps down and rectifies the **line** voltage. It provides a fully regulated +5 V digital supply, and several preregulated voltages that go to the **A8** post regulator assembly for additional regulation.

The **A15** preregulator assembly includes the line power module, a 60 kHz switching preregulator, and overvoltage protection for the +5 V digital supply. It provides **LEDs**, visible from the rear of the instrument, to indicate either normal or shutdown status.

Line Power Module

The line power module includes the line power switch, voltage selector switch, and main fuse. The line power switch is activated from the front panel. The voltage selector switch, accessible at the rear panel, adapts the analyzer to local line voltages of approximately 115 V or 230 V (with 350 VA maximum). The main fuse, which protects the input side of the preregulator against drawing too much line current, is also accessible at the rear panel. Refer to the *HP 8719D/20D/22D Network Analyzer Installation and Quick Start Guide* for line voltage tolerances and other power considerations.

Preregulated Voltages

The switching preregulator converts the line voltage to several DC voltages. The regulated +5V digital supply goes directly to the motherboard. The following partially regulated voltages are routed through A15W1 to the A8 post regulator for final regulation:

+70 V +25 V +18 V -18 V +8 V -8 V

Regulated +5 V Digital Supply

The +5 V supply is regulated by the control circuitry in the A15 preregulator. It goes directly to the motherboard, and from there to all assemblies requiring a low noise digital supply. A +5 V sense line returns from the motherboard to the A15 preregulator. The +5 V CPU is derived from the +5 V in the A8 post regulator and goes directly to the A19 graphics system processor.

In order for the preregulator to function, the +5 V digital supply must be loaded by one or more assemblies, and the +5 V sense line must be working. If not, the other preregulated voltages will not be correct.

Shutdown Indications: the Green LED and Red LED

The green LED is on in normal operation. It is off when line power is not connected, not switched on, or set too low, or if the line fuse has blown.

The red LED, which is off in normal operation, lights to indicate a fault in the +5 V supply. This may be an over/under line voltage, over line current, or overtemperature condition. Refer to the troubleshooting chapters for more information.

A8 Post Regulator

The **A8** post regulator filters and regulates the DC voltages received from the **A15** preregulator. It provides fusing and shutdown circuitry for individual voltage supplies. It distributes regulated constant voltages to individual assemblies throughout the instrument. It includes the overtemperature shutdown circuit, the variable fan speed circuit, and the air flow detector. Nine green **LEDs** provide status indications for the individual voltage supplies.

Refer to the Power Supply Block Diagram located at the end of Chapter 5, “Power Supply Troubleshooting”, to see the voltages provided by the **A8** post regulator.

Voltage Indications: the Green **LEDs**

The eight green **LEDs** along the top edge of the **A8** assembly are on in normal operation, to indicate the correct voltage is present in each supply. If they are off or flashing, a problem is indicated. The troubleshooting procedures later in this chapter detail the steps to trace the cause of the problem.

Shutdown Circuit

The shutdown circuit is triggered by overcurrent, overvoltage, undervoltage, or overtemperature. It protects the instrument by causing the regulated voltage supplies to be shut down. It also sends status messages to the **A7** CPU to trigger warning messages on the analyzer display. The voltages that are not shut down are the + **5VD** and + **5VCPU** digital supplies from the preregulator, the fan supplies, and the display supplies. The shutdown circuit can be disabled momentarily for troubleshooting purposes by using a jumper to connect the **SDIS** line (**A8TP4**) to ground.

Variable Fan Circuit and Air Flow Detector

The fan power is derived directly from the + 18 V and -18 V supplies from the **A15** preregulator. The fan is not fused, so that it will continue to provide airflow and cooling when the instrument is otherwise disabled. If overheating occurs, the main instrument supplies are shut down and the fan runs at full speed. An overtemperature status message is sent to the **A7** CPU to initiate a warning message on the analyzer display. The fan also runs at full speed if the air flow detector senses a low output of air from the fan. (Pull speed is normal at initial power on.)

Display Power

The **A8** assembly supplies +5V_{CPU} and +65 V (not used) to the **A22** GSP interface board. The +5V_{CPU} is routed to the **A19** GSP where it is regulated to +3.3 V and sent to the display. The **A19** GSP also controls and supplies power to the **A20** backlight inverter. The voltages generated by the inverter are then routed to the display. Display power is not connected to the protective shutdown circuitry so that the **A18** display assemblies can operate during troubleshooting when other supplies do not work.

Note If blanking pulses from the **A19** GSP are not present, then +3.3 V will not be sent to the display.

Digital Control Theory

The digital control functional group consists of the following assemblies:

- A1 front panel
- A2 front panel processor
- A7 CPU
- A10 digital IF
- A16 rear panel
- A18 display
- A19 GSP
- A20 Inverter

These assemblies combine to provide digital control for the entire analyzer. They provide math processing functions, as well as communications between the analyzer and an external controller and/or peripherals. Figure 6-1 is a block diagram of the digital control functional group.

A1 Front Panel

The A1 front panel assembly provides user interface with the analyzer. It includes the keyboard for local user inputs, and the front panel LEDs that indicate instrument status. The RPG (rotary pulse generator) is not electrically connected to the front panel, but provides user inputs directly to the front panel processor.

A2 Front Panel Processor

The A2 front panel processor detects and decodes user inputs from the front panel and the RPG, and transmits them to the CPU. It has the capability to interrupt the CPU to provide information updates. It controls the front panel LEDs that provide status information to the user.

A7 CPU/A10 Digital IF (firmware revisions 6.xx and below)

The A7 CPU assembly contains the main CPU (central processing unit), the digital signal processor, memory storage, and interconnect port interfaces. The main CPU is the master controller for the analyzer, including the other dedicated microprocessors. The memory includes EEPROM, RAM, EPROM, and ROM.

Data from the receiver is serially clocked into the A7 CPU assembly from the A10 digital IF. The data taking sequence is triggered either from the A14 fractional-N assembly, **externally** from the rear panel, or by software on the A7 assembly.

A7 CPU/A10 Digital IF (firmware revisions 7.xx and above)

The A7 CPU assembly contains the main CPU (central processing **unit**), the digital signal processor, memory storage, and interconnect port interfaces. The main CPU is the master controller for the analyzer, including the other dedicated microprocessors. The memory includes EEPROM, DRAM, flash ROM, SRAM, and boot ROM.

Data from the receiver is serially clocked into the A7 CPU assembly from the A10 digital IF. The data taking sequence is triggered either from the A14 fractional-N assembly, externally from the rear panel, or by software on the A7 assembly.

Main CPU (**firmware** revisions **6.xx** and below)

The main CPU is a **16-bit** microprocessor that maintains digital control over the entire instrument through the instrument bus. The main CPU receives external control information from the front panel or HP-IB, and performs processing and formatting operations on the raw data in the main RAM. It controls the digital signal processor, the front panel processor, the display processor, and the interconnect port interfaces. In addition, when the analyzer is in the system controller mode, the main CPU controls peripheral devices through the peripheral port interfaces.

The main CPU has a dedicated EPROM that contains the operating system for instrument control. **Front** panel settings are stored in CMOS RAM, with a battery providing at least 5 years of backup storage when external power is off.

Main CPU (**firmware** revisions **7.xx** and above)

The main CPU is a **32-bit** microprocessor that maintains digital control over the entire instrument through the instrument bus. The main CPU receives external control information from the front panel or HP-IB, and performs processing and formatting operations on the raw data in the main RAM. It controls the digital signal processor, the front panel processor, the display processor, and the interconnect port interfaces. In addition, when the analyzer is in the system controller mode, the main CPU controls peripheral devices through the peripheral port interfaces.

The main CPU has a dedicated flash ROM that contains the operating system for instrument control. Front panel settings are stored in SRAM, with a battery providing at least 5 years of backup storage when external power is off.

Main RAM

The main RAM (random access memory) is shared memory for the CPU and the digital signal processor. It stores the raw data received from the digital signal processor, while additional calculations are performed on it by the CPU. The CPU reads the resulting formatted data from the main RAM and converts it to GSP commands. It writes these commands to the GSP for output to the analyzer display.

EEPROM

EEPROM (**electrically-erasable** programmable read only memory) contains factory set correction constants unique to each instrument. These constants correct for hardware variations to maintain the highest measurement accuracy.

The correction constants can be updated by executing the routines in Chapter 3, “Adjustments and Correction Constants.”

Digital Signal Processor

The digital signal processor receives the digitized data from the **A10** digital IF. It computes discrete Fourier transforms to extract the complex phase and magnitude data from the 4 **kHz** IF signal. The resulting raw data is written into the main RAM.

A18 Display

The **A18** display is an 8.4 inch LCD with associated drive circuitry. It receives a +3.3 V power supply from the **A19** GSP, along with the voltage generated from the **A20** backlight inverter. It receives the following signals from the **A19** GSP:

- digital **TTL** horizontal sync
- digital **TTL** vertical sync
- blanking
- data clock
- digital **TTL** red video
- digital **TTL** green video
- digital **TTL** blue video

A19 GSP

The **A19** graphics system processor provides an interface between the **A7** CPU and the **A18** display. The CPU (**A7**) converts the formatted data to GSP commands and writes it to the GSP. The GSP processes the data to obtain the necessary video signals and sends the signals to the **A18** display. It **also** produces VGA compatible RGB output signals which are sent to the **A22** GSP interface and then routed to the **A16** rear panel. The assembly receives one power supply voltage from the **A22** GSP interface: +5V_{CPU}, which is used for processing and supplying power to the **A20** backlight inverter and the **A18** display.

A20 Inverter

The **A20** backlight inverter assembly supplies the ac voltage for the backlight tube in the **A18** display assembly. This assembly takes the **+5.16Vdc** from the A1 mother board and converts it to approximately **380 Vac** with 5 ma of current at **40 kHz**. There are two control lines:

- Digital ON/OFF
- Analog Brightness
 - 100% intensity is 0 V
 - 50% intensity is 4.5 V

A16 Rear Panel

The **A16** rear panel includes the following interfaces:

TEST SET I/O INTERCONNECT. This provides control signals and power to operate duplexer test adapters.

EXT REF. This allows for a frequency reference signal input that can phase lock the analyzer to an external frequency standard for increased frequency accuracy.

The analyzer automatically enables the external frequency reference feature when a signal is connected to this input. When the signal is removed, the analyzer automatically switches back to its internal frequency reference.

10 MHZ PRECISION REFERENCE. (Option 1D5) This output is connected to the EXT REF (described above) to improve the frequency accuracy of the analyzer.

AUX INPUT. This allows for a dc or ac voltage input from an external signal source, such as a detector or function generator, which you can then measure, using the S-parameter menu. (You can also use this connector as an analog output in service routines.)

EXT AM. This allows for an external analog signal input that is applied to the ALC circuitry of the analyzer's source. This input analog signal amplitude modulates the RF output signal.

EXT TRIG. This allows connection of an external negative-going **TTL-compatible** signal that will trigger a measurement sweep. The trigger can be set to external through **softkey** functions.

TEST SEQ. This outputs a **TTL** signal that can be programmed in a test sequence to be high or low, or pulse (10 μ seconds) high or low at the end of a sweep for a robotic part handler interface.

LIMIT TEST. This outputs a **TTL** signal of the limit test results as follows:

Pass: **TTL** high

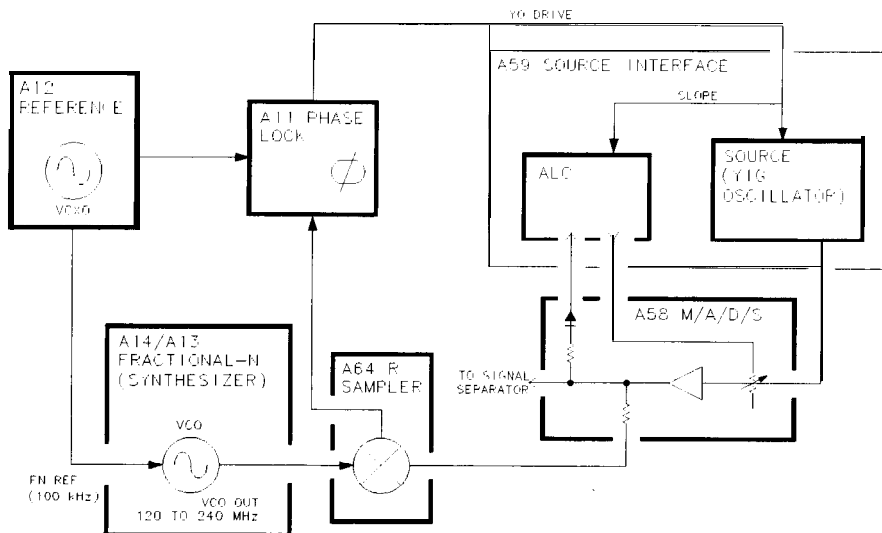
Fail: **TTL** low

VGA OUTPUT. This provides a video output of the analyzer display that is capable of running a PC VGA monitor.

Source Group Theory

The source functional group produces a stable output signal by phase locking a YIG oscillator to a synthesized VCO (voltage controlled oscillator). The full frequency range of the source is generated in subsweeps by harmonic mixing.

The output is a swept or CW signal with a maximum leveled power of + 5 **dBm** (-10 **dBm**, HP 8722D) at the front panel measurement ports (minimum -65 **dBm**). **Figure 12-3** illustrates the operation of the source functional group.



sb621d

Figure 12-3. Source Functional Group, Simplified Block Diagram

The **subsweep** sequence takes place in the following steps. The paragraphs below describe the details of this process, and provide additional information on the assemblies in the source group.

1. The source is pretuned low. The source signal (SOURCE OUT) is fed to the R sampler.
2. A signal (VCO OUT) is generated by the VCO in the fractional-N synthesizer.
3. A comb of harmonics (**1st LO**) is produced in the pulse generator.
4. A synthesizer harmonic (**1st LO**) and the source signal (SOURCE OUT) are mixed in the sampler. A difference frequency (**1st IF**) is generated.
5. The **1st IF** signal from the R sampler is fed back and compared to a reference. A tune current is generated.
6. The tune current is used to set the frequency of the source YIG oscillator.
7. Phase lock is acquired and a synthesized **subsweep** is generated. The source tracks the synthesizer.

Source Pretune

The pretune DAC (digital-to-analog converter) in the All phase lock assembly sets the source YIG oscillator frequency to approximately 2.4 GHz. This signal (SOURCE OUT) goes to the R sampler assembly.

A14/A13 Fractional-N Synthesizer

The A14/A13 fractional-N assemblies comprise the synthesizer. The source feedback circuit phase locks the YIG oscillator to the synthesizer output signal as explained below under “All Phase Lock: Comparing Phase and Frequency. ”

The VCO in the A14 fractional-N (digital) assembly generates a swept or CW signal in the range of 60 to 240 MHz, such that a harmonic is 10 MHz above the desired start frequency. This is divided down and phase locked (in the A13 assembly) to a 100 kHz signal FN REF from the A12 reference. A programmable divider is set to some number, N, such that the integer part of the expression $FVCOM$ is equal to 100 kHz. To achieve frequencies between integer multiples of the reference, the divider is programmed to divide by N part of the time and by N + 1 part of the time. The ratio of the divisions yields an average equal to the desired fractional frequency. API (analog phase interpolator) current sources in the A13 assembly correct for phase errors caused by the averaging. The resulting synthesized signal goes to the pulse generator.

A52 Pulse Generator: the Harmonic Comb

The signal from the synthesizer drives a step recovery diode (SRD) in the A52 pulse generator assembly. The SRD generates a comb of harmonic multiples (1st LO) of the VCO frequency, which goes to the samplers. One of the harmonics is 10 MHz above the desired start frequency.

A64 R Sampler: Down-Converting the Signals

The A64 assembly is part of the receiver functional group. It is also included here because it is an integral part of the source phase locking scheme. In the R sampler, the 1st LO signal from the pulse generator is mixed with the SOURCE OUT signal from the source. The difference IF (intermediate frequency) produced is nominally 10 MHz. For phase locking, part of this IF signal is routed back to the All phase lock assembly. (Additional information on the sampler assemblies is provided in “Receiver Theory. ”)

A11 Phase Lock: Comparing Phase and Frequency

The 10 MHz **1st IF signal** from the **A64** sampler is fed back to the All phase lock assembly. In All it is amplified, limited, and filtered to produce a 10 MHz square wave. This is divided down to 1 MHz, then applied to a phase/frequency detector that compares it to a crystal controlled 1 MHz signal (**PL REF**) from the **A12** reference assembly (see “**A12 Reference: the Crystal Reference Frequencies,**” below). Any phase or frequency difference between these two signals produces a proportional DC voltage.

Tuning the YIG Oscillator

The output of the phase/frequency detector is filtered to remove any 1 MHz feedthrough, and fed to an integrator. The output of the integrator is converted to a tune current. This brings the appropriate **YIG** oscillator closer to the desired frequency, which in turn reduces the phase/frequency detector output voltage. When the voltage is reduced to zero, and the divided-down **1st IF** frequency is equal to the 1 MHz reference frequency **PL REF**, phase lock is achieved.

Phase Locked Sweep

When the source is phase locked to the synthesizer at the start frequency, the synthesizer starts to sweep. The phase-locked loop forces the source to track the synthesizer, maintaining a constant 10 MHz **1st IF** signal.

The full sweep is generated in a series of subsweeps, by phase locking the source signal to the harmonic multiples of the synthesizer. At the transitions between subsweeps, phase lock is broken, the source is held at this frequency. **Table 12-1** lists the **sub sweep** frequencies from the synthesizer and the source.

Table 12- 1. Sub sweep Frequencies

Band	Synthesizer (MHz)	Harmonic Number (N)	Source (MHz) Frequency
Low	60 - 120	1	50 - 110
	120 - 240	1	110 - 230
	120 - 240	2	230 - 470
	160 - 236	3	470 - 698
	141.6 - 236	5	698 - 1170
	147.5 - 236	8	1170 - 1878
	157.3 - 213.3	12	1878 - 2550
High Mid (HP 8722D)	128 - 236	20	2550 - 4710
	131.1 - 220/6	36	4710 - 8256
	142.5 - 234	58	8256 - 13562
	159.7 - 235.4	85	13562 - 20000
High (HP 8722D)	178.7 - 223.3	112	20000 - 25000
	148.9 - 238.2	168	25000 - 40000

A12 Reference: the Crystal Reference Frequencies

This assembly provides stable reference frequencies to the rest of the instrument by dividing down the output of a 40 MHz VCXO (voltage-controlled crystal oscillator). One of the divided-down signals is the 100 kHz FN REF for phase locking the synthesizer signal in **A13**. Another is the 1 MHz main phase-locked loop reference signal PL REF that goes to the phase comparator in **A11**. (The **2nd** LO signal and the timing signal for the **A10** digital IF assembly are explained in “Receiver Theory.”) The EXT REF rear panel input provides the option of using an external reference with a frequency of 1, 2, 5, or 10 MHz, instead of the internal 40 MHz VCXO.

Source Block: The YIG Oscillator Signals

The source block includes two **YIG** oscillators and a 3.8 **GHz** **fixed** oscillator. The outputs of these oscillators produce the source signal. In phase-locked operation, this signal tracks the stable output of the synthesizer. Figure 12-4 illustrates the assemblies in the source block.

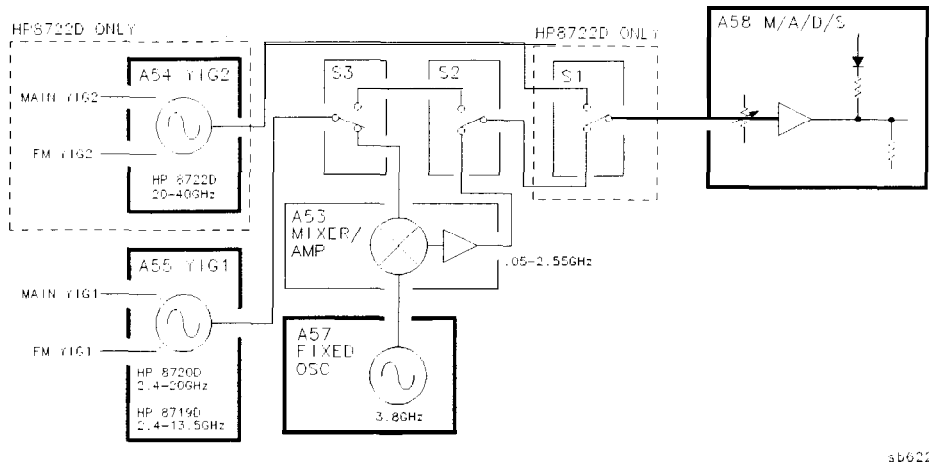


Figure 12-4. Simplified **Diagram** of the Source Block

The YIG oscillator has a main coil and an FM coil. These are analogous to the woofer and the tweeter in a stereo speaker: the woofer reproduces low frequencies and the tweeter reproduces high frequencies. Similarly in the YIG oscillator, the main coil allows large, slow changes in frequency but cannot respond to high frequency deviations, which are sent to the faster-acting FM coils.

The tune current from the All phase lock assembly splits into two paths. One path is **lowpass filtered**, removing high frequency components, and goes to the YIG main coil; the other path is **highpass** filtered, removing low frequency components, and goes to the YIG FM coils. The filters are matched in stop-band response, such that one picks up where the other leaves off.

The full YIG oscillator frequency range is achieved in two bands:

Band	Frequency Range
Low	50 MHz to 2.55 GHz
High	2.55 GHz to 20.0 GHz
Mid (HP 8722D)	
High (HP 8722D)	20 GHz to 40 GHz

In the low band, the 2.4 to 20 GHz output of YIG1 and the fixed 3.8 GHz output of the A57 fixed oscillator are mixed in the A53 mixer/amplifier assembly. In this band, S2 and S3 switch A53 into the circuit.

The high band (mid band, HP 8722D) uses the output of YIG1.

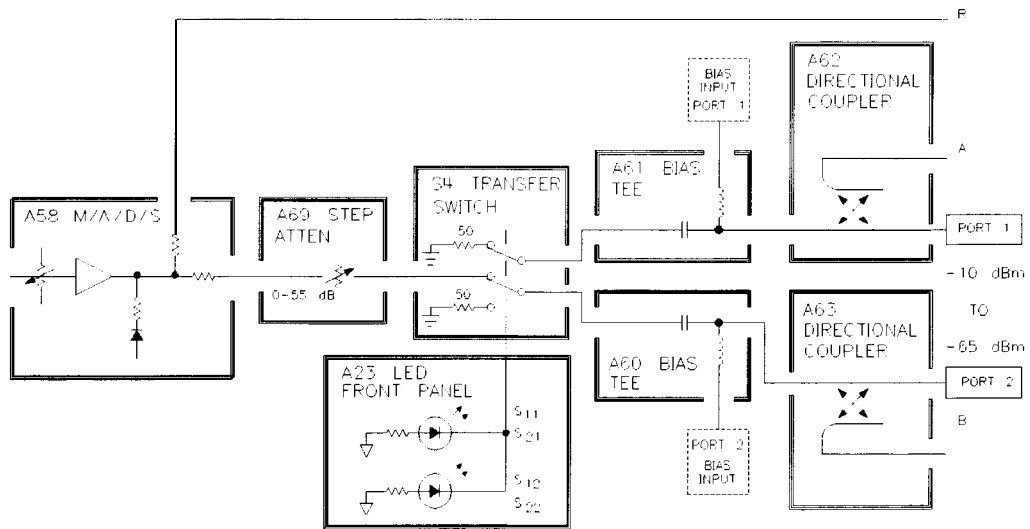
The high band (HP 8722D) uses the output of YIG2.

In the A58 M/A/D/S microcircuit, the YIG oscillator signal is modulated by the ALC OUT signal (explained below) to provide power control and leveling.

ALC: Automatic Leveling Control

A portion of the source output is detected in the M/A/D/S and sent back to the source Interface Board ALC circuit. This circuit generates a control signal which is sent to the modulator in the M/A/D/S to control the power. The tune voltage from the main coil drive is used to change the source amplitude as a function of frequency, thus compensating the source for losses in the transfer switch, bias tees, and couplers.

Signal Separation



sb623d

Figure 12-5. Signal Separation, Simplified Block Diagram

A58 M/A/D/S Modulator, Amplifier, Detector, Splitter

The M/A/D/S microcircuit accomplishes four separate functions:

The modulator controls the output power proportionally to the signal produced by the ALC circuit on the source Interface board.

The amplifier provides up to + 30 dB of amplification that will allow up to + 5 dBm (-10 dBm, HP 8722D) to be output from the test port.

The detector outputs a voltage that is proportional to the RF power out of the amplifier. This voltage is used by the ALC circuit on the source Interface board.

The power source divides the source signal into two parts. One signal is routed directly to the A64 R sampler and the other is sent through the A69 step attenuator, S4 transfer switch, A60 and A61 bias tees, A62/A63 directional couplers and to the test ports.

The M/A/D/S microcircuit is controlled by the ALC circuitry on the source interface board. The CPU provides fine control of the test port power for applications such as power sweep.

Option 400 A58 M/A/D, and A74 Switch Splitter

The M/A/D (Modulator/Amplifier/Detector) microcircuit accomplishes three functions:

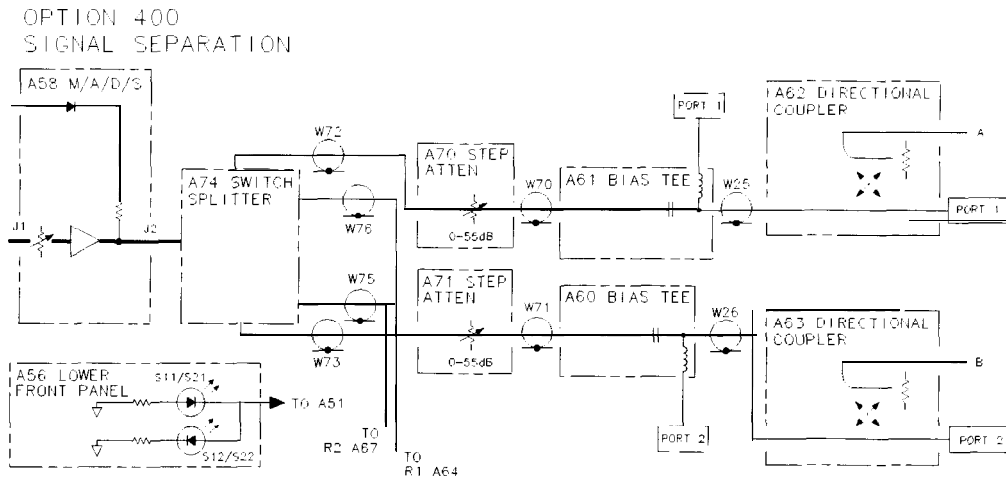
The modulator controls the output power proportionally to the signal produced by the **ALC** circuit on the source interface board.

The amplifier can provide **+30 dB** of amplification for test port output power levels up to **+5 dBm** for HP 8719D/20D (**-10 dBm** for HP 8722D).

The detector outputs a voltage that is proportional to the RF power out of the amplifier. The voltage is used by the **ALC** circuit **on**the source interface board.

The switch splitter (**A74**) divides three inputs:

- a path routed directly to **A64 (R1 sampler)**
- a path routed directly to the **A67 (R2 sampler)**
- a path switched to the appropriate output port (through **A70/71** step attenuators, **A60/61** bias tees, and **A62/63** directional couplers)



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Figure 12-6. Option 400 Signal Separation

A69 Step Attenuator

The step attenuator provides coarse power control for the source signal. It is an electro-mechanical attenuator, controlled by the **A7 CPU**, that provides 0 to 55 **dB** of attenuation in 5 **dB** steps. It adjusts the power level to the DUT without changing the level of the incident power in the reference path.

S4 Transfer Switch

The output of the step attenuator is fed into the **S4** transfer switch. This is a solid-state switch. It switches between the port 1 and port 2 measurement paths, automatically enabling alternate forward and reverse measurements. In addition, **S4** provides an internal termination for the measurement port that is inactive.

A56 Lower Front Panel Assembly

LEDs on the lower front panel indicate the status of the transfer switch.

A60 and A61 DC Bias Tees

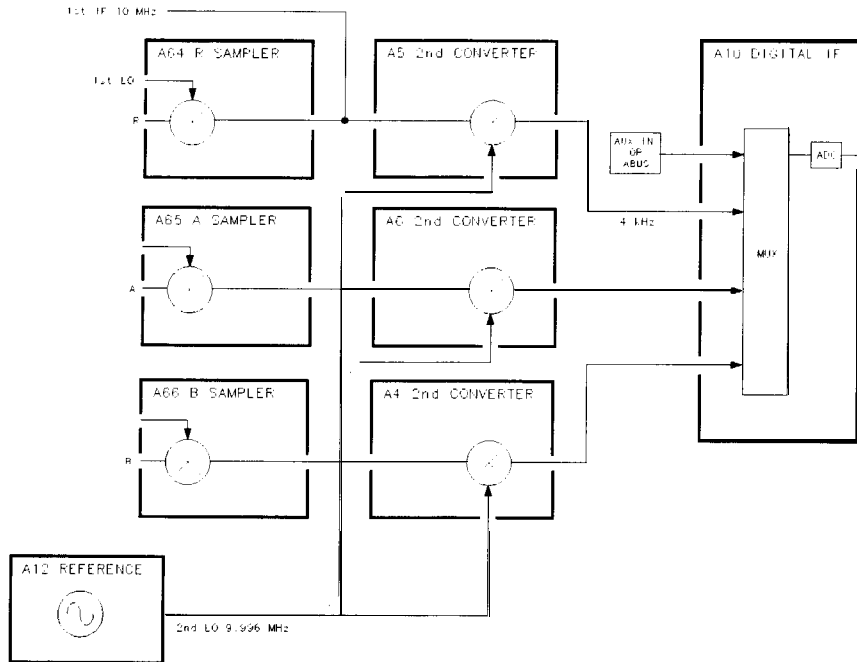
The DC bias tees provide a means of biasing active devices with an external DC voltage connected to the rear panel DC BIAS CONNECT ports. The DC voltage is applied directly to the center conductor of the test port connectors. A blocking capacitor ensures that the bias current goes only to the device under test, and not back into the source. Likewise, an inductor in the bias path prevents RF from being imposed on the external DC supply.

A62 and A63 Directional Couplers

The test signal goes into the through-line arm of the couplers, and from there to the test ports and the device under test. The coupled arm of the couplers carries the signal reflected from or transmitted through the device under test to the receiver for measurement. The coupling coefficient of the directional couplers is nominally 20 **dB** (40 **dB** at 50 MHz).

Receiver Theory

The receiver measures and processes the input signals into digital information for display. Figure 12-7 is a simplified block diagram of the receiver functional group. The **A12** reference assembly, which is part of the source group, is also included in the illustration to show how the **2nd LO** signal is derived.



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Figure 12-7. Receiver Functional Group, **Simplified** Block Diagram

Samplers and Second Converters

Each input signal goes to one of three identical pairs of sampler and second converter assemblies (R, A, and B) that down-convert the signals to a **fixed 4 kHz 2nd IF** with magnitude and phase corresponding to the input.

The **1st LO Signal** is a comb of harmonics of the synthesizer signal, produced by a step recovery diode in the **A52** pulse generator. Refer to “Source Group Theory” for details.

A64/A65/A66 (A67 Option 400) Samplers. The signal from the source is mixed with the **1st** LO harmonics in the samplers. One of the harmonic signals is 10 MHz above the desired frequency. The mixing products are **filtered**, leaving only the difference between that harmonic and the source frequency: this fixed 10 MHz signal is the **1st** IF ($F_{IF} = N \times F_{VCO} - F_s$, where N is the harmonic number). Part of the **1st** IF signal from the R sampler is fed back to the All phase lock assembly to complete the source phase-locked loop. The **1st** IF from all three samplers goes to the corresponding second converters. The **A67** sampler is only used in Option 400 instruments.

2nd LO Signal. The stable **2nd** LO signal is produced in the **A12** reference assembly by phase locking and mixing a 39.984 MHz VCO with the 40 MHz VCXO to derive a difference of 16 kHz. This is compared to a 16 kHz reference produced by dividing 40 MHz by 2500. The phase-locked output of the 39.984 MHz oscillator is divided by 4 to provide the 9.996 MHz **2nd** LO.

A4/A5/A6 Second Converters. The **1st** IF and the **2nd** LO are mixed in the second converter. The resulting difference frequency is a constant 4 kHz **2nd** IF signal that retains the amplitude and phase characteristics of the measured signal. The **2nd** IF signals from all three second converter assemblies are input to the **A10** digital IF assembly.

A10 Digital IF

In this assembly, the **2nd** IF signals from the A and B second converters go through a gain stage. Signals lower than -30 dB on these two signal paths are amplified by 24 dB to ensure that they can be detected by the ADC (analog-to-digital converter). For troubleshooting purposes, the gain can be forced on or off using the service menus (refer to “Receiver Troubleshooting”). The R path signal is **fixed** at a level high enough to maintain phase lock, and therefore requires no amplification.

All three signals are sampled at a 16 kHz rate set by a divided-down 4 MHz clock pulse from the **A12** reference assembly. The signals are sequentially multiplexed into the ADC, where they are converted to digital form. The ADC conversions are triggered by timing signals from the CPU or the synthesizer, or an external signal at the rear panel EXT TRIG connector. The digitized data is serially clocked into the **A7** CPU assembly to be processed into magnitude and phase data.

The processed and formatted data is **finally** routed to the display, and to the HP-IB for remote operation. Refer to “Digital Control Theory” in this section and to Data Processing in the **first** chapter of the Reference for more information on signal processing.

An additional input to the **A10** assembly is the analog bus (**ABUS**), a built-in service tool for testing analog circuits within the instrument. This is a single multiplexed line that networks analog nodes throughout the instrument, or monitors an external input at the rear panel AUX INPUT connector. It is controlled by the CPU, and used like an oscilloscope or frequency counter to make internal voltage and frequency measurements.

Replaceable Parts

This chapter contains information for ordering replacement parts for the HP 8719D/8720D/8722D network analyzer. Replaceable parts include the following:

- major assemblies
- cables
- hardware

In general, parts of major assemblies are not listed. Refer to **Table 13-2** at the back of this chapter to help interpret part descriptions in the replaceable parts lists that follow.

Replacing an assembly

The following steps show the sequence to replace an assembly in an HP 8719D/8720D/8722D network analyzer.

1. Identify the faulty group. Refer to Chapter 4, “Start Troubleshooting Here.” Follow up with the appropriate troubleshooting chapter that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, “Replaceable Parts.”
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, “Assembly Replacement and Post-Repair Procedures.”
4. Perform the necessary adjustments. Refer to Chapter 3, “Adjustments and Correction Constants. ”
5. Perform the necessary performance tests. Refer to Chapter 2, “System Verification and Performance Tests. ”

Rebuilt-Exchange Assemblies

Under the rebuilt-exchange assembly program, certain factory-repaired and tested modules (assemblies) are available on a trade-in basis. These assemblies are offered for lower cost than a new assembly, but meet **all** factory specifications required of a new assembly.

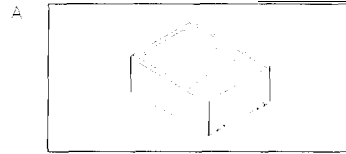
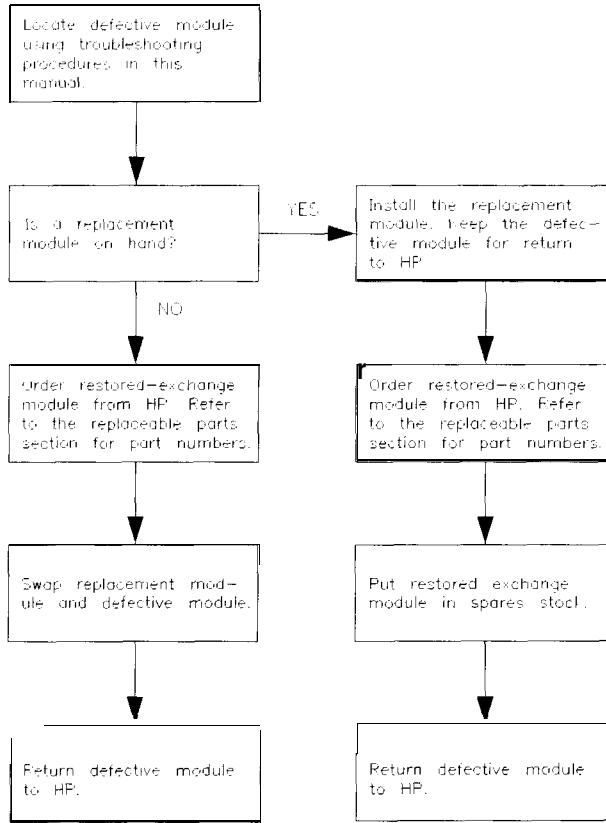
The defective assembly must be returned for credit under the terms of the rebuilt-exchange assembly program. Any spare assembly stock desired should be ordered using the new assembly part number. Figure 13-1 illustrates the module exchange procedure. “Major Assemblies, **Top**” and “Major Assemblies, **Bottom**” list all major assemblies, including those that can be replaced on an exchange basis.

Ordering Information

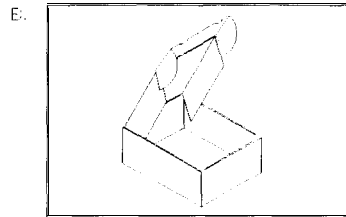
To order a part listed in the replaceable parts lists, quote the Hewlett-Packard part number, indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The Hewlett-Packard Sales and Service Offices table is located in Chapter 15.

To order a part that is not listed in the replaceable parts lists, include the instrument model number, complete instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

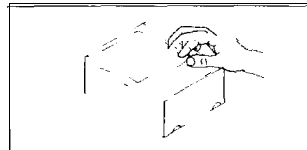
The module exchange program described here is a fast, efficient, economical method of keeping your Hewlett-Packard instrument in service.



Restored-exchange modules are shipped individually in boxes like this. In addition to the circuit module, the box contains:
Exchange assembly failure report
Return address label



Open box carefully—it will be used to return defective module to HP. Complete failure report. Place it and defective module in box. Be sure to remove enclosed return address label.



Seal box with tape. Inside U.S.A.*, stick preprinted return address label over label already on box, and return box to HP. Outside U.S.A., do not use address label; instead address box to the nearest HP office.

*HP pays postage on boxes mailed in U.S.A.

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Figure 13-1. Module Exchange Procedure

Replaceable Part Listings

The following pages list the replacement part numbers and descriptions for the HP 8719D/8720D/8722D Network Analyzer. Illustrations with reference designators are provided to help identify and locate the part needed. The parts lists are organized into the following categories:

- Major Assemblies, **Top**
- Major Assemblies, Bottom
- Cables, **Top**
- Cables, Bottom
- Cables, Front
- Cables, Rear
- Front Panel, Outside
- Front Panel, Inside
- Rear Panel
- Rear Panel, Option 1D5
- Hardware, **Top**
- Hardware, Bottom
- Hardware, Front
- Hardware, Preregulator
- Chassis Parts, Outside
- Chassis Parts, Inside
- Miscellaneous

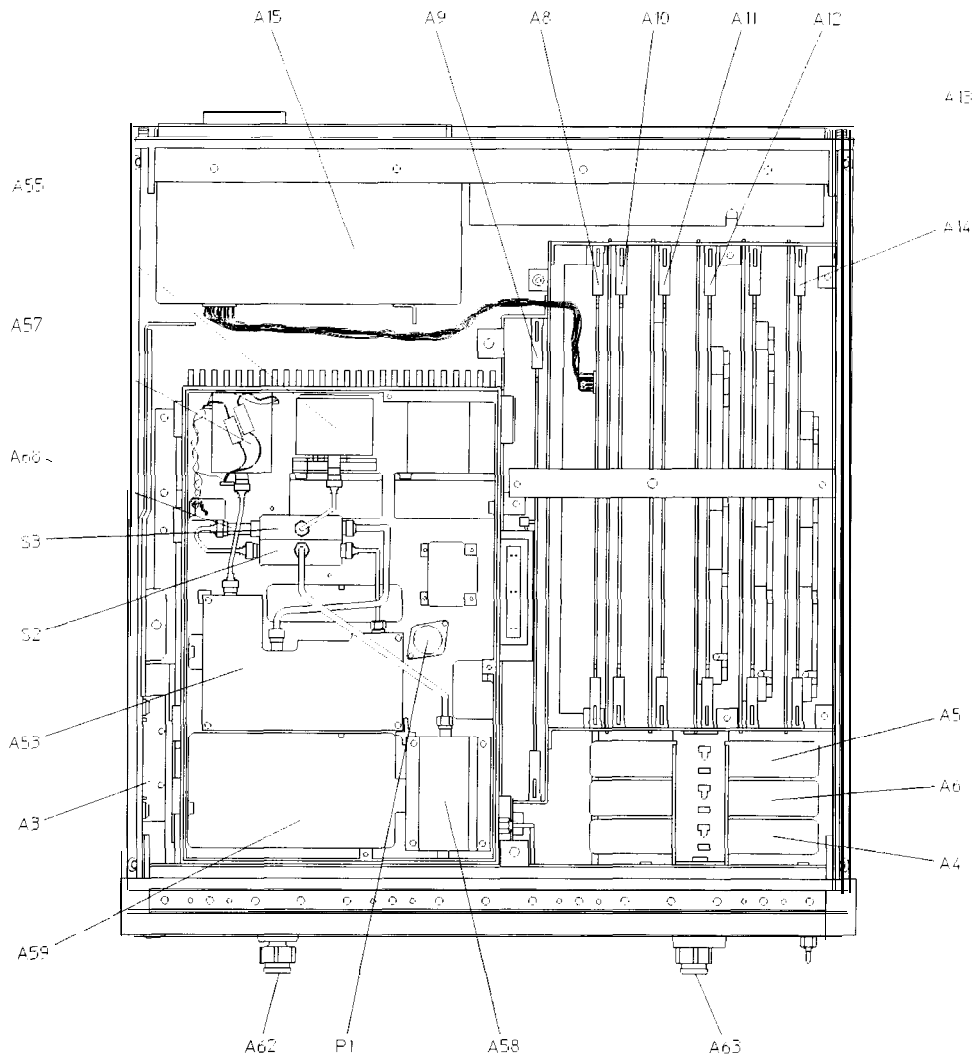
Major Assemblies, **Top**

Ref. Desig.	Option	HP Part Number	Qty	Description
A1				NOT SHOWN (see "Front Panel Assembly, Inside")
A2				NOT SHOWN (see "Front Panel Assembly, Inside")
A3		08720-60190	1	DISK DRIVE ASSY
A4, A5, A6		08720-60156	1	ASSY-SECOND CONVERTER
A7				NOT SHOWN (see "Major Assemblies, Bottom")
A8*		08722-60011	1	BD ASSY-POST REGULATOR (8719D/8720D)
A8*		08722-69011	1	BD ASSY-POST REGULATOR (REBUILT-EXCHANGE) (8719D/8720D)
A8*		08722-60011	1	BD ASSY-POST REGULATOR (8722D)
A9		08720-60129	1	BD ASSY-SOURCE CONTROL
A10		08763-60095	1	BD ASSY-DIGITAL IF
A10		08763-69095	1	BD ASSY-DIGITAL IF (REBUILT-EXCHANGE)
A11		08720-60181	1	BD ASSY-PHASE LOCK
A12		08720-60252	1	BD AMY-REFERENCE
A12		08720-69252	1	BD ASSY-REFERENCE (REBUILT-EXCHANGE)
A13		08720-60049	1	BD ASSY-FRAC N ANALOG
A13		08720-69049	1	BD ASSY-FRAC N ANALOG (REBUILT-EXCHANGE)
A14		08720-60179	1	BD ASSY-FRAC N DIGITAL
A14		08720-69179	1	BD ASSY-FRAC N DIGITAL (REBUILT-EXCHANGE)
A15		08763-60098	1	ASSY-PREREGULATOR
A15		08763-69098	1	ASSY-PREREGULATOR (REBUILT-EXCHANGE)
A16				NOT SHOWN (see "Rear Panel Assembly")
A17				NOT SHOWN (see "Chassis Parts, Inside")
A18				NOT SHOWN (see "Front Panel Assembly, Inside")
A19				NOT SHOWN (see "Cables, Front")
A20				NOT SHOWN (see "Front Panel Assembly, Inside")
A22				NOT SHOWN (see "Cables, Front")
A26	1D5			NOT SHOWN (see "Rear Panel Assembly, Option 1D5")
A51				NOT SHOWN (see "Major Assemblies, Bottom")
A53		5086-7583	1	ASSY-LOW BAND
A53		5086-6583	1	ASSY-LOW BAND (REBUILT-EXCHANGE)
A54		08722-60013	1	ASSY-YIG OSCILLATOR 20 GHZ TO 40 GHZ (8722D)
A55		08720-60082	1	ASSY-YIG OSCILLATOR 2.4 GHZ TO 20 GHZ (8720D/8722D)
A55		08719-60009	1	ASSY-YIG OSCILLATOR 2.4 GHZ TO 13.6 GHZ (8719D)

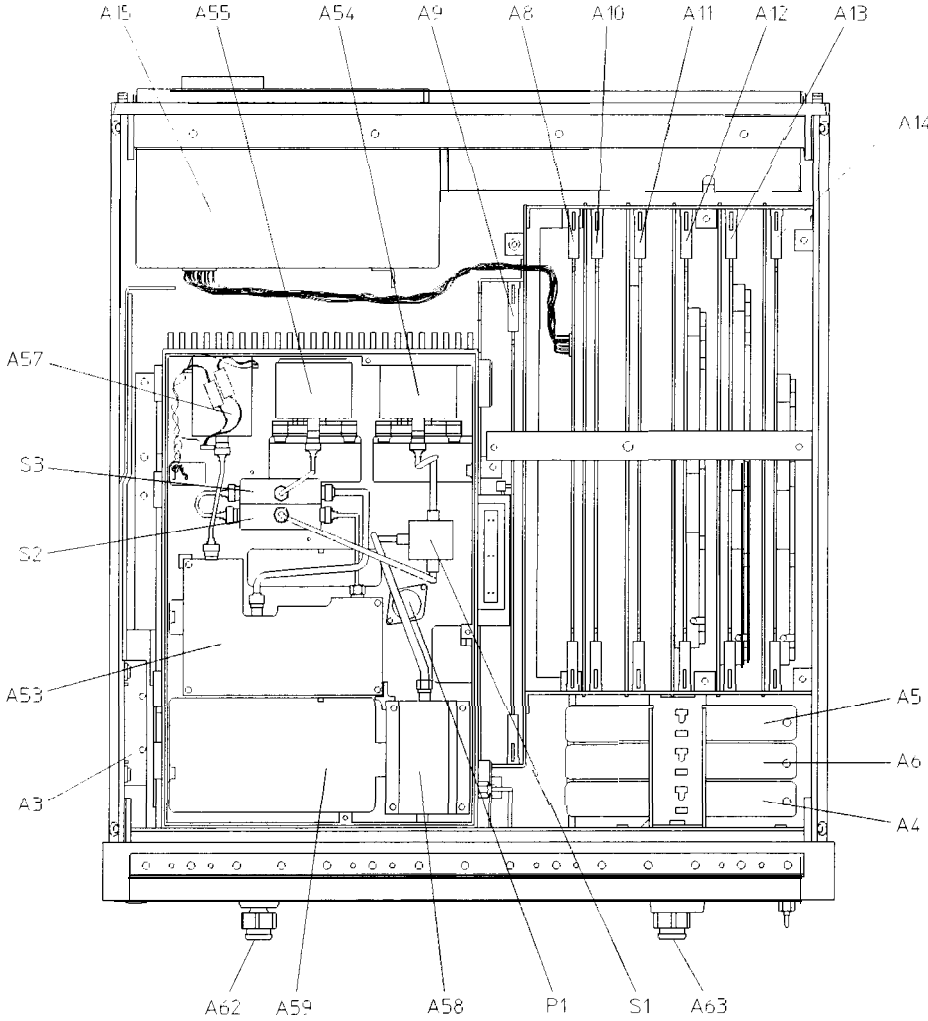
Ref. Desig.	option	HP Part Number	Qty	Description
A56				NOT SHOWN (see 'Cables, Front')
A57		08720-60073	1	ASSY-FIXED OSCILLATOR
A58		5086-7519	1	ASSY-M/A/D/S (8719D/8720D)
A58		5086-6519	1	ASSY-M/A/D/S (8719D/8720D) (REBUILT-EXCHANGE)
A58	004	5086-7974	1	ASSY-M/A/D2 (8719D/8720D)
A58	004	5086-6974	1	ASSY-M/A/D/S2 (8719D/8720D) (REBUILT-EXCHANGE)
A58		5086-7615	1	ASSY-SUPER M/A/D/S (8722D)
A58		5086-7615	1	ASSY-SUPER M/A/D/S (8722D) (REBUILT-EXCHANGE)
A58	400	5086-7980	1	ASSY-M/A/D/S2 (8722D)
A58	400	5086-6980	1	ASSY-M/A/D/S2 (8722D) (REBUILT-EXCHANGE)
A59		08720-60139	1	BD ASSY-SOURCE INTERFACE
A62, 63		5086-7968	2	ASSY-DIRECTIONAL COUPLER (8719D/8720D)
A62, 63		5086-7518	2	ASSY-DIRECTIONAL COUPLER (8722D)
A68		0955-0462	1	ATTENUATOR 6 DB (8719D/8720D)
A72, A73				NOT SHOWN (see 'Cables, Front')
A75				NOT SHOWN (see 'Cables, Front')
A76				NOT SHOWN (see 'Cables, Front')
P1		1826-0423	1	IC-VOLTAGE REGULATOR
S1		5086-7589	1	ASSY-SWITCH 40 GHZ (8722D)
S2,S3		08415-60057	1	ASSY-MICROWAVE SWITCH

* For fuse part numbers on the A8 Post Regulator refer to Table 13-1 in this chapter.

Major HP 8719D/20D Assemblies, Top



Major HP 8722D Assemblies, Top



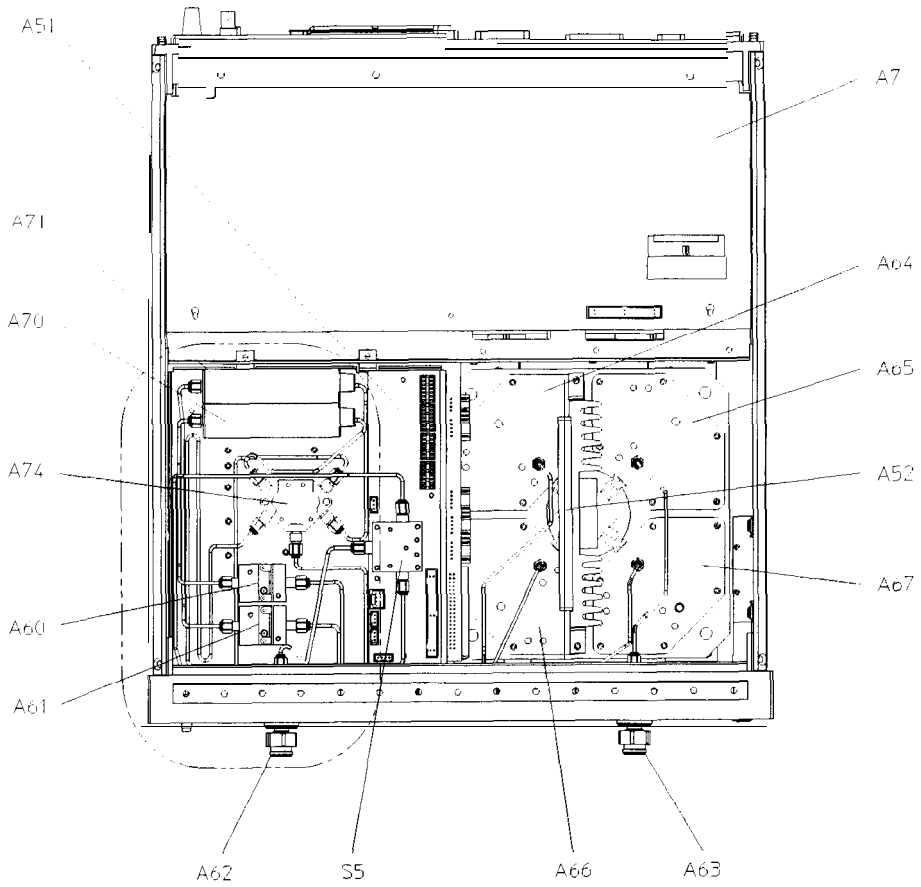
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Major Assemblies, Bottom

Major Assemblies, Bottom

Ref. Desig.	option	HP Part Number	Qty	Description
A7		08720-60140	1	BD ASSY-CPU (F/W REV 6.XX AND BELOW)
A7		08720-60253	1	CPU REPAIR KIT (F/W REV 7.XX AND ABOVE)
A7		08720-69263	1	CPU REPAIR KIT (F/W REV 7.XX AND ABOVE) (REBUILT-EXCHANGE)
A7BT1		1420-0338	1	BATTERY-LITHIUM 3 v 1.2AH
A51		08720-60137	1	BD ASSY-TEST INTERFACE
A51	400	08720-60178	1	BD ASSY-TEST INTERFACE
A52		5086-7456	1	ASSY-PULSE GENERATOR
A52		6086-6466	1	ASSY-PULSE GENERATOR (REBUILT-EXCHANGE)
A60,61		5086-7458	1	BIAS TEE (8719D/8720D)
A60,61		5086-6458	1	BIAS TEE (8719D/8720D) (REBUILT-EXCHANGE)
A60,61		5086-7484	1	BIAS TEE (8722D)
A60,61		5086-6484	1	BIAS TEE (8722D) (REBUILT-EXCHANGE)
A62,63		5086-7968	2	ASSY-DIRECTIONAL COUPLER (8719D/8720D)
A62,63		5086-6968	2	ASSY-DIRECTIONAL COUPLER (8719D/8720D) (REBUILT-EXCHANGE)
A62,63		5086-7518	2	ASSY-DIRECTIONAL COUPLER (8722D)
A62,63		5086-6518	2	ASSY-DIRECTIONAL COUPLER (8722D) (REBUILT-EXCHANGE)
A64,A65, A66,A67		5086-7614	1	ASSY-SAMPLER
A64,A65, A66,A67		5086-6614	1	ASSY-SAMPLER (REBUILT-EXCHANGE)
A69	ALL BUT 085,400	33321-60050	1	ATTENUATOR 0-55 DB
A69	085,400	33326-60006	1	ATTENUATOR 0-55 DB
A70,A71, A75,A76		33326-60006	1	ATTENUATOR 0-55 DB
A74	400,089	5086-7975	1	ASSY-SWITCH SPLITTER (8719D/8720D)
474	400,089	5086-6975	1	ASSY-SWITCH SPLITTER (8719D/8720D) (REBUILT-EXCHANGE)
A74	400,089	5087-7002	1	ASSY-SWITCH SPLITTER (8722D)
A74	400,089	5087-6002	1	ASSY-SWITCH SPLITTER (8722D) (REBUILT-EXCHANGE)
34		5086-7642	1	ASSY-TRANSFER SWITCH SOLID STATE (8719D/8720D)
34	007	08720-60006	1	ASSY-TRANSFER SWITCH (8719D/8720D)
34	007	08722-60015	1	ASSY-TRANSFER SWITCH (8722D)
34	007	08722-69015	1	ASSY-TRANSFER SWITCH (8722D) (REBUILT-EXCHANGE)
34		85831-60033	1	ASSY-TRANSFER SWITCH (8722D)
36	089	5086-7689	1	SWITCH

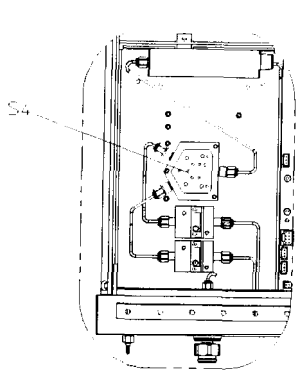
Major Assemblies, Bottom



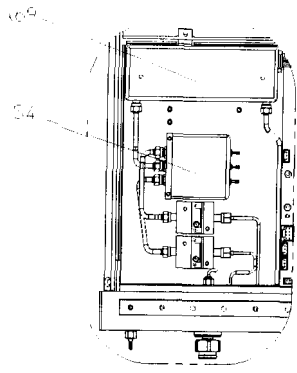
HP 8722D OPTIONS 400, 089
HP 8719D/20D OPTIONS 400, 089

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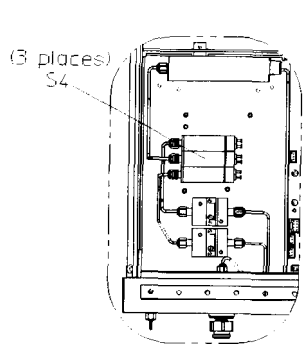
Major Assemblies, Bottom



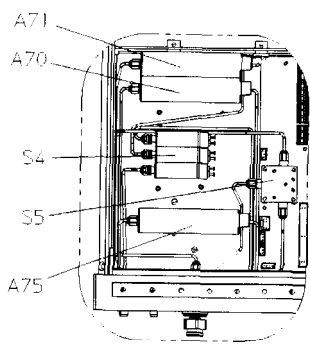
HP 8722D
STANDARD



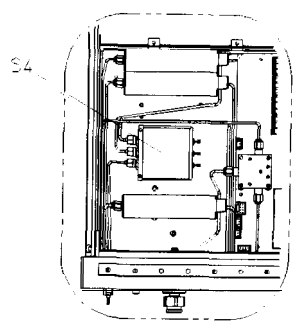
HP 8719D/20D
STANDARD OPTION 007



HP 8722D
OPTION 007



HP 8722D
OPTIONS 085, 089



HP 8719D/20D
OPTIONS 085, 089

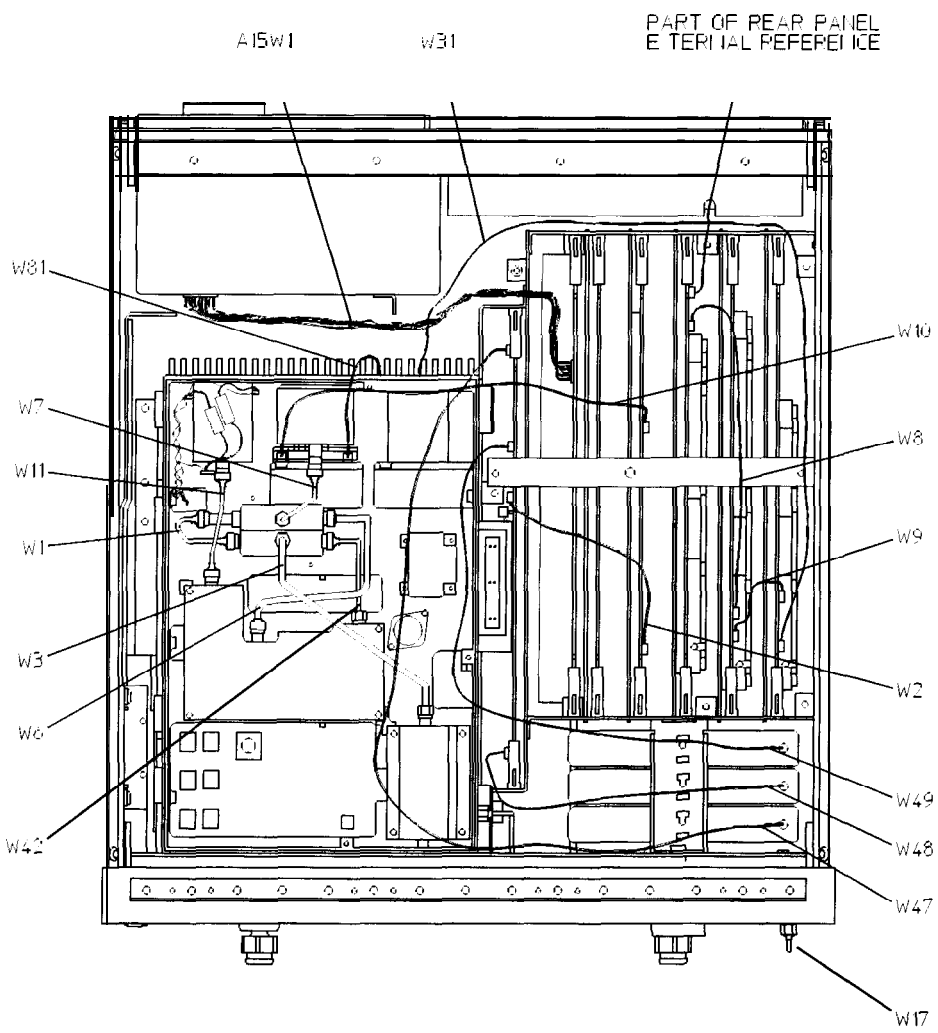
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Cables, Top

Ref. Desig.	Type*	Opt	HP Part Number	Qty	Description
A15W1	18W		(part of A15)	1	A15 to A8 and A17
W1	SR		08720-20064	1	S2 TO A68 (8719D/8720D)
W1	SR		08720-20014	1	S2 TO S3 (8722D)
W2	F		08720-60141	1	A9J3 TO A11J1
W3	SR		08720-20062	1	A58 TO S2 (8719D/8720D)
W3	SR		08720-20015	1	S2 TO S1 (8722D)
W5	SR		08722-20017	1	S1 TO A58 (8722D)
W6	SR		08720-20068	1	A53 TO S3
W7	SR		08720-20063	1	A55 TO S3
W8	F		08415-60040	1	A12 TO A13
w9	F		08415-60041	1	A14 TO A13
W10	F		08415-60031	1	A55 TO A11
W11	SR		08720-20065	1	A57 TO A53
W31	F		08415-60035	1	A52 TO A14
W42	SR		08720-20061	1	A53 TO S2
W43	SR		08722-20016	1	A54 TO S1 (8722D)
W47	F		08720-60132	1	A9J1 TO A4
W48	F		08720-60134	1	A9J2 TO A6
W49	F		08720-60133	1	A9J5 TO A5
W79	F		08514-60033	1	A11J3 TO A54J2 (8722D)
W80	F		08720-60131	1	A17J15 TO A54 (8722D)
W81	F		08720-60144	1	A17J15 TO A55

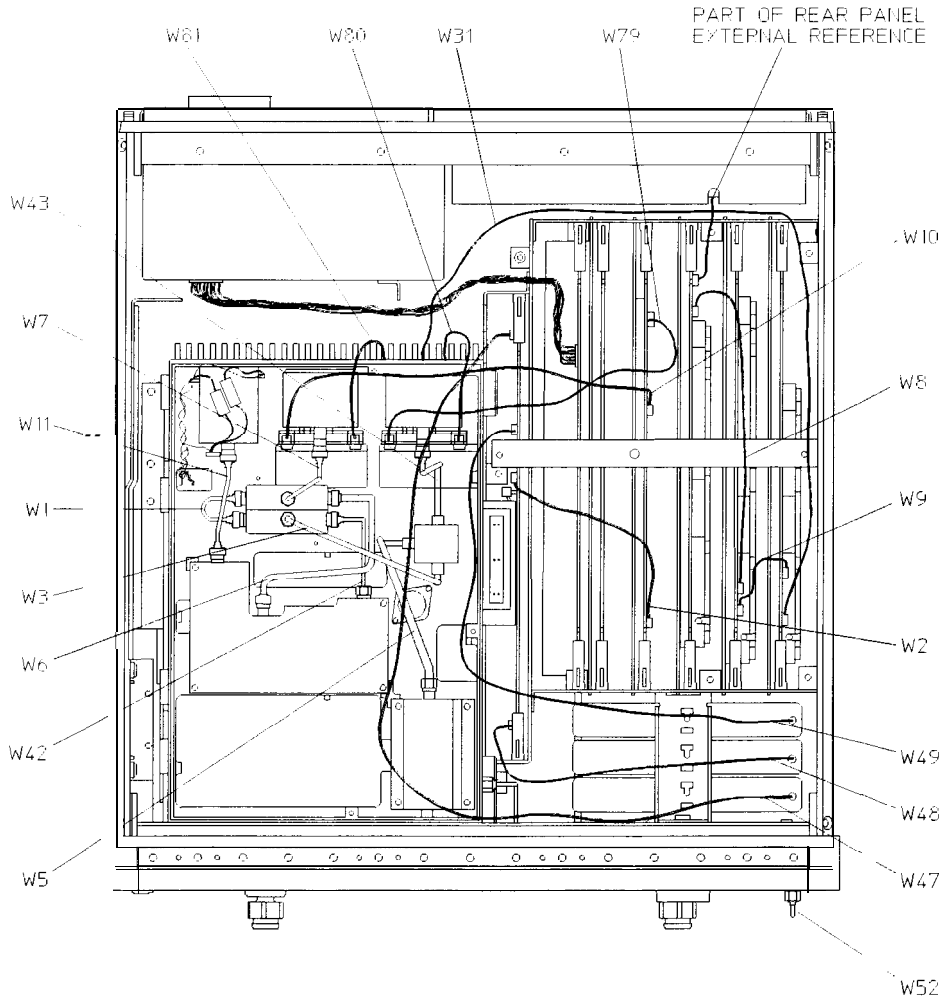
- * **nW** Wire Bundle (*n* is the number of wires in the bundle)
F Flexible Coax Cable
SR Semi-Rigid Coax Cable

HP 8719D/20D Cables, Top



sbc74d

HP 8722D Cables, Top



sb6111d

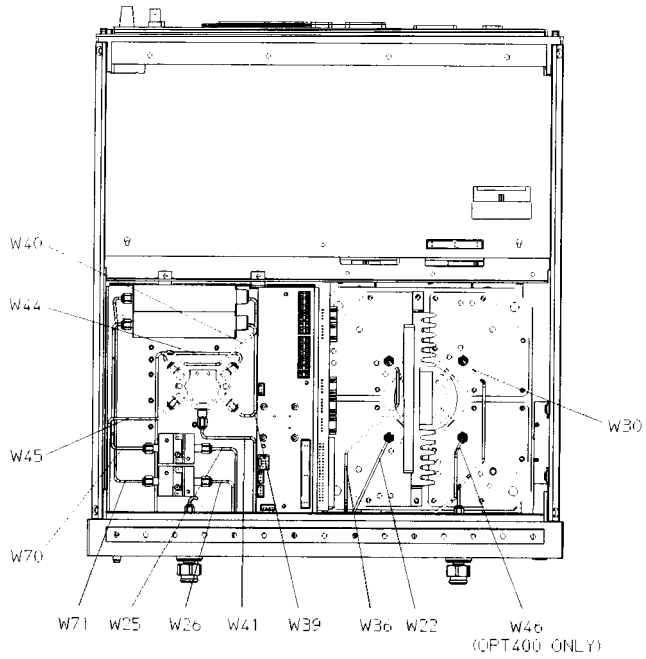
Cables, Bottom

Ref. Desig.	Type	Opt	HP Part Number	Qty	Description
W17	SR	085,089	08720-20150	1	S5 TO FRONT PANEL R CHANNEL IN (8719D/8720D)
W17	SR	085,089	08722-20058	1	S5 TO FRONT PANEL R CHANNEL IN (8722D)
W19	SR	085,089	08722-20058	1	S5 TO A58 (8722D)
W19	SR	400	08720-20174	1	A74 TO A55 (8719D/20D)
W19	SR	400	08722-20064	1	A74 TO A55 (8722D)
W20	SR	089	08720-20134	1	S5 TO A74
W20	SR	085	08720-20147	1	S5 TO A74
W20	SR	400	08720-20134	1	A75 TO A55 (8719D/20D)
W20	SR	400	08722-20134	1	A75 TO A55 (8722D)
W22	SR		08720-20026	1	A63 TO A66
W24	SR	007	08722-20076	1	S4 TO A69 (8722D)
W25	SR		08720-20249	1	A60 TO A62 (8719D/8720D)
W25	SR		08722-20056	1	A60 TO A62 (8722D)
W26	SR		08720-20025	1	A61 TO A63 (8719D/8720D)
W26	SR		08722-20057	1	A61 TO A63 (8722D)
W27	SR		08720-20248	1	S4 TO A60 (8719D/8720D)
W27	SR		08722-20073	1	S4 TO A60 (8722D)
W27	SR	007	08722-20077	1	S4 TO A60 (8722D)
W28	SR		08720-20011	1	S4 TO A61 (8719D/8720D)
W28	SR		08722-20074	1	S4 TO A61 (8722D)
W28	SR	007	08722-20078	1	S4 TO A61 (8722D)
W29	SR		08720-20009	1	S4 TO A69 (8719D/8720D)
W29	SR		08722-20072	1	S4 TO A69 (8722D)
W29	SR	007	08722-20076	1	S4 TO A69 (8722D)
W30	SR		08720-20033	1	A62 TO A65
W32	SR	3TD,012, 007,089	08720-20021	1	A58 TO A69 (8719D/8720D)
W32	SR	085,089	08720-20146	1	A58 TO A69 (8719D/8720D)
W32	SR	3TD,012, 007,089	08722-20069	1	A58 TO A69 (8722D)
W32	SR	085	08722-20086	1	A58 TO A69 (8722D)
W32	SR	400	08720-20073	1	A58 TO A74 (8719D/8720D)
W32	SR	400	08722-20054	1	A58 TO A74 (8722D)

Ref. Desig.	Type*	Opt	HP Part Number	Qty	Description
W36	SR		08720-20041	1	A72 TO A64
W39	SR		08720-20169	1	A74 TO A70 (8719D/8720D)
W39	SR		08722-20063	1	A74 TO A70 (8722D)
W40	SR		08720-20168	1	A74 TO A71 (8719D/8720D)
W40	SR		08722-20062	1	A74 TO A71 (8722D)
W41	SR		08720-20173	1	A74 TO A58 (8719D/8720D)
W41	SR		08722-20054	1	A74 TO A58 (8722D)
W44	SR	400	08720-20171	1	A74 TO A76 (8719D/8720D)
W44	SR	400	08722-20055	1	A74 TO A76 (8722D)
W45	SR		08720-20174	1	A74 TO S5 (8719D/8720D)
W45	SR		08722-20064	1	A74 TO S5 (8722D)
W46	SR		08720-20103	1	A67 TO A73
W52	SR	TD, 012, 085	08720-20075	1	JUMPER (8719D/8720D)
W52	SR		08722-20024	1	JUMPER (8722D)
W58	SR	085	08720-20135	1	A69 TO REAR PANEL SOURCE OUT (8719D/8720D)
W58	SR	085	08722-20085	1	A69 TO REAR PANEL SOURCE OUT (8722D)
W59	SR	085	08720-20144	1	S4 TO REAR PANEL SOURCE IN (8719D/8720D)
W59	SR	085	08722-20084	1	S4 TO REAR PANEL SOURCE IN (8722D)
W60	SR	085	08720-20159	1	S4 TO PORT 2 SWITCH (8719D/8720D)
W60	SR	085	08722-20097	1	S4 TO PORT 2 SWITCH (8722D)
W64	SR	085	08720-20143	1	A62 TO A70
W65	SR	085	08720-20158	1	A65 TO A70
W66	SR	085	08720-20157	1	A66 TO A71
W67	SR	085	08720-20142	1	A63 TO A71
W70	SR	400	08720-20145	1	A60 TO A75 (8719D/8720D)
W70	SR	400	08722-20061	1	A60 TO A75 (8722D)
W71	SR	400	08720-20136	1	A61 TO A76 (8719D/8720D)
W71	SR	400	08722-20059	1	A61 TO A76 (8722D)

* SR Semi-Rigid Coax Cable

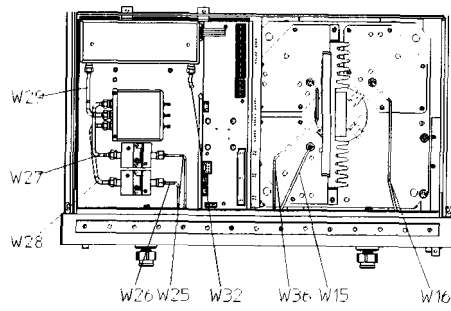
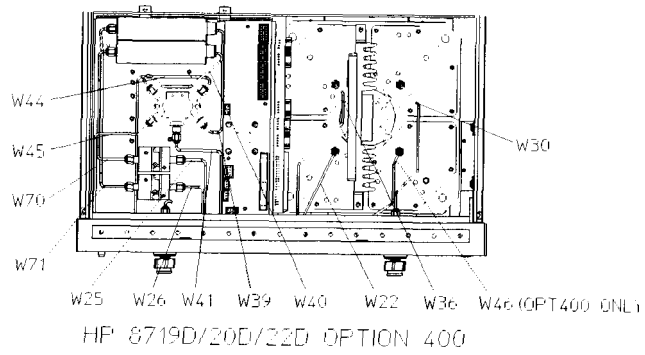
Cables, Bottom



HP 8719D/20D/22D OPTION 400

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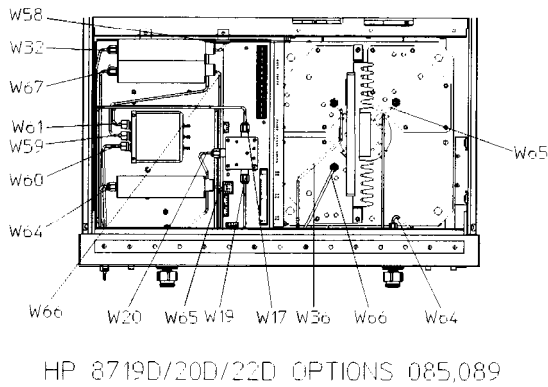
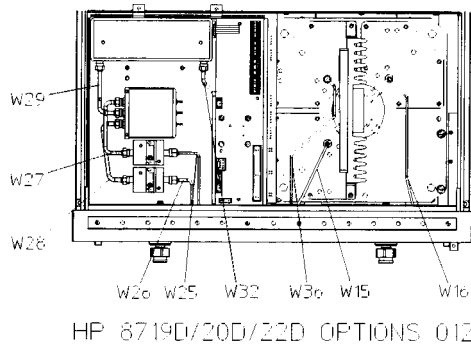
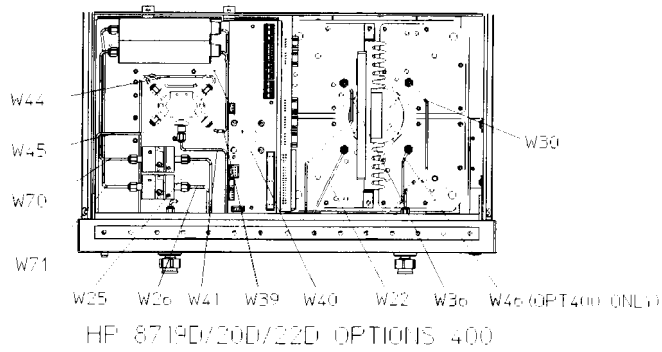
Cables, Bottom



HP 8719D/20D/22D OPTION 012

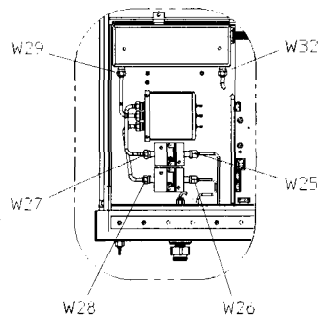
sbo133d

Cables, Bottom

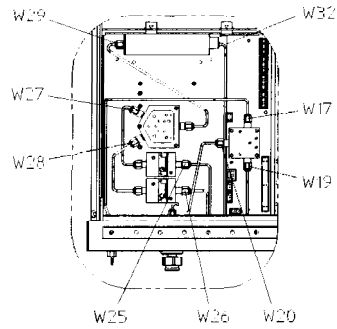


sbe137d

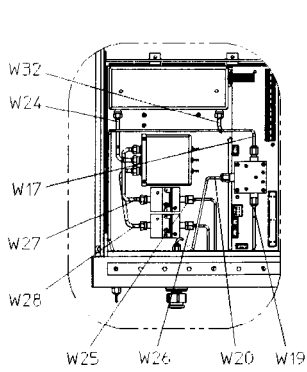
Cables, Bottom



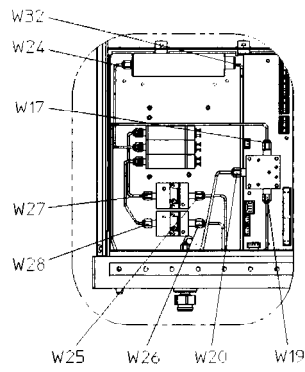
HP 8719D/20D
STANDARD



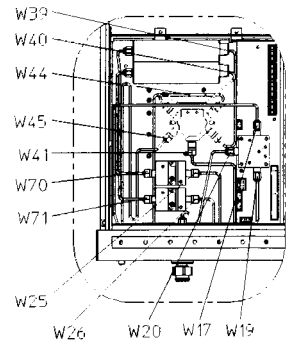
HP 8732D
OPTION 089



HP 8719D/20D
OPTION 089



HP 8719D/20D/22D
OPTIONS 007,089



HP 8719D/20D/22D
OPTIONS 400,089

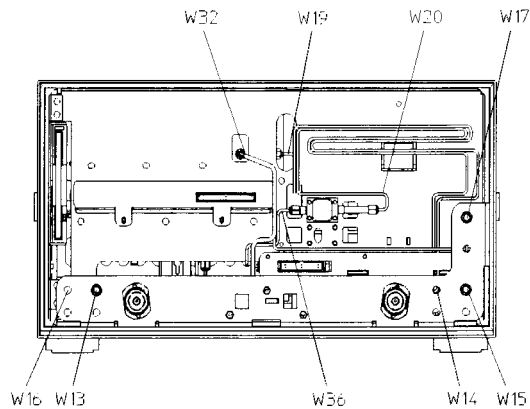
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Cables, **Front**

Ref. Desig.	Type.	Opt	HP Part Number	Qty	Description
A19			08720-60130	1	BD ASSY-GSP
A22			08720-60152	1	BD ASSY-DISPLAY INTERFACE (NOT SHOWN)
A56			08720-60182	1	BD ASSY-LED
A72,A73			5087-7072	2	R CHANNEL BUFFER AMPLIFIER
A75,A76			8490D OPT 006	2	ATTENUATOR 6 DB
A75,A76		400	8490D OPT 010	2	ATTENUATOR 10 DB (8722D)
W13	SR	012	08720-20164	1	A62 TO FRONT PANEL OUT (8719D/8720D)
W14	SR	012	08720-20154	1	A63 TO FRONT PANEL OUT. (8719D/8720D)
W13,W14	SR	012	08722-20102	1	A62,A63 TO FRONT PANEL OUT (8722D)
W15	SR	012	08720-20058	1	A66 TO FRONT PANEL IN (8719D/8720D)
W15	SR	012	08722-20079	1	A66 TO FRONT PANEL IN (8722D)
W16	SR	012	08720-20104	1	A65 TO FRONT PANEL JN (8719D/8720D)
W16	SR	012	08722-20081	1	A65 TO FRONT PANEL IN (8722D)
W17	SR	085,089	08720-20105	1	36 TO FRONT PANEL R CHANNEL IN (8719D/8720D)
W17	SR	085,089	08722-20058	1	35 TO FRONT PANEL R CHANNEL IN (8722D)
W19	SR	085,089	08722-20058	1	36 TO A68 (8722D)
W20	SR	080	08720-20134	1	36 TO A75
W20	SR	085	08720-20147	1	36 TO A75
W23	SR		08720-20047	1	A58 TO FRONT PANEL R CHANNEL OUT (8719D/20D)
W23	SR		08722-20071	1	A58 TO FRONT PANEL R CHANNEL OUT (8722D)
W32	SR	STD,012, 007,089	08720-20021	1	A58 TO A69 (8719D/8720D)
W32	SR	085,089	08720-20146	1	A58 TO A69 (8719D/8720D)
W32	SR	STD,012, 007,089	08722-20069	1	A58 TO A69 (8722D)
W32	SR	085	08722-20086	1	A58 TO A69 (8722D)
W33	SR		08720-20046	1	A75 TO FRONT PANEL R CHANNEL IN (8719D/20D)
W33	SR		08722-20098	1	A75 TO FRONT PANEL R CHANNEL IN (8722D)
W36	SR		08720-20041	1	A75 TO A64
W41	SR	400	08720-20173	1	A74 TO A58 (8719D/8720D)
W41	SR	400	08722-20054	1	974 TO A58 (8722D)
W60	SR	085	08720-20159	1	34 TO PORT 2 SWITCH (8719D/8720D)
W60	SR	085	08722-20097	1	34 TO PORT 2 SWITCH (8722D)
W61	SR	085	08720-20161	1	34 TO PORT 1 SWITCH (8719D/8720D)
W61	SR	085	08722-20098	1	34 TO PORT 1 SWITCH (8722D)

Ref. Desig.	Type*	opt	HP Part Number	Qty	Description
W62	SR	085	08720-20162	1	A63 TO PORT 2 COUPLER (8719D/8720D)
W62	SR	085	08720-20103	1	A63 TO PORT 2 COUPLER (8722D)
W63	SR	085	08720-20163	1	A62 TO PORT 1 COUPLER (8719D/8720D)
W63	SR	085	08722-20104	1	A62 TO PORT 1 COUPLER (8722D)
W68	SR	012,085, 080	08720-20165	1	A71 TO FRONT PANEL B IN (8719D/8720D)
W68	SR	012,085, 089	08722-20099	1	A71 TO FRONT PANEL B IN (8722D)
W69	SR	012,085, 089	08720-20166	1	A70 TO FRONT PANEL A IN (8719D/8720D)
W69	SR	012,085, 080	08722-20101	1	A70 TO FRONT PANEL A IN (8722D)
W73	SR	400	08720-20169	1	A74 TO A75
W75	SR	400	08720-20171	1	A74 TO A75 (8719D/8720D)
W75	SR	400	08722-20055	1	A74 TO A75 (8722D)
W77	SR	400	08720-20103	1	A67 TO A75

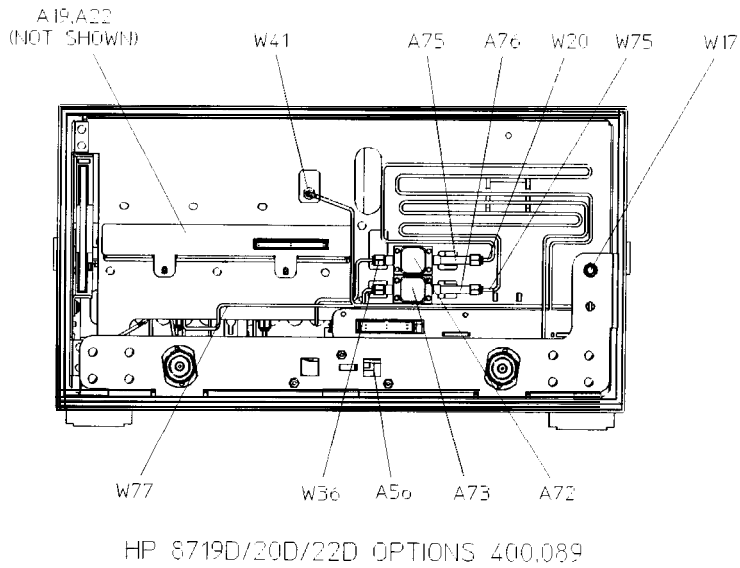
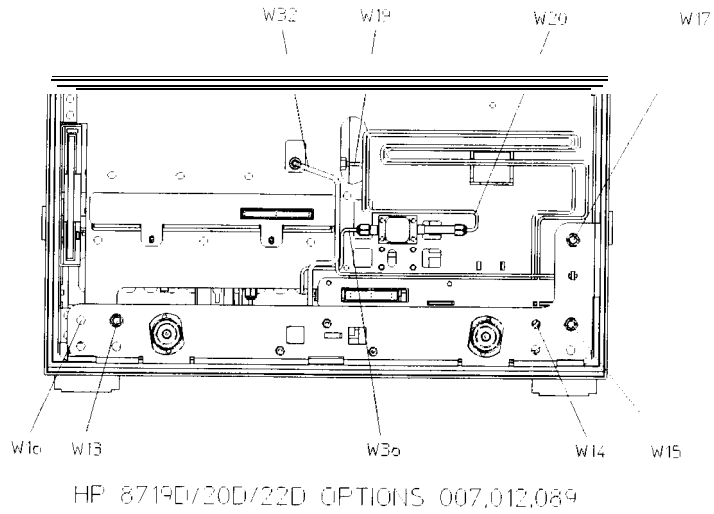
* SR Semi-Rigid Coax Cable



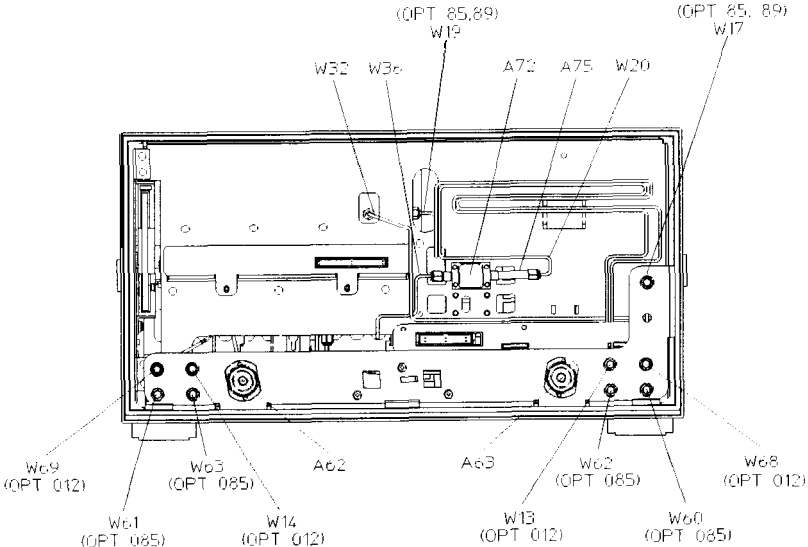
HP 8719D/20D/22D OPTIONS 007,012,089

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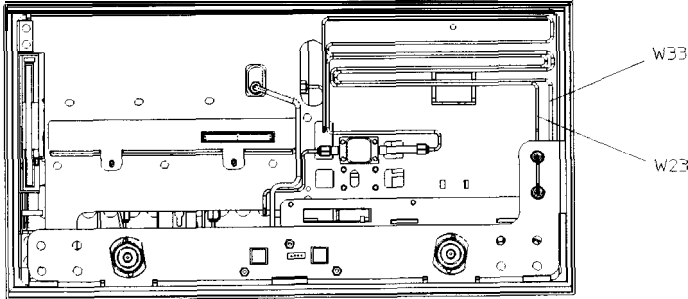
Cables, Front



Cables, Front



HP 8719D/20D/22D OPTION 085,012,089



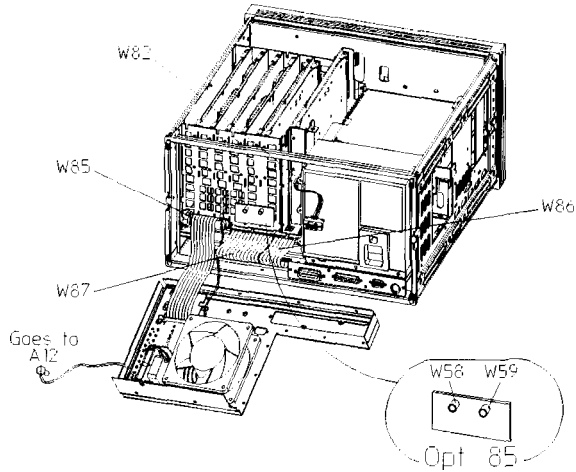
HP 8719D/20D STANDARD

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Cables, Rear

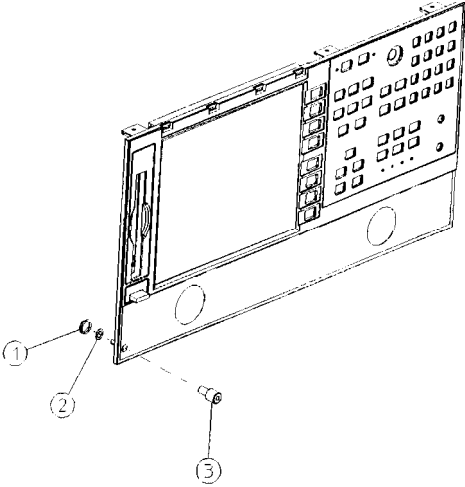
Ref. Desig.	Type*	Opt	HP Part Number	Qty	Description
W52	SR	085	08720-20098	1	REAR PANEL SOURCE OUT TO IN (W58 TO W59) (8719D/20D)
W52	SR	085	08722-20024	1	REAR PANEL SOURCE OUT TO IN (W58 TO W59) (8722D)
W58	SR	085	08720-20135	1	A69 TO REAR PANEL SOURCE OUT (8719D/8720D)
W58	SR	085	08722-20085	1	A69 TO REAR PANEL SOURCE OUT (8722D)
W59	SR	085	08720-20144	1	S4 TO REAR PANEL SOURCE IN (8719D/8720D)
W59	SR	085	08722-20084	1	S4 TO REAR PANEL SOURCE IN (8722D)
W82	1W		8120-6876	1	VGA OUT TO A22J2
W85	3W		8120-6407	1	A16 TO A17
W86	2W		8120-6382	1	A7 TO A17
W87	5W		8120-6379	1	A7 TO A17

* nW Wire Bundle (n is the number of wires in the bundle)



Front Panel Assembly, Outside

Ref. Desig.	option	HP Part Number	Qty	Description
1		2950-0006	1	NUT HEX 1/4-32
2		2190-0067	1	WASHER LK .256 ID
3		1510-0038	1	GROUND POST

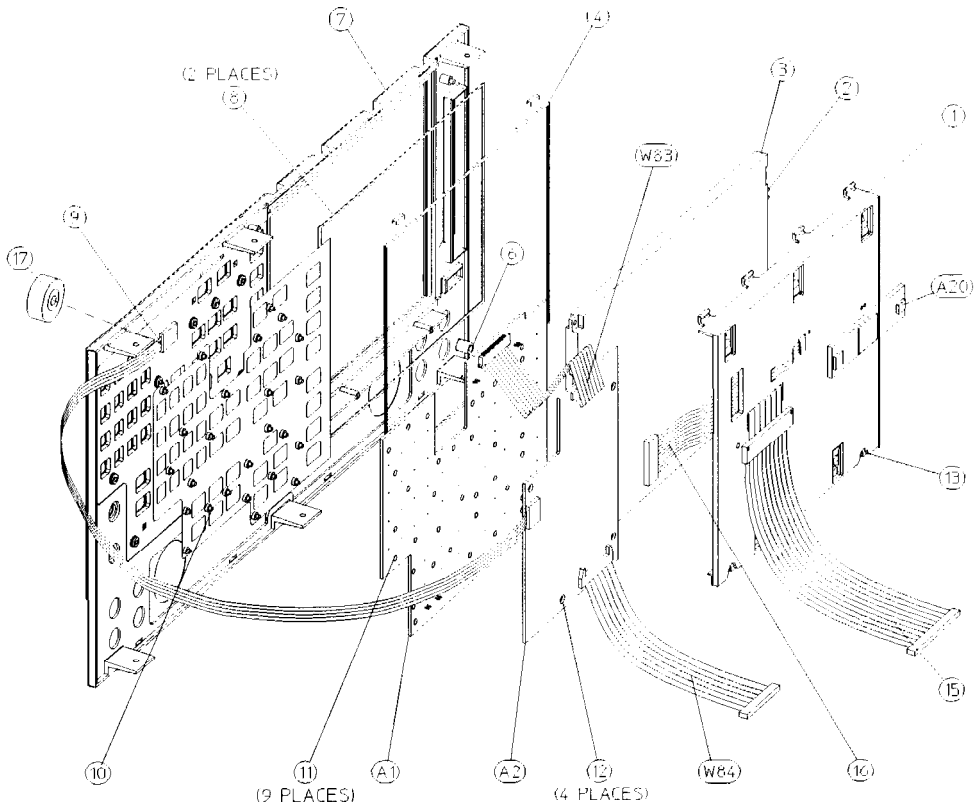


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Front Panel Assembly, Inside

Ref. Desig.	Option	HP Part Number	Qty	Description
1		08720-40012	1	DISPLAY HOLD DOWN
2		2090-0566	1	DISPLAY LAMP
3		08720-60160	1	ASSY-COLOR LCD (A18)
4		1000-0995	1	DISPLAY GLASS
6		2190-0067	1	WASHER LK .256 ID
6		2950-0006	1	NUT HEX 1/4-32
7	STD,089	08720-60162	1	FRONT PANEL-ASSY
7	012	08720-60163	1	FRONT PANEL-ASSY
7	085	08720-60164	1	FRONT PANEL -ASSY
7	012,085	08720-60165	1	FRONT PANEL-ASSY
8		08720-00096	2	GASKET
0		1990-1864	1	RPG (INCLUDES CABLE AND HARDWARE)
10		08720-40010	1	FLUBBER KEYPAD
11		0515-0430	0	SCREW SM 3.0 6 CWPNTX
12		0515-0665	4	SCREW SMM 3.0 14 CWPNTX
13		0515-0372	3	SCREW SMM 3.0 8 CWPNTX
1b		8120-6892	1	CABLE-GSP TO FLEX CIRCUIT
16		08720-60180	1	CABLE-FLEX CIRCUIT
17		E4400-40003	1	RPG KNOB
18		08719-80022	1	3719D NAME PLATE (not shown)
18		08720-80045	1	3720D NAME PLATE (not shown)
18		08722-80019	1	3722D NAME PLATE (not shown)
A1		08720-60127	1	BD ASSY-FRONT PANEL
A2		08720-60128	1	BD ASSY-FRONT PANEL INTERFACE
A20		0950-3068	1	ASSY-INVERTER
W88		8120-6432	1	A1 TO A2
W84		08720-60074	1	A2 TO A17

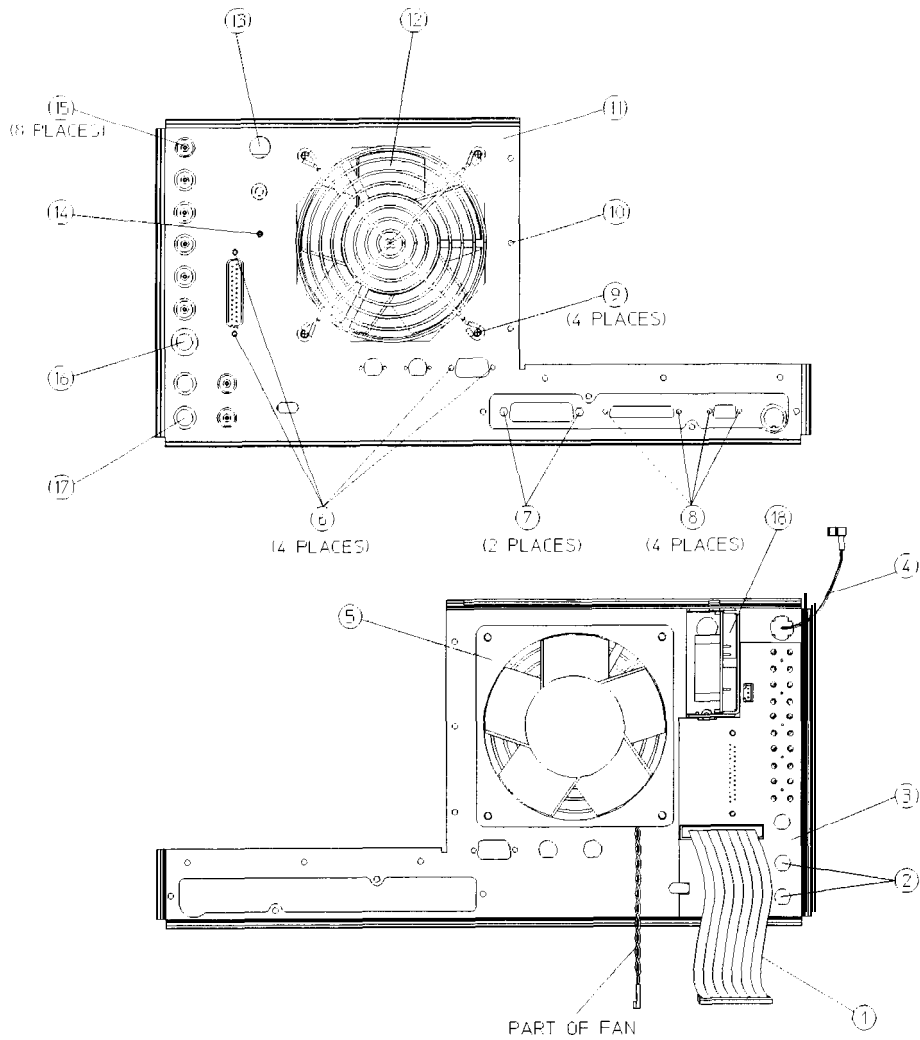
Front Panel Assembly, Inside



Rear Panel Assembly

Ref. Desig.	Option	HP Part Number	Qty	Description
1		8120-6407	1	W85-A17 TO A16
2		85047-60005	2	ASSY-FUSE
3		08720-60138	1	BD ASSY-REAR PANEL INTERFACE (A16)
4		08758-60026	1	ASSY-EXTERNAL REFERENCE CABLE
5		08415-60036	1	ASSY-FAN
6		1251-2942	4	FASTENER CONN RP LOCK
7		2190-0034	2	WASHER LK .194ID10
7		0380-0644	2	NUT STDF .327L 6-32
8		1251-2942	4	FASTENER CONN RP LOCK
9		0515-2040	4	SCREW SMM 3.6 16 PCFLTX
10		0515-0372	10	SCREW SMM 3.0 8 CWPNTX
11		08720-00071	1	REAR PANEL
12		3160-0281	1	FAN GUARD
13	1D5	0500-1310	1	NUT SPCL 1/2-28
13	1D5	2100-0068	1	WASHER LK .505ID
14	1D5	0515-0372	1	SCREW SMM 3.0 8 CWPNTX
16		2100-0102	1	WASHER LK .472ID
15		2950-0035	8	NUT HEX 15/32-32
16		0400-0271	8	GROMMET SN.5-515ID
17		2110-0047	2	FUSE
17		1400-0112	2	FUSE CAP
18	1D5			see "Rear Panel Assembly, Option 1D5"

Rear Panel Assembly

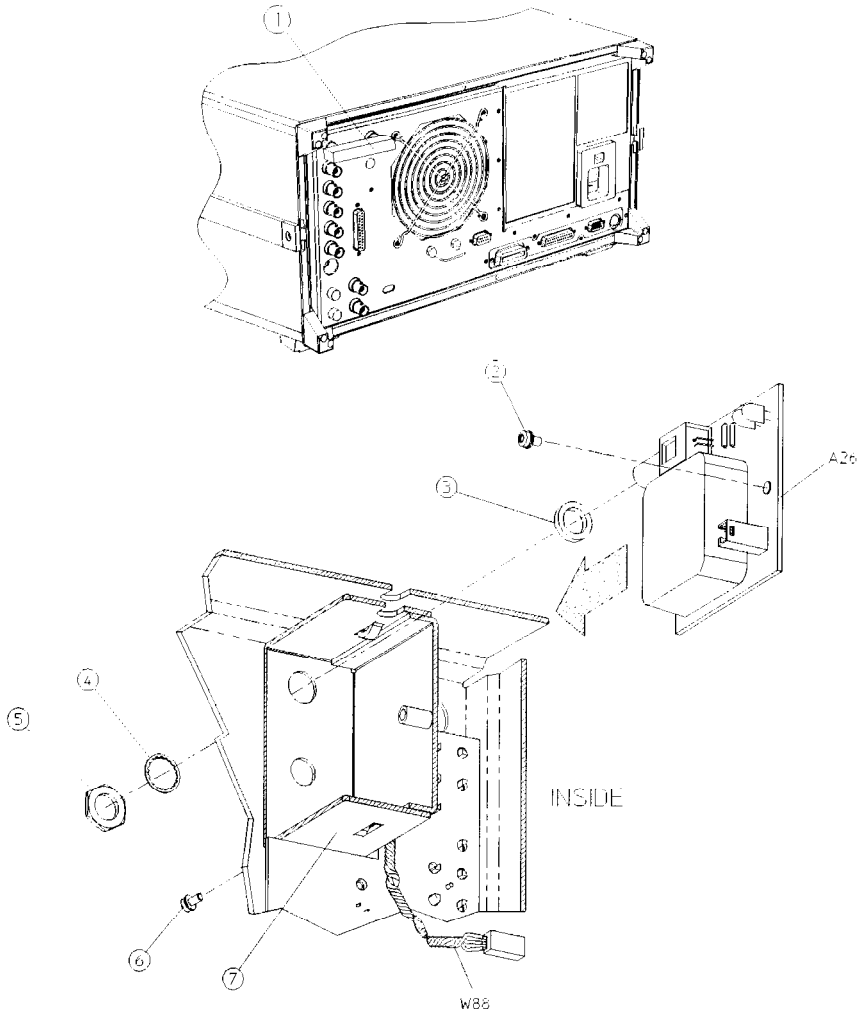


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Rear Panel Assembly, Option **1D5**

Ref. Desig.	option	HP Part Number	Qty	Description
1	1D5	1250-1859	1	ADAPTER-COAX
2	1D5	0515-0374	1	SCREW-MACHINE M3.0× 10 CW-PN-TX
3	1D5	3050-1546	1	WASHER-FLAT .505ID NY
4	1D5	2190-0068	1	WASHER-LOCK .505ID
5	1D5	0590-1310	1	NUT-SPECIALTY 1/2-28
6	1D5	0515-0430	1	SCREW-MACHINE M3.0× 6 CW-PN-TX
7	1D5	08753-00078	1	BRACKET-OSC BD
A26	1D5	08753-60158	1	BD ASSY-HIGH STABILITY FREQ REF
W88	1D5	8120-6458	1	RP INTERFACE (A16J3) to HIGH-STABILITY FREQ REF (A26J1)

Rear Panel Assembly, Option 1D5

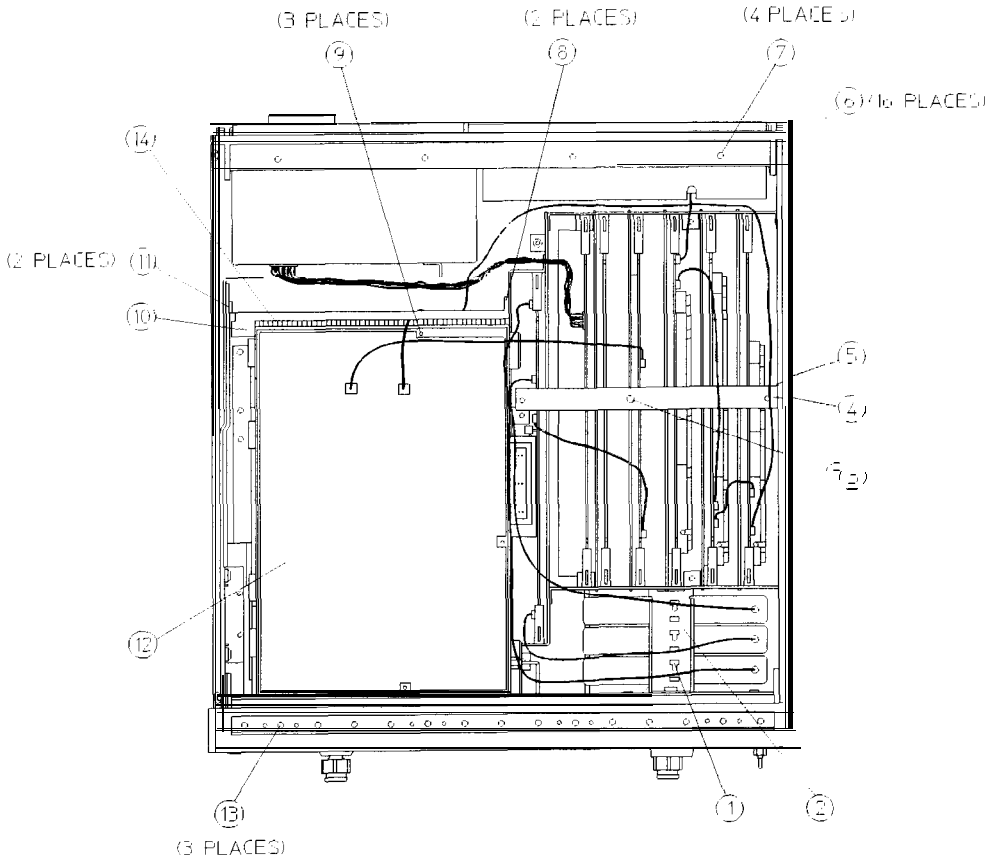


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Hardware, **Top**

Ref. Desig.	option	HP Part Number	Qty	Description
1		08720-40004	3	LOCATOR HOLD DOWNS
2		08720-00066	1	CAN HOLD DOWN
3		0515-2035	1	SCREW SMM 3.0 16 PCFLTX
4		08763-20062	1	PC STABILIZER CAP
5		08720-40001	1	PC BOARD STABILIZER
6		0515-2086	16	SCREW SMM 4.0 7 PCFLTX
7		0515-0458	4	SCREW SMM 3.6 10 CWPNTX
8		0515-0431	2	SCREW SMM 3.6 6 CWPNTX
9		0515-0430	3	SCREW SMM 3.0 6 CWPNTX
10		08720-00023	1	SOURCE HOLD DOWN
11		0515-0377	2	SCREW SMM 3.6 10 CWPNTX
12		08720-00038	1	SOURCE COVER
13		0515-1400	3	SCREW SMM 3.6 8 PCFLTX
14		08720-20185	1	SOURCE CASTING

Hardware, Top

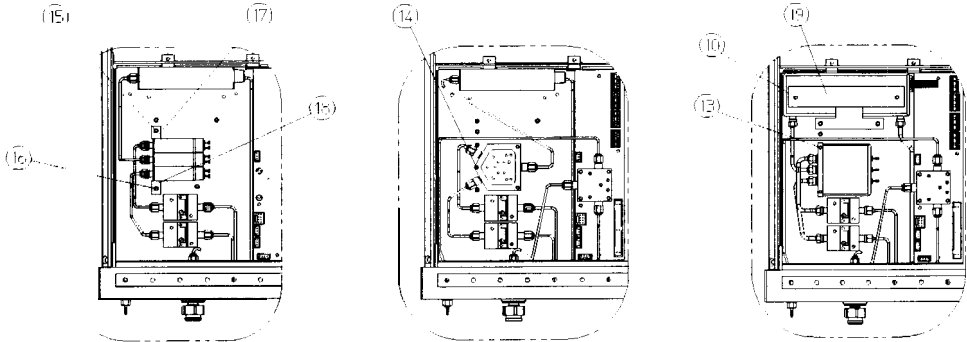


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Hardware, Bottom

Ref. Desig.	Option	HP Part Number	Qty	Description
1		0515-0430	1	SCREW SMM 3.0 6 CWPNTX
2		0515-0458	4	SCREW SMM 3.5 8 CWPNTX
3		0515-0430	2	SCREW SMM 3.0 6 PCFLTX
4		0515-2086	6	SCREW SMM 4.0 7 PCFLTX
5		0515-1400	4	SCREW SMM 3.5 8 PCFLTX
6		0515-0433	4	SCREW SMM 4.0 8 CWPNTX
6		3050-0001	4	WASHER FL .172ID 8
7		0515-0375	4	SCREW SMM 3.0 6 CWPNTX
8		0515-0430	4	SCREW SMM 3.0 6 CWPNTX
0		0515-1400	1	SCREW SMM 3.5 8 PCFLTX
10		2200-0105	2	SCREW SM 440 .312 PCFLTX
11		0515-0375	4	SCREW SMM 3.0 16 CWPNTX
12		0515-0375	2	SCREW SMM 3.0 16 CWPNTX
13		0515-0666	2	SCREW SMM 3.0 18 CWPNTX
14		0515-0665	3	SCREW SMM 3.0 14 CWPNTX
15		0515-0430	2	SCREW SMM 3.0 6 CWPNTX
16		08722-00016	2	SWITCH BRACKET
17		0515-2194	1	SCREW SMM 3.0 50 CWPNTX
18		0535-0031	1	NUT HEX SMM 3.0
19		08720-00113	1	BRACKET, ATTENUATOR

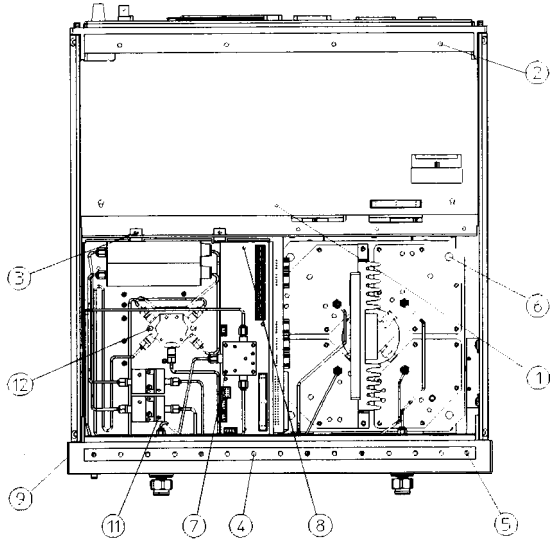
Hardware, Bottom



HP 8722D
OPTION 007

HP 8722D

HP 8719D/20D

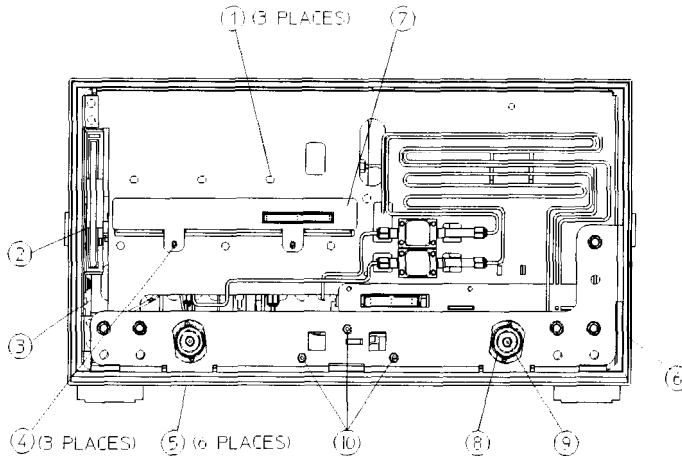


HP 8722D
OPTION 400

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Hardware, Front

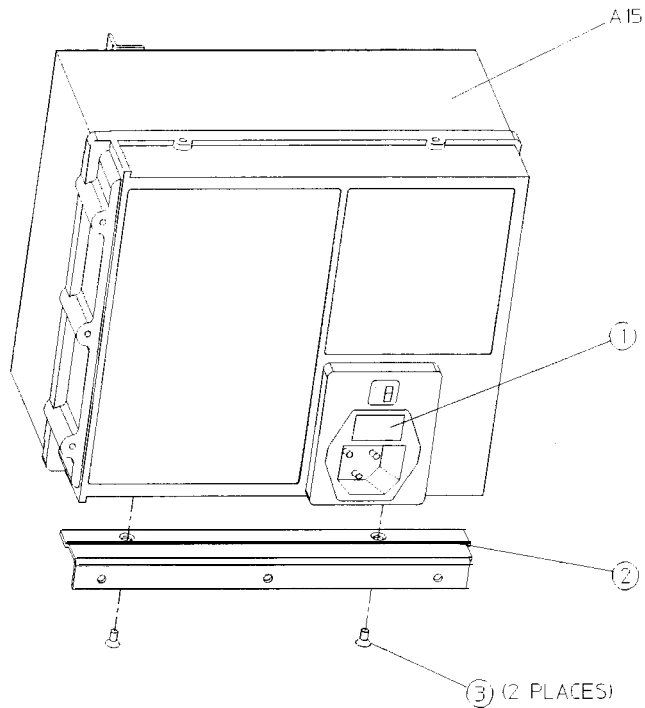
Ref. Desig.	option	HP Part Number	Qty	Description
1		0515-0382	3	SCREW SMM 4.0 12 CWPNTX
2		08720-00021	1	DISK DRIVE BRACKET
2		0505-1934	4	SCREW SMM 2.5 6 CWPNTX
3		08720-00077	1	ACTUATOR SWITCH ARM
3		08720-40014	1	AC LINE BUTTON
4		0515-0430	2	SCREW SMM 3.0 6 CWPNTX
5		0515-2086	6	SCREW SMM 4.0 7 PCFLT
6		0515-1400	1	SCREW SMM 3.5 8 PCFLT
7		08720-00093	1	CABLE MOUNTING BRACKET
8		5022-1087	2	NUT-FLANGE
9		08720-60159	1	TEST PORT CONNECTOR REPLACEMENT KIT (BP 8719D/20D)
9		08517-60027	1	TEST PORT CONNECTOR REPLACEMENT KIT (BP 8722D)
10		0515-0430	3	SCREW SMM 3.0 6



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Hardware, Preregulator

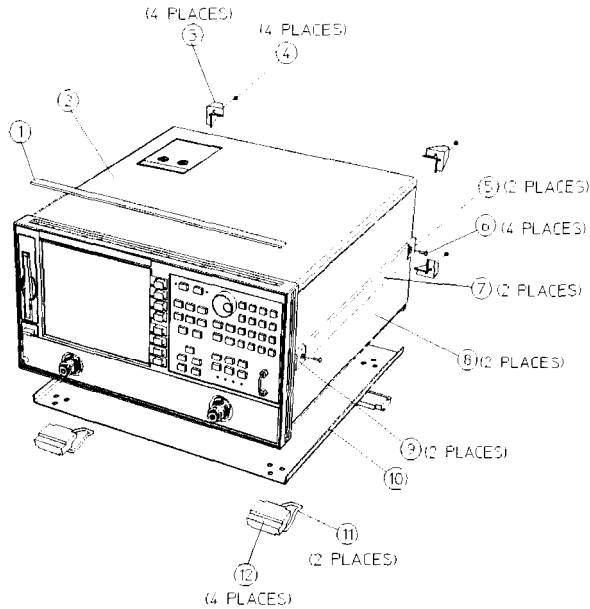
Ref. Desig.	option	HP Part Number	Qty	Description
1		2110-0780	1	FUSE 3A 250 V NON-TIME DELAY
2		08753-00065	1	BRACKET-PREREGULATOR
3		0515-1400	2	SCREW-MACHINE M3.5× 8 CW-FL-TX
A15		08753-60098	1	PREREGULATOR-ASSY
A15		08753-69098	1	PREREGULATOR-ASSY (REBUILT-EXCHANGE)



sg691d

Chassis Parts, Outside

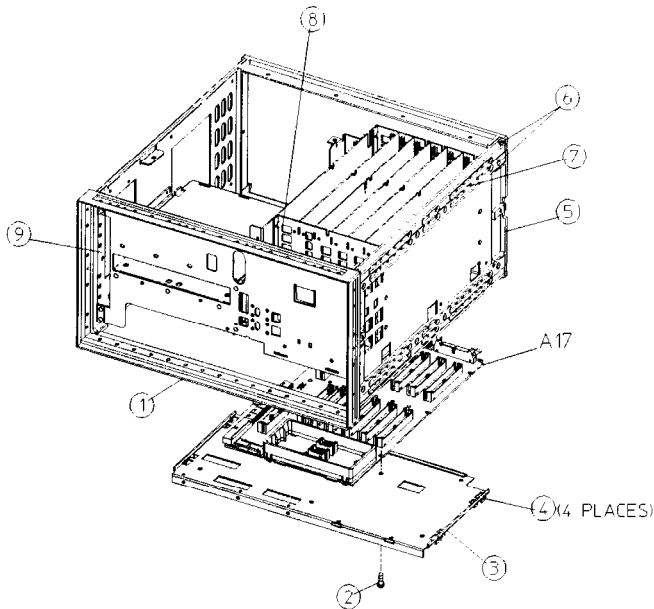
Ref. Desig.	Option	HP Part Number	Qty	Description
1		6041-9176	2	TRIM STRIP
2		08720-00078	1	COVER-TOP
3		5041-9188	4	REAR STANDOFF
4		0515-1402	4	SCREW SMM 3.6 8 PCPNTX
5		5041-9187	2	REAR CAP-SIDE STRAP
6		0515-1884	4	SCREW SMM 5.0 10 PCFLTXX
7		08720-00081	2	SIDE STRAP
8		08720-00080	2	COVER-SIDE
9		6041-9186	2	FRONT CAP-SIDE STRAP
10		08720-00079	2	COVER-BOTTOM
11		1460-1345	2	FOOT ELEVATOR
12		5041-9167	4	FOOT



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Chassis Parts, Inside

Ref. Desig.	option	HP Part Number	Qty	Description
1		5022-1190	1	FRONT PANEL FRAME
2		0515-0375	1	SCREW SMM 3.0 16 CWPNTX
3		08720-00076	1	MEMORY DECK
4		0515-0458	4	SCREW SMM 3.5 8 CWPNTX
5		5021-5808	1	REAR FRAME
6		0515-2086	16	SCREW SMM 4.0 7 PCFLT
7		08720-20131	4	SIDE STRUTS
8		08720-60116	1	ASSY-CHASSIS
9		08720-60116	1	ASSY-DISK DRIVE
A17		08720-60170	1	BD ASSY-MOTHERBOARD



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Table 13- 1. Miscellaneous Replaceable **Parts**

Description	HP Part Number
service Tools	
<p>IP 8719D/8720D/8722D TOOL KIT <i>includes the following:</i></p> <p>ADAPTER 2.4-mm (F) APC 3.5 (F) ADAPTER 2.4-mm (F) APC 3.5 (M) EXTENDER BOARD ASSEMBLY-FOR 2ND CONVERTERS EXTENDER BOARD ASSEMBLY SOURCE CONTROL EXTENDER BOARD ASSEMBLY ADAPTER-SMB (M) TO SMB (M) ADAPTER-SMB (F) TO BNC (F) ADAPTER-SMA (F) TO SMA (F) ADAPTER-SMA (M) TO SMA (M) SMBTEE FUSE .5A 125 V FUSE 1A 125 V FUSE 2A 125 V FUSE 4A 125 V FUSE 3.15A 250 V CABLE ASSEMBLY-EXTENDER RF CABLE ASSEMBLY-SMA FLEX WRENCH-OPEN ENDED 5.5 BAG-ANTISTATIC 12.0 x 15.0D</p>	08722-60018
Documentation	
<p>P 8719D/8720D/8722D SERVICE GUIDE P 8719D/8720D/8722D MANUAL SET <i>includes the following:</i> HP 8753D EXAMPLE PROGRAM DISK #1 HP BASIC HP 8753D EXAMPLE PROGRAM DISK #2 QUICKC AND QUICK BASIC HP 8719D/8720D/8722D PROGRAMMER'S GUIDE HP 8719D/8720D/8722D USER'S GUIDE (<i>includes Quick Reference, 08720-90289</i>) HP 8719D/8720D/8722D INSTALLATION/QUICK START GUIDE</p>	08720-90292 08720-90282 08753-10028 08753-10029 08720-90293 08720-90288 08720-90291

Table 13-1. Miscellaneous Replaceable **Parts** (continued)

Description	HP Part Number
Upgrade Kits	
FIRMWARE UPGRADE KIT	08720-60168
MECHANICAL TRANSFER SWITCH UPGRADE KIT ¹	OPTION 007
TIME DOMAIN CAPABILITY UPGRADE KIT ¹	OPTION 010
DIRECT SAMPLER ACCESS UPGRADE KIT ¹	OPTION 012
HIGH-POWER S-PARAMETER TEST SET UPGRADE KIT ¹	OPTION 085
FREQUENCY OFFSET MODE UPGRADE KIT ¹	OPTION 089
HIGH-STABILITY FREQUENCY REFERENCE UPGRADE KIT ¹	OPTION 1D5
FOURTH SAMPLER AND TRL CALIBRATION FIRMWARE UPGRADE KIT ¹	OPTION 400
Protective Caps for Connectors	
FEMALE HP-IB CONNECTOR	1252-5007
FEMALE PARALLEL PORT	1252-4690
RS-232 CONNECTOR	1252-4697
7-mm TEST PORTS	1401-0249
FEMALE 3.5 MM TEST PORTS	1401-0245
Fuses used on the A8 Post Regulator	
FUSE 2A 125 V NON-TIME DELAY 0.25×0.27	2110-0425
FUSE 0.75A 125 V NON-TIME DELAY 0.25×0.27	2110-0424
FUSE 2A 125 V NON-TIME DELAY 0.25×0.27	2110-0425
FUSE 4A 125 V NON-TIME DELAY 0.25×0.27	2110-0475
FUSE 1A 125 V NON-TIME DELAY 0.25×0.27	2110-0047
FUSE 0.5A 125 V NON-TIME DELAY 0.25×0.27	2110-0046
HP-IB Cables	
HP-IB CABLE, 1M (3.3 FT)	HP 10833A
HP-IB CABLE, 2M (6.6 FT)	HP 10833B
HP-IB CABLE, 4M (13.2 FT)	HP 10833C
HP-IB CABLE, 0.5M (1.6 FT)	HP 10833D
Touch-up Paint	
DOVE GRAY for <i>use on frame around front panel and painted portion of handles</i>	6010-1146
FRENCH GRAY for <i>use on side, top, and bottom covers</i>	6010-1147
PARCHMENT WHITE for <i>use on rack mount flanges, rack support flanges, and front panels</i>	6010-1148

Order the model number (HP 8719DU, 8720DU, 8722DU) plus the upgrade option designation.

Table 13-1. Miscellaneous Replaceable Parts (continued)

Description	HP Part Number
ESD Supplies	
ADJUSTABLE ANTISTATIC WRIST STRAP	9300-1367
5 FT GROUNDING CORD <i>for wrist strap</i>	9300-0980
2 x 4 FT ANTISTATIC TABLE MAT WITH 15 FT GROUND WIRE	9300-0797
<i>ANTISTATIC HEEL STRAP for use on conductive floors</i>	9300-1126
Other	
KEYBOARD OVERLAY <i>for external keyboard</i>	08753-80131
SYSTEM RACK KIT, ALSO ORDER THE FOLLOWING:	HP 85043D
FILLER PANEL-7 INCH	HP 40104A
RACK MOUNT FLANGE KIT, <i>for instruments with handles</i>	5063-9223
RACK MOUNT FLANGE KIT, <i>includes instrument handles</i>	5063-9236
RACK MOUNT FLANGE KIT, <i>instrument handles not included</i>	5063-9216
FRONT HANDLE	5063-9229
FLOPPY DISKS, 3.5 INCH DOUBLE-SIDED (box of 10)	HP 92192A

Table 13-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS	
A	assembly
B	fan; motor
J	electrical connector (stationary portion); jack
RPG	rotary pulse generator
W	cable; transmission path; wire
ABBREVIATIONS	
A	ampere
ALC	automatic level control
ASSY	assembly
AUX	auxiliary
BD	board
COAX	coaxial
CPU	central processing unit
CW	conical washer (screws)
D	diameter
ESD	electrostatic discharge
EXT	external
EYO	YIG oscillator
FL	flathead (screws)
FP	frontpanel
FRAC-N	fractional N
FREQ	frequency
GHz	gigahertz
HEX	hexagonal
HP	Hewlett-Packard
HP-IB	Hewlett-Packard interface bus
HX	hex recess (screws)
ID	inside diameter
IF	intermediate frequency
I/O	input/output
LED	light-emitting diode
M	meters
M	metric hardware
MHz	megahertz
mm	millimeters
MON	monitor
NOM	nominal
NY	nylon
OD	outside diameter
Opt	option
OSC	oscillator
PN	panhead
PC	patch lock (screws)
PC	printed circuit
PIG	peripheral interface group
PN	panhead (screws)
REF	reference
REPL	replacement
RP	rear panel
SH	socket head cap (screws)
TX	TORX recess (screws)
Qty	quantity
V	volt
WFR	wire formed
w/o	without
YIG	yttrium-iron garnet

Assembly Replacement and Post-Repair Procedures

This chapter contains procedures for removing and replacing the major assemblies of the HP 8719D/8720D/8722D network analyzer. A table showing the corresponding post-repair procedures for each replaced assembly is located at the end of this chapter.

Replacing an Assembly

The following steps show the sequence to replace an assembly in an HP 8719D/8720D/8722D Network Analyzer.

1. Identify the faulty group. Refer to Chapter 4, “Start Troubleshooting Here.” Follow up with the appropriate troubleshooting chapter that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, “Replaceable Parts.”
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, “Assembly Replacement and Post-Repair Procedures.”
4. Perform the necessary adjustments. Refer to Chapter 3, “Adjustments and Correction Constants.”
5. Perform the necessary performance tests. Refer to Chapter 2, “System Verification and Performance Tests.”

Warning **These** servicing instructions are for use by qualified personnel only. To avoid electrical shock, do not perform **any** servicing unless you are qualified to do so.

Warning **The** opening of covers or removal of parts is likely to expose dangerous voltages. Disconnect the instrument from **all** voltage sources while it is being opened.

Warning The power cord is connected to internal capacitors that may remain live for 10 seconds after disconnecting the plug from its power supply.

Caution Many of the assemblies in this instrument are very susceptible to damage from ESD (electrostatic discharge). Perform the following procedures only at a static-safe workstation and wear a grounding strap.

Procedures Described in this Chapter

The following pages describe assembly replacement procedures for the HP **8719D/8720D/8722D** assemblies listed below:

- Line Fuse
- Covers
- Front Panel Assembly
- Front Panel Interface and Keypad Assemblies
- Display Lamp and Assembly
- Rear Panel Assembly
- Rear Panel Interface Board Assembly
- Source Assemblies
- **A7** CPU Board Assembly
- **A7BT1** Battery
- **A15** Preregulator Assembly
- **A19** Graphics Processor Assembly
- **A3** Disk Drive Assembly
- **A62, A63** Test Port Couplers and LED Board Assemblies
- **A26** High Stability Frequency Reference (Option **1D5**) Assembly
- **B1** Fan Assembly

Line Fuse

Tools Required

- small slot screwdriver

Removal

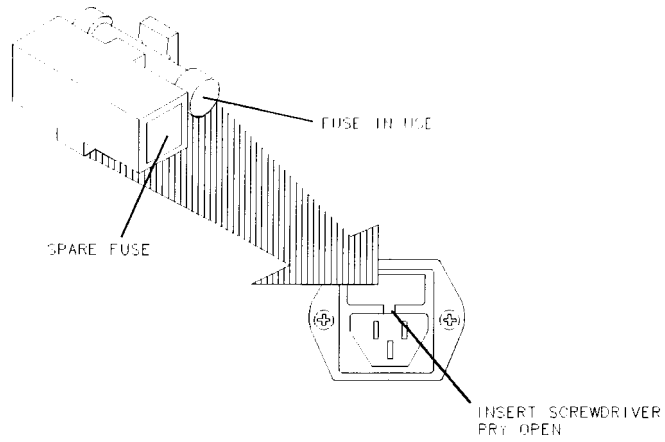
Warning For continued protection against **fire hazard**, replace fuse only with same type and rating (3 A 250 V **F**). **The** use of other fuses or materials is prohibited.

1. Disconnect the power cord.
2. Use a small slot screwdriver to pry open the fuse holder.
3. Replace the blown fuse with a 3 A 250 V F fuse (HP part number 2110-0708).

Replacement

1. Replace the fuse holder.

Line Fuse



qq6524

Covers

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- T-20 TORX screwdriver

Removing the top cover

1. Remove both upper rear feet (item 1) by loosening the attaching screws (item 2).
2. Loosen the top cover screw (item 3).
3. Slide cover off.

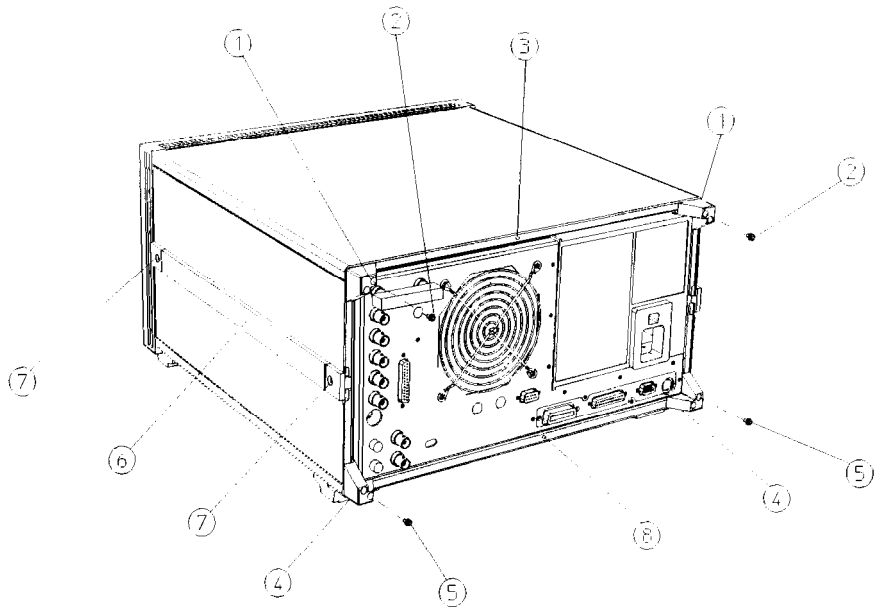
Removing the side covers

1. Remove the top cover.
2. Remove the lower rear foot (item 4) that corresponds to the side cover you want to remove by loosening the attaching screw (item 5).
3. Remove the handle assembly (item 6) by loosening the attaching screws (item 7).
4. Slide cover off.

Removing the bottom cover

1. Remove both lower rear feet (item 4) by loosening the attaching screws (item 5).
2. Loosen the bottom cover screw (item 8).
3. Slide cover off.

Covers



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Front Panel Assembly

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- small slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- 5/16-inch open-end torque wrench (set to 10 in-lb)

Removal

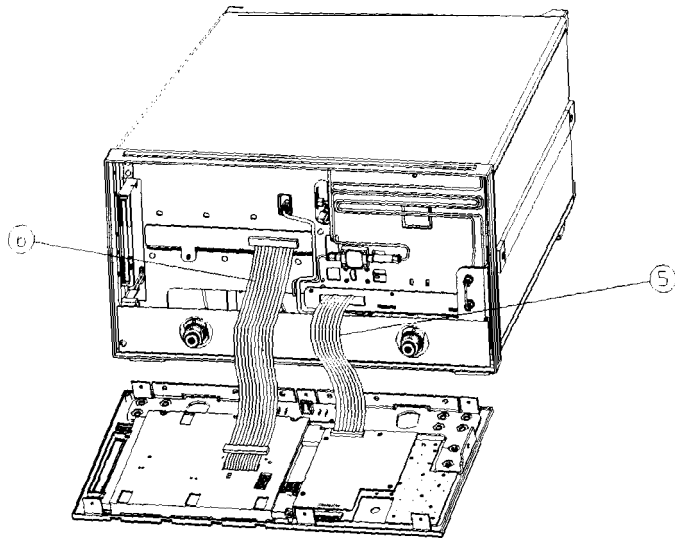
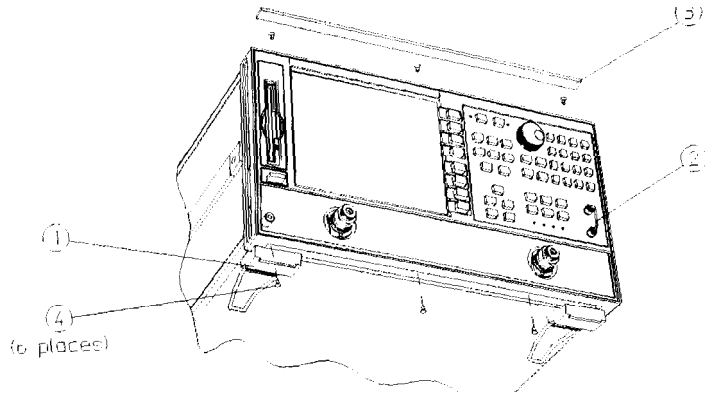
1. Disconnect the power cord.
2. Remove the front bottom feet (item 1).
3. Remove all of the RF cables that are attached to the front panel (item 2).
4. Remove the trim strips (item 3) from the top and bottom edges of the front frame by prying under the strip with a small slot screwdriver.
5. Remove the six screws (item 4) from the top and bottom edges of the frame.
6. Slide the front panel over the test port connectors.
7. Disconnect the ribbon cables (item 5) and (item 6). The front panel is now free from the instrument.

Replacement

1. Reverse the order of the removal procedure.

Note When reconnecting semi-rigid cables, it is recommended that the connections be torqued to 10 in-lb.

Front Panel Assembly



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Front Panel Interface and Keypad Assemblies

Tools Required

- **T-10** TORX screwdriver
- **T-15** TORX screwdriver
- small slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- **5/16-inch** open-end torque wrench (set to 10 in-lb)

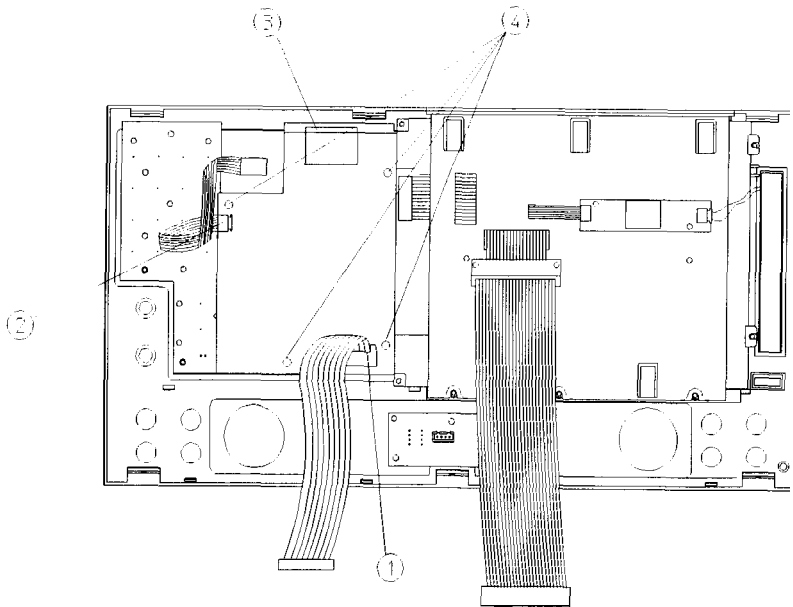
Removal

1. Remove the front panel assembly from the analyzer (refer to “Front Panel Assembly” in this chapter).
2. Remove the ribbon cable (item 1) from the front panel interface.
3. Disconnect the RPG cable (item 2) from the front panel interface.
4. Disconnect the ribbon cable (item 3) by sliding your finger nail between the connector and the cable.
5. Remove the four screws (item **4**), attaching the interface board.
6. Remove the nine screws from the AI front panel board to access and remove the keypad.

Replacement

1. Reverse the order of the removal procedure.

Front Panel Interface and Keypad Assemblies



Display Lamp and Assembly

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- small slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- 5/16-inch open-end torque wrench (set to 10 m-lb)

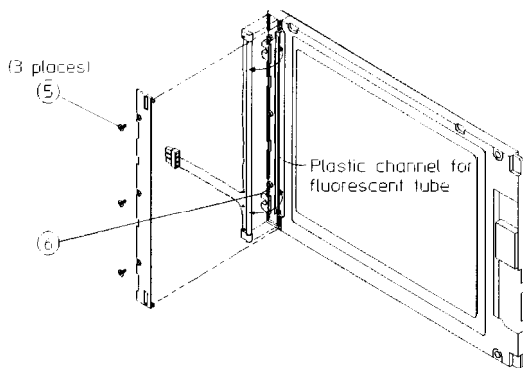
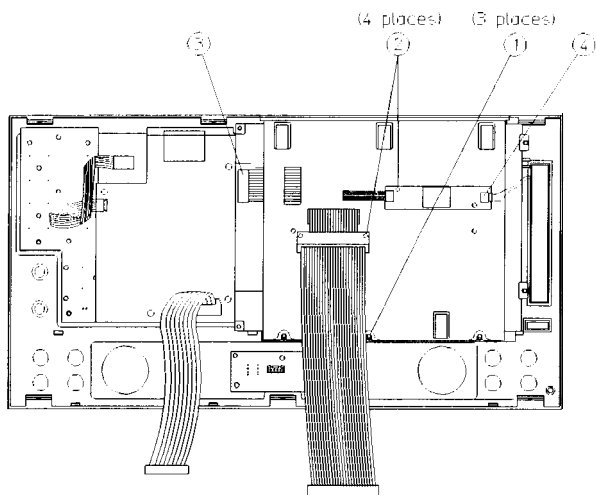
Removal

1. Remove the front panel assembly (refer to “**Front Panel Assembly**” in this chapter).
2. Remove the three screws (item 1) that attach the display to the front panel.
3. Remove the four screws (item 2), disconnecting the accessories from the display.
4. Disconnect the cable (item 3) from the AI assembly.
5. Disconnect the display lamp cable (item 4).
6. Lift the display from the front panel and remove the three screws (item 5) from the outside of the display.
7. Pull the lamp (item 6) out with a curving side motion, as shown.

Replacement

1. Reverse the order of the removal procedure.

Display Lamp and Assembly



Rear Panel Assembly

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

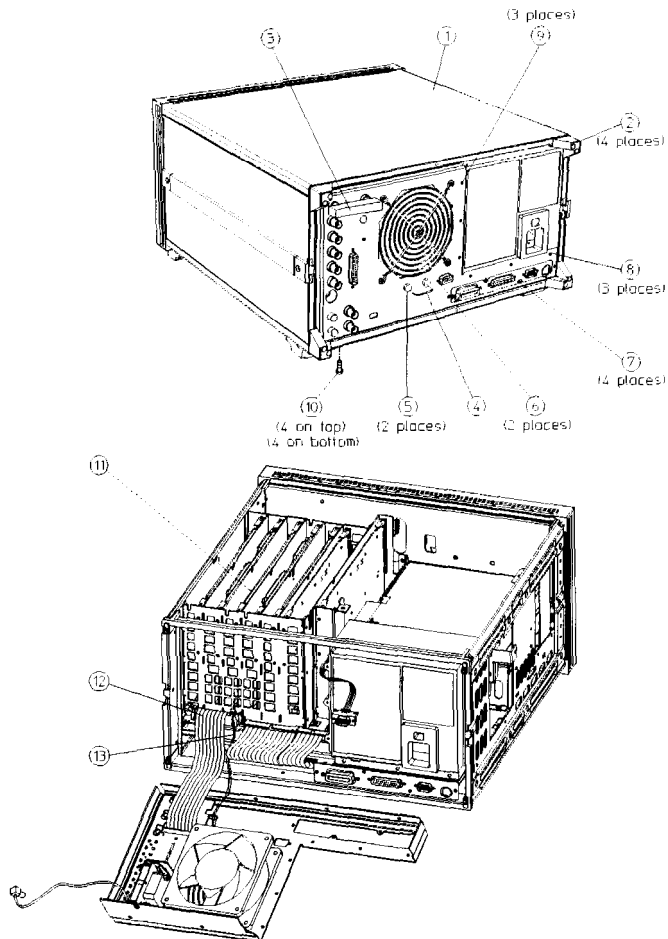
Removal

1. Disconnect the power cord and remove the top (item 1) and bottom covers (refer to “Covers” in this chapter).
2. Remove the four rear standoffs (item 2).
3. If the analyzer has option **1D5**, remove the BNC jumper from the high stability frequency reference (item 3).
4. If the analyzer has option 085, remove the RF cable (item 4) and the connectors’ attaching hardware (item 5).
5. Remove the hardware (item 6) that attaches the **RS-232** connector to the rear panel.
6. Remove the four screws (item 7) that attach the interface bracket to the rear panel.
7. Remove the six screws (item 8) and (item 9), that attach the **preregulator** to the rear panel.
8. Remove the eight screws (item 10) from the rear frame: four from the top edge and four from the bottom edge.
9. Remove the screw from the pc board stabilizer and remove the stabilizer.
10. Lift the reference board (**A12**) from its motherboard connector and disconnect the flexible RF cable (item 11).

11. Pull the rear panel away from the frame. Disconnect the ribbon cable (item 12) from the motherboard connector, pressing down and out on the connector locks. Disconnect the wiring harness (item 13) from the motherboard.

Replacement

1. Reverse the order of the removal procedure.



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Rear Panel Interface Board Assembly

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

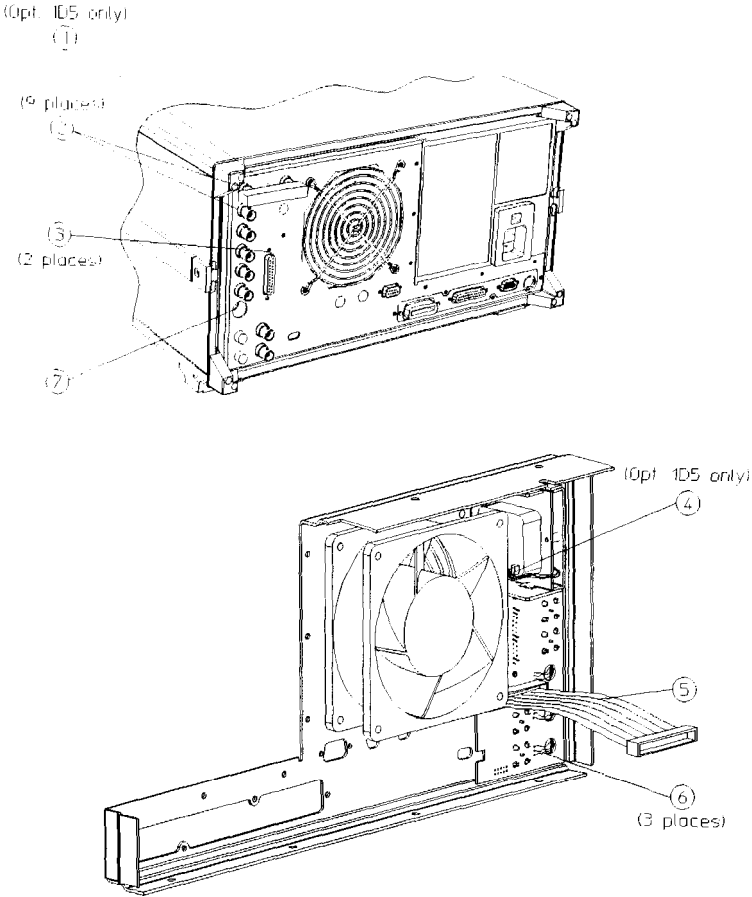
Removal

1. Disconnect the power cord and remove the top and bottom covers (refer to “Covers” in this chapter).
2. If the analyzer has option **1D5**, remove the high-stability frequency reference jumper (item 1).
3. Remove the hardware that attaches the nine BNC connectors to the rear panel (item 2).
4. Remove the hardware that attaches the interface connector to the rear panel (item 3).
5. Remove the rear panel from the analyzer (refer to “Rear **Panel** Assembly” in this chapter).
6. If the analyzer has option **1D5**, disconnect the cable (item 4) from the rear panel interface board.
7. Disconnect the ribbon cable (item 5) from the rear panel interface board.
8. Disconnect the wiring for the three BNC connectors and remove the attaching hardware (item 6).
9. Remove the **MEAS** RESTART connector from the interface board, approaching it from the outside of the rear panel assembly (item 7).

Replacement

1. Reverse the order of the removal procedure.

Rear Panel Interface Board Assembly



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Source Assemblies

Tools Required

- T-15 TORX screwdriver
- 5/16-inch open-end torque wrench (set to 10 in-lb)
- ESD (electrostatic discharge) grounding wrist strap

Removal

1. Disconnect the power cord and remove the top cover (refer to “Covers” in this chapter).
2. Remove the front panel (refer to “Front Panel Assembly” in this chapter).
3. Remove the source module cover.

A58 M/A/D/S Removal

4. Disconnect the cables (item 2) and (item 3 for all but Option 400) from the M/A/D/S.
5. Remove the four screws (item 6) from each corner of the assembly.

Oscillator Removal

6. Remove the three screws (item 1) that attach the source module to the analyzer.
7. Disconnect the cables (item 2) and (item 3 for **all** but Option 400) from the M/A/D/S.
8. Remove the four screws (item 4) and (item 5) from the source module bracket. Remove the bracket.
9. Lift the source module out of the analyzer.
10. Remove a screw (item 7) from the back of the oscillator.
11. Disconnect attaching RF cables.

A9 Source Control Board Removal

12. Remove the three screws (item 1) that attach the source module to the analyzer.
13. Disconnect the cables (item 2) and (item 3 for all but Option 400) from the M/AID/S.
14. Remove the four screws (item 4) and (item 5) from the source module bracket. Remove the bracket.
15. Lift the source module out of the analyzer.
16. Remove three screws to detach the bottom source module cover.
17. Remove four screws that **attach** the source control board to the source module frame.
18. Place one hand on the top of the **A9** board, with your thumb near the **A58** M/A/D/S, to push the board. Place your other hand on the bottom side of the **A9**, with your thumb and index **finger** put through the drilled holes, to pull the board.

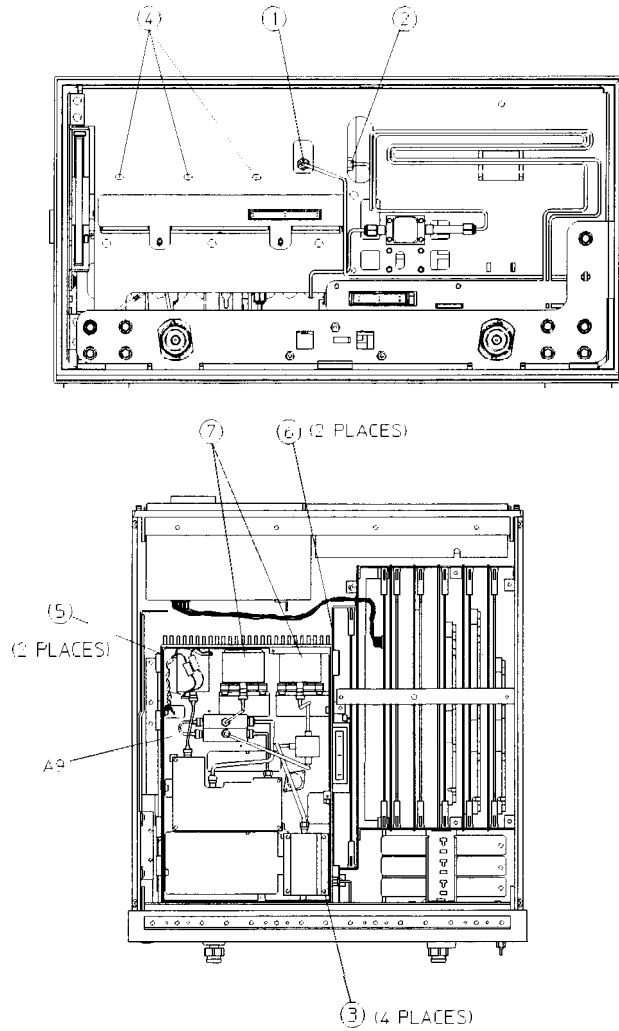
Source Assemblies

Replacement

1. Reverse the order of the removal procedure.

Note	When replacing the A9 source control board, push the board evenly on all the microcircuit pins.
	Check all the pin sockets from the back of the A9 board to ensure that all of the pins are inserted. For HP 8722Ds , you may need an eye glass to inspect the shallow pins of the S1 high band switch.
	When replacing the source module into the analyzer, push the cables aside before seating the module.

Source Assemblies



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A7 CPU Board Assembly

Tools Required

- T-10 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

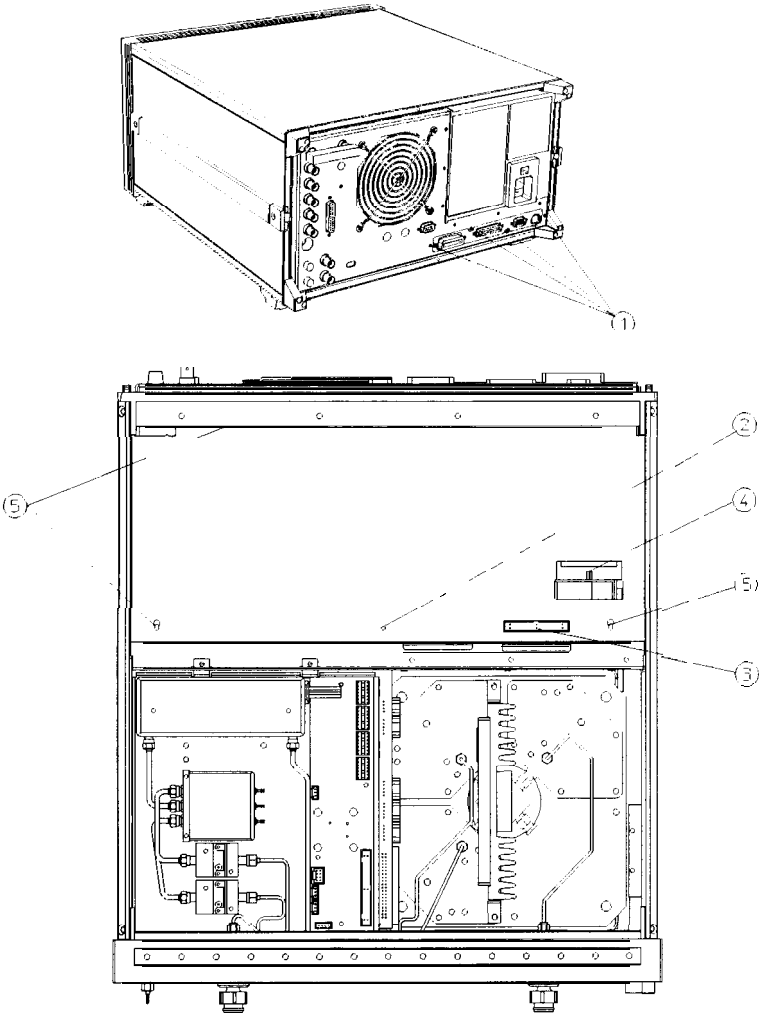
Removal

1. Disconnect the power cord.
2. Remove the four bottom feet and bottom cover (refer to “Covers” in this chapter).
3. Remove the four screws (item 1) on the rear panel.
4. Turn the analyzer over and remove the screw (item 2) that secures the CPU board to the deck.
5. Disconnect the ribbon cable (item 3), sliding your **finger** nail between the cable and the connector.
6. Disconnect the ribbon cable (item 4) from the CPU board.
7. Slide the board towards the front of the instrument so that it disconnects from the three standoffs (item 5).
8. Disconnect the ribbon attached at the rear of the CPU board.
9. Lift the board off of the standoffs.

Replacement

1. Reverse the order of the removal procedure.

A7 CPU Board Assembly



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A7BT1 Battery

Tools Required

- T-10 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- soldering iron with associated soldering tools

Removal

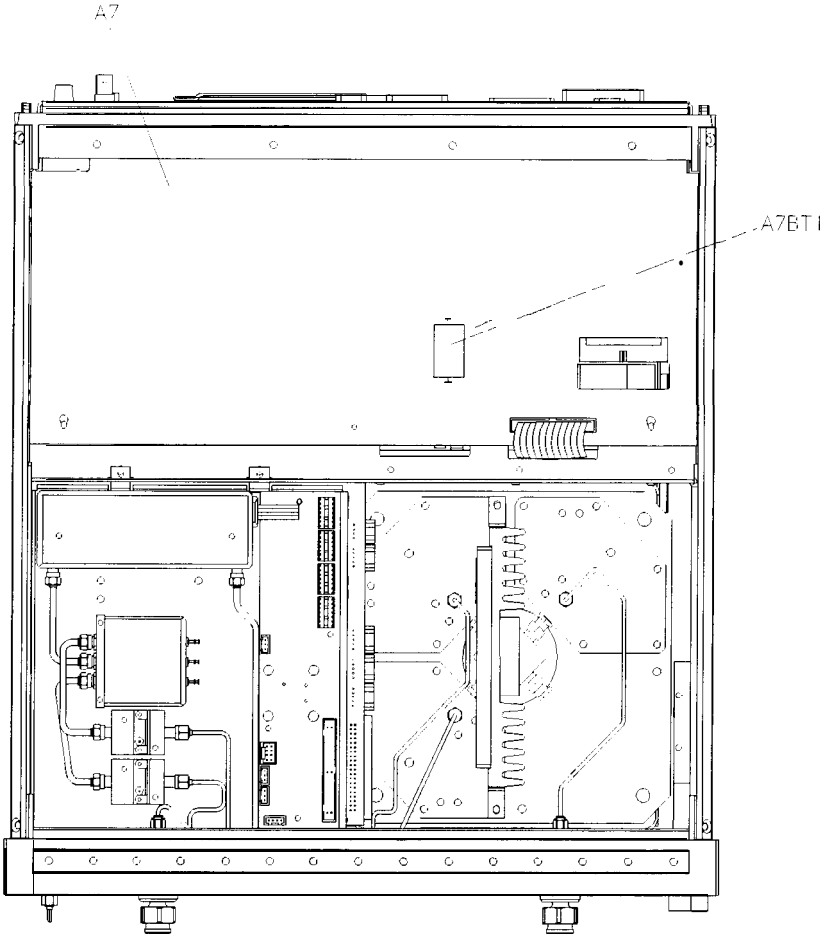
1. Remove the **A7** CPU board (refer to “**A7** CPU Board Assembly” in this chapter).
2. Unsolder and remove **A7BT1** from the **A7** CPU board.

Warning Battery **A7BT1** contains lithium. The battery may explode if it is incorrectly replaced. Do not incinerate or puncture this battery. Either dispose of the discharged battery, according to manufacturer’s instructions, or collect as small chemical waste.

Replacement

1. Make sure the new battery is inserted into the **A7** board with the correct polarity.
2. Solder the battery into place.
3. Replace the **A7** CPU board (refer to “**A7** CPU Board Assembly” in this chapter).

A7BT1 Battery



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A 15 Preregulator Assembly

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

Removal

1. Remove the rear panel (refer to “Rear Panel Assembly” in this chapter).
2. Disconnect the wire bundles (item 1) (item 2) from the analyzer.
3. Remove the preregulator (**A15**) from the frame.

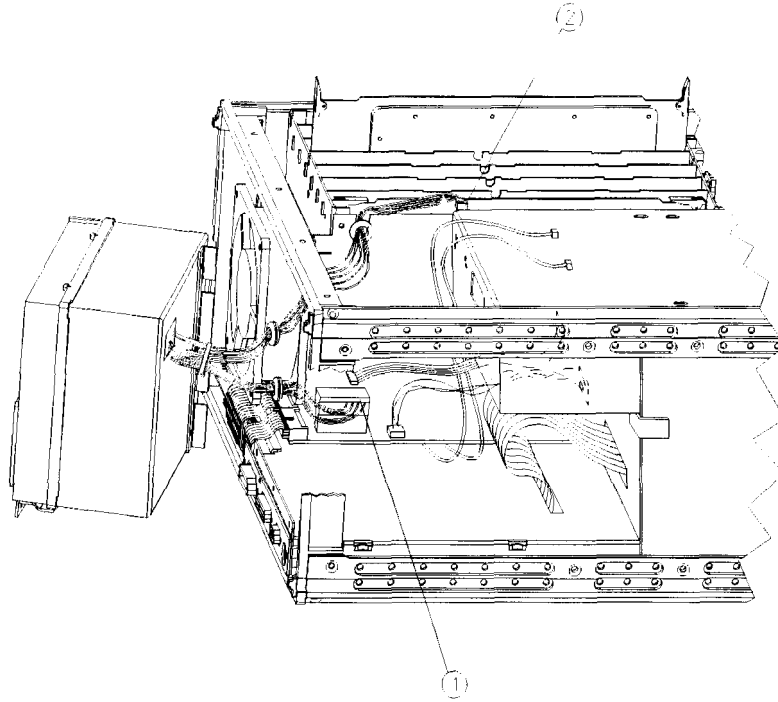
Replacement

1. Reverse the order of the removal procedure.

Note

- When reinstalling the preregulator (**A15**), make sure the three grommets on the wiring bundles are seated in the slots on the back side of the preregulator and also in the slot in the card cage wall.
 - After reinstalling the preregulator (**A15**), be sure to set the line voltage selector to the appropriate setting, 115 V or 230 V.
-

A 15 Preregulator Assembly



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A19 Graphics Processor Assembly

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

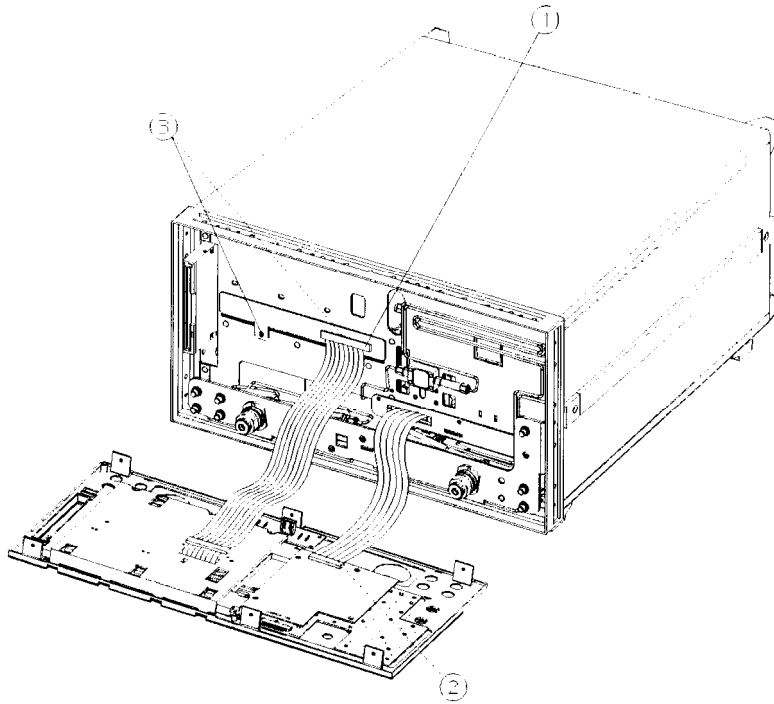
Removal

1. Disconnect the power cord and remove the front panel (refer to “**Front Panel Assembly**” in this chapter).
2. Disconnect the two ribbon cables (item 1) and (item 2).
3. Remove the two screws (item 3) that attach the GSP to the front of the analyzer.
4. Pull the GSP board out of the analyzer.

Replacement

1. Reverse the order of the removal procedure.

A19 Graphics Processor Assembly



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A3 Disk Drive Assembly

Tools Required

- 2-mm extended bit allen wrench
- T-S TORX screwdriver
- T-10 TORX screwdriver
- T-15 TORX screwdriver
- T-20 TORX screwdriver
- small slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap

Required Diskette

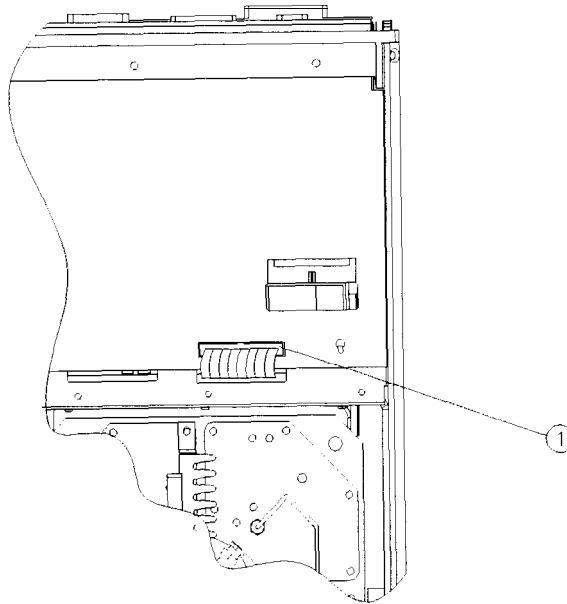
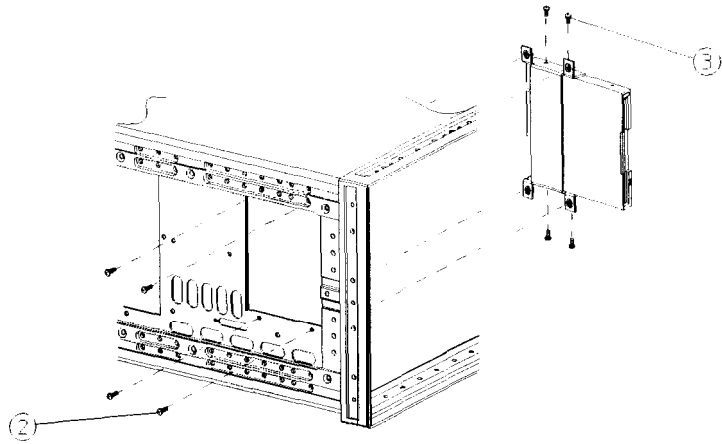
- 3.5" diskette, 1.44 MB, formatted (DOS)

Removal

1. Disconnect the power cord and remove the top, bottom, and left side covers (refer to “Covers” in this chapter).
2. Remove the front panel (refer to “**Front Panel Assembly**” in this chapter).
3. Turn the instrument upside-down and disconnect the ribbon cable (item 1) from the disk drive.
4. Remove the four screws (item 2) that secure the disk drive to the disk drive bracket. There are two screws on the top, and two screws on the bottom.
5. Slide the disk drive out of the analyzer, and set the disk drive aside..
6. Remove the four screws (item 3) that secure the disk drive bracket to the side of the analyzer, and remove the bracket.

Note Save the screws removed in this step for use later when installing the new disk drive bracket.

A3 Disk Drive Assembly



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A3 Disk Drive Assembly

Replacement

1. Attach the plug (part number 08753-40016) to the new disk drive with a #2 hex screw (part number 0515-1048).
2. Attach the disk-drive bracket (part number 08753-00152) to the disk drive with the three remaining #2 socket-head screws.

Note	Place the disk drive on a horizontal and flat surface when attaching the bracket. This helps assure that there is no unnecessary distortion of the disk drive assembly.
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3. Slide the disk drive and bracket assembly into the analyzer.
4. Loosely secure the disk drive bracket to the side of the frame using the four screws saved previously.
5. Connect the existing ribbon cable to the replacement disk drive.

Note	Make sure the disk drive connector contacts touch the ribbon cable contact areas (the ribbon cable contact areas must face the contacts in the disk drive connector). Also assure that the connector is properly locked.
-------------	--

6. Replace the front panel with the exception of fastening the top left screw (refer to “Front Panel Assembly” in this chapter).
7. While adjusting the position of the disk drive, tighten the screws that secure the disk drive bracket to the side of the frame.
8. Insert a disk into the disk drive and then eject the disk.
 - If the disk drive door operation is satisfactory, continue with step 10.
 - If the disk drive door operation is not satisfactory, continue with step 9.
9. Loosen and then retighten the four screws that secure the disk drive to the disk drive bracket:
 - a. Loosen the three screws that are readily accessible.
 - b. Loosen the uppermost, frontmost screw through the top left access hole in the front frame.
 - c. After disk drive tension has been released, retighten all four screws.

A3 Disk Drive Assembly

10. Finish the front panel replacement procedure by fastening the remaining screw (top left) to the front panel.
11. Replace the covers (refer to “Covers” in this chapter).
12. Connect the line cord and turn the analyzer on. Test the disk drive by saving and **recalling** a **file**.

A62, A63 Test Port Couplers and LED Board Assemblies

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- **small** slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- **5/16-inch** open-end torque wrench (set to 10 in-lb)

Removal

1. Remove the bottom cover (refer to “Covers” in this chapter).
2. Remove the front panel (refer to “Front Panel Assembly” in this chapter).
3. Reaching the connections from the bottom of the analyzer, disconnect the four RF cables attached to the couplers: two from the back of the couplers and two from between the couplers.
4. Remove the six screws (item 1) from the bottom edge of the front panel frame.
5. Remove one screw (item 2) from the right side of the coupler bracket.
6. Remove the coupler nuts (item 3).

LED Board Removal

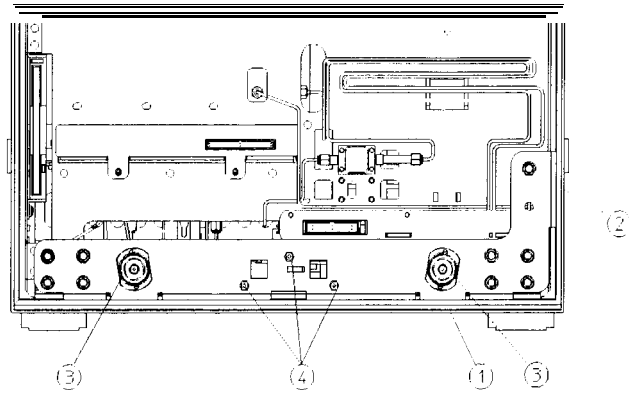
7. Remove the three screws (item 4) that attach the LED board to the coupler bracket.

Replacement

1. Reverse the order of the removal procedure.

Note When reconnecting semi-rigid cables, it is recommended that the connections be torqued to 72 in-lb.

A62, A63 Test Port Couplers and LED Board Assemblies



sbe135d

A26 High Stability Frequency Reference (Option 1D5) Assembly

Tools Required

- **T-10** TORX screwdriver
- **T-15** TORX screwdriver
- **9/16-inch** hex-nut driver
- ESD (electrostatic discharge) grounding wrist strap

Removal

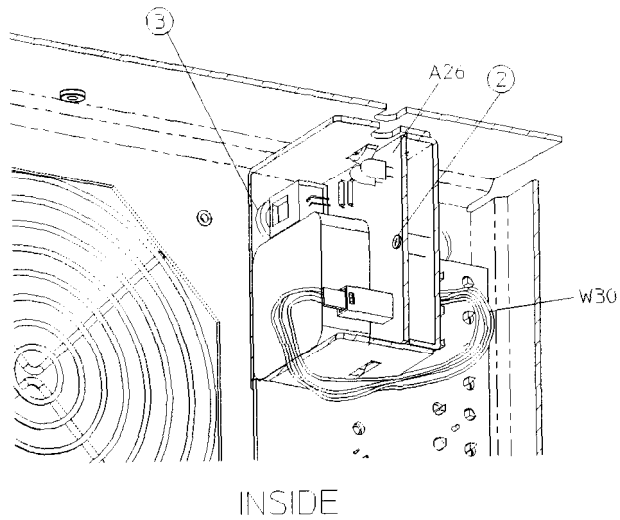
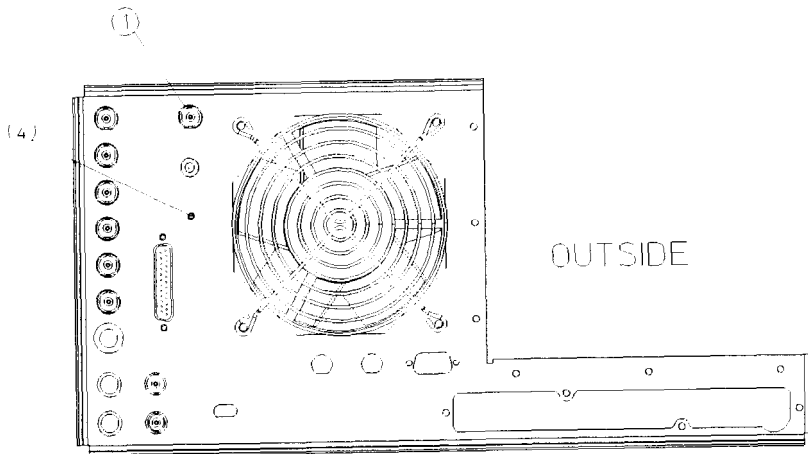
1. Remove the rear panel (refer to “Rear Panel Assembly” in this chapter).
2. Disconnect **W30** from the high stability frequency reference board (**A26**).
3. Remove the BNC connector nut and washer from the “**10 MHz PRECISION REFERENCE**” connector (item 1) on the rear panel.
4. Remove the screw (item 4) that attaches the **1D5** assembly to the rear panel.
5. Remove the screw (item 2) that secures the high stability frequency reference board (**A26**) to the bracket.
6. Slide the board out of the bracket. Be careful not to lose the plastic spacer washer (item 3) that is on the BNC connector as the board is being removed.

Replacement

1. Reverse the order of the removal procedure.

Note	Before reinserting the high stability frequency reference board (A26) into the bracket, be sure the plastic spacer washer (item 3) is on the BNC connector.
-------------	--

A26 High Stability Frequency Reference (Option 1D5) Assembly



sb658d

Bl Fan Assembly

Tools Required

- 2.5-mm hex-key driver
- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

Removal

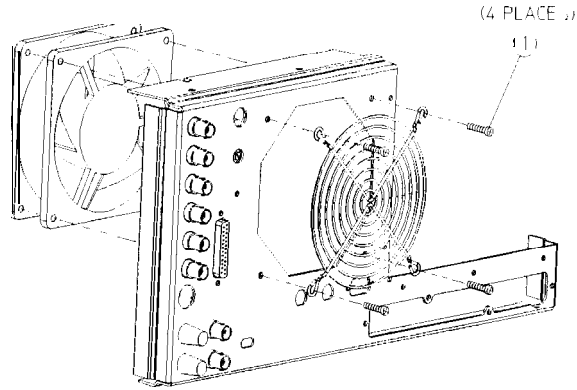
1. Remove the rear panel (refer to “Rear Panel Assembly” in this chapter).
2. Remove the four screws (item 1) that secure the fan and fan cover to the rear panel.

Replacement

1. Reverse the order of the removal procedure.

Note	The fan should be installed so that the direction of the air flow is away from the instrument. There is an arrow on the fan chassis indicating the air flow direction.
-------------	--

B1 Fan Assembly



sb067d

Post-Repair Procedures

The following tables list the additional service procedures which you must perform to ensure that the instrument is working correctly, following the replacement of an assembly. These procedures can be located in either Chapter 2 or Chapter 3.

Perform the procedures in the order that they are listed in the table.

Table 14-1. Related Service Procedures (1 of 4)

Replaced Assembly	Adjustments/ Correction Constants (Ch. 3)	Verification (Ch. 2)
41 Front Panel Keyboard	None	Internal Test 0 Internal Test 12 Internal Test 23 Internal Test 24
42 Front Panel Processor	None	Internal Test 0 Internal Test 12 Internal Test 23
44/A5/A6 Second Converter	None	System Verification
A52 Pulse Generator	Output Power Adjustments	System Verification
A8 Post Regulator	None	Internal Test 0 Check A8 test point voltages
A7 CPU ¹	A7 Jumper/Switch Positions Load Firmware* CC Retrieval Serial Number CC (Test 49) Option Number CC (Test 50) Display Intensity CC (Test 45) Analog Bus CC (Test 44) Source Pretune CC (Test 43) IF Amplifier CC (Test 47) EEPROM Backup Disk	Power Level Test Dynamic Range Test or System Verification

¹ If you have **an** EEPROM backup disk available, you only need to perform the **first** five tests **listed**.

² **Only** for instruments with **firmware** revisions **7.xx** and above.

Table 14-1. Related Service Procedures (2 of 4)

Replaced Assembly	Adjustments/ Correction constants (ch. 3)	Verification (Ch. 2)
A9 Source Control	None	System Verification
A10 Digital IF	A7 Jumper/Switch Positions Analog Bus CC (Test 44) IF Amplifier CC (Test 47)	Dynamic Range Test System Verification Internal Test 17 Internal Test 18 Internal Test 19 or System Verification
All Phase Lock	A7 Jumper/Switch Positions Analog Bus CC (Test 44) Source Pretune CC (Test 43)	Frequency Range and Accuracy or System Verification
A12 Reference	A7 Jumper/Switch Positions Reference Assembly VCO Tune Frequency Accuracy	Frequency Range and Accuracy
A13 Fractional-N (Analog)	A7 Jumper/Switch Positions Analog Bus CC (Test 44) Fractional-N Spur Avoidance and FM Sideband Adjustment	Internal Test 20 Frequency Range and Accuracy
A14 Fractional-N (Digital)	A7 Jumper/Switch Positions Analog Bus CC (Test 44)	Frequency Range and Accuracy Internal Test 20 or System Verification
A15 Preregulator	None	Self-Test [†]
A16 Rear Panel Interface	None	Internal Test 13, Rear Panel
A17 Motherboard	None	Self-Test [†]
† These tests are located in Chapter 4, "Start Troubleshooting Here."		

Table 14-1. Related Service Procedures (3 of 4)

Replaced Assembly	Adjustments/ Correction Constants (Ch. 8)	Verification (Ch. 2)
A18 Display	None	None
A19 Graphics System Processor	None	Observation of Display Tests 59–76*
A51 Test Set Interface	None	Operation Check†
A53 Low Band Assembly	Output Power Adjustments	Power Level Test Frequency Range and Accuracy
A54 YIG2 20-40 GHz (HP 8722D Only)	Source Pretune	Power Level Test Frequency Range and Accuracy
A55 YIG1 2.4-20 GHz	Source Pretune	Power Level Test Frequency Range and Accuracy
A56 Lower Front Panel Assembly	None	Observation (watch LEDs when switching from S11 to S22)
A57 Fixed Oscillator	Output Power Adjustments	Power Level Test Frequency Range and Accuracy
A58 M/A/D/S	Output Power Adjustments	Power Level Test
A59 Source Interface	Output Power Adjustments	Power Level Test
A60/61 DC Bias Tees	None	System Verification
<p>* These tests are located in Chapter 6, "Digital Control Troubleshooting." † These checks are located in Chapter 4, "Start Troubleshooting Here."</p>		

Table 14-1. Related Service Procedures (4 of 4)

Replaced Assembly	Adjustments/ Correction Constants (Ch. 3)	Verification (Ch. 2)
A62/A63 Directional Couplers	None	System Verification
A64 R1 Sampler	Sampler Check Power Adjustment	System Verification Power Level Test
A64 R2 Sampler (Option 400 Only)	Sampler Check† Power Adjustment	System Verification Power Level Test
A65 A Sampler	Sampler Check	System Verification
A66 B Sampler	Sampler Check	System Verification
A68 6 dB Attenuator	None	Operation Check
A69 Step Attenuator	None	Operation Check
S1 Switch (HP 8722D Only)	None	Operation Check
S2/S3 Switches	None	Operation Check
S4 Transfer Switch	None	Operation Check
† These checks are located in Chapter 4, "Start Troubleshooting Here. "		

Safety and Licensing

Notice

The information contained in this document is subject to change without notice.

Hewlett-Packard makes no warranty of any kind with regard to this material, including but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this material.

Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology, to the extent **allowed** by the Institute's calibration facility, and to the calibration facilities of other International Standards Organization members.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office.

Shipment for Service

If you are sending the instrument to Hewlett-Packard for service, ship the analyzer to the nearest HP service center for repair, including a description of any failed test and any error message. Ship the analyzer, using the original or comparable anti-static packaging materials. A listing of Hewlett-Packard sales and service offices is provided on the next page.

Table 15-1. Hewlett-Packard Sales and Service Offices

UNITED STATES		
Instrument Support Center Hewlett-Packard Company (800) 403-0801		
EUROPEAN FIELD OPERATIONS		
Headquarters Hewlett-Packard S.A. 150, Route du Nant-d'Avril 1217 Meyrin P/Geneva Switzerland (4122) 780.8111	France Hewlett-Packard France 1 Avenue Du Canada Zone D'Activite De Courtaboeuf F-91947 Les Ulis Cedex France (33 1) 69 82 60 60	Germany Hewlett-Packard GmbH Hewlett-Packard Strasse 61352 Bad Homburg v.d.H Germany (49 6172) 16-0
Great Britain Hewlett-Packard Ltd. Eskdale Road , Winnersh Triangle Wokingham , Berkshire RG41 5DZ England (4.4 734) 696622		
INTERCON FIELD OPERATIONS		
Headquarters Hewlett-Packard Company 3495 Deer Creek Road Palo Alto, California, USA 94304-1316 (416) 857-5027	Australia Hewlett-Packard Australia Ltd. 31-41 Joseph Street Blackburn, Victoria 3130 (61 3) 895-2895	Canada Hewlett-Packard (Canada) Ltd. 17500 South Service Road Trans-Canada Highway Kirkland, Quebec H9J 2X8 Canada (514) 697-4232
China China Hewlett-Packard Company 38 Bei San Huan X1 Road Shuang Yu Shu Hai Dian District Beijing , china (86 1) 256-8888	Japan Hewlett-Packard Japan, Ltd. 9-1 Takakura-Cho , Hachioji Tokyo 192, Japan (81 426) 60-2111	Singapore Hewlett-Packard Singapore (Pte.) Ltd. 150 Beach Road #29-00 Gateway West Singapore 0718 (65) 291-9088
Taiwan Hewlett-Packard Taiwan 8th Floor , H-P Building 337 Fu Hsing North Road Taipei, Taiwan (886 2) 7129404		

Safety Symbols

The following safety symbols are used throughout this manual. Familiarize yourself with each of the symbols and its meaning before operating this instrument.

Caution Caution denotes a hazard. It calls attention to a procedure that, if not correctly performed or adhered to, would result in damage to or destruction of the instrument. Do not proceed beyond a caution note until the indicated conditions are fully understood and met.

Warning **Warning** denotes a hazard. It calls attention to a procedure which, if not correctly performed or adhered to, could result in injury or loss of life. Do not proceed beyond a warning note until the indicated conditions are fully understood and met.

Instrument Markings



The instruction documentation symbol. The product is marked with this symbol when it is necessary for the user to refer to the instructions in the documentation.

“CE” The CE mark is a registered trademark of the European Community. (If accompanied by a year, it is when the design was proven.)

“ISM1-A” This is a symbol of an Industrial Scientific and Medical Group 1 Class A product.

“CSA” The CSA mark is a registered trademark of the Canadian Standards Association.

General Safety Considerations

Safety Earth Ground

Warning This is a Safety Class I product (provided with a protective earthing ground incorporated in the power cord). The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. Any interruption of the protective conductor, inside or outside the instrument, is likely to make the instrument dangerous. Intentional interruption is prohibited.

Before Applying Power

Caution The front panel LINE switch disconnects the mains circuits from the mains supply after the EMC **filters** and before other parts of the instrument.

Caution This product is designed for use in Installation Category **II** and Pollution Degree 2 per **IEC** 1010 and 664 respectively.

Caution Make sure that the analyzer line voltage selector switch is set to the voltage of the power supply and the correct fuse is installed.

Caution If this product is to be energized via an autotransformer make sure the common terminal is connected to the neutral (grounded side of the mains supply).

Servicing

Warning No operator serviceable parts inside. Refer servicing to qualified personnel. To prevent electrical shock, do not remove covers.

Warning **These** servicing instructions are for use by qualified personnel only. To avoid electrical shock, do not perform **any** servicing unless you are qualified to do so.

Warning The opening of covers or removal of parts is likely to expose dangerous voltages. Disconnect the instrument from all voltage sources while it is being opened.

Warning Adjustments described in this document may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Warning The power cord is connected to internal capacitors that may remain live for 5 seconds after disconnecting the plug from its power supply.

Warning For continued protection against **fire** hazard replace line fuse only with same type and rating (3 A 250 V **F**). The use of other fuses or material is prohibited.

Compliance with German **FTZ** Emissions Requirements

This network analyzer complies with German **FTZ 526/527** Radiated Emissions and Conducted Emission requirements.

Compliance with German Noise Requirements

This is to declare that this instrument is in conformance with the German Regulation on Noise Declaration for Machines (Laermangabe nach der Maschinenlaermverordnung -3. GSGV Deutschland).

Acoustic Noise Emission/Geraeuschemission	
LpA<70 dB	Lpa<70 dB
Operator Position	am Arbeitsplatz
Normal Operation per ISO 7779	normaler Betrieb nach DIN 45635 t. 19

Determining System Measurement Uncertainties

In any measurement, certain measurement errors associated with the system add uncertainty to the measured results. This uncertainty defines how accurately a device under test (DUT) can be measured.

Network analysis measurement errors can be separated into two types: raw and residual. The raw error terms are the errors associated with the uncorrected system that are called systematic (repeatable), random (non-repeatable), and drift errors. The residual error terms are the errors that remain after a measurement calibration.

The error correction procedure, also called measurement calibration, measures a set of calibration devices with known characteristics. It uses the measurement results to effectively remove systematic errors, using the vector math capabilities of the analyzer. The residual systematic errors remain after error correction, primarily due to the limitations of how accurately the electrical characteristics of the calibration devices can be **defined** and determined. Also, the random (non-repeatable) and drift errors, cannot be corrected because they cannot be quantified and measured during the measurement calibration and device measurement. However, the effects of random errors can be reduced through averaging. Random errors, that occur during a measurement calibration, are part of the error correction and become systematic errors when the calibration is turned on. For this reason, it is best to use a large number of averages during measurement calibration to reduce to the effect of the random errors. The averaging may then be reduced for device measurement. The residual systematic errors along with the random and drift errors continue to affect measurements after **error correction**, adding an uncertainty to the measurement results. Therefore, measurement uncertainty is defined as the combination of the residual systematic (repeatable), random (non-repeatable), and drift errors in the measurement system after error correction.

The following measurement uncertainty equations and system error models (flowgraphs) show the relationship of the systematic, random, and drift errors. These are useful for predicting overall measurement performance.

Sources of Measurement Errors

Sources of Systematic Errors

The residual (after measurement calibration) systematic errors result from imperfections in the calibration standards, the connector interface, the interconnecting cables, and the instrumentation. All measurements are affected by dynamic accuracy and frequency error effects. For reflection measurements, the associated residual errors are effective directivity, effective source match, and effective reflection tracking. For transmission measurements, the additional residual errors are effective crosstalk, effective load match, and effective transmission tracking.

The listing below shows the abbreviations used for residual systematic errors that are in the error models and uncertainty equations.

- Efd, Erd = effective directivity
- Efs, Ers = effective source match
- Efr, Err = effective reflection tracking
- Etc, Erc = effective crosstalk
- Efl, Erl = effective load match
- Eft, Ert = effective transmission tracking
- Crm, Ctm = cable stability (**deg./GHz**)
- Abl, Ab2 = dynamic accuracy
- F = frequency

The sources for dynamic accuracy error effects are from errors during internal self-calibration routines, gain compression in the microwave frequency converter (sampler) at high signal levels, errors generated in the synchronous detectors, localized non-linearities in the IF **filter** system, and from **LO** leakage into the IF signal paths.

Sources of Random Errors

The random error sources are noise, connector repeatability and dynamic accuracy. There are two types of noise in any measurement system: low level noise (noise floor) and high level noise (phase noise of the source).

Low level noise is the broadband noise floor of the receiver which can be reduced through averaging or by changing the IF bandwidth.

High level noise or jitter of the trace data is due to the noise floor and the phase noise of the **LO** source inside the test set.

Connector repeatability is the random variation encountered when connecting a pair of RF connectors. Variations in both reflection and transmission can be observed.

The listing below shows the abbreviations used for random errors in the error models and uncertainty equations.

- Rnt = raw noise on trace (rms)
- Rnf = raw noise on floor (rms)
- Cr1 = port 1 connector reflection repeatability error
- Crt1 = port 1 connector transmission repeatability error
- Crr2 = port 2 connector **reflection** repeatability error
- Crt2 = port 2 connector transmission repeatability error

Sources of Drift Errors

Drift has two categories: frequency drift of the signal source and instrumentation drift. Instrumentation drift affects the magnitude and phase of both reflection and transmission measurements.

The primary causes for instrumentation drift are the thermal expansion characteristics of the interconnecting cables within the test set and the conversion stability of the microwave frequency converter.

The list below shows the drift errors in the error models and uncertainty equations.

- Dmxbx, Dmsax = drift magnitude
- Dpxbx, Dpsax = drift phase
- Dpfbx, Dpfsax = drift phase/f

Sources of Additional Measurement Errors

Two additional categories of measurement errors are connection techniques and contact surfaces.

The connection techniques category includes torque limits, flush setting of sliding load center conductors, and handling procedures for **beadless** airlines.

The contact surfaces category includes cleaning procedures, scratches, worn plating, and rough seating.

These types of errors are not accounted for in the uncertainty analysis.

Measurement Uncertainty Equations

Any measurement result is the vector sum of the actual test device response plus all error terms. The precise effect of each error term depends on its magnitude and phase relationship to the actual test device response. When the phase of an error response is not known, phase is assumed to be worst case (-180° to $+180^\circ$). Random errors such as noise and connector repeatability are generally combined in a root-sum-of-the-squares (RSS) manner.

Due to the complexity of the calculations, the performance verification/specifications software calculates the system measurement uncertainty. The following equations are representative of the equations the performance verification/specifications software uses to generate the system measurement uncertainty plots and tables.

Reflection Uncertainty Equations

Total Reflection Magnitude Uncertainty (Erm)

An analysis of the error model in Figure A-1 yields an equation for the reflection magnitude uncertainty. The equation contains all of the first order terms and the significant second order terms. The terms under the radical are random in character and are combined on an RSS basis. The terms in the systematic error group are combined on a worst case basis. In all cases, the error terms and the S-parameters are treated as linear absolute magnitudes.

Reflection magnitude uncertainty (forward direction) =

$$Erm = Systematic + \sqrt{(Random)^2 + (Drift\ and\ Stability)^2}$$

$$Systematic = Efd + Efr S11 + Efs S11^2 + S21 S12 Efl + Abl S11$$

$$Random = \sqrt{(Cr)^2 + (Rr)^2 + (Nr)^2}$$

$$Cr = \sqrt{(Crm1)^2 + (2Ctm1S11)^2 + (Crm1S11)^2 + (Crm2S21S12)^2}$$

$$Rr = \sqrt{(Crr1 + 2Crt1S11 + Crr1S11^2)^2 + (Crr2S21S12)^2}$$

$$Nr = \sqrt{(EfmtS11)^2 + Efnf^2}$$

$$Drift\ and\ Stability = Dmlbl S11$$

where

- Efnt = effective noise on trace
- Efnf = effective noise floor
- Crtl = connector repeatability (transmission)
- Crrl = connector repeatability (reflection)
- Ctml = cable 1 transmission magnitude stability
- Crml = cable 1 reflection magnitude stability
- Crm2 = cable 2 reflection magnitude stability
- Dmsl = drift magnitude/°C source to port 1
- Efs = effective source match error
- Efr = effective reflection tracking error
- Efl = effective load match error
- Efd = effective directivity error
- Crr2 = Connector repeatability (reflection)

The detailed equation for each of the previous terms is derived from the signal flow model, located at the end of this appendix.

Reflection Phase Uncertainty (Erp)

Reflection phase uncertainty is determined from a comparison of the magnitude uncertainty with the test signal magnitude. The worst case phase angle is computed, This result is combined with the error terms related to thermal drift of the total system, port 1 cable stability, and phase dynamic accuracy.

$$Erp = \text{Arcsin} \left(\frac{Erm}{S11} \right) + 2Cpf1 \times f + Dpsl + Dpfs1 \times f$$

where

Cpfl = cable phase/frequency port 1

Dpsl = drift phase/degree source to port 1

Dpfs1 = drift phase/degree/frequency source to port 1

Transmission Uncertainty Equations

Transmission Magnitude Uncertainty (Etm)

An analysis of the error model, located at the end of this appendix, yields an equation for the transmission magnitude uncertainty. The equation contains all of the **first** order terms and some of the significant second order terms. The terms under the radical are random in character and are combined on an RSS basis. The terms in the systematic error group are combined on a worst case basis. In **all** cases, the error terms are treated as **linear** absolute magnitudes.

$$\text{Transmission magnitude uncertainty (forward direction)} = Etm =$$

$$Ert = \text{Systematic} + \sqrt{(\text{Random})^2 + (\text{Drift and Stability})^2}$$

$$\text{Systematic} = Efc + (Eft + EfsS11 + EflS22 + EfsEflS21S12 + Ab2) S21$$

$$\text{Random} = \sqrt{(Ct)^2 + (Rt)^2 + (Nt)^2}$$

$$Ct = S21\sqrt{(Ctm1)^2 + (Ctm2)^2 + (Crm1S11)^2 + (Crm2S22)^2}$$

$$Rt = S21\sqrt{(Crt1)^2 + (Crt2)^2 + (Crr1S11)^2 + (Crr2S22)^2}$$

$$Nt = \sqrt{(EfntS21)^2 + Efnf^2}$$

$$\text{Drift and Stability} = Dm2b2S21$$

where

Crt2 = Connector repeatability (transmission) port 2

Crr2 = Connector repeatability (reflection) port 2

Efnt = effective noise on trace

Efnf = effective noise floor

Crr1 = connector repeatability (reflection)

Crt1 = connector repeatability (transmission)

Ctm1 = cable 1 transmission magnitude stability

Ctm2 = cable 2 reflection magnitude stability

Crm2 = cable 2 reflection magnitude stability

Dm2b2 = drift **magnitude**/°C source to port

Efs = effective source match error

Eft = effective transmission tracking error

Efl = effective load match error

Efc = effective crosstalk error

The detailed equation for each of the above terms is derived from the signal flow model, located at the end of this appendix.

Transmission Phase Uncertainty (**Etp**)

Transmission phase uncertainty is calculated from a comparison of the magnitude uncertainty with the test signal magnitude. The worst case phase angle is computed. This result is combined with the error terms related to phase dynamic accuracy, cable phase stability, and thermal drift of the **total** system.

$$Etp = \text{Arcsin} \left(\frac{Ert}{S21} \right) + Cpf1 \times f + Cpf2 \times f + Dpsl + Dpfsl \times f$$

where

Cpf1 = Cable phase/frequency port 1

Cpf2 = Cable phase/frequency port 2

Dpsl = drift phase/degree source to port 1

Dpfsl = drift phase/degree/frequency source to port 1

Dynamic Accuracy

On the following page is a typical dynamic accuracy and noise curve for the analyzer. This curve is based on statistical samples of units **built** at the factory with an IF BW of 10 Hz.

Since this curve combines the effects of dynamic accuracy and noise, if used in uncertainty calculations, the effects of the noise terms in the corresponding equations can be eliminated.

$$\text{Dynamic Accuracy (linear)} = 10^{\frac{\pm \text{DynAcc(dB)}}{20}} \pm 1$$

$$\text{Dynamic Accuracy (dB)} = 20 \log(1 \pm \text{Dynamic Accuracy (linear)})$$

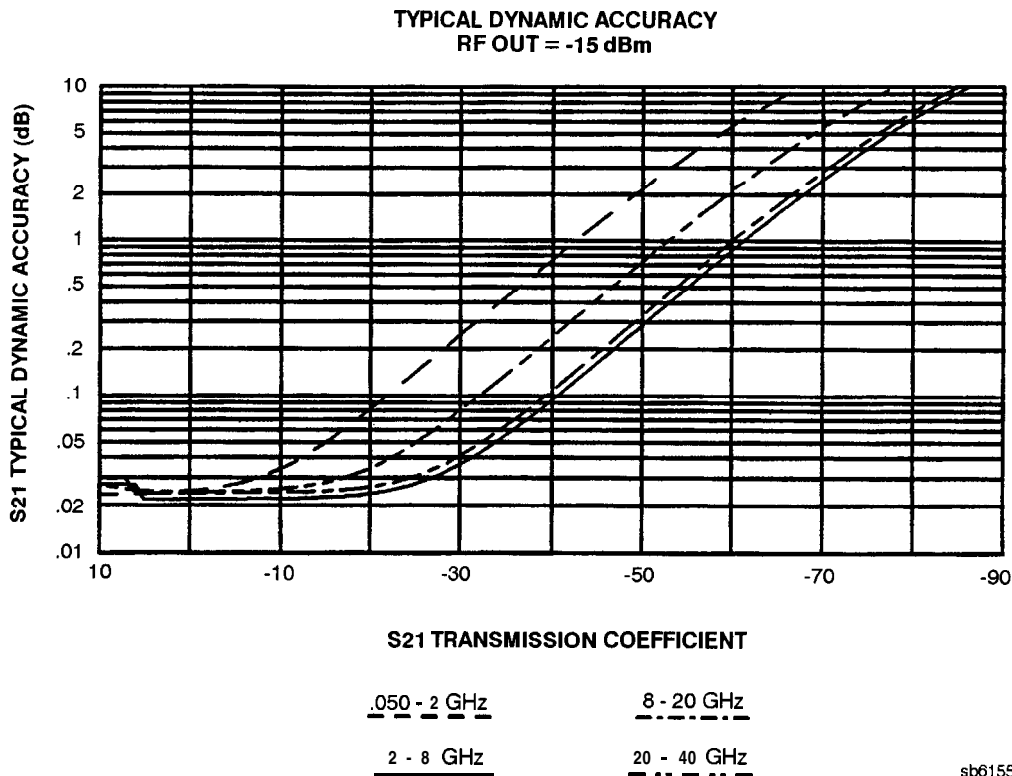


Figure A-1. Typical Dynamic Accuracy

Determining Expected System Performance

Use the uncertainty equations, dynamic accuracy calculations in this appendix, and tables of system performance values from the “Specifications and Measurement Uncertainties” chapter in the *HP 8719D/20D/22D Network Analyzer User’s Guide* to calculate the expected system performance. The following pages explain how to determine the residual errors of a particular system and combine them to obtain total error-corrected residual uncertainty values, using worksheets provided. The uncertainty graphs in the user’s guide are examples of the results that can be calculated using this information.

Procedures

Use the measurement uncertainty worksheet to calculate the residual uncertainty in transmission and reflection measurements. Determine the linear values of the residual error terms and the nominal linear S-parameter data of the device under test as described below and enter these values in the worksheets. Then use the instructions and equations in the worksheets to combine the residual errors for total system uncertainty performance. The resulting total measurement uncertainty **values** have a confidence factor of 99.9%.

S-parameter Values. Convert the S-parameters of the test device to their absolute linear terms.

Noise Floor and Crosstalk. If a full **2-port** calibration is performed, the residual crosstalk term can be ignored. Connect an impedance-matched load to each of the test ports and measure **S21** or **S12**. Use the statistic function to measure the mean **value** of the trace. Use this **value** plus one standard deviation as the noise floor value of your system.

Dynamic Accuracy. Determine the absolute linear magnitude dynamic accuracy from the dynamic accuracy graph (see **Figure A-1**).

Other Error Terms. Depending on the connector type in your system, refer to residual error specifications in the “Specifications and Measurement Uncertainties” chapter *in* the *HP 8719D/20D/22D Network Analyzer User’s Guide*, and the “Characteristic **values Table**” in this chapter to **find** the absolute linear magnitude of the remaining error terms.

Combining Error Terms. Combine the above terms using the reflection or transmission uncertainty equation in the worksheets.

Characteristic **Values Table**

	7 mm	3.5 mm	Type-N	2.4 mm
Crr1 = Port 1 Reflection Connector Repeat	-65 dB	-60 dB	-60 dB	-60 dB
Crr2=Port 2	-65 dB	-60 dB	-60 dB	-60 dB
Crtl =Port 1 Transmission Connector Repeat	-65 dB	-60 dB	-60 dB	-60 dB
Crt2=Port 2	-65 dB	-60 dB	-60 dB	-60 dB
Crm 1-Cable Refl Mag Stability Port 1	-60 dB	-54 dB	-60 dB	-50 dB
Crm2-Cable Refl Mag Stability Port 2	-60 dB	-54 dB	-60 dB	-50 dB
Ctm 1 -Cable Tran Mag Stability Port 1	±0.03 dB	±0.03 dB	±0.01 dB	±0.03 dB
Ctm2-Cable Tran Mag Stability Port 2	±0.03 dB	±0.03 dB	±0.01 dB	±0.03 dB
Cpf 1 -Cable Phase Stability Port 1 & Port 2	±0.09°/GHz	±0.09°/GHz	±0.1°/GHz	±0.09°/GHz
D_{ms1,2}-Magnitude Drift	0.0015°/°C	0.0015°/°C	0.0015°/°C	0.0015°/°C
D_{ps1,2}-Phase Drift	0.01°/°C	0.01°/°C	0.01°/°C	0.01°/°C
D_{psf1,2}-Phase Drift with Temp & Frequency	0.15°/°C	0.15°/°C	0.15°/°C	0.15°/°C

Measurement Uncertainty Worksheet (1 of 3)

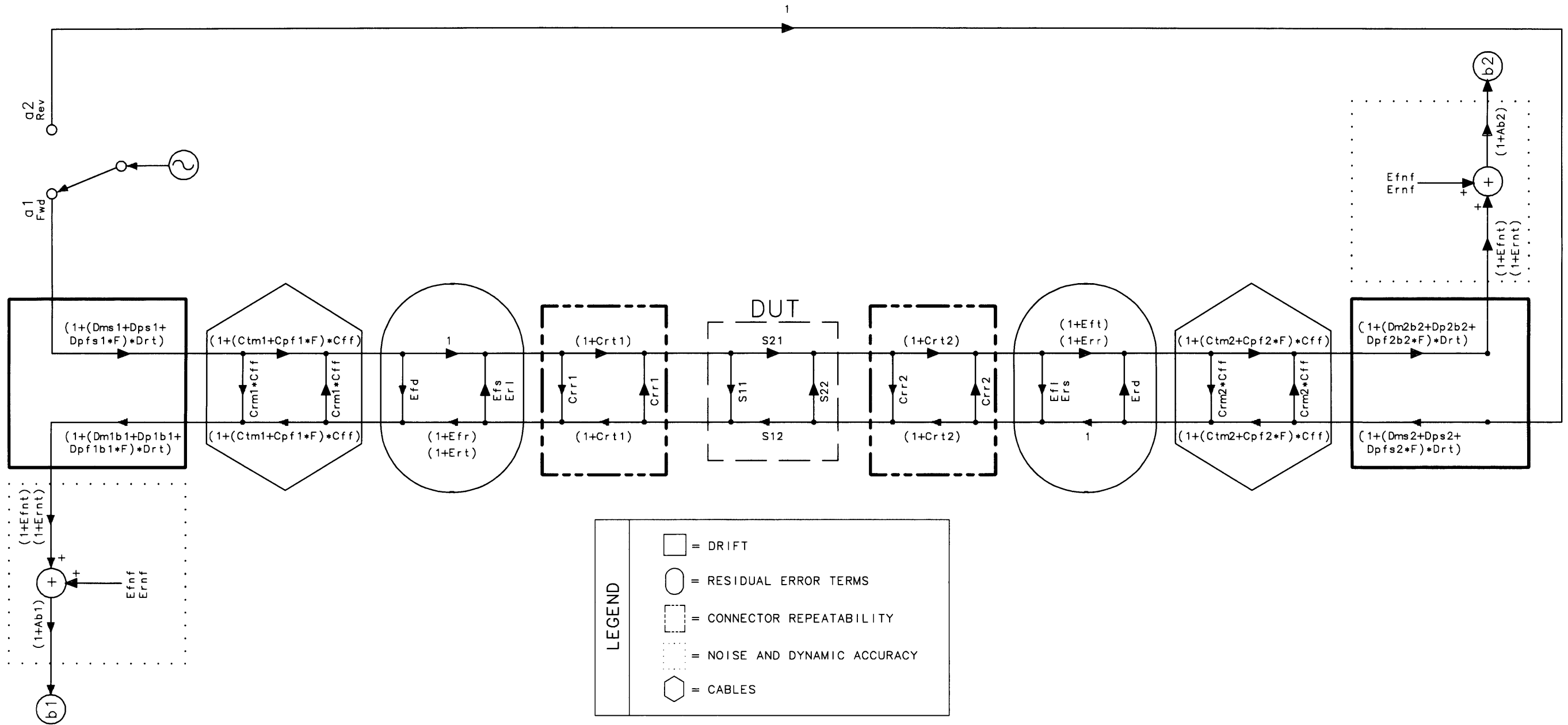
Error Term	Symbol	dB Value	Linear Value
S₁₁	S₁₁		
S₂₁	S₂₁		
S₁₂	S₁₂		
S₂₂	S₂₂		
Directivity	E_{fd}		
Reflection Tracking	E_{fr}		
Source Match	E_{fs}		
Load Match	E_{fl}		
Transmission Tracking	E_{ft}		
Effective Crosstalk	E_{fc}		
Dynamic Accuracy (Magnitude)	A_{b1}, A_{b2}		
Noise Floor	E_{tnf}		
High Level Noise	E_{nt}		
Connector Reflection Repeatability Port 1	C_{rr1}		
Connector Transmission Repeatability Port 1	C_{rt1}		
Magnitude Drift Due to Temperature	D_{ms1,2}		
Phase Drift Due to Temperature	D_{ps1,2}		
Phase Drift Due to Temperature and Frequency	D_{pf1,2}		
Cable Reflection Stability	C_{rm1}		
Cable Transmission Stability	C_{rm2}		
Connector Reflection Repeatability Port 2	C_{rr2}		
Connector Transmission Repeatability Port 2	C_{rt2}		
Cable Phase/Frequency Port 1	C_{pf1}		
Cable Phase/Frequency Port 2	C_{pf2}		

Measurement Uncertainty Worksheet (2 of 3)

Magnitude Combine Systematic Errors. In the space provided, enter the appropriate linear values from the list of errors. Then combine these errors to obtain the total sum of systematic errors.	
E_{fd} $E_f \times S_{11}$ $E_{fs} \times S_{11} \times S_{11}$ $E_{fl} \times S_{21} \times S_{12}$ $A_{b1} \times S_{11}$ Subtotal: $k + l + m + n + o$	$\underline{\quad} = \underline{\quad}$ (k) $\underline{\quad} \times \underline{\quad} = \underline{\quad}$ (l) $\underline{\quad} \times \underline{\quad} \times \underline{\quad} = \underline{\quad}$ (m) $\underline{\quad} \times \underline{\quad} \times \underline{\quad} = \underline{\quad}$ (n) $\underline{\quad} \times \underline{\quad} = \underline{\quad}$ (o) $\underline{\quad} + \underline{\quad} + \underline{\quad} + \underline{\quad} + \underline{\quad} = \underline{\quad}$ (S)
Combine Random Errors. In the space provided, enter the appropriate linear values from the list of errors. Then combine these errors in an RSS fashion to obtain a total sum of the random errors.	
$(E_{flt} \times S_{11})^2 + E_{mf}^2$ $(C_{m1} + 2 \times C_{m1} \times S_{11} + C_{m1} \times S_{11}^2)^2$ $+ (C_{m2} \times S_{21} \times S_{12})^2$ $C_{m1}^2 + (2 \times C_{m1} \times S_{11})^2 +$ $(C_{m1} \times S_{11})^2 + (C_{m1} \times S_{11})^2 +$ $(C_{m2} \times S_{21} \times S_{12})^2$ $(D_{mb1} \times S_{11})^2$ $\sqrt{w^2 + x^2 + y^2 + z^2}$ Subtotal: $S + R$	$(\underline{\quad} \times \underline{\quad})^2 + \underline{\quad} = \underline{\quad}$ (w^2) $(\underline{\quad} + 2 \times \underline{\quad} \times \underline{\quad} + \underline{\quad} \times \underline{\quad}^2)^2$ $+ (\underline{\quad} \times \underline{\quad} \times \underline{\quad})^2 = \underline{\quad}$ (x^2) $\underline{\quad}^2 + (2 \times \underline{\quad} \times \underline{\quad})^2 +$ $(\underline{\quad} \times \underline{\quad})^2 + (\underline{\quad} \times \underline{\quad})^2$ $+ (\underline{\quad} \times \underline{\quad} \times \underline{\quad}) = \underline{\quad}$ (y^2) $(\underline{\quad} \times \underline{\quad})^2 = \underline{\quad}$ (z^2) $\sqrt{\underline{\quad} + \underline{\quad} + \underline{\quad} + \underline{\quad}} = \underline{\quad}$ (R) $\underline{\quad} + \underline{\quad} = \underline{\quad}$ (V_r)
Total Magnitude Errors:	
$E_{m(\text{linear})} = V_r$ $E_{m(\text{log})} = \text{Log}(1 \pm E_m/S_{11})$	$\underline{\quad} = \underline{\quad}$ $20 \text{ Log}(1 \pm \underline{\quad}/\underline{\quad}) = \underline{\quad} \text{ dB}$
Phase	
$E_{rp} = \text{Arcsin}(E_m/S_{11}) + 2 \times C_{pfl} \times f$ $+ D_{ps1} + D_{pfs1} \times f$	$\text{Arcsin}(\underline{\quad}/\underline{\quad}) + 2 \times \underline{\quad} + \underline{\quad} + \underline{\quad} = \underline{\quad} \text{ degrees}$

Measurement Uncertainty Worksheet (3 of 3)

Magnitude Combine Systematic Errors. In the space provided, enter the appropriate linear values from the list of errors. Then combine these errors to obtain the total sum of systematic errors.	
E_{fc} $E_{ft} \times S_{21}$ $E_{fs} \times S_{11} \times S_{21}$ $E_{ft} \times S_{22} \times S_{21}$ $E_{fs} \times E_{ft} \times S_{21}^2 \times S_{12}$ $A_{b2} \times S_{21}$ Subtotal: k + l + m + n + o	$\underline{\hspace{2cm}} = \underline{\hspace{2cm}}$ (k) $\underline{\hspace{2cm}} \times \underline{\hspace{2cm}} = \underline{\hspace{2cm}}$ (l) $\underline{\hspace{2cm}} \times \underline{\hspace{2cm}} \times \underline{\hspace{2cm}} = \underline{\hspace{2cm}}$ (m) $\underline{\hspace{2cm}} \times \underline{\hspace{2cm}} \times \underline{\hspace{2cm}} = \underline{\hspace{2cm}}$ (n) $\underline{\hspace{2cm}} \times \underline{\hspace{2cm}} \times \underline{\hspace{2cm}} \times \underline{\hspace{2cm}} = \underline{\hspace{2cm}}$ (o) $\underline{\hspace{2cm}} \times \underline{\hspace{2cm}} = \underline{\hspace{2cm}}$ (p) $\underline{\hspace{2cm}} + \underline{\hspace{2cm}} + \underline{\hspace{2cm}} + \underline{\hspace{2cm}} + \underline{\hspace{2cm}} = \underline{\hspace{2cm}}$ (S)
Combine Random Errors. In the space provided, enter the appropriate linear values from the list of errors. Then combine these errors in an RSS fashion to obtain a total sum of the random errors.	
$(E_{fnt} \times S_{21})^2 + E_{fnr}^2$ $S_{21}^2 (C_{rt1}^2 + C_{rt2}^2 + (C_{rt1} \times S_{11})^2 + (C_{rt2} \times S_{22})^2)$ $S_{21}^2 (C_{tm1}^2 + C_{tm2}^2 + (C_{tm1} \times S_{11})^2 + (C_{tm2} \times S_{22})^2)$ $(D_{m2b2} \times S_{21})^2$ $\sqrt{w^2 + 2x + 2y + 2z}$ Subtotal: S + R	$(\underline{\hspace{2cm}} \times \underline{\hspace{2cm}})^2 \times \underline{\hspace{2cm}}^2 = \underline{\hspace{2cm}}$ (w ²) $\underline{\hspace{2cm}}^2 (\underline{\hspace{2cm}}^2 + \underline{\hspace{2cm}}^2 + (\underline{\hspace{2cm}} \times \underline{\hspace{2cm}})^2 + (\underline{\hspace{2cm}} \times \underline{\hspace{2cm}})^2) = \underline{\hspace{2cm}}$ (x ²) $\underline{\hspace{2cm}}^2 (\underline{\hspace{2cm}}^2 + \underline{\hspace{2cm}}^2 + (\underline{\hspace{2cm}} \times \underline{\hspace{2cm}})^2 + (\underline{\hspace{2cm}} \times \underline{\hspace{2cm}})^2) = \underline{\hspace{2cm}}$ (y ²) $(\underline{\hspace{2cm}} \times \underline{\hspace{2cm}})^2 = \underline{\hspace{2cm}}$ (z ²) $\sqrt{\underline{\hspace{2cm}} + \underline{\hspace{2cm}} + \underline{\hspace{2cm}} + \underline{\hspace{2cm}}} = \underline{\hspace{2cm}}$ (R) $\underline{\hspace{2cm}} + \underline{\hspace{2cm}} = \underline{\hspace{2cm}}$ (V _r)
Total Magnitude Errors:	
$E_{rm}(\text{linear}) = V_r$ $E_{rm}(\text{log}) = \text{Log} (1 \pm E_{rm}/S_{11})$	$\underline{\hspace{2cm}} = \underline{\hspace{2cm}}$ $20 \text{ Log} (1 \pm \underline{\hspace{2cm}}/\underline{\hspace{2cm}}) = \underline{\hspace{2cm}}$ dB
Phase	
$E_{tp} = \text{Arcsin} (E_{rm}/S_{21}) + C_{pf1} \times f + C_{pt2} \times f + D_{ps1} + D_{pts1} \times f$	$\text{Arcsin} (\underline{\hspace{2cm}}/\underline{\hspace{2cm}}) + \underline{\hspace{2cm}} + \underline{\hspace{2cm}} + \underline{\hspace{2cm}} = \underline{\hspace{2cm}}$ degrees



sb6158d

ERROR MODEL FLOW CHART

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