Errata

Title & Document Type: 8018A Data Generator Operating and Service Manual

Manual Part Number: 08018-90003

Revision Date: 1980-11-01

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

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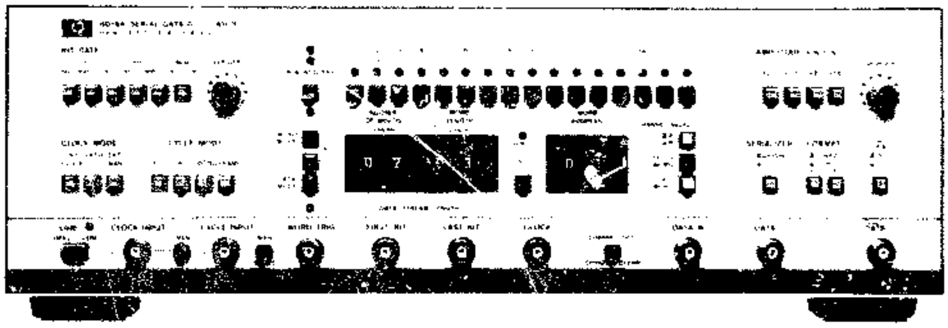
Agilent Technologies

HP 8018A

OPERATING AND SERVICE MANUAL

8018A
DATA GENERATOR



HEWLETT PACKARD

HP 8018A

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment, except that in the case of certain components listed in Section I of this manual, the warranty shall be for the specified period. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

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ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

8018A DATA GENERATOR

SERIAL NUMBERS

This manual applies directly to instruments with serial number 1826 G 00706 and higher. Any changes made in instruments having serial numbers higher than the above number will be found in a "Manual Changes" supplement supplied with this manual. Be sure to examine this supplement for any changes which apply to your instrument and record these changes in the manual. Any changes made in instruments having serial numbers lower than the above number can be found in the Backdating Section 7.

D-703 BÖBLINGEN, HERRENBERGER STR. 110,
FEDERAL REPUBLIC OF GERMANY

MANUAL PART NO. 08018-90003
Microfiche Part No. 08018-95003

Printed: Nov. 1980

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TABLES

ILLUSTRATIONS

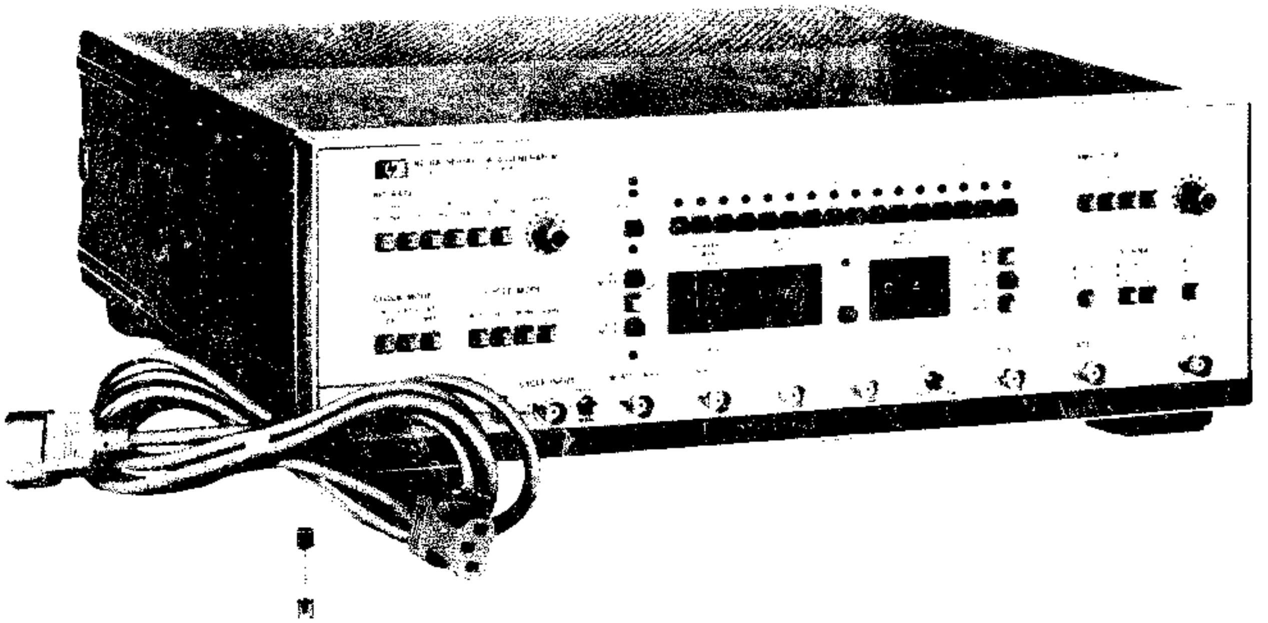
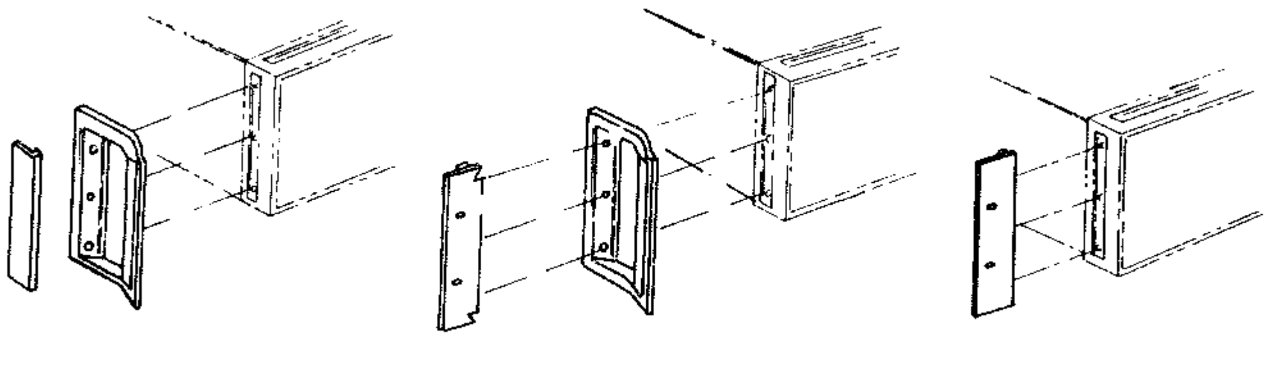


Figure 1–1. 8018A and supplied Accessories



Front handle
Order Option 907
(H.P. Part No.
5061–0089)

Rack flange with front handle
Order Option 909
(H.P. Part No.
5061–0083)

Rack flange
Order Option 908
(H.P. Part No.
5061–0077)

Figure 1–2. Available Rack Mounting Accessories

SECTION I
GENERAL INFORMATION

1–1 INTRODUCTION

1–2 This Operating and Service Manual contains information required to install, operate, test, adjust and service the Hewlett-Packard Model 8018A. Figure 1–1 shows the mainframe and accessories supplied. This section covers instrument identification, description, accessories, specifications, and other basic information.

1–3 A microfiche version of this manual is available on 4 x 6 inch microfilm transparencies (order number on title page). Each microfilm contains up to 60 photo-duplicates of the manual pages. The microfiche package also includes the latest Manual Changes supplement as well as all pertinent Service Notes.

1–4 SPECIFICATIONS

1–5 Instrument specifications are listed in Table 1–2. These specifications are the performance standards or limits against which the instrument is tested.

1–6 SAFETY CONSIDERATIONS

1–7 The Model 8018A is a Safety Class 1 instrument (it has an exposed metal chassis that is directly connected to earth via the power supply cable).

1–8 This operating and service manual contains information, cautions, and warnings which must be followed by the user to ensure safe operation and to maintain the instrument in a safe condition.

1–9 INSTRUMENTS COVERED BY MANUAL

1–10 Attached to the rear of this instrument is a serial number plate (Figure 1–3). The first four digits of the serial number only change when there is a significant change to the instrument. The last five digits are assigned to instruments sequentially. The contents of this manual apply directly to the instrument serial number quoted on the title page. For instruments with lower serial numbers, refer to the backdating information in Section 8 of this manual. For instruments with higher serial numbers, refer to the Manual Change sheets at the end of this manual. In addition to change information, the Manual Change sheets may contain information for correcting errors in the manual. To keep this manual as up-to-date and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Change supplement. The supplement for this manual is identified with this manual's print date and part number, both of which appear on this manual's title page. Complimentary copies of the supplement are available from Hewlett-Packard.

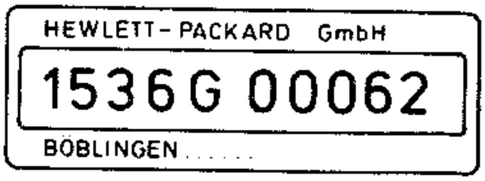


Figure 1–3. Serial Number Plate

1–11 DESCRIPTION

1–12 The 8018A is a dual channel, 50 MHz serial data generator with a 1024 bit memory capacity per channel. Memory content is freely programmable either from the front panel or via Option 001 (HP-IB), with a 'fetch' facility which returns data from the memory to front panel LEDs for checking or transferring. For outputting data from the memory, there are 4 main modes of operation:

- Word Mode (CHANNEL A and CHANNEL B)
- Data Mode (CHANNEL A and CHANNEL B)
- PRBS Mode (CHANNEL A ONLY)
- Mixed Mode (CHANNEL A ONLY)

In each mode, output levels of CHANNEL A can be selected to be CMOS, ECL or TTL compatible.

1–13 OPTIONS

1–14 8018A – Option 001: This enables the bit pattern to be programmed from a calculator, a computer, or any other controller which is compatible with the HP Interface Bus (HP-IB). Refer to Manual Part Number 08018–90002

1–15 8018A – Option 002: Provides a card reader which, together with Option 001, can program the memory content of the 8018A in approximately 2 seconds. Refer to Manual Part Number 08018–90002

1–16 8018A – Options 907, 908 and 909: Provide means of rack mounting the 8018A. Further details are given in Figure 1–2.

1–17 8018A – Option 910: Provides for two manuals to be delivered with the instrument.

1–18 All options will be delivered with the instrument if ordered with the instrument.

1–18 ACCESSORIES SUPPLIED

1–19 The 8018A is supplied complete with the following items (see Figure 1–1):

ITEM	HP PART NUMBER
1A Fuse for 230V operation	2110–0007
2A Fuse for 115V operation	2110–0303
Power cable	see Figure 2–2

1–20 ACCESSORIES AVAILABLE

1–21 Accessories available are listed as follows:

Model 15450A	4-Channel Adapter
Model 15451A	4-Channel TTL-CMDS Translator

1–22 RECOMMENDED TEST EQUIPMENT

1–23 Equipment required to maintain the model 1223A is listed in Table 1–1. Other equipment can be substituted if it meets or exceeds the critical specifications listed in the table.

INSTRUMENT TYPE	RECOMMENDED MODEL	REQUIRED CHARACTERISTICS	REQUIRED FOR
Electronic Counter	HP 5245 L	50 MHz; Start-Stop 50 MHz	A P
Scope Mainframe	HP 180C/182C		A P T
Vertical Plug-In	HP 1809A	100 MHz Bandwidth	A P T
Time Base Plug-In	HP 1825A		A P T
Sampling Plug-In	HP 1810A	1 GHz Bandwidth	A P T
50Ω Feedthrough	HP 10100C		A P
4 x BNC-BNC cable	HP 11170C	50Ω coax cable	A P
Logic Trigger	HP 1230A		P
Logic Analyzer	HP 1600S		T
Logic Probe ECL	HP 10525E		T
Logic Probe TTL/CMOS	HP 545A		T
Logic Pulser	HP 546A		T
Current Tracer	HP 547A		T
20 dB Coax-Attenuator		Wattage ≥ 4.5 Watts	A P T
Variable Transformer			A T
Digital Voltmeter	HP 34740A + 34702A	DC 10V–100V; Ω; AC	A T
Scope Probe			T
Pulse Generator	HP 8013B	50 MHz. Var Pulse Width, DC offset	P

Table 1–1. Recommended Test Equipment

NOTE: A = Adjustments
P = Performance Check
T = Troubleshooting

Table 1–2. Specifications

WORD AND DATA GENERATION

NUMBER OF CHANNELS: 2

CHANNEL LENGTH: 1024 bits (2048 bit total memory capacity).

WORD LENGTH (M): Variable from 3 to 99 bits (to 2048 bits in Data mode).

NUMBER OF WORDS (N): Variable from 1 to 99.

CHANNEL SERIALIZATION: Channels can be cascaded to extend Channel A length to 2048 bits.

DATA CONTENT: Programmable using front panel switches, or via optional HP-IB Interface.

DATA FORMATTING: RZ and NRZ formats independently selectable for A and B channels. Width in RZ format approximates width of clock output pulse.

DATA GENERATION MODES

WORD Mode: Data frame consists of N words of length M bits/word.

DATA Mode: Data frame consists of a continuous pattern of length between 3 and 2048 bits. Frame length is determined by 4-digit number set into thumbwheel switches.

PRBS Mode: Pseudo-Random Binary Sequence of length 2^n-1 bits is produced: n = 9, 10, 15, 20. Sequence is generated by a variable-length shift register with feedback as follows:

Number of shift register stages	Feedback at stages	Sequence length
9	5 and 9	511
10	7 and 10	1023
15	14 and 15	32767
20	17 and 20	1048575

MIXED Mode: As WORD mode with PRBS sequence inserted after every odd number word. Simulates preamble-data-postamble codes. Max bit rate 40 MHz.

CHANNEL SET/CLEAR: Fills selected data channel with ones or zeros.

OUTPUT CHARACTERISTICS (See Table for detailed specifications).

DATA A

CONTENT: Channel A memory, or A and B channel memories serialized.

AMPLITUDE: Variable in 3 ranges to 15 V, or ECL levels.

FORMAT: RZ NRZ selectable.

$\overline{\text{DATA A}}$

CONTENT: Data A inverted

OUTPUT CHARACTERISTICS: common with Data A.

DATA B

CONTENT: B channel memory

FORMAT: RZ NRZ independent from Data A

SYNCHRONIZING OUTPUTS

CLOCK: Occurs with each data bit.

FIRST BIT: Identifies first bit of data pattern.

LAST BIT: Identifies last bit of data pattern.

WORD TRIG: Identifies first bit of each word

PRBS TRIG (rear panel): Identifies each PRBS pattern (not in MIXED mode).

CLOCKING

INTERNAL

Bit Rate: 50 Hz to 50 MHz (40 MHz max in MIXED mode).

Jitter: 0.2% + 50 ps.

Controls: 5 decade ranges, 3-turn vernier adjusts within ranges

EXTERNAL CLOCK INPUT

Bit Rate: DC to 50 MHz (40 MHz in MIXED mode)

Trigger Level and Pulse Amplitude:

	EXT+	EXT−
Nom. Trigger Level	0.5 V	1.2 V
Min. Pulse Amplitude	1.0 V	0.8 V

Trigger Slope: Positive.

Minimum Pulse Width: 6 ns typical. (Variable-width source may be required in 30–50 MHz range).

Input Resistance: 50 Ω. Internal switch A3S1 increases resistance to 1 LS-TTL load in series with 300 Ω (max. bit rate 40 MHz, TTL levels, source impedance ≤ 4 kΩ).

Overload Protection: ± 7 V. Withstands 0–16 V when current limited to 20 mA.

MAN: Pushbutton switch enables single data bits.

Table 1–2 (cont'd)

Output Characteristics

These specifications apply when the outputs are all terminated by an external 50 Ω load.
Voltages from 50 Ω sources approximately double when working into open circuit.
All outputs are protected against short-circuit to ground and open circuit.

ECL levels internally adjustable.

	Adjust	Adjustment Range
Low level	A8R27	−1.7 to +0.8 V
Amplitude	A8R23	0.45 to 1.05 V
Low level drift:	≤ 10 % amplitude	

Parameter	Data A and $\overline{\text{Data A}}$			Data B	Clock	First Bit, Last Bit Word Synch	Prbs Trigger
	ECL	Variable					
Source resistance (typ) Ω	50	50	1 K	50	50	50	50
Low Level	See panel above	0 V ± 10 % amplitude		0 V ± 200 mV			
Amplitude, V.		1.25 to 7.5	2.5 to 15.0	≥ 2.4	≥ 2.4	≥ 1.2	≥ 1.2
Perturbation, % ampl	≤ 15 %	≤ 10 %	≤ 10 %	≤ 15 %	≤ 15 %	≤ 15 %	
Amplitude reduction at max bit rate	≤ 15 %	≤ 10 %	≤ 10 %	≤ 10 %	≤ 10 %	≤ 10 %	
Transition times	≤ 6 ns	≤ 6 ns	≤ 8 ns	≤ 6 ns	≤ 6 ns	≤ 6 ns	
Max bit rate	50 MHz	50 MHz	40 MHz	50 MHz	50 MHz	No operational restrictions	
Max external voltage	0 V to +16 V			2 V, +5 V (up to +16 V if current limited to 20 mA)			
Format/Width	RZ/NRZ selectable			RZ/NRZ selectable	50 ± 20 % of internal clock period		1 int clock period
Relation to clock output	± 3 ns			± 3 ns		± 3 ns	

CYCLE MODES

AUTO: Data frame recycles continuously.

SINGLE CYCLE:

BIT: Single bits are triggered by pulses at the CYCLE INPUT. If the input is held high, data bits are continuously generated. Data generation ceases when the input goes low. It continues from where it stopped when the input is returned to the high state.

WORD: Single words are triggered by pulses at the CYCLE INPUT. If the input is held high, words are continuously generated. When the input goes low, data generation ceases after completion of the current word. Data generation continues with the next word when the CYCLE INPUT is returned to the high state.

End bit: An end bit can be inserted after each word by setting internal switch A7S1 to 'ONE'. In NRZ operation, this provides a high level between words.

FRAME: Single data frames are generated by pulses at the cycle input. If the input is held high, frames are continuously generated. When the input goes low, the current frame is completed and data generation ceases.

End bit: An end bit can be inserted after each frame by setting internal switch A7S1 to 'ONE'. In NRZ operation, this provides a high level between frames.

CYCLE INPUT

Nominal Trigger Level: 0.5 V

Trigger Slope: Positive

Minimum Pulse Amplitude: 1.0 V

Minimum Pulse Width: 10 ns

Input Resistance: 50 Ω to ground. Internal switch A3S2 increases resistance to 1 LS-TTL load in series with 300 Ω (TTL levels, min pulse width 15 ns, source impedance ≤ 4 kΩ).

Overload Protection: ± 7 V. Withstands 0–16 V when current limited to 20 mA.

MAN: Switch enables outputting single bits, words, or frames.

RESET: Returns generator to bit 1.

GENERAL

POWER REQUIREMENTS: 100 V, 120 V, 220 V, or 240 V rms, +5 to −10 %, 48 to 440 Hz; 230 VA max.

Table 1–2 (cont'd)

ENVIRONMENTAL

OPERATING TEMPERATURE: 0 to 50°C

HUMIDITY: 95 % R.H., 0 to 40°C

STORAGE TEMPERATURE: 40 to +70°C

WEIGHT: Net 12 kg (26.5 lbs.) Shipping 16 kg (35.3 lbs.)

DIMENSIONS: 133 mm high, 426 mm wide, 422 mm deep (5.2 x 16.8 x 16.6 in).

ACCESSORIES SUPPLIED

Power Cord, Operating and Service Manual, Operating Card.

ACCESSORIES AVAILABLE

HP-IB Cables, for Option 001:	10631A	1 m
	10631B	2 m
	10631C	4 m
	10631D	0.5 m

OPTIONS

OPTION 001: HP-IB Interface. Permits loading the 8018A memory, word length, and number of words from any HP-IB compatible controller. Starting and stopping of data generation is also remotely controllable

OPTION 002: 15263A Card Reader. Enables fast set-up of 8018A. Data stored on punched or marked cards is loaded into the 8018A via its HP-IB interface. Requires option 001.

OPTION 907: Front Handle Kit (Part no. 5061–0089).

OPTION 908: Rack Mounting Kit (Part no. 5061–0077).

OPTION 909: Combined Front Handle and Rack Mounting Kit (Part no. 5061–0083).

OPTION 910: Extra 8018A Operating and Service Manual (Part no. 08018–90001).

Data subject to change.

SECTION II
INSTALLATION

2–1 INTRODUCTION

2–2 This section provides installation instructions for the instrument and its accessories. It also includes information about initial inspection and damage claims, preparation for use, and packaging, storage and shipment.

2–3 INITIAL INSPECTION

2–4 Inspect the shipping container for damage. If the container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. The contents of the shipment should be as shown in Figure 1–1 plus any accessories that were ordered with the instrument. Procedures for checking the electrical operation are given in Section 3. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the operator's checks, notify the nearest Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement without waiting for settlement.

2–5 PREPARATION FOR USE

2–6 Power Requirements

2–7 The instrument requires a power source of 100V, 120V, 220V or 240V (+5%, −10%) at a frequency of 48 to 66 Hz single phase. The maximum power consumption is 120V A.

2–8 Line Voltage Selection

CAUTION

BEFORE SWITCHING ON THIS INSTRUMENT make sure that the instrument is set to the local line voltage.

2–9 Figure 2–1 provides information for line voltage and fuse selection:

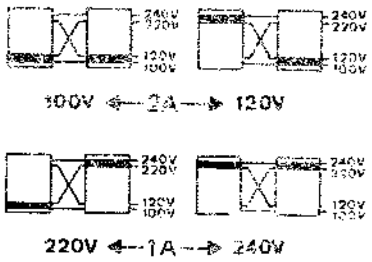


Figure 2–1. Switch Settings for the various Nominal Power-line Voltages

2–10 Power Cable

WARNING

To avoid the possibility of injury or death, the following precautions must be followed before the instrument is switched on:

a. If this instrument is to be energized via an autotransformer for voltage reduction, make sure that the common terminal is connected to the grounded pole of the power source.

b. The power cable plug shall only be inserted into a socket outlet provided with a protective ground contact. The protective action must not be negated by the use of an extension cord without a protective conductor.

c. Before switching on the instrument, the protective ground terminal of the instrument must be connected to a protective conductor of the power cable. This is verified by checking that the resistance between the instrument chassis and the front panels of all modules in the instrument and the ground pin of the power cable plug is zero ohms.

2–11 In accordance with international safety standards, this instrument is equipped with a three-wire power cable. When connected to an appropriate ac power receptacle, this cable grounds the instrument cabinet. The type of power cable shipped with each instrument depends on the country of destination. Refer to Figure 2–2 for the part number of the power cords available.

2–12 If the plug on the cable supplied does not fit your power outlet, then cut the cable at the plug end and connect a suitable plug. The plug should meet local safety requirements and include the following features:

Minimum current rating of 2A
Ground connection
Cable clamp.

The colour coding used in the cable will depend on the cable supplied (see Figure 2–2).

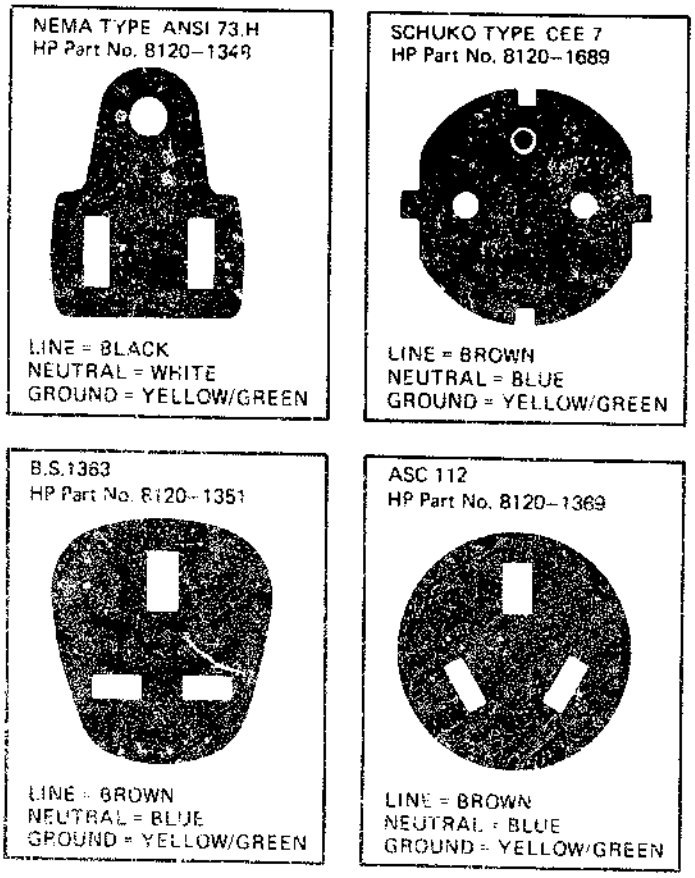


Figure 2–2. Power Cables Available: Plug Identification

2–13 Operating Environment

2–14 The instrument will operate within specifications when the ambient temperature is between 0°C and 55°C.

2–15 FRONT HANDLE/RACK MOUNTING

2–16 Figure 1–2 shows the possible handle/rack-mounting configurations. If handles are fitted and subsequently need to be removed, the plastic trim must first be taken off as shown in Figure 2–3.

Figure 2- 3. Removing Plastic Trim

2–17 CLAIMS AND REPACKAGING

2–18 Claims for Damage

2–19 If physical damage is evident or if the instrument does not meet specification when received, notify the carrier and the nearest Hewlett-Packard Sales/Service Office. The Sales/Service Office will arrange for repair or replacement of the unit without waiting for settlement of the claim against the carrier.

2–20 STORAGE AND SHIPMENT

2–21 The instrument can be stored or shipped at temperatures between –40°C and 75°C. The instrument should be protected from temperature extremes which cause condensation within the instrument.

2–22 If the instrument is to be shipped to a Hewlett-Packard Sales/Service Office, attach a tag showing owner, return address, model number and full serial number and the type of service required. The original shipping carton and packaging material may be re-usable but the Hewlett-Packard Sales/Service office will also provide information and recommendations on materials to be used if the original packing is not available or re-usable. General instructions for re-packing are as follows:

1. Wrap instrument in heavy paper or plastic.

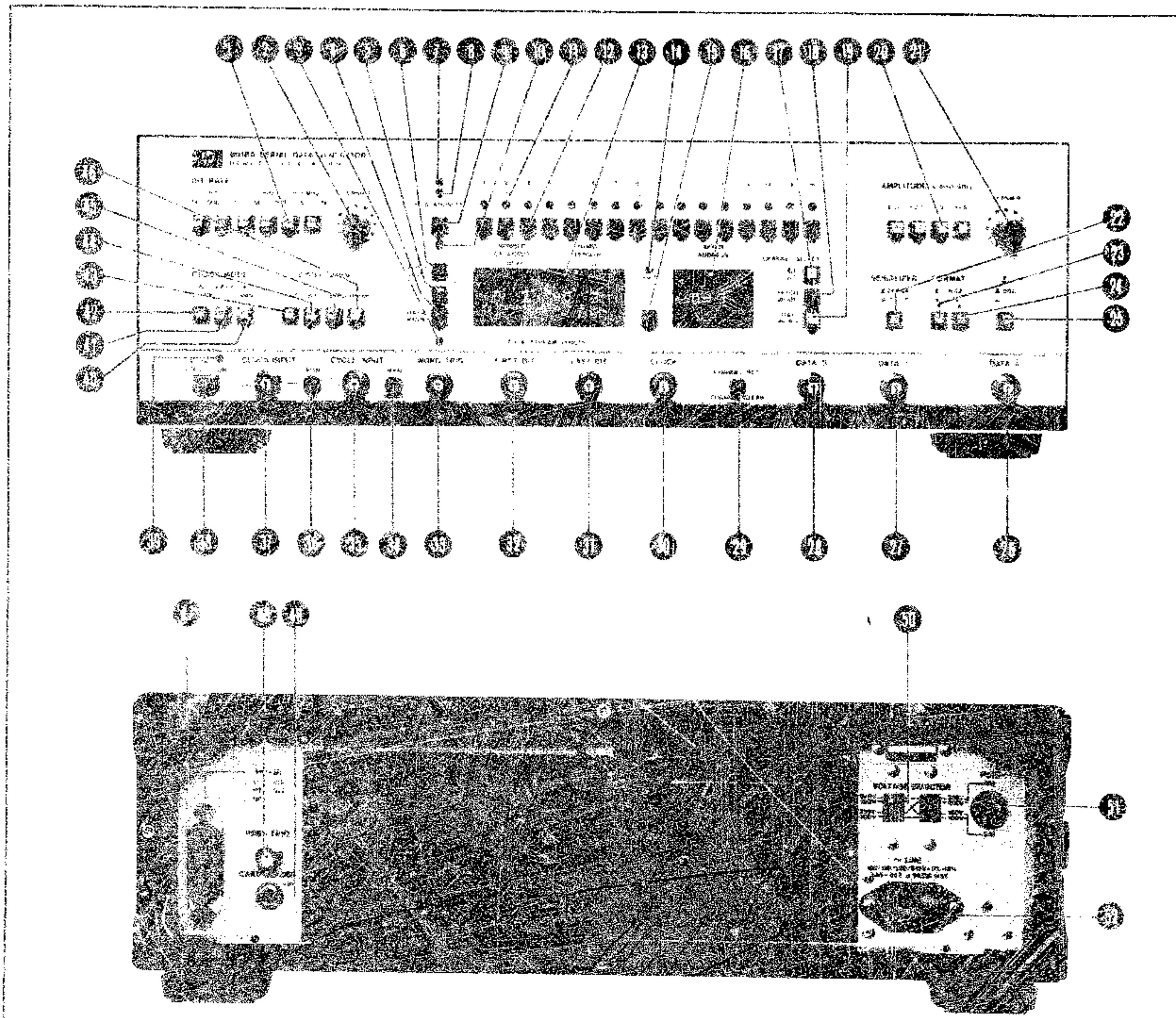
2. Use strong shipping container. A double wall carton made of 350-pound test material is adequate.

3. Use enough shock-absorbing material (3 to 4-inch layer) around all sides of instrument to provide firm cushion and prevent movement inside container. Protect control panel with cardboard.

4. Seal shipping container securely.

5. Mark shipping container FRAGILE to encourage careful handling.

6. In any correspondence, refer to instrument by model number and serial number.



1 **BIT RATE.** Mutually exclusive pushbuttons for selecting range of bit rate when INT CLOCK [illegible] selected. When EXT (+) or EXT (-) ([illegible] and [illegible]) selected, BIT RATE pushbuttons are disabled.

2 **VERNIER.** For continuous adjustment of the bit rate within the range selected at 1. Clockwise rotation increases the bit rate.

3 **DATA MODE LED.** Indicates that DATA MODE is selected and that thumbwheel switch 15 is used to set length of data stream.

4 **DATA MODE.** Pushbutton for selecting data to be outputted as a continuous stream of preselected length. This length can be set from 3 to 2048 bits by thumbwheel switch [illegible].

5 **PRBS.** Pushbutton for selecting data to be outputted as a pseudo-random binary sequence of length 2^n-1 bits. The factor 'n' is set by thumbwheel switch [illegible] to 9, 10, 15 or 20 (see also MIXED MODE).

Figure 3–1. Front and Rear Panel Controls, Connectors and Indicators.

(6) **WORD MODE.** Pushbutton for selecting data to be outputted as a frame consisting of N words of length M bits/word. N is set by the first two digits of thumbwheel switch (13), and M is set by the last two digits of the same switch. (See also MIXED MODE).

MIXED MODE. Selected by pressing WORD MODE and PRBS pushbuttons simultaneously. Data is then outputted as described in WORD MODE except that PRBS is inserted after every odd-numbered word.

(7) **1-16 ROW ADDRESS LED.** Indicates that pushbutton row (12) can be used to set bits 1-16 in a 32-bit word.

(8) **17-32 ROW ADDRESS LED.** Indicates that push-button row (12) can be used to set bits 17-32 in a 32-bit word.

(9) **ROW ADDRESS.** Pushbutton which determines whether bits '1-16' or '17-32' can be set by push-button row. (12). LED's (7) and (8) give a visual indication of which bit sequence is selected.

(10) **WORD MODE LED.** Indicates that WORD MODE is selected i.e. thumbwheel switch (13) is used to set NUMBER OF WORDS (first two digits) and WORD LENGTH (last two digits).

(11) **LED ROW.** Gives visual indication of the bit pattern being loaded or fetched. An illuminated LED indicates data bit is set to logic '1'.

(12) **DATA PROGRAMMING.** A row of pushbuttons used for setting a 16-bit buffer register, the set pattern being transferred to memory on pushing LOAD pushbutton. The set 16-bit word can be assigned to the first half or second half of a 32-bit word using ROW ADDRESS pushbutton (9). Visual indication of the set 16-bit pattern is given by LED row (11).

(13) **DATA FORMATTING THUMBWHEELS.** Switch whose function depends on the data generation mode selected. When WORD MODE or MIXED MODE is selected, then the first two digits set the number of words to be outputted; the last two digits set the number of bits in each word. When DATA MODE is selected, all four digits are used to set the data stream length for loading and outputting.

(14) **REMOTE LED** Provides visual indications that the 8018A is in the REMOTE state. In this state memory programming can only be accomplished via the HP-IB (i.e. front panel LOAD pushbutton disabled). Data formatting thumbwheel switches and the CYCLE INPUT function are also programmable.

(15) **LOCAL/RESET.** Returns the 8018A from REMOTE state to local (front panel) control.

(16) **WORD ADDRESS.** Thumbwheel switch for selecting the memory address to/from which data is loaded/fetched respectively.

(17) **CHANNEL SELECT.** Pushbutton which selects the channel for loading, fetching, setting and clearing.

(18) **FETCH WORD.** Operating this pushbutton recalls data from the memory address, selected by (16), to the LED register (11).

(19) **LOAD WORD.** Operating this pushbutton transfers data, set by pushbutton row (12), to the memory location selected by thumbwheel switch (16).

(20) **AMPLITUDE.** Mutually exclusive pushbuttons for selecting the amplitude of DATA A and $\overline{\text{DATA A}}$ outputs. Amplitude depends on source and load impedances. ECL pushbutton sets DATA A and $\overline{\text{DATA A}}$ outputs to ECL compatible levels (levels internally adjustable).

(21) **VERNIER.** For continuous adjustment of the amplitude selected, ECL selection excluded.

(22) **A PAR B/A SER B.** Pushbutton for configuring memory as two 1024 bit (2x1024/1x2048) channels (A and B) or one 2048 bit channel (A).

(23) **FORMAT B.** Selects RZ or NRZ format for DATA B output.

(24) **FORMAT A.** Selects RZ or NRZ format for DATA A and $\overline{\text{DATA A}}$ outputs.

(25) **Z_S** Sets the source impedance, 50 Ω or high Z, for DATA A and $\overline{\text{DATA A}}$ outputs. When ECL amplitude selected at (20), then ZS switch should be set to 50 Ω for true ECL levels.

(26) **$\overline{\text{DATA A}}$** BNC connector for outputting the complement of channel A data.

(27) **DATA A** BNC connector for outputting channel A data.

(28) **DATA B** BNC connector for outputting the channel B memory content.

(29) **CHANNEL SET / CHANNEL CLEAR.** Toggle switch for setting (logical 1's) or clearing (logical 0's) the complete memory content of the channel selected by (16).

(30) **CLOCK.** BNC connector for outputting the 8018A clock signal.

(31) **LAST BIT.** BNC connector for outputting an RZ pulse corresponding to the last bit of the data pattern.

(32) **FIRST BIT.** BNC connector for outputting an RZ pulse corresponding to the first bit of the data pattern.

(33) **WORD TRIGGER.** BNC connector for outputting an RZ pulse corresponding to the first bit of each word in WORD or MIXED mode.

(34) **RESET/MAN.** In MAN position, gives cycle command for data generation as defined by switches (44) (45) and (46) e.g. if BIT selected, then one bit is generated. Pressing this toggle switch to RESET ensures that the next bit delivered is the first bit of the data pattern.

(35) **CYCLE INPUT.** BNC connector for signal to trigger data generation in BIT, WORD or FRAME cycle mode.

(36) **MAN.** Pushbutton for providing a manual clock signal when MAN CLOCK MODE selected at (40).

(37) **CLOCK INPUT.** BNC connector for providing an external clock signal when EXT CLOCK MODE selected at (40) or (41).

(38) **LINE OFF/ON.** Switch for applying primary ac power to the instrument.

(39) **LINE LED.** Indicates when primary ac power is applied to the instrument.

(40) **EXT (–) / MAN.** Pushing this button enables the data generator to be clocked manually (via (36)) or by a negative external clock signal.

(41) **EXT (+).** Pushing this button enables the data generator to be clocked by an external positive clock signal.

(42) **INT CLOCK.** Pushing this button selects the internally generated clock signal for clocking the data generator.

(43) **AUTO.** When AUTO is selected, data is cycled continuously.

(44) **BIT.** Pressing this pushbutton enables data to be delivered bit by bit upon cycle commands applied to connector (35), or by pressing switch (34) to MAN.

(45) **WORD.** Pressing this pushbutton, enables data to be delivered word by word upon cycle commands to connector (35), or pressing switch (34) to MAN.

(46) **FRAME.** Pressing this pushbutton, enables data to be delivered frame by frame upon cycle commands to connector (35), or pressing switch (34) to MAN.

(47) **HP-IB.** Space for fitting the HP-IB remote connector when Option 001 included in instrument (see Appendix A).

(48) **PRBS TRIG.** BNC connector which outputs an NRZ pulse to identify the beginning of each PRBS pattern.

(49) **CARD READER.** +5V supply output connector for the Option 002 Card Reader.

(50) **VOLTAGE SELECTOR.** These switches connect the internal power transformer to accept the primary power source voltage. BOTH SWITCHES must be set to the position marked for power source being used.

(51) **FUSE.** Accepts standard fuses to provide instrument protection in case of current overload. A 1A slow-blow fuse must be used when operating from 240V/220V power source. A 2A fuse is used when operating from 100V/120V power source.

(52) **LINE.** A three-prong receptacle to provide chassis ground through the power cable for operator protection.

SECTION VIII
SERVICE

8–1 INTRODUCTION

8–2 This section contains the information to service the HP Model 8018A. The information includes theory of operation, troubleshooting, schematics, component layouts and block diagram.

8–3 The schematics and component layouts are organized as 'Service Sheets' which are identified by a large number within a square in the lower corners. A table relating these Service Sheets to board assemblies is given in Table 8–1. Schematic diagram symbols are given in Table 8–3.

Table 8–1. Index to Assemblies

Assembly	Service Sheet
A2 Control Board	2
A3 Bit Rate Board	3,4
A4 Data Format Board	6
A5 PRBS Board	7
A6 Memory Board	8, 9
A7 Sync Amplifier Board	11
A8 Output Amplifier Board	12
A9 Mother Board	5, 13
A10 Power Supply Board	14
A11 Distribution Board	2, 5
A12 Memory Extension Board	10
A13 Register Board	4, 12, 13
A14 LED Board	4, 7, 12, 13
A15 Trigger Board	3, 4, 6
A16 Mode Board	7
A17 Load Board	2
A18 RZ Board	2
A21 Fan Board	15
A29 Rectifier Board	14

8–4 SAFETY CONSIDERATIONS

8–5 This section contains warnings and cautions that must be followed for your protection and to avoid damage to the equipment:

WARNING

Maintenance described herein is performed with power supplied to the instrument and protective covers removed. Such maintenance should be performed only by service-trained personnel who are aware of the hazards involved (for example, fire and electrical shock). Where maintenance can be performed without power applied, the power should be removed.

When servicing is completed, the After Service Safety Check must be performed.

8–6 AFTER SERVICE SAFETY CHECK

8–7 Execute the following checks when servicing is completed.

3–8 Disconnect power cord from line. Visually inspect interior of instrument for any sign of abnormal internally generated heat, such as discolored printed circuit boards or components, damaged insulation, or evidence of arcing. Determine cause and remedy.

8–9 Check cabinet/ground pin continuity in accordance with IEC/VDE. Flex the power cord while making the measurement to detect any intermittent discontinuity. Check internal ground connections on boards and frame. Also check resistance of any front or rear panel ground terminals marked ⏚

8–10 Check cabinet/line isolation in accordance with IEC/VDE. Replace any component which results in a failure or refer to production Memo or Service Note issued by product division for alternate action.

8–11 Check line fuse to verify that the proper value is installed.

8–12 Check that safety covers are installed.

8–13 Check that all coaxial and flat cables inside are properly connected. Check that all boards and the heatsink on the chassis are properly connected. Verify that the board clamp is fitted.

8–14 Inform Hewlett-Packard (internally, the responsible product division) of any repeated failures in the above tests or any other safety features.

8–15 SERVICE BLOCKS (THEORY/ TROUBLESHOOTING)

8–16 The theory of operation and troubleshooting is divided into Service Blocks, each Service Block corresponding to a complete function within the 8018A. Service Block 1 deals with overall instrument troubleshooting, including a detailed block diagram of all HP 8018A functions. The purpose of the general instrument troubleshooting is to provide a fast means of isolating a fault down to a function. The Serviceman should then proceed to the Service Block providing detailed theory of operation and troubleshooting hints for that function. A table relating function to Service Block is given in Table 8–2.

Table 8–2. Index to Service Blocks

Service Block	Function
1	**Troubleshooting Hints**
2	**Control ASM**
3	**Rate Generation and External Cycle Inputs**
4	**Data Formatting and Cycling**
5	**Memory**
6	**Sync and Output Amplifiers**
7	**Parallel/Serial Loading**
8	**Power Supply**
A1–1	**HP-IB**

8–17 Tables and Figures within each Service Block are given three-digit codes e.g. Figure 8–3–1. The first digit refers to the Manual Section (8), the second digit to the Service Block and the third to the Figure number, e.g. Figure 8–3–1 means Section 8, Service Block 3, Figure 1.

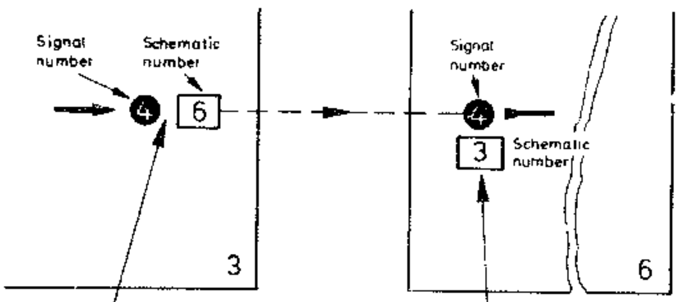
Table 8–2. Schematic Diagram Notes (1 of 2)

The following symbols conform, as far as possible, with ANSI Y32.2, IEEE No. 315 and ANSI Y32.14 (for the logic symbols). These standards should be consulted when further informations is required.

General

Units	Resistance values are in ohms, capacitance values in microfarads and inductance values in microhenries unless otherwise noted!
P/O	Part of
*	Asterisk denotes a factory selected value. The value shown is the nominal value.
	Encloses front panel nomenclature
	Encloses rear panel nomenclature
	Heavy line indicates signal path
	Heavy dashed line indicates primary feedback path
947	Wire colour code. Same as resistor colour code. First number is wire body colour.
	Wire or plug used as link.
	Test point in a circuit. Point may/may not be identified on P. C. board.
	Used with trimmer potentiometers or capacitors to indicate screwdriver adjustment.
	Direct connection to earth.
	Ground connection to instrument chassis or frame.
	Used when a number of common-return connections are at the same potential. If there is more than one such system in the same circuit, numbers are written in the triangles so that all connections with the same potential have the same number.
xV	Specific potential difference with respect to a potential reference level, eg. +10V

Schematic Referencing



These references on a signal leaving a schematic diagram indicate the signal destination. The circle contains the signal number and the square contains the number of the schematic to which that signal goes

These references on a signal entering a schematic diagram indicate the signal origin. The circle contains the signal number and the square contains the number of the schematic on which that signal originates

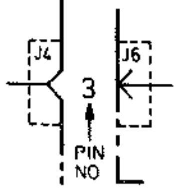
Components

	Normally open toggle switch. Circles (O) are used for the contacts to indicate a locking type switch.
	Spring return, 2-position transfer switch. Triangles (▲) are used for the contacts to indicate a non-locking type switch.
	2-position, 2-pole slide switch.
	Air cored inductor.
	Air cored transformer. The dot (•) is used, when necessary, to indicate instantaneous polarity.
	Iron core
	Ferrite core
bead	Ferrite bead
	Varactor diode
	Multi-junction diode
	Diode
	Zener diode
	Schottky diode
	Light Emitting Diode (LED)
	Photodiode
	Fuse
	Neon
	Filament lamp

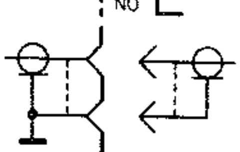
Table 8–2. Schematic Diagram Notes (2 of 2)

Terminals and Connectors

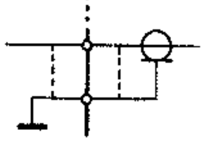
Soldered connection.



Example of fixed male and female connectors with plug and socket and contact designators, eg. P.C. board edge connector and socket.

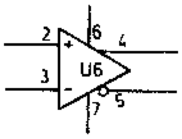


example of bulkhead mounted coaxial socket with free coaxial plug and cable.



example of coaxial cable with termination soldered to P. C. board.

Analog Symbols

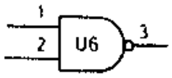


Operational amplifier

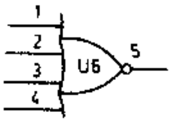
Voltage source

Current source

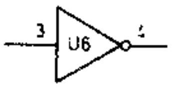
Logic Symbols



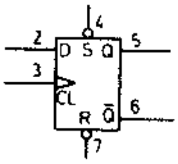
2-input NAND gate



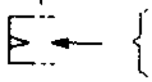
4-input NOR gate



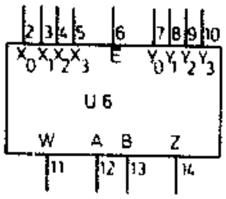
Inverter



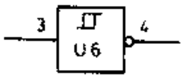
Flip-flop.



The dynamic indicator denotes that this is a dynamic input and operates on a transition, not a level.



Complex functions represented by rectangular box. Letters inside the rectangle indicate the function which may be further clarified by a truth table.



Schmitt trigger

Wired AND connection

Wired OR connection

SERVICE BLOCK 1
TROUBLESHOOTING HINTS

The purpose of the following troubleshooting hints is to provide a fast means of isolating a fault down to a function, as well as providing general information (e.g. mnemonic definitions) to aid understanding of the 8018A operation. For detailed theory of operation on a specific function, the serviceman should proceed to the associated Service Block, e.g. Service Block 2 for Control ASM.

In general, 8018A operation can be divided into two functional areas:

1. Data output and trigger signal generation
2. Data fetching and loading

The Algorithmic State Machine (ASM) on Board A2 is only activated when the LOAD or FETCH pushbuttons are operated, and is therefore only in use in the second of the above-mentioned functional areas.

Before down to component troubleshooting, first check front panel operation via the following checklist:

1. Any signal whatsoever at the data and sync outputs ?
2. Is it possible to change the sync signals via the thumbwheel switches ?
3. Are the sync signals correct in their timing relationships ?

If the output signals indicate a timing fault, check the rate generator on board A3, the word/address counters on board A4 , the sync amplifier on board A7 and output amplifier on board A8.

If the sync signals are correct, check the LOAD and FETCH functions.

General Troubleshooting

Use the following procedure for a fast ASM checkout:

Set the first bit in the first row to high [LED is lit] and press the LOAD pushbutton. If all other LED's glow, the ASM is working.

The following tips can aid a fast troubleshooting down to function:

1. Inspect the PC connectors, and if necessary, clean using a plastic eraser.
2. To ensure that data generation is not locked by the A2 control board, A2 can be removed. Connect a jumper from A3U7 pin 4 to ground, and set A3S2 to the TTL position. All sync signals are generated and a random data patterns is output.
3. When troubleshooting in the memory area, connect a jumper from A6U34 pin 5 to ground if board A6 is operated without board A12.
4. A12 can be hooked up in 'piggy-back' arrangement to A6 for troubleshooting purposes.
5. If switch A3S2 is set in position 300 Ω (TTL) and the External Cycle Input is not terminated, A3U15 pin 13 sees a high input. This makes it impossible to select BIT, WORD or FRAME CYCLE.

8018A Signal Mnemonics

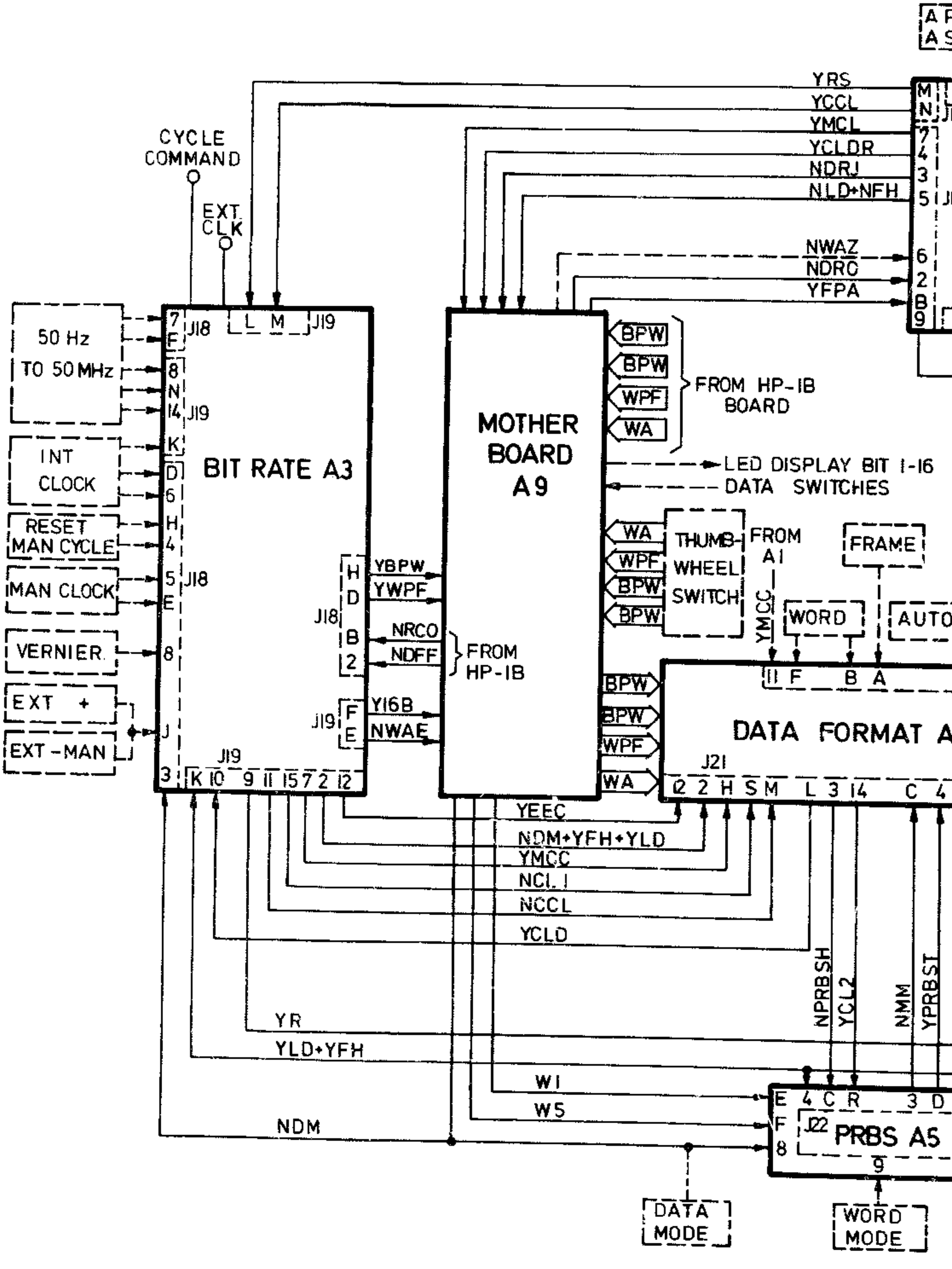
The following is a list of all the signal mnemonics to be found within the 8018A schematics, together with a short description for each mnemonic.

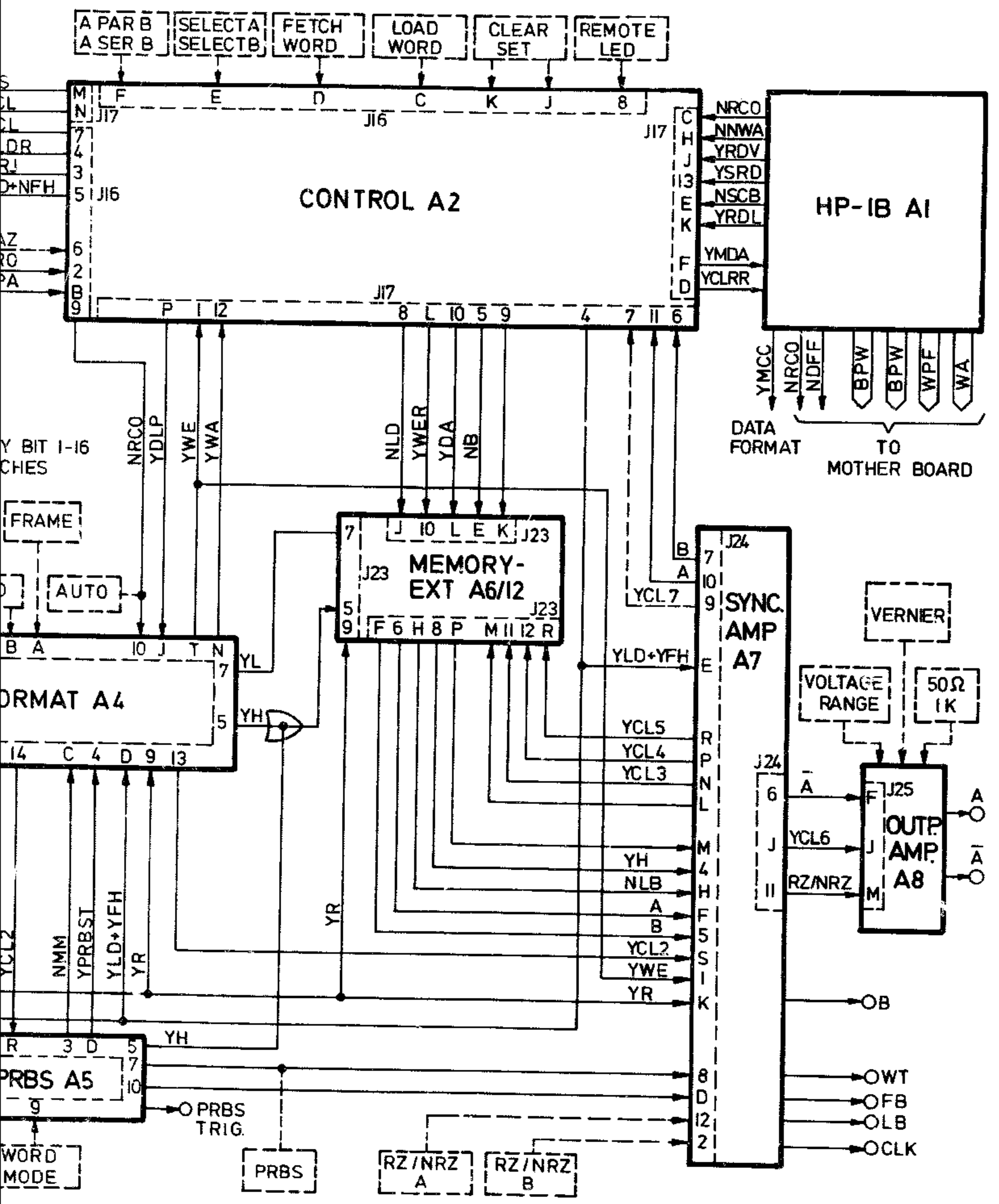
NOTE: In the schematics, each of the following mnemonics is preceeded by 'N' or 'Y'. 'N' indicates that the signal is true on a low state or low-going transition, 'Y' indicates that the signal is true on a high state or high-going transition.

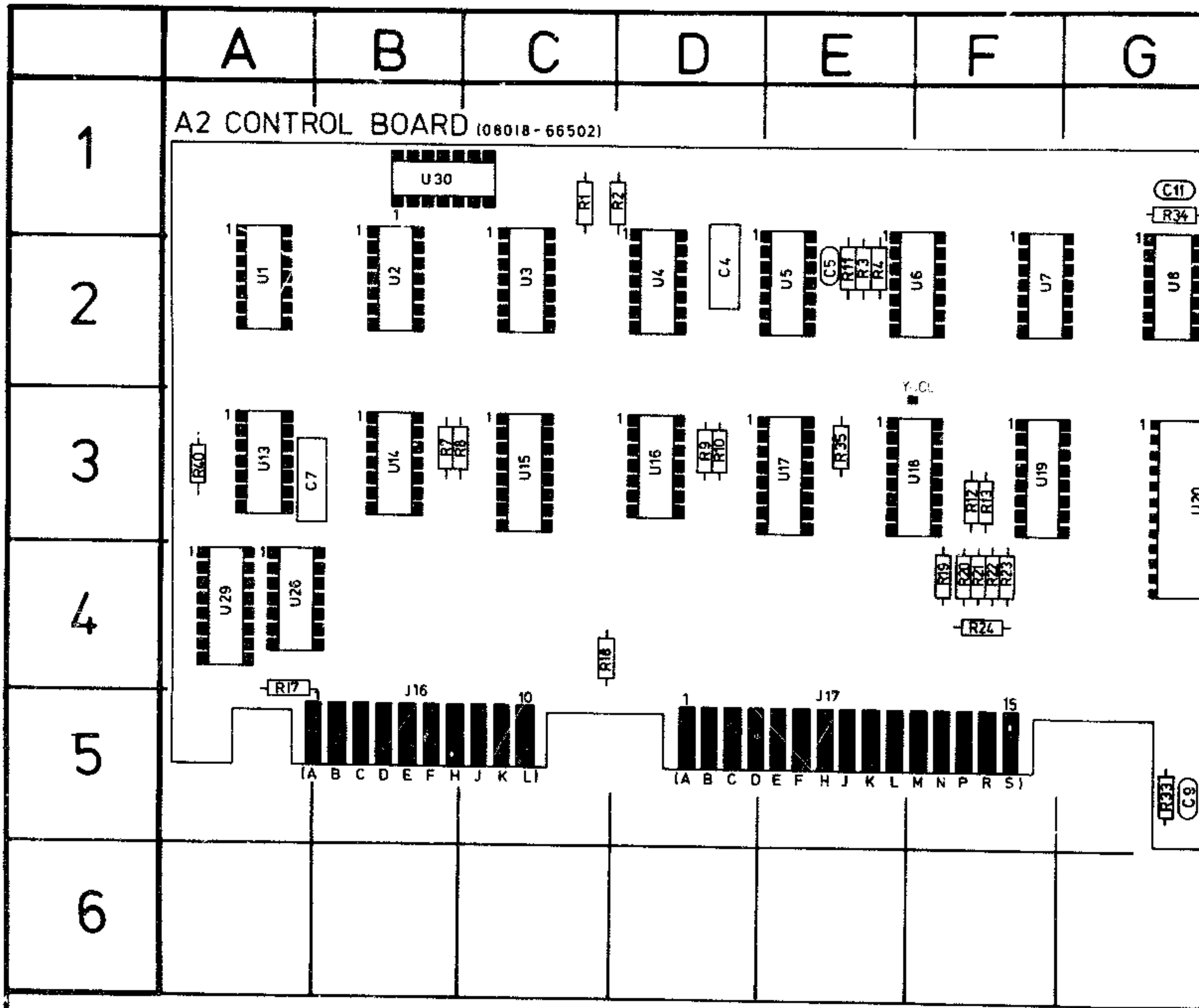
A	A-Channel Selected
ACD	Accept Data
ATN	Attention
AC	Auto Cycle
B	B-Channel Selected
BC	Bit Cycle
BPW	Bit per Word
1023	Bit 1023
1024	Bit 1024
1025	Bit 1025
CCL	Control Clock
CWA	Count Word Address
CL RR	Clock Remote Register
CLDR	Clock Data Register
CL1...	Clock 1...
CLD	Clock Disable
CC	Clear Counter U23
CL16	Clock 16 bit CTR
CR	Clear Register (Memory)
CHA	Channel A
DM	Data Mode
DA	Data (into RAM)
DFT	Data Format Trigger
DRI	Data Register Input
DAWNS	Disable Acceptor, Wait for New State
DRO	Data Register Output
DAV	Data Valid
DAC	Data Accepted
DFF	Data Format Follows
DLP	Disable Last Pulse
DFT	Data Format Trigger
DCL	Device Clear
ECC	External Cycle Command
FFS	Flip-Flop State
FH	Fetch
FPA	First Part Row Address
FC	Frame Cycle
GTL	Go to Local
H	Hold
IFC	Interface Clear
L	Last Bit
LAC	Listener Accepts Commands
LBY	Load Byte
LM	Load M-Words per Frame
LN	Load N-Bits per Word
LWA	Load Word Address
LLO	Local Lock Out
LOC	Local
LD	Load
LW	Load Word
LAD	Listener Accepts Data
M	M = Words per Frame
MDA	More Data
MLA	My Listen Address
MCC	Manual Cycle Command
MP1	Multiplexer
MP2	Multiplexer
MP3	Multiplexer
MCL	Manual Clock
MM	Mixed Mode
N	N =Bits per Word
NWA	New Word Address
NRDY	Not Ready for Data
NLD	Load
PAR	Parallel
PRBS	Pseudo Random Sequence
PRBSH	Pseudo Random Sequence Hold

PRBST	Pseudo Random Sequence Trigger
PON	Power On
Q	= Qualifier
R	Reset
RA	Read Address
RB 1–8	Read Bit 1–8
RBPW	Read Bit per Word
RCB	Reset Control Board
RCC	Remote Cycle Command
RCO	Remote Control
RD	Read
RDV	Remote Data Valid
RDL	Remote Data Line
RRD	Remain Read
RHS	Reset Whole System
RMDB	Reset More Data Binary
RS	Reset
RSA	Remote Start
RFD	Ready for Data
REN	Remote Enable
RC	Remote Cycle
RW1–8	Read Word 1–8
SCB	Select Channel B
SRD	Set Read
SHI	Shift Data (to instrument)
SMDB	Set More Data Binary
SBB	Set Blank Binary
STB	Set to B
SR	Set Register (Memory)
SITB	HP-IB Channel B Select
SDC	Set Device Clear
TFF	Toggle Flip-flop
UNL	Unlisten
WE	Word End
WAZ	Word Address Zero
WER	Write Enable RAM
WA	Word Address
WAE	Word Address Enable
WPF	Words per Frame
WT	Word Trigger
WM	Word Mode

WC	Word Cycle
WE1	Write Enable 1
WE2	Write Enable 2
WE3	Write Enable 3
WE4	Write Enable 4
16BE	16 BIT Enalbe
16	16 Bit

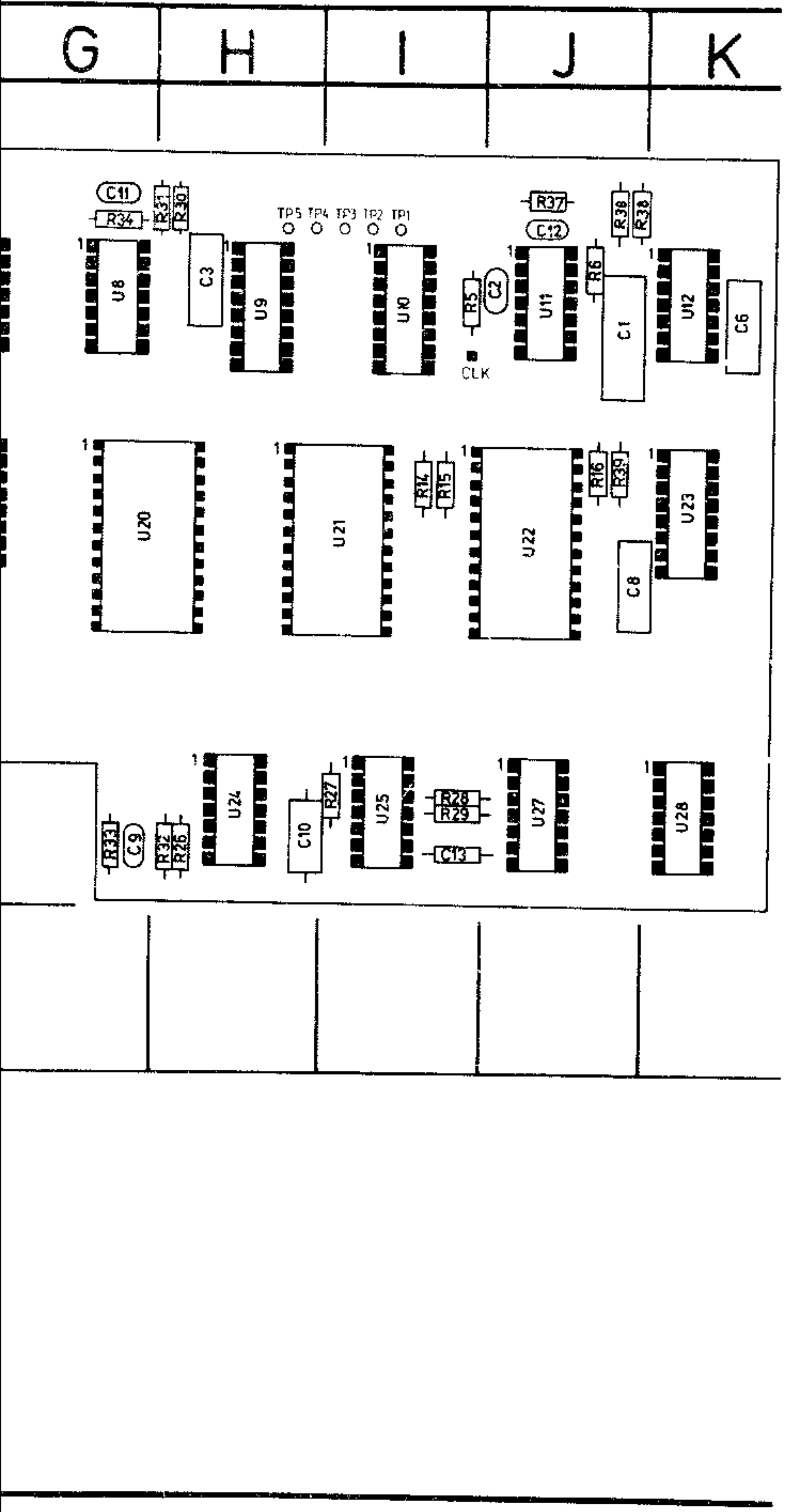

CYCLE COMMAND
EXT. CLK
50 Hz TO 50 MHz
INT CLOCK
RESET MAN CYCLE
MAN CLOCK
VERNIER
EXT +
EXT - MAN
BIT RATE A3
MOTHER BOARD A9
FROM HP-IB BOARD
LED DISPLAY BIT 1-16
DATA SWITCHES
THUMB-WHEEL SWITCH
FROM A1
FRAME
WORD
AUTO
DATA FORMAT A
PRBS A5
DATA MODE
WORD MODE
FROM HP-IB
YRS
YCCL
YMCL
YCLDR
NDRJ
NLD+NFH
NWAZ
NDRC
YFPA
YBPW
YWPF
NRCO
NDFF
Y16B
NWAE
YEEC
NDM+YFH+YLD
YMCC
NCL 1
NCCL
YCLD
YR
YLD+YFH
W1
W5
NDM
NPRBSH
YCL2
NMM
YPRBST
BPW
WPF
WA
J18
J19
J21
J22


A PAR B
A SER B
SELECT A
SELECT B
FETCH WORD
LOAD WORD
CLEAR SET
REMOTE LED
CONTROL A2
HP-IB A1
NRCO
NNWA
YRDV
YSRD
NSCB
YRDL
YMDA
YCLRR
YMCC
NDFF
BPW
WPF
WA
DATA FORMAT
TO MOTHER BOARD
Y BIT 1-16
CHES
NRCO
YDLP
YWE
YWA
NLD
YWER
YDA
NB
FRAME
AUTO
MEMORY-EXT A6/12
ORMAT A4
YL
YH
YR
SYNC. AMP A7
YLD+YFH
YCL5
YCL4
YCL3
YCL7
YH
NLB
A
B
YCL2
YWE
YR
VERNIER
VOLTAGE RANGE
50Ω 1K
OUTP. AMP. A8
YCL6
RZ/NRZ
NMM
YPRBST
YLD+YFH
YCL2
PRBS A5
PRBS TRIG.
WORD MODE
PRBS
RZ/NRZ A
RZ/NRZ B
OB
OWT
OFB
OLB
OCLK



A
B
C
D
E
F
G
1
2
3
4
5
6
A2 CONTROL BOARD (08018-66502)
U30
U1
U2
U3
U4
U5
U6
U7
U8
U13
U14
U15
U16
U17
U18
U19
U29
U26
C4
C5
C7
C9
C11
R1
R2
R3
R4
R7
R8
R9
R10
R11
R12
R13
R17
R18
R19
R20
R21
R22
R23
R24
R33
R34
R35
R40
J16
J17
(A B C D E F H J K L)
(A B C D E F H J K L M N P R S)

2



REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	J2	U5	E2
C2	J2	U6	E/F2
C3	H2	U7	F2
C4	D2	U8	G2
C5	E2	U9	H2
C6	K2	U10	I2
C7	A3	U11	Y2
C8	J/K 3/4	U12	K2
C9	G5	U13	A3
C10	H5	U14	B3
C11	G1	U15	C3
C12	J1	U16	D3
C13	I5	U17	E3
R1	C1	U18	E/F3
R2	C/D1	U19	F3
R3	E2	U20	G/H 3/4
R4	E2	U21	H/I 3/4
R5	I2	U22	J3/4
R6	J2	U23	K3
R7	B3	U24	H5
R8	B3	U25	I5
R9	D3	U26	A4
R10	D3	U27	J5
R11	E2	U28	K5
R12	F3	U29	A4
R13	F3	U30	B/C1
R14	I3	TP1	I1
R15	I3	TP2	I1
R16	J3	TP3	I1
R17	A5	TP4	I1
R18	C4	TP5	H1
R19	F4		
R20	F4		
R21	F4		
R22	F4		
R23	F4		
R24	F4		
R26	H5		
R27	I5		
R28	I5		
R29	I5		
R30	H1		
R31	G1		
R32	H5		
R33	G5		
R34	G1		
R35	E3		
R36	J1		
R37	J1		
R38	J1		
R39	J3		
R40	A3		
U1	A2		
U2	B2		
U3	C2		
U4	D2		

SERVICE BLOCK 2
CONTROL ASM A2 [2]

THEORY OF OPERATION

General

The ASM (Algorithmic State Machine) controls all data loading and fetching, whether by front panel operation or via HP-IB. A functional diagram of the ASM is given in Figure 8–2–1. In principle, the ASM comprises a 5-bit D Register with Clear (U10), a Read Only Memory (U9), a 16 to 1 Data Multiplexer/Selector with inverting output (U22), two 4-bit Instruction Decoder/Multiplexers (U20/U21) and a Clock Generator (U11 A/B).

The "power on circuit" (U11 D/C) clears the Register U10 during power on and ensures that the ASM starts with state address 00000.

The ROM U9 has 8 data outputs, where D5 to D8 are used to select the qualifier E0 to E15 of U22, and D1 to D4 are fed to D1 to D4 of U10 as part of the 'next state address'. The fifth and most significant bit of the 'next state address' is provided by the $\overline{W}$ output of U22, the logic state of this output being the inverse of the currently selected qualifier.

The inputs, therefore, of U10 indicate the 'next state address' (waiting for the next clock pulse), whereby the outputs indicate the currently selected state address of ROM U9. Address line A4 of U9 also selects instruction decoder U21 (A4 low) or instruction decoder U20 (A4 high), whereas address lines A0 to A3 select the instruction by switching one of the U21/U20 outputs to low.

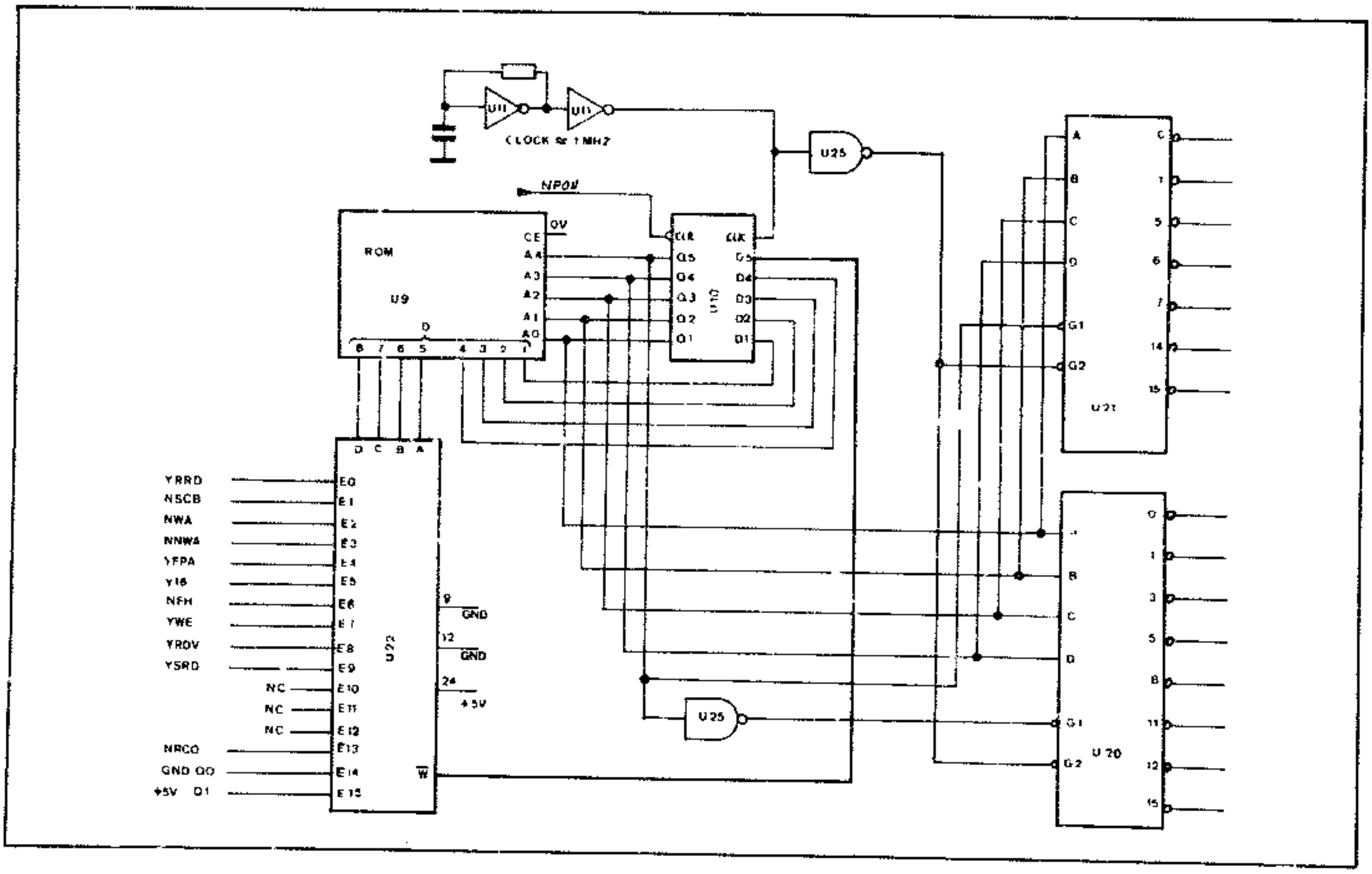


Figure 8–2–1. Functional diagram of ASM

ASM Qualifier Selection and State Addressing

After power-on, signal NPON is held low for several milliseconds to clear register U10 thus ensuring that the first state address for ROM U9 is 00000.

As can be seen from Table 8–2–1, the corresponding ROM output for state address 00000 (and for all state addresses) is divided into two groups i.e. D1 to D4, and D5 to D8. Outputs D5 to D8 are used for qualifier selection, and in this case are 0000, which selects the E0 (YRRD) input of U22. Outputs D1 to D4 provide the first 4 bits for the next state address, which again in this case are 0000. The fifth bit of the next state address is provided by the $\overline{W}$ output of U22. Should the qualifier E0 (YRRD) be true i.e. high, the $\overline{W}$ output is 0. (Note: the qualifier mnemonic of E0 is YRRD, the 'Y' at the beginning indicating that qualifier true is a logic high. Similarly, qualifier mnemonic beginning with N (e.g. NFH at input E6) indicates low true). On the next clock pulse at U10, therefore, the state address applied to ROM U9 remains at 00000, this cycle being repeated for as long as E0 remains true (high).

E0 goes low when FETCH, LOAD, CHANNEL SET or CHANNEL CLEAR is pressed, or when HP-IB is activated. With E0 low, output $\overline{W}$ goes high, thus changing the next state address at the input of U10 to 10000. When this address is clocked on to the ROM address lines, the outputs D5 to D8 select qualifier E1 (see Table 8–2–1). Depending on whether this qualifier is true or not, the next state address will either be 10001 (qualifier true) or 00001 (qualifier not true). For next state address 10001, the next qualifier to be selected by the ROM output will be E15 (see Table 8–2–1); if 00001 is the next state address, qualifier E2 will be selected.

Table 8–2–1: Qualifier Selection and State Addresses

STATE ADDRESS										QUALIFIER SELECTED		NEXT STATE ADDRESS (Qualifier True)					NEXT STATE ADDRESS (Qualifier Not True)				
A4	A3	A2	A1	A0	U9 U22	D8 D	D7 C	D6 B	D5 A		NAME	U22$\overline{W}$ (D6)	D4	D3	D2	D1	U22$\overline{W}$ (D5)	D4	D3	D2	D1
0	0	0	0	0		0	0	0	0	E0	YRRD	0	0	0	0	0	1	0	0	0	0
0	0	0	0	1		0	0	1	0	E2	NWA	1	0	0	1	0	0	0	0	1	0
0	0	0	1	0		1	1	1	1	E15	+5 V Q1	0	0	0	0	1	1	0	0	0	1
0	0	0	1	1		0	1	0	0	E4	YFPA	0	0	1	0	0	1	0	1	0	0
0	0	1	0	0		0	1	1	0	E6	NFH	1	0	1	1	0	0	0	1	1	0
0	0	1	0	1		1	1	1	1	E15	+5 V Q1	0	0	1	0	0	1	0	1	0	0
0	0	1	1	0		0	1	1	1	E7	YWE	0	1	0	0	1	1	1	0	0	1
0	0	1	1	1		1	1	1	1	E15	+5 V Q1	0	1	0	0	1	1	1	0	0	1
0	1	0	0	0		1	1	1	1	E15	+5 V Q1	0	1	1	0	0	1	1	1	0	0
0	1	0	0	1		0	1	0	1	E5	Y16	0	1	0	1	1	1	1	0	1	1
0	1	0	1	0		1	1	1	1	E15	+5 V Q1	0	1	0	0	1	1	1	0	0	1
0	1	0	1	1		1	1	1	1	E15	+5 V Q1	0	1	1	0	0	1	1	1	0	0
0	1	1	0	0		1	1	1	0	E14	Ground Q0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1		1	0	0	1	E9	YSRD	0	1	1	1	0	1	1	1	1	0
0	1	1	1	0		0	0	0	0	E0	YRRD	0	0	0	0	0	1	0	0	0	0
0	1	1	1	1		1	1	1	0	E14	Ground Q0	1	0	1	0	1	0	0	1	0	1
1	0	0	0	0		0	0	0	1	E1	NSCB	1	0	0	0	1	0	0	0	0	1
1	0	0	0	1		1	1	1	1	E15	+5 V Q1	0	0	0	0	1	1	0	0	0	1
1	0	0	1	0		1	1	0	1	E13	NRCO	1	0	0	1	1	0	0	0	1	1
1	0	0	1	1		1	0	0	0	E8	YRDV	0	1	1	0	1	1	1	1	0	1
1	0	1	0	0		0	1	0	1	E5	Y16	0	0	1	0	1	1	0	1	0	1
1	0	1	0	1		1	1	1	0	E14	Ground Q0	1	0	1	0	0	0	0	1	0	0
1	0	1	1	0		0	1	1	1	E7	YWE	0	1	0	1	0	1	1	0	1	0
1	0	1	1	1		1	1	1	0	E14	Ground Q0	1	1	1	0	1	0	1	1	0	1
1	1	0	0	0		1	1	1	1	E15	+5 V Q1	0	0	1	1	0	1	0	1	1	0
1	1	0	0	1		0	1	0	1	E5	Y16	0	1	0	0	0	1	1	0	0	0
1	1	0	1	0		0	1	0	1	E5	Y16	0	1	1	0	0	1	1	1	0	0
1	1	0	1	1		1	1	0	1	E13	NRCO	1	0	1	1	1	0	0	1	1	1
1	1	1	0	0		1	1	1	0	E14	Ground Q0	1	0	1	1	0	0	0	1	1	0
1	1	1	0	1		1	1	1	0	E14	Ground Q0	1	0	0	1	1	0	0	0	1	1
1	1	1	1	0		0	0	1	1	E3	NNWA	1	1	1	1	1	0	1	1	1	1
1	1	1	1	1		1	1	1	1	E15	+5 V Q1	0	1	1	1	0	1	1	1	1	0

Qualifier Mnemonics (U22 inputs E0 to E15)

YRRD (REMAIN READ) is high, as long as the 8018A is active. The ASM is in a loop where the next state address remains 00000 until the YRRD qualifier changes to low. YRRD goes low if one of the following 4 inputs of U3A is set to low:

NFH via U15B to U3A/5 – when FETCH button is pressed

NLW via U15D to U3A/4 – when LOAD button is pressed

NSR via U4A to U3A/2 – when Channel SET is pressed

NCR via U4A to U3A/2 – when Channel CLEAR is pressed

NNWA (NEW WORD ADDRESS) to U3A/1 – from the HP-IB board.

NSCB (SELECT CHANNEL B) Derived from the HP-IB board if data has to be loaded into channel B memory.

NWA (WORD ADDRESS) is generated when the selected word address is reached (Word Address Counters A4 U4/U3 have counted down to 1). The signal is derived from the DATA FORMAT BOARD A4 (YWA) via A2 U18 and A2 U28.

NNWA (NEW WORD ADDRESS) Derived from the HP-IB board when a new word address is required.

YFPA (FIRST PART) Is set to high when ROW ADDRESS 1–16 is selected on the 8018A front panel (Low for ROW ADDRESS 17–32), and set to low when channel clear or channel set is pressed.

Y16 (16 BIT) Indicates that the complete shift register A9 U9 and A9 U10 is loaded; also indicates if the word length is less than 16 bits. Counter A2 U23 is clocked by the data register clock YCLDR. The carry is fed via A2 U12 to E5 of A2 U22.

NFH (FETCH) Low when FETCH is pressed (via U15B).

YWE (WORD END) is generated on the A4 DATA FORMAT board when the word address counters have first counted down to 1 and then the bit per word counters A4U8 and A4U1 have counted up to the selected word length.

RDV (REMOTE DATA VALID) Indicates that data is derived from the HP-IB board

YSRD (SET READ) Allows ASM to jump back into the HP-IB read loop.

NRCO (REMOTE CONTROL) Detects whether the 8018A is under remote control or not.

Q0 0 V Selects U20

Q1 +5 V Selects U21

ASM Instruction Decoder

Instruction decoders U20 and U21 can only be enabled when the clock signal from U11B is low. State address line A4 then enables either decoder U20 or U21 (with A4 low, U21 is selected; with A4 high, U20 is selected), and state address lines A0 to A3 are used to select the instruction, the corresponding decoder output being set to low (all other outputs of both U20 ana U21 remain high).

Table 8–2–2 lists the state addresses, their corresponding instruction and the decoder output associated with each instruction.

Example: State address (U9 A0 to A4) is dec 19 (binary 10011).
Line A4 is high, therefore decoder U20 is selected via U25.
State address lines A0 to A3 are set at binary 0011 which is equivalent to decimal 3, therefore output 3 is enabled and instruction NSMDB is carried out.

Table 8–2–2. Instruction Selection and State Addresses

STATE								INSTRUCTION
		A4	A3	A2	A1	A0		
DEC		W	D	C	B	A	O/P	
0	U21 SELECTED	0	0	0	0	0	0	NRD
1		0	0	0	0	1	1	YCCL
2		0	0	0	1	0	2	---
3		0	0	0	1	1	3	---
4		0	0	1	0	0	4	---
5		0	0	1	0	1	5	NCC
6		0	0	1	1	0	6	NWER, NRMDB
7		0	0	1	1	1	7	NSBB
8		0	1	0	0	0	8	---
9		0	1	0	0	1	9	---
10		0	1	0	1	0	10	---
11		0	1	0	1	1	11	---
12		0	1	1	0	0	12	---
13		0	1	1	0	1	13	---
14		0	1	1	1	0	14	YR, NRCB, NCC
15		0	1	1	1	1	15	---
16	U20 SELECTED	1	0	0	0	0	0	YR, NCC
17		1	0	0	0	1	1	NSITB
18		1	0	0	1	0	2	---
19		1	0	0	1	1	3	NSMDB
20		1	0	1	0	0	4	---
21		1	0	1	0	1	5	YCLDR, YCCL, YDLP, YCL16
22		1	0	1	1	0	6	---
23		1	0	1	1	1	7	---
24		1	1	0	0	0	8	---
25		1	1	0	0	1	9	YCCL, YCLDR, YDLP, YCL16
26		1	1	0	1	0	10	---
27		1	1	0	1	1	11	YCCL, YCLDR, YCL16
28		1	1	1	0	0	12	YCCL, YCLDR, YCL16
29		1	1	1	0	1	13	---
30		1	1	1	1	0	14	---
31		1	1	1	1	1	15	NRCB

Instruction Mnemonics

NRD	(READ). As long as FETCH or LOAD is not pressed, U21 output 0 (pin 1) is switched to low when the ASM-clock U11B/6 goes low. The output U5/11 of flip-flop U5B/D is held low, which sets the output U5A/3 high. The signal YLD + YFH at the output of U2C/8 is low (not true) and the 8018A output is activated.
YCCL	(CONTROL CLOCK). Derived from U21 output 1 (pin 2) via U6D, U6B and U17C. It is fed via U7A/B on the bit rate board to the BPW and WPF (WA) counters on the DATA FORMAT BOARD. As YCL2, it is fed during FETCH and LOAD to the SYNC AMP. BOARD. CCL is used during FETCH and LOAD to clock the WPF, WA and RAM counters to the correct Word Address (YWA) and to the end of the selected word (YWE).
YWER	(WRITE ENABLE RAMS). Enables RAMS to accept data (1 bit at a time) during LOAD.
NRMDB	(RESET MORE DATA BINARY). U21 output 6 (pin 7 ensures that the output of flip-flop U15A is set to high. U26C disables data flow from the HP-IB board via U1A, U13A and sets YMDA (MORE DATA) to not true.
NSBB	(SET BLANK BINARY). U21 output 7 (pin 8) sets the output of flip-flop U12B to low after the word end (YWE) has been reached. This disables U14A, and the output of U1C goes low which blanks (via U1D and U13A) all bits more than the selected word length set in the shift register.
YR	(RESET). U21 output 14 (pin 15) clears the 16 bit counter U23 and flip-flop U12. YR is routed via the BIT RATE BOARD to the DATA FORMAT BOARD, MEMORY BOARD and SYNC AMPLIFIER BOARD where it sets or resets counters and flip-flops to start conditions.
NRCB	(RESET CONTROL BOARD). U21 output 14 (pin 15) or U20 output 15 (pin 17) resets CONTROL BOARD (with the exception of the ASM).
NCC	(CLEAR COUNTER). Clears 16-bit counter U23 and flip-flop U12, via U6C and U4D, to establish start conditions.
NSITB	(HP-IB CHANNEL B SELECT). U20 output 1 (pin 2) sets output of flip-flop U15C low (via U4B) to select channel B (YB).
NSMDB	(SET MORE DATA BINARY). U20 output 1 (pin 2) is used in HP-IB operation. Flip-Flop U15A is reset, and YMDA (YES MORE DATA) is set ture via U26C. U1A is enabled and data can be transferred from the HP-IB board (YRDI REMOTE DATA INPUT) to the shift register via U1A and U13A.
YCLDR	(CLOCK DATA REGISTER). U20 output 5 (pin 6) clocks the data into the shift register (display) during FETCH, or out of the shift register during LOAD. In addition, the 16-bit counter, U23, is clocked by YCL16.
YDLP	(DISABLE LAST PULSE). Is generated by YCLDR via U28C and U27D. It is fed to the DATA FORMAT BOARD A4 and sets flip-flop A4 U19 to supress YL (LAST BIT) generation during FETCH and LOAD.
YCL 16	(CLOCK 16 BIT COUNTER). Is generated from YCLDR, and clocks the 16-bit counter until Y16 is generated, thus ensuring complete shift register loading (with blanks after the word end).

ASM Loops

Figure 8–2–2 shows the complete Control ASM flowchart. From this flowchart, it can be seen that there are 6 main loops, each of which is briefly described in the following. Additional information i.e. qualifier and instruction descriptions, can be found in the previous paragraphs of this Service Block.

Loop 1: The 8018A ASM stays in this loop when the FETCH, LOAD, SET or CLEAR pushbuttons have not been pressed. During this loop time, data can be generated. If one of the afore-mentioned pushbuttons is pressed, data generation is stopped and the ASM prepares the instrument for data fetching or data loading.

Loop 2: The memory address counters have to be set to the bit address number corresponding to the first bit of the selected word address within the serial datastream. The number of clock pulses (YCCL) needed to set the counters can be calculated via the formula [BPW x (WA−1)] + 1.

Example: BPW (bits per word or word length) = 06
WA (word address) = 04
Number of clock pulses = [6 x (4−1)] + 1 = 19

Loop 3: After the memory address counters are set and the LOAD pushbutton has been pressed, the entire RAM's are enabled by YWER (write enable ram). If the word length is less than 16 bits, the algorithm jumps out of Loop 3 into Loop 4 after the word end (YWE) has been reached. If the word length is 16 bits, it jumps out of the Loop at qualifier Y16.

Loop 4: To ensure that bits which are set outside the selected word length are blanked in the LED display shift register, the algorithm stays in Loop 4 until qualifier Y16 is true. All bits are blanked by NSBB between word end and the maximum allowable 16 bits.

Loop 5: If the second row (bits 17–32) is selected, bits 1 to 16 have to be counted after the word address has first been reached. After the 16 counts, during which no data is loaded or fetched, the algorithm jumps to Loop 3 if the LOAD pushbutton is pressed, or to Loop 6 if the FETCH pushbutton is pressed. If the instrument is in remote control, the control clock YCCL is replaced by remote register clock YCLRR.

Loop 6: Loop 6 has the same function for data fetch as Loop 3 has for data load. When the FETCH push-button is pressed, data is clocked into the LED display shift register until the word end is reached (RAMs are set to read). If the word length is 16 bits, the algorithm jumps out of the Loop at qualifier Y16; if the word length is less than 16 bits, it jumps to Loop 4. Here, bits surplus to the selected word length are blanked.

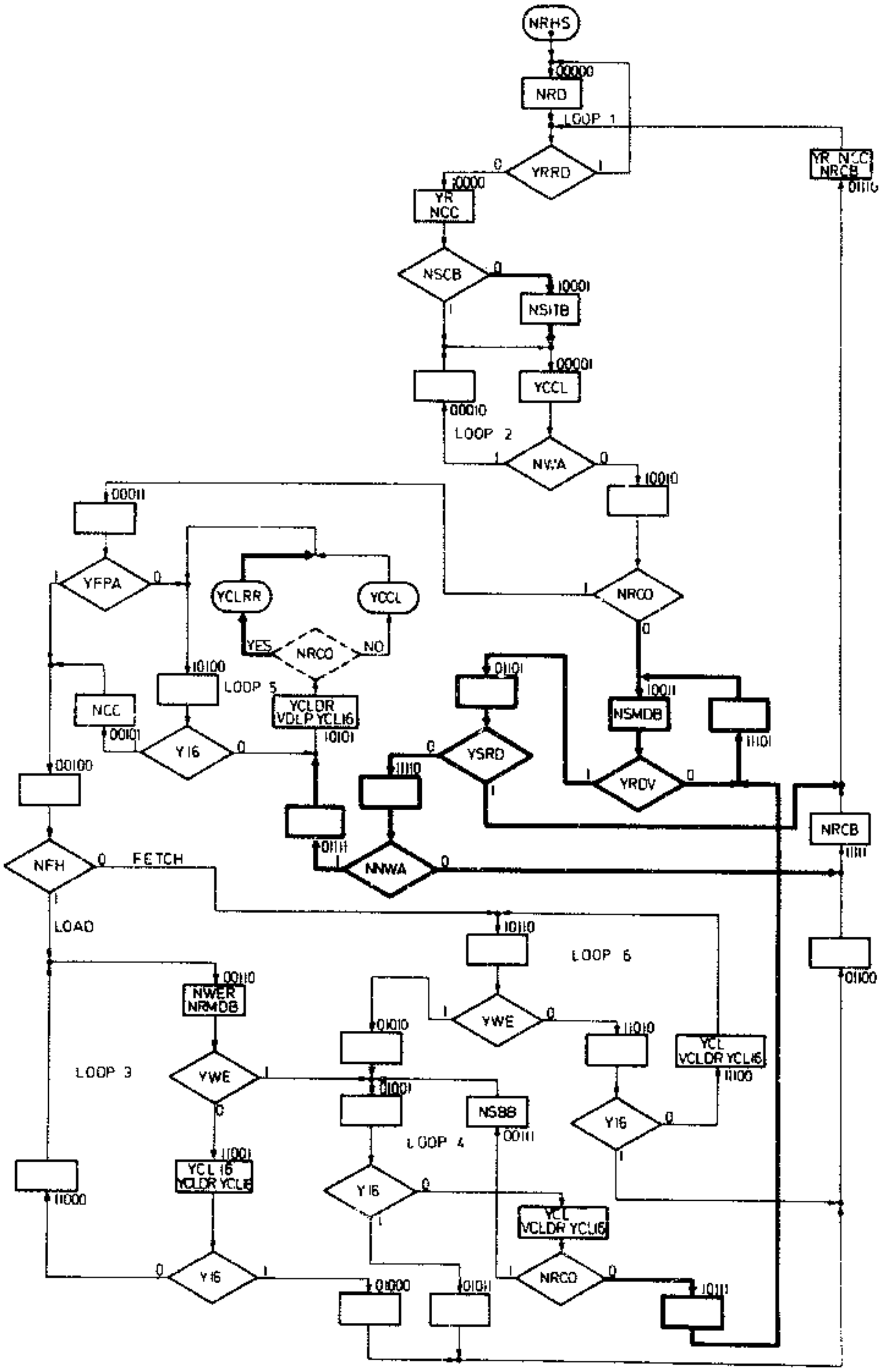


Figure 8–2–2. Control ASM Flowchart

TROUBLESHOOTING

Procedure

Equipment: Logic State Analyzer
Oscilloscope

1. Connect the Logic Analyzer D0 to D4 to testpoints TP1 to TP5 (TP5 = most significant bit) and the clock to the CLK testpoint on the A2 Control Board.

2. Connect Ground to chassis ground.

3. Set the Trigger Word to 00000.

4. Set the 8018A for WORD MODE FETCH or WORD MODE LOAD as indicated in the associated program listings (Tables 8–2–3 and 8–2–4).

5. Press LOAD or FETCH and Lock the pushbutton by inserting a wedge (e.g. matchstick) between the pushbutton and its associated front panel bezel. This causes the ASM to work in repetitive mode.

6. Before stepping through the flowchart and program listings, it would be helpful to acquaint oneself with the following rules:

   – Y preceeding a mnemonic indicates that the mnemonic (Qualifier or State) is true on a positive level or edge.

   – N preceding a mnemonic indicates that the mnemonic is true on a negative level or edge.

   – 1 at a decision block (qualifier) indicates the direction of the program flow if a high level is present at the corresponding qualifier input of A2 U22.

   – 0 at a decision block (qualifier) indicates the direction of the program flow if a low level is present at the corresponding qualifier input of A2 U22.

   – the binary number following a decision block shows the next state address, where the most significant bit is the inverted qualifier level (inverted by A2 U22).

     Example: Qualifier input NWA is 0 (low), then the next state address is 10010. Qualifier input NWA is 1 (high), then the next state address is 00010.

   – the heavy lines and symbols indicate program flow with HP-IB.

   – mnemonics behind the binary program listings are the corresponding instructions which should be generated.

   – instructions and qualifiers are explained at the beginning of this Service Block.

7. Using the Logic Analyzer delay facility, compare actual program flow with the program listings given in Tables 8–2–3 and 8–2–4 (for pre-determined 8018A switch settings), and with their corresponding flowcharts, Figures 8–2–3 and 8–2–4 respectively.

Table 8–2–3. Program Listing for Load Word Mode

A4	A3	A2	A1	A0	
0	0	0	0	0	NRD
1	0	0	0	0	YR
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
1	0	0	1	0	*
0	0	0	1	1	*
0	0	1	0	0	*
0	0	1	1	0	NWER NRMDB
1	1	0	0	1	YCCL YCLDR YDLP YCL16
1	1	0	0	0	*
0	0	1	1	0	NWER NRMDB
1	1	0	0	1	YCCL YCLDR YDLP YCL16
1	1	0	0	0	*

A4	A3	A2	A1	A0	
0	0	1	1	0	NWER NRMDB
1	1	0	0	1	YCCL YCLDR YDLP YCL16
1	1	0	0	0	*
0	0	1	1	0	NWER NRMDB
1	1	0	0	1	YCCL YCLDR YDLP YCL16
1	1	0	0	0	*
0	0	1	1	0	NWER NRMDB
1	1	0	0	1	YCCL YCLDR YDLP YCL16
1	1	0	0	0	*
0	0	1	1	0	NWER NRMDB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
0	1	0	1	1	*
0	1	1	0	0	*
1	1	1	1	1	NRCB
0	1	1	1	0	YR YRCB NCC

Notes

1 * = don't care

2 The 8018A settings are as follows:

WORD MODE
ROW ADDRESS 1–16
WORD ADDRESS (WA) 04
WORD LENGTH (WL) 06
LOAD WORD depressed

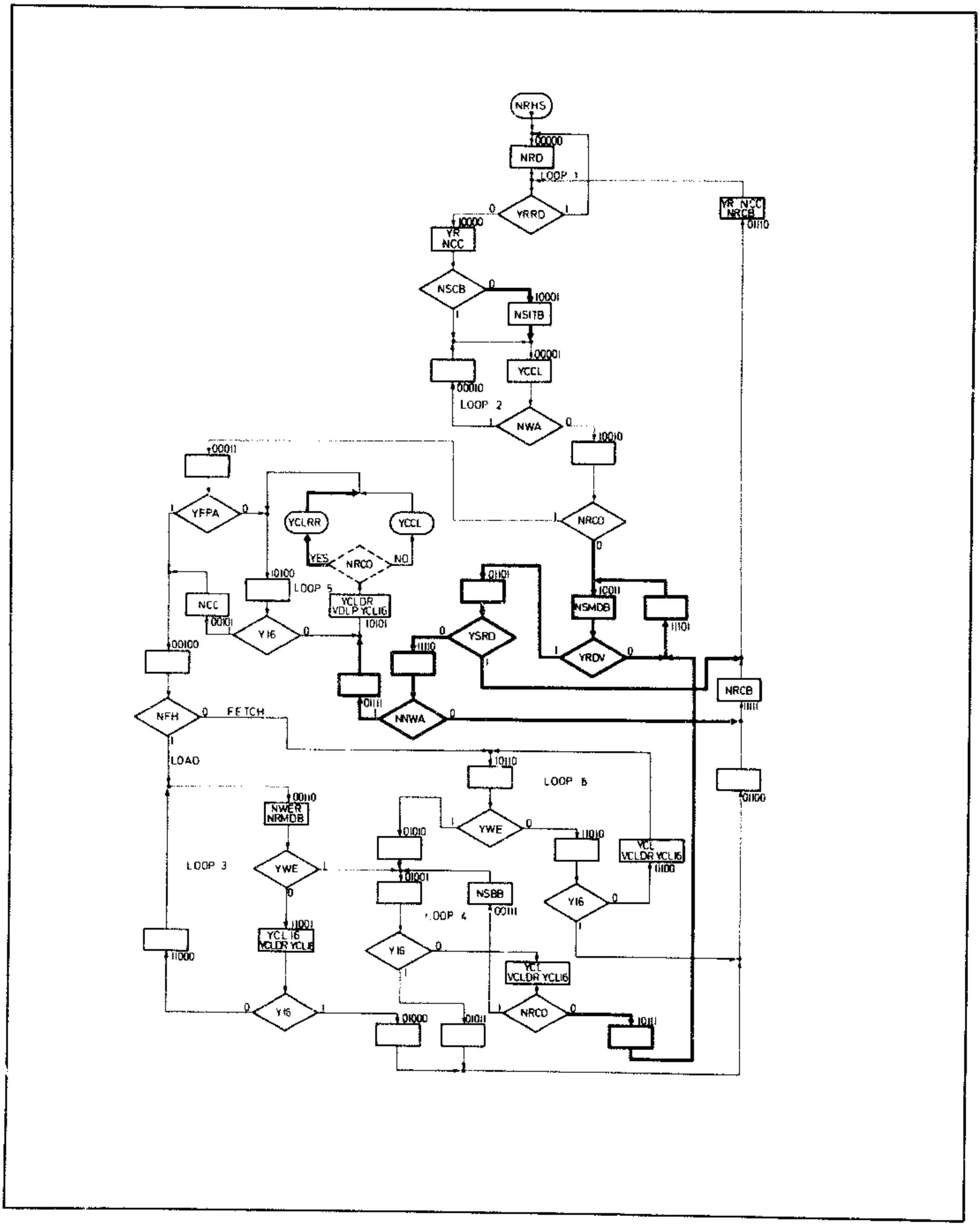


Figure 8–2–3. ASM Flowchart for Load Word Mode

Table 8–2–4. Program Listing for Fetch Word Mode

A4	A3	A2	A1	A0	
0	0	0	0	0	
1	0	0	0	0	YR
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
0	0	0	1	0	*
0	0	0	0	1	YCCL
1	0	0	1	0	*
0	0	0	1	1	*
0	0	1	0	0	*
1	0	1	1	0	*
1	1	0	1	0	*
1	1	1	0	0	YCCL YCLDR YCL16
1	0	1	1	0	*
1	1	0	1	0	*
1	1	1	0	0	YCCL YCLDR YCL16

A4	A3	A2	A1	A0	
1	0	1	1	0	*
1	1	0	1	0	*
1	1	1	0	0	YCCL YCLDR YCL16
1	0	1	1	0	*
1	1	0	1	0	*
1	1	1	0	0	YCCL YCLDR YCL16
1	0	1	1	0	*
1	1	0	1	0	*
1	1	1	0	0	YCCL YCLDR YCL16
1	0	1	1	0	*
0	1	0	1	0	*
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
1	1	0	1	1	YCCL YCLDR YCL16
0	0	1	1	1	NSBB
0	1	0	0	1	*
0	1	0	1	1	*
0	1	1	0	0	*
1	1	1	1	1	NRCB
0	1	1	1	0	YR NRCB NCC

Notes

1 * = don't care

2 The 8018A settings are as follows:

WORD MODE
ROW ADDRESS 1–16
WORD ADDRESS (WA) 04
WORD LENGTH (WL) 06
FETCH WORD depressed

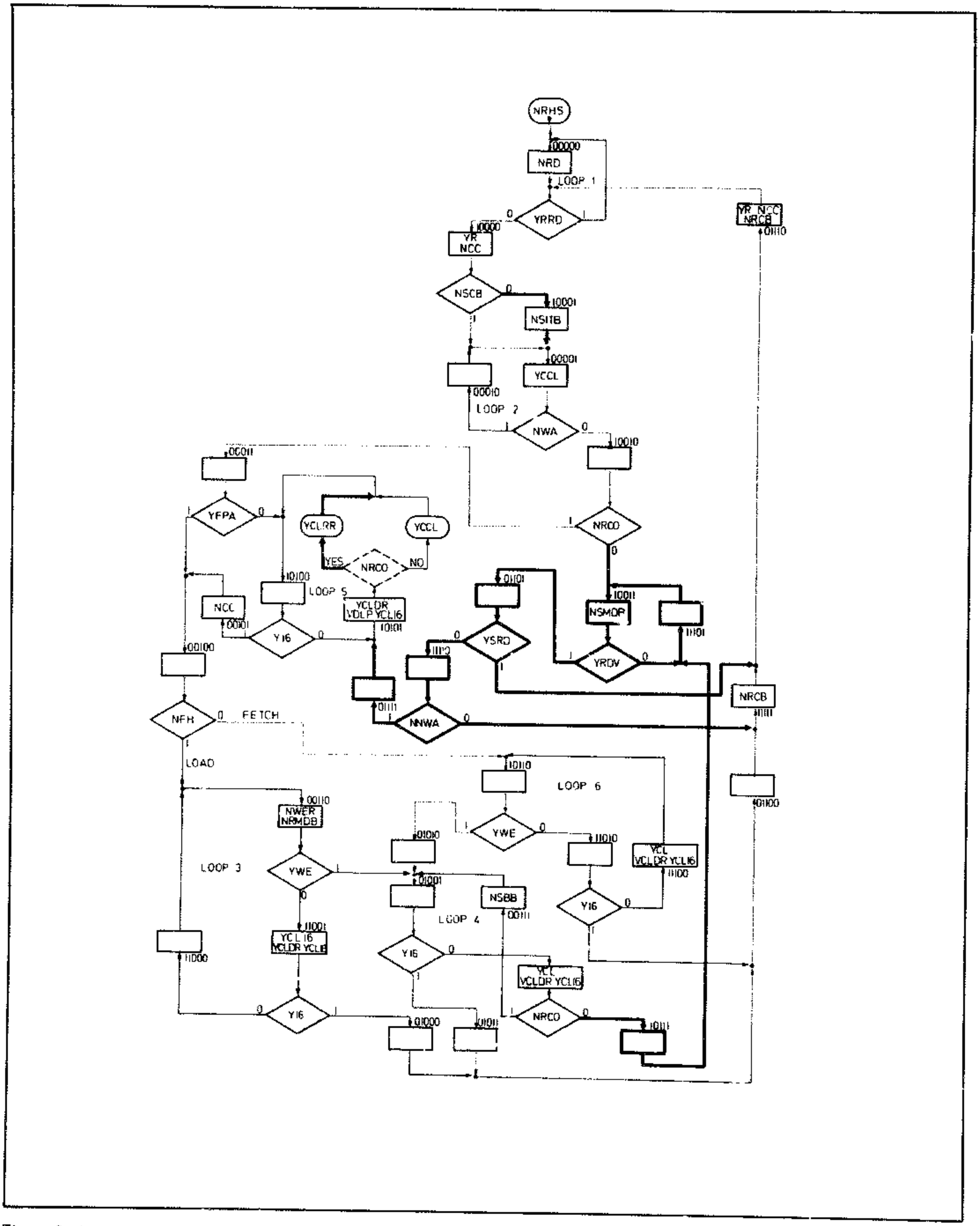


Figure 8–2–4. ASM Flowchart for Fetch Word Mode

ASM Troubleshooting Hints

1. If the Logic Analyzer indicates NO CLOCK, check A2U11A and U11B. The frequency of the ASM Clock Generator should be approx. 1.5 MHz.

2. When the FETCH or LOAD pushbutton is depressed (locked with a matchstick) and the ASM stays in the remain read loop (Loop 1), check the clear input (NPON) of A2U10 and the qualifier input YRRD of A2 U22. Clear of A2 U10 must be high and YRRD must be low.

3. Remove the A1 HP-IB board to ensure that qualifiers NSCB (E1), NNWA (E3), YRDV (E8), YSRD (E9) and NRCO (E13) are not true. A5, A6, A7 and A8 can also be removed for ASM troubleshooting.

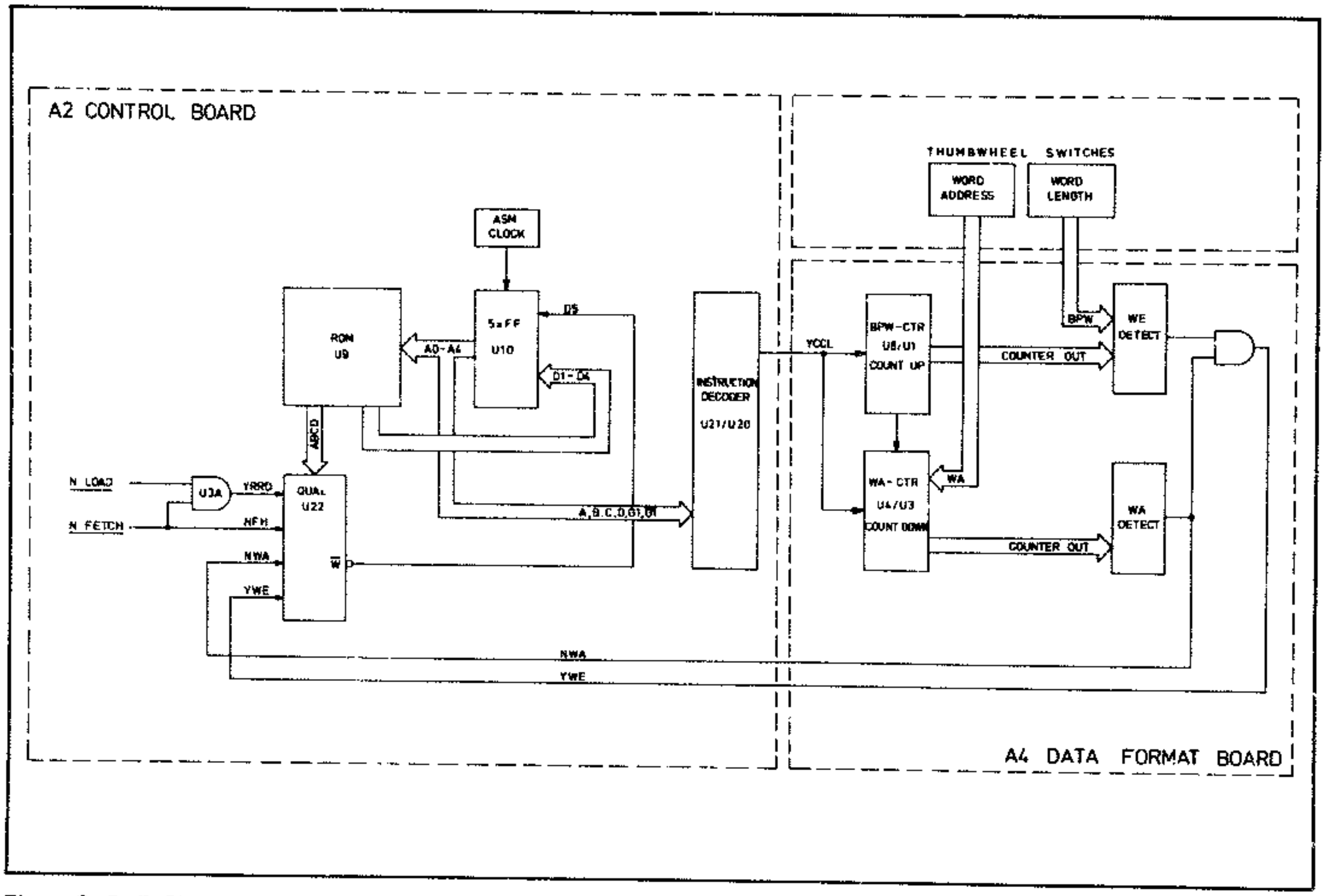
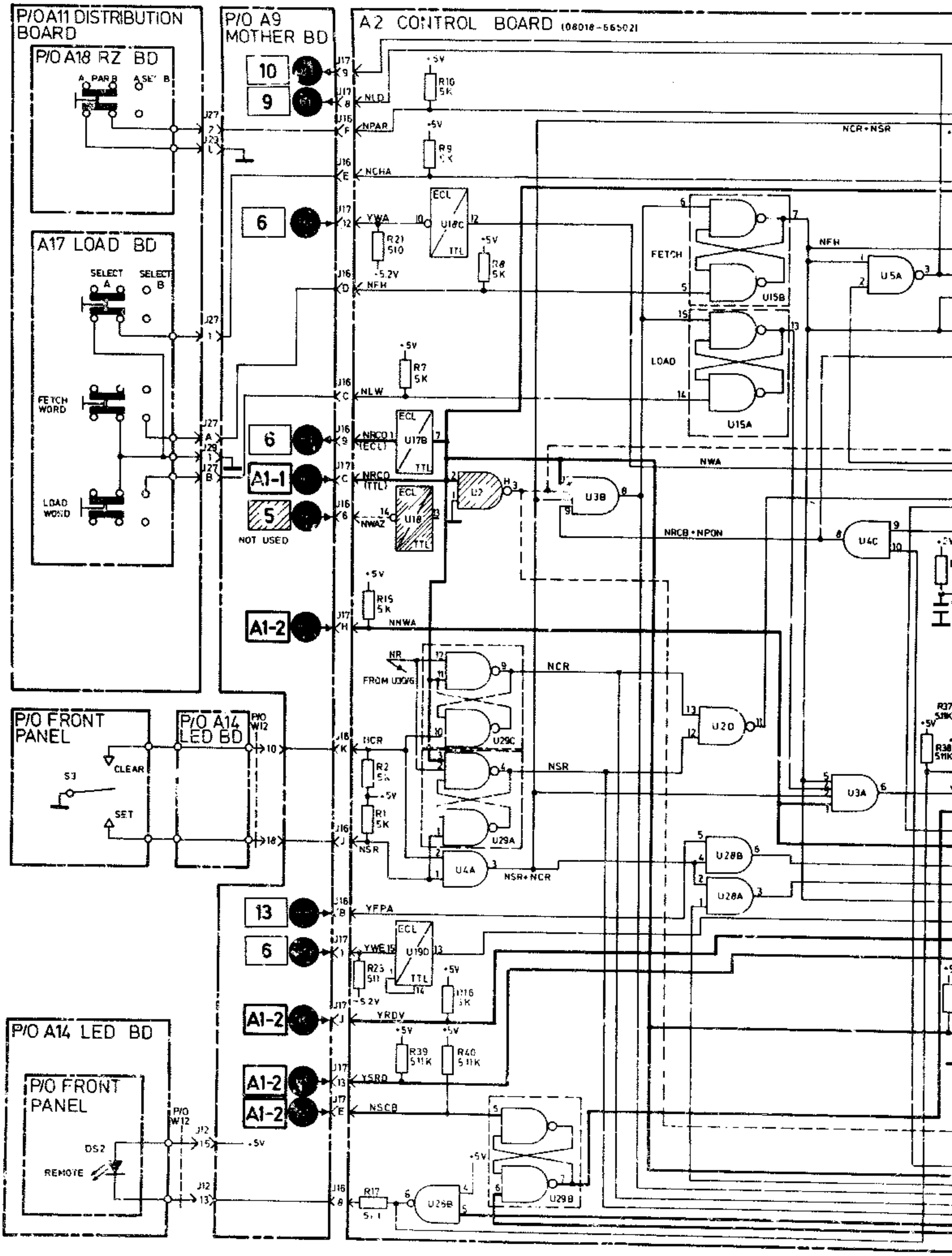


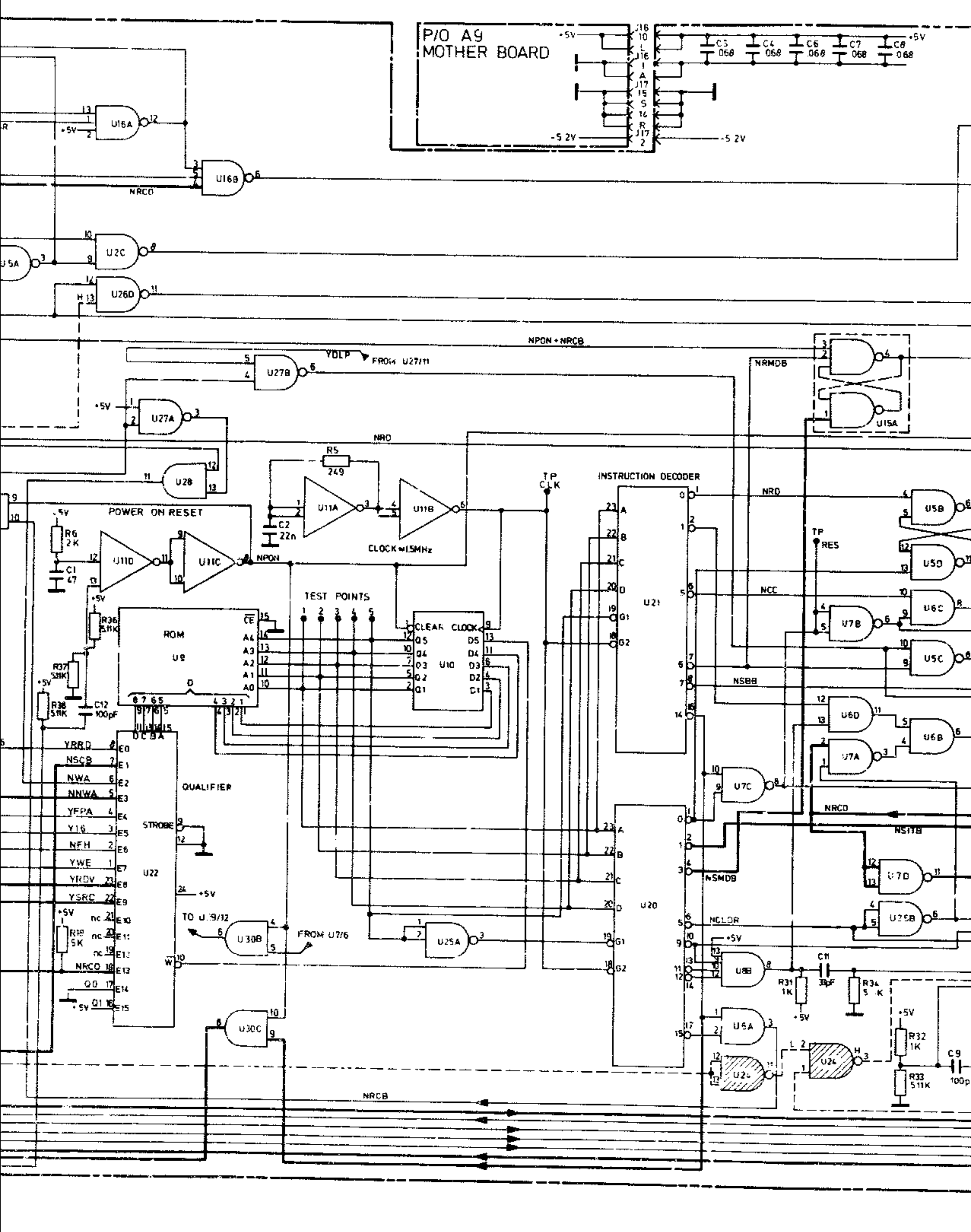
Figure 8–2–5. Simplified Block Diagram of ASM

4. Figure 8–2–5 shows a simplified block diagram of the 8018A ASM and the BPW/WA counters connected via the two most important qualifiers NWA (Word Address) and YWE (Word End). NWA (true) is the feedback from the word address counter when the word address is reached. YWE (true) is the feedback when fetch or load word is completed. If these qualifiers are not correct, check the BPW (Bit Per Word) and WA (word address) counters on the A4 Data Format board. This can be done with FETCH and LOAD pushbutton released (8018A is active). See also troubleshooting hints and circuit description for the A4 board.

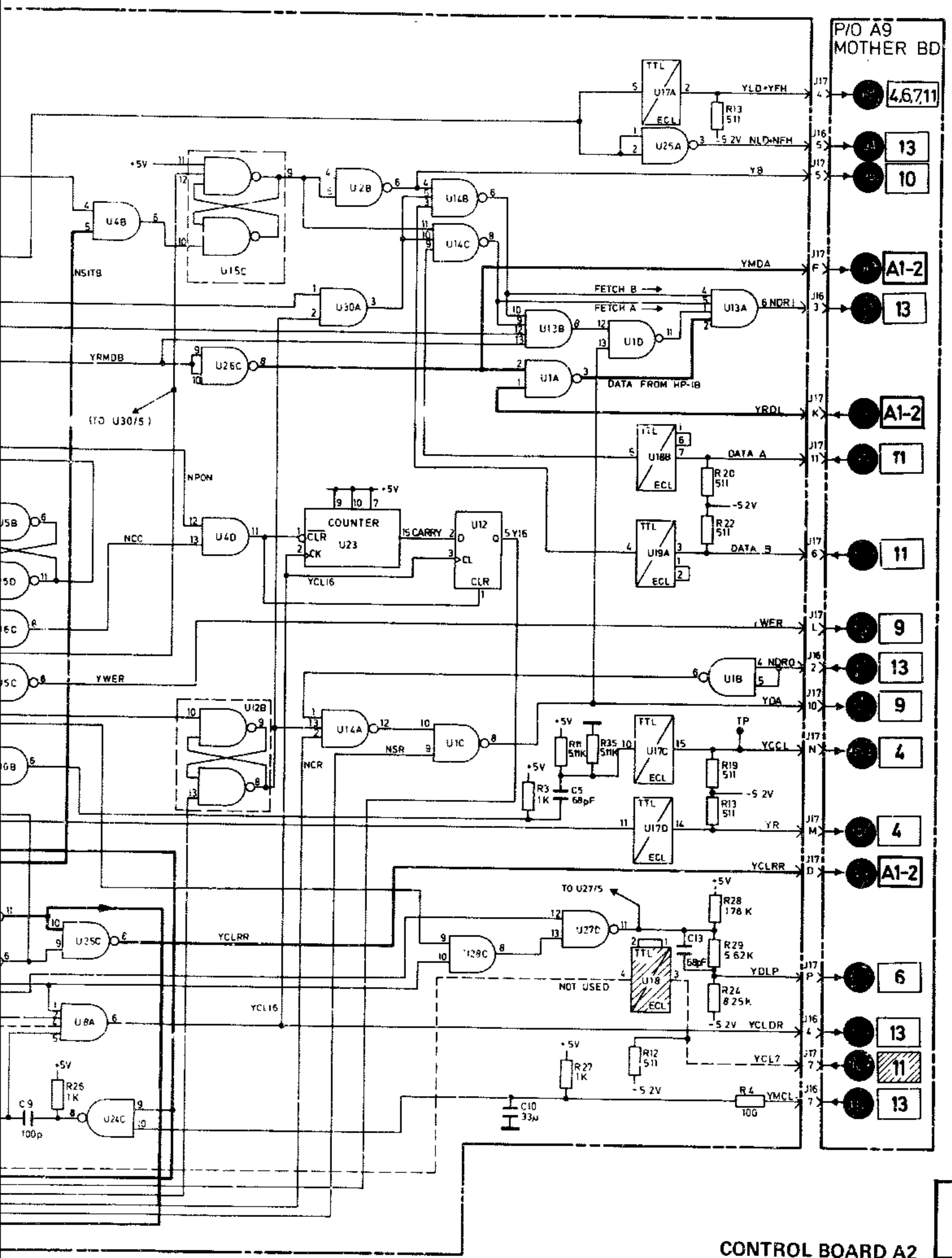
5. When more bits than the selected wordlength are loaded into the LED display shift register and the additional bits are not blanked, check the Y16 counter and qualifier on the A2 board.

6. To check the instructions use the Logic Analyzer to trigger the Oscilloscope.


P/O A11 DISTRIBUTION BOARD
P/O A18 RZ BD
A17 LOAD BD
SELECT A
SELECT B
FETCH WORD
LOAD WORD
P/O A9 MOTHER BD
A2 CONTROL BOARD (08018-66502)
NOT USED
P/O FRONT PANEL
P/O A14 LED BD
CLEAR
SET
S3
P/O A14 LED BD
P/O FRONT PANEL
DS2
REMOTE
FETCH
LOAD
U15B
U15A
U5A
U3B
U4C
U20
U29C
U29A
U4A
U28B
U28A
U3A
U29B
U25B
U18C
U17B
U19D
NLD
NPAR
NCHA
YWA
NFH
NLW
NRCO
NWAZ
NNWA
NCR
NSR
NSR+NCR
NCR+NSR
NWA
NRCB+NPON
YFPA
YWE
YRDY
YSRD
NSCB
FROM U30/6

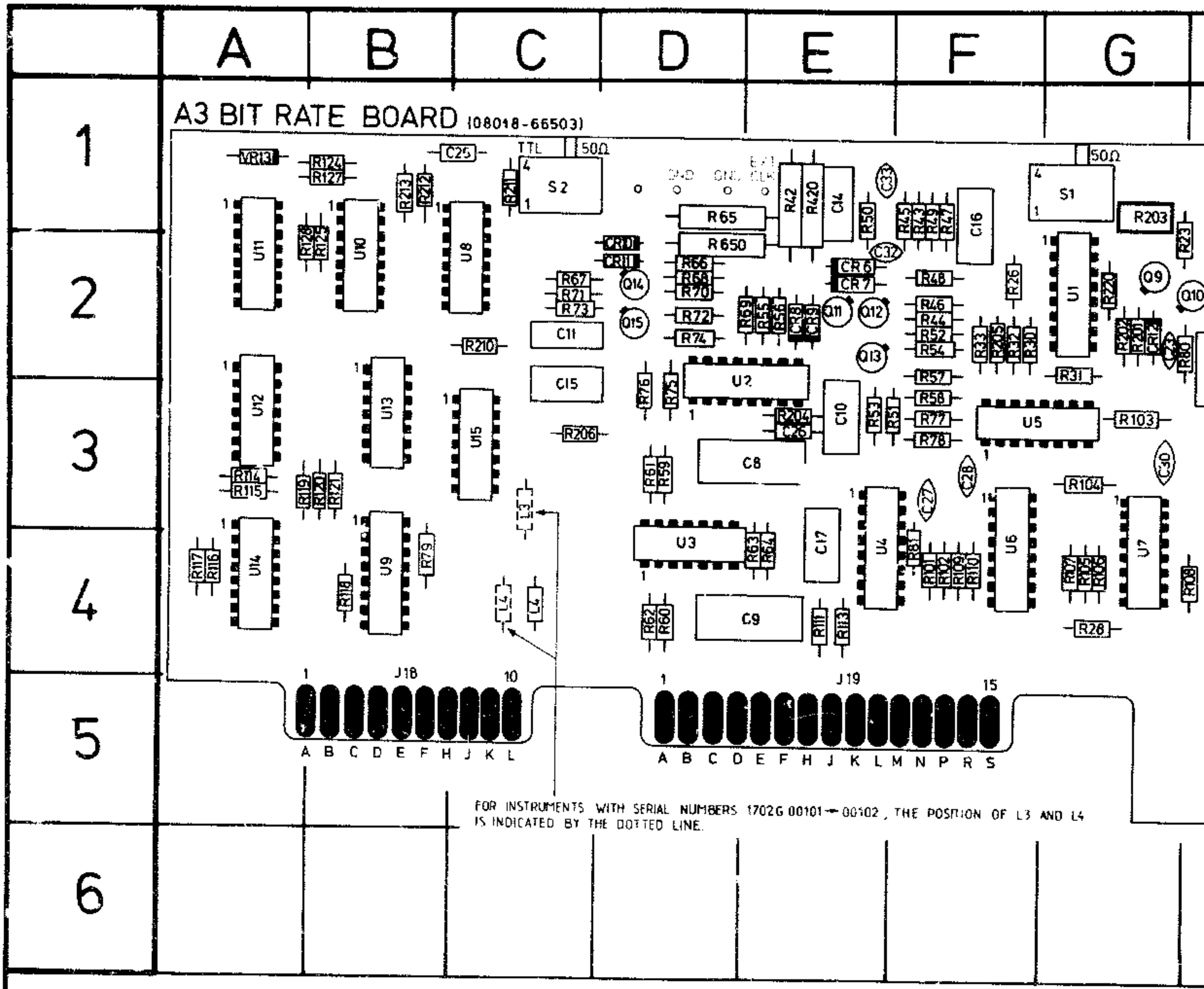


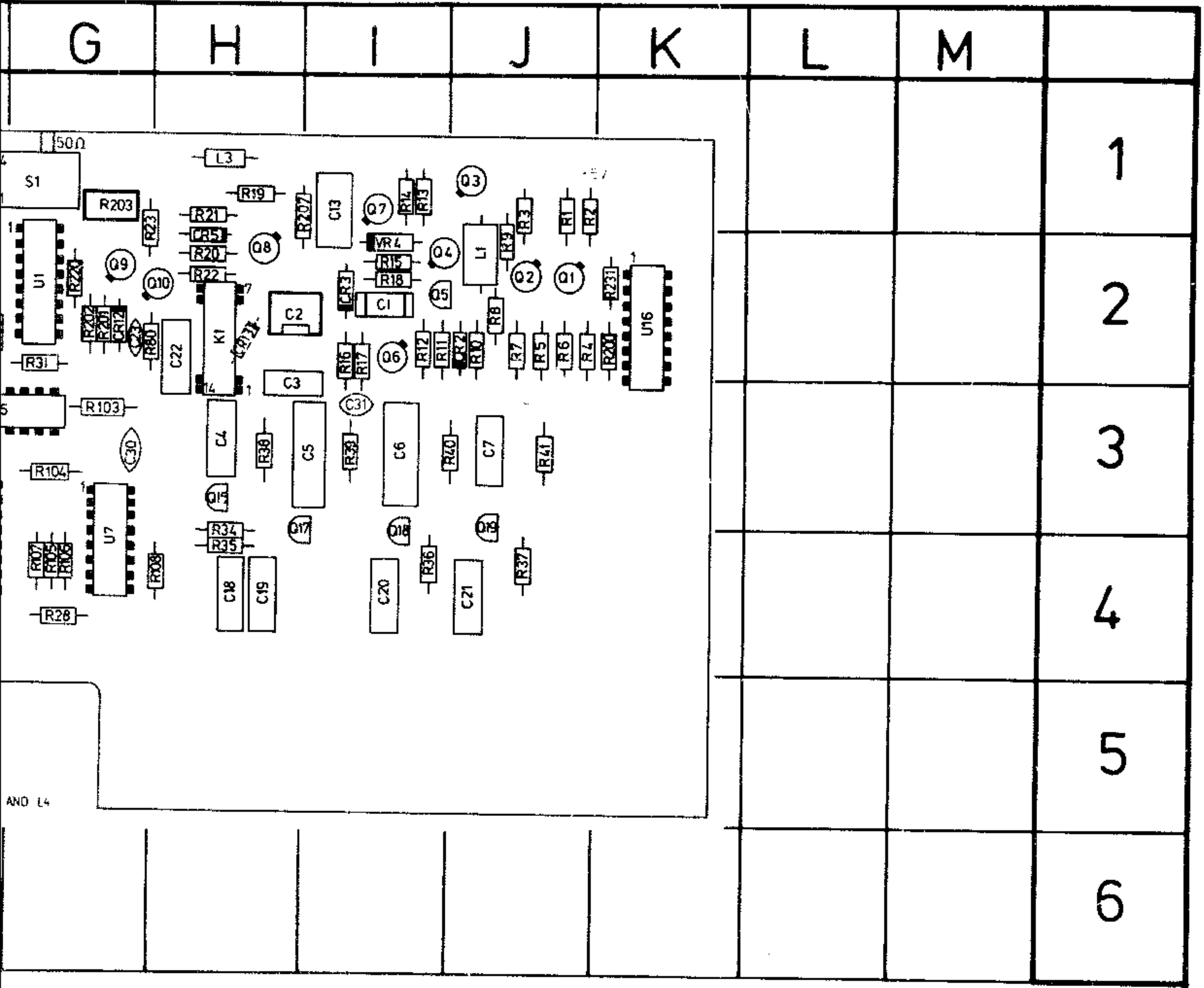
P/O A9
MOTHER BOARD
POWER ON RESET
INSTRUCTION DECODER
TEST POINTS
ROM
U9
U10
U20
U21
U22
QUALIFIER
STROBE
CLEAR
CLOCK
CLOCK ≈1.5MHz
NPON + NRCB
NPON
NRO
NRD
NCC
NSBB
NRMDB
NRCD
NSITB
NSMDB
NCLDR
NRCB
NRCO
YDLP
FROM U27/11
TO U19/12
FROM U7/6
TP CLK
TP RES
YRRD
NSCB
NWA
NNWA
YEPA
Y16
NFH
YWE
YRDV
YSRC
U16A
U16B
U2C
U26D
U27A
U27B
U28
U11A
U11B
U11C
U11D
U15A
U5B
U5C
U5D
U6B
U6C
U6D
U7A
U7B
U7C
U7D
U8B
U25A
U25B
U30B
U30C
U5A
U24
R5 249
R6 2K
C1 47
C2 22n
R36 511K
R37 511K
R38 511K
C12 100pF
R19 5K
R31 1K
C11 33pF
R32 1K
R33 511K
C9 100p
C3 .068
C4 .068
C6 .068
C7 .068
C8 .068
+5V
-5.2V



CONTROL BOARD A2

2


A
B
C
D
E
F
G
1
2
3
4
5
6
A3 BIT RATE BOARD (08018-66503)
TTL
50Ω
S2
S1
J18
J19
FOR INSTRUMENTS WITH SERIAL NUMBERS 1702G 00101 → 00102, THE POSITION OF L3 AND L4 IS INDICATED BY THE DOTTED LINE.


G H I J K L M
1 2 3 4 5 6
50Ω
S1
L3
R19
R203
R23
R21
CR5
R20
R22
R207
C13
Q7
R14
R13
Q3
R3
R1
R2
Q8
VR4
R15
R18
Q4
L1
R9
Q2
Q1
R231
U1
R220
Q9
Q10
CR3
C1
Q5
C2
K1
R8
U16
R202
R201
CR12
R80
C22
R16
R17
Q6
R12
R11
CR2
R10
R7
R5
R6
R4
R200
R31
C3
R103
C31
C30
C4
R38
C5
R39
C6
R40
C7
R41
R104
U7
Q15
Q17
Q18
Q19
R34
R35
R36
R37
R107
R105
R106
R108
C18
C19
C20
C21
R28
AND L4

M

1

2

3

4

5

6

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	I2	Q11	E2	R52	F2	R202	G2
C2	H/I2	Q12	E2	R53	E3	R203	G1
C3	H/I3	Q13	E2	R54	F2	R204	E3
C4	H3	Q14	D2	R55	E2	R205	F2
C5	I3	Q15	D2	R56	E2	R206	C3
C6	I3	Q16	H3	R57	F2	R210	C2
C7	J3	Q17	I3/4	R58	F3	R211	C1
C8	D/E3	Q18	I3/4	R59	D3	R212	B1
C9	D/E4	Q19	J3/4	R60	D4	R213	B1
C10	E3	R1	J1	R61	D3	R220	G2
C11	C2	R2	J/K1	R62	D4	R420	E1/2
C13	I1/2	R3	J1	R63	E4	R650	D2
C14	E1	R4	J/K2	R64	E4	S1	G1
C15	C2/3	R5	J2	R65	D1	S2	C1
C16	F1/2	R6	J2	R66	D2	U1	G2
C17	E3/4	R7	J2	R67	C2	U2	D/E 2/3
C18	H4	R8	J2	R68	D2	U3	D4
C19	H4	R9	J2	R69	D/E2	U4	E3/4
C20	I4	R10	J2	R70	D2	U5	F/G3
C21	J4	R11	I/J2	R71	C2	U6	F3/4
C22	H2	R12	I2	R72	D2	U7	G3/4
C23	G2	R13	I1	R73	C2	U8	C1/2
C25	B/C1	R14	I1	R74	D2	U9	B4
C26	E3	R15	I2	R75	D2/3	U10	B1/2
C27	F3	R16	I2	R76	D2/3	U11	A1/2
C28	F3	R17	I2	R77	F3	U12	A3
C30	G3	R18	I2	R78	F3	U13	B3
C31	I3	R19	H1	R79	B4	U14	A4
C32	E2	R20	H2	R80	G/H2	U15	C3
C33	E1	R21	H1	R81	F4	U16	K2
CR2	J2	R22	H2	R101	F4	VR4	I2
CR3	I2	R23	G/H1/2	R102	F4	VR13	A1
CR5	H2	R28	G4	R103	G3		
CR6	E2	R26	F2	R104	G3		
CR7	E2	R30	F2	R105	G4		
CR8	E2	R31	G2	R106	G4		
CR9	E2	R32	F2	R107	G4		
CR10	D2	R33	F2	R108	H4		
CR11	D2	R34	H4	R109	F4		
CR12	G2	R35	H4	R110	F4		
CR13	H2	R36	I4	R111	E4		
K1	H2	R37	J4	R113	E4		
L1	J2	R38	H3	R114	A3		
L2	I1/2	R39	I3	R115	A3		
L3	H1	R40	J3	R116	A4		
L4	C4	R41	J3	R117	A4		
Q1	J2	R42	E1/2	R118	B4		
Q2	J2	R43	F1	R119	A3		
Q3	J1	R44	F2	R120	B3		
Q4	I/J2	R45	F1	R121	B3		
Q5	I/J2	R46	F2	R124	B1		
Q6	I2	R47	F1	R125	B2		
Q7	I1	R48	F2	R127	B1		
Q8	H2	R49	F1	R128	A2		
Q9	H2	R50	E1	R200	K2		
Q10	G2	R51	E/F3	R201	G2		

SERVICE BLOCK 3
RATE GENERATION AND EXTERNAL INPUT CIRCUITS BOARD A3 [3], [4]

THEORY OF OPERATION

RATE GENERATION (SCHEMATIC 4)

The rate Schmitt trigger comprises Q3, Q4 and current source Q5. The base of Q4 acts as a ramp node for the ramp (rate) charging capacitors C1 to C7, the capacitors being switched onto the node via transistor switches Q16 to Q19. Positive current source Q8 charges the ramp capacitors with a current adjustable via RATE VERNIER R1 until the Schmitt trigger threshold is reached, at which point Q4 turns on, and Q7 turns off due to the decreased base voltage. The negative current now supplied via R16 and R17 into the Q6 base turns the negative current source Q6 on, and the ramp capacitors are discharged (Q6 saturates causing a rapid discharge).

Upon ramp discharge, the rate Schmitt trigger switches again, Q4 turning off and Q7 turning on. With Q7 switched on, the negative current supplied by R16 is routed via Q7. When AUTO CYCLE is not selected, the rate Schmitt trigger is disabled in BIT, WORD and FRAME CYCLE by signal YCLD on U4 pin 13 at the end of a cycle. The high YCLD is routed via U16/Q2 to the base of Q6, thus preventing the ramp node from discharging and the Schmitt trigger cannot switch.

Similarly in FETCH and LOAD operations, the rate Schmitt trigger is disabled by signal YFD + YLD on U4 pin 12. This signal is high which holds Q6 off (via U16/Q2) and prevents the ramp node from discharging.

Internal Clock (Schematic 4): With INT CLOCK selected, gate U5 (pin 3 output) is enabled to allow the signal from the internal clock generator through, and gate U5 (output pin 14) is disabled by applying an ECL high to input pin 13. The route for the external clock signal is thus effectively disabled.

External Clock (Schematic 4): With the INT CLOCK pushbutton released (i.e. External Clock selected), an ECL high is applied to gate U5 input pin 4, thus disabling output pin 3 and preventing the internal clock signal from passing through.

Manual Clock (Schematic 4): A single clock pulse is generated by pressing the MAN CLOCK switch which causes flip-flop U4/U5 to toggle once.

Duty Cycle

The sawtooth signal from the ramp capacitors is amplified by Q9 and Q10, and then applied to the line receiver U1. This line receiver is wired as a Schmitt trigger with a fixed threshold level. By varying the dc offset via R203, the trigger point of U1, relative to the ramp voltage, can be varied.

External Inputs

External Clock (Schematic 3): The external clock signal is routed to switch A3 S1. If EXT + CLOCK MODE is selected, switch S1 can be set to 50 Ω or high impedance (for TTL triggering). In this mode, the 50 Ω-setting routes the clock signal via diode bridge CR6 to CR9 to the differential amplifier Q11/Q12. As the positive-going edge of the clock signal rises above ~0.5 V, the differential amplifier Q11/Q12 switches (i.e. Q11 off; Q12 on), and signal is fed via Q13 and pins 3/2 of switch S1 to the Schmitt trigger U2 (U2 is a line receiver wired as a Schmitt trigger with a fixed threshold level). In the high impedance setting of S1, the external clock signal is routed direct to U2 via gates U15.

If EXT – CLOCK MODE is selected, switch S1 must be set to the 50 Ω-setting. Once again the clock signal is routed via the diode bridge CR6 → CR9 to the differential amplifier Q11/Q12, the trigger level now being ~ −1.2 V. As the positive-going edge of the clock signal rises above this trigger level, Q11/Q12 switch (Q11 off; Q12 on), and the signal is fed via Q13 and pins 3/2 of switch S1 to Schmitt trigger U2.

Cycle Command (Schematic 3): The cycle command signal is routed to switch A3 S2, which can be set to either 50 Ω input impedance or high input impedance (TTL signals). In the 50 Ω-setting, the command signal is routed via diodes CR10/CR11 to the differential amplifier Q14/Q15. As the positive-going edge of the command signal rises above the trigger level (~ 0.5 V) of differential amplifier Q14/Q15, Q14 turns off and Q15 turns on. The resultant negative-going edge at Q14 collector is routed via pin 5 and 6 of switch S2 to the Schmitt trigger U2 (U2 is a line receiver wired as a Schmitt trigger with a fixed threshold level).

In the TTL-setting of switch S2, the command signal is routed via gate/inverter U15 to the Schmitt trigger U2.

Manual Cycle Commands (Schematic 4): Manual cycle commands are generated via switch S2 on the front panel. By pressing this switch to the MAN CYCLE position, a low is applied to AND gate U3 pin 1 which generates YMCC via gate U8.

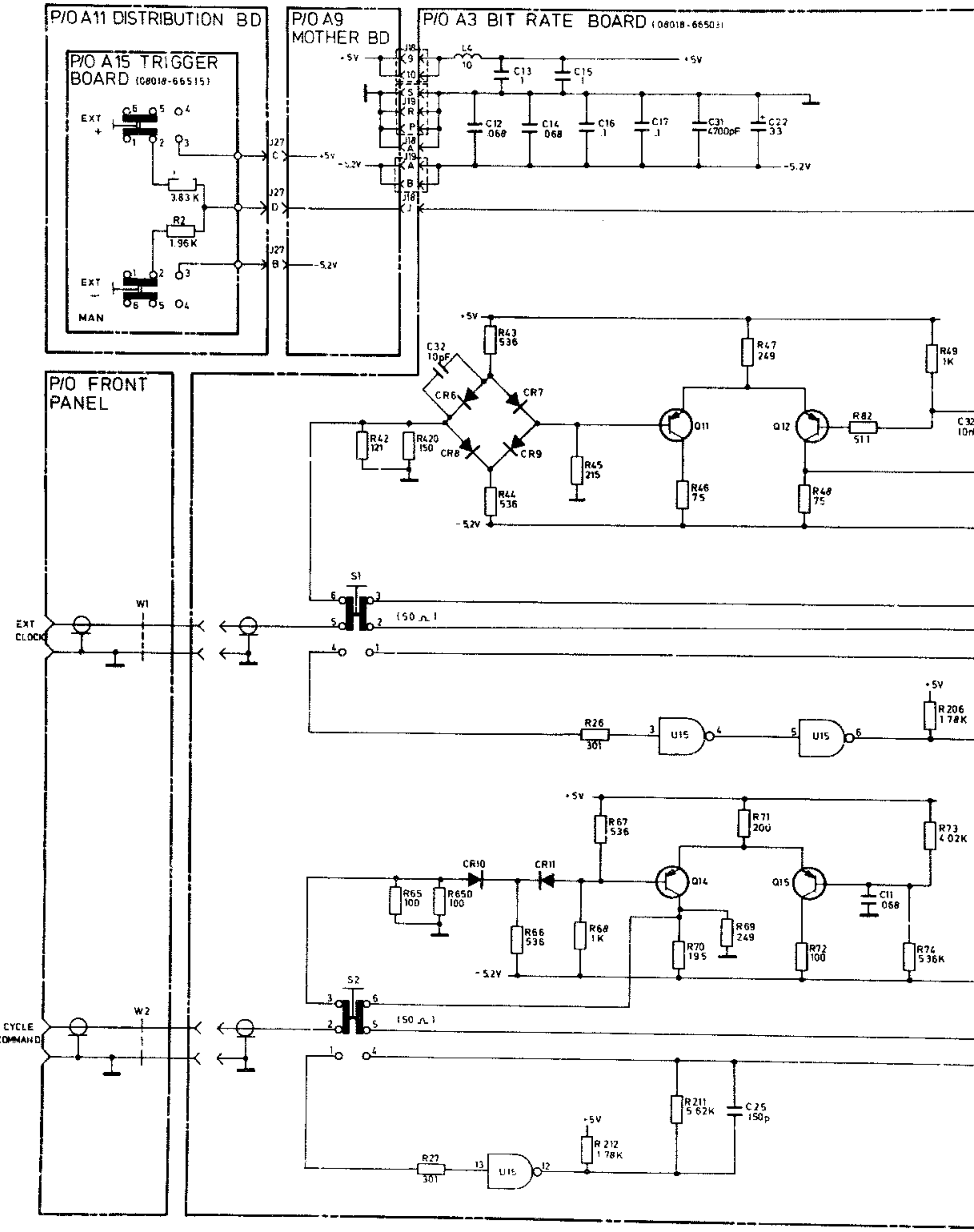
The reset pulse YR is similarly generated via gates U3/U4.

TROUBLESHOOTING

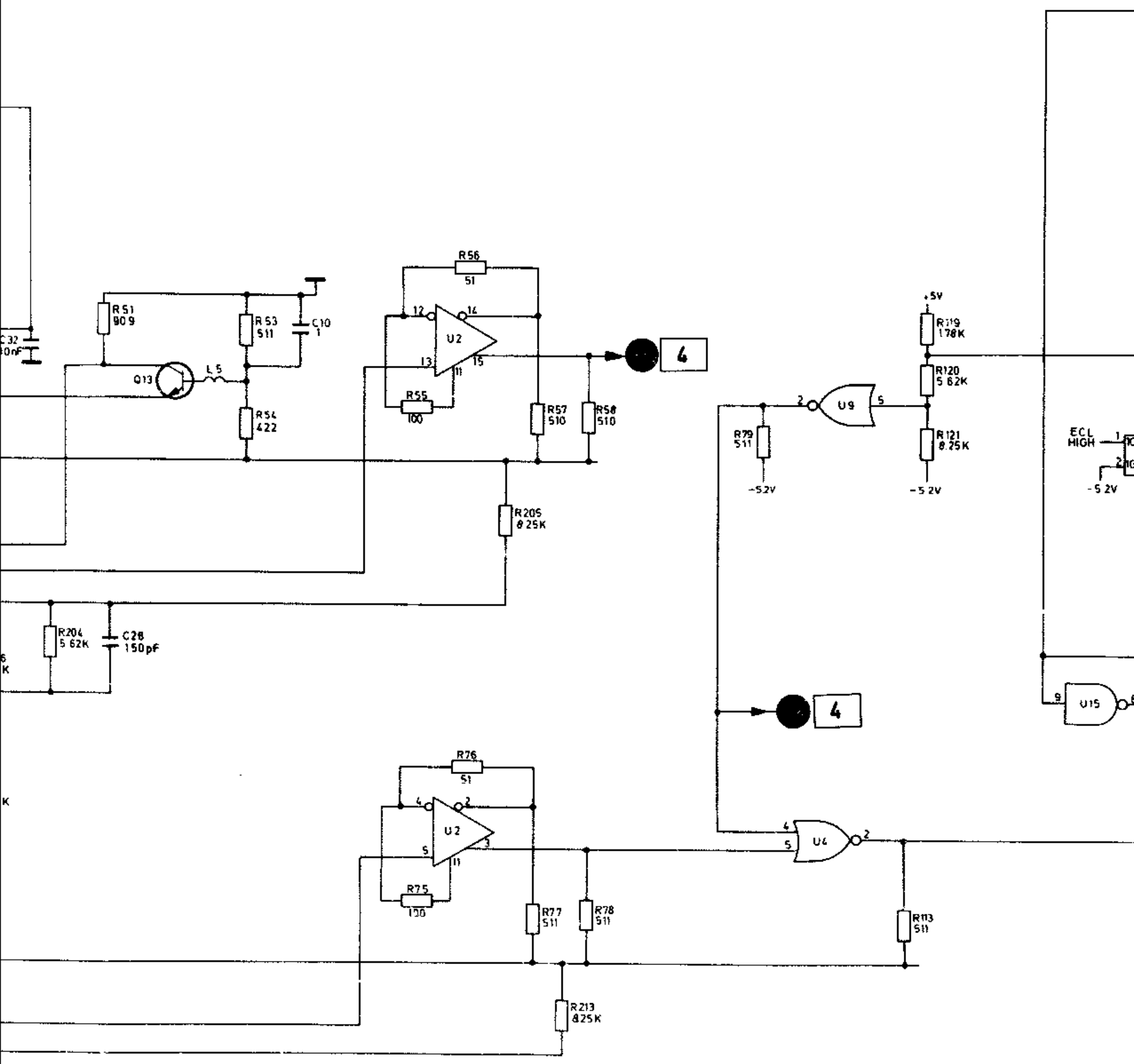
The following tips are given to aid troubleshooting the rate generator:

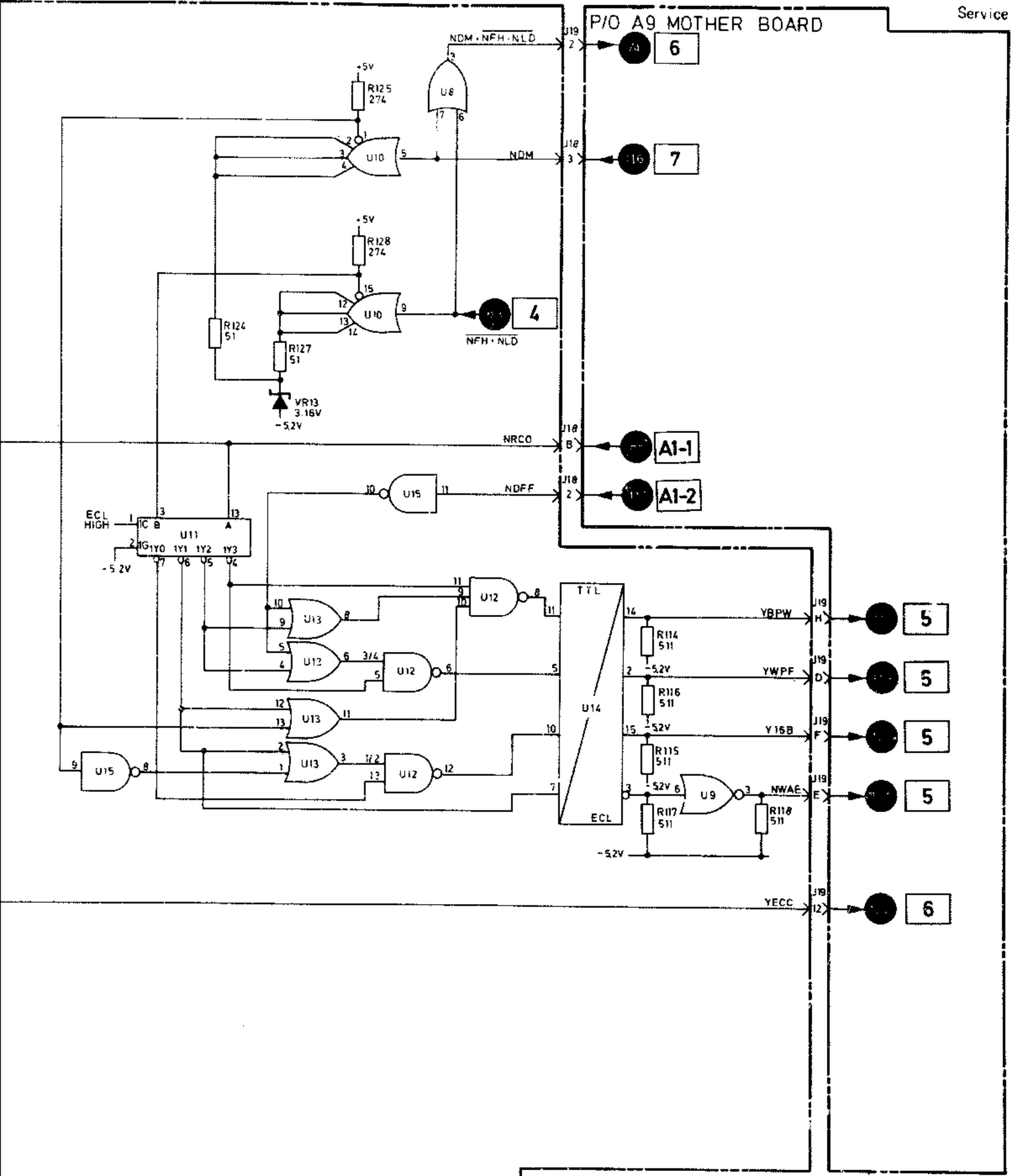
– Before troubleshooting down to component level on the rate generator, check U1 pin 6 output with INT CLOCK selected. If no signal is present, check the dc level at U16 pin 1, which should be +0.4 V or +2.7 V to enable and disable the rate generator respectively. Also, if the Schmitt trigger is disabled, the Q2 collector should be at approximately +1.6 V.

  If the rate generator is enabled, both input pins 12 and 13 of gate U4 should be low.



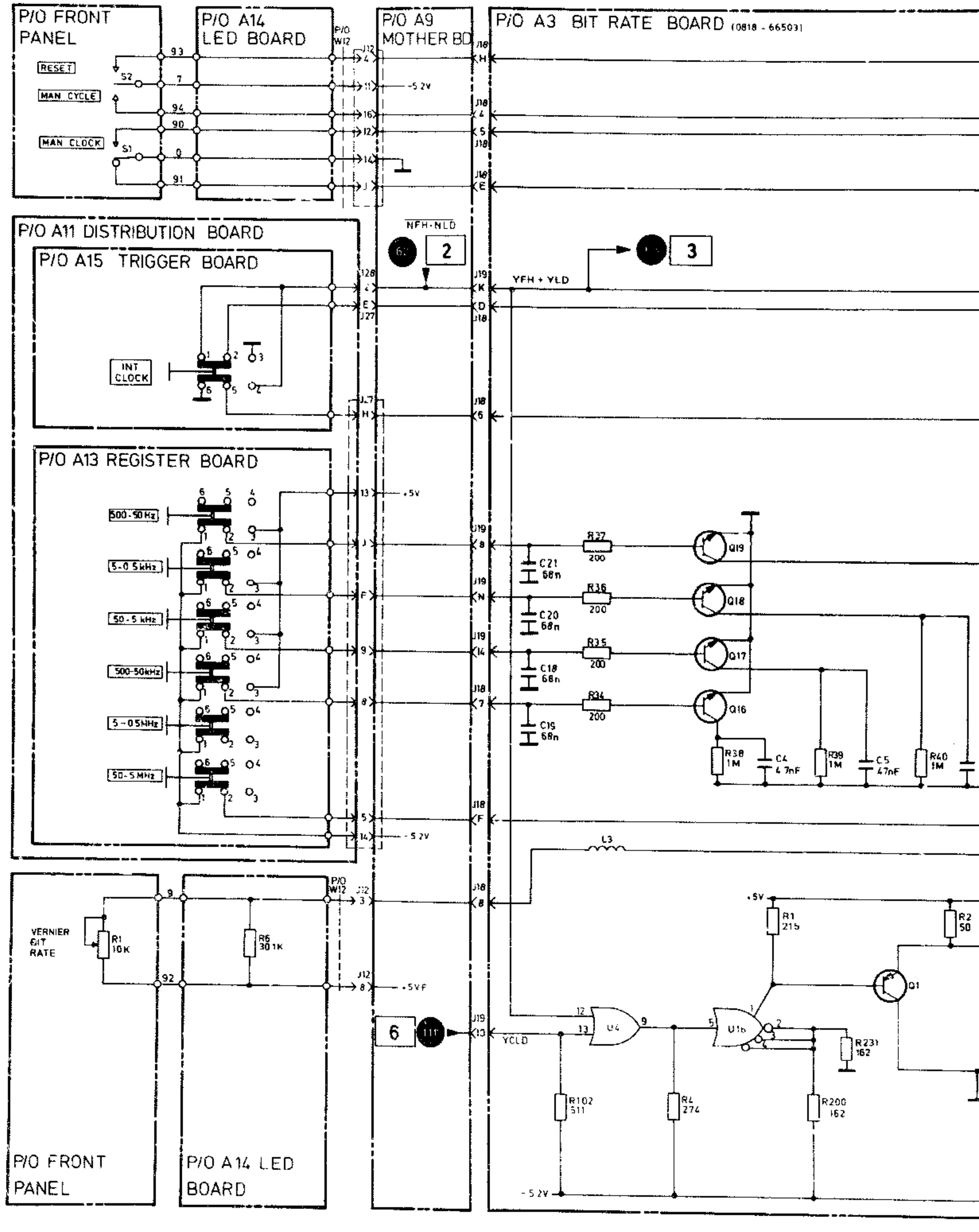
P/O A11 DISTRIBUTION BD
P/O A15 TRIGGER BOARD (08018-66515)
EXT +
EXT −
MAN
3.83 K
R2 1.96 K
P/O A9 MOTHER BD
J27 C
J27 D
J27 B
P/O A3 BIT RATE BOARD (08018-66503)
L4 10
C13 .1
C15 .1
C12 .068
C14 .068
C16 .1
C17 .1
C31 4700pF
C22 33
+5V
−5.2V
P/O FRONT PANEL
EXT CLOCK
W1
CYCLE COMMAND
W2
R43 536
R44 536
C32 10pF
CR6
CR7
CR8
CR9
R42 121
R420 150
R45 215
Q11
Q12
R46 75
R47 249
R48 75
R49 1K
R82 511
S1
(50 Ω)
R26 301
U15
R206 1.78K
R67 536
R71 200
R73 4.02K
CR10
CR11
Q14
Q15
R65 100
R650 100
R66 536
R68 1K
R69 249
R70 195
R72 100
R74 5.36K
C11 .068
S2
R211 5.62K
C25 150p
R212 1.78K
R27 301


R56
51
R51
909
R53
511
C10
1
C32
Q13
L5
R54
422
12
14
U2
13
15
11
R55
100
R57
510
R58
510
4
R205
8.25K
R204
5.62K
C28
150pF
+5V
R119
178K
R120
5.62K
R121
8.25K
-5.2V
2
U9
5
R79
511
-5.2V
ECL HIGH
-5.2V
9
U15
4
R76
51
4
2
U2
5
3
11
R75
100
R77
511
R78
511
4
5
U4
2
R113
511
R213
825K

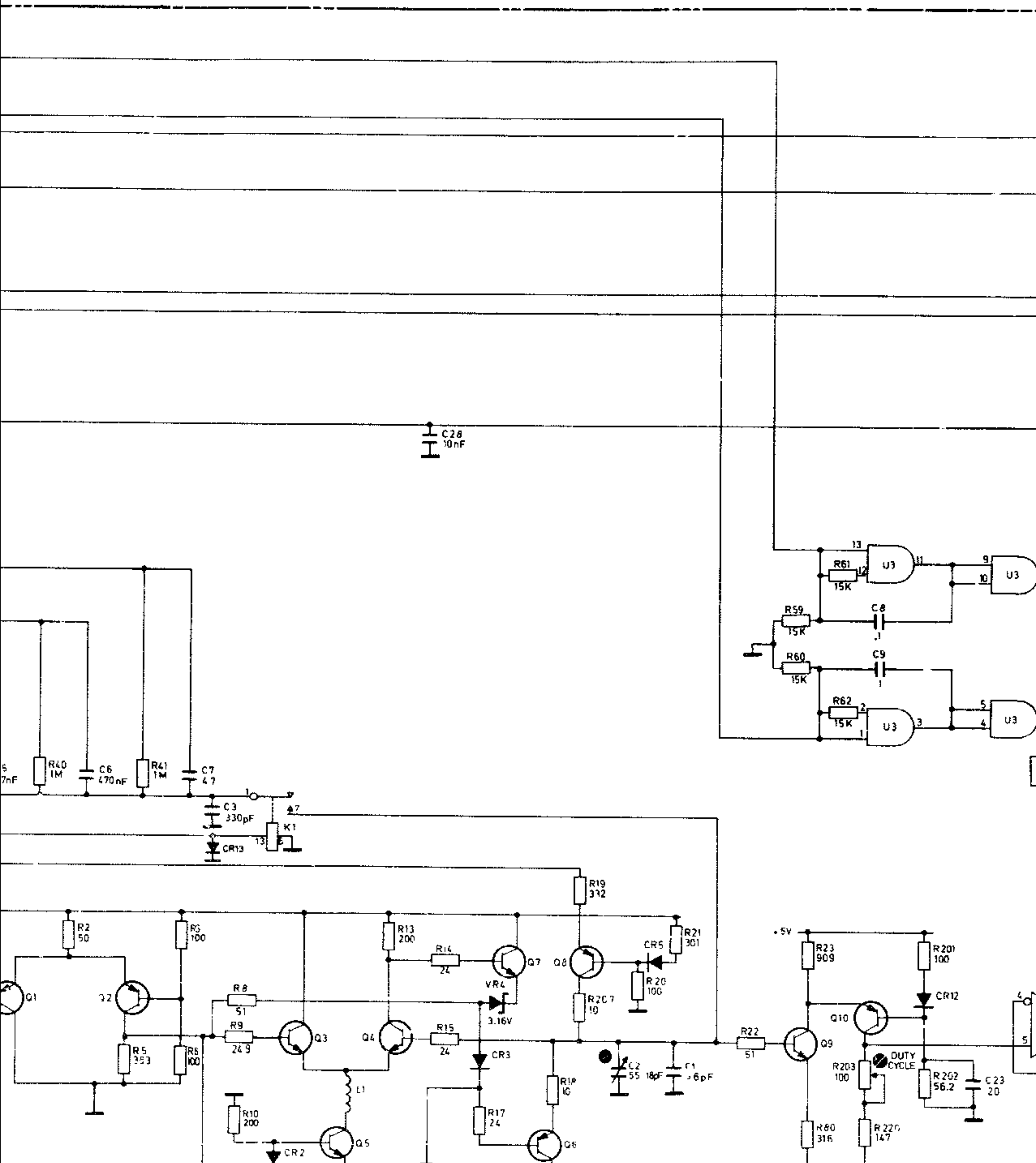


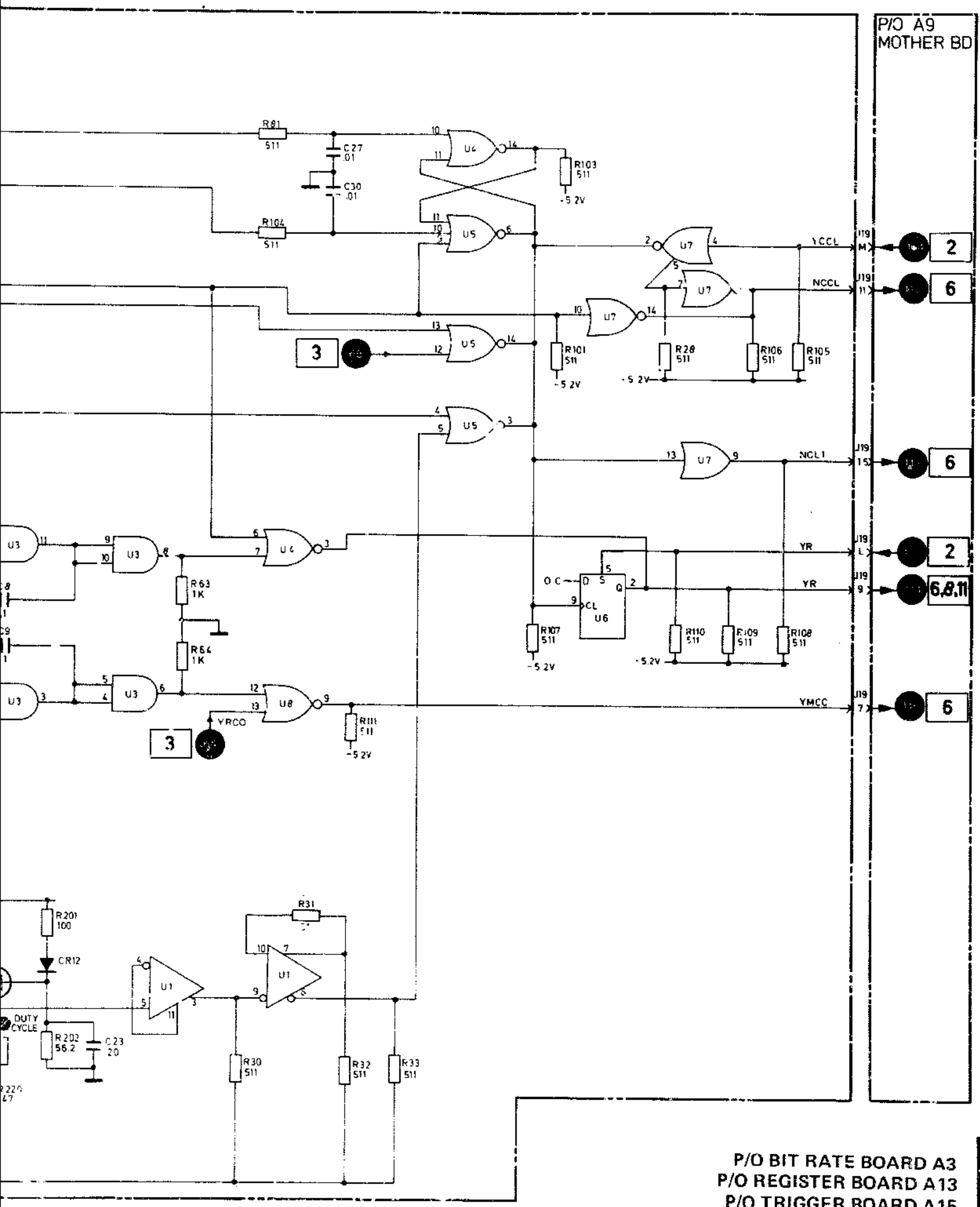
P/O BIT RATE BOARD A3
P/O TRIGGER BOARD A15

3



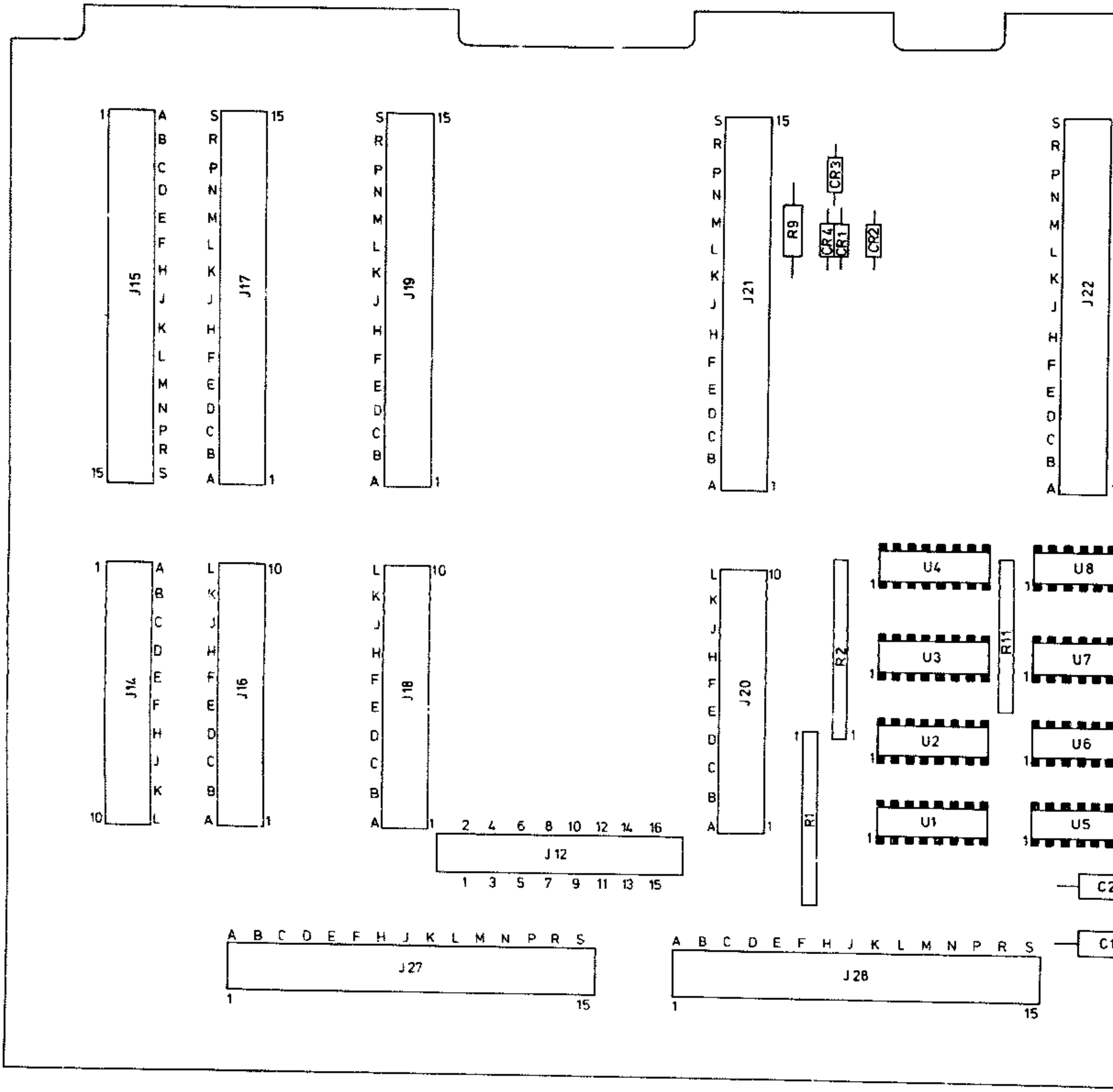
P/O FRONT PANEL
RESET
MAN CYCLE
MAN CLOCK
P/O A14 LED BOARD
P/O W12
P/O A9 MOTHER BD
P/O A3 BIT RATE BOARD (0818 - 66503)
P/O A11 DISTRIBUTION BOARD
P/O A15 TRIGGER BOARD
INT CLOCK
NFH·NLD
YFH + YLD
P/O A13 REGISTER BOARD
500-50Hz
5-0.5kHz
50-5 kHz
500-50kHz
5-0.5MHz
50-5MHz
+5V
-5.2V
R37 200
R36 200
R35 200
R34 200
C21 68n
C20 68n
C18 68n
C19 68n
Q19
Q18
Q17
Q16
R38 1M
C4 4.7nF
R39 1M
C5 47nF
R40 1M
L3
VERNIER BIT RATE
R1 10K
R6 30.1K
+5VF
YCLD
U4
U1b
R1 215
R2 50
Q1
R231 162
R102 511
R4 274
R200 162
P/O FRONT PANEL
P/O A14 LED BOARD


C28
10nF
U3
R61
15K
R59
15K
C8
.1
R60
15K
C9
.1
R62
15K
R40
1M
C6
470nF
R41
1M
C7
4.7
C3
330pF
K1
CR13
R19
332
R2
50
R3
100
R13
200
R14
24
Q7
Q8
CR5
R21
301
R20
100
+5V
R23
909
R201
100
CR12
Q10
Q1
Q2
R8
51
VR4
3.16V
R207
10
R9
24.9
Q3
Q4
R15
24
CR3
R22
51
Q9
DUTY
CYCLE
R203
100
R202
56.2
C23
20
R5
383
R6
100
L1
R18
10
C2
55
18pF
C1
R17
24
R10
200
Q5
CR2
Q6
R80
316
R220
147
R16
200
R7
590
R11
82.5
R12
51



P/O BIT RATE BOARD A3
P/O REGISTER BOARD A13
P/O TRIGGER BOARD A15

A9 MOTHER BOARD (08018-66509)



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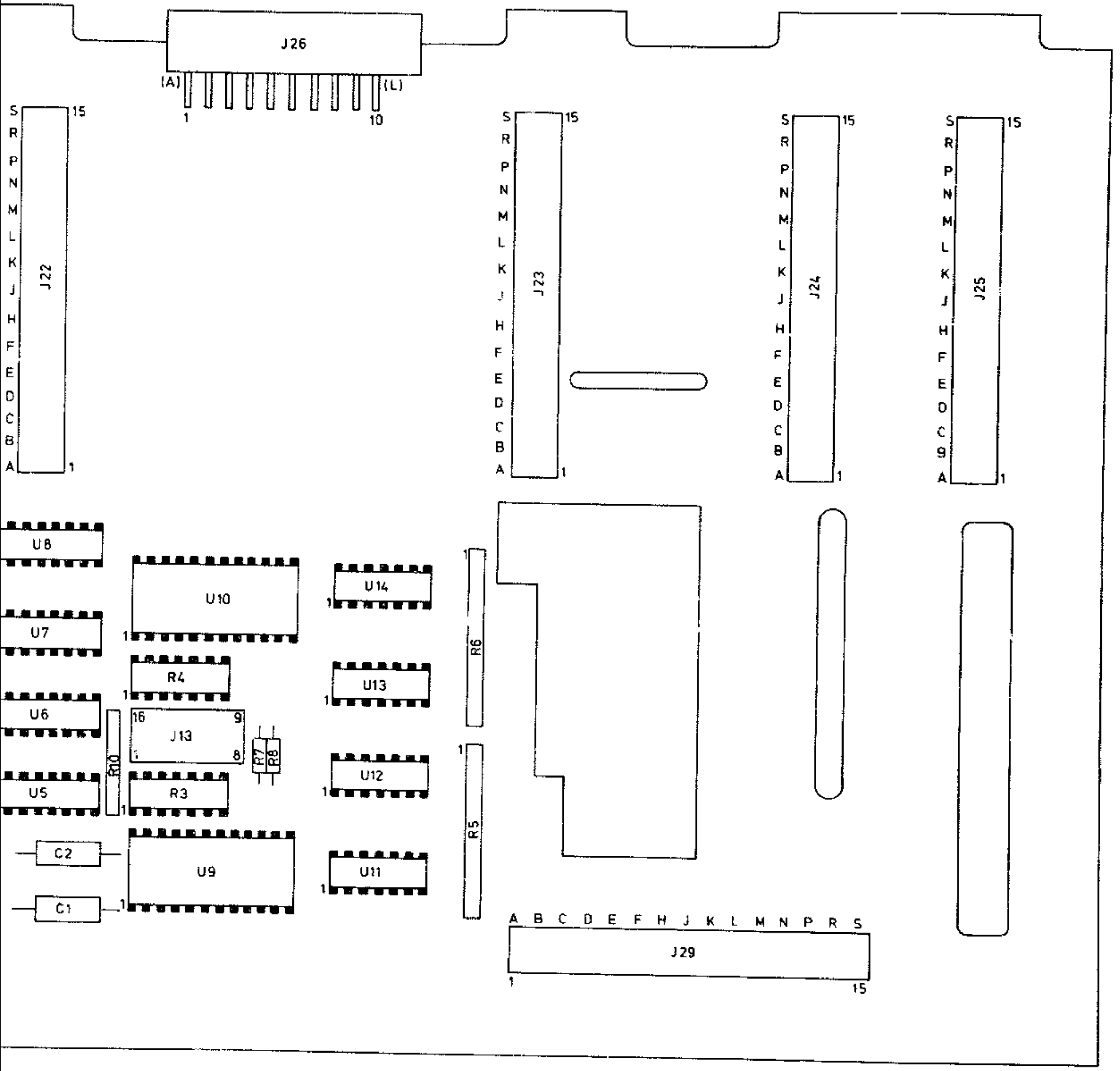

J26
(A)
(L)
1
10
J22
J23
J24
J25
S R P N M L K J H F E D C B A
15
1
U8
U7
U6
U5
U10
U9
U14
U13
U12
U11
R4
R3
R6
R5
R10
R7
R8
J13
16
9
8
C1
C2
J29
A B C D E F H J K L M N P R S

SERVICE BLOCK 4
DATA FORMATTING AND CYCLING A11, A9 5, A4 6, A5 7

THEORY OF OPERATION

Bits per Word Selection and Words per Frame/Word Address Selection (Schematic 5)

Bits per word, words per frame and word address are selected by BCD thumbwheel switches A11 S1 and A11 S2. Whereas switch S2 is always enabled by an ECL high (ground) at the enable inputs, switch S1 is divided into 2 sections, the 'bits per word' section being enabled by the ECL high level signal YBPW, and the 'words per frame' section being enabled by the ECL high level signal YWPF. Should either YBPW or YWPF be in a low state, then the related S1 outputs are set to low.

When the 8018A is active (i.e. data output enabled), the 'bits per word' (BPW) setting and 'words per frame' (WPF) setting are routed via A9 U1/U2 and A9 U3/U4, respectively, to the A4 Data Format Board, where they are compared to the BPW and WPF counter outputs for generation of sync signals.

During data loading and data fetching, the 'bits per word' and the 'word address' information is required to find the correct memory location. The bits per word' part of S1 is therefore enabled by YBPW, and the 'words per frame' part of S1 is disabled (YWPF = low). A low NWAE (word address enable) signal allows the word address setting to be transferred via A9 U5/U6/U7/U8/U3 and U4 to the Data Format Board for loading into the word address count-down counter. (Note: Signal NWAZ (word address zero) is not used in the 8018). If data is loaded or fetched in DATA MODE, the bits per word part of thumbwheel switch S1 is disabled. Signal Y16B (16 Bit) becomes true which automatically sets bits per word at the outputs of A9 U1/U2 to 16 bits (in DATA MODE data must be loaded in 16-bit bytes).

With HP-IB selected, the BPW circuit (A11 S1, A9 U1/U2), WPF circuit (A11 S1, A9 U3/U4) and word address circuit (A9 U3, U4) are disabled. The format information is then derived from the A1 HP-IB board.

Word Mode Readout (Schematic 6)

The number of bits within one frame (cycle) in WORD MODE is the product of the WORD LENGTH (bits per word – BPW) and the NUMBER OF WORDS (words per frame – WPF). To ensure that the correct number of bits are output, therefore, two counters are employed. The BPW counter mainly comprises U1/U8, and the WPF counter mainly comprises U3/U4. Figure 8–4–1 shows a simplified functional diagram of the two counters and their control logic.

In the case of the BPW counter, the start conditions are established during the last clock cycle of the previous word. With YWE (WORD END) true at U16B $\overline{Q}$ output, the low on the Q output presets U8 and U1 (S2 input). On the next clock pulse (i.e. the first of the new word) the binary equivalent of decimal 2 is loaded into the counter. (The junction of CR2/CR3 sets an ECL high onto the D1 input of U8; all other data inputs of U8 and U1 are set to low via the ECL low generated at the junction of CR1/R1). The reason for the bit count starting at 2 is that in any complete word cycle, the first clock pulse is needed to load the start number into the counter, and the last clock pulse is required to clock the detected 'end of word' at U17/pin 14 through flip-flop U16B. To accommodate these requirements within a word cycle, therefore, at the same time ensuring that the correct number of bits are output, the bit count is equal to the preset WORD LENGTH minus two.

With the last clock cycle within a word being needed to clock the 'end of word' through U16B, the counter outputs during this cycle are no longer equivalent to the thumbwheel switch inputs to EX-OR gates

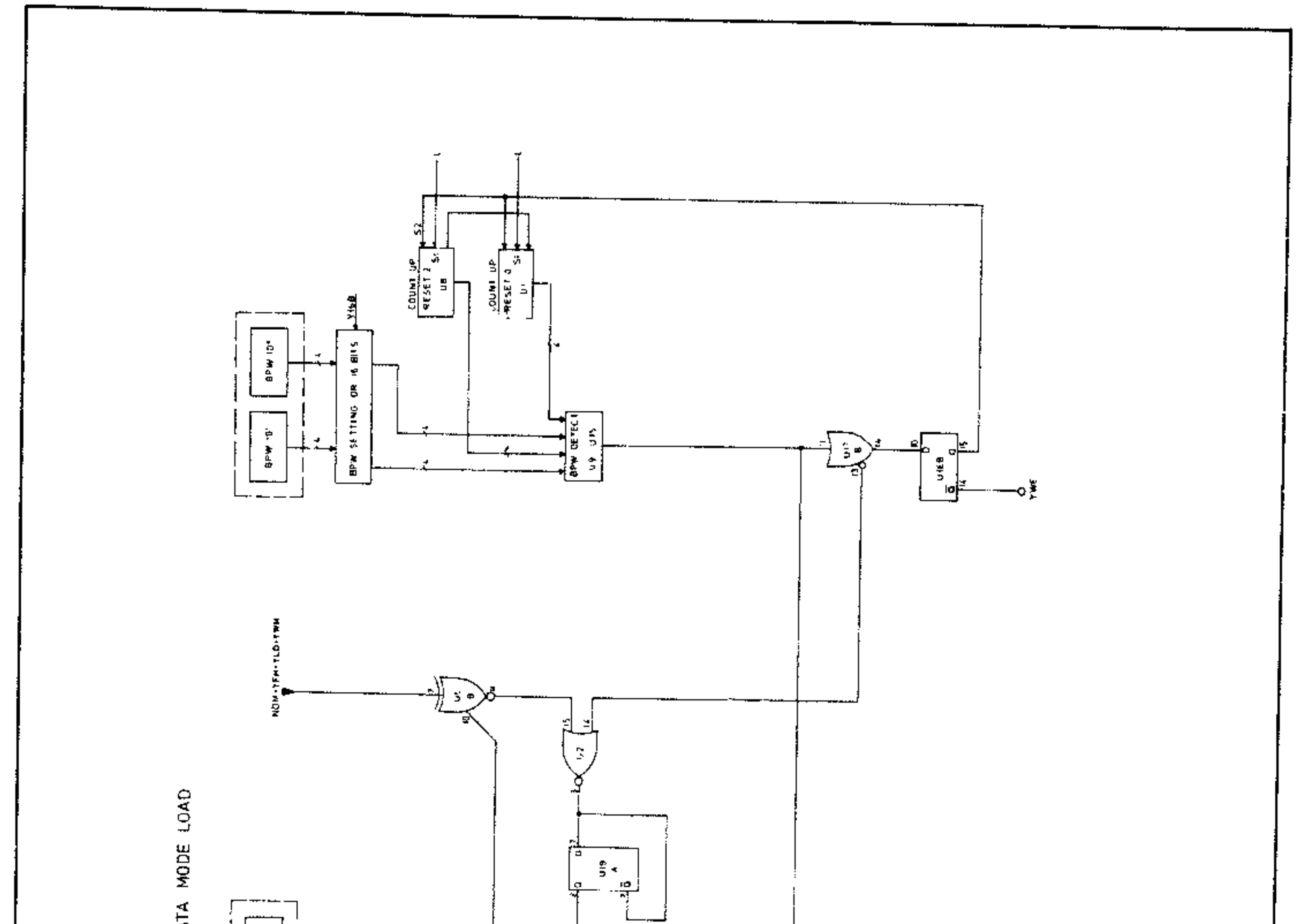


Figure 8–4–1. Functional Diagram for Word Mode Readout

U9/U15. A high is therefore generated at U17B pin 14, this high being clocked through U16B on the first clock pulse of a new word. With a high on the S2 inputs of counter U1/U8, the counter is in increment mode, and remains in increment mode until equivalence is again detected by U9/U15. As already described, the resulting low is then clocked through U16B to the S2 inputs for presetting purposes.

The equivalence detection at U9/U15 output is also routed via U17B pin 13/U2/U19A as a carry signal for the WPF counter U4/U3.

In the case of the WPF counter, it is preset on the last clock cycle of a frame, the necessary low on the S1 inputs being derived from the 'last bit' detect at U17A pin 2. During the last clock cycle within a frame, the YL signal is true i.e. high, and U20B Q output is low (the D-input of both flip-flops U20B and U19B being set low on the previous clock cycle by the 'last bit' detect U17A pin 2). During the first clock cycle of a new frame, therefore, the binary coded NUMBER OF WORDS setting is loaded into the counter. Also during this cycle, the signal YL is 'not true', U20 Q output is now high thus putting the counter in decrement mode via its S1 inputs. Each carry signal from the BPW counter then decrements the WPF counter until U3 registers zero at its outputs and U4 registers decimal 1. Because WORD MODE is selected, EX-OR gate U5C pin 15 is high, therefore at count 1, the high on U5C pin 14 generates a low at U5C pin 13 (all outputs of counter U3/U4 are low except the U4 Q0 output). One word before the selected NUMBER OF WORDS, therefore, a low level is established at U17A pin 7 and U11B pin 11. When the BPW counter counts up to the WORD LENGTH setting during the last word, U17A pin 6 also goes low due to the 'word end' detect action of U9/U15 thus generating the last bit signal, NL, at U17A pin 2.

The inverted signal at U11B pin 14 during last word is the qualifier YWA (word address is reached) for the ASM in fetch and load operations.

Note: Additional conditions during fetch and load:

1. Signal YL is supressed by YDLP (Disable Last Pulse) from the ASM which holds Flip-Flop U19B in a set conditions.
2. Start (preset) conditions for the BPW counters are established by resetting U16B with YR (Reset) from the ASM. YR also presets the WPF counters via U25D and U20B/Q.
3. The control clock (YCCL) replaces the read clock YCL1.

Data Mode Readout (Schematic 6)

When DATA MODE is selected, the decimal number set at the thumbwheel switch A11 S1 is the number of bits genreated within one data stream. Similar to that described in WORD MODE, two counters are employed such that the BPW (U1/U8) counter now counts up to 99 (this being repeated according to the multiple of 10^2 set for the DATA STREAM LENGTH e.g. for LENGTH 980, the BPW counter counts 9 times up to 99, the 10th count being up to 80), and counters U4 and U3 count multiples of 10^2 and 10^3 respectively. Whereas counter U1/U8 operates in increment mode during data generation, counter U3/U4 operates in decrement mode, the decrement clock being the carry signal derived from U1/U8. This carry signal is derived via the '98' detect at U2 input pins 4, 7 and 12 – as opposed to the carry signal in WORD MODE at pin 14 (U2) which is now disabled by the NDM signal at U5B/pin 7 (U5/pin 11 is now high). A functional diagram is given in Figure 8–4–2. The conditions for presetting the counters (i.e. low on both S1 and S2 inputs) are established during the last clock cycle of a data stream readout. On the second last clock cycle, a low is present at the U11A pin 2 output due to the 'zero detect' signal from U5C pin 13 (inverted at U11 pin 12 to a high state). On the last clock cycle, therefore, this low is clocked through flip-flop U16B to the S2 inputs of U1/U8 for presetting. The first clock pulse of the new data stream then clocks decimal 2 into the counter (see WORD MODE description for an explanation of the decimal 2 start condition). Simultaneously for counter U3/U4, during the second last clock cycle of the data stream, a low is present at U17 pin 2 due to the 'last bit' detect (YL). This low is also clocked through flip-flop U20 on the last clock cycle, thus allowing the 10^2 and 10^3 digits in the selected DATA STREAM LENGTH to be loaded into counter U3/U4 on the first clock pulse of the new data stream (on condition that the DATA STREAM LENGTH is > 99).

The necessary counter preset conditions are established during fetch and load operations via the YR signal from the control ASM. Signal YR resets both flip-flops U16B and U20B to provide the necessary low at the Q outputs for presetting the counters.

During the first clock cycle of a data stream the counters are not only loaded with the start number, in addition, highs at the Q outputs of flip-flops U16B and U20B (the conditions generating the lows during the previous clock cycle are no longer true e.g. last bit) change the mode of counters U1/U8 and U3/U4 to increment and decrement respectively.

> Note: If the DATA STREAM LENGTH is < 100, all inputs to counter U3/U4 are low which is detected by gates U7A and U7B. The resultant high at U7A pin 3 thus disables the C input of U4, and only counter U1/U8 is in operation. Additionally the resultant low at U7A pin 2 is inverted by U25A to reset flip-flop U20B, the low at the Q output holding counter U3/U4 in preset mode.

After loading, counter U1/U8 counts up to 98, the 10^0 and 10^1 coincidence detect, via gates U9 and U15, being suppressed via the wired-OR connection of U17 pin 14 and U11A pin 2. A high is present at U11A pin 2 due to the lows on pins 5 and 6 of U11A (pin 6 is held low by U5 pin 10 which in turn is held low by the true NDM signal; pin 5 is low due to the non-zero detect state of U5C pin 13 which is in turn inverted at U11B pin 12) thus holding the D-input of flip-flop U16B high and preventing the counter U8/U1 being preset by a low to the S2 input. Upon reaching 98, U2 pin 3 goes low, this being clocked through U19A on the 99th clock pulse to provide the carry signal for U4/U3.

After counter U3/U4 has counted down to zero, U5C pin 13 is low, which in turn causes U11A pin 2 to go low. During the next count-up sequence of counter U1/U8, therefore, the $10^0/10^1$ coincidence detect signal at U17 pin 14 is no longer suppressed and enables the YWE signal to be generated, and the counters are once more preset. U17A pin 2 also goes low to generate the last bit signal (YL) which is used to preset counter U3/U4.

Mixed Mode Readout (Schematic 6)

A simplified functional diagram of the control logic in MIXED MODE is given in Figure 8–4–3. As can be seen from this diagram, the main functional elements are the WPF and BPW counters, and the 4 flip-flops U13A, U16B, U19A and U20A. The two counters operate as already described in 'WORD

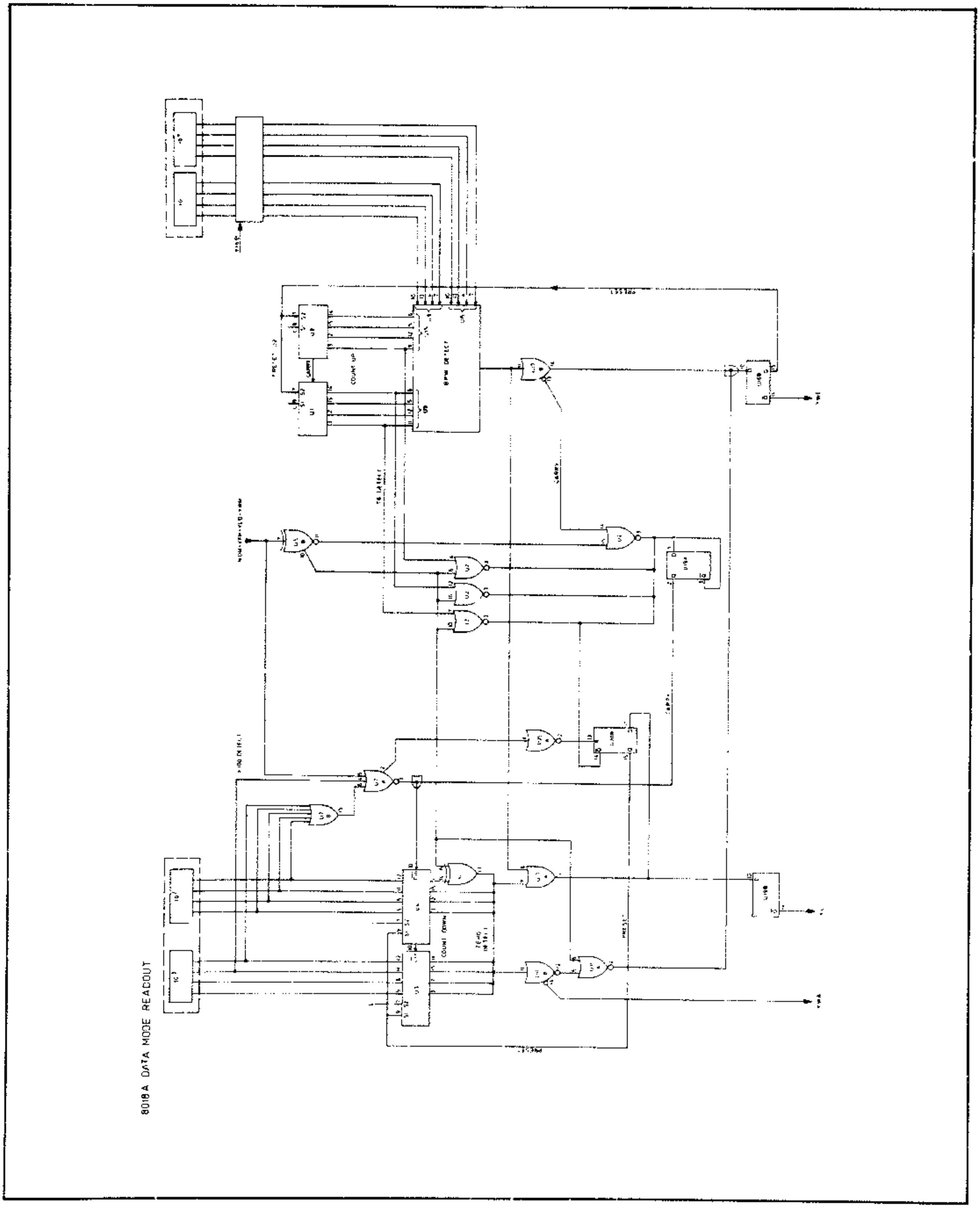


Figure 8–4–2. Functional Diagram for Data Mode Readout

MODE Readout', the BPW counter operating in increment mode after being preset to the start number 2, and the WPF counter operating in decrement mode after presetting, the decrement clock being derived from the 'word end' (YWE) detect signal at U9/U15 output. The main functions of the 4 flip-flops are given as follows:

- U16B is employed basically for generating the YWE signal and the preset condition (low at the S2 inputs of the BPW counter) for the BPW counter.
- U20A is employed to switch the PRBS generator on/off as well as disabling the carry signal to the WPF counter for each word immediately prior to the PRBS generation (i.e. Word 1, 3, 5 etc).
- U13A is basically employed to generate signal YH which stops the RAM multiplex counter during PRBS generation, and also disables the BPW detect logic U9/U15 during PRBS generation.
- U19A generates the carry signal which decrements the WPF counter and clocks U20A to provide the necessary output states during PRBS or word generation.

A more detailed description of MIXED MODE operation is given as follows and is based on the timing diagram Figure 8–4–4. As already described in 'WORD MODE Readout', the preset conditions for the BPW counter and WPF (NUMBER OF WORDS) counters are established during the last two clock cycles of the previous frame. On the second last clock cycle, a low is generated at U17 pin 14 (word end detect) and U17 pin 2 (last bit detect), each of which is clocked through flip-flops U16B and U20B on the last clock cycle for presetting the requisite counters. The first clock cycle of the new frame clocks the preset numbers (2 into the BPW counter and NUMBER OF WORDS into the WPF counter) into the respective counter, at the same time setting the BPW counter to increment mode (a high is generated at U16B Q output on the first clock cycle of a frame as 'word end' (YWE) is no longer true – a high at the S2 inputs setting the counter to increment mode) and the WPF counter to decrement mode (a high is generated at U20B Q output because 'last bit (YL) is no longer true on the first clock cycle of a frame – a high at the S1 inputs setting the counter to decrement mode).

Another important start condition is generated at flip-flop U20A outputs at the end of a frame. The YPRBST signal at the end the last PRBS sequence in a frame sets U20A, which in turn puts a low on the $\overline{Q}$ output. This low is then combined with the low MIXED MODE signal at gate U6C to generate a low at the D-input of U20A during the last word of a frame. Upon generation of the last carry signal at the end of the last word, the low is clocked through U20A to the Q output. During WORD 1 generation, therefore, a low is present at pins 9 and 11 (YPRBST not true) of U12B, the high at pin 10 of U12B (due to the BPW detect output being high) disabling the PRBS generator via signal NPRBSH. At the end of WORD 1, the BPW detect output goes low (on second last clock cycle) which removes the disable signal (NPRBSH now high) from the PRBS generator, at the same time blocking the 'carry' signal to the WPF counter by holding the D-input of U19A high (via the wired-OR arrangement of U2 pin 3 and U12 pin 12).

Simultaneously, the BPW detect low sets U10A pin 3 high (input pin 7 is low due to the U20A $\overline{Q}$ high – see last paragraph; input pin 11 is also low until the end of a PRBS burst), this high being clocked through flip-flop U13A on the last clock cycle of WORD 1. With a high at the Q output of U13A, the BPW detect is disabled (all outputs of U15/U9 remain low as long as a high is present at the enable inputs), and the low on the $\overline{Q}$ output sets YH true via gate U12A, which stops the RAM multiplex counter on board A6 during PRBS generation. Also, the feedback loop from U13A $\overline{Q}$ output via gate U6B ensures that the D-input is held high during PRBS generation.

Upon the second last clock cycle before PRBS completion, signal YPRBST is generated (and remains true during the last clock cycle) which sets flip-flop U20A, removes the high from the D-input of U13A, removes the 'carry suppress' signal at U12 pin 12, and generates the NPRBSH signal at U12B pin 13 to disable the PRBS generator. On the last PRBS clock cycle, therefore, the BPW detect is enabled by the U13A Q output; signal YH is 'not true' due to the high on the U13A $\overline{Q}$ output, thus enabling the RAM multiplex counter once more; and a carry signal is generated at U19A Q output for the WPF counter. Note: This carry signal has no effect on the U20A output as the YPRBST signal is still true at the set input.

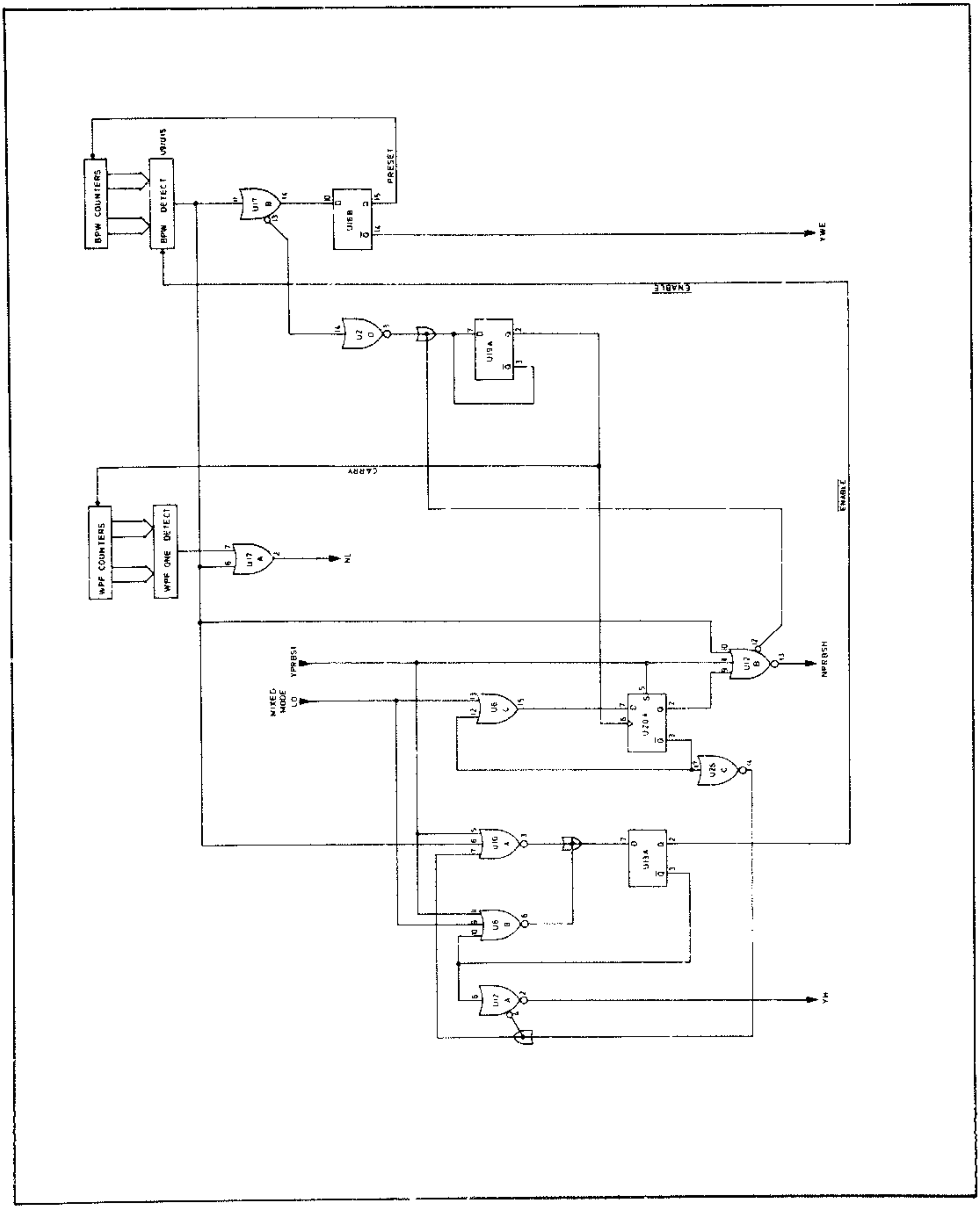


Figure 8–4–3. Mixed Mode Functional Diagram

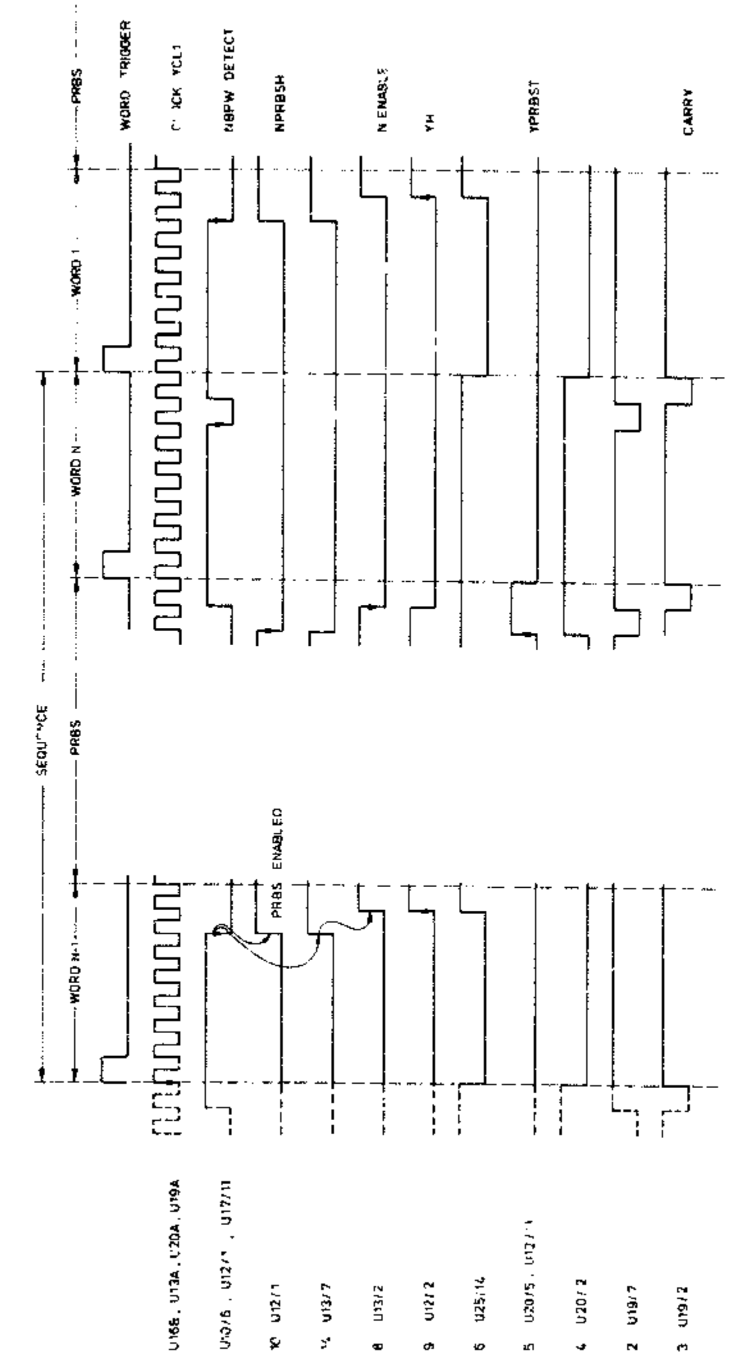


Figure 8–4–4. Mixed Mode Timing Diagram

During WORD 2 generation, the Q output of U20A is high, U12B pin 12 is low, thus the carry signal generated by the BPW detect at the end of WORD 2 passes through flip-flop U19A (the D-input is no longer held high as in WORD 1). The low on the D-input of U20A is then clocked through to the Q output, and the start conditions at the gate U12B inputs for WORD 3 are identical to those at the beginning of WORD 1 (a low on pins 9 and 11 and a high on pin 10). The logic operations already described for WORD 1 are now repeated for WORD 3 and all subsequent odd-numbered words (5, 7, 9 etc). Similarly, all even-numbered words (4, 6, 8 etc) are as described for WORD 2 generation.

The 'last bit' (NL) signal is generated at U17 pin 2 after WPF and BPW detection (see WORD MODE Readout description). For a description of PRBS operation in MIXED MODE – see the 'Note' at the end of the 'PRBS MODE Readout' description.

PRBS Mode Readout (Schematic 7)

With PRBS MODE selected, the number set at the thumbwheel switch A11 S2 determines the shift register length (i.e. 9, 10, 15 or 20 flip-flops) for PRBS generation. The shift register and its associated feedback loops are enabled via gate U10B pins 14 and 12 respectively. (The 2 enable signals are low due to the permanent high in PRBS MODE at J14D pin 15). A third output of gate U10B , pin 13, is used to enable the PRBS TRIG output by applying a low to gate U5B pin 9. During a PRBS cycle, a condition is arrived at whereby all flip-flops (with the exception of U9D) in the shift register have a logic '0' at their Q outputs. This 'all-zero' state is detected by gates U4A, U11A, U11B, U13A and U13B, the resultant low being routed to U5B pin 11. Simultaneously, the logic '1' at the U9D Q output (at least one Q output within the shift register must be at logic '1' to ensure continued PRBS generation) is inverted by U5C and routed to U5B pin 10. U5B pin 6 then goes high, this high being clocked through flip-flop U16 on the next clock cycle to generate PRBS TRIG.

Throughout PRBS generation, whenever a logic '1' is present at U9D Q output, it is fed back via gate U5C and one of gates U2A, U2B, U2C or U12A for re-entry into the shift register, and thus ensure continued PRBS generation.

At power-on, in the event that all 20 flip-flops in the shift register indicate logic '0', a logic '1' is generated via gate U5D and applied to the D-input of flip-flop U9D. On the first clock pulse after power-on, in this case, a high is then generated at U9D Q output, this being fed back, as already described, into the shift register for continued PRBS.

> Note: The prevailing conditions in MIXED MODE of operation are different to those just described for PRBS MODE. In MIXED MODE, U14D pin 15 is low, which is transferred after 2 clock cycles (via flip-flop U9E) to flip-flop U9C Q output, thus enabling gate U10A. In MIXED MODE, the 'all zero' state (of flip-flops 2 to 20) which occurs in every PRBS cycle is now defined as the end of the cycle. At this stage, pins 5 and 6 of 10A and pins 4 and 5 of U5A are all low, causing U10A pin 2 and U5A pin 3 to go high. Signal YPRBST is thus generated and the resultant NPRBSH signal stops the PRBS generator for a time depending upon the selected WORD LENGTH setting. (With NPRBSH low, the shift register and its associated feedback loops are disabled via U10B pins 12 and 14). Signal YPRBST remains high for 2 clock cycles due to the time required for the high at U5D, pin 15 to be clocked through to flip-flop U9C Q output. The signal duration of YPRBST is thus independent of WORD LENGTH setting.

Cycling

The main control element in the cycle logic circuitry is U22A/U22B. In AUTO CYCLE U22B is permanently enabled (a low at pin 11) thus allowing the main clock (NCL1) through at pin 10 to the BPW and WPF counters. In BIT, WORD and FRAME CYCLE, U22B is enabled according to which cycle mode is selected and to which external cycle command is used in conjunction i.e. External Cycle Command (YECC), Manual Cycle Command (YMCC) or Remote Cycle Command (YRC).

When BIT, WORD or FRAME CYCLE is selected, the AUTO CYCLE pushbutton is released which applies a low level to:

- U6A pin 5 to enable the cycle detect circuit U13B, U18A and U6A.
- U22A pin 4
- U23D pin 10 to enable the external cycle command inputs YECC, YMCC and YRC (U24C is disabled by a high at pin 11).

The following description describes how the various external cycle commands affect the control logic in BIT, WORD and FRAME CYCLE.

Bit Cycle: In BIT CYCLE output U5A pin 3 and U23 pin 15 are high and disable gates U10A and U10B. Also, U24B pin 6 is high which enables gate U24A by applying a low to pin 4 and sets U21B/6 to low.

The positive transition of YMCC or YRC cycle command then clocks flip-flop U14 Q output to high. This high is routed via gates U21C and U24A to set U22A pin 3 low, which enables the clock generator. The first positive transition (clock) at U18B pin 13 is then routed back to set flip-flop U14 and return the $\overline{Q}$ output to low, which disables the clock generator. (This low is routed via gates U21C and U24A to set U22A pin 3 to high). Irrespective, therefore, of how long YMCC or YRC remains high, only one bit is generated. With the YECC command, however, bits are generated for the duration of the cycle command. In this case, the high at U21C pin 12 is routed via U24A to set U22A pin 3 low for the duration of the YECC pulse period.

Word Cycle: In WORD CYCLE, U23C pin 15 is low which enables gate U10A to detect 'bits per word' (BPW). Gate U10B is disabled by the high at U5A pin 3. Also in WORD CYCLE, the signal YBC (bit cycle) is now low at pin U21B pin 10. Via U24B and U24A, U22A/6 is set to low. The positive transition of a YMCC or YRC cycle command then sets flip-flop U14 $\overline{Q}$ output high, which in turn sets U21B pin 6 high via U21C. This sets U22A pin 3 low and the clock generator is enabled. Although the first positive transition at U18B pin 13 causes U14 $\overline{Q}$ output to return to low, flip-flop U21A/U21B does not toggle until the reset pulse appears at U21B pin 9. This reset pulse is generated after a word cycle has been detected and causes U21B pin 6 to go low and disables the clock generator via U22A. A complete word is generated, therefore, for each transition of a YMCC or YRC command (assuming the transition does not occur during word generation). With the YECC cycle command, however, words are generated for the duration of the cycle command (a word being completed when the command ends during a word). In this case, the high YECC command prevents flip-flop U21A/U21B from toggling (via U21C) even when a reset pulse occurs from the BPW detect gate U10A.

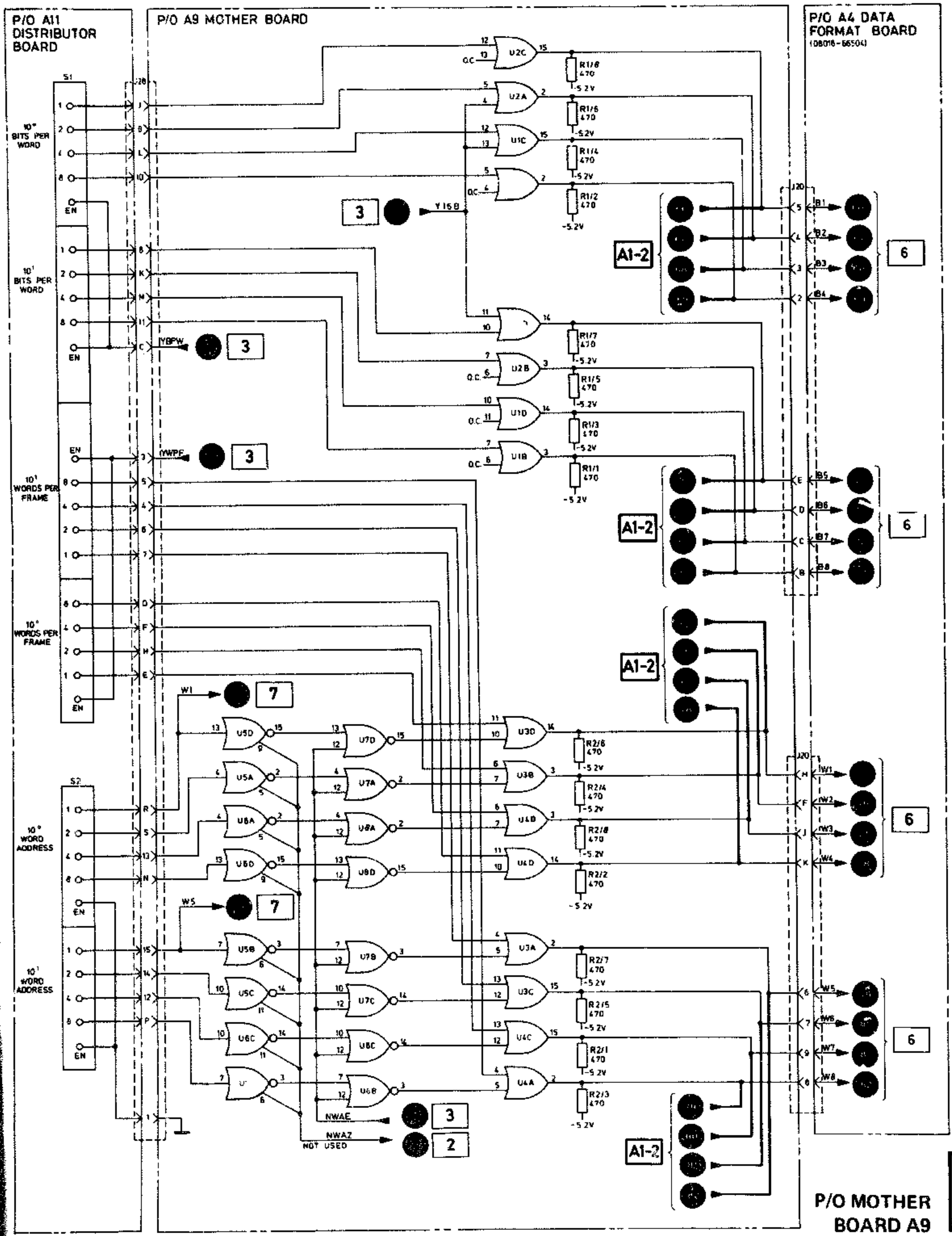
Frame Cycle: In FRAME CYCLE, U5A pin 3 is low which enables gate U10B to detect BPW (bits per word) and WPF (words per frame). Also in FRAME CYCLE, the signal YBC (bit cycle) is now low at pin U21B pin 10 thus enabling flip-flop U21A/U21B. The positive transition of a YMCC or YRC cycle command then sets flip-flop U14 $\overline{Q}$ output high, which in turn sets U21B pin 6 high via U21C. This sets U22A pin 3 low and the clock generator is enabled. Although the first positive transition at U18B pin 13 causes U14 $\overline{Q}$ output to return to low, flip-flop U21A/U21B does not toggle until the reset pulse appears at U21B pin 9. This reset pulse is generated after a frame cycle has been detected and causes U21B pin 6 to go low and disables the clock generator via U22A. A complete frame is generated, therefore, for each transition of a YMCC or YRC command (assuming the transition does not occur during frame generation). With the YECC cycle command, however, frames are generated for the duration of the cycle command (a frame being completed when the command ends during a frame). In this case, the high YECC command prevents flip-flop U21A/U21B from toggling (via U21C), even when a reset pulse occurs from the frame detect gate U10B.

TROUBLESHOOTING

The following procedure is given as a troubleshooting aid for PRBS Board A5.

1. Remove jumpers A and B. Jumper A interrupts the feedback in order to check the flip-flop chain. Jumper B disconnects the internal clock.
2. Select PRBS length n = 20.
3. Connect the D input of U6A to ECL low.
4. Check that the feedback path is only enabled via U12A.
5. Using a pulse generator in manual clock mode and ECL level output pulse, clock slowly through the register.
6. Using an ECL Logic Probe or an Oscilloscope, check the Q outputs of the flip-flops.

Repeat steps 3 to 6 with U6A/D connected to ECL high (ground).



P/O MOTHER BOARD A9

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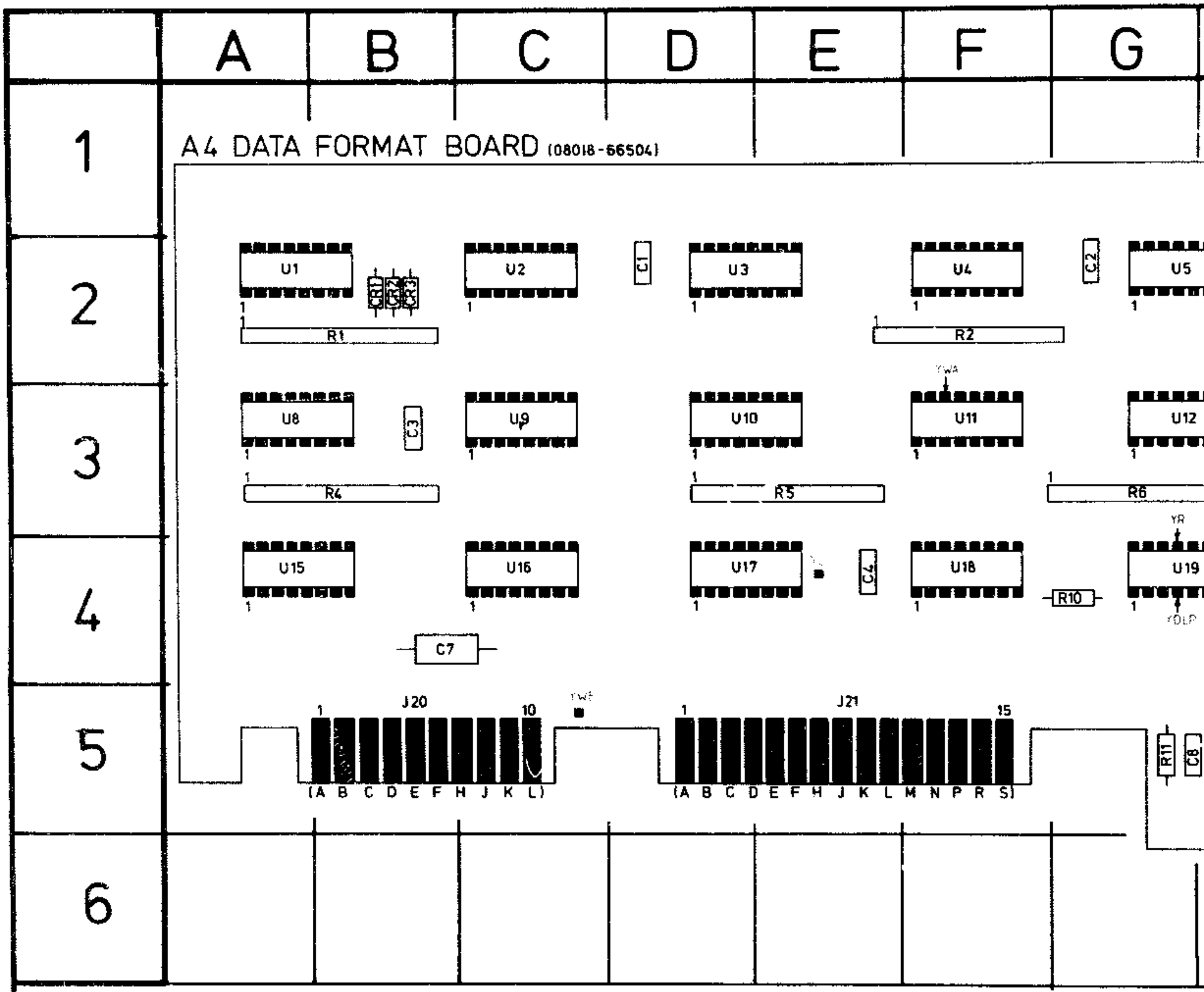
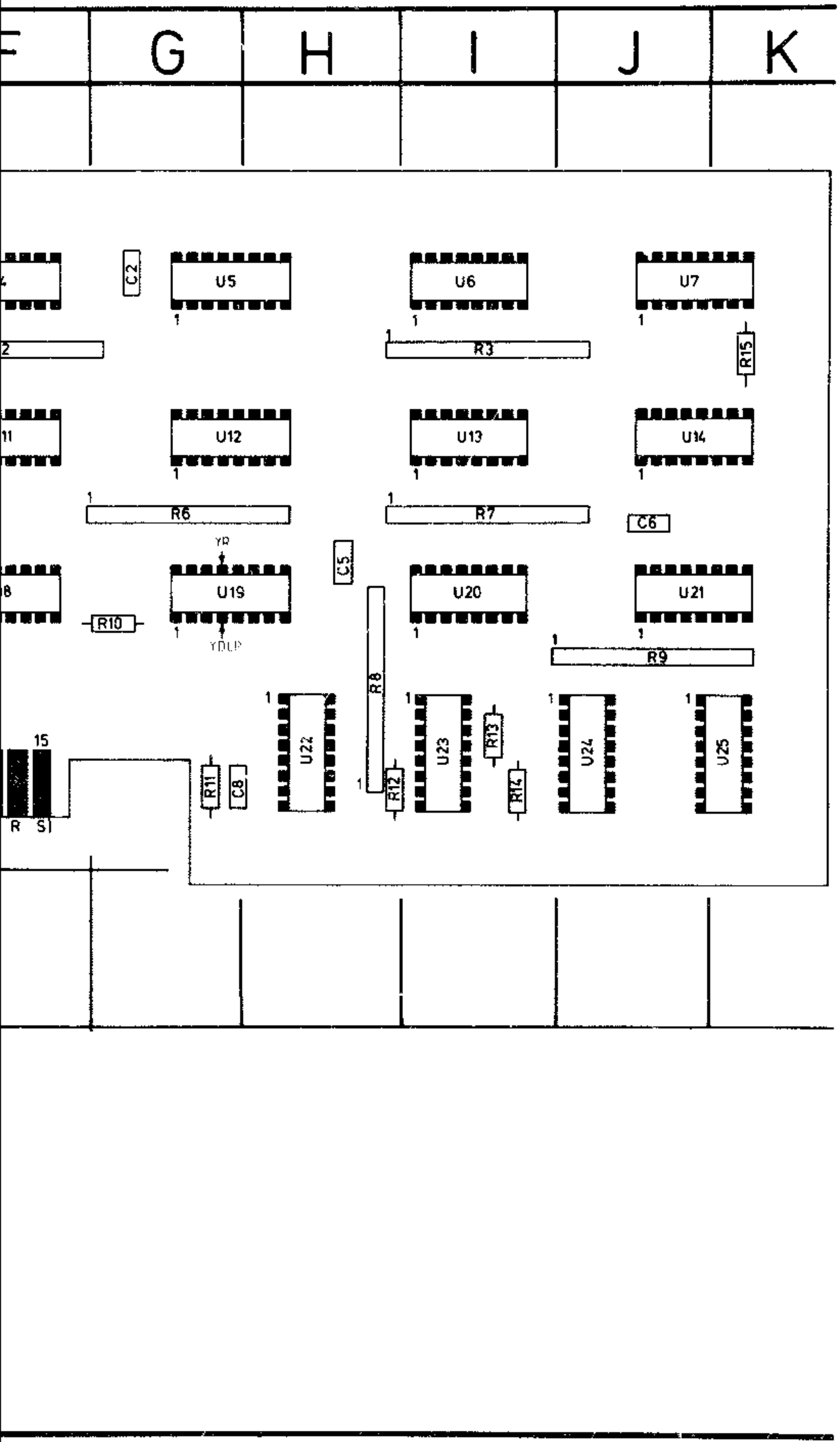
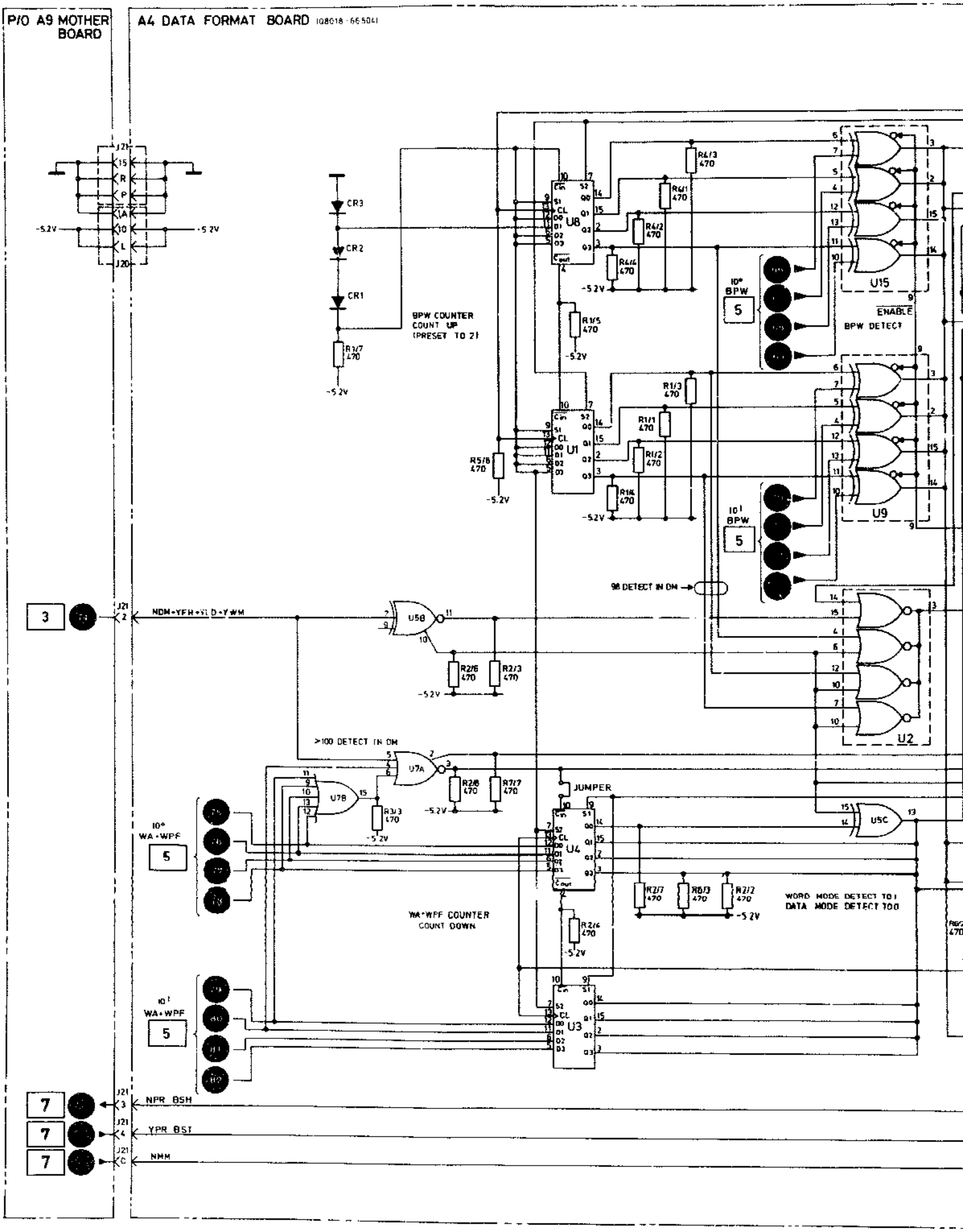

A4 DATA FORMAT BOARD (08018-66504)
A
B
C
D
E
F
G
1
2
3
4
5
6
U1
U2
U3
U4
U5
CR1
CR2
CR3
C1
C2
R1
R2
U8
U9
U10
U11
U12
C3
YWA
R4
R5
R6
YR
U15
U16
U17
U18
U19
C4
R10
YDLP
C7
J20
J21
TWE
R11
C8
(A B C D E F H J K L)
(A B C D E F H J K L M N P R S)

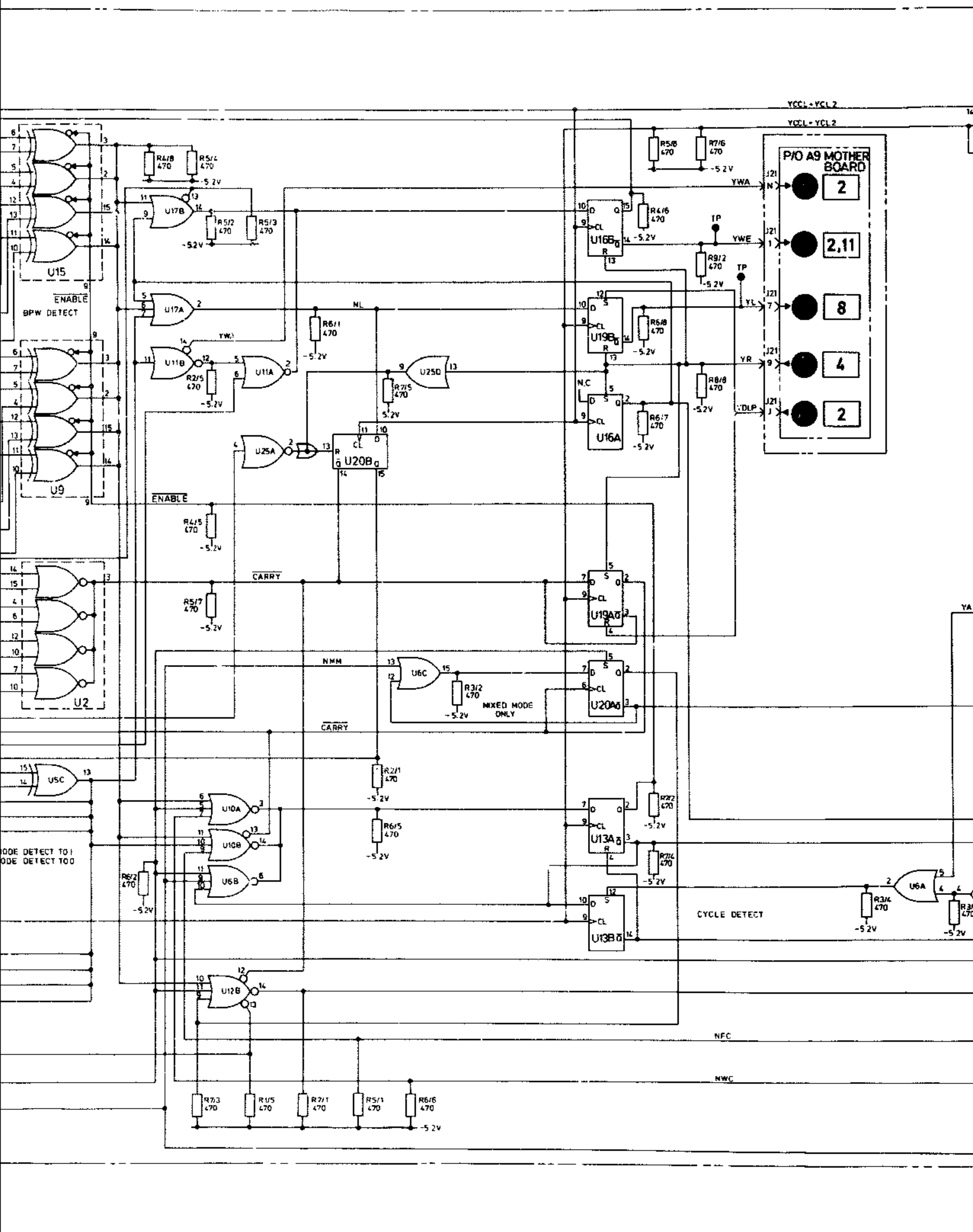
6



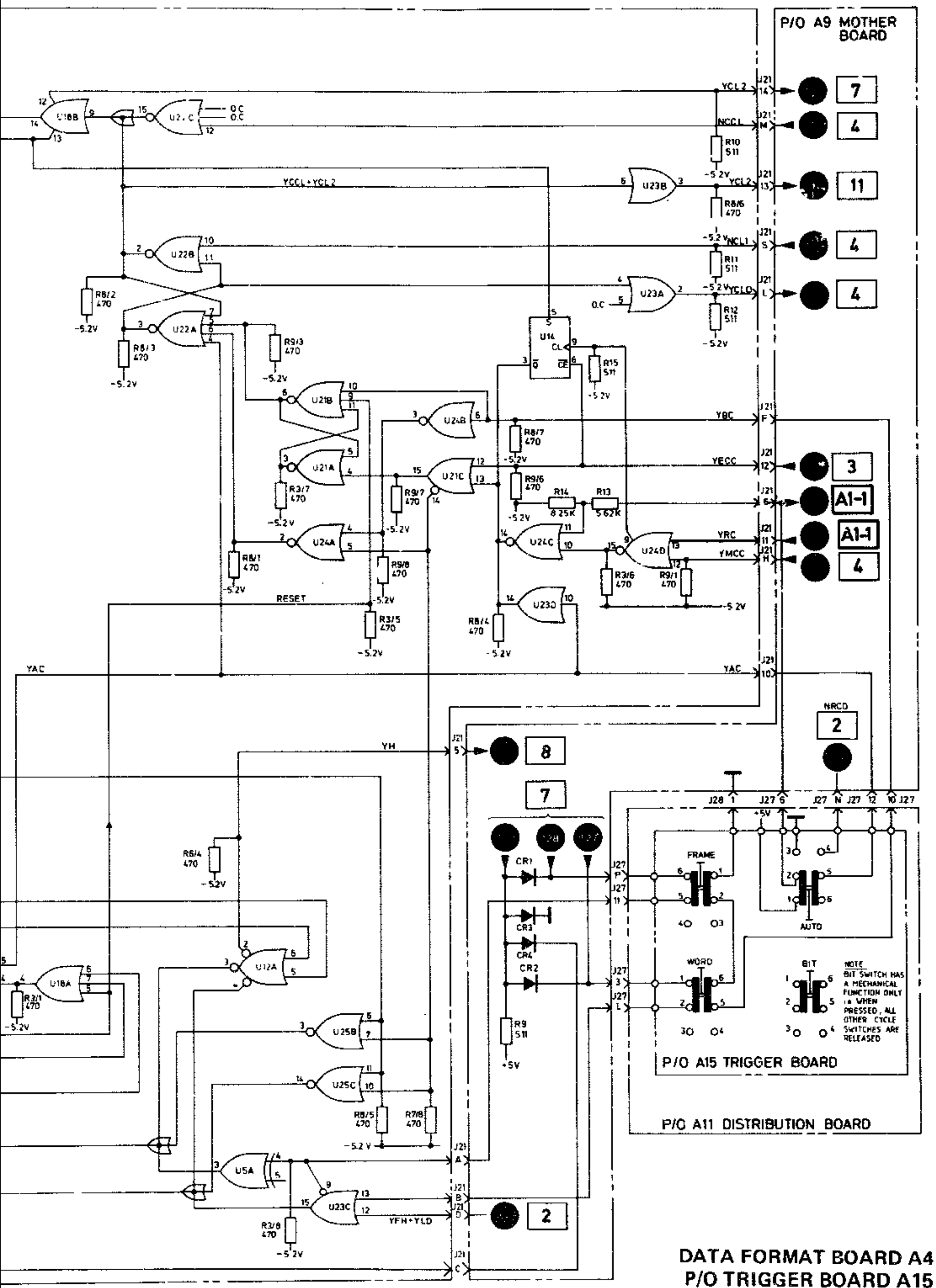
REF DESIG	GRID LOC
C1	D2
C2	G2
C3	B3
C4	E4
C5	H3/4
C6	J3
C7	B4
C8	G5
CR1	B2
CR2	B2
CR3	B2
R1	A/B2
R2	F2
R3	I2
R4	A/B3
R5	D/E3
R6	G3
R7	I3
R8	H4/5
R9	J4
R10	G4
R11	G5
R12	H5
R13	I5
R14	I5
R15	K2
U1	A/B2
U2	C2
U3	D/E2
U4	F2
U5	G/H2
U6	I2
U7	J/K2
U8	A/B3
U9	C3
U10	D/E3
U11	F3
U12	G/H3
U13	I3
U14	J/K3
U15	A/B4
U16	C4
U17	D/E4
U18	F4
U19	G/H4
U20	I4
U21	J/K4
U22	H5
U23	I4/5
U24	J4/5
U25	K5



P/O A9 MOTHER BOARD
A4 DATA FORMAT BOARD (08018-66504)
BPW COUNTER COUNT UP (PRESET TO 2)
10° BPW
5
10¹ BPW
5
ENABLE
BPW DETECT
98 DETECT IN DM
NDM+YFR+YLD+YWM
>100 DETECT IN DM
JUMPER
10° WA+WPF
5
10¹ WA+WPF
5
WA+WPF COUNTER COUNT DOWN
WORD MODE DETECT TO 1
DATA MODE DETECT 100
3
7
NPR BSH
7
YPR BST
7
NMM
-5.2V

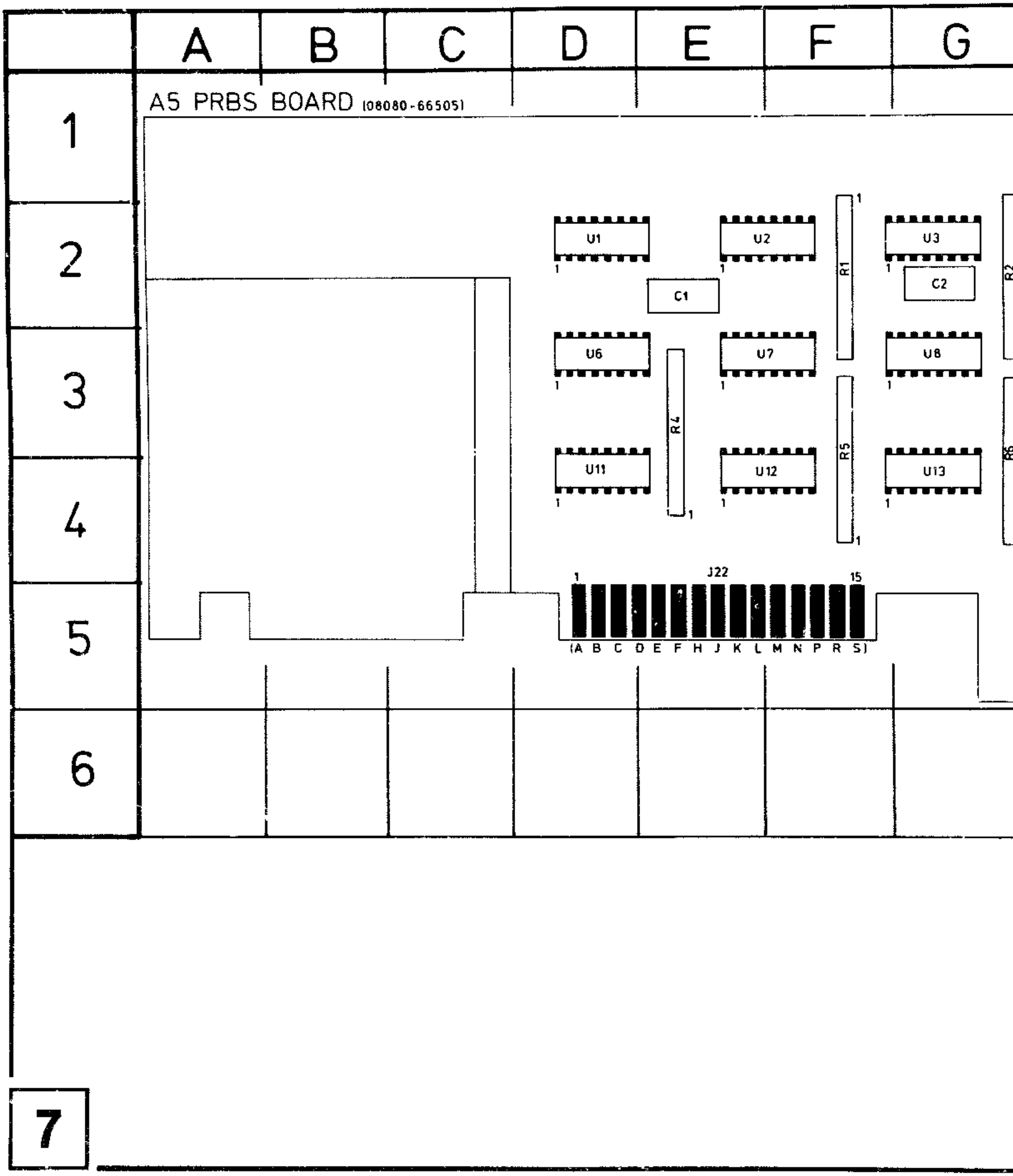


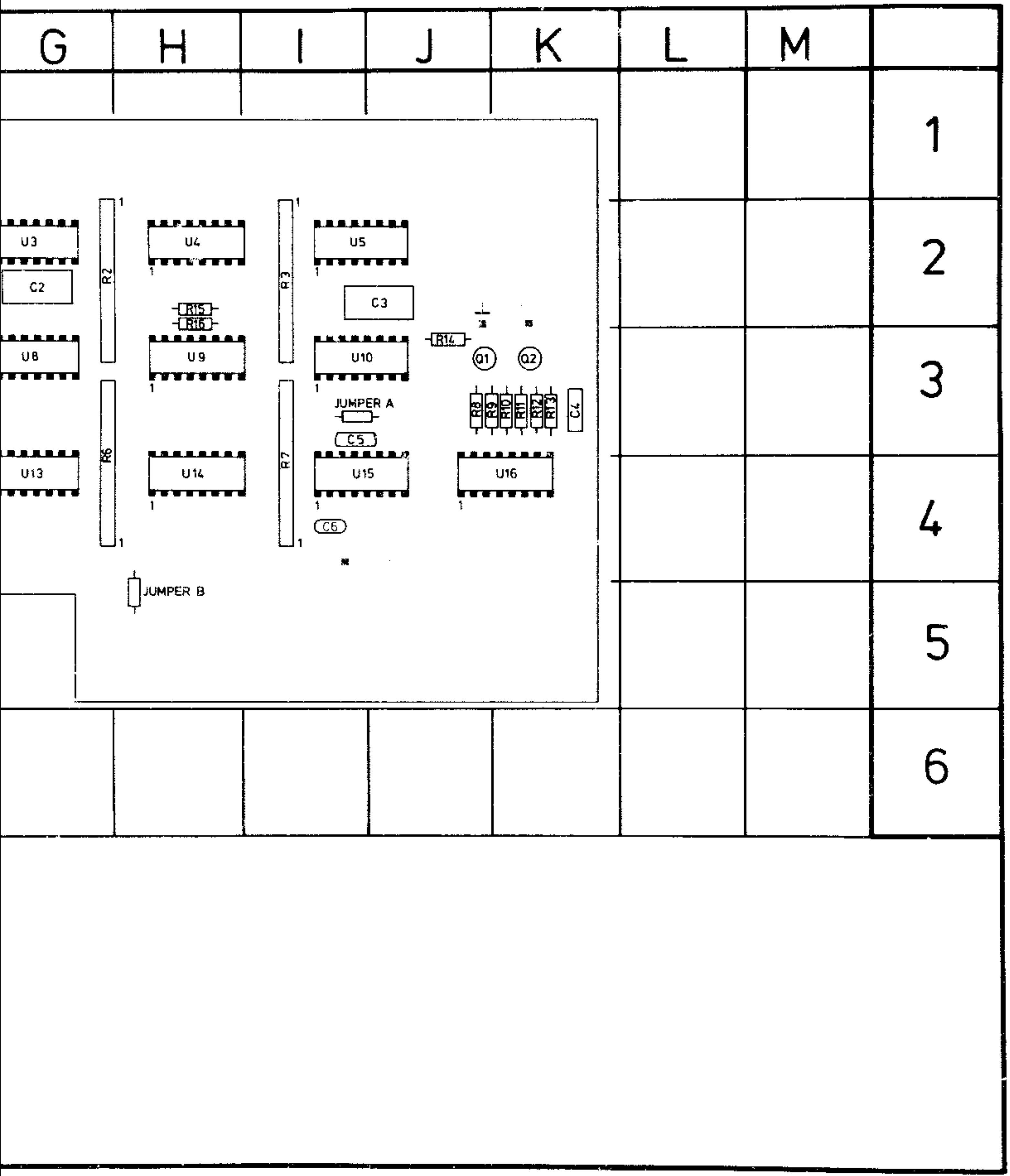
U15
ENABLE
BPW DETECT
U9
U2
U17B
U17A
U11B
U11A
U25A
U25D
U20B
U16B
U19B
U16A
U19A
U20A
U13A
U13B
U6C
U5C
U10A
U10B
U6B
U12B
U6A
YWA
YWE
YL
YR
YDLP
TP
NL
CARRY
NMM
MIXED MODE ONLY
CYCLE DETECT
NFC
NWC
YCCL + YCL 2
YCCL • YCL 2
P/O A9 MOTHER BOARD
J21
2
2,11
8
4
2
-5.2V
470

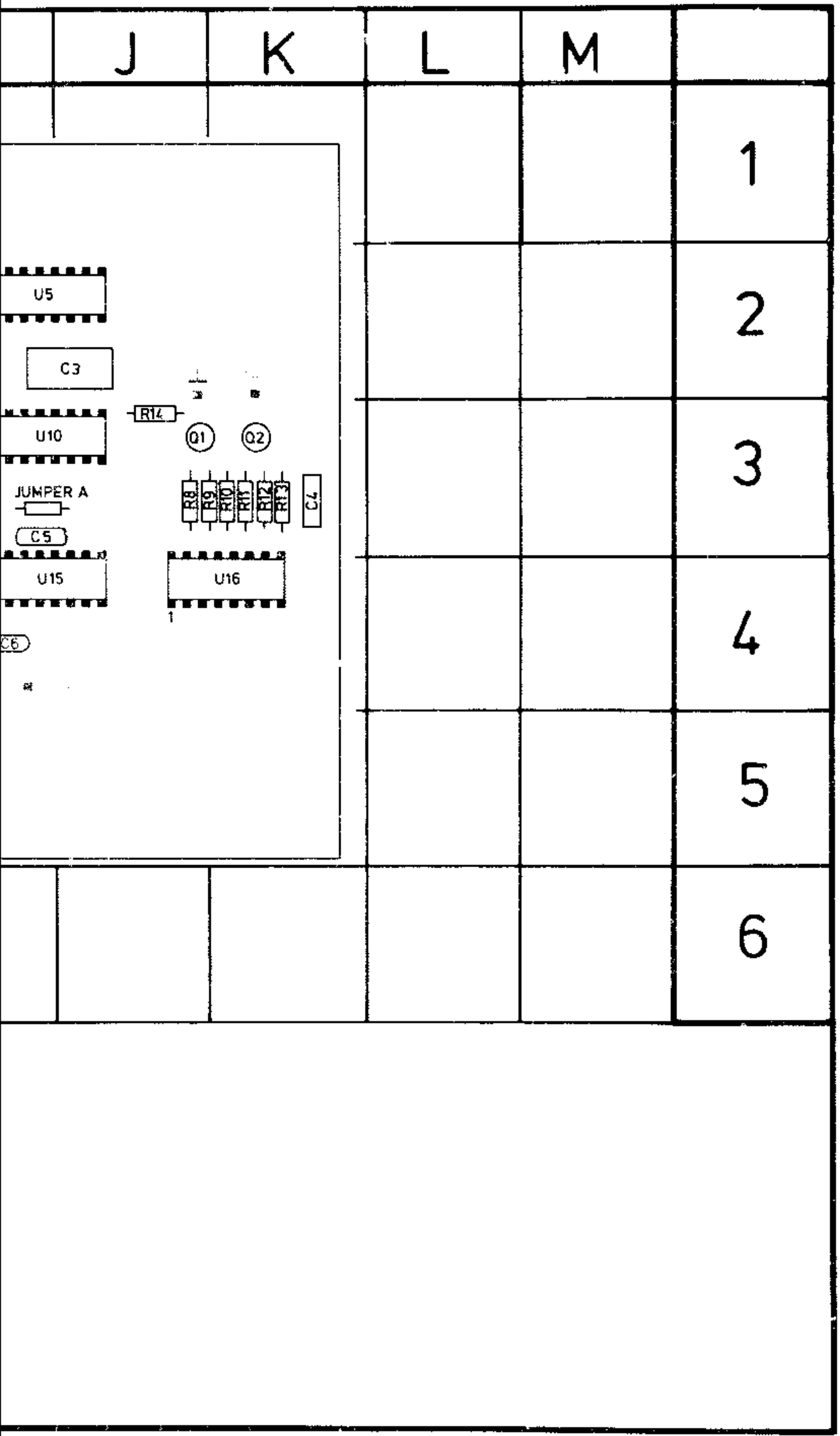


6

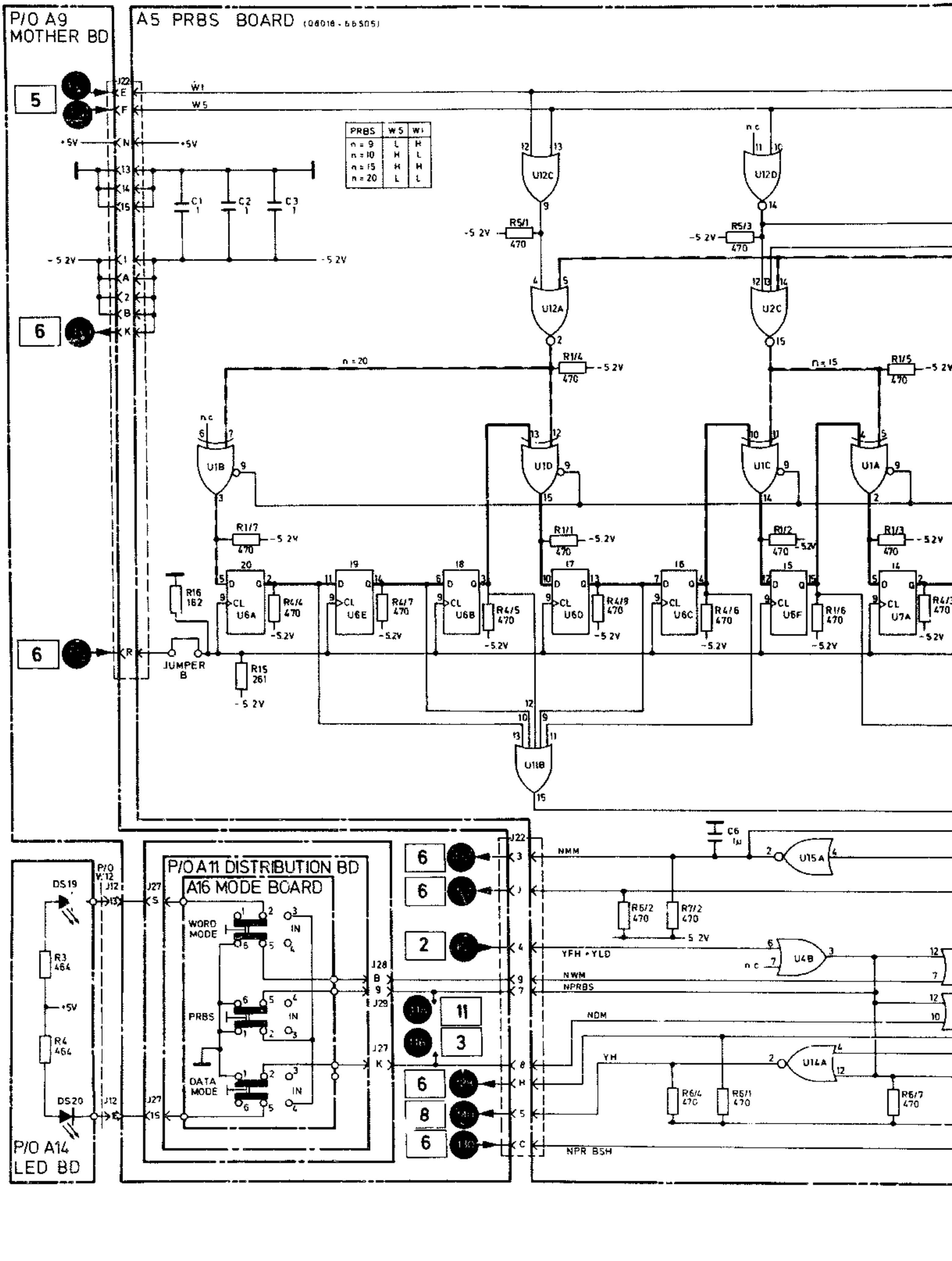
DATA FORMAT BOARD A4
P/O TRIGGER BOARD A15

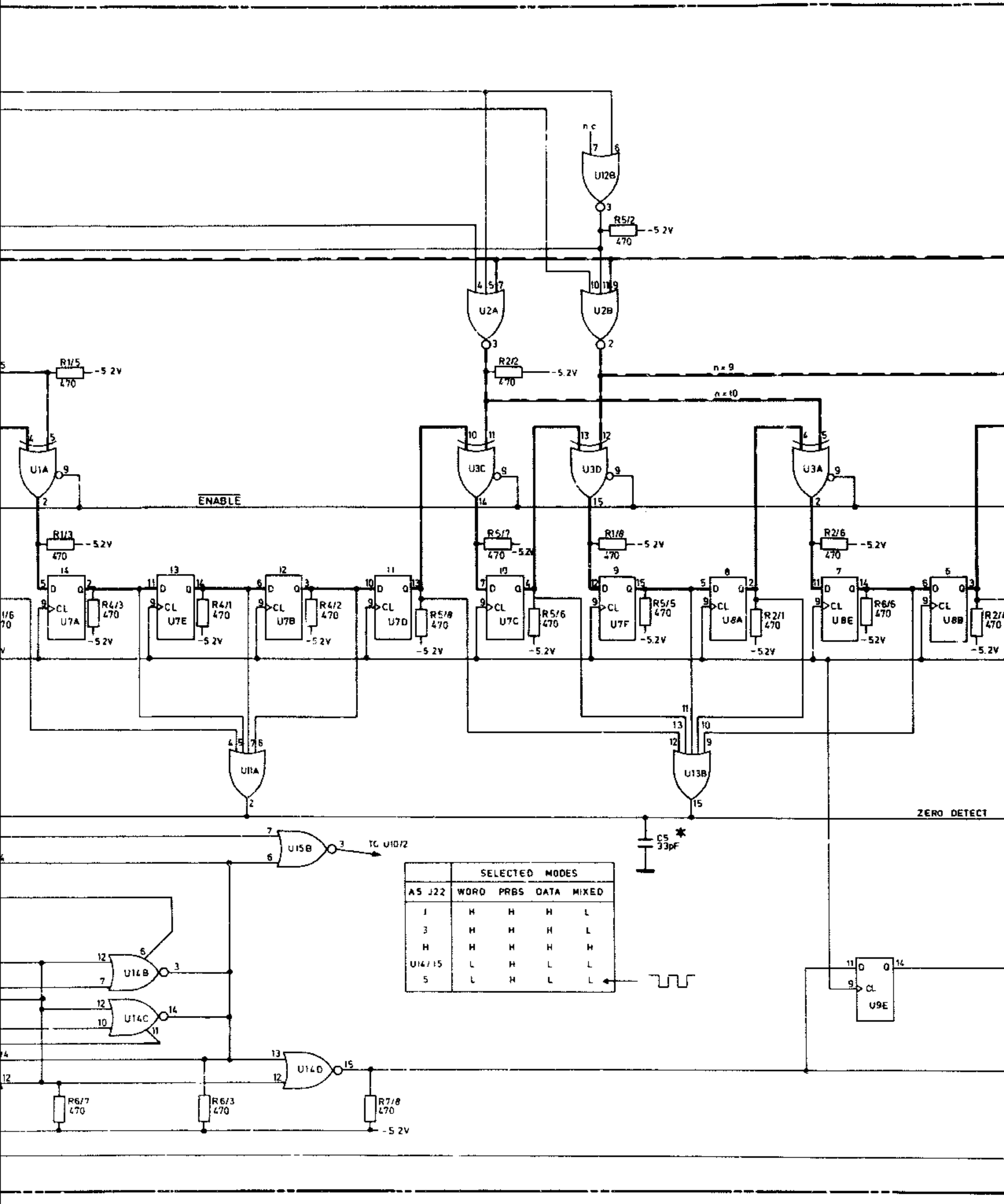

A
B
C
D
E
F
G
1
2
3
4
5
6
7
A5 PRBS BOARD (08080-66505)
U1
U2
U3
U6
U7
U8
U11
U12
U13
C1
C2
R1
R2
R4
R5
R6
J22
(A B C D E F H J K L M N P R S)


G
H
I
J
K
L
M
1
2
3
4
5
6
U3
U4
U5
C2
R2
R3
C3
R15
R16
R14
U8
U9
U10
Q1
Q2
JUMPER A
R8
R9
R10
R11
R12
R13
C4
C5
R6
R7
U13
U14
U15
U16
C6
JUMPER B



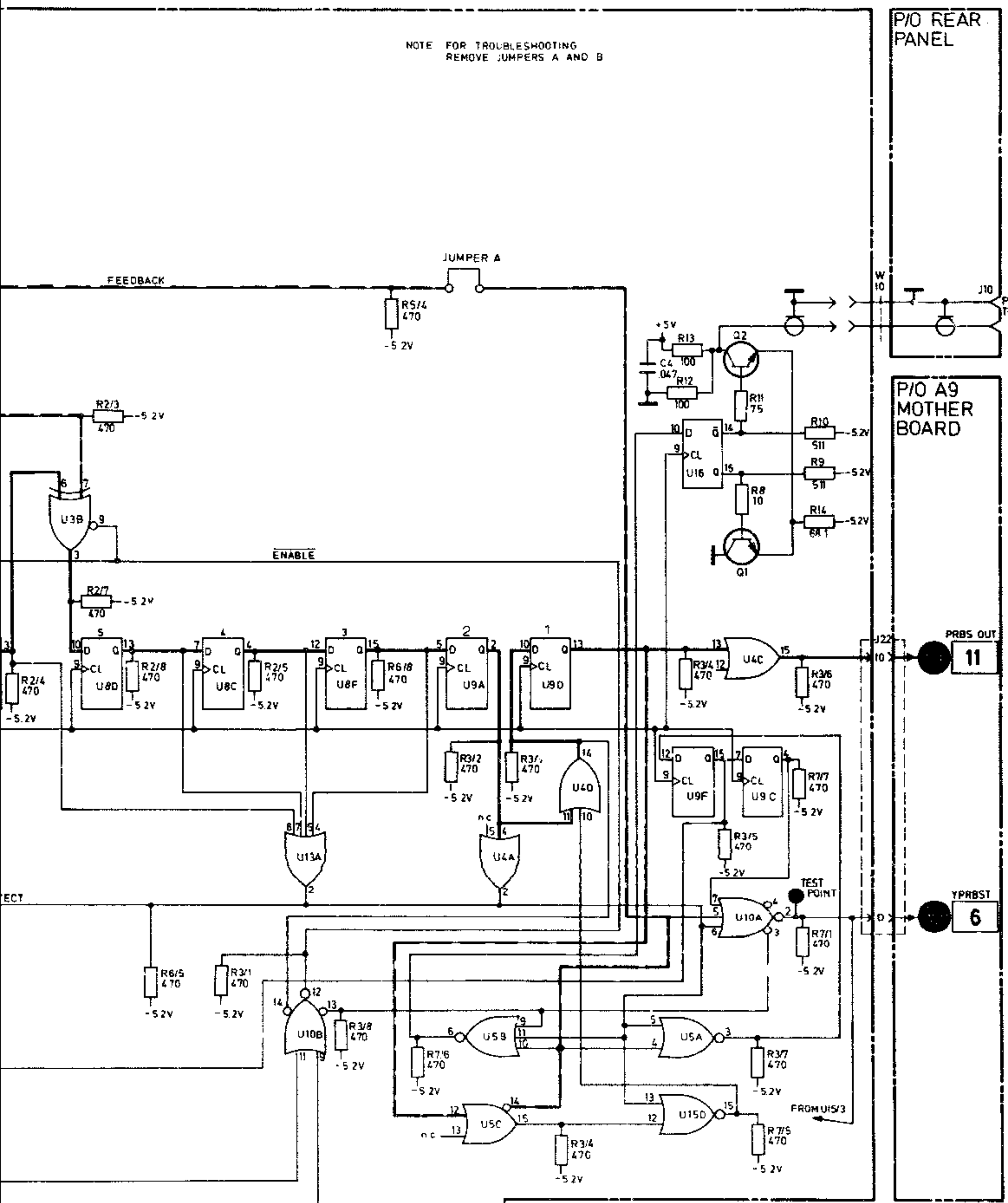
REF DESIG	GRID LOC
C1	E2
C2	G2
C3	I/J2
C4	K3
C5	I3
C6	I4
Q1	J3
Q2	K3
R1	F2/3
R2	G2/3
R3	I2/3
R4	E3/4
R5	F3/4
R6	G3/4
R7	I3/4
R8	J3
R9	K3
R10	K3
R11	K3
R12	K3
R13	K3
R14	J3
R15	H2
R16	H2
R7	I3/4
U1	D2
U2	E/F2
U3	G2
U4	H2
U5	I/J2
U6	D3
U7	E/F3
U8	G3
U9	H3
U10	I/J3
U11	D4
U12	E/F4
U13	G4
U14	H4
U15	I/J4
U16	J/K4


P/O A9
MOTHER BD
A5 PRBS BOARD (08018-66505)
PRBS | W5 | W1
n = 9 | L | H
n = 10 | H | L
n = 15 | H | H
n = 20 | L | L
JUMPER B
P/O A11 DISTRIBUTION BD
A16 MODE BOARD
WORD MODE
PRBS
DATA MODE
P/O A14
LED BD
NMM
YFH + YLD
NWM
NPRBS
NDM
YH
NPR BSH
U12C
U12D
U12A
U2C
U1B
U1D
U1C
U1A
U6A
U6E
U6B
U6D
U6C
U6F
U7A
U11B
U15A
U4B
U14A
DS19
DS20



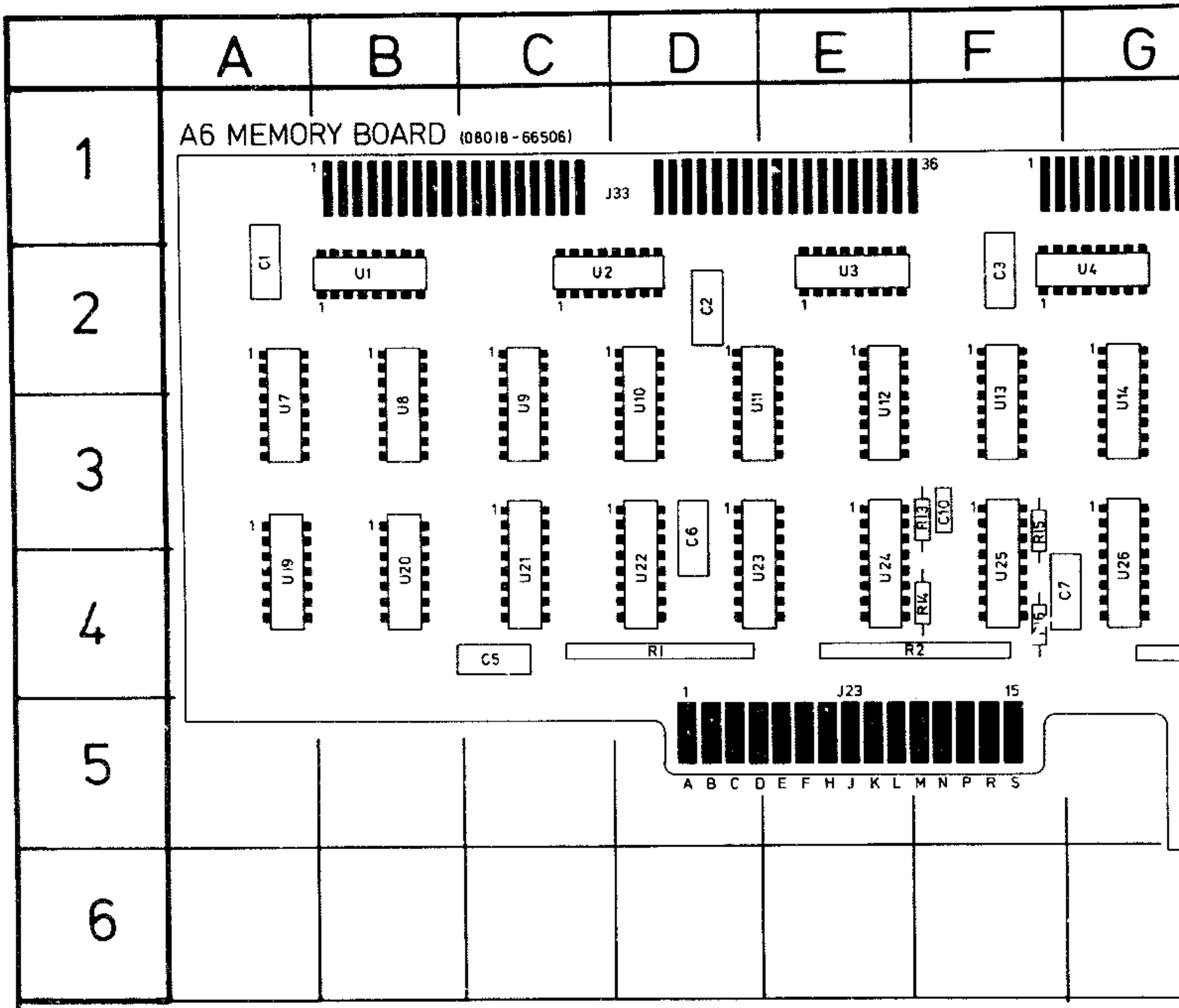
SELECTED MODES

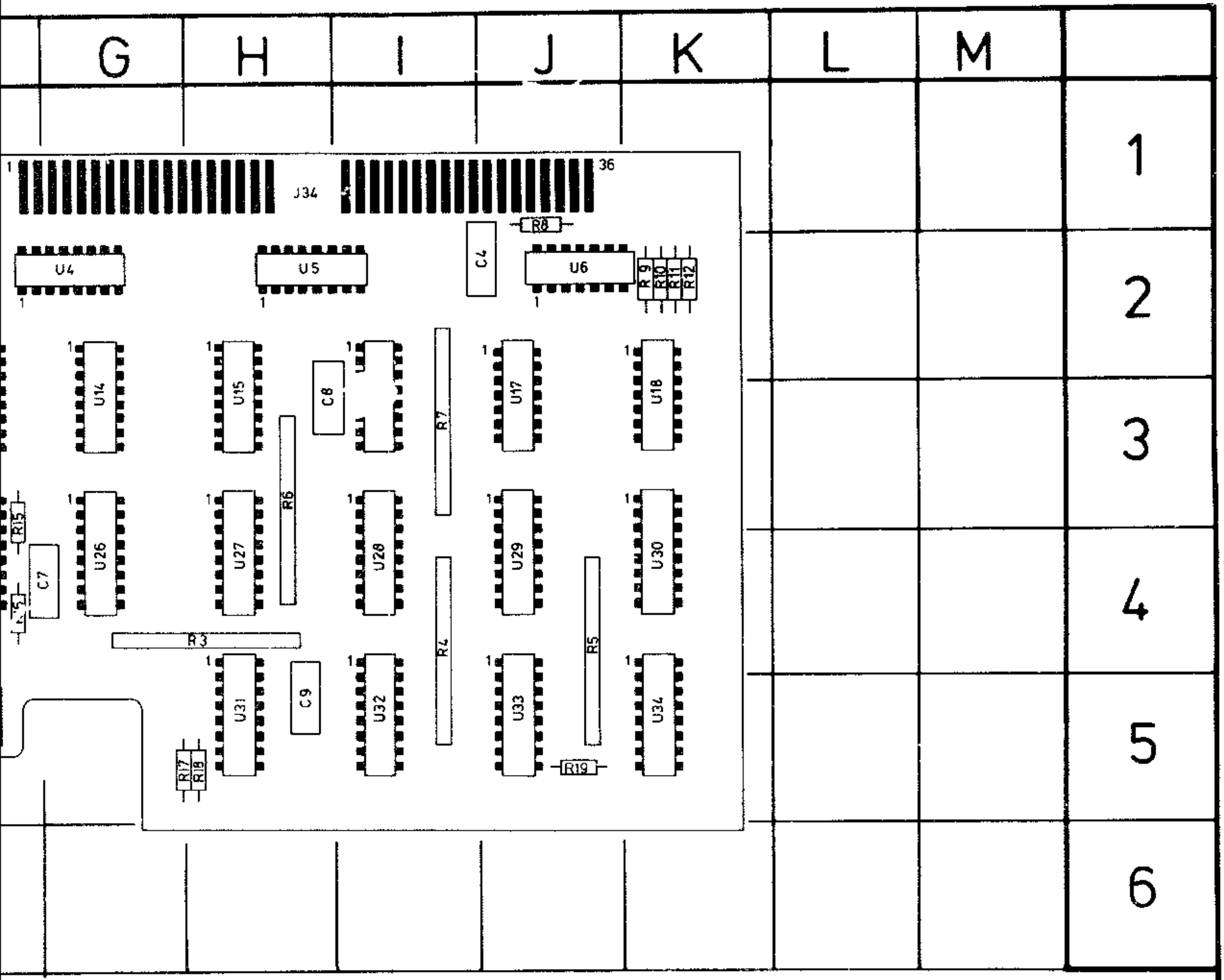
A5 J22	WORD	PRBS	DATA	MIXED
1	H	H	H	L
3	H	H	H	L
H	H	H	H	H
U14/15	L	H	L	L
5	L	H	L	L

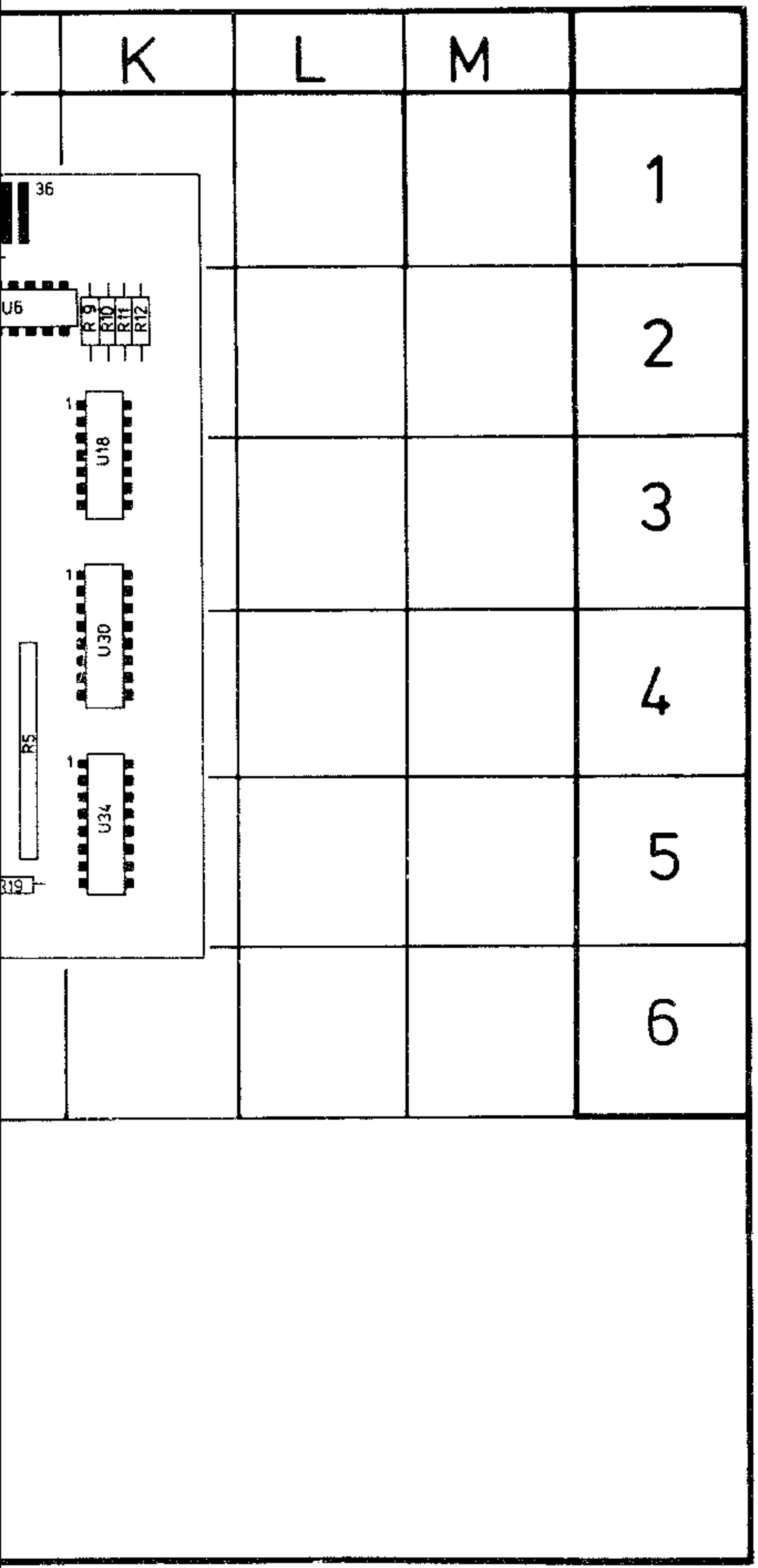


PRBS BOARD A5
P/O LED BOARD A14
MODE BOARD A16

7


A B C D E F G
1 2 3 4 5 6
A6 MEMORY BOARD (08018-66506)
J33
36
U1 U2 U3 U4
C1 C2 C3
U7 U8 U9 U10 U11 U12 U13 U14
U19 U20 U21 U22 U23 U24 U25 U26
C5 C6 C7 C10
R1 R2 R13 R14 R15
J23
15
A B C D E F H J K L M N P R S


G
H
I
J
K
L
M
1
2
3
4
5
6
J34
36
U4
U5
U6
C4
R8
R9
R10
R11
R12
U14
U15
C8
R7
U17
U18
R6
R15
C7
U26
U27
U28
U29
U30
R3
R4
R5
U31
C9
U32
U33
U34
R17
R18
R19



REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	A1/2	U28	I3/4
C2	D2	U29	J3/4
C3	F2	U30	K3/4
C4	I/J1/2	U31	H4/5
C5	B/C4	U32	I4/5
C6	D3/4	U33	J4/5
C7	F/G4	U34	K4/5
C8	H2/3		
C9	H4/5		
C10	F3		
R1	C/D4		
R2	E/F4		
R3	G/H4		
R4	I4/5		
R5	J4/5		
R6	H3/4		
R7	I2/3		
R8	J1		
R9	K2		
R10	K2		
R11	K2		
R12	K2		
R13	E/F3		
R14	E/F4		
R15	F3/4		
R16	F4		
R17	G5		
R18	H5		
R19	J5		
U1	B2		
U2	C/D2		
U3	E2		
U4	F/G2		
U5	H/I2		
U6	J2		
U7	A2/3		
U8	B2/3		
U9	C2/3		
U10	D2/3		
U11	D2/3		
U12	E2/3		
U13	F2/3		
U14	G2/3		
U15	H2/3		
U16	I2/3		
U17	J2/3		
U18	K2/3		
U19	A3/4		
U20	B3/4		
U21	C3/4		
U22	D3/4		
U23	D3/4		
U24	E3/4		
U25	F3/4		
U26	G3/4		
U27	H3/4		

SERVICE BLOCK 5
MEMORY BOARDS A6, A12 8 9 10

THEORY OF OPERATION

General

To read data out of the 8018A memory up to 50 MHz, a minimum access time of 20 nano seconds is required for the entire RAM's. As the access time for RAM's A6U4 to U1 and A12U4 to U1 is 80 nano seconds, the addresses are multiplexed by four to allow the data to settle within the specified time.

The first four bits of one cycle are stored in flip-flops A6U17 A/B, A6U18 A/B for the channel A memory and in A12U10 A/B, A12U9 A/B for the channel B memory.

This allows the RAM data to settle when reading the first four data bits out of the flip-flops, and avoids a time gap when switching from the last data bit to the first data bit.

The following description covers the channel A memory (A6) circuit and the additional circuits used for the A12 channel B memory. To aid this description, a block diagram of the 8018A memory and its associated logic circuits is given in Figure 8–5–1.

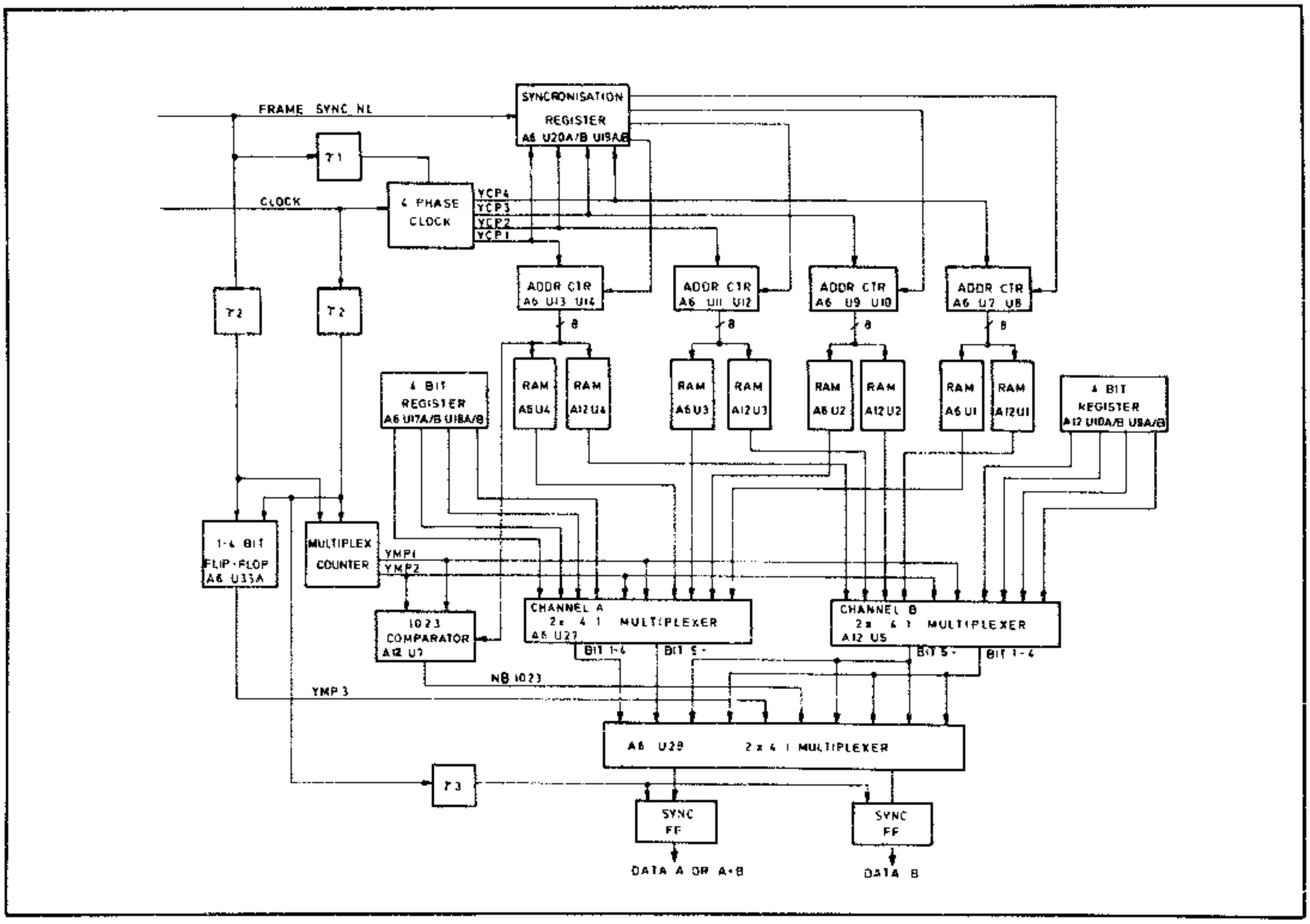


Figure 8–5–1. Memory Block Diagram

Multiphase Clock Generation (Schematic 8)

Figure 8–5–2 shows the logic elements involved in the multiphase clock generation together with a timing diagram showing the clocks and their sync signals.

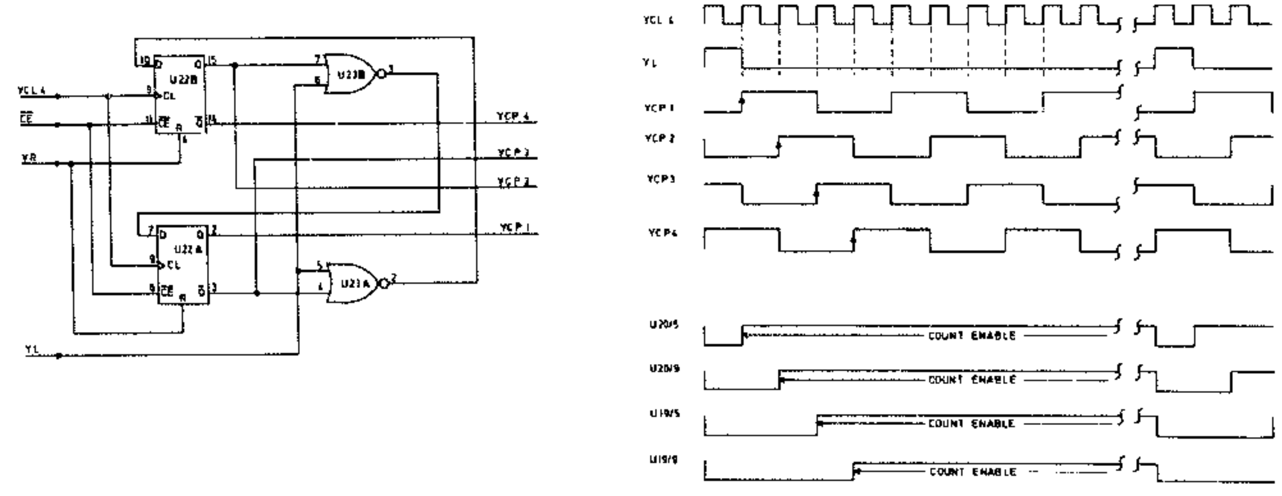


Figure 8–5–2. Multiphase Clock Generation

As can be seen from Figure 8–5–2, U22 A/B and U23 A/B form a ring counter which generates the four clock phases YCP1, YCP2, YCP3 and YCP4 for the RAM address counters A6U14 to U7.

Sync Circuit U20 A/B U19 A/B (Schematic 9)

Signal YL (Last bit) is inverted by the ECL/TTL translator U26 and clears U20 A/B and U19 A/B. This sets the address counters U7 to U14 to the load position.

YCP 1 then clocks U13/U14, presetting (loading) U13 to one and U14 to zero, at the same time removing the load signal (low) from U13/U14 via U20A. Similarly, YCP2, YCP3 and YCP4 preset and enable counters U11/U12, U9/U10 and U7/U8 respectively.

NOTE: Because the first four bits are stored in flip-flops (and not in the RAMs), the RAM address counters start at count 1.
Simultaneous to the address counters being preset to 1, the first four data bits are read out of flip-flops U17 A/B and U18 A/B. As a result, the fifth data bit stored in RAM U4 has had time to settle, and is now routed to the output. During the following U3 readout, the next address is set for U4. This cycle is then repeated for U2/U3 and U1/U2.

NOTE: The counter outputs QA, QB, QC and QD are not connected in numerical order to RAM address inputs A0 to A3 (e.g. when counter outputs indicate 1, the RAM address 2 is selected).

Multiplex Counter (Schematic 8)

Figure 8–5–3 shows the logic elements involved in the multiplex signal generation, together with a timing diagram showing the signal timing relationships.

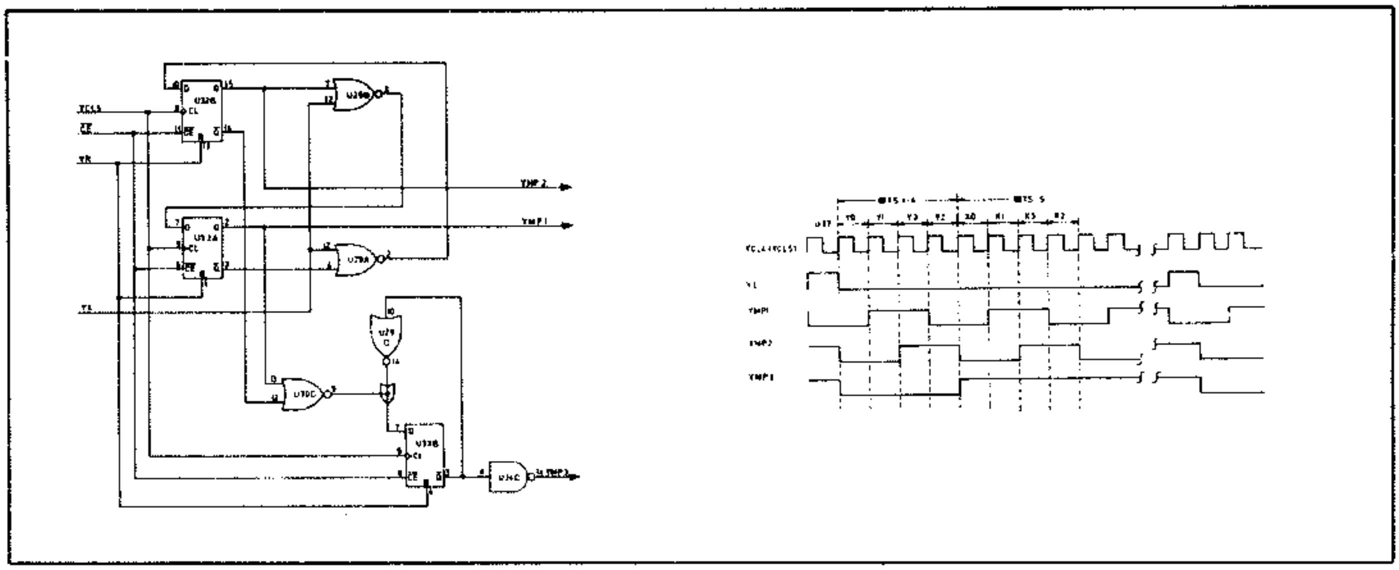


Figure 8–5–3. Multiplex Counter

As can be seen from Figure 8–5–3, U29 A/B and U32 A/B form a similar ring counter to that used in the multiphase clock generation. In this case, only signals YMP1 and YMP2 are used to select the outputs of RAMs U1 to U4.

YMP1 and NMP2 (U32B $\overline{Q}$-output) are used to hold U33B $\overline{Q}$-output high for 3 clock cycles. After the fourth clock, U30C pin 9 goes high and the fifth clock sets U33B $\overline{Q}$-output low. This low is inverted by U29C and U34C – via U29C so that U33B $\overline{Q}$-output is held low until U33B is reset, and via U34C to generate signal YMP3.

Data Multiplexer (Schematic 9)

Signals YMP1 and YMP2 are applied to the A/B select inputs of multiplexer A6U27 (A12U5) and determine which one of four active data inputs is valid for each multiplexer. Signal YMP3 is routed to U28, and for as long as it is in a low state, the XO and YO inputs are selected. During this 'low' time, only bits 1–4 are switched to the W- and Z-outputs. When YMP3 is high, inputs X1 and Y1 are selected which are the inputs for data derived from the RAM's.

When data has to be loaded, signal YWER (Write Enable RAM) becomes true (high). As long as YMP3 is low, multiplexer U5A is enabled via U6 A/B and the first four data bits from the control board can be clocked into flip-flops U17 A/B and U18 A/B. When YMP3 goes high, U5B is enabled via U6C. RAM's U1 to U4 are then selected via signals YMP1/YMP2 by switching one of the U5B multiplexer outputs to low.

Memory Extension A12 (Schematic 10)

The Memory Extension Board A12 has a similar structure to that for the memroy on the A6 board. The first four bits are stored in flip-flops U10A/B and U9A/B. Bits 5 and onwards are stored in RAM's U1, U2, U3 and U4. The data is multiplexed by U5 via select signal YMP1 and YMP2.

Memory Serialization (Schematic 10)

Figure 8–5–4 provides a timing diagram of the memory readout during serialization.

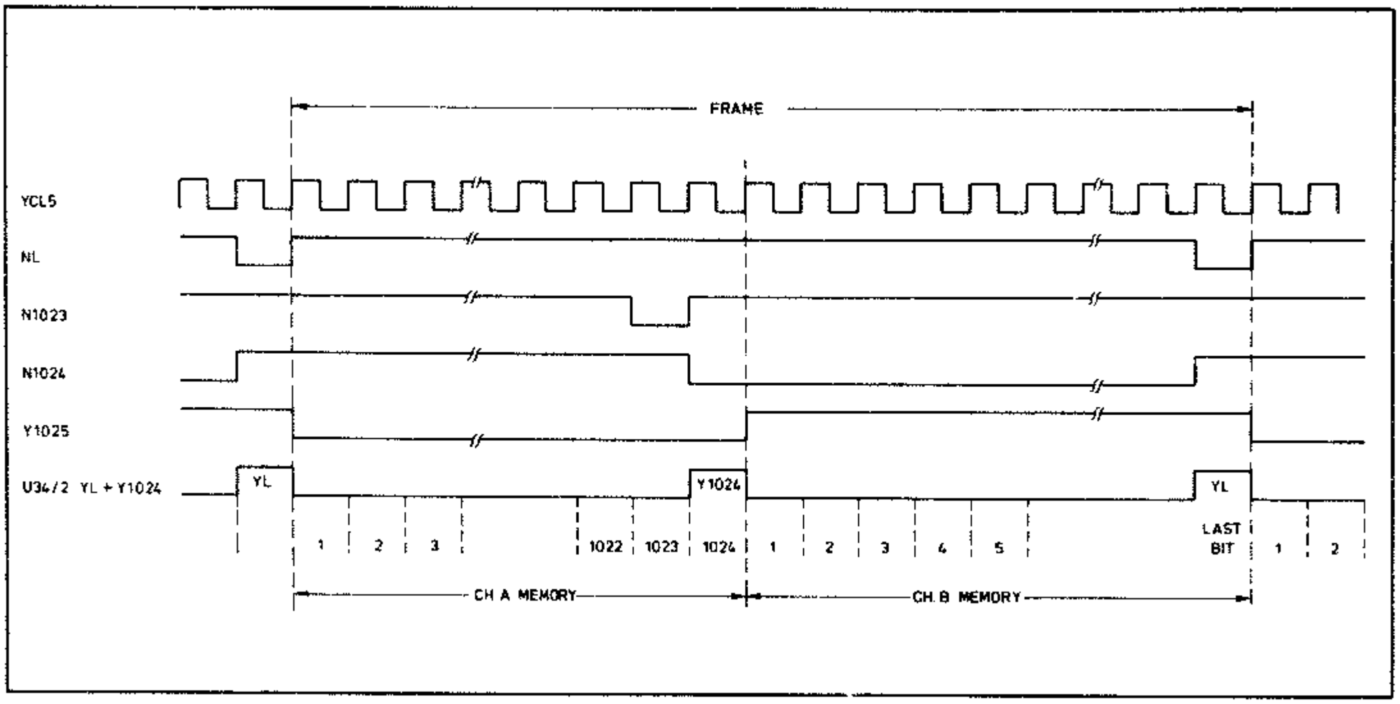


Figure 8–5–4. Timing Diagram for Memory Serialization

When the 1 x 2048 button is pressed, A12U7/5 is set to high via U11D (NSER). This enables A12U7 to detect the end of the channel A memory readout (address 254 of the last RAM). When 1023 bits are detected, signal N 1023 is generated and fed to the K-input of U17B. After the next clock, the $\overline{Q}$ output of U17B goes low (N 1024). As the $\overline{Q}$ output of U17A is still low, U13 switches to high and sets the multiphase and multiplex counter in start position for the second part of the frame. After the frame is completed, start conditions are established by YL again.

TROUBLESHOOTING

Memory Organization

Table 8–5–1 provides an overview of how the 8018A memory is organized.

Table 8–5–1. Memory Organization

bit	FLIP-FLOP
1	U17A (U10A)
2	U17B (U10B)
3	U18A (U9A)
4	U18B (U9B)

bit				RAM A6 (A12)	
5	9	13	17 ... 1021	U4 (U4)	x mod 4 = 1
6	10	14	18 ... 1022	U3 (U3)	x mod 4 = 2
7	11	15	19 ... 1023	U2 (U2)	x mod 4 = 3
8	12	16	20 ... 1024	U1 (U1)	x mod 4 = 0

If a bit fails anywhere within the entire memory, the defective RAM can be easily located by using Table 8–5–1 and the following formula:

X mod 4 = Y   where X is the number of the faulty bit

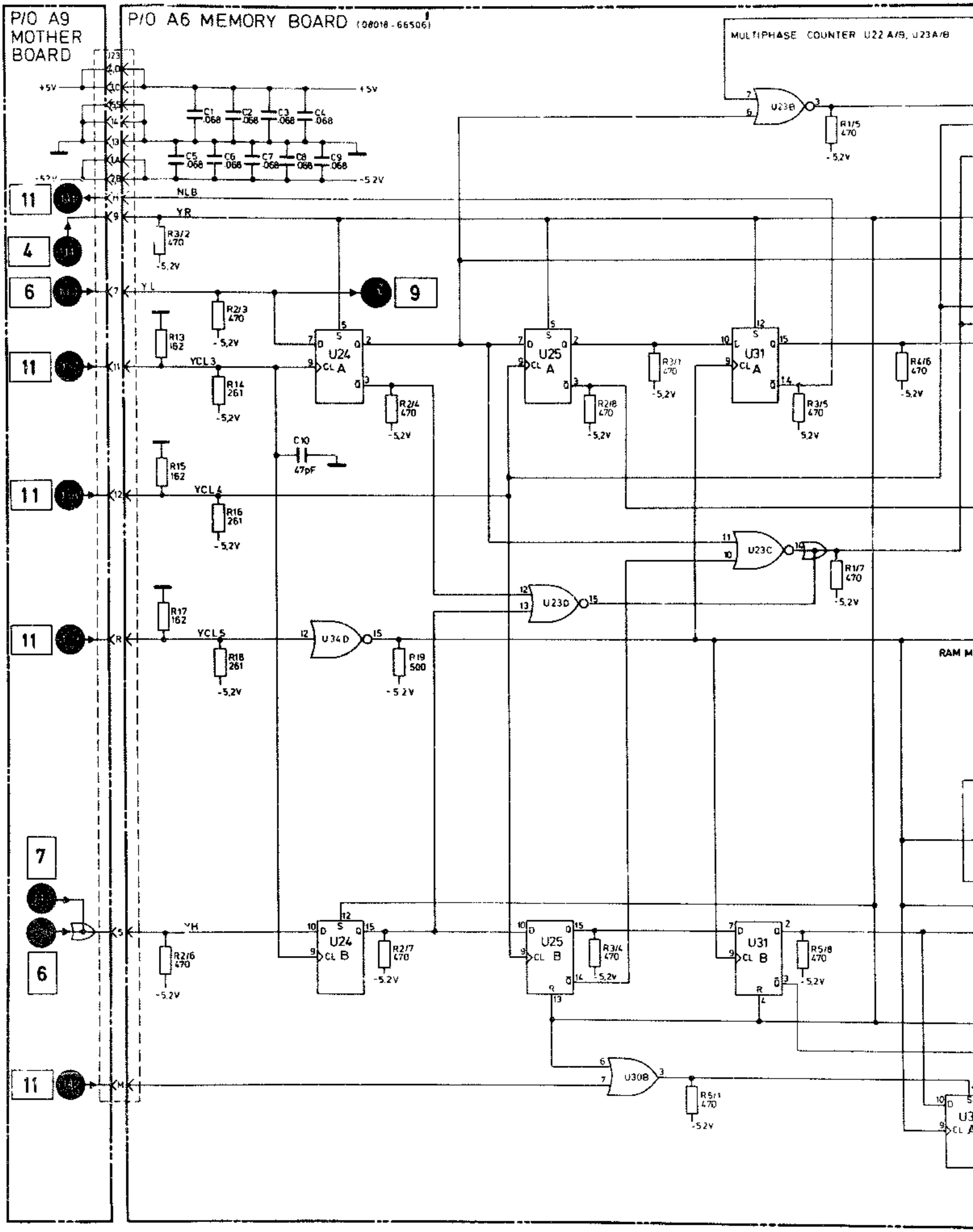
If Y = 1, the fault is in A6U4 (A12U4 for Channel B memory.
If Y = 2, the fault is in A6U3 (A12U3 for Channel B memory).

NOTE: Modulus (mod) 4 in the above equation is similar to a normal division by 4, but instead of taking the complete multiples of 4 as a result, mod takes the remainder and returns it as a result. e.g. 13 mod 4 = 1; 13 : 4 = 3 remainder 1.

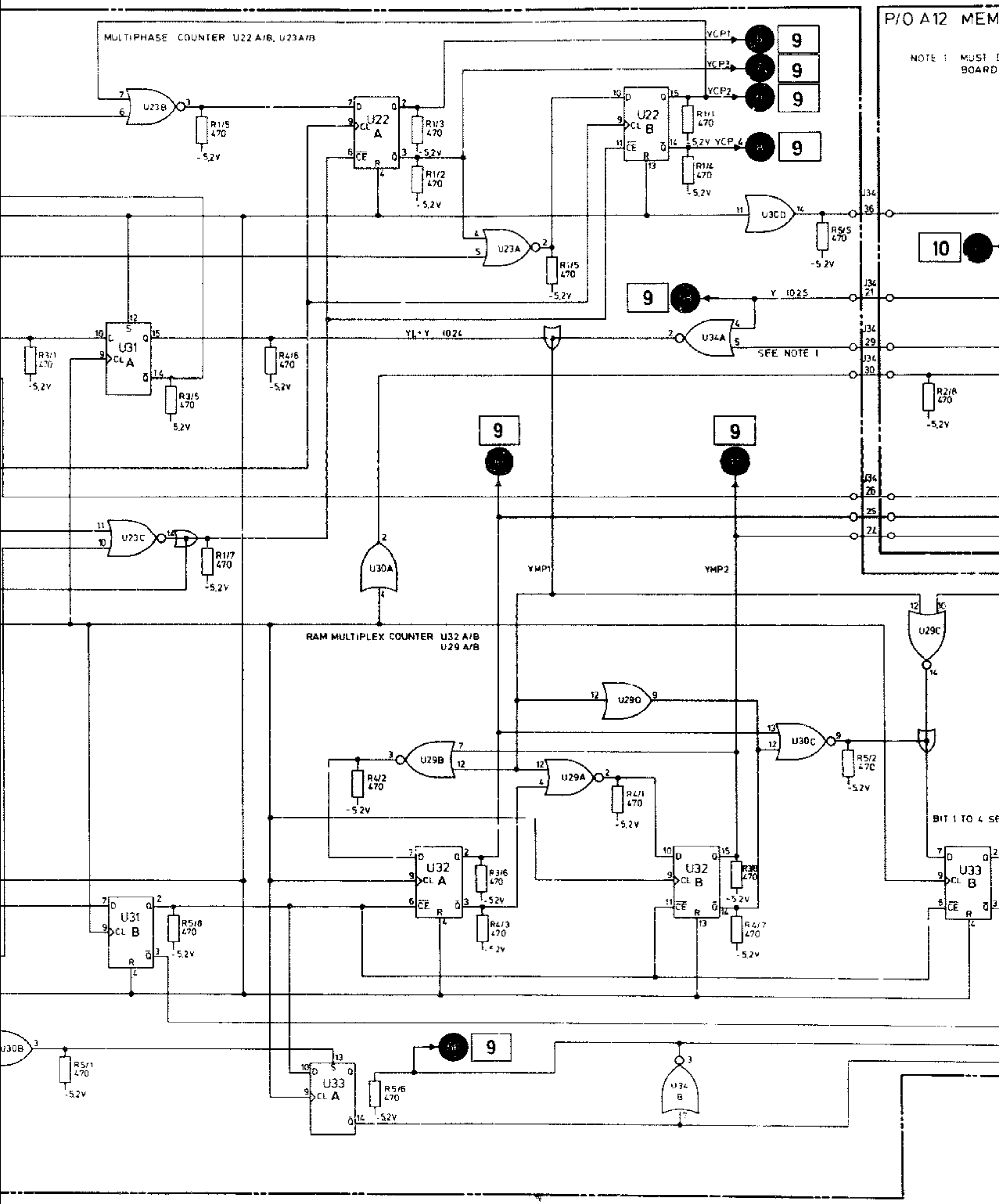
Memory Splitting

To ensure that the Channel A memory (A6) is not influenced or distorted by the Channel B memory (A12), A12 can be removed from the A6 board. Without A12, **A6U24 pin 5 must be connected to ground** (high) to enable the Multiphase and Multiplex Counters.

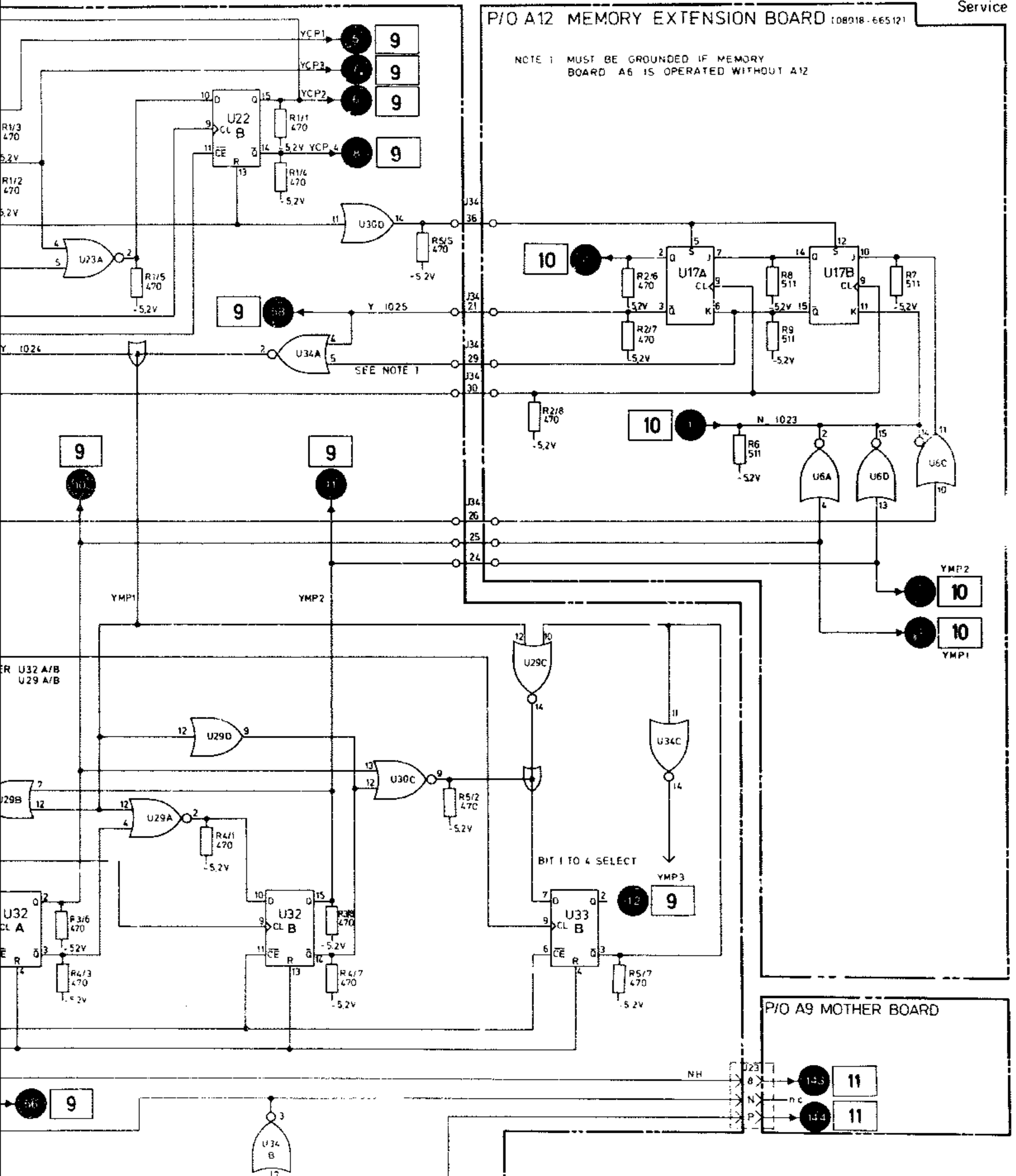
NOTE: For troubleshooting trigger oscilloscope to YL.



P/O A9 MOTHER BOARD
P/O A6 MEMORY BOARD (08018-66506)
MULTIPHASE COUNTER U22 A/B, U23A/B
U23B
U24 A
U25 A
U31 A
U23C
U23D
U34D
U24 B
U25 B
U31 B
U30B
RAM M
NLB
YR
YL
YCL 3
YCL 4
YCL 5
YH
C10 47pF
R13 162
R14 261
R15 162
R16 261
R17 162
R18 261
R19 500
+5V
-5.2V

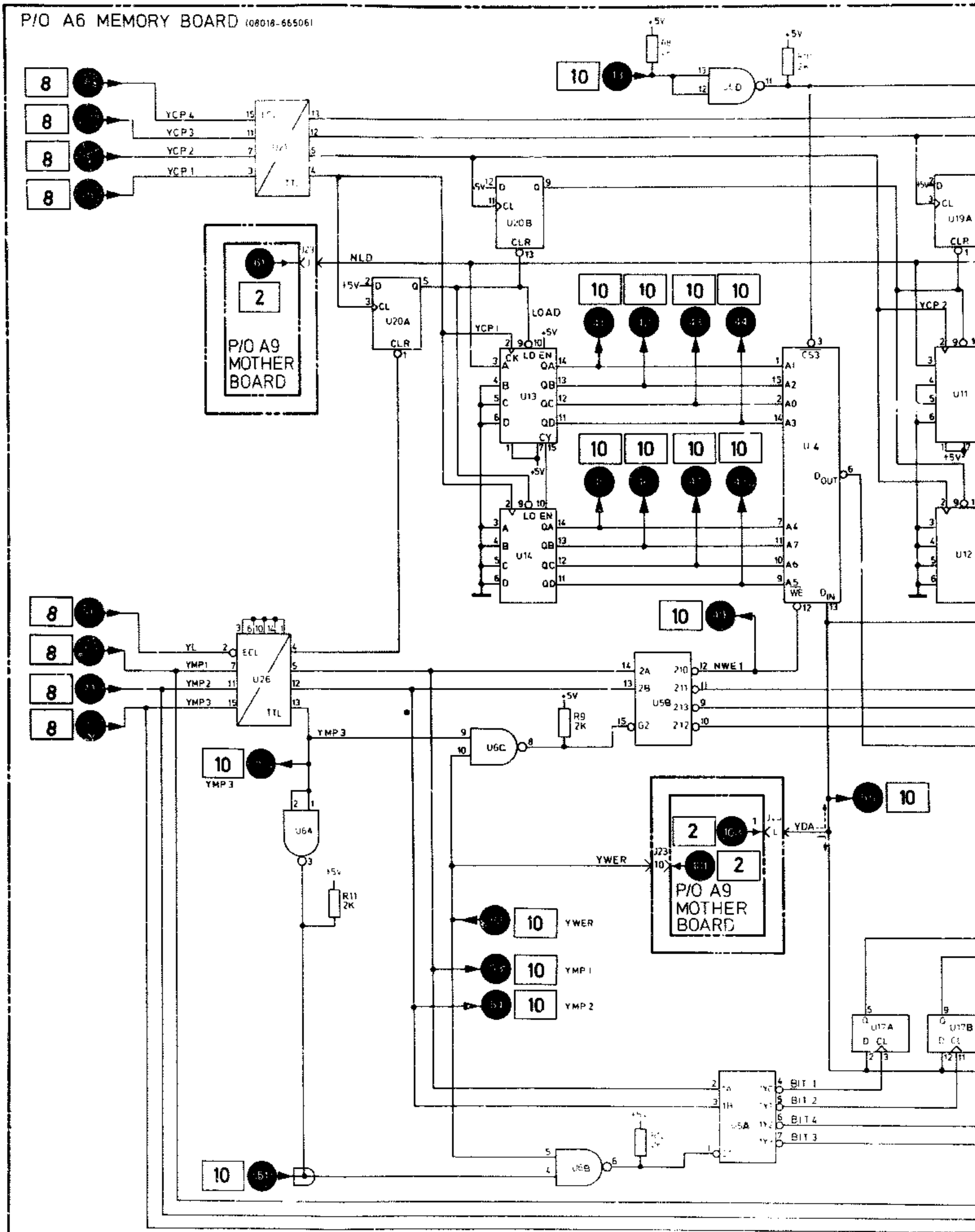


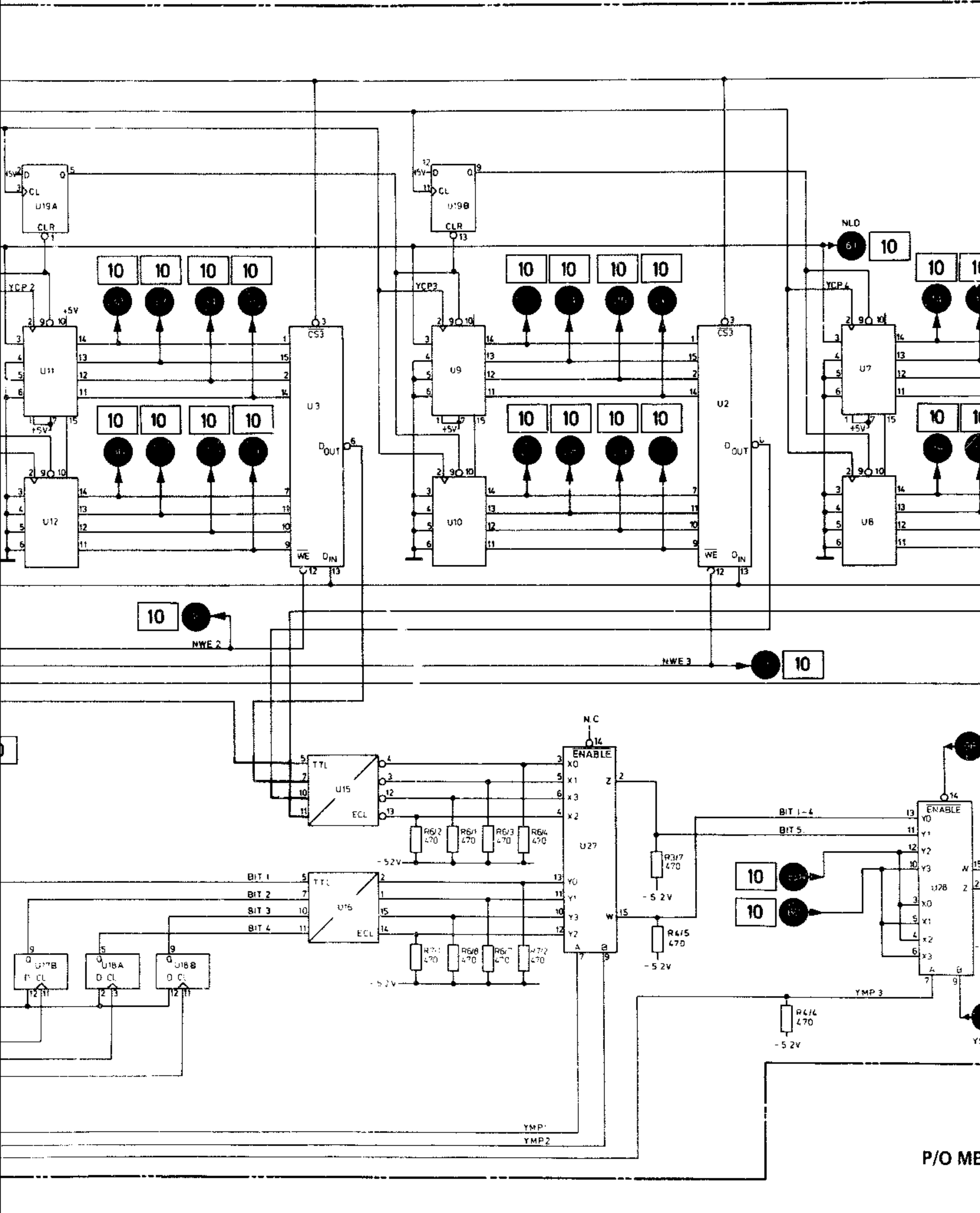
P/O A12 MEM
NOTE 1 MUST
BOARD
MULTIPHASE COUNTER U22 A/B, U23A/B
RAM MULTIPLEX COUNTER U32 A/B
U29 A/B
YCP1
YCP2
YCP2
YCP 4
Y 1025
YL+Y 1024
SEE NOTE 1
YMP1
YMP2
BIT 1 TO 4 SE
U22 A
U22 B
U23B
U23A
U23C
U30D
U30A
U30C
U30B
U31 A
U31 B
U32 A
U32 B
U33 A
U33 B
U34A
U34 B
U29B
U29A
U29D
U29C
9
10

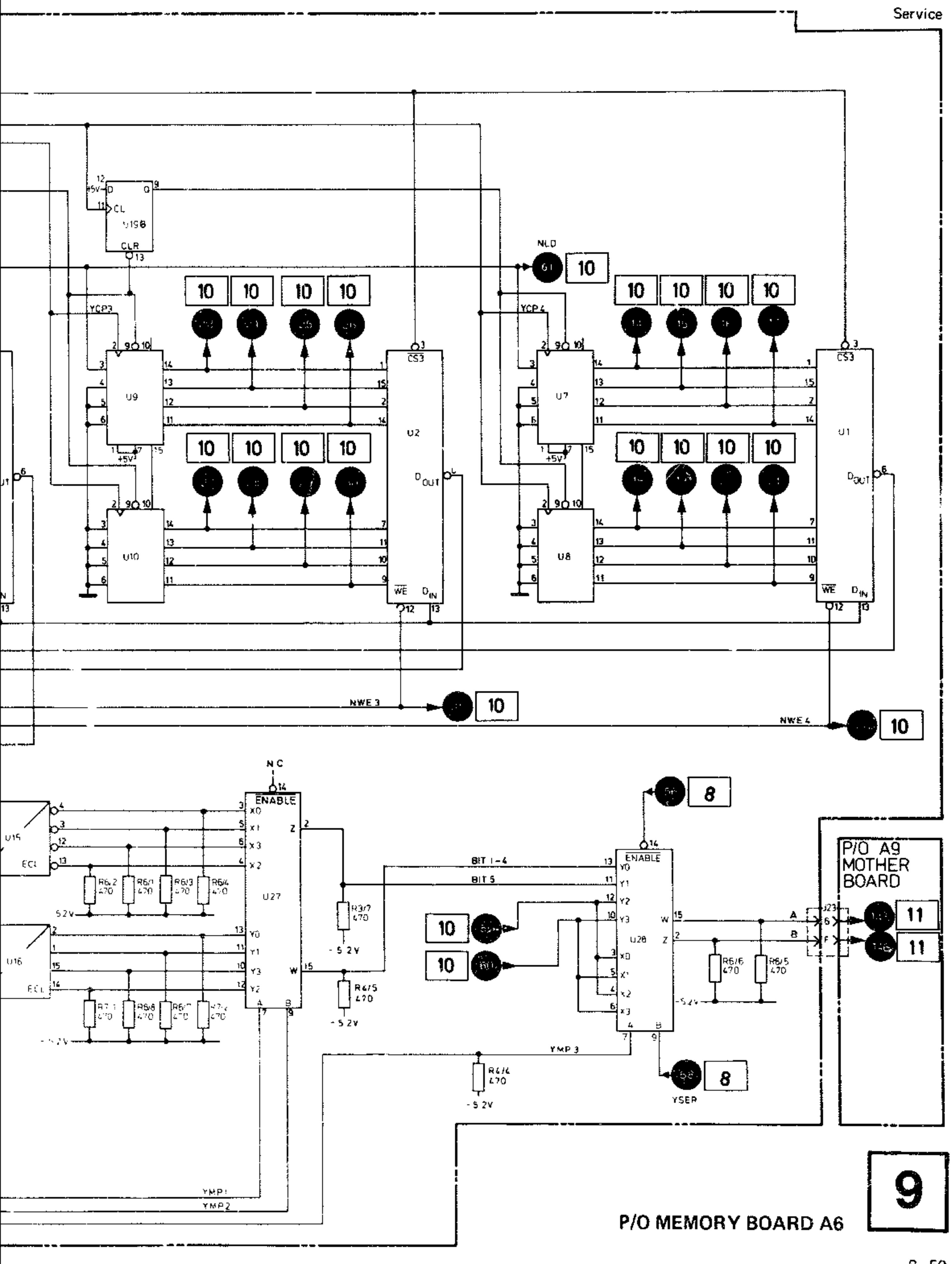


P/O MEMORY BOARD A6
P/O MEMORY EXTENSION BOARD A12

8

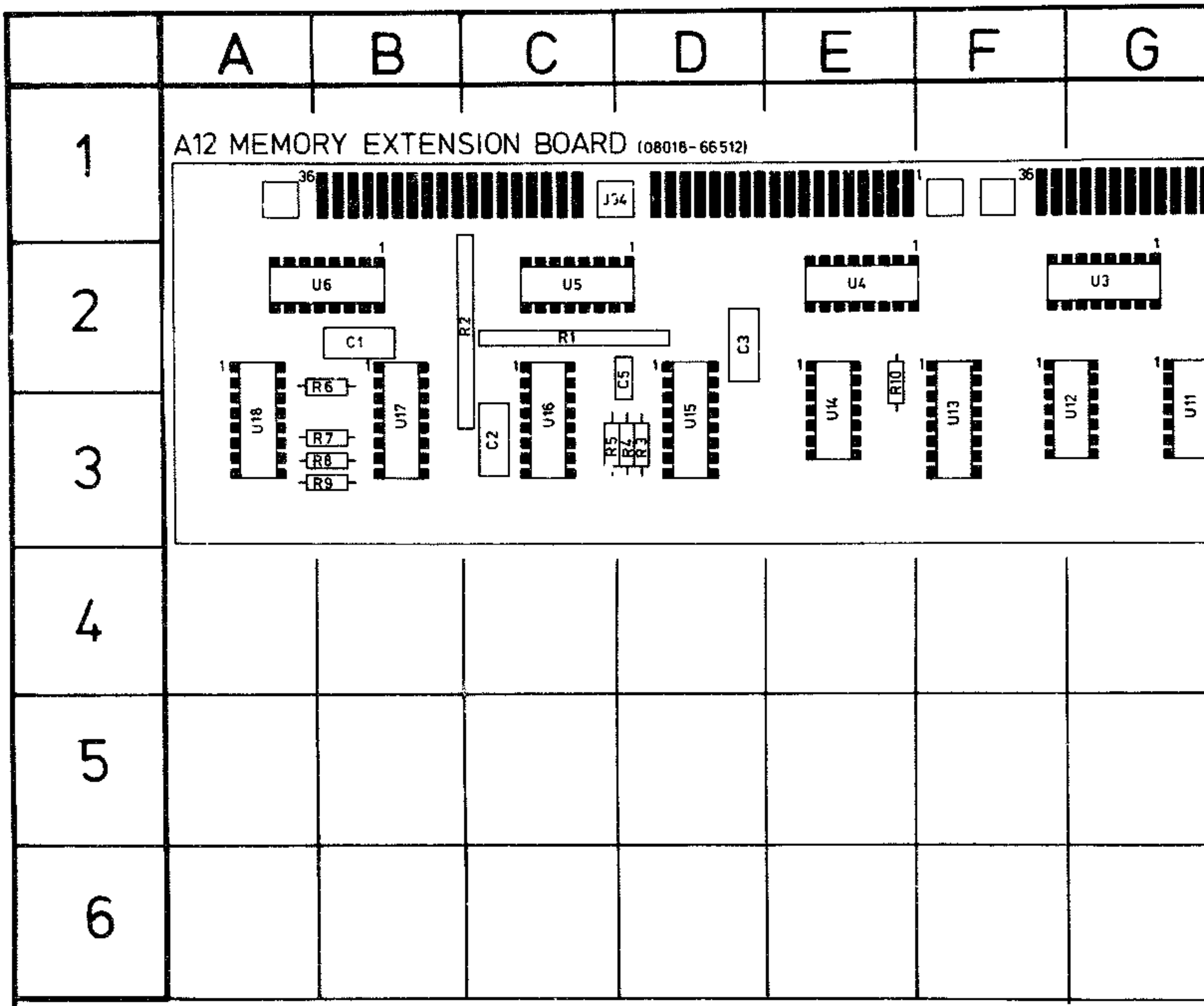

P/O A6 MEMORY BOARD (08018-66506)
P/O A9 MOTHER BOARD
P/O A9 MOTHER BOARD
YCP 4
YCP 3
YCP 2
YCP 1
NLD
LOAD
YCP 1
U20B
U20A
U13
U14
U4
U19A
U11
U12
YL
YMP1
YMP2
YMP3
U26
U5B
NWE 1
U6C
R9 2K
U64
R11 2K
YMP 3
YWER
YDA
YWER
YMP 1
YMP 2
U6B
U5A
BIT 1
BIT 2
BIT 4
BIT 3
U17A
U17B


U19A
U19B
U11
U12
U3
U9
U10
U2
U7
U8
U15
U16
U27
U28
U17B
U18A
U18B
NLD
YCP 2
YCP3
YCP 4
NWE 2
NWE 3
N.C
ENABLE
BIT 1
BIT 2
BIT 3
BIT 4
BIT 1 - 4
BIT 5
YMP 1
YMP 2
YMP 3
-5.2V
+5V
R3/7 470
R4/5 470
R4/4 470
R6/1 470
R6/2 470
R6/3 470
R6/4 470
R6/6 470
R6/8 470
R7/2 470
TTL
ECL
P/O ME

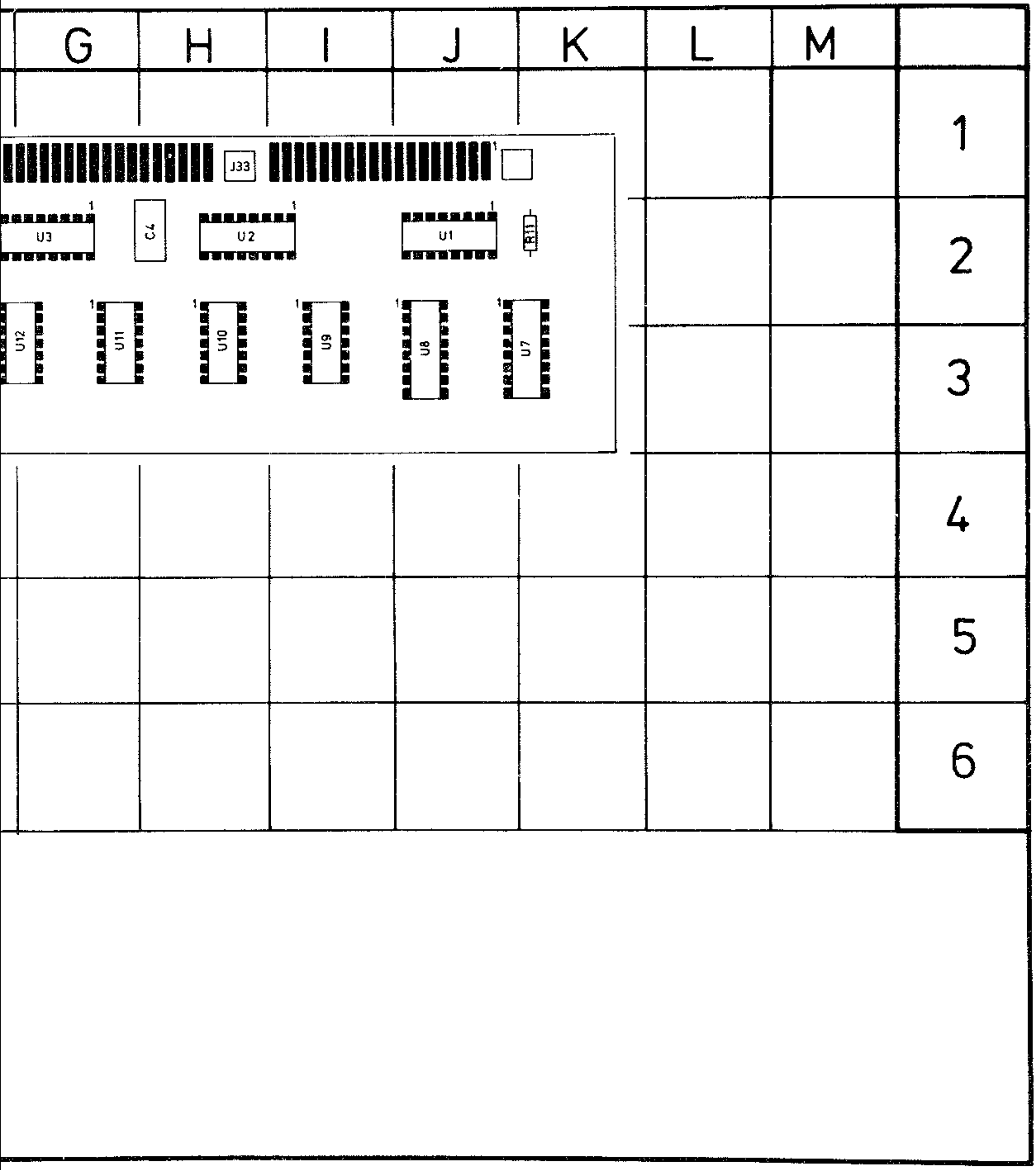


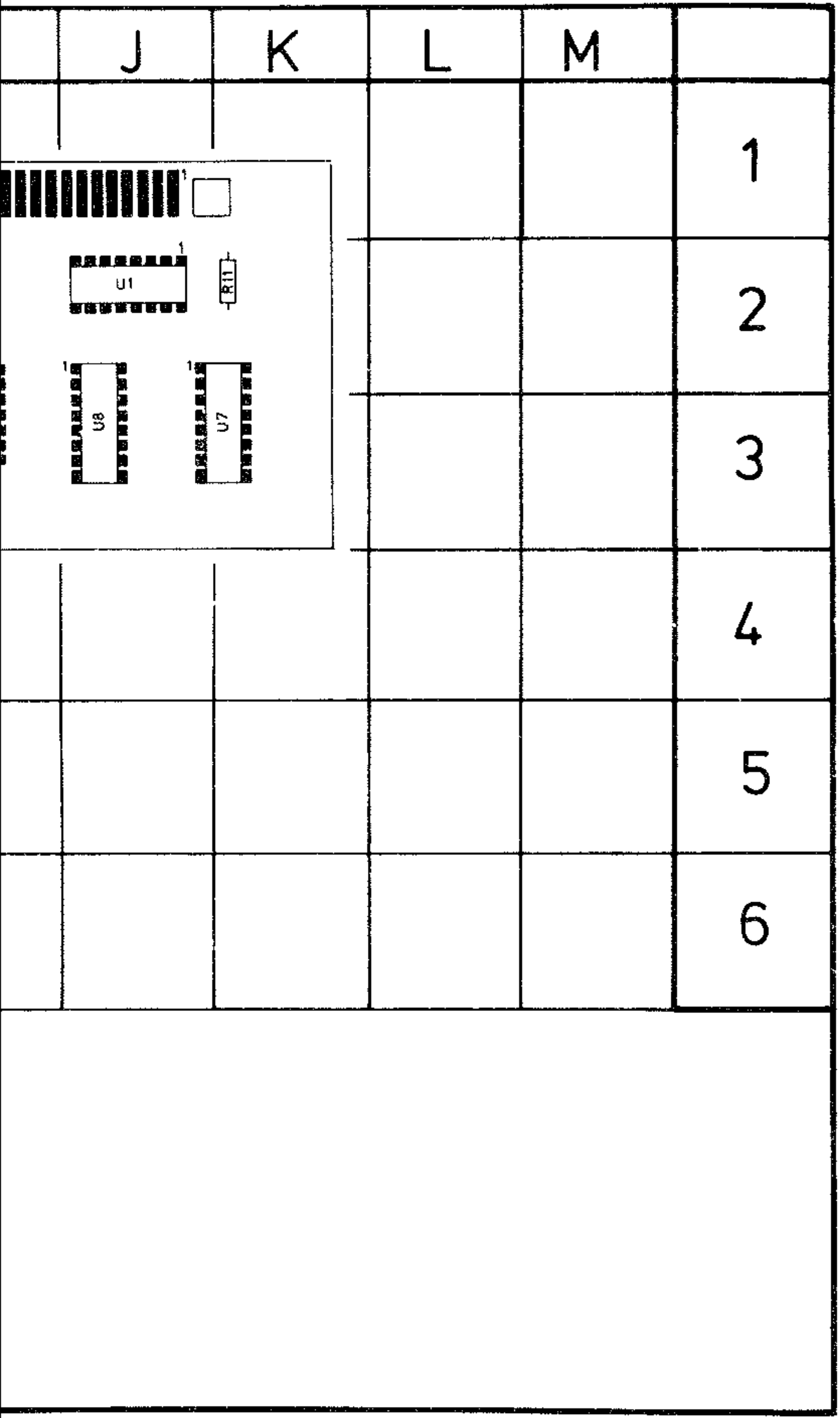
P/O MEMORY BOARD A6

9

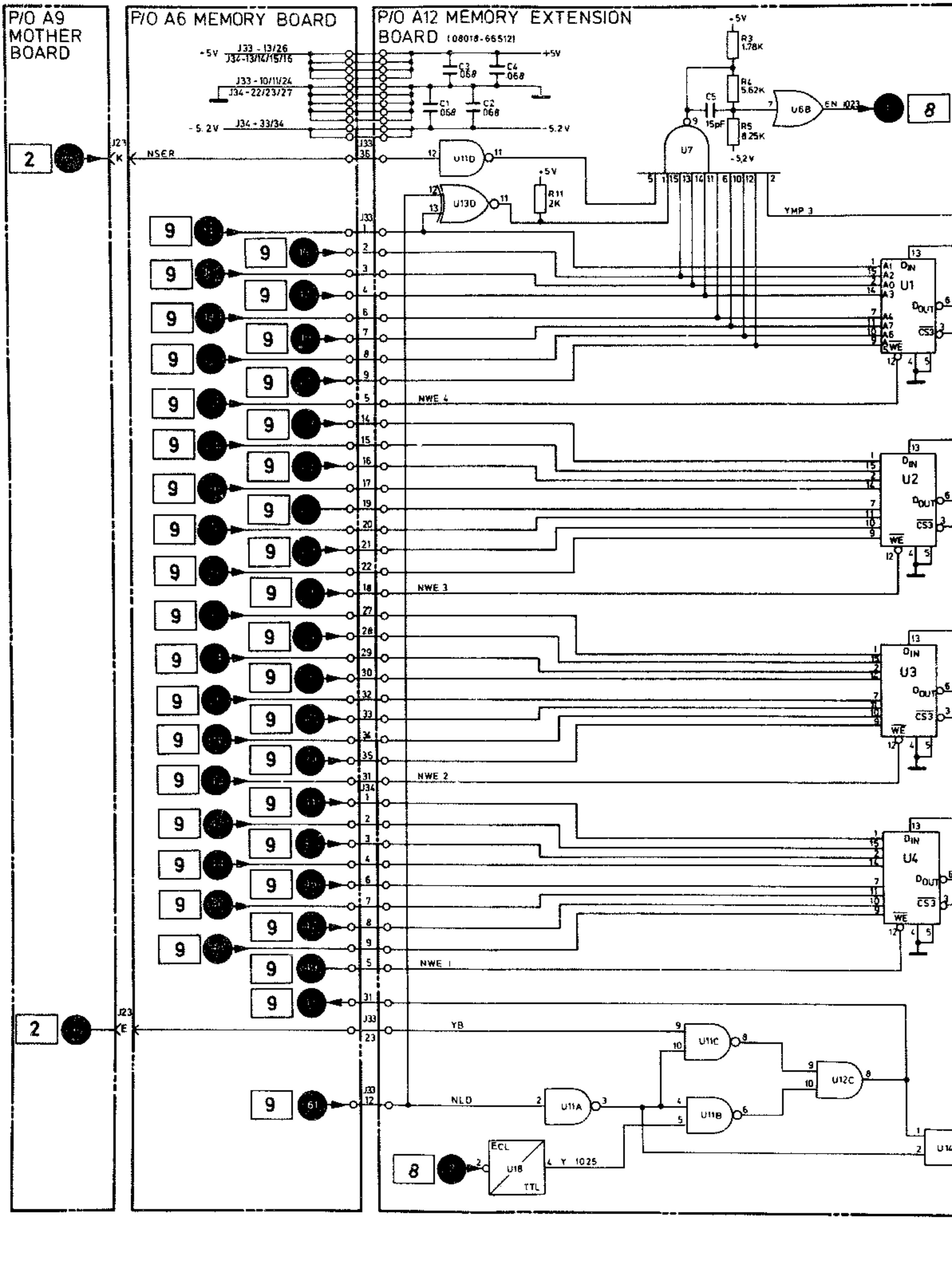

A B C D E F G
1 2 3 4 5 6
A12 MEMORY EXTENSION BOARD (08018-66512)
36
J34
1
U6
U5
U4
U3
C1
R2
R1
C3
U18
R6
U17
U16
C5
U15
U14
R10
U13
U12
U11
R7
R8
R9
C2
R5
R4
R3

10

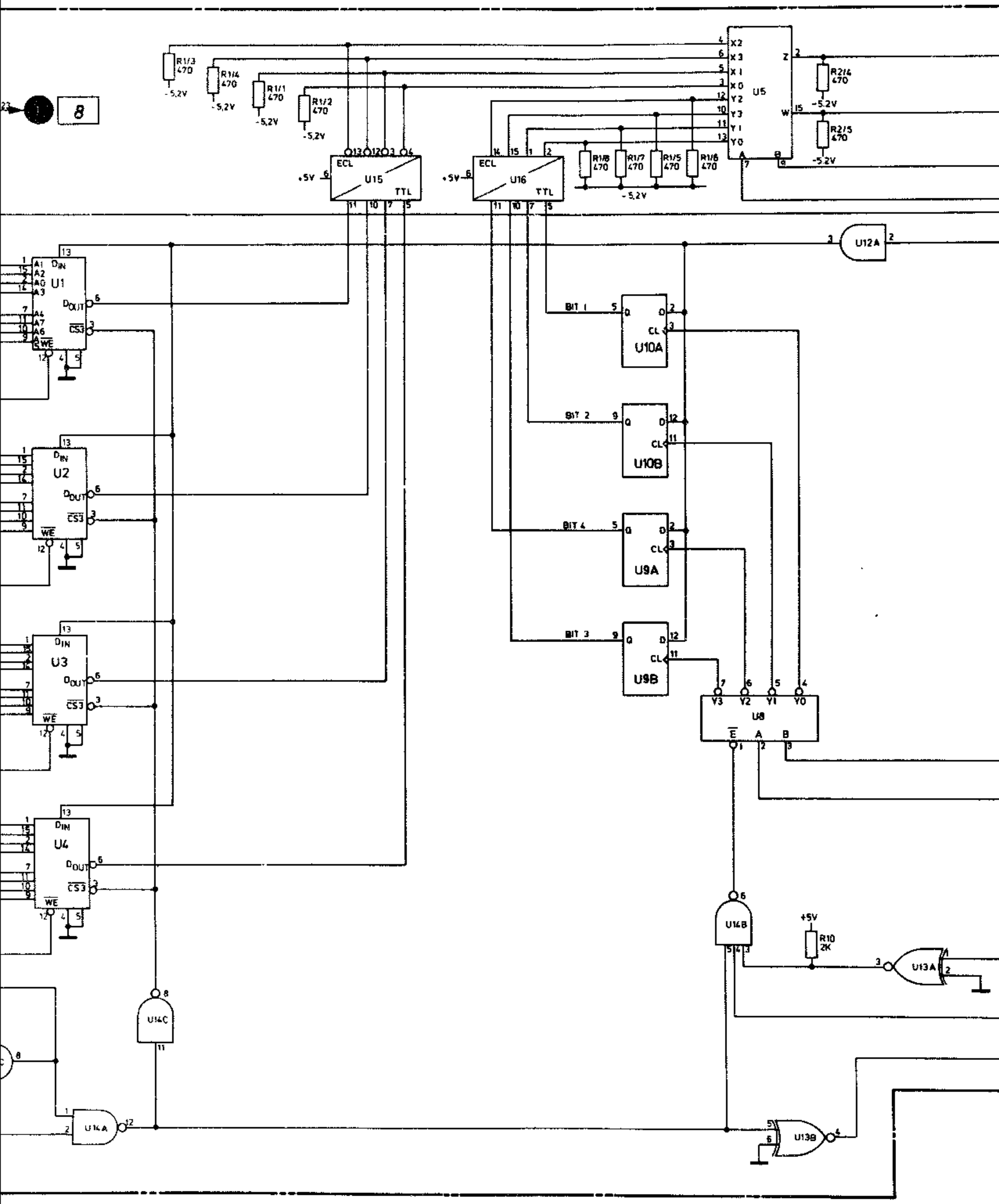

G
H
I
J
K
L
M
1
2
3
4
5
6
J33
U3
C4
U2
U1
R11
U12
U11
U10
U9
U8
U7

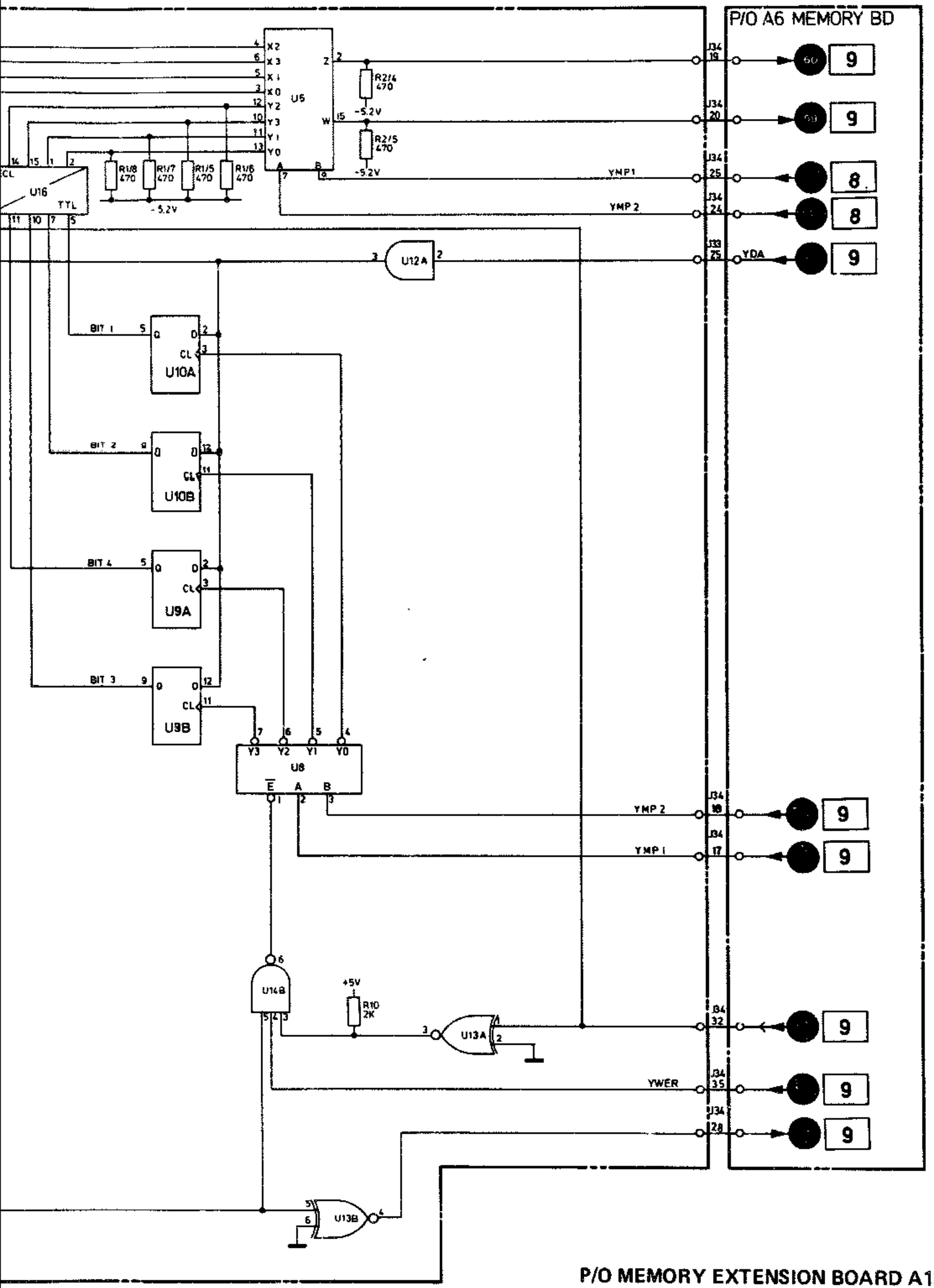


REF DESIG	GRID LOC
C1	B2
C2	C3
C3	D2
C4	H2
C5	C/D2
R1	C2
R2	B2
R3	D3
R4	D3
R5	C3
R6	A/B2
R7	A/B3
R8	A/B3
R9	A/B3
R10	E2/3
R11	K2
U1	J2
U2	H/I2
U3	G2
U4	E2
U5	C2
U6	A/B2
U7	K2/3
U8	J2/3
U9	I2/3
U10	H2/3
U11	G2/3
U12	F/G2/3
U13	F2/3
U14	E2/3
U15	D2/3
U16	C2/3
U17	B2/3
U18	A2/3



P/O A9 MOTHER BOARD
P/O A6 MEMORY BOARD
P/O A12 MEMORY EXTENSION BOARD (08018-66512)
+5V
J33 - 13/26
J34 - 13/14/15/16
J33 - 10/11/24
J34 - 22/23/27
-5.2V
J34 - 33/34
C3 .068
C4 .068
C1 .068
C2 .068
R3 1.78K
R4 5.62K
R5 8.25K
C5 15pF
U6B
EN
U7
U11D
U13D
R11 2K
NSER
YMP 3
NWE 4
NWE 3
NWE 2
NWE 1
U1
U2
U3
U4
YB
U11C
U12C
NLD
U11A
U11B
ECL
U18
TTL
Y 1025

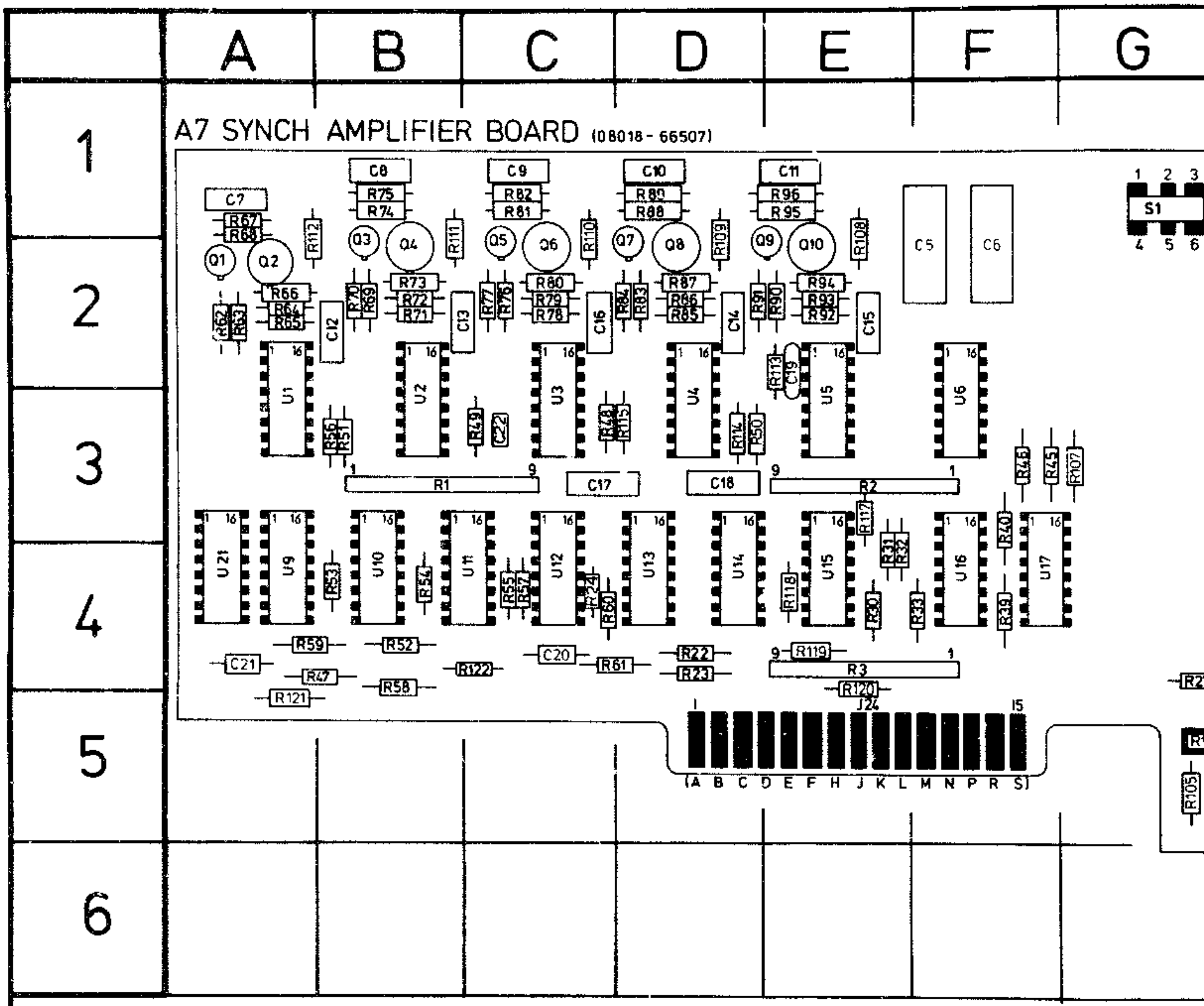

8
R1/3
470
-5,2V
R1/4
470
R1/1
470
R1/2
470
U5
X2
X3
X1
X0
Y2
Y3
Y1
Y0
Z
W
A
B
R2/4
470
-5.2V
R2/5
470
ECL
U15
TTL
U16
+5V
R1/8
470
R1/7
470
R1/5
470
R1/6
470
U12A
U1
U2
U3
U4
D_{IN}
D_{OUT}
$\overline{CS3}$
$\overline{WE}$
A1
A2
A0
A3
A4
A7
A6
A5
BIT 1
BIT 2
BIT 4
BIT 3
U10A
U10B
U9A
U9B
Q
D
CL
U8
Y3
Y2
Y1
Y0
$\overline{E}$
U14B
+5V
R10
2K
U13A
U14C
U14A
U13B

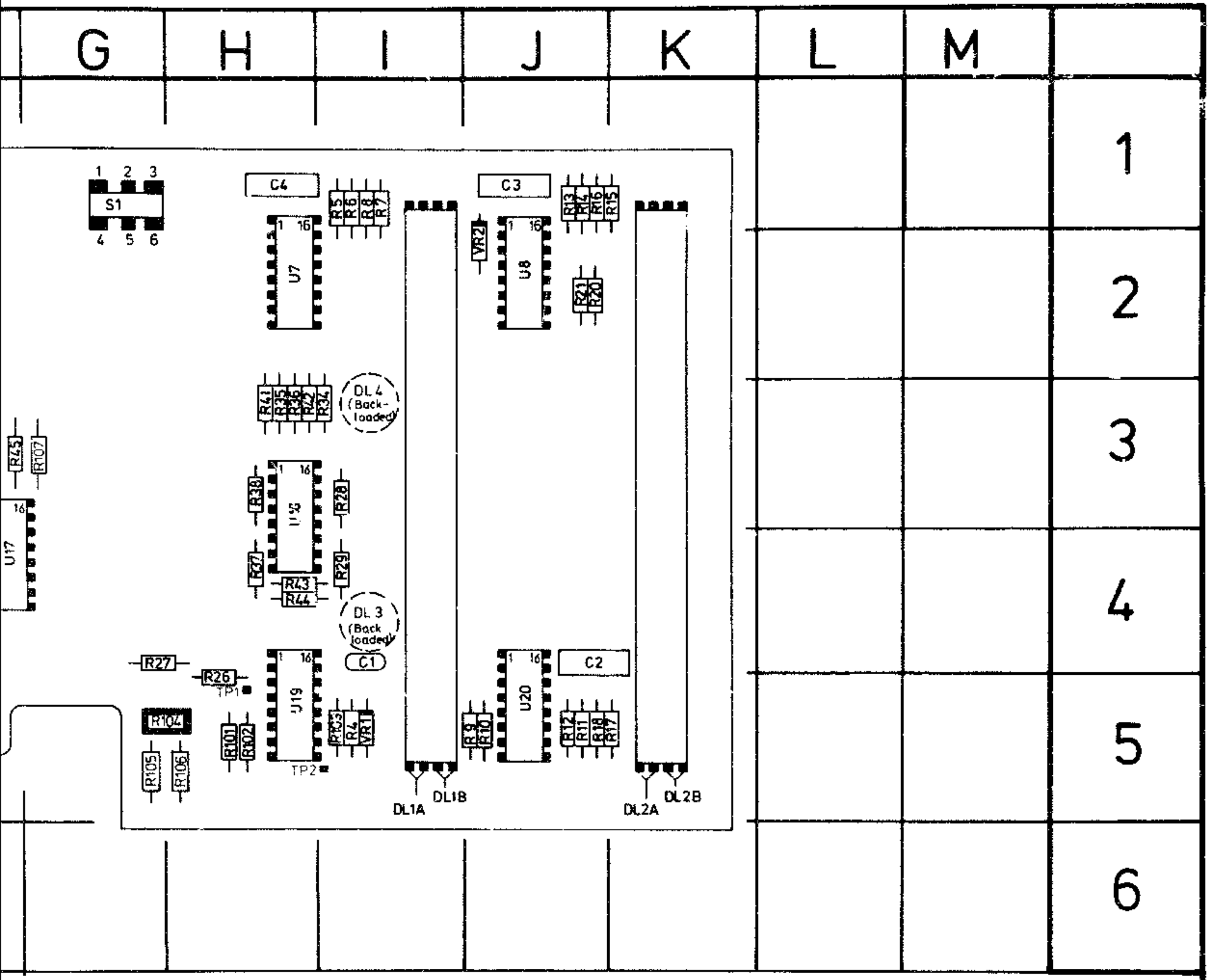


P/O MEMORY EXTENSION BOARD A12

10

A7 SYNCH AMPLIFIER BOARD (08018-66507)




G
H
I
J
K
L
M
1
2
3
4
5
6
S1
C4
C3
C2
C1
U7
U8
U19
U20
U17
VR2
VR1
R5
R6
R8
R7
R13
R14
R16
R15
R21
R20
R41
R35
R36
R42
R34
DL 4 (Back-loaded)
DL 3 (Back loaded)
R45
R107
R38
R28
R37
R29
R43
R44
R27
R26
TP1
TP2
R104
R105
R106
R101
R102
R103
R4
R9
R10
R12
R11
R18
R17
DL1A
DL1B
DL2A
DL2B

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	I4	R22	D4	R79	C2	U16	F3/4
C2	J/K4	R23	D4	R80	C2	U17	F3/4
C3	J1	R24	C4	R81	C1	U18	H3/4
C4	H1	R26	H5	R82	C1	U19	H4/5
C5	E/F1/2	R27	G4	R83	D2	U20	J4/5
C6	F1/2	R28	I3	R84	C/D2	U21	A4
C7	A1	R29	I4	R85	D2	VR1	I5
C8	B1	R30	E4	R86	D2	VR2	J2
C9	C1	R31	E4	R87	D2	TP1	H5
C10	D1	R32	E4	R88	D1	TP2	I5
C11	E1	R33	E/F4	R89	D1		
C12	A/B2	R34	I3	R90	E2		
C13	B2	R35	H3	R91	D2		
C14	D2	R36	H3	R92	E2		
C15	E2	R37	H4	R93	E2		
C16	C2	R38	H3	R94	E2		
C17	C/D3	R39	F4	R95	E1		
C18	D3	R40	F3/4	R96	E1		
C19	E2	R41	H3	R101	H5		
C20	C4	R42	H3	R102	H5		
C21	A4	R43	H4	R103	I5		
C22	C3	R44	H4	R104	G/H5		
DL1	I/...5	R45	F3	R105	G5		
DL2	K/...5	R46	F3	R106	H5		
DL3	I4	R47	A/B4	R107	G3		
DL4	I3	R48	C3	R108	E1/2		
Q1	A2	R49	B/C3	R109	D1/2		
Q2	A2	R50	D3	R110	C1/2		
Q3	B1/2	R51	B3	R111	B1/2		
Q4	B1/2	R52	B4	R112	A1/2		
Q5	C1/2	R53	B4	R113	E2		
Q6	C1/2	R54	B4	R114	D3		
Q7	C/D1/2	R55	C4	R115	C/D3		
Q8	D1/2	R56	B3	R116	A3		
Q9	D/E1/2	R57	C4	R117	E3		
Q10	E1/2	R58	B4/5	R118	E4		
R1	B/C3	R59	A4	R119	E4		
R2	E/F3	R60	C4	R120	E4/5		
R3	E/F4	R61	C/D4	R121	A5		
R4	I5	R62	A2	R122	B4		
R5	I1	R63	A2	S1	G1		
R6	I1	R64	A2	U1	A2/3		
R7	I1	R65	A2	U2	B2/3		
R8	I1	R66	A2	U3	C2/3		
R9	J5	R67	A1	U4	D2/3		
R10	J5	R68	A2	U5	E2/3		
R11	J5	R69	B2	U6	F2/3		
R12	J5	R70	B2	U7	H2		
R13	J1	R71	B2	U8	J2		
R14	J1	R72	B2	U9	A3/4		
R15	K1	R73	B2	U10	B3/4		
R16	J1	R74	B1	U11	B/C3/4		
R17	K5	R75	B1	U12	C3/4		
R18	J5	R76	C2	U13	D3/4		
R20	J2	R77	C2	U14	D3/4		
R21	J2	R78	C2	U15	E3/4		

SERVICE BLOCK 6
SYNC AND OUTPUT AMPLIFIERS A7 [11], A8 [12]

THEORY OF OPERATION

Sync Amplifier (Schematic 11)

The main function of the sync amplifier board is to compensate for the different delays due to the combination of ECL and TTL technology used within the 8018A, as well as synchronizing data and trigger signals at the 8018A outputs. For this reason, clock signal YCL2 (derived from the main clock) is used to generate clock signals for the sync flip-flops on board A7, for the timing flip-flops on the memory board A6 (YCL3, YCL4, YCL5), and for the Channel A flip-flop on board A8 (YCL6). (NOTE: Small changes in the duty cycle of YCL2 can be accomplished via R104 for operation at high frequencies). Delays lines DL1A, DL1B, DL2A and DL2B each delay YCL2 by approximately 20 ns. The resulting negative-going clock signal at U20 pin 14 is routed via gate U18 and delay line DL4 to gate U16. The signal at output pin 13 of gate U16 is then used to clock the A and B signals to control board A2; the signal at output pin 14 of gate U16 clocks the sync signals and DATA B signal to the output connectors. The DATA A output is clocked via YCL6 on the output amplifier board A8.

A second route for the U20 pin 14 signal is via U8 and U18 to generate positive-going spikes (due to the printed circuit delay line at U18 pin 11) at both gate U16 output pins 3 and 2. Both these U16 output signals are then used to set/reset flip-flops U1 → U4 to ensure that width of the WORD TRIGGER, FIRST BIT, LAST BIT and CLOCK output is half a clock period.

The negative-going spikes at gate U16 pin 5 input are also routed to gate U17 pin 13. Depending on whether RZ format is selected for DATA B, gate U17 is enabled and the output signal sets flip-flop U5 after half a clock period giving a 'return-to-zero' output signal at DATA B. Similarly, if RZ format is selected for DATA A, gate U17 pin 11 is low, the output pin 14 low then being wire-ORed with the negative-going spikes from U18 pin 13 to allow flip-flop A8 U1 to be reset after half a clock period.

The FIRST BIT and LAST BIT output signals are derived from the NLB (Last Bit) signal at J24 pin H. NLB is applied to U12 pin 11, where it is inverted and routed to flip-flop U3 pin 7 to generate the LAST BIT sync output. NLB is also routed to flip-flop U3 pin 10, where it is delayed for one clock cycle by flip-flops U3 and U2 to generate the FIRST BIT sync output.

ZERO and ONE Pause Generation (Schematic 11)

A low or high level can be generated in the pause-time between frames or words when FRAME CYCLE or WORD CYCLE is selected. If NRZ format is selected, a steady high/low level state is held for the duration of the pause-time. If RZ format is selected, an extra bit is generated within this pause-time. With switch A7 S1 set to ZERO, an ECL high is applied to U12 pin 13. This high is then routed via U14 pin 2/U13 pin 2/U13 pin 3 to the D-input of U5, which ensures that Channel B remains low at the end of a word/frame cycle if NRZ format is selected. (A high Q-output switches Q10 on and applies a low level to the DATA B output connector). Similarly the U12 high is routed via U14 pin 3/U13 pin 9 to the Channel A flip-flop U1 on board A8. Once again, this causes the channel A output to remain low at the end of a word/frame cycle when NRZ format is selected.

With switch A7S1 set to ONE, U12 pin 13 is low, this being applied to the D-inputs of the Channel A and Channel B flip-flops (A8 U1 for Channel A; A7 U5 for Channel B). As a result, the corresponding outputs remain high when NRZ format is selected.

Output Amplifier (Schematic 12)

A block diagram of the output amplifier is given in Figure 8–6–1. As can be seen from this diagram, the data signal is clocked through ECL flip-flop U1, and pre-amplified/level shifted by differential amplifiers Q1/Q2 and Q3/Q4. The signal is then routed via the main 3-stage amplifier and common-base output stage to the output connectors. A more detailed description of the individual function blocks is given in the following paragraphs.

The data signal present at the D-input of flip-flop U1 is clocked through with the negative-going transition of YCL6. If RZ output format is selected for Channel A on the front panel, U1 is then reset via a signal derived from the positive-going transition of YCL6. If NRZ format is selected, this reset signal is suppressed on board A7 via a high at gate U17 pin 14 output. This high is inverted on board A8 by gate U4 pin 14 to permanently disable the reset input of U1.

From flip-flop U1, the data signal is routed via two pre-amplifier stages, Q1/Q2 and Q3/Q4, to the main output stage. Pre-amplifier Q1/Q2 is a differential amplifier providing a level shift from the U1 ECL levels to approximately 22 V. Transistor Q27 is the voltage source for this stage. Pre-amplifier Q3/Q4 is also a differential amplifier, the voltage source being provided by Q28. With this second pre-amplifier stage, the incoming signal is attenuated according to the AMPLITUDE switch setting and AMPLITUDE VERNIER via current source U2/Q5. Resistors R79/R80 sense the current being drawn by the main output amplifier, the resultant voltage drop at U2 pin 3 causing U2 pin 6 to fall and thus increase the current through transistor Q5.

The main output amplifier comprises 3 differential amplifier stages, each stage with its own current source. With +7.5 V/+15 V amplitude selected on the front panel, all 3 stages are active. With +5 V/+10 V selected, stage Q12/Q15 is switched off by switching off the current source Q10 (25 V emitter supply is switched off). With +2.5 V/+5 V selected, both stages Q12/Q15 and Q11/Q16 are switched off by switching off current sources Q10 and Q8 respectively (25 V emitter supply switched off for both transistors). In each of the 3 amplitude switch-settings just mentioned, the current through the activated current sources is controlled via U3 and the AMPLITUDE VERNIER setting. For the ECL amplitude switch-setting, stages Q12/Q15 and Q11/Q16 are also switched off by switching off the current source transistors Q10 and Q8 respectively, the current through the active stage now being controlled by U3 and the ECL AMPLITUDE resistor A8 R23 setting. ECL offset is set via A8 R22.

The 3 common-base stages Q18/Q21, Q17/Q22 and Q19/Q20 provide coupling between the driver stage already described and the output connectors.

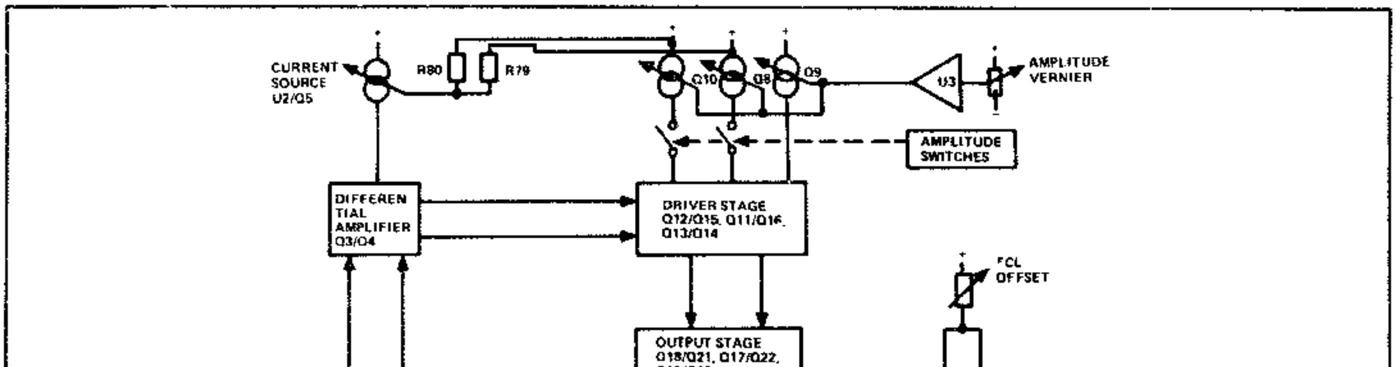
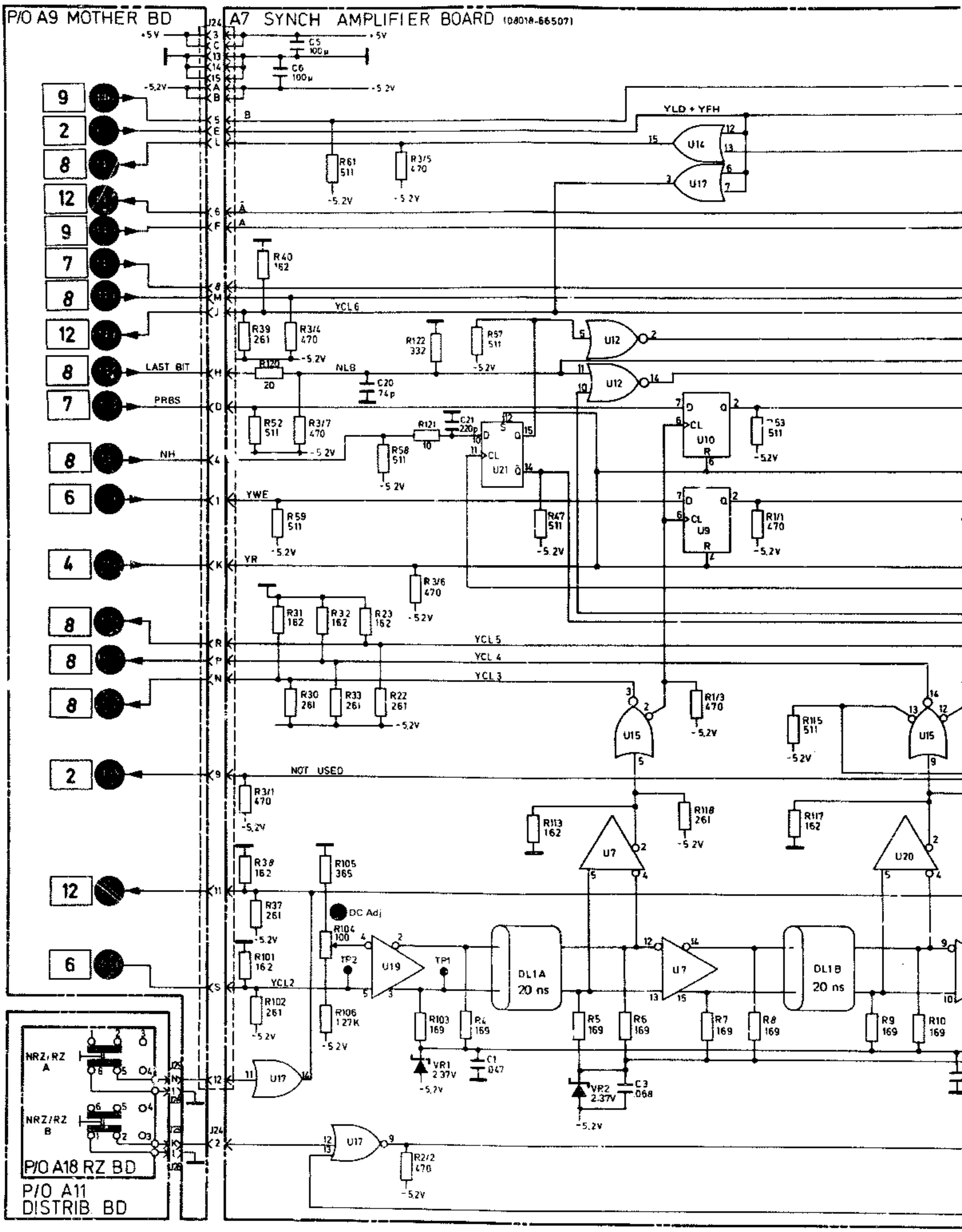
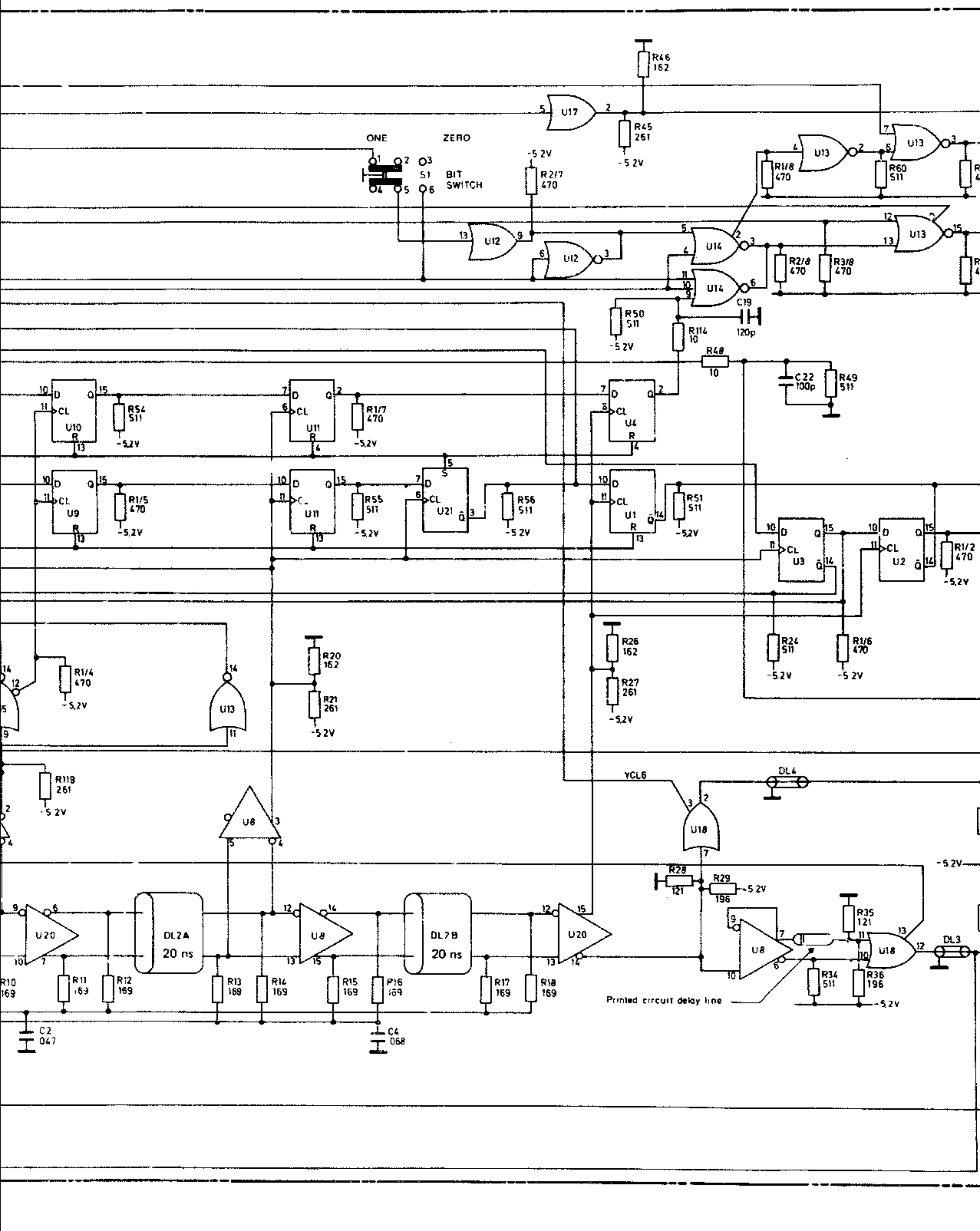
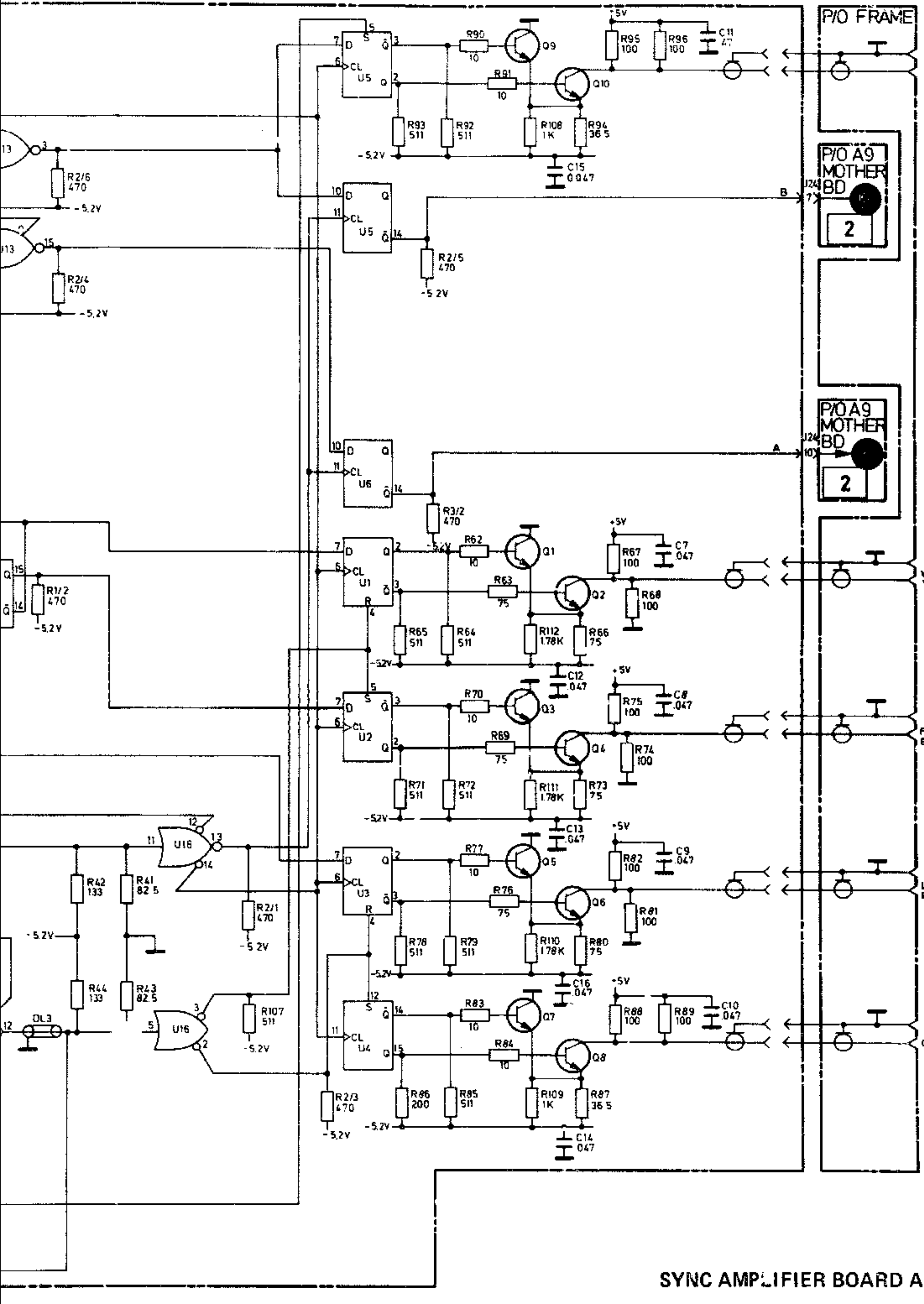


Figure 8–6–1. Output Amplifier Block Diagram


P/O A9 MOTHER BD
A7 SYNCH AMPLIFIER BOARD (08018-66507)
YLD + YFH
LAST BIT
PRBS
NH
YWE
YR
YCL 6
YCL 5
YCL 4
YCL 3
YCL2
NLB
NOT USED
DC Adj
DL1A 20 ns
DL1B 20 ns
NRZ/RZ A
NRZ/RZ B
P/O A18 RZ BD
P/O A11 DISTRIB. BD

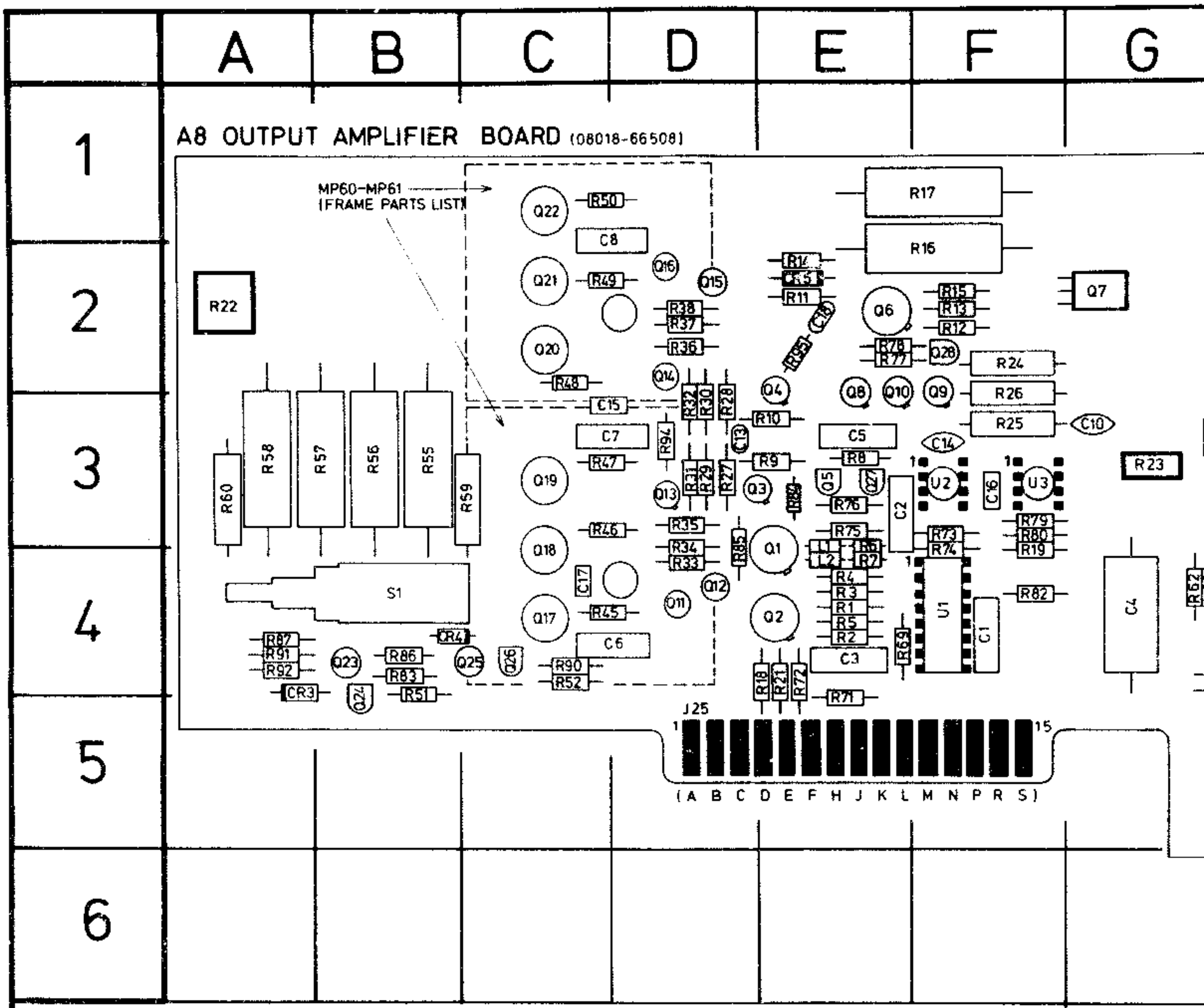

ONE
ZERO
S1
BIT SWITCH
R46 162
R45 261
-5.2V
R2/7 470
U17
U12
U13
U14
R1/8 470
R60 511
R2/8 470
R3/8 470
R50 511
R114 10
C19 120p
R48 10
C22 100p
R49 511
U10
U9
U11
U21
U4
U1
U3
U2
R54 511
R1/5 470
R1/7 470
R55 511
R56 511
R51 511
R1/2 470
R24 511
R1/6 470
R26 162
R27 261
R20 162
R21 261
R1/4 470
R118 261
U8
U18
YCL6
DL4
DL3
R28 121
R29 196
R35 121
R34 511
R36 196
Printed circuit delay line
U20
DL2A 20 ns
DL2B 20 ns
R10 169
R11 169
R12 169
R13 169
R14 169
R15 169
R16 169
R17 169
R18 169
C2 047
C4 068



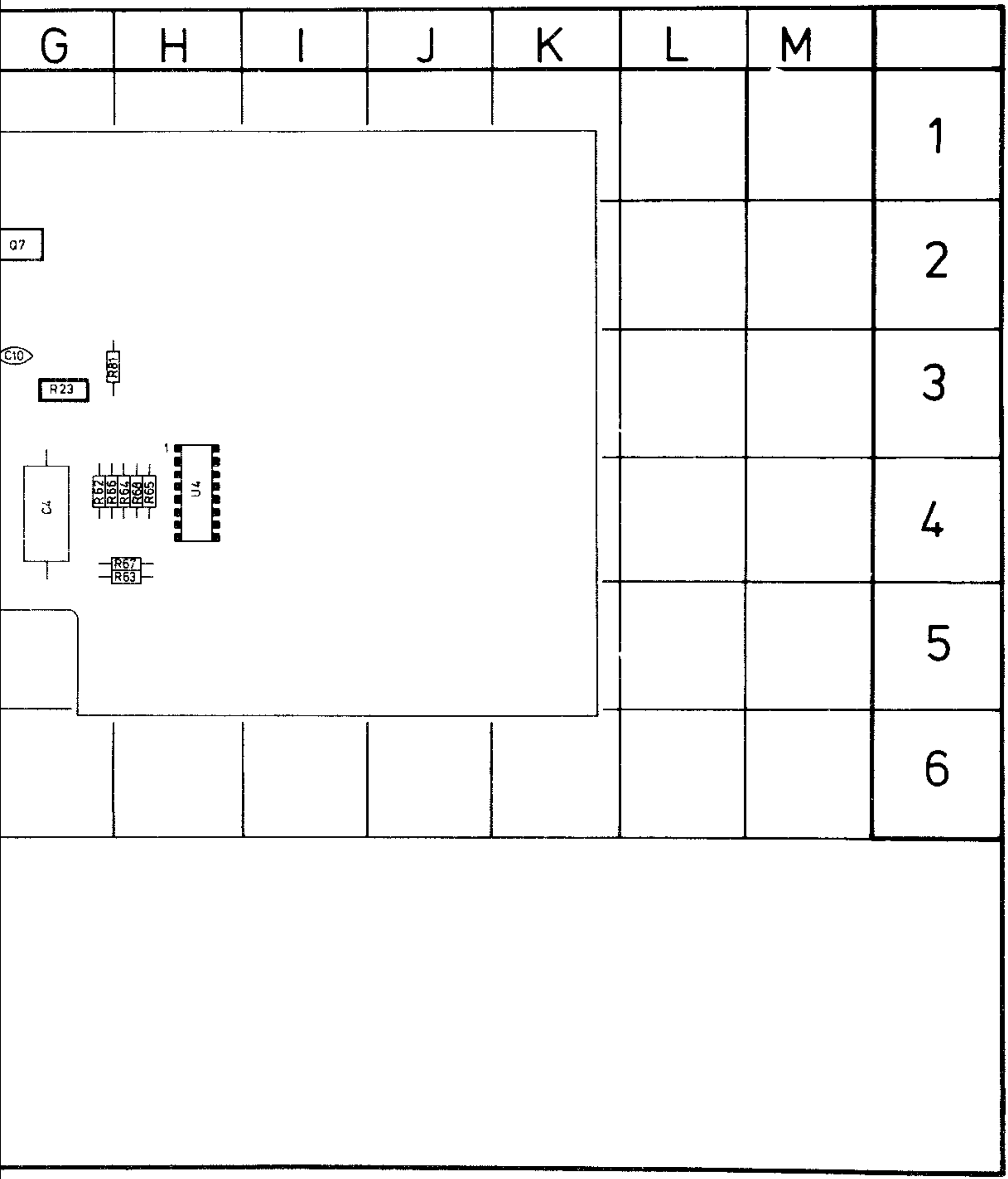
SYNC AMPLIFIER BOARD A7

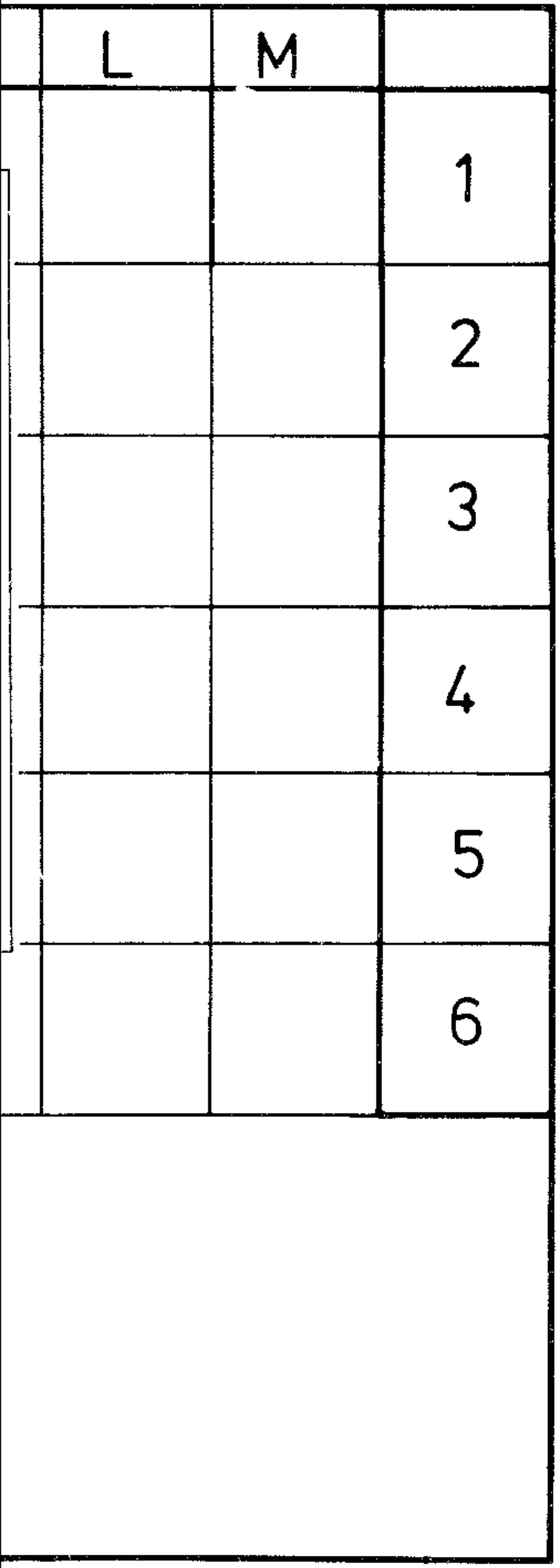
11

A8 OUTPUT AMPLIFIER BOARD (08018-66508)

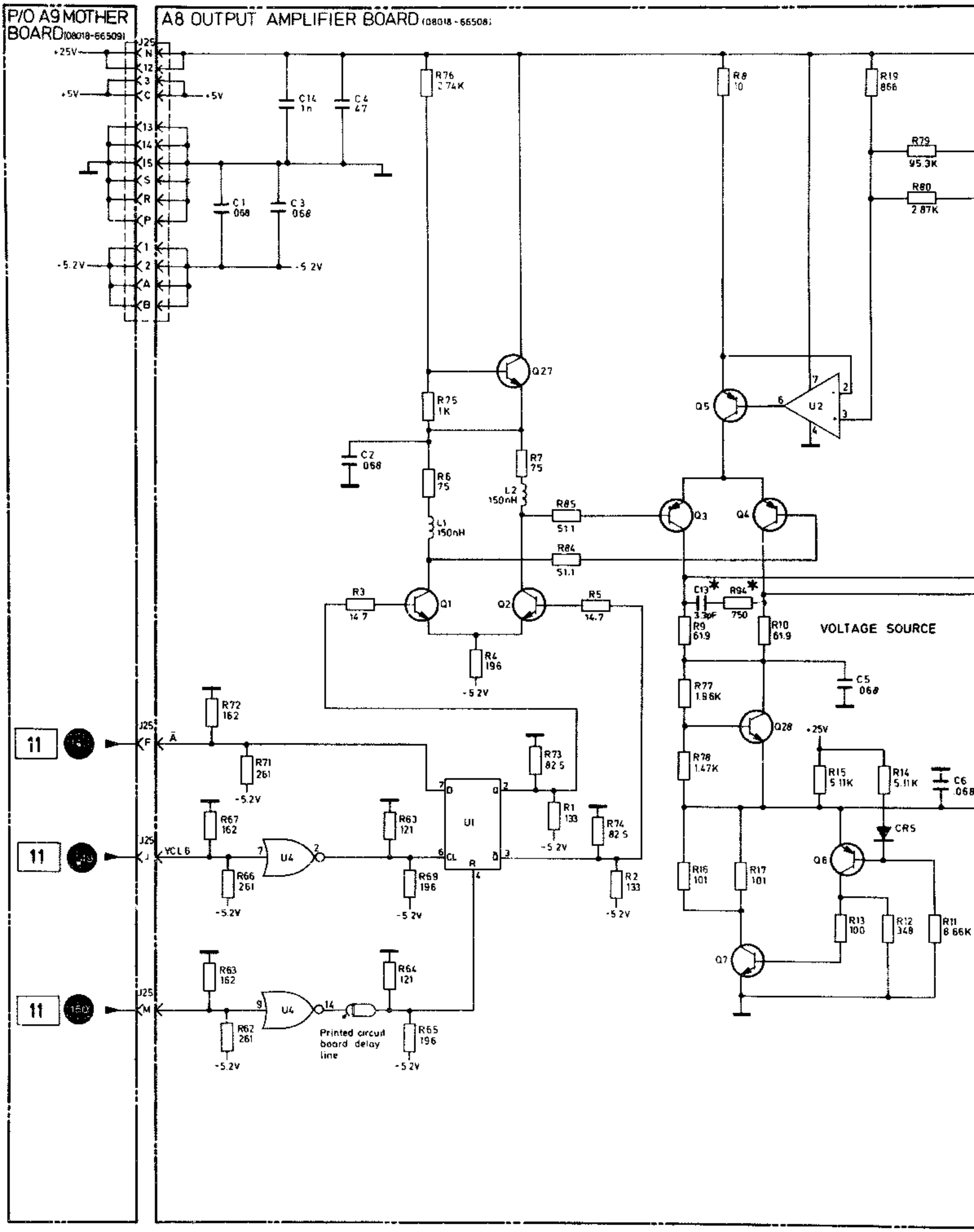


12

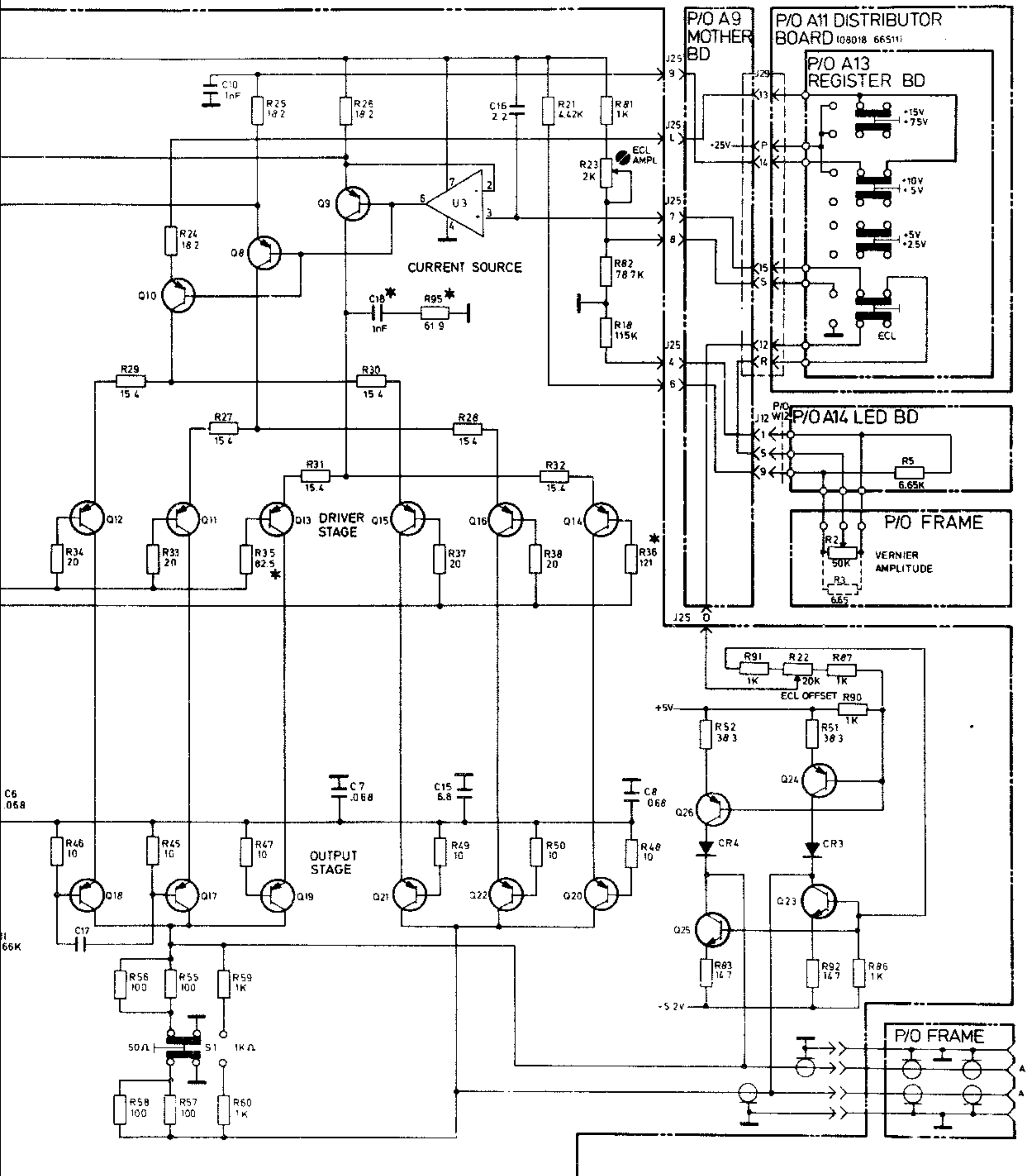

G
H
I
J
K
L
M
1
2
3
4
5
6
Q7
C10
R81
R23
1
U4
C4
R62
R66
R64
R68
R65
R67
R63



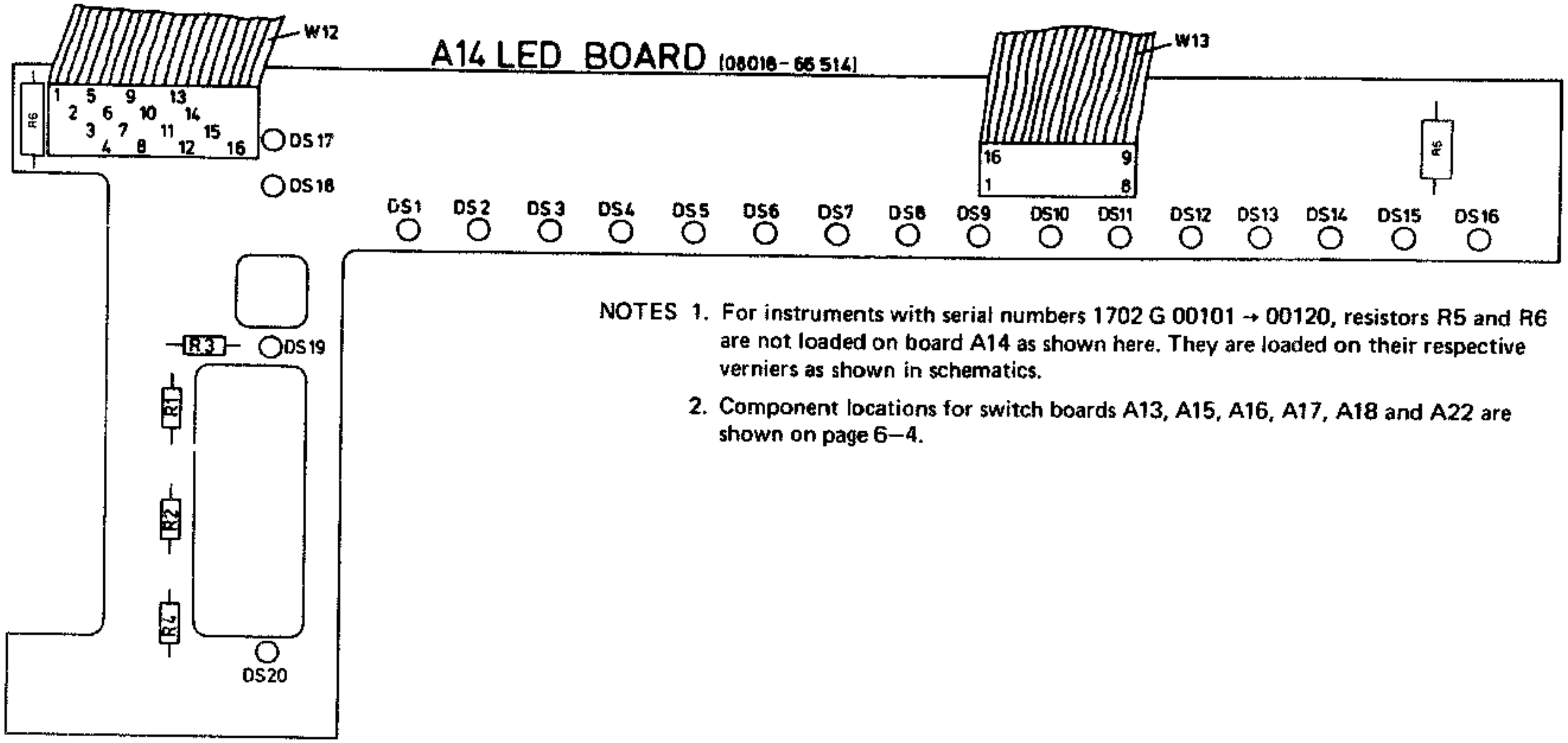
REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	F4	R6	E3	R73	F3
C2	E3	R7	E4	R74	F3/4
C3	E4	R8	E3	R75	E3
C4	G4	R9	D/E3	R76	E3
C5	E3	R10	D/E3	R77	E2
C6	C/D4	R11	E2	R78	E2
C7	C/D3	R12	F2	R79	F3
C8	C/D1	R13	F2	R80	F3
C9	E4	R14	E2	R81	G3
C10	G3	R15	F2	R82	F4
C11	E2	R16	E/F1/2	R83	B4
C12	E2	R17	E/F1	R84	D/E3
C13	D3	R18	D4	R85	D3/4
C14	F3	R19	F3/4	R86	B4
C15	C/D3	R21	F4	R87	A4
C16	F3	R22	A2	R90	C4
C17	C4	R23	G3	R91	A4
C18	E2	R24	F2	R92	A4
CR3	A4	R25	F3	R94	D3
CR4	B4	R26	F2	R95	E2
CR5	E2	R27	D3	S1	A/B4
L1	C3/4	R28	D2/3	U1	F4
L2	C2	R29	D3	U2	F3
Q1	E3/4	R30	D2/3	U3	F3
Q2	E4	R31	D3	U4	H4
Q3	D3	R32	D2/3		
Q4	E2	R33	D4		
Q5	E3	R34	D3/4		
Q6	E2	R35	D3		
Q7	F2	R36	D2		
Q8	E2	R37	D2		
Q9	F2	R38	D2		
Q10	E2	R45	C/D4		
Q11	D4	R46	C3		
Q12	D4	R47	C3		
Q13	D3	R48	C2		
Q14	D2	R49	C/D2		
Q15	D2	R50	C/D1		
Q16	D2	R51	B4		
Q17	C4	R52	C4		
Q18	C3/4	R55	B3		
Q19	C3	R56	B3		
Q20	C2	R57	A/B3		
Q21	C2	R58	A3		
Q22	C1	R59	B/C3		
Q23	B4	R60	A3		
Q24	B4/5	R62	G4		
Q25	B/C4	R63	H4		
Q26	C4	R64	H4		
Q27	E3	R65	H4		
Q28	F2	R66	G4		
R1	E4	R67	H4		
R2	E4	R68	H4		
R3	E4	R69	E4		
R4	E4	R71	E4		
R5	E4	R72	E4		



P/O A9 MOTHER BOARD (08018-66509)
A8 OUTPUT AMPLIFIER BOARD (08018-66508)
J25
+25V
+5V
-5.2V
C14 1n
C4 47
C1 .068
C3 .068
R76 2.74K
Q27
R75 1K
C2 .068
R6 75
L1 150nH
R7 75
L2 150nH
R85 51.1
R84 51.1
Q1
Q2
R3 14.7
R5 14.7
R4 196
R8 10
R19 866
R79 95.3K
R80 2.87K
Q5
U2
Q3
Q4
C13 3.3pF
R94 750
R9 61.9
R10 61.9
VOLTAGE SOURCE
C5 .068
R77 1.96K
Q28
R78 1.47K
R15 5.11K
R14 5.11K
C6 .068
CR5
Q6
R16 101
R17 101
R13 100
R12 348
R11 8.66K
Q7
R72 162
R71 261
R73 82.5
R1 133
R74 82.5
R2 133
U1
R67 162
R66 261
U4
YCL6
R63 121
R69 196
R63 162
R62 261
R64 121
R65 196
Printed circuit board delay line
11



OUTPUT AMPLIFIER BOARD A8



NOTES 1. For instruments with serial numbers 1702 G 00101 → 00120, resistors R5 and R6 are not loaded on board A14 as shown here. They are loaded on their respective verniers as shown in schematics.

2. Component locations for switch boards A13, A15, A16, A17, A18 and A22 are shown on page 6—4.

SERVICE BLOCK 7
PARALLEL/SERIAL LOADING, BOARDS A9, A13, A14 13

THEORY OF OPERATION

Shift registers U9 and U10 on board A9 can be loaded in parallel when input SO (NLD + NFH) is set to high, and in serial when SO (NLD + NFH) is set to low. In both cases, a positive clock transition is required at the clock input to load data. The parallel inputs are A to H and the serial input is L1. Both shift registers are connected in series whereby U10 pin 22 (L1) is the serial data input and QA of U9 the serial data output (NDRO).

Parallel Loading (FETCH and LOAD pushbutton released)

If one of the pushbuttons for bits 1 to 16 (register board A13) is pressed, one of the EX-OR gate inputs of U11 to U14 is set to high via resistor arrays R5 and R6. Depending on the state of the corresponding shift register output, the output of the EX-OR gate becomes high or stays low. The necessary clock transition to load the state of the EX-OR gate into the shift register is the signal YMCL which changes from low to high when one of the pushbuttons 1–16 is pressed and is fed to the control board A2 U24C where it is differentiated by C9. The differentiated signal is applied to A2 U8A and clocks the shift registers on board A9 as YCLDR (clock data register). With this clock transition the information at the shift register input is transferred to the Q output and turns the corresponding LED on or off.

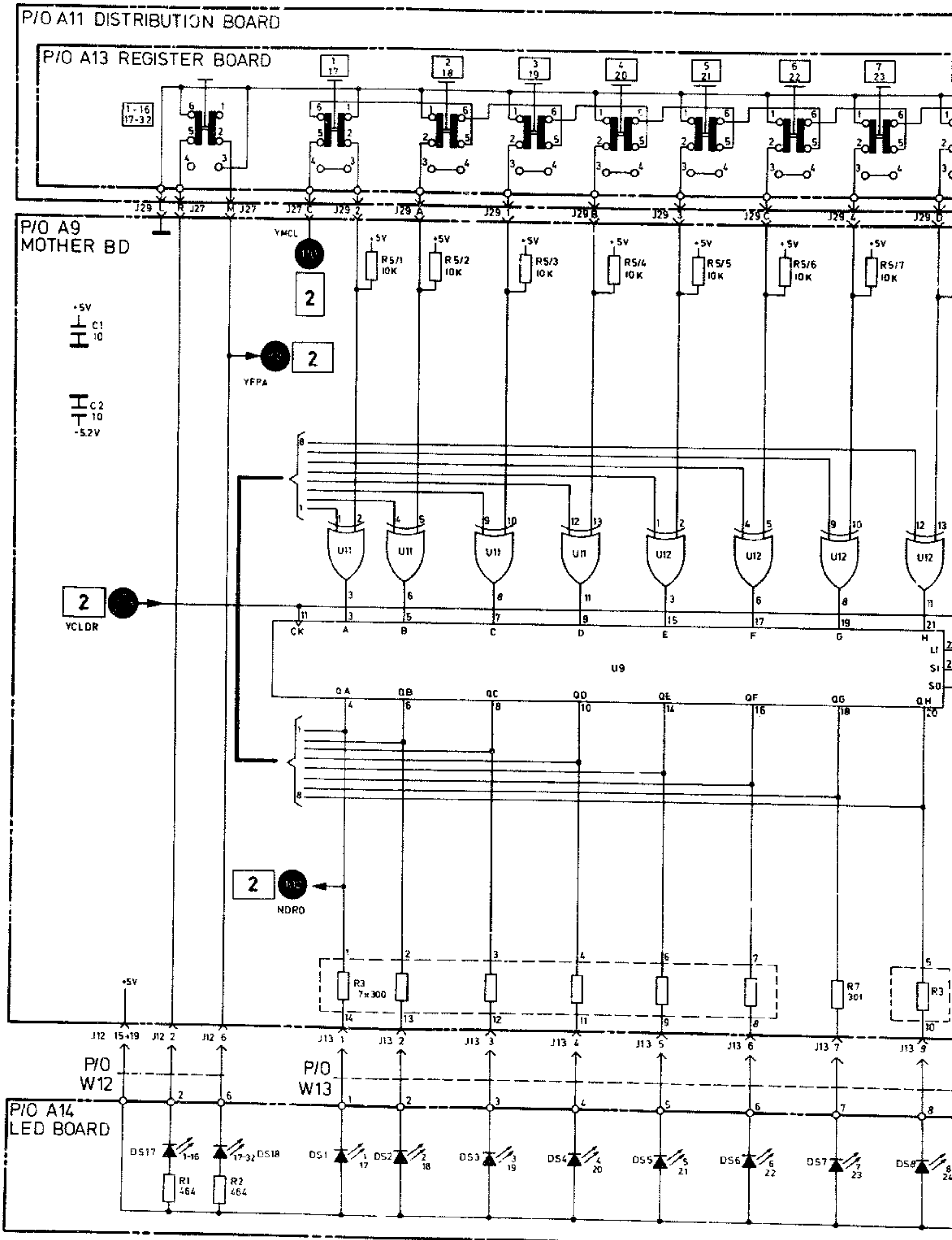
Serial Loading

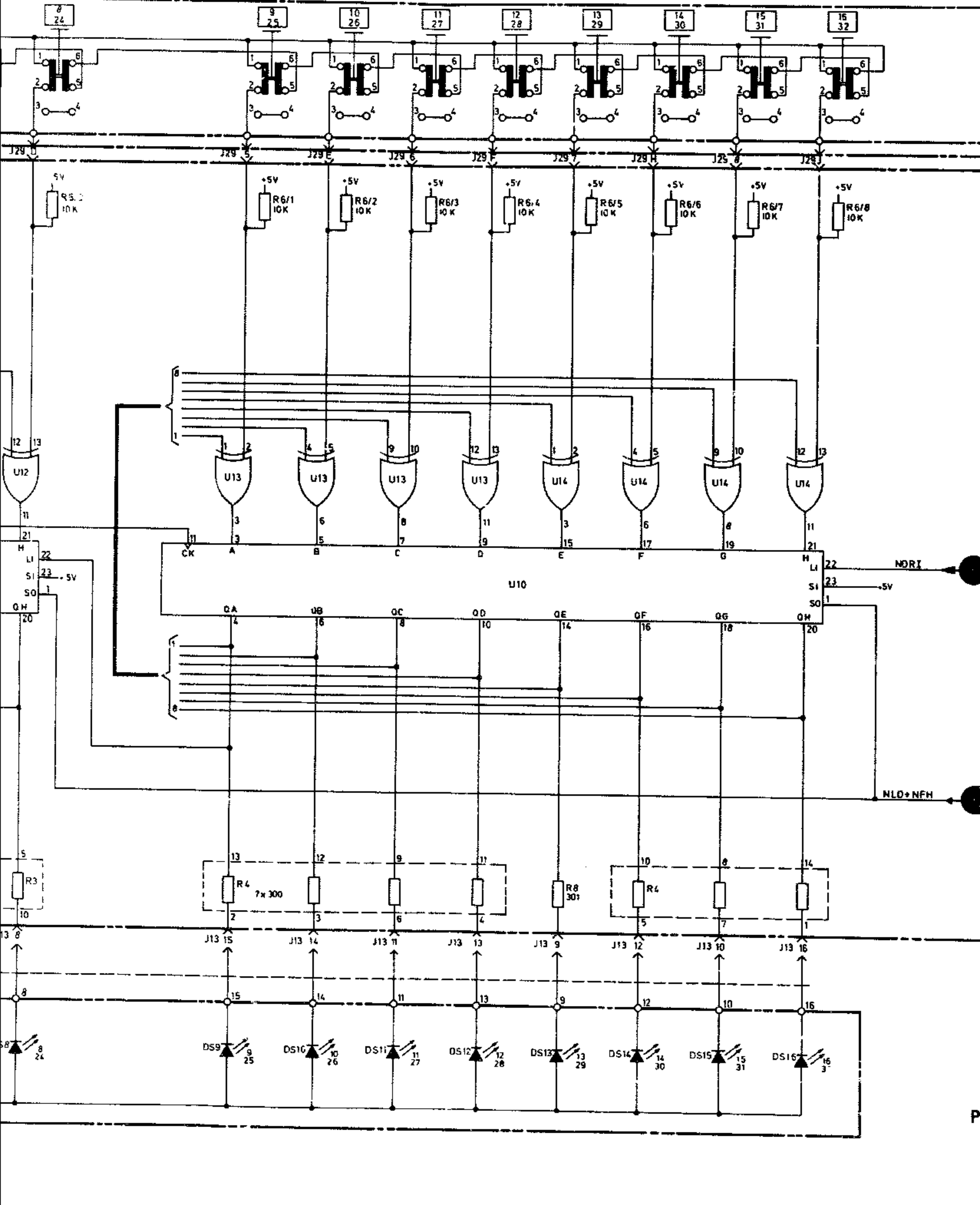
When pressing FETCH or LOAD, signal NLD + NFH becomes low (true). This programs the shift register to shift left (load serial). The register clock (YCLDR) is generated by the ASM on the A2 Control Board.

With LOAD is pressed, the data content of the shift registers is clocked as signal NDRO via A2 U1B, U14A, U1C to the memory (YDA).

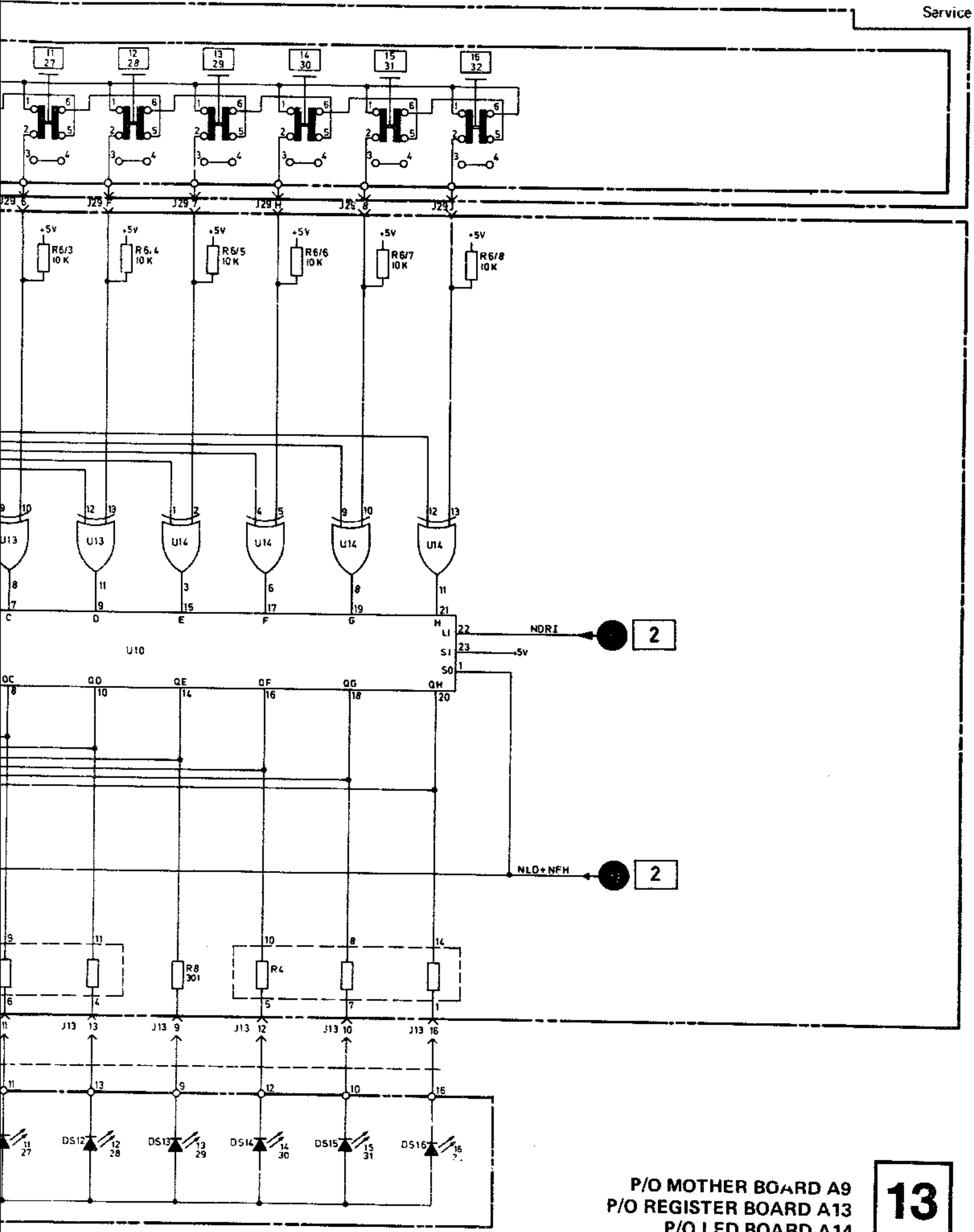
In addition, data (YDA) is fed back via A2 U1D and A2 U13A to the data register input (NDRI) at A9 U10 pin 22. By feeding back the data to the shift register A9 U10/U9, the data content and the LED data patterns display is still present after LOAD has been released.

With FETCH pressed, data is loaded into the shift register from the Channel A memory via A2 U18B, A2 U14C and A2 U13A and from the Channel B memory via A2 U19A, A2 U14B and A2 U13A.


P/O A11 DISTRIBUTION BOARD
P/O A13 REGISTER BOARD
P/O A9
MOTHER BD
YMCL
YFPA
YCLDR
NDRO
U9
U11
U12
R5/1 10K
R5/2 10K
R5/3 10K
R5/4 10K
R5/5 10K
R5/6 10K
R5/7 10K
R3 7x300
R7 301
C1 10
C2 10
+5V
-5.2V
J29
J27
J12
J13
P/O W12
P/O W13
P/O A14
LED BOARD
DS17
DS18
DS1
DS2
DS3
DS4
DS5
DS6
DS7
DS8
R1 464
R2 464
1-16
17-32

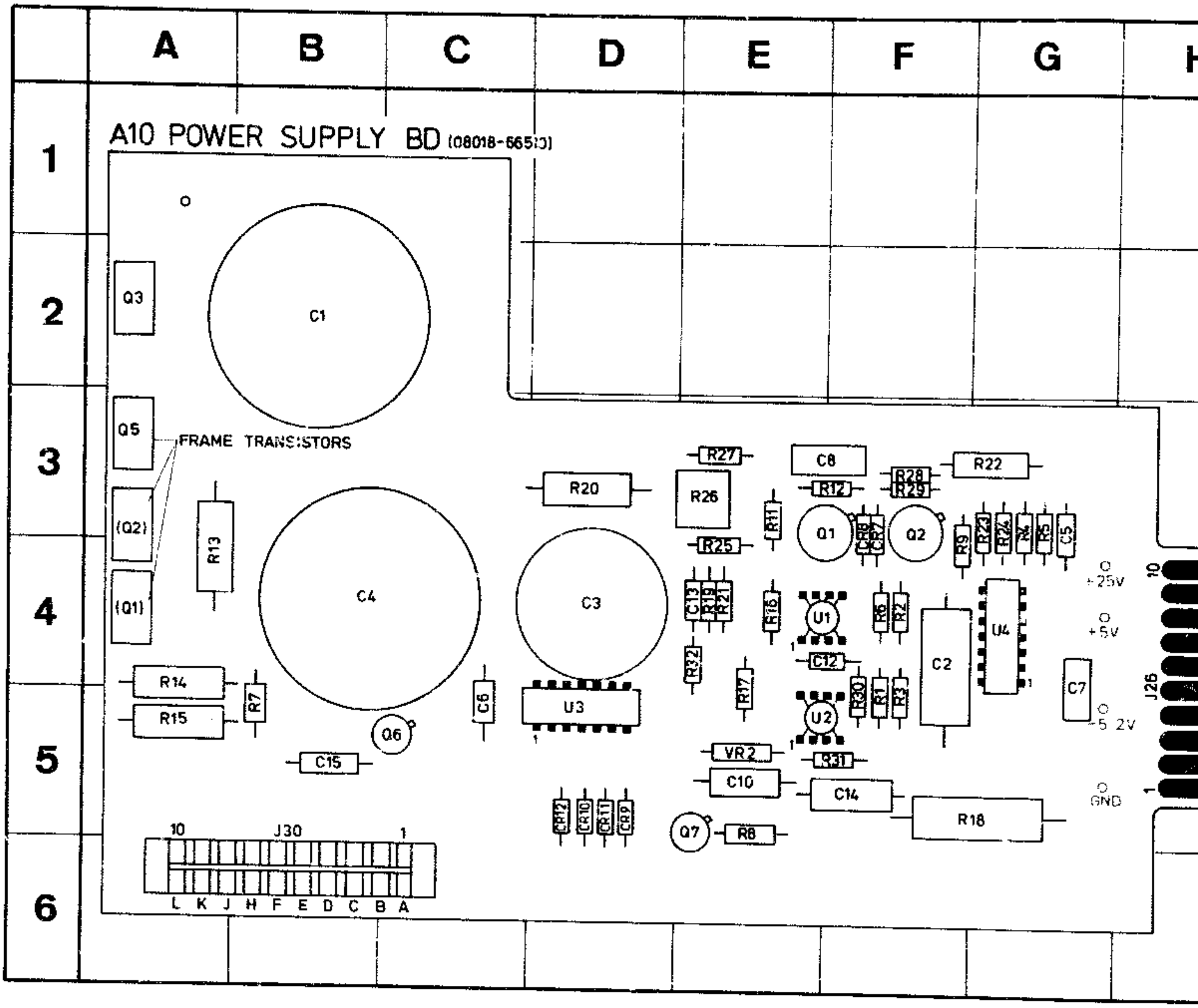


U12
U13
U14
U10
NDRI
NLO+NFH
R4
7x300
R8
301
R3
J29
J13
DS9
DS10
DS11
DS12
DS13
DS14
DS15
DS16

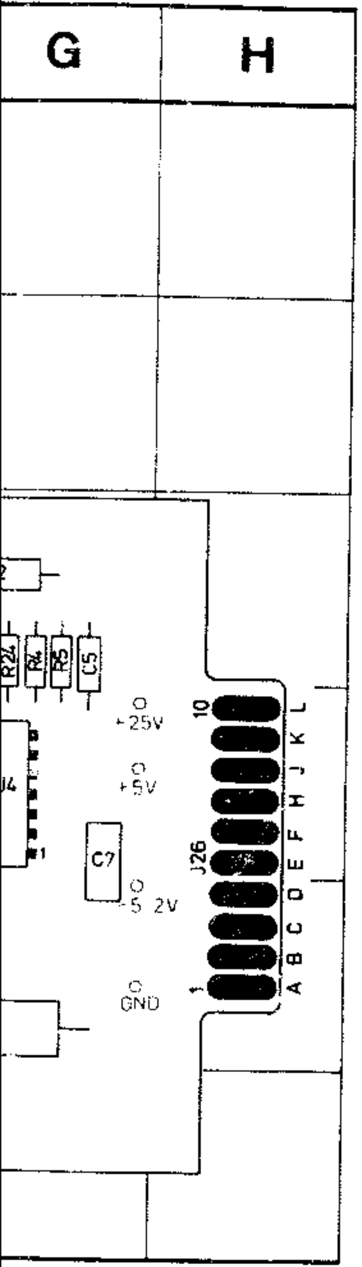


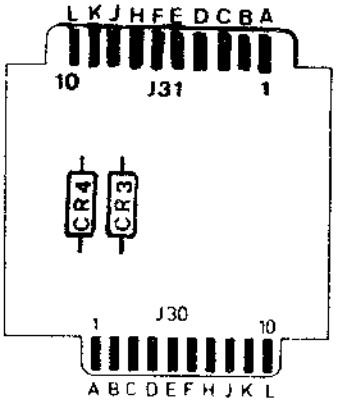
P/O MOTHER BOARD A9
P/O REGISTER BOARD A13
P/O LED BOARD A14

13


A10 POWER SUPPLY BD (08018-66510)
FRAME TRANSISTORS
J30
J26
+25V
+5V
-5 2V
GND

14





A29 RECTIFIER BOARD (08018-66529)

SERVICE BLOCK 8
POWER SUPPLY BOARD A10 14

THEORY OF OPERATION

General

Power Supply Board A10 provides 3 series regulated voltages (+2.5 V, +5 V and −5.2 V) for internal circuit operation of the 8018A. The +25 V supply is used as reference voltage for the +5 V supply, the +5 V supply then being used as reference voltage for the −5.2 V supply. (Note: When adjusting the +25 V supply via R26, adjustment should be made such that the +5 V supply registers exactly +5 V at the supply test pin).

+25 V Supply

In normal operation, series regulation is provided by transistor Q1 the base current of which is delivered by U3 pin 11 via Q6. Current limiting is provided by pins 2 and 3 of IC U3 which detect any excess current through resistor R20 and adjust the Q6 emitter current (Q1 base current) accordingly. Voltage regulation is achieved by U3 pin 4 which senses any change in the +25 V supply voltage via voltage divider R25/R26/R27. Any upward swing in the supply voltage causes the current to Q6 emitter (Q1 base) to be reduced. The supply voltage for U3 operation is determined via Q7 and Zener diode VR2 at pin 12 of U3.

+5 V Supply

Operation of this supply is similar to that for the +25 V supply, series regulation being provided by transistor pair Q2/Q5.

Current limiting is provided by pins 2 and 3 of U4 which detect any excess current through R22, and adjust the Q2 base current (and therefore the Q2/Q5 base currents) accordingly.

Voltage regulation is a achieved via U4 pin 4 which senses the +5 V supply voltage and adjusts the Q2 base current accordingly. Any upward swing in the supply voltage causes the Q2 base current to be reduced (and therefore the Q2/Q5 base currents).

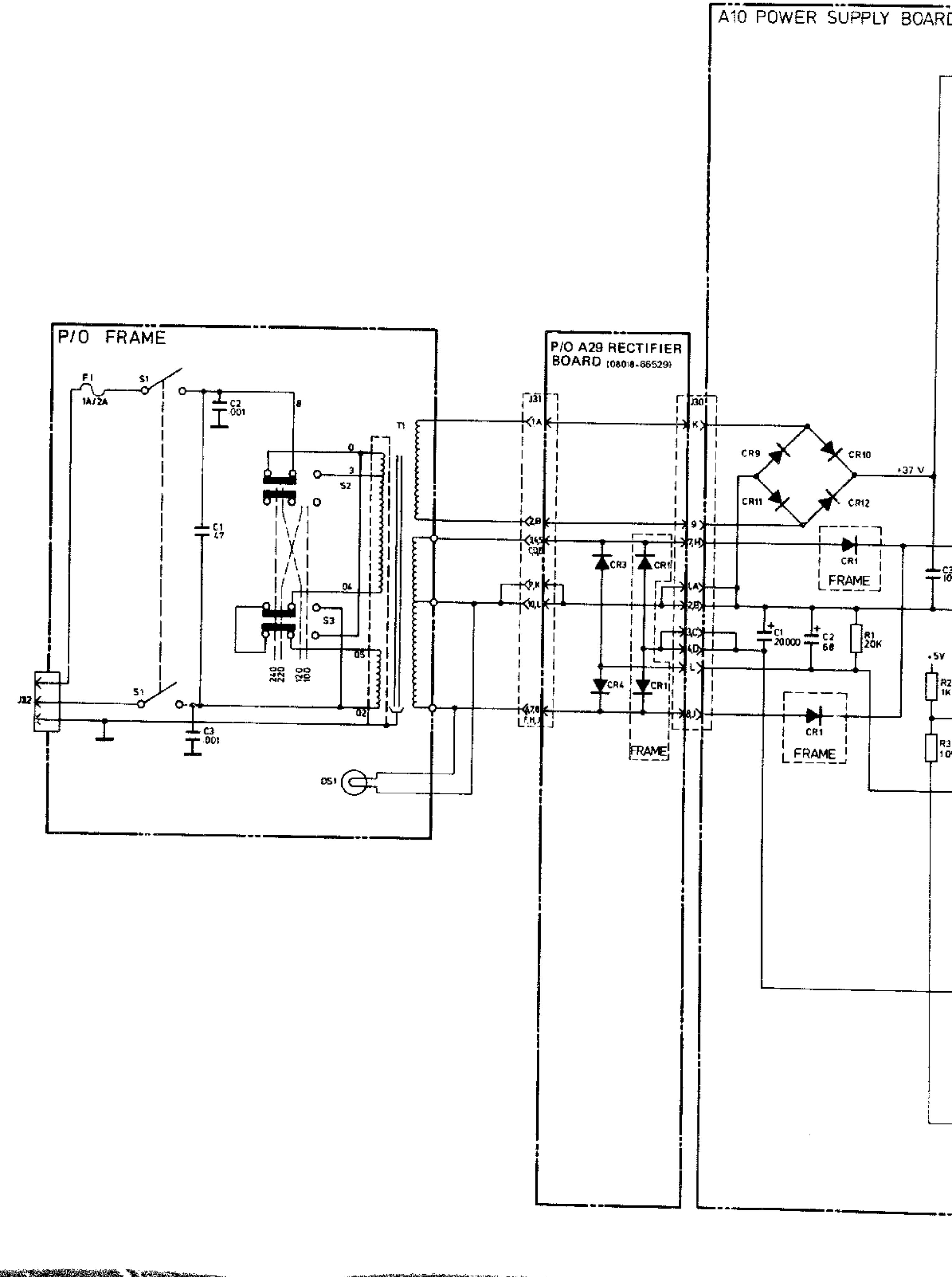
−5.2 V Supply

For the −5.2 V supply, transistor Q4 is used for series regulation, the base current of Q4 being delivered by Darlington pair Q1/Q3.

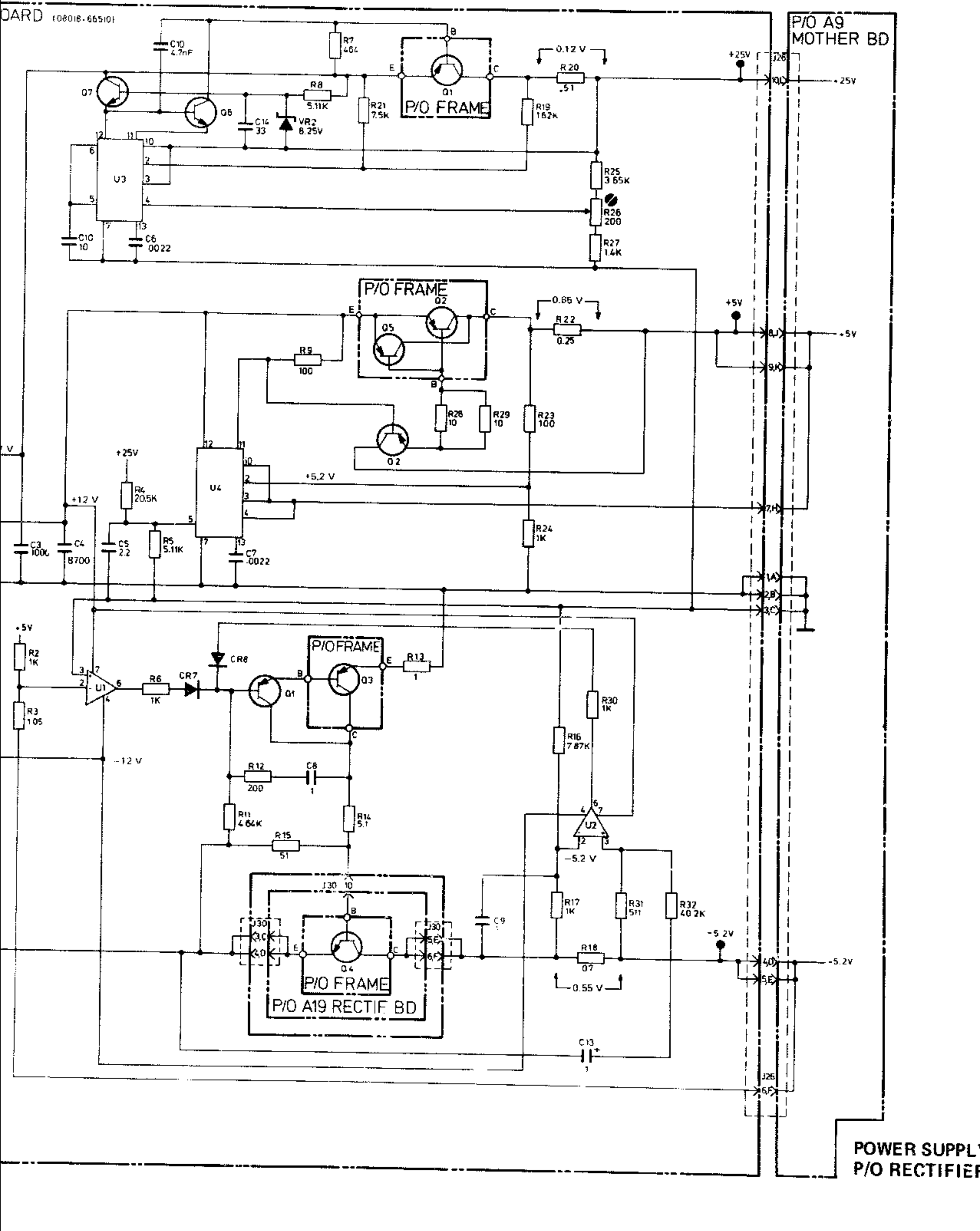
Current limiting is provided by operational amplifier U2, resistor R30, and diode CR8, U2 sensing any excess current through R18. Voltage regulation is via operational amplifier U1, resistor R6 and diode CR7, any fluctuation in the −5.2 V supply voltage being sensed via R3.

TROUBLESHOOTING

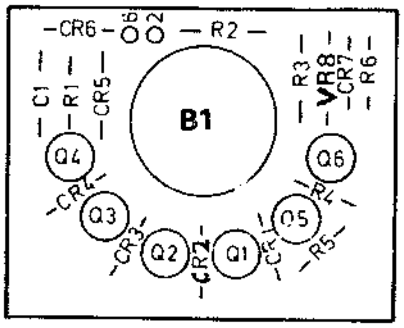
Begin troubleshooting in the power supply area by measuring the supply voltages in the following sequence – +25 V, +5 V, −5.2 V. The next step should then be to measure the voltage drop across current limiting resistors R20, R22 and R18 and check against the values given in the schematic.



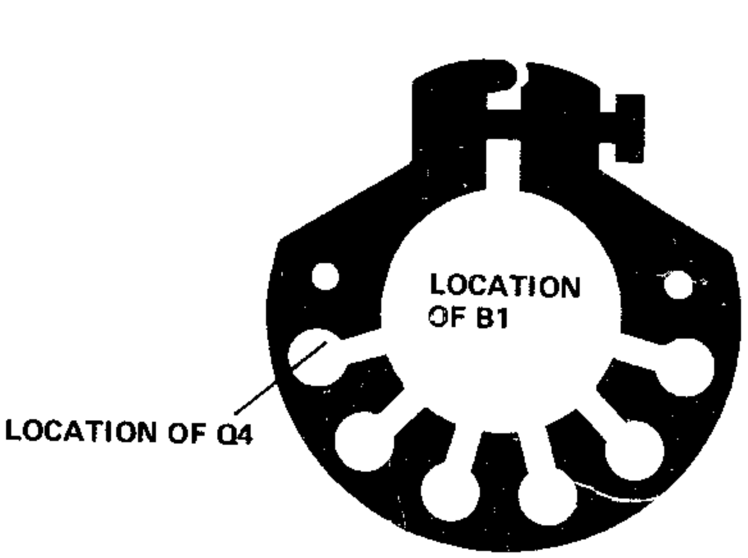
A10 POWER SUPPLY BOARD
P/O FRAME
P/O A29 RECTIFIER
BOARD (08018-66529)
F1
1A/2A
S1
C2
.001
C1
.47
C3
.001
J32
S2
S3
T1
DS1
240
220
120
100
J31
J30
CR9
CR10
CR11
CR12
+37 V
CR3
CR4
CR1
FRAME
C1
20000
C2
68
R1
20K
+5V



OARD (08018-66510)
P/O A9
MOTHER BD
P/O FRAME
P/O FRAME
P/OFRAME
P/O FRAME
P/O A19 RECTIF BD
C10 4.7nF
R7 464
Q1
Q7
Q6
C14 33
VR2 8.25V
R8 5.11K
R21 7.5K
R20 .51
0.12 V
R19 162K
+25V
J26
+25V
U3
R25 3.65K
R26 200
R27 1.4K
C10 10
C6 .0022
Q2
Q5
R9 100
0.65 V
R22 0.25
+5V
+5V
R28 10
R29 10
R23 100
Q2
U4
+5.2 V
+12 V
+25V
R4 20.5K
R5 5.11K
C3 1000
C4 8700
C5 2.2
C7 .0022
R24 1K
+5V
R2 1K
R3 105
U1
R6 1K
CR7
CR8
Q1
Q3
R13 1
-12 V
R12 200
C8 1
R11 4.64K
R14 5.1
R15 51
R30 1K
R16 7.87K
U2
-5.2 V
J30
Q4
C9
R17 1K
R31 511
R32 40.2K
R18 .07
0.55 V
-5.2V
-5.2V
C13 1
J26
POWER SUPPLY
P/O RECTIFIER

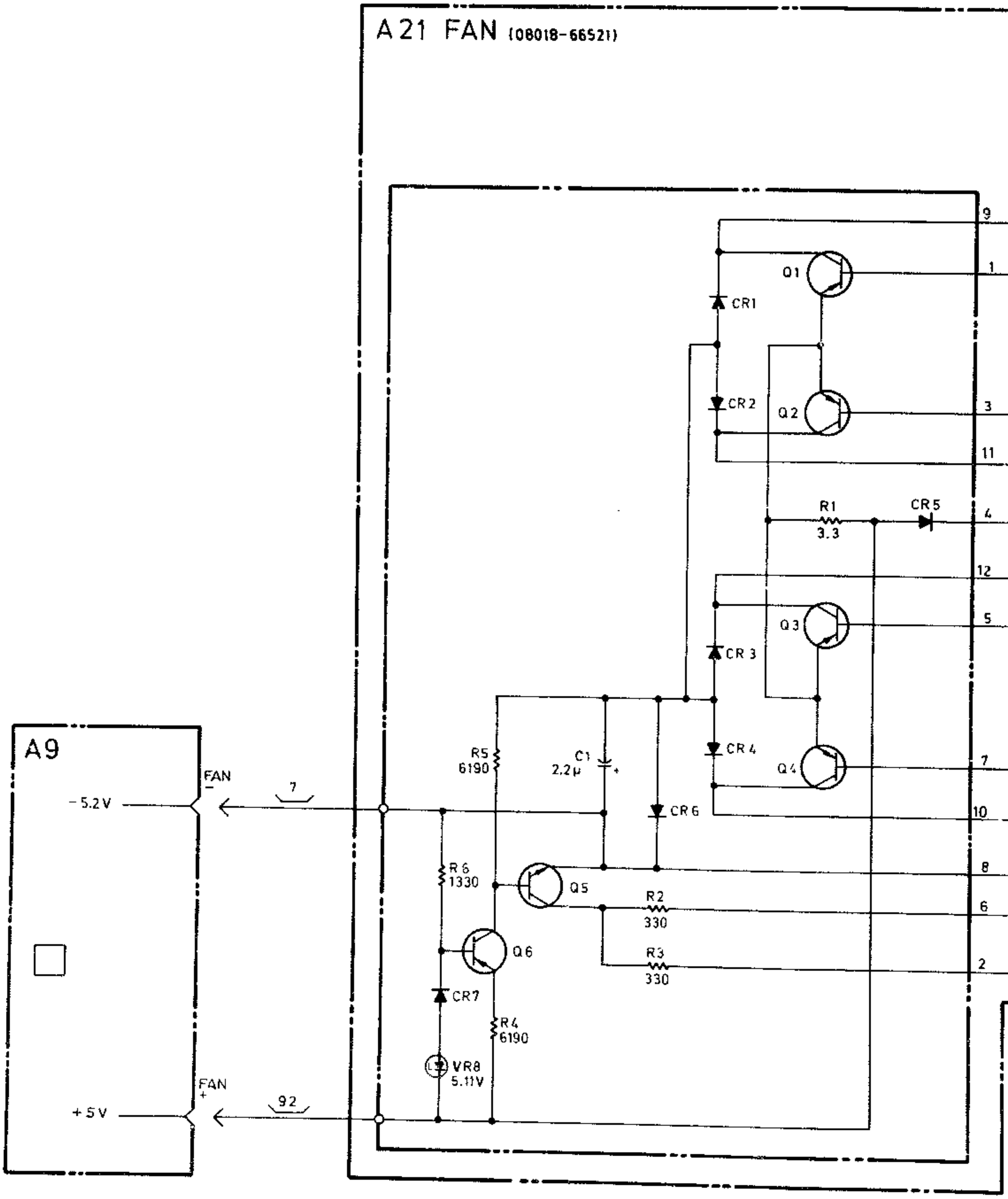


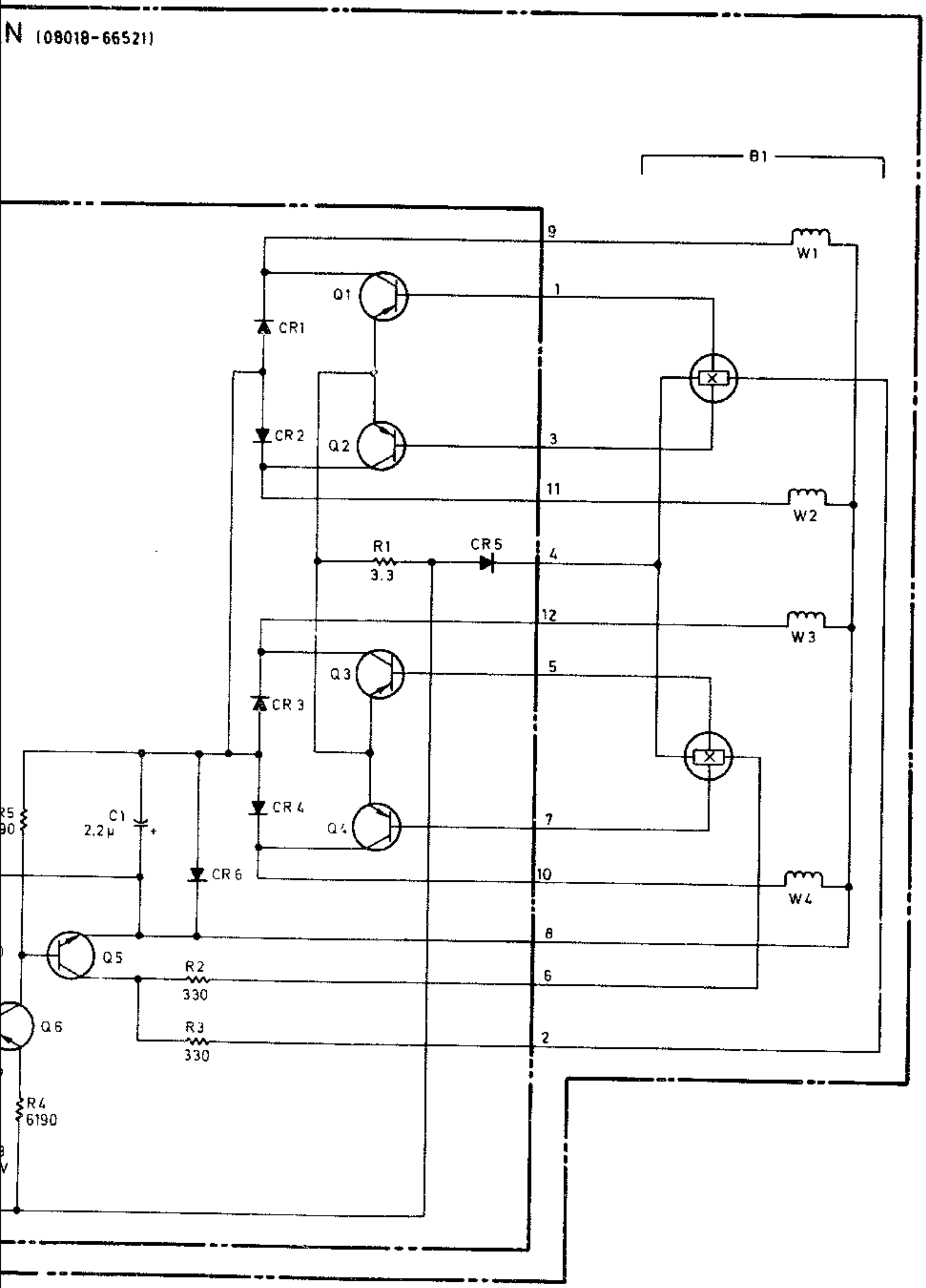
A21 FAN BOARD
08018-66521



MP26 BRACKET, MOTOR

3A


A21 FAN (08018-66521)
A9
-5.2V
FAN
-
+5V
FAN
+
7
92
Q1
Q2
Q3
Q4
Q5
Q6
CR1
CR2
CR3
CR4
CR5
CR6
CR7
R1
3.3
R2
330
R3
330
R4
6190
R5
6190
R6
1330
C1
2.2μ
VR8
5.11V
9
1
3
11
4
12
5
7
10
8
6
2


N (08018-66521)
B1
W1
W2
W3
W4
Q1
Q2
Q3
Q4
Q5
Q6
CR1
CR2
CR3
CR4
CR5
CR6
R1
3.3
R2
330
R3
330
R4
6190
C1
2.2µ
9
1
3
11
4
12
5
7
10
8
6
2

FAN MOTOR