

Errata

Title & Document Type: 6130C Digital Voltage Source Operating and Service Manual

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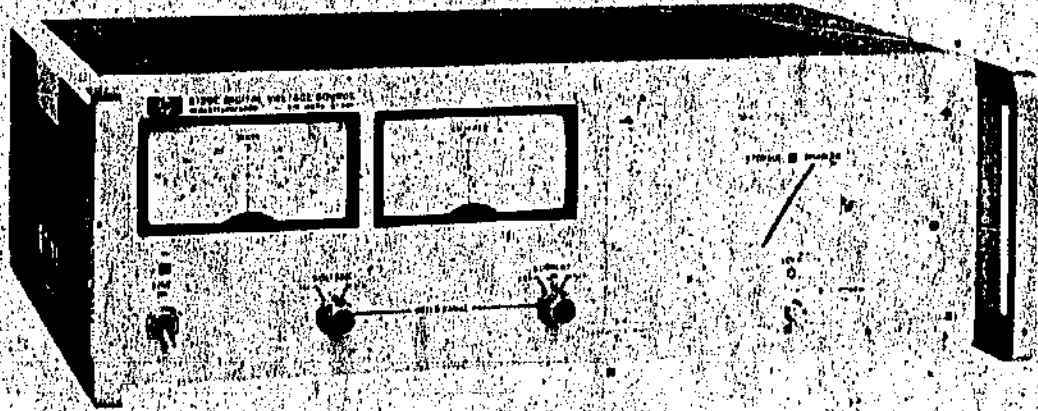
HP 6130C

OPERATING AND SERVICE MANUAL

DIGITAL VOLTAGE SOURCE

MODEL 6130C

BINARY LOGIC



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HP 6130C

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CERTIFICATION

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**DIGITAL VOLTAGE SOURCE
MODEL 6130C
BINARY LOGIC**

**OPERATING AND SERVICE MANUAL
FOR SERIALS 1312A-00101 AND ABOVE**

***For Serials Above 1312A-00101
a change page may be included.**

Hewlett-Packard

HP Part No. 06130-90004

Printed: October, 1973

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SECTION I GENERAL INFORMATION

1-1 DESCRIPTION

1-2 The Digital Voltage Source (DVS) is a complete digital-to-analog link between a computer (or other digital source) and any application requiring a fast accurately settable source of dc or low-frequency ac power.

1-3 A constant voltage/current limiting source, the DVS will furnish full rated output voltage at the maximum rated output current or can be continuously programmed throughout two output voltage ranges. The output is bipolar, and is programmable on either side of, or through, zero without output polarity switches or "notch" effects. In addition, the DVS has low output impedance—the load does not degrade the accuracy specification. The DVS analog output is floating and fully isolated from the digital inputs, thus avoiding ground loops between the output ground and the computer ground.

1-4 The output voltage is controlled by digital data inputs applied to the DVS via a ribbon connector on the rear panel.

1-5 Overcurrent protection is provided by a current "latch" circuit which can be externally or internally programmed to one of eight values between 2% and 100% of the units rated output current. When activated, the current latch circuit turns off the output power amplifier reducing the output current to less than 10mA. The reaction time of the current latch circuit (time between the start of a current overload and turn off of the power amplifier) can be adjusted by adding an external capacitor at the rear terminals. The upper current limit is safeguarded by a separate fixed current limit circuit that prevents the output current from exceeding 110% of the current rating. The computer is continuously informed of possible current overload or current latch conditions by status outputs which are fed back to the user's source.

1-6 For maximum reliability and minimum size and weight, the DVS utilizes all solid state circuitry. Most of the DVS circuitry is contained on five removable plug-in circuit boards, accessible from the front of the unit through an access door.

1-7 Output voltage and current are continuously displayed on two front panel meters. The front

panel METER RANGE switches select the desired voltage and current ranges.

1-8 The DVS also limits sink current (resulting from an active load forcing energy back into the DVS) to a value between 0, 25A and 1.1A as a function of sink voltage magnitude.

1-9 Terminals for High Output, High Sensing, Low Output, Low Sensing, Chassis Ground, Current Latch Delay, Analog Input, and Current Monitor are included on a rear barrier strip. The Low Output terminal may be connected to the ground terminal, or the output may be floated up to 300 volts above ground. The output terminals are automatically shorted if the digital input cable is disconnected or if the input power is removed. The Sensing terminals may be used when the load is remotely located from the DVS in order to avoid degradation in regulation at the load due to voltage drop in the load leads.

1-10 INTERFACING

1-11 Each DVS is pre-interfaced with its controlling computer, or other digital device, by modifying three of the plug-in boards. Five standard sets of these boards (Option J20 and Options 061 through 064) satisfy the majority of interfacing requirements. Each instrument must have either an Option number or a "Special" modification number (e. g., J01, J02, etc.) for identification. The Jxx numbers are used for instruments which do not fit into the standard option category. Detailed descriptions of the different options are included in Appendixes at the rear of each manual while descriptions of special options are included on blue modification sheets in the front of applicable manuals. The option number for each instrument appears on an identification tag at the rear of the unit.

1-12 As supplied from the factory, the DVS can be operated from a 115Vac $\pm 10\%$, 48-440Hz power source. In addition, the DVS can be operated from a 230Vac $\pm 10\%$ single phase input when the unit is equipped with Option 28 (see Paragraph 1-15). This versatility makes the instrument compatible with the European power system.

1-13 SPECIFICATIONS

1-14 Complete specifications for the Digital Volt-

age Source are given in Table 1-1.

1-15 OPTIONS

1-16 As mentioned previously all DVS's are pre-interfaced at the factory. There is no standard instrument; each unit has an option number for identification. There are five "standard" options which satisfy the majority of interfacing requirements. Two of these options (061 and 063) are for BCD instruments while the other three (120, 062, and 064) are for binary units. Detailed coverage of these options is included in Appendixes at the rear of the manual.

Option No.	Description
028	<u>Rewire for 230Vac Input:</u> Consists of reconnecting the input transformers for 230 volt operation and changing the fuse. (Refer to Section II for details.)
120	<u>Binary Interface for 1265IA DVS Program Card:</u> Input/output circuits on P.C. boards A1, A2 and A6 are modified to interface with a computer. (Refer to proper Appendix for details.)
061	<u>BCD Interface for NPN Open Collector Circuits:</u> Input/output circuits on P.C. boards A1, A2 and A6 are modified to interface with a BCD digital source employing "open collector" drivers. (Refer to proper Appendix for details.)
062	<u>Binary Interface for NPN Open Collector Circuits:</u> Input/output circuits on P.C. boards A1, A2, and A6 are modified to interface with a binary source employing "open collector" drivers. (Refer to proper Appendix for details.)
063	<u>BCD Interface for Microcircuit Logic Levels:</u> Input/output circuits on P.C. boards A1, A2, and A6 are modified

to interface with a BCD source employing microcircuit logic of the TTL or DTL family. (Refer to proper Appendix for details.)

064 Binary Interface for Microcircuit Logic Levels: Input/output circuits on P.C. boards A1, A2, and A6 are modified to interface with a binary source employing microcircuit logic of the TTL or DTL family. (Refer to proper Appendix for details.)

1-17 INSTRUMENT IDENTIFICATION

1-18 Hewlett-Packard instruments are identified by a three-part serial number. The first part is the power supply model number. The second part is the serial number prefix, consisting of a number-letter combination denoting the date of a significant design change. The first digits indicate the year (10 = 1970, 11 = 1971, etc.); the second two digits indicate the week; and the letter "A" designates the U.S.A. as the country of manufacture. The third part is the power supply serial number; a different 5-digit sequential number is assigned to each power supply, starting with 00101.

1-19 If the serial number on your instrument does not agree with those on the title page of the manual, Change Sheets supplied with the manual or Manual Backdating Changes define the differences between your instrument and the instrument described by this manual.

1-20 ORDERING ADDITIONAL MANUALS

1-21 One manual is shipped with each power supply. Additional manuals may be purchased from your local Hewlett-Packard field office (see list at rear of this manual for addresses). Specify the model number, serial number prefix, and I/O Part number shown on the title page.

Table 1-1. Specifications

<p>INPUT AND OUTPUT POWER</p> <p><u>Input:</u> 115Vac $\pm 10\%$, 48-440Hz, 1.2A, 100W (Standard) 230Vac $\pm 10\%$, 48-440Hz, 0.6A, 100W (Option 28 only)</p> <p><u>Output:</u> X1 Range: -16.384 to +16.385Vdc @ 1.0A Source X10 Range: -50 to +50Vdc @ 1.0A Source</p> <p><u>Sink Current Compliance:</u> A sink condition results from an active load attempting to force energy back into the DVS. This can appear as current flow into the HI output terminal when the terminal is positive, or current flow out of the terminal when it is negative. In either case the current is limited to a value ranging linearly from 0.25A at 50V to 1.1A at 0V.</p> <p>ACCURACY</p> <p><u>Basic Accuracy:</u> DC voltage accuracy at 23°C $\pm 3^\circ\text{C}$, 115Vac input, no load, following 30 minutes warm-up. X1 Range: 1mV X10 Range: 10mV</p> <p><u>Source Effect (Line Regulation):</u> Change in output voltage for any change in line voltage from 104 to 126Vac (or 208 to 254V ac). X1 Range: 500μV X10 Range: 5mV</p> <p><u>Load Effect (Load Regulation):</u> Change in output voltage for any change in load current within rating. X1 Range: 150μV X10 Range: 500μV</p> <p><u>Temperature Coefficient:</u> Change in output voltage per degree Centigrade change in ambient temperature. X1 Range: 160$\mu\text{V}/^\circ\text{C}$ X10 Range: 800$\mu\text{V}/^\circ\text{C}$</p> <p>PERIODIC AND RANDOM VOLTAGE DEVIATIONS</p> <p><u>Drift (Stability):</u> DC output voltage drift under constant line, load, and ambient temperature for 8 hours after 30 minutes warm-up. X1 Range: 500μV X10 Range: 2.5mV</p> <p><u>PARD (Ripple and Noise):</u> p-p rms (dc to 50MHz), at any line voltage</p>	<p>and under any load condition within rating. X1 Range: 2mV p-p/0.5mV rms X10 Range: 7mV p-p/1.5mV rms</p> <p><u>Load Transient Recovery Time:</u> Time required for output voltage to recover within 0.1% of full range voltage following a full load current change. X1 or X10 Range: 150μsec.</p> <p>SPEED</p> <p><u>Programming Time:</u> Maximum time required for the output voltage to settle within 0.1% of the programmed voltage change after simultaneous receipt of data and gate signals with a resistive load connected across the output terminals. X1 or X10 Range: 300μsec. Voltage range change required 2msec.</p> <p>ANALOG INPUT</p> <p><u>Impedance:</u> 10kΩ $\pm 1\%$ <u>Maximum Input Voltage (Full Range):</u> X1 Range: $\pm 20\text{V}$ X10 Range: $\pm 5.0\text{V}$ <u>Bandwidth (to -3dB Point):</u> Approx. 25kHz. <u>DC Gain:</u> X1 Range: $1 \pm 0.2\%$ X10 Range: $10 \pm 0.2\%$</p> <p><u>Stability (8 hours):</u> X1 Range: Same as stability of input signal + 500μV. X10 Range: Same as stability of input signal + 5mV.</p> <p>CURRENT SENSING</p> <p><u>Impedance:</u> 800Ω <u>Coefficient:</u> 1 Volt/Amp <u>Accuracy:</u> 3% $\pm 2\text{mA}$</p> <p>TEMPERATURE RATINGS</p> <p><u>Operating:</u> 0°C to +55°C. <u>Storage:</u> -40°C to +75°C.</p> <p>COOLING Convection cooling is employed.</p> <p>ACCESSORIES FURNISHED</p> <p>50-Contact Rear Plug, HP Part No. 1251-0086. Rack Mounting Kit, HP Part No. 5060-8740 Plug-In Extender Board, HP Part No. 5060-7948</p> <p>ACCESSORIES AVAILABLE</p> <p>Pocket Programmer, Model 14533B. This accessory permits manual programming of all input functions by switch closures. 3-Foot Extension Cable for Pocket Programming, Model 14534A. This accessory may be used with the Pocket Programmer for maximum convenience.</p>
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SECTION II INSTALLATION

2-1 INITIAL INSPECTION

2-2 Before shipment, this instrument was inspected and found to be free of mechanical and electrical defects. As soon as the instrument is received, proceed as instructed in the following paragraphs.

2-3 MECHANICAL CHECK

2-4 If external damage to the shipping carton is evident, ask the carrier's agent to be present when the instrument is unpacked. Check the instrument for external damage such as broken controls or connectors, and dents or scratches on the panel surfaces. If the instrument is damaged, file a claim with the carrier's agent and notify Hewlett-Packard Sales and Service Office as soon as possible. If the instrument appears undamaged, perform the electrical check given in the following paragraph.

2-5 ELECTRICAL CHECK

2-5 Check the electrical performance of the instrument as soon as possible after receipt. Section V of this manual contains performance check procedures which will verify instrument operation within the specifications stated in Table 1-1. This check is also suitable for incoming quality control inspection. Refer to the inside front cover of the manual for the Certification and Warranty statements.

2-7 REPACKING FOR SHIPMENT

2-8 When shipping the entire instrument, it is recommended that the package designed for the instrument be used. The original packaging material is reusable. If it is not available, contact your local Hewlett-Packard field office to obtain the materials. This office will also furnish the address of the nearest service office to which the instrument can be shipped. Be sure to attach a tag to the instrument specifying the owner, model number, full serial number, and service required, or a brief description of the trouble.

2-9 INSTALLATION DATA

2-10 The instrument is shipped ready for bench operation. Power connections are made through the power cable supplied with the unit. The digi-

tal inputs to control the output voltage, current limit, etc., must be supplied through the data input plug (P1) at the rear of the unit. Section III of this manual provides a complete description of the interfacing requirements.

2-11 LOCATION

2-12 This instrument is convection cooled. Sufficient space should be allotted so that a free flow of air can reach the rear of the instrument when it is in operation. It should be used in an area where the ambient temperature remains between 0°C and +55°C.

2-13 OUTLINE DIAGRAM

2-14 Figure 2-1 shows the outline and dimension information for the instrument which can be used to plan a specific installation.

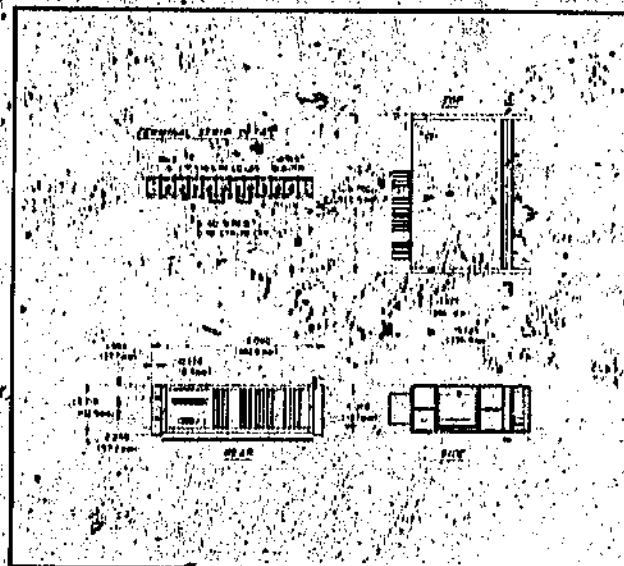


Figure 2-1. Outline Diagram

2-15 RACK MOUNTING

2-16 To mount the unit in a standard rack panel, proceed as follows:

- a. Remove gray plastic trim strips (glued on) at each side of unit by inserting a thin screwdriver

at edge or top of strip and prying gently away from unit.

b. Attach rack ears (furnished with each unit) to side of unit using screws supplied with ears.

c. Mount unit in rack, using standard mounting screws.

2-17 INPUT POWER REQUIREMENTS

2-18 POWER REQUIREMENTS

2-19 This instrument may be operated continuous-

ly from either a nominal 115 volt or 230 volt, 48-440Hz power source. The unit as shipped from the factory is wired for 115 volt operation. The input power required when operated from a 115 volt power source at full load is 1.2 amperes, 100 watts.

2-20 CONNECTIONS FOR 230 VOLT OPERATION (Figure 2-2)

2-21 Normally, the primary windings of input transformers T2 and T3 are connected in parallel for operation from a 115 volt source. To convert the unit to operate from a 230 volt source, the primary windings of each transformer must be connected in series as follows:

a. Unplug line cord and remove top cover.

b. Looking from the rear of unit, locate the 115Vac jumpers between terminals 1, 3, and 2, 4 of transformer T3 (see Figure 2-2).

c. Remove both 115Vac jumpers and solder the 230Vac jumper between terminals 2 and 3 of transformer T3 as shown in Figure 2-2.

d. Replace existing fuse (on rear panel) with 1 ampere, 230V fuse.

2-22 POWER CABLE

2-23 To protect operating personnel, the National Electrical Manufacturers' Association (NEMA) recommends that the instrument panel and cabinet be grounded. This instrument is equipped with a three conductor power cable. The third conductor is the ground conductor and when the cable is plugged into an appropriate receptacle, the instrument is grounded. The offset pin on the power cable's three prong connector is the ground connection.

2-24 To preserve the protection feature when operating the instrument from a two-contact outlet, use a three-prong to two-prong adapter and connect the ground lead on the adapter to ground.

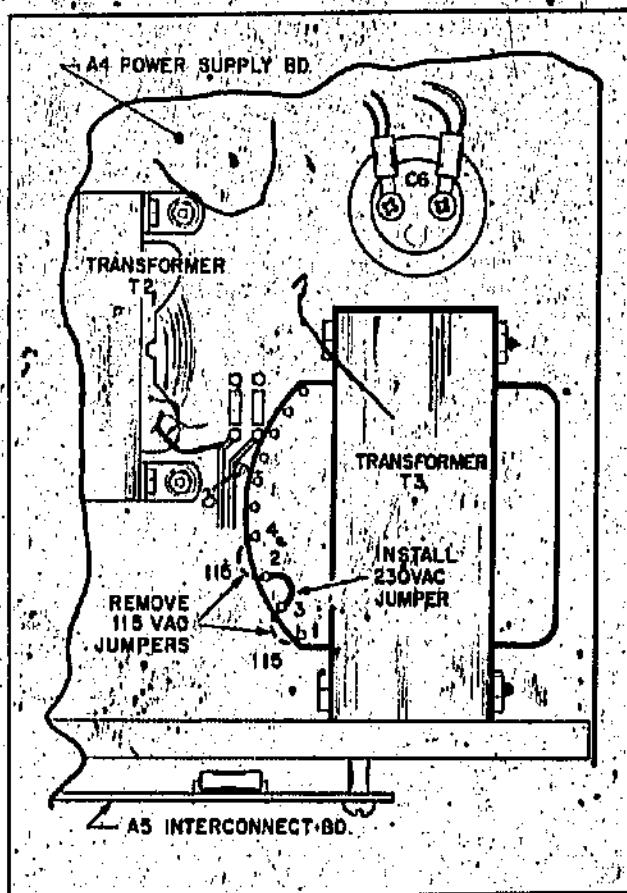


Figure 2-2. Primary Connection for 230Vac Operation

SECTION III OPERATING INSTRUCTIONS

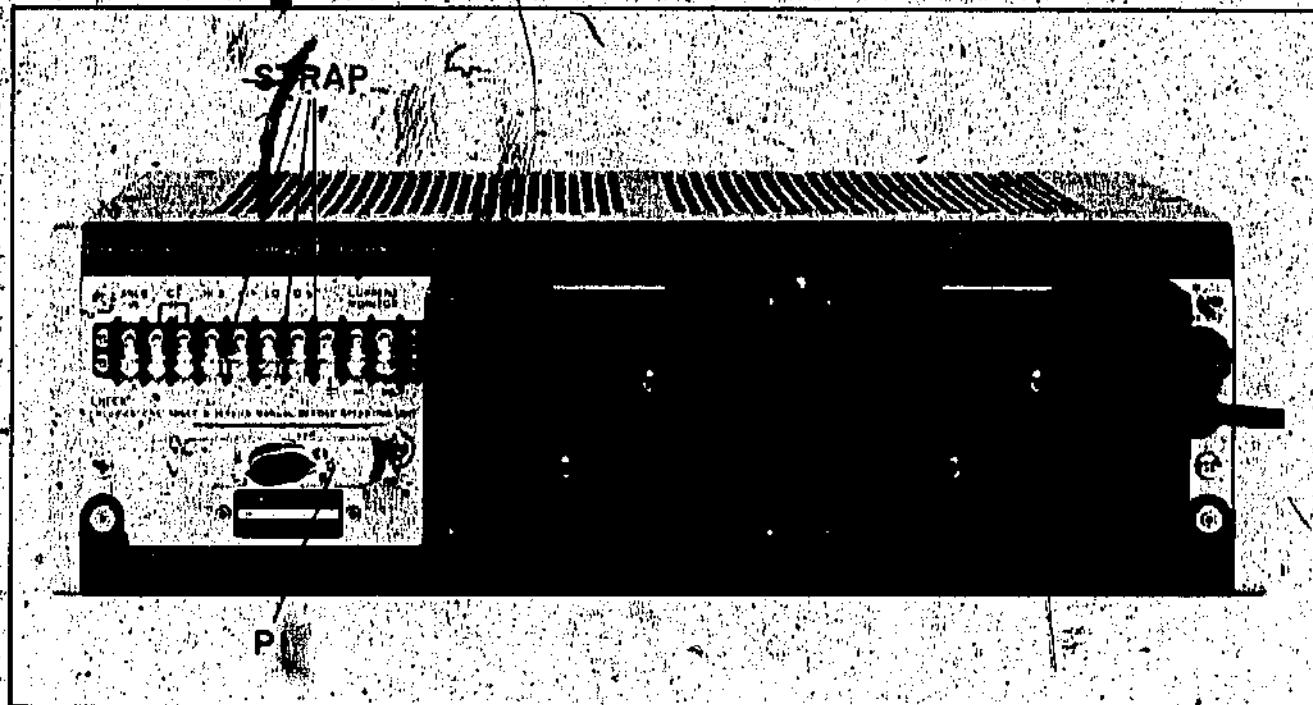


Figure 3-1. Model 6130C, Rear View

3-1 DATA INPUT CONNECTOR

3-2 Before output voltage can be obtained, data input plug P1 must be in place as shown in Figure 3-1. A connection must be made between the cable continuity interlock pin 25 and the computer common (relay A4K1 must be energized; see Figure 7-2, Sheet 3). If this connection is not present or if the input connector is removed, the output terminals will be shorted and the output current will be reduced to less than 10mA. This protects any loads connected to the DVS in the event that the cable is inadvertently disconnected. Note also that the output is shorted when ac power is removed.

3-3 AC INPUT

3-4 To turn on the unit, set the LINE switch (item ① in Figure 3-2) to ON. The pilot light directly above the LINE switch should light. Fuse 1 (2A at 115Vac or 1A at 230Vac) protects the main power supply.

NOTE

Any deflection of the current meter after turn-off does not represent current flowing in the load but rather is current flowing through the internal shorting relay.

3-5 VOLTMETER RANGES

3-6 The VOLTAGE control ② selects either the 50V or 10V range, which corresponds to the upper and lower scales on the voltmeter. The shaded area on the front panel meter face indicates the amount of output voltage that is available (5V) in excess of the normal rated output. Although the instrument will operate in this shaded region without being damaged, it is not guaranteed to meet all of its performance specifications.

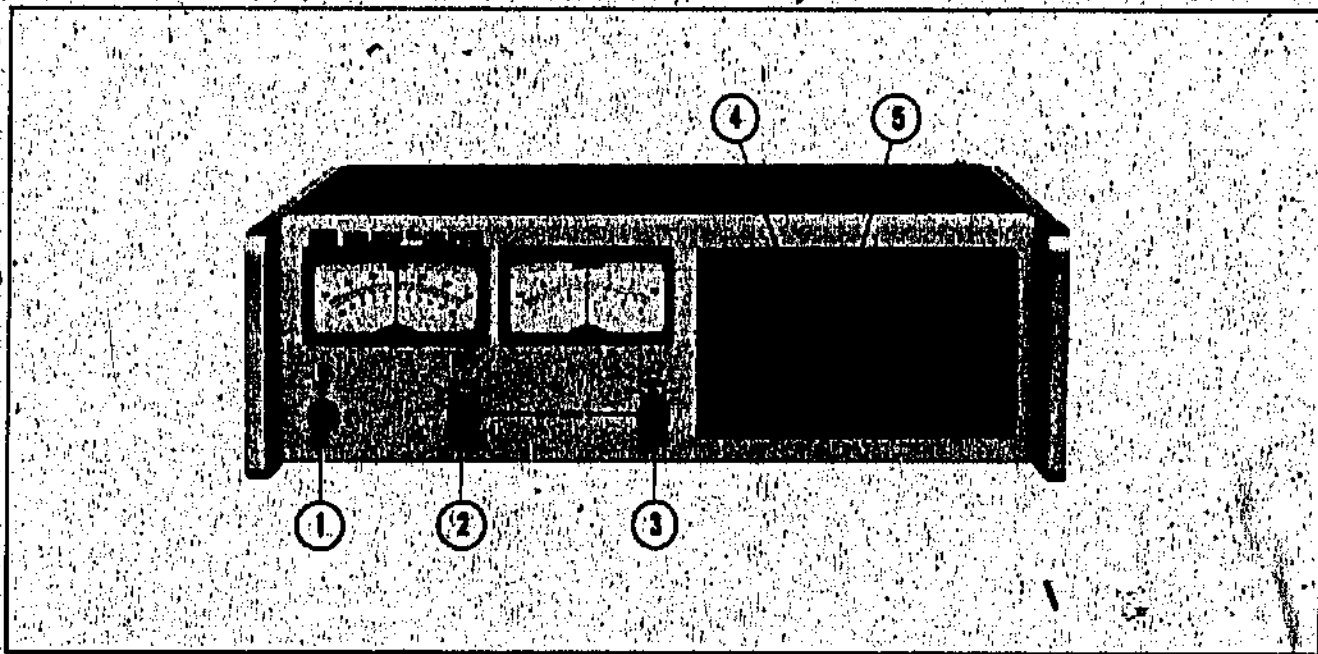


Figure 3-2. Operating Controls and Indicators

3-7 AMMETER RANGES

3-8 The CURRENT control, ③ selects the current range on the front panel meter, 0.12, 0.3, or 1.2A. A 2-amp slo-blo fuse is used as shown on the rear of the unit.

3-9 PROGRAMMING

3-10 Input/output data is connected from a digital computer to P1/J1 on the rear of the DVS as shown in Figure 3-3. A substitute for the computer is HP Pocket Programmer. This accessory plugs into J1 and manually programs all the input to the DVS by switch closures. An extension cable, with connectors on both ends, is also available to mate with J1 and the Programmer plug. Pocket Programmers can be purchased from your local Hewlett-Packard Sales Office.

3-11 The coding, voltage levels, and polarity of the input/output data are selected by the customer to fit his application. Three plug-in boards, A1 Input, A2 Logic, and A6 Control, are modified at the factory to fit these requirements. Most customer requirements can be satisfied by one of the standard options for this instrument. For requirements beyond the scope of the standard options, special modifications are made to the A1, A2, and A6 boards. Either an option number or a special (J) number is assigned to each instrument and is printed on an identification tag on the rear heat sink of the unit. Options are described in Appendixes located at the rear of the manual while special changes are described in an "Instrument

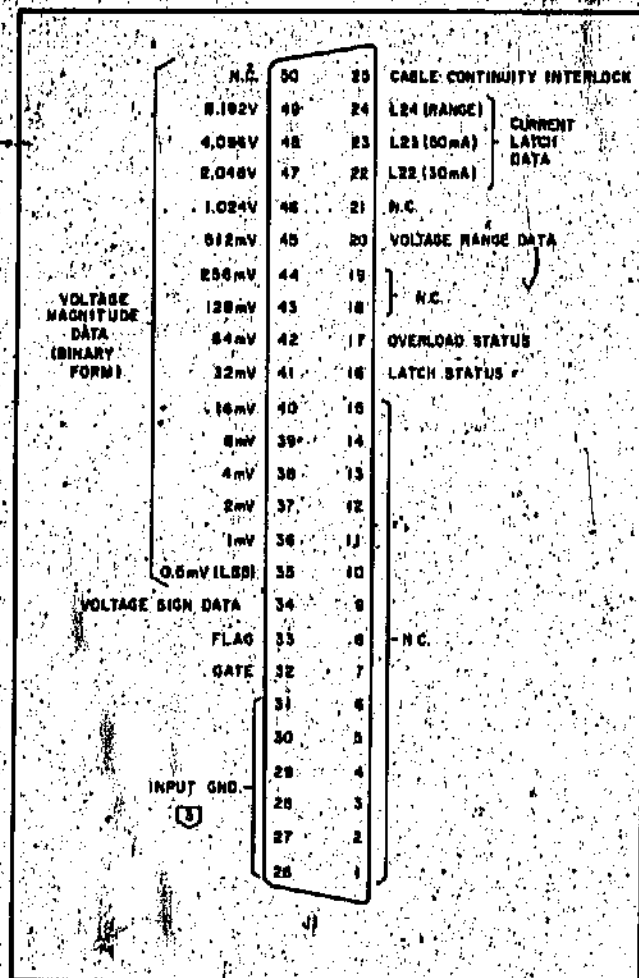


Figure 3-3. Input/Output Data Connector

Modification" sheet which is inserted in the front of any applicable manual.

3-12 The following paragraphs describe the input/output data that is transferred between the computer and the DVS. Sufficient detail to operate the instrument is included; more detailed information is included in Section IV.

3-13 VOLTAGE MAGNITUDE AND VOLTAGE SIGN DATA INPUTS

3-14 Fifteen lines designated according to their positive analog equivalent value in millivolts (0, 5, 1, 2, 4, 8, ..., 4096 and 8192) comprise the voltage magnitude input. This input is received from the computer, or other programming source, in a "computer binary" code. Positive numbers are received in straight binary form while negative numbers are received in negative 2's complement form; that is, the equivalent positive number is complemented (all ones become zeros, all zeros become ones) and a binary one is added to the least significant bit. Notice that because of the nature of negative 2's complementing, it is impossible to program for "negative zero" volts output. The lowest negative number that can be programmed is -0.5mV . Hence, to obtain an output of zero volts, the sign must be positive.

3-15 The voltage magnitude and sign data are stored in the DVS upon the receipt of a gate input from the computer. As shown in Figure 3-4, the voltage magnitude and sign data bits must remain for at least $10\mu\text{sec}$ after the triggering edge of the Gate. Once the $10\mu\text{sec}$ period is expired, the voltage program and sign can be changed to prepare for the next gate. The gate must reset for at least $2\mu\text{sec}$ before starting a new gate, and the time between the leading edges of two consecutive gates must be at least $55\mu\text{sec}$.

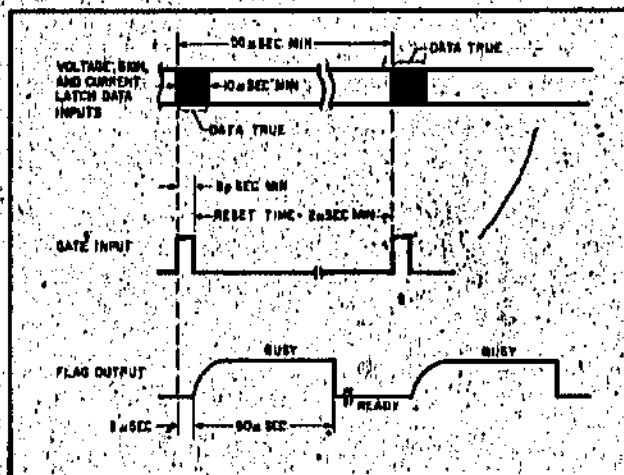


Figure 3-4. Timing Diagram, No Range Change

3-16 Notice that in addition to initiating the storage and processing of voltage and sign data, the Gate also stores the voltage range and current latch data which are discussed in subsequent paragraphs. It should be noted, though, that the trailing edge of the Flag indicates to the computer that the voltage processing is complete and will occur $55\mu\text{sec}$ after the leading edge of the Gate provided the voltage range of the DVS has not been changed. If a voltage range change is programmed, the trailing edge of the Flag is delayed to 2msec from the leading edge of the Gate (refer to Paragraph 3-21).

3-17 STORAGE

3-18 With the STORAGE switch (4) (Figure 3-2) in the STORE position, the voltage, sign, range, and current latch program data are stored when the gate is received from the computer. In the DISABLE position, indicator DB1 (5) lights and the data are processed as soon as they are received.

3-19 Storage can be disabled in cases where a manual programmer is used or where the computer has internal storage for the voltage magnitude and sign data.

3-20 VOLTAGE RANGE

3-21 The voltage range data input from the computer multiplies the voltage magnitude data X1 for the lower range or X10 for the higher range. In the X1 range, the maximum output voltage swing is from -16.384 to $+16.385$ volts. In the X10 range, the output voltage swing is from -50.00 to $+50.00$ volts. The range of the DVS is controlled by the voltage range data bit from the computer which is stored (along with the voltage magnitude, sign) and current latch data) in the DVS when the Gate input is received. As shown in Figure 3-5, the voltage range data bit must remain for at least $10\mu\text{sec}$ after the triggering edge of the gate. Once the $10\mu\text{sec}$ period is expired the voltage range input can be removed. The gate must reset for at least $2\mu\text{sec}$ before starting a new gate, and the time between the leading edges of two consecutive gates must be at least 2msec .

3-22 If a range change is programmed, then, the trailing edge of the Flag sent to the computer is delayed 2msec after the leading edge of the Gate. If a range change is not programmed, the DVS Flag is returned $55\mu\text{sec}$ after the Gate as indicated in Figure 3-4 and discussed in paragraph 3-15.

3-23 Voltage Range Programming. The voltage range bit from the computer has two states, X1 and X10. In the X1 range, the voltage magnitude data input is multiplied by 1 so that the output voltage can be varied (in 0.5mV or greater steps) between 0.000 and $+16.385$ volts (positive sign

bit of 0, 0015, and +16.384 volts (negative sign if 1). At the X10 range, the voltage magnitude data output is multiplied by 10 so that the output voltage can be varied (in 5mV steps or greater) between -50.00 and +50.00 volts.

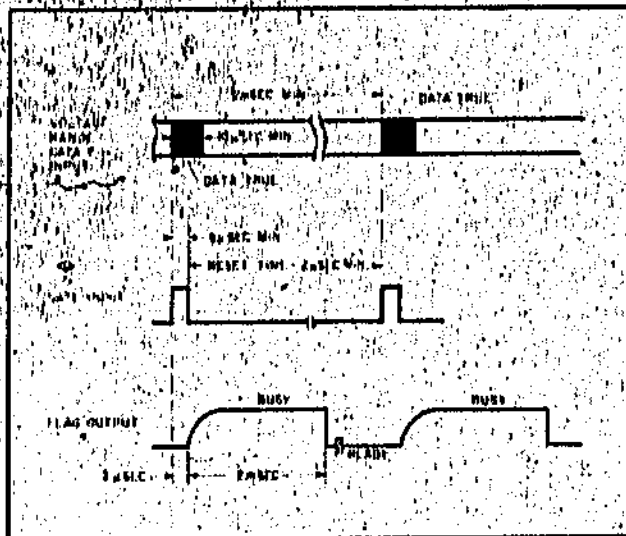


Figure 3-5. Timing Diagram, Range Change

3-24 CURRENT LIMIT

3-26 The DVS provides a maximum (gross) limit and a programmable current limit (referred to as current latch on this unit). Each current limit is controlled independently by a separate circuit. The gross current limit circuit is fixed to activate at approximately 110% of the rated output current (approximately 1.1A). The adjustable current latch circuit can be programmed to 20, 50, 70, 100, 200, 500, 700, or 1000mA. Current latch input data consist of three lines: L22 (30mA), L23 (50mA), and L24 (range, X1 or X10). All three inputs are stored in the DVS when the gate signal is received. As shown in Figure 3-4, the current latch data must remain for at least 10µsec after the triggering edge of the gate. The flag signal is sent to the computer 55µsec after the gate to indicate that current latch processing is complete.

3-26 If the overload condition persists for a certain variable delay period, the current latch circuit is activated and the output current is reduced to from 0 to 10mA, depending on the type of load connected to the unit. The output voltage, under current latch conditions, depends on the programmed output voltage and the type of load. With a full resistive load connected to the unit, the output voltage (and current) are reduced to nearly zero. At no load, the output voltage will correspond to the programmed voltage; up to a maximum of 40

volts. After the load current is reduced or the current latch increased, the next gate that is received will reset the current latch circuit and return the unit to normal operation.

3-27 In addition to the current limits described above, the current limit circuits also protect the DVS from active loads that force energy back into the DVS (sink condition). This can appear as current flow into the III output terminal when the terminal is positive, or current flow out of the terminal when it is negative. Figure 3-6 shows the normal operating locus of the DVS. As shown, the DVS will limit the sink current to a value ranging linearly from 0.25A at 50V to 1.1A at 0V.

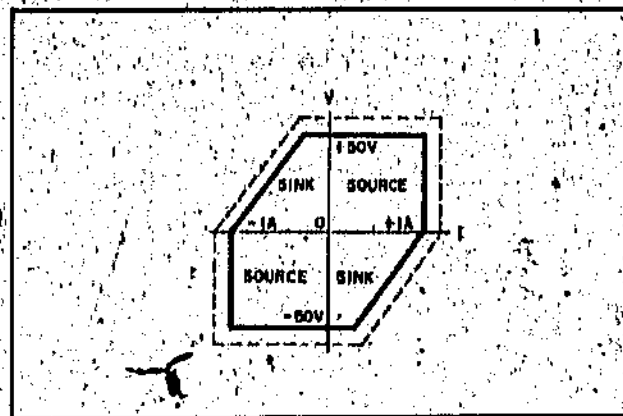


Figure 3-6. 6130C Output Ranges

CAUTION

Externally applied terminal-to-terminal voltage in excess of 55V will damage the DVS.

3-28 Current Latch Programming. The current latch data bits L22 (30mA), L23 (50mA), and L24 (range) from the computer form a 3-bit binary code to program the DVS current latch value. The states of the 30mA and 50mA bits determine the basic value; the state of the range bit multiplies that value by 1 or 10. The following chart illustrates the code for each current latch value in standard option (NPN) units. The three current latch bits provide a maximum of eight possible combinations as shown in the chart. If the pocket programmer is used to program the current latch, refer to the associated manual.

3-29 CURRENT OVERLOAD AND LATCH

3-30 If the output current exceeds the value of the programmed current latch a 10µsec flag signal and the overload status signal are sent to the computer.

NPN CURRENT LATCH CODING

CURRENT LATCH (mA)	L24 (RANGE)	L23 (50mA)	L22 (30mA)
20	HI	HI	HI
50	HI	HI	LO
70	HI	LO	HI
100	HI	LO	LO
200	LO	HI	HI
500	LO	HI	LO
700	LO	LO	HI
1000	LO	LO	LO

HI = more positive voltage
LO = more negative voltage

as shown in Figure 3-7. If the overload condition still exists after a variable delay period, (refer to next paragraph) the unit commences current latch operation and the latch status signal changes state. The current overload status signal switches to the normal state when the current latch mode commences. A second 10- μ sec wide flag signal is produced when current latch begins.

NOTE

For standard Option J20, the two 10 μ sec flag outputs corresponding to the leading and trailing edges of the Overload status output are disabled and not transmitted to the computer.

3-31 Current Latch Delay. Two terminals, C_T , on the rear barrier strip are provided for connection of a capacitor to delay the current latch circuit. Capacitor C_T determines the delay between detection of an over-current condition (current overload status) and the time that current latch begins (the current latch status signal switches to the overload state). Some delay is desirable when driving a capacitive load, since current surges higher than the current latch setting would activate the current latch circuitry. If the C_T terminals are open, a natural delay period of from 3 to 10 μ sec (approximate) will result. If capacitor C_T is utilized, the delay is adjustable between 5 μ sec and 2msec at the rate of approximately 1 μ F per msec.

3-32 The current latch status signal will switch from overload to normal state approximately 10 μ sec after the next gate providing that the overload condition no longer exists. Therefore, to program the DVS out of the current latch condition and back to normal operation, the overload must be removed or the current latch increased; and then a new gate must be issued. The flag will switch to busy 5 μ sec after the gate is received and remain in that state for 50 μ sec.

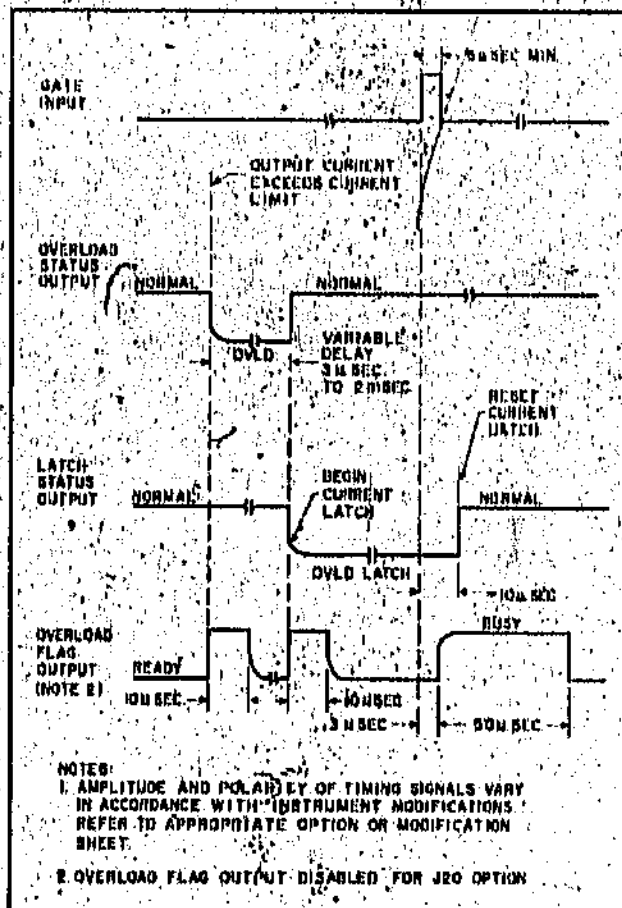


Figure 3-7. Current Latch Overload Timing Diagram

3-33 Current Latch Disable. The current latch circuit within the DVS can be disabled by shorting the C_T terminals at the rear of the unit. Under these conditions, the current limit is governed solely by the gross current limit circuit which fixes the current limit at about 101 amperes. Although the current latch status signal is not generated, the overload status signal is switched to the overload state if the output current exceeds the programmed current latch value. Shorting the C_T terminals is useful during calibration or troubleshooting when it is desirable to keep the unit out of the current latch mode. Ensure that the shorting wire(s) across the C_T terminals is short (less than six inches long). The inductance of long wires could cause the current latch circuit to become activated.

3-34 Current Latch At Turn On. At turn-on, the output terminals are shorted for approximately 0.2 second. This will activate the current latch circuitry reducing the output current accordingly. After the short is removed from the output terminals, a gate input must be received from the computer to reset the latch circuit and return the unit to normal operation.

3-35 CONNECTING THE LOAD

3-36 Low sense (LO, S.) and high sense (HI, B.) should be connected to LO and HI respectively, as shown in Figure 3-1.

3-37 Remote Sensing is used to maintain good regulation at the load and reduce the degradation of regulation which would occur due to the voltage drop in the leads between the power supply and the load. Remote sensing is accomplished by utilizing the strapping pattern shown in Figure 3-8. The power supply should be turned off before changing strapping patterns. The leads from the sensing terminals to the load will carry much less current than the load leads and it is not required that these leads be as heavy as the load leads. However, they should be twisted or shielded to minimize noise pickup. Remote sensing leads longer than 15 feet may have high frequency resonances which can cause the power supply to oscillate. If long leads are anticipated consult your local Hewlett-Packard Sales Engineer for techniques to eliminate oscillation.

3-38 Note that it is desirable to minimize the voltage drop in the load leads and it is recommended that the drop not exceed 1 volt per lead if the power supply is to meet its dc specifications. If a larger drop must be tolerated, please consult an HP Sales Engineer.

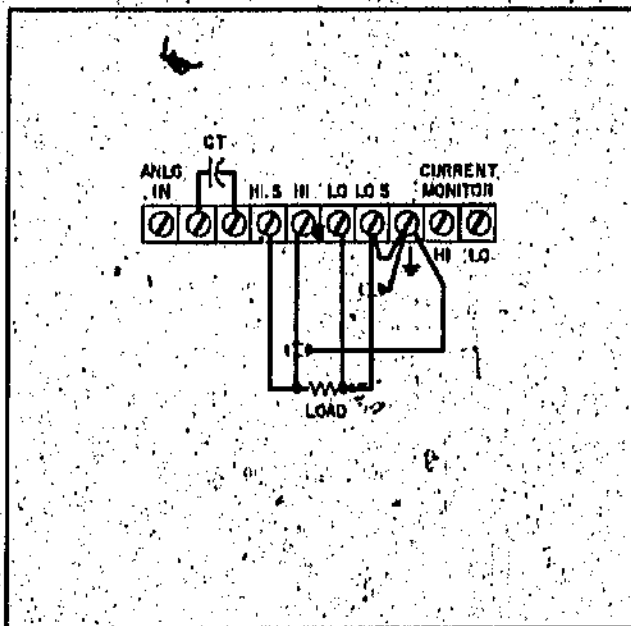


Figure 3-8. Remote Sensing, Strapping Pattern

3-39 Grounding. Proper grounding will greatly reduce output ripple and noise. It is recommended that the LO output terminal be connected to the

GND terminal. The HI output terminal should not be connected to GND during normal operation.

3-40 If the output terminals must be floated at some dc potential, a capacitor (between 0.05 and 0.1 μ F) should be connected between the LO and GND terminals. If the above capacitor is not connected, a common-mode noise signal will be induced in the output leads. Since this noise signal will have an amplitude of approximately 100mV, it is recommended that the above capacitor be utilized.

3-41 CURRENT MONITOR

3-42 The CURRENT MONITOR terminals (Figure 3-8) can be used to monitor the output current of the DVS without affecting the output voltage. To monitor the output current, a DVM is connected across the CURRENT MONITOR HI and LO terminals. The output voltage reading is proportional to the current output in the ratio of 1 volt/1 ampere output current. With a positive output programmed through a resistive load, the LO terminal is positive with respect to the HI terminal. The accuracy of the CURRENT MONITOR reading is $\pm 3\%$. For example, a reading of 250mV indicates that the DVS output current is 250- ± 7.5 mA.

3-43 ANALOG INPUT

3-44 The ANALG IN terminal (Figure 3-8) can be used to program the output of the DVS with an analog input. The analog input signal can be a dc level or a variable signal (a sinewave, for instance). The analog input signal is connected between the ANALG IN and LO S terminals.

3-45 The analog input is summed with the digital voltage magnitude data (after it is converted to its equivalent analog current) at the input to the DVS power amplifier. The result of the summation is used to drive the power amplifier which produces the specified output voltage. Since the power amplifier inverts its input, the analog input voltage must be of opposite polarity with respect to the polarity of the desired output voltage. The power amplifier amplifies the input signal by 1 in the X1 range and by 10 in the X10 range.

CAUTION

To protect the DVS from damage, the combination of digital voltage magnitude data and analog input should not cause the DVS to exceed its rated limits (± 50 Vdc). Further, regardless of the digital voltage input, the analog input in the X1 range should not be greater than ± 20 V nor greater than ± 5.0 V in the X10 range.

3-46 The DVS output voltage can be determined by the following formula: $V_{OUT} = -Range \times Analog\ Input + Digital\ Program\ Voltage$. For example, if a +5.000Vdc output is desired with no digital voltage-program input, a -5.000Vdc input can be applied to the ANLG IN terminal with the DVS set to the X1 range. The equation is: $V_{OUT} = -1 \times (-5.000) + 0 = +5.000Vdc$. This same output, of course, could also be obtained by applying a

-0.500Vdc input with the DVS in the X10 range. Negative DVS output is obtained in a similar manner; that is, by applying a positive analog input at the ANLG IN terminal. The bandwidth of the analog input (measured at the -3dB point) is approximately 25kHz. In other words, the gain of the power amplifier falls off if the analog input frequency exceeds 25kHz with the amplifier approaching unity gain at 100kHz.

SECTION IV PRINCIPLES OF OPERATION

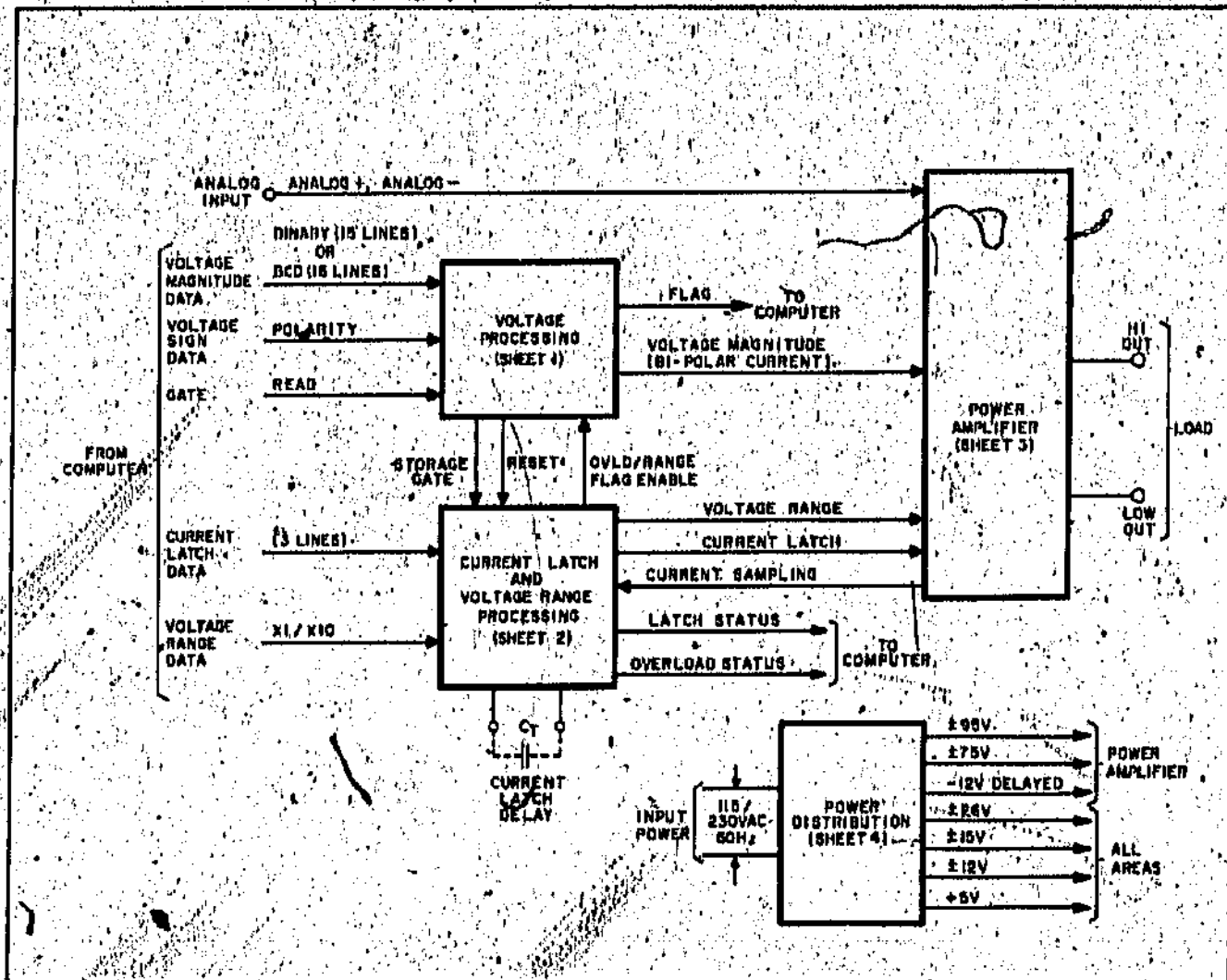


Figure 4-1. Basic Block Diagram.

4-1. INTRODUCTION

4-2 This section contains the principles of operation for the Digital Voltage Source (DVS). The section is divided into three main paragraphs; a basic block diagram discussion, a detailed block diagram discussion, and a detailed circuit analysis. The depth of coverage increases with each level of discussion until, in the detailed circuit analysis, the function of each major component is described using the schematic diagrams of Figure 7-2.

4-3 BASIC BLOCK DIAGRAM DISCUSSION

4-4 Figure 4-1 is a basic block diagram of the DVS showing its four major circuits, together with the principle input/output signals of each circuit. Each major circuit has an associated sheet number for correlation of this diagram with the schematic sheets at the end of the manual.

4-5 The Digital Voltage Source is a digital-to-analog "link" capable of providing an accurately

settable source of dc or low frequency ac power. It provides -16,384 to +16,385 volts (in 0.5mV steps) or -50 to +50 volts (in 5mV steps) at 0 to 1A, from dc to 25kHz. Current limit protection is provided by a current "latch" circuit which can be programmed to activate at one of eight values ranging from 20mA to 1000mA. Back-up protection is provided by a gross current limit circuit which prevents the output current from exceeding 110% (maximum) of the rated output current.

4-6 VOLTAGE PROCESSING

4-7 The voltage processing circuits interface, isolate, store, and convert to analog form the digital input data representing the magnitude and sign of the required output voltage. The input circuits adapt the DVS to the requirements of the driver circuits to be used and provide dc isolation between the computer ground and the DVS output. Integrated circuits store the received data and a digital-to-analog converter translates the stored data to a bi-polar analog current. This bi-polar analog current signal controls the output of the power amplifier.

4-8 The input gate signal initiates timing and storage functions for both the voltage processing and current latch and voltage range processing circuits. The storage function allows the voltage processing circuits to continuously provide a voltage magnitude output without the need for repeated voltage magnitude and sign inputs from the computer. Each time the input gate is received, a storage gate reset signal and a flag are generated. The storage gate signal initiates the storage function within the current latch and voltage range processing circuits. The reset output signal resets the current latch circuit if (1) the circuit is in the latch condition; and (2) if the condition that originally caused the latch has been corrected. The reset signal is ignored if these two conditions have not been satisfied.

4-9 The flag output provides timing information to the computer concerning the status of the voltage processing and current latch and voltage range processing circuits. It is generated in response to the gate input or the overload/range enable inputs from the current latch and voltage range circuits.

4-10 CURRENT LATCH AND VOLTAGE RANGE PROCESSING

4-11 Current latch and voltage range processing circuits interface, isolate, store, and process input digital information to provide the current latch and voltage range output signals to the power amplifier. Input circuits, similar to those used in voltage processing, adapt the DVS to the com-

puter circuits and provide dc isolation. Integrated circuits store the information when the storage gate is received from voltage processing. The stored current latch and voltage range data is then processed by separate circuits (as will be described in subsequent paragraphs).

4-12 Current Latch Processing. The three lines of current latch data are decoded and are used to establish a reference current limit which is compared with a sample of the output current (current sampling input from the power amplifier). If the current sampling input equals, or exceeds, the reference current limit, a current overload status signal is immediately sent to the computer informing it that an overload condition exists. If the overload condition still exists after a variable delay period, the current latch and current latch status output signals are simultaneously generated. The current latch delay period is approximately 3 to 10µsec with the C_T terminals open and with added capacitance can be extended to 2msec. The time delay should be extended for applications involving capacitive loads to prevent surge currents from initiating premature current latch action. When the C_T terminals are shorted, the current latch circuitry is disabled inhibiting the generation of the current latch and latch status output signals. If generated, the current latch output signal turns off the power amplifier so that the output current is reduced to a safe value (less than 10mA). The latch status signal informs the computer of the current latch status of the DVS.

4-13 Whenever a current overload or latch condition occurs, an overload flag enable signal is sent to the voltage processing circuits which, in turn, issues a flag output to the computer.

4-14 Voltage Range Processing. The voltage range data input is stored, and then sent as a voltage range select signal to control the power amplifier range relays. With the relays energized, the voltage program input signal is multiplied by 1 (X1 range). With the relays deenergized, the voltage magnitude is multiplied by 10 (X10 range). Similar to current overload condition, a range flag enable, and then a flag signal is issued whenever a voltage range change occurs.

4-15 POWER AMPLIFIER

4-16 The power amplifier amplifies the bi-polar voltage magnitude input current to provide a bi-polar output voltage across the load connected between the HI and LO output terminals. An external analog input signal can also be applied to the power amplifier. A signal applied to the analog input terminal is summed with the voltage magnitude signal from voltage processing. For this condition, the power amplifier amplifies the sum

of these signals. Shunt feedback is employed to prevent changes in the output voltage without a change in the input signal. Additional feedback networks are used within the amplifier stages for stability purposes.

4-17 As mentioned previously, the amplifier circuits multiply the current input signal by X1 or X10, depending on the status of the voltage range input from the voltage range processing circuit.

4-18 The power amplifier includes a self-contained, gross current limit circuit which is fixed to activate at 110% (maximum) of the rated output current. When activated, the gross current limit circuit limits the conduction of the power amplifier preventing the output current from exceeding the maximum current limit value.

4-19 Additional protection for the load is provided by a circuit which shorts the output of the amplifier whenever input power is interrupted or the input cable from the computer is disconnected.

4-20 POWER DISTRIBUTION

4-21 Power distribution circuits accept 115 volts or 230 volts, single phase, 60Hz input power and provide unregulated dc bias voltage outputs to the three major circuits. Additional regulated bias voltages are generated by reference supplies and voltage regulators in voltage processing and the power amplifier. Overload protection is provided by a fuse in the input circuit. The delayed -12 volt output to the power amplifier provides protection of the output load by keeping the amplifier output shorted until the internal bias supplies within the DVS have stabilized.

4-22 DETAILED BLOCK DIAGRAM DISCUSSION

4-23 Figure 7-1 is a detailed block diagram of the Digital Voltage Source showing each stage, or group of stages, within each of the three major circuits. The major circuits are bracketed by heavy-weight lines and sheet numbers are provided to correlate this drawing with the overall schematics of Figure 7-2. For the sake of simplicity the bias supplies and regulators are not included on Figure 7-1; but are discussed in the detailed circuit analysis.

4-24 The detailed block diagram discussion describes, in block diagram terms, the operation of each major circuit. Details concerning the components inside the many circuit blocks are given in the detailed circuit analysis which also includes information on the internal adjustments and controls. Waveforms and timing diagrams are included throughout to supplement the text. For ease of un-

derstanding, the waveforms are idealized. The waveforms are keyed to various points on Figure 7-1 by means of encircled test point numbers.

4-25 VOLTAGE PROCESSING

4-26 The voltage processing circuits consist of an input board, logic board, and a digital-to-analog converter board. The circuit will be explained functionally based on signal flow from board-to-board. A timing diagram for the voltage processing circuits is included on Figure 7-1.

4-27 Voltage Magnitude Input Data. Incoming voltage magnitude data (TP10) is in "computer binary" form—where positive numbers are received from the computer in straight binary and negative numbers are received in the negative 2's complement code. Negative 2's coding consists of complementing the corresponding positive number (changing all logical zeros to ones and all ones to zeros) and adding binary "1" to the least significant bit. (Examples of positive and negative input numbers will be given later.)

4-28 Input Isolators. Voltage magnitude and voltage sign data input isolators provide the logic interface and dc isolation required between the user's computer and the DVS. Incoming voltage magnitude data is applied first to a resistive voltage divider which establishes voltage levels that can be readily utilized by the DVS. DC isolation is provided by a photo-isolator. The input isolator circuit inverts the polarity of the input data, and, in the case of PNP driver circuit, converts it to signal levels appropriate to the NPN logic circuits of the DVS.

4-29 Gate Input and Timing. The gate input (TP1) initiates storage and other timing functions within the DVS. As described in Section III (Figure 3-4) the leading edge of the gate must be received at least 10µsec before the voltage magnitude (data) and sign bits are terminated.

4-30 The input gate signal is first level-set by a resistive voltage divider and then inverted. If necessary, to ensure that the 3-microsecond delay circuit receives a positive-going input transition. The 3-microsecond delay circuit produces a 3-microsecond negative pulse (TP4) whose trailing edge activates the 50-microsecond delay circuit. The two complementary outputs of the 50-microsecond delay are 50-microsecond pulses delayed from the input gate by 3-microseconds. The 3-microsecond delay ensures that the resulting storage gate occurs after the start of the incoming data pulses. The negative 50-microsecond gate pulse (TP6) serves as the input to the gate pulse isolator while the positive output is the input to

the flag isolator.

4-31 The flag output to the computer (TP16) is produced by an OR gate whose inputs are the 50-microsecond pulse (TP40), a pair of pulses occurring at the beginning and end of a current overload, and a 2-millisecond pulse which occurs during a change in voltage range. Waveforms for the flag output signals may be found in Figures 3-4, 3-5, and 3-7. The isolator for the flag signal output permits the output amplifier/inverter to be biased and configured to interface with the computer's receiver circuit. The trailing edge of the 50-microsecond flag produced by a gate input informs the computer that voltage processing is complete and the unit should be producing the requested output. The gate pulse isolator provides dc isolation. The isolator output (TP7) triggers the gate pulse generator and also resets the current latching flip-flop. The gate pulse generator produces a 2-microsecond positive pulse (TP8) with its leading edge delayed by 3-microseconds from that of the input gate.

4-32 With the storage disable switch in the STORE position, the gate pulse generator output pulse is the input to an OR gate whose output (TP9) is the storage gate for voltage magnitude and voltage sign bits. Putting the storage disable switch in the DISABLE position substitutes a fixed positive voltage for this pulse. This permits the bits to pass directly through the storage flip-flops. The output of the OR gate either gates or disables the current latch and voltage range storage flip-flops in the same manner.

4-33 As the unit is turned on, the initial gate pulse generator produces a storage gate input to the OR gate that assures that the storage flip-flops are in the desired initial state.

4-34 Storage. Having storage capability permits the DVS to provide a continuous output after initial data is no longer present. Fifteen latching flip-flops are provided for the voltage magnitude bits and one for voltage sign storage. A storage gate (TP9) strobes the flip-flops, allowing the magnitude and sign inputs to either set or reset them. If the data source is either NPN positive logic or PNP positive logic, the non-inverting outputs of the voltage storage flip-flops are connected. For negative logic inputs, the inverting outputs are connected. The proper outputs are selected by locating the storage flip-flop packages at appropriate locations on the board. Since the data has already been inverted (complemented) once by the input isolators, the outputs of the flip-flops are low for the bits of the incoming data from the computer that are ones. The polarity of the sign bit

is adapted to the logic of the DVS inputs by means of a jumper at the output of the sign flip-flop. Storage can be disabled by the storage/disable switch on the logic board, in which case the outputs of the storage flip-flops follow the data inputs continuously. Voltage and sign data from storage is applied to the digital-to-analog converter.

4-35 Digital-To-Analog Converter. The digital-to-analog converter converts the digital data to either a positive polarity analog current (for negative voltage magnitude inputs) or a negative polarity analog current (for positive voltage magnitude inputs). The latter is accomplished by a negative reference current applied to the converter by the polarity offset switch whenever the input is positive. The magnitude of the D/A converter output current varies between plus and minus 1.6384mA according to the value of the incoming voltage and sign data.

4-36 The D/A converter contains a series of switches (transistors) which are activated by the input data bits from storage. These switches then action a resistive ladder network which produces an output current (in milliamperes) which is proportional to the numerical value of the input data. The combined output of the ladder network and the polarity offset switch make up the voltage magnitude signal. This signal is applied to the power amplifier where it is summed with the current produced by the external analog input, if any. The algebraic sum of these currents is inverted by the power amplifier and appears at the output terminals as the programmed output voltage.

4-37 Polarity Offset Switch and -16.384V

Reference. For input data bearing a negative sign, the polarity offset switch is held off by the sign input from storage and has no effect on the operation of the D/A converter. Under those conditions, the D/A converter supplies a positive output current which is proportional to the applied binary data. For positive input data, the sign input turns on the polarity offset switch and a negative reference current of 1.6384mA is applied to the D/A converter from the -16.384V reference source. The negative reference current is then summed (within the D/A converter) with a positive current which is numerically equivalent to the complemented value of the original input data. The resultant output then is a negative analog current which has been restored to the original numerical value of the positive input data (prior to complementing) by the addition of the -1.6384mA reference current.

4-38 To better understand the processes which take place within the voltage processing circuits, refer to Figure 4-2. With +4 volts programmed

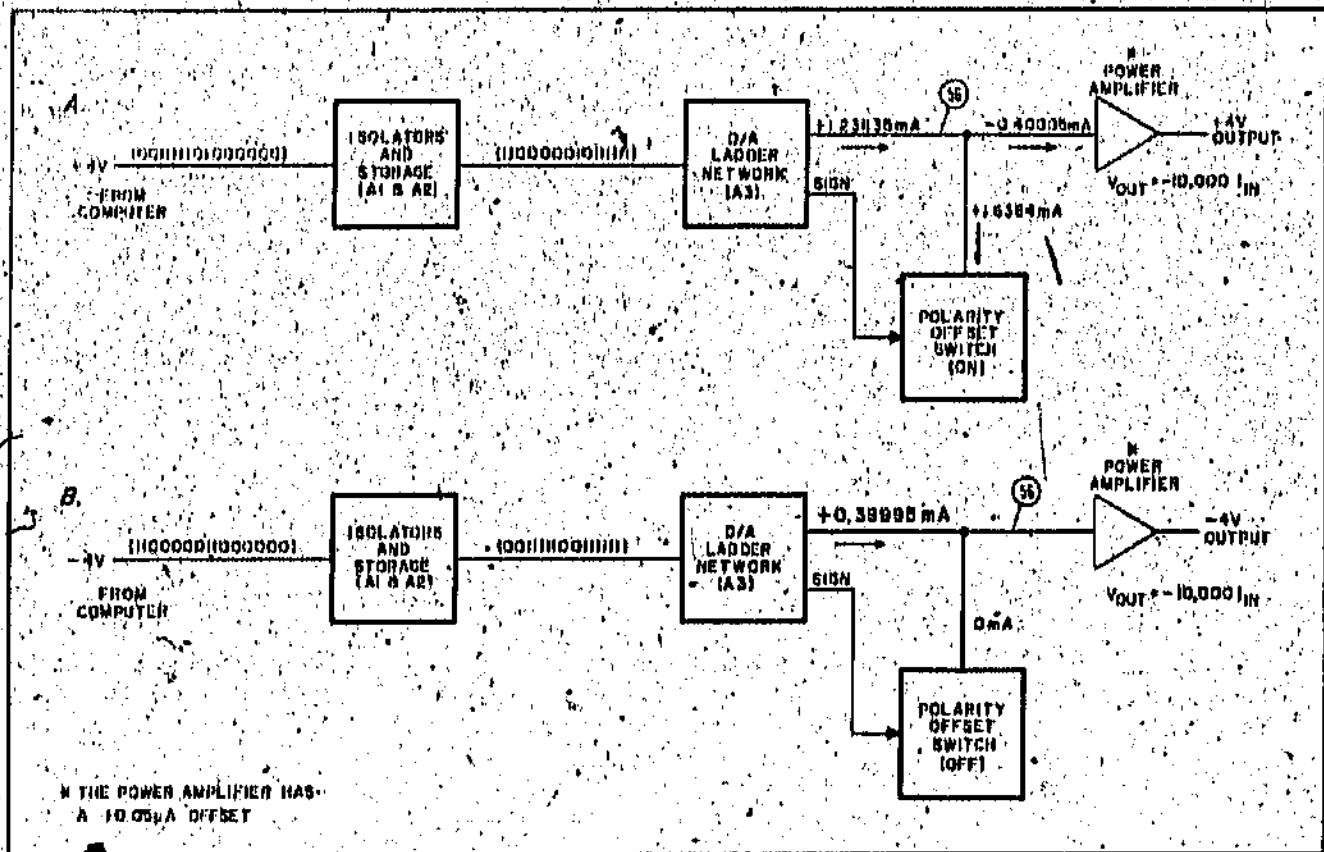


Figure 4-2. Voltage Processing Circuits, Simplified Schematic

into the DVS, the isolators/storage circuits invert the signal which is then changed into a programming current, the result of which is 1.23835mA flowing into TP56 on the D/A Board (A3). The polarity offset is turned on by the positive sign program bit. This draws a current of 1.6384mA from TP56 leaving -0.40005mA to be amplified and inverted by the amplifier section; the result of this will be +4 volts at the output terminals (the amplifier section has a +0.05µA offset).

4-39 If -4 volts (negative 2's complement) were programmed into the Instrument (Figure 4-2B), again the isolators/storage circuits would invert the signal and the ladder network converts the resultant signal into a programming current, the value of which is +.39995mA. The polarity offset switch is turned off by the negative sign program input, thus no current is drawn from TP56. The +.39995mA is amplified and inverted by the power amplifier and the result of this will be -4 volts at the output terminal (again, the power amplifier has a +0.05µA offset).

4-40 POWER AMPLIFIER

4-41 The precision power amplifier consists basically of three major stages; a feedback differential amplifier, coupling amplifier, and power amplifier. Negative feedback is employed, from output to input, creating a near zero-impedance summing junction at the input of the feedback differential amplifier. The amplifier provides an output of -1 volt for every 100µA of input current ($E_{OUT} = -10,000 \times I_{IN}$) in the X1 range or -10 volts for every 100µA of input current ($E_{OUT} = -100,000 \times I_{IN}$) in the X10 range. Hence, in the X1 range, the D/A converter supplies its maximum input current of approximately ±1638.4 microamperes to obtain a ±16.384 volt output. For the X10 range, however, the D/A converter need provide only ±500µA to attain the maximum rated output of ±50 volts. If a number larger than 50 is programmed in the X10 range, the additional D/A input current has little effect on the output because the output of the amplifier is internally limited to approximately (110%) 55 volts.

4-42 Feedback Differential Amplifier. This circuit amplifies and inverts the D/A output and/or analog input signal before applying it to the coupling amplifier. It provides most of the voltage gain of the overall amplifier. Negative feedback is employed with an equalizing network which shapes the high frequency response for stability purposes.

4-43 Voltage Range. A range input from the voltage range processing circuits controls the operation of the range relays which, in turn, determine the impedance of both the equalizing and main feedback networks. In the X1 range, the relays are energized reducing the impedance of the feedback networks and thus increasing the amount of negative feedback through both networks. In the X1 range the overall amplification is multiplied by a factor of 1. In the X10 range, the relays are deenergized, multiplying the amplification by 10.

4-44 Coupling Amplifier. This inverting stage couples the input stage of the overall amplifier to the power amplifier stages which are at a much higher power level. The voltage and current gain of the coupling amplifier is minimal.

4-45 Power Amplifier. The power amplifier stage furnishes most of the current gain of the overall amplifier. The output stage is a class AB, push-pull complementary connected amplifier which produces the positive or negative output voltage. The output, at the high sense terminal, is fed back to the input of the overall amplifier resulting in a constant output voltage which is independent of load variations.

4-46 Current Latch Input. The current latch signal is received from the latch processing circuits if the preselected current latch value is exceeded. An isolating oscillator first isolates the power amplifier from the current latch circuit. The isolator output then activates the current latch switch which turns off the power amplifier.

4-47 Under current latch conditions, the non-conducting power amplifier presents an impedance of approximately 20K Ω in series with the high output terminal. The output current is limited to between 0 and approximately 10mA, depending on the programmed output voltage and the type of load.

4-48 Gross Current Limit. The positive and negative gross current limit comparators provide additional current limit protection. They are fixed to operate at the maximum current limit of approximately $\pm 1.1A$ providing protection for the DVS and the load during the variable current latch delay period or in the event of failures in the current latch circuit.

4-49 The comparators each monitor the voltage

drop across the current sampling resistor. Since the IR drop across the sampling resistance varies in proportion to the output current, both comparators effectively monitor the output current of the DVS. The use of two comparators allows sampling of output current flowing in either direction with the negative gross current limit comparator monitoring negative output currents, and the positive comparator monitoring positive output errors. For nominal source currents (below the 1.1A threshold) the comparators are biased below cutoff and do not influence amplifier operation. However, if the gross current limit threshold is exceeded, the appropriate comparator conducts sending a gross current limit signal to the coupling amplifier. This signal turns down the coupling amplifier, and hence the power amplifier, preventing the output current from exceeding the maximum current limit. For sink currents, the trip point is reduced.

4-50 Disconnect Interlock. A disconnect interlock relay provides load protection by shorting the output of the DVS whenever the computer cable is disconnected or source power is interrupted. Under these conditions, the relay is deenergized (as shown on Figure 7-1) and contacts of the relay short the output terminals. The output is disconnected at turn-on (for approximately 0.2 seconds) and turn-off of the unit which protects the load from possible transients during these times. For normal operating conditions, the relay is energized removing the short between the output terminals, and connecting the interlock signal to the current latch and voltage processing circuits.

4-51 Metering Circuits. The metering circuits provide continuous indications of output voltage and current on the front panel meters. The meters operate in conjunction with front panel range switches and appropriate resistive voltage dividers to permit voltage display in one of two ranges and current indications in one of three ranges.

4-52 CURRENT LATCH AND VOLTAGE RANGE PROCESSING

4-53 These circuits are located on the control board A6. They consist of input isolating circuits, storage, decoding, current sampling and current overload circuits. The circuits will be described functionally based on signal flow from input to output.

4-54 Input Data. The current latch data input from the computer consists of a three bit binary code which is shown in Section III of this manual. This code establishes the point at which the DVS will current latch. The voltage range data input is a single binary bit which determines the voltage range, X1 or X10;

4-55 Input Isolators. Four input isolator circuits, identical to the voltage magnitude input isolators described above, are utilized. They provide the logic interface and dc isolation for the current latch and voltage range data signals from the computer.

4-56 Storage and Storage Disable. In store mode, the three bits of current latch data (TP74) are stored in flip-flops along with the one bit of voltage range data (TP76). These storage flip-flops are enabled by the storage gate and are identical to the ones used in the voltage processing storage circuit. If the storage disable switch in the voltage processing circuit is in the DISABLE position, these flip-flops as well as those in voltage processing are disabled and pass data directly through without storing it. The three current latch data output lines from storage (TP75) are applied to the current latch decoder and the voltage range storage output (TP73) to the range pulse generator.

4-57 Current Latch Decoder. The current latch decoder generates a reference voltage for each of the eight current latch bit combinations. As just mentioned, the current latch bits are received from storage. The incoming bits are first converted to an analog reference current which is then used to develop the negative reference voltage. This voltage is fed directly to the negative current comparator and to the negative reference inverter which provides an equal amplitude, opposite polarity reference voltage to the positive current comparator.

4-58 Current Comparators. The positive and negative current comparators compare a sample of the output current (voltage drop across the current sampling resistance) with the negative or positive reference. If the IR drop across the sampling resistance equals, or exceeds, the reference voltage, an overload signal (TP17—Figure 4-3) is generated. The polarity of the output current determines which of the comparators is activated. The overload signal is fed both to the current overload circuits (isolator and overload flag generator) and the current latch circuit (variable delay). Once the unit switches to the current latch mode, the output current is reduced to under 10mA and the current overload signal at TP17 reverts to its normal state.

4-59 Current Overload Circuits. The current overload circuits comprise an isolator, output amplifier, and overload flag generator. The isolator, a photo isolator of the type used throughout the DVS, provides dc isolation between the computer and the DVS. The output amplifier interfaces the DVS overload circuits with the computer receiver circuits by providing an overloaded status signal (TP25) of the proper magnitude and

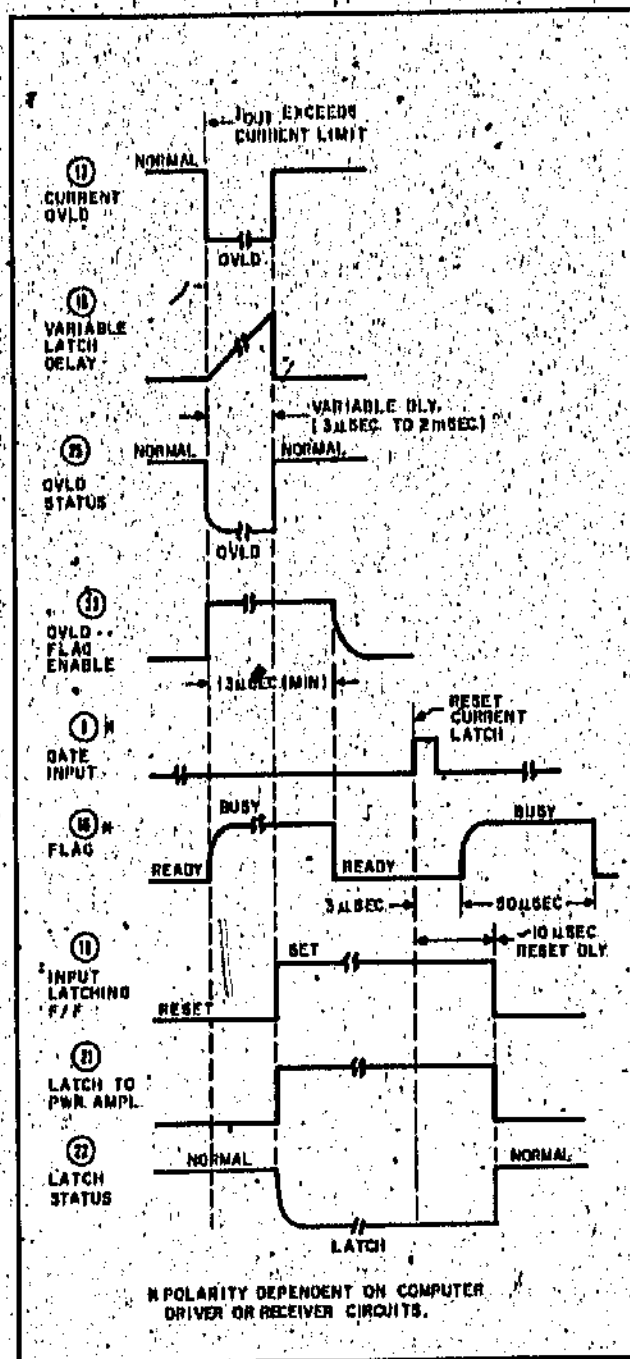


Figure 4-3. Current Overload and Latch Circuits, Timing Diagram.

polarity.

4-60 The overload flag generator provides a 10μsec wide flag enable output signal (TP33) at both the leading and trailing edges of the current overload signal at TP17. The first trip signal indicates the start of an overload while the second denotes that current latch has occurred. If the variable delay period is less than 10μsec, note that the trip signals at TP33 will overlap and

appear as one signal. Since the minimum latch delay is approximately 3µsec, the minimum trip signal width is 13µsec. The overload flag trip signal are OR'ed with the voltage range flag signal and then applied through a photo-isolator and an output amplifier to the voltage processing circuits. This signal (overload/range flag enable) is applied to an OR circuit in the voltage processing circuits which in turn generates the flag signal which is applied to the computer through another photo-isolator and an output amplifier/inverter circuit.

4-61 Current Latch Circuits. These circuits are composed of a variable delay, level detector, latching flip-flop, reset amplifier, isolator, and output amplifier. If a current overload condition persists for a certain preset delay period, these circuits generate a current latch signal. The current latch signal ultimately biases the power amplifier to cut-off, or near cutoff, limiting the output current to less than 10mA. A current latch indicator signal is also generated if a current latch condition occurs.

4-62 The variable delay circuit delays the fall time of the current overload input (TP17). The degree by which the leading edge of this signal is retarded, determines the current latch delay period. The variable delay circuit operates in conjunction with the C_T terminals on the rear of the unit. As mentioned previously, the condition of these C_T terminals determines the current latch delay. With the C_T terminals open, a natural delay period of from 3µsec to 10µsec results. If the user connects a capacitor across the C_T terminals, the current latch delay period can be extended from 5µsec to 2msec at the rate of approximately 1µF per msec. The user can also disable the current latch circuits by shorting the C_T terminals. This disables the variable delay circuit preventing the generation of the current latch signals to the power amplifier and computer. The user could employ this method during testing or troubleshooting when the unit is "off line", or in any case where programmable latching is not desired.

4-63 When the input at TP18 (Figure 4-3) becomes sufficiently positive the level detector (a Schmitt trigger) is activated. The positive going output (TP19) sets the latching flip-flop which, in turn, provides a current latch signal (TP21) to the power amplifier and a latch status signal (TP22) to the computer via an isolator and output amplifier. Similar to the other output circuits in the DVS, this amplifier issues a latch status output signal which is of the polarity and amplitude necessary to interface with the computer receiver circuits.

4-64 The latching flip-flop remains set until approximately 10µsec after the next gate input (TP1) is received from the computer. The leading edge

of the 50µsec delayed signal (TP7) is amplified and used to reset the flip-flop. Notice that if the current overload still exists after the latch is reset, the entire current overload and current latch process is repeated and the unit will again revert to the current latch state.

4-65 Voltage Range. The voltage range circuits consist of a range pulse generator and a 2msec delay circuit. The voltage range, similar to the current latch, is established by the voltage range data bit from the computer. The range pulse generator provides two outputs; one for the range relays in the power amplifier and the other for the generation of a voltage range flag signal to the computer. If the input voltage range bit calls for the X1 range, the range pulse generator connects a ② common to the power amplifier range relays to energize them. In the X10 range, the range relay lead is open and the relays are deenergized. The range pulse generator also provides a negative output pulse for each positive or negative transition of the voltage range input. The positive going output triggers a 2msec delay circuit which provides the voltage range flag signal. This signal is OR'ed with the overload flag signal and applied to the voltage processing circuits through a photo-isolator and an output amplifier. The overload/range flag enable output signal drives the flag OR circuit in the voltage processing circuits. An example of a voltage range flag is shown on Figure 3-5. The 2msec delay period allows time for operation of the range relays and for processing of the voltage range input bit.

4-66 DETAILED CIRCUIT ANALYSIS

4-67 VOLTAGE PROCESSING (See Figure 7-2, Sheet 1)

4-68 Input Isolator Circuits. The input isolator circuits (A1-A15) for the fifteen voltage data bits and for the sign bit (A17) are all identical. They employ light-emitting-diode/phototransistor isolators to eliminate dc paths between the computer and the DVS output. A biased attenuator network (R1, R2, and R3) makes it possible, by selecting appropriate values, to adapt to any of the three standard binary interface options, or, through resistor choice and/or resistor bias polarity, to adapt to other driver circuits as required, whether NPN or PNP. The logic convention of the source may either be positive true or negative true (See Figure 4-4). The voltage levels and circuit details for the inputs (and outputs) of instruments having any of the standard options are given in the appropriate Option Appendix in the back of this manual. Interface information for other instruments is given on the Instrument Modification Sheet included with the instrument.

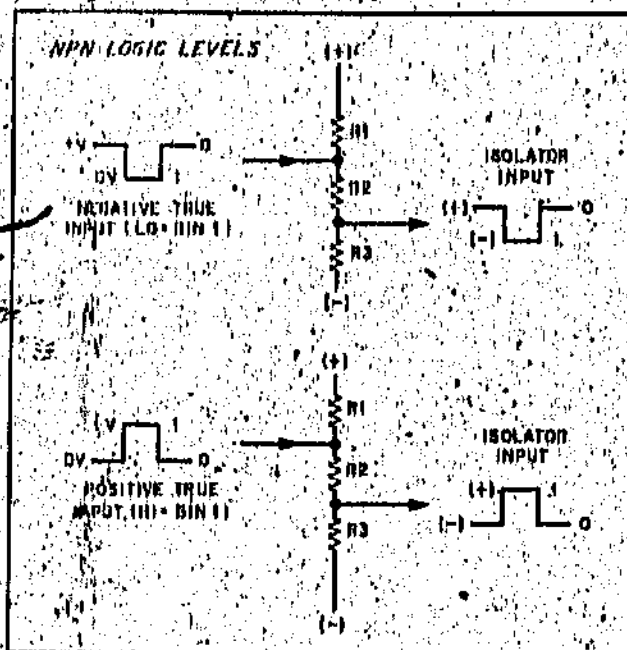


Figure 4-4. Input Voltage Divider Networks

4-69. When the input (TP10) is at its more positive level, Q1 is turned on and energizes the LED in photo-isolator assembly Z1. The photons emitted by the diode cause the phototransistor to conduct, turning on Q2 to apply a low to the data input (TP13) of the storage flip-flop for that data bit. CR1 and R5 form a low impedance load for the photo-transistor to minimize its switching time. A more negative level from the computer produces a high input to the flip-flop. Note that a signal level inversion occurs between the isolator input and output.

4-70. Storage. When a high level is present at the clock inputs of the storage circuits, the level present at the data inputs appears at the Q outputs and the complement of that data at the \bar{Q} outputs. Whatever data is present when the clock input becomes low is stored in the flip-flops and continues to appear at the outputs until the next high clock input occurs. In STORAGE DISABLE mode, the clock input remains high. The logic board has two sets of four sockets for these IC packages. One set is designated Z1 through Z4 and connects the inverting (Q) outputs. The other, Z9 through Z12, connects the non-inverting (Q) outputs. The proper choice of sockets for these IC's depends on the interface requirements of the DVS and whether an inversion of the voltage magnitude bits is needed. The fifteen voltage magnitude outputs from storage to the D/A converter must be low for those bits that are true. The voltage sign output from storage must be low for

a positive output voltage and high for a negative one. Since one inversion occurs at the input isolators, negative true voltage magnitude inputs from the computer require the use of the inverting Z1 through Z4 sockets and positive true inputs require the non-inverting Z9 through Z12 sockets to be used. The proper polarity of the sign bit is obtained by positioning Jumper W1 in the B position for positive = HI inputs and the A position if the input is positive = LO.

4-71. Gate Input and Timing. In instruments equipped with one of the standard options, the gate input from the computer (TP1) is a negative-going transition. A biased attenuator network (R1, R2, and R3) identical to those of the voltage and sign bit inputs adapts the gate input to the interface requirements of the driver circuit. Inverter Q2 provides the positive-going transition needed at the input (TP3) of one-shot multivibrator Z3, which has a Schmitt trigger input sensitive to positive levels. For special modifications, an additional inverting stage that is normally jumpered out may be added ahead of Q2 to accommodate a positive-going input gate. The 3-microsecond duration of the negative pulse at the output of Z3 (TP4) is determined by the values of R7 and C5. The trailing edge of the negative 3-microsecond pulse triggers another one-shot multivibrator identical to the first except that its timing components, R8 and C6, cause it to produce an output pulse 50-microseconds long. Multivibrator Z4 produces a negative 50-microsecond pulse at its Q output (TP6) and a positive 50-microsecond pulses at its \bar{Q} output (TP40). Both of these pulses start 3-microseconds after the start of the incoming gate. The negative output (TP6) drives the light-emitting diode of the gate pulse isolator circuit. This isolator circuit, similar to those used for the voltage magnitude inputs lines, produces a negative output pulse (TP7). This pulse is inverted by part of A225 in order to obtain the positive-going transition (TP43) needed to drive another one-shot multivibrator. A226-A226 is identical A123 and A124 except that its timing components are chosen for a 2-microsecond output pulse (TP8).

4-72. If the storage disable switch is in the STORAGE position, this 2-microsecond positive pulse is applied to one of the inputs of the OR gate composed of Q1, Q2, and Q3. The output of the OR gate (TP9) is a positive 2-microsecond storage gate to the clock inputs of the voltage magnitude and sign flip-flops. This output is also inverted by another section of A225 and sent to the current latch and voltage range processing circuits to control the storage flip-flops there. The other input of the OR gate is connected to an r-c

differentiating network that produces a 20-milli-second pulse when the instrument is energized. This pulse assures that the A2 and A6 storage flip-flops are in the desired initial state.

4-73 If the storage disable switch is in the STORAGE DISABLE position, an input gate does not produce a storage gate. The pulse input to the OR gate is disconnected by the switch and Q1 is saturated by the current through R6. The continuously high output from Q2 keeps all of the storage flip-flops enabled so that data inputs are reflected at the flip-flop outputs continuously. Placing the switch in STORAGE DISABLE also lights the STORAGE DISABLE lamp.

4-74 The other output of multivibrator A124, the 50-microsecond positive pulse (TP40) mentioned above, is one of two input signals to an OR gate consisting of A10R1 and A6CR20. The other input will be discussed under current latch and voltage range processing. The output of this OR gate (TP31) feeds the flag isolator, which is similar to the input isolator described above. In this instance, the isolator is not used to isolate the computer from the D/A output; since the input and output are both referenced to common

(3). Here it is used to make it possible to shift the dc level of the output stage so that it can interface with either an NPN or a PNP receiver circuit.

4-75 Following Q5 of the flag isolator are two optional amplifier/inverter stages, Q6 and Q7. The standard options either include an NPN Q6 stage as an inverter, if that option requires a ready = LO and busy = HI output, or else leave Q6 out if the reverse logic sense is required. Other instrument modifications may require an NPN or a PNP output of either logic sense. To provide an PNP output, jumpers W1, W2, and W3 are connected so that the entire output side of the isolator is connected between -12 volts and common (3) and PNP transistors are used for Q6 and Q7. Circuit details depend on interface requirements. Refer to the appropriate Option Appendix or the Instrument Modification Sheet for this unit.

4-76 Digital-To-Analog Converter. The digital-to-analog circuits consist of bit switches and ladder networks, a polarity offset switch and two reference voltage circuits. The D/A converter provides discrete output currents as determined by the voltage magnitude input bits from the storage flip-flops,

4-77 D/A Bit Switches and Ladder Networks. This circuit is composed of four similar sets of bit

switches and resistive-ladder networks (one per bit). The switching circuits consist of transistors A3A2Q1-3 through A3A15Q1-3 while the analog ladder networks consist of resistors A3R50 through A3R96. Since all four networks are similar, only the network for the four most significant digits is described in the following paragraphs.

4-78 The bit switch network consists of a driver, Q1, and two low-saturation switching translators, Q2 and Q3. With a voltage program input of +4 volts (001111101000000), the D/A board switching circuits receive the complemented input of -12.3836 (110000010111111). The high inputs (the digits which have a value of binary 1; A16, A15, A9, etc.), at the base of Q1, are inverted and, through steering diode CR1, cause Q2 to turn on placing a +16.384V on the input line to the ladder network. The low inputs (the digits which have a value of binary 0; A14, A13, A12, etc.), at the base of Q1, are inverted and, through steering diode CR2, cause Q3 to turn on placing 0V (ground) on the input line to the ladder network.

4-79 In the simplified schematic of Figure 4-5, the switching transistors are represented by mechanical switches connecting each of the four rungs in the analog ladder network to either 16.384V or ground (2). Again, the switch positions represent the binary input of 1100, the four most significant bits of the inverted input of 4 volts.

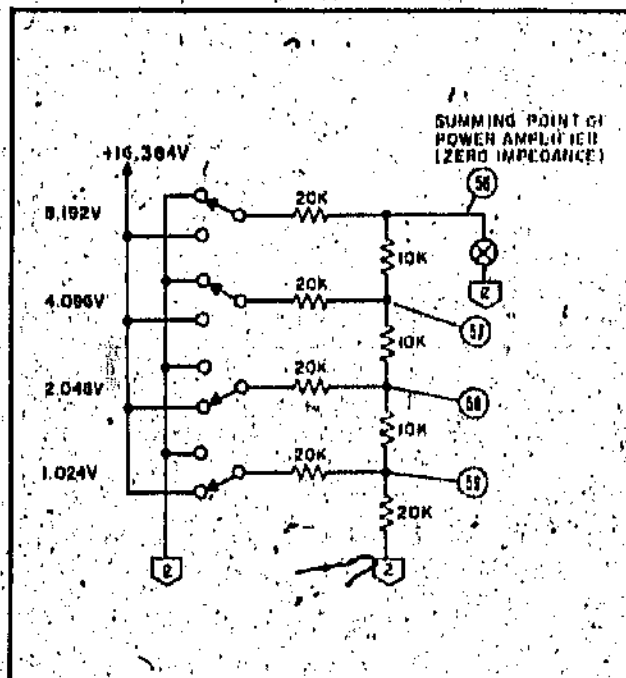


Figure 4-5. Ladder Network, Simplified Schematic

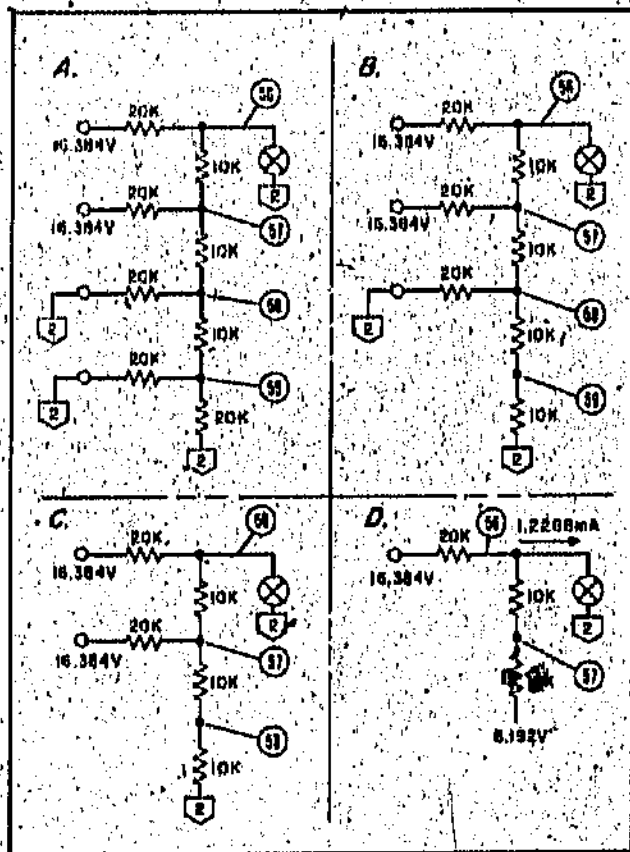


Figure 4-6. Ladder Network Thevenin Equivalents

4-80 Figure 4-6A shows the voltages at the input of each rung. To determine the current flowing into the summing point (X) from the ladder network, a Thevenin Equivalent can be constructed for each rung. If the circuit is broken above TP59, the open circuit voltage at TP59 is 0V and the impedance looking into TP59 is 20K in parallel with 20K or 10K. Thus, the Thevenin Equivalent is 0V (ground) in series with 10K, as shown in Figure 4-6B. Breaking the circuit at TP58 and replacing this portion by its Thevenin Equivalent, we have the circuit shown in Figure 4-6C. Now, breaking the circuit at TP57 and solving for the voltage at this point ($16.384 \times \frac{20K}{40K} = 8.192V$), we are left with the circuit shown in Figure 4-6D. This figure shows that the current flowing into the summing point (TP56) is 1.2288mA.

4-81 The currents flowing into the summing point from the other three ladder networks may be solved in the same manner and the results will be 0.0064 milliamperes, 0.0026mA and 0.00035mA. Summing all four currents together yields a final result of 1.23835mA total flowing into TP56 from the ladder network. As described previously, the +1.23835mA output of the ladder network is summed with -1.6384mA from the polarity switch yielding a net

input to the power amplifier of -0.40005mA. A continuous offset current of +0.05mA at the operational amplifier input yields an effective power amplifier input of -0.40000mA. The power amplifier amplifies this current to produce a +4V DVB output voltage.

4-82 Potentiometers A3R52 through A3R59 are adjusted to compensate for the conducting resistances of Q2-Q3 and resistance tolerances within the network. With these controls properly adjusted, the total series resistances in each rung are 20K, as shown in Figures 4-5 and 4-6. Notice that the output current of each of the four ladder networks are weighted in powers of 16. Thus, resistor A3R92 divides the output current of that rung by 16, resistors A3R93, R94 divide the next rung output current by 256 and resistors A3R95, R96 divide the output current of the remaining rung by 4096.

4-83 Polarity Offset Switch Circuit. This circuit consists of amplifier A3Q13 and switch A3Q14. A constant reference of -16.384V is supplied to the emitter of switch Q14. With a negative sign input A3Q13 receives a high level input signal and switch A3Q14 does not conduct. With positive input sign, however, Q13 receives a low input causing Q14 to saturate. A path for the offset current of 1.6384mA is now completed to the summing point. Potentiometer A3R100 provides a means of adjusting the offset current.

4-84 D/A Converter, +16.384 Volt Reference Circuit. This circuit provides a regulated output voltage of +16.384Vdc. To maintain the output voltage constant, a series regulating feedback loop is employed. A reference comparator circuit, AR-Z1, compares a portion of the output voltage, across divider R34, R36, and AR-R3) with an internal zener diode reference voltage. If a difference exists, the comparator sends an error signal to series regulator Q31 via driver Q32. This error signal is of the phase and amplitude necessary to counteract the original difference. Transistor Q30 provides a constant biasing current to Q32 and AR-Z1. Potentiometer R36 can be adjusted to alter the voltage divider resistance and thus, the +16.384V output. Output capacitor C30 stabilizes the feedback loop.

4-85 D/A Converter, -16.384 Volt Reference Circuit. This regulator circuit is similar to the +16.384V reference supply except that the -16.384V reference supply utilizes the regulated +16.384V as one of its dc inputs in a kind of "Auto-Tracking" configuration. With this technique, any change in the +16.384V output causes an equal percentage change in the -16.384V output thereby minimizing inaccuracies in the D/A converter due to drift or other disturbances.

4-86 The -16, 384V reference supply contains a series regulating feedback loop composed of: comparison amplifier Q11, error amplifiers Q12 and Q15, and series regulator Q10. Incipient changes in the -16, 384V output are detected by Q11B, amplified by Q12 and Q15 and applied to the series regulator. Feedback loop stability is maintained by output capacitor C13 and feedback network C12, R21.

4-87 +21.5 Volt Regulator. A regulated +21.5 volts is obtained from series regulator A3Q40 and zener diode VR40 which keeps the base voltage of Q40 at a constant level.

4-88. CURRENT LATCH AND VOLTAGE RANGE PROCESSING (See Figure 7-2, Sheet 2)

4-89 Input Isolator Circuits. The four input isolators (A6A1 through A6A4) for the latch bits (range, 50mA, and 30mA) and the voltage range bit are identical to those used in voltage processing (refer to paragraph 4-68). The current latch range (X1 or X10) input bit (L24) is at a positive level for the X1 range and a more negative level for the X10 range. The 30mA and 50mA bits (L22 and L23) of current latch data must be in LO = true, negative logic form. For example, when the 30mA input (L22) is LO (more negative level), the 30mA bit is present, and when the 30mA input is HI (more positive level), the 30mA bit is absent. The voltage range input bit is at a more negative level for the X1 range and a positive level for the X10 range. The input isolators invert these input levels.

4-90 Storage. The current latch and voltage range storage flip-flops (A6Z2) are identical to those used on board A2 in voltage processing. When a high storage gate level is present at the clock inputs to the storage flip-flops, the levels present at the data inputs appear at the Q outputs and the complement of that data at the \bar{Q} outputs. Whatever data is present when the storage gate (clock) input becomes low is stored in the flip-flops and continues to appear until the next high clock input occurs. In the storage disable mode, the clock input remains high, and the flip-flops pass the data bits directly through to the current latch decoder and range pulse generator without storing them.

4-91 Storage Gate. The storage gate circuit develops the clock signals for the storage flip-flops. The storage gate signal is received from the logic board in the voltage processing circuits and is applied to the base of Q4 through speed up network (C1 and R62). Q4 and R63 comprise a level setting circuit to provide the proper interface with the logic board. Note that the emitter of Q4 is returned to (4) (-26V) while the emitters of Q5

and Q6 are connected to (2). The storage gate signal is inverted by Q5 and again by Q6 to provide the proper clock level to the storage flip-flops.

4-92 Current Latch Decoder. This circuit converts the three coded current latch bits to an analog output current. Eight possible analog output currents can be obtained; one for each of the eight current latch bit combinations. The output current of the current latch decoder appears at a current summing junction (collectors of A6Q1, Q12, and Q13) and is determined by the conduction of these transistors. The resultant current at the junction flows through A6R30 and A6R37 to develop negative and positive reference voltages, respectively, for the comparators.

4-93 Current latch range is determined by the range bit which turns on A6Q1 in the X1 range and turns off A6Q1 in the X10 range. With Q1 on, (X1 range) a path is completed for the voltage divider network (R8-R13) in its collector circuit. Bias voltages which are less positive now permit transistors Q8, Q9 and Q10 to conduct effectively shorting out resistors R16, R17, and R18, respectively, in the base circuits of Q11, Q12, and Q13. This action insures that the conduction of Q11 is decreased by a factor of 10. If transistors Q12 and/or Q13 are conducting, their conduction is likewise 10x less than that of the X10 current latch range.

4-94 Transistor Q11 is biased in its active region and always conducts one of two fixed amounts of reference current to the summing junction. As just described, the two fixed currents vary by a factor of 10 and depend on the status of the current latch range bit.

4-95 Transistors Q12 and Q13 may, or may not, be conducting depending on the status of the 50mA and 30mA current latch input bits. If transistor Q2 is conducting, Q14 is cut off and Q12 (50mA stage) does not conduct. Under these conditions, no reference current is supplied to the summing junction by Q12. Conversely, when Q2 is cut off, Q12 is allowed to conduct one of two fixed amounts of current as determined by the current latch range bit. Transistor Q13 (30mA stage) is controlled in a similar manner by the 30mA bit and the range bit.

4-96 To better illustrate the action of this circuit, assume that the programmed current latch is 20mA (the three current latch data inputs are all HI). In this case, transistor Q12 and Q13 are not conducting because of high level inputs to Q2 and Q3. Transistors Q1 and Q8 are conducting thus limiting the conduction of Q11 to its X1 range value. If a 200mA current latch is programmed (same as above except current latch range data input is LO),

transistors Q12 and Q13 are cut off, as before, but range transistor Q1 is not conducting. This cuts off Q8 and the conduction of Q11 is increased to its X10 value.

4-97 Negative and Positive Current Comparators.

The current comparators compare the voltage drop across current sampling resistor A5R5 (proportional to the output current) with the voltage drop across A6R30 or A6R37 (proportional to the current latch value). If the output current equals or exceeds the current latch reference value, one of the 24 comparators (positive or negative) generates a negative going current overload signal to turn on the appropriate OR gate diode (CR1 or CR2). The polarity of the output current determines which of the comparators is activated. The positive current comparator (Z4, R32, R34, R43) is activated for positive output currents to monitor the difference between the output and latch reference current. The current sampling signal (J6-N) is one input to the positive current comparator and the positive reference signal is the other input. The positive reference signal is developed by the negative reference inverter (Z3 and Q23). For excessive positive output currents, the positive current comparator generates a negative going output signal causing CR2 to conduct. The negative current comparator (Z4, R31, R33, R39) is activated for negative output currents to monitor the difference between the output and latch reference currents. The current sampling signal is one input to the negative current comparator and the negative reference signal is the other input. For excessive negative output currents, the negative current comparator generates a negative going signal causing CR1 to conduct. With CR1 or CR2 conducting, an overload signal is passed to the current latch and current overload circuits.

4-98 Current Latch Circuits. If a current overload signal is generated, these circuits generate a current latch signal which turns off the power amplifier. The latch output signal is not generated until after variable delay period has elapsed. The delay ranges from approximately 3 μ sec to 2msec. Variable delay stage, Q16, receives the overload signal and, if the C_T terminals are open, passes the inverted signal on to Q17 with a minimal delay (less than 1 μ sec). Under these conditions, the latch delay period is dependent solely on the natural circuit delays of the level detector, latching flip-flop, current latch switch, and the power amplifier (see Sheet 3). The time required to initiate turn-off at the power amplifier with the C_T terminals open is approximately 3 to 10 μ sec.

4-99 For greater latch delays, a capacitor can be connected across the C_T terminals. When Q16 is cut off by the negative going overload signal, the

positive going slope on its collector is now determined by the time taken by capacitor C_T to charge through R42. Hence, increasing the value of C_T increases the latch delay period.

4-100 Shorting the C_T terminals places the collector of Q16 at 0 potential preventing Q17 from conducting. This prevents the unit from operating in the current latch mode. Note that if the unit is already in the current latch mode shorting the C_T terminals will not transfer it out of current latch.

4-101 Level Detector. Transistors Q17 and Q18 form a Schmitt trigger circuit which switches state when the positive going input signal reaches the threshold level. Transistor Q17 conducts when the threshold is reached biasing Q18 below cutoff. The positive going rise on the collector of Q18 is then coupled through limiting diode CR9 to set the latching flip-flop. When current latch commences the Schmitt trigger input goes negative cutting off Q17 and returning the circuit to its original state. The latching flip-flop remains in the set state, however, because diode CR9 blocks the negative going excursion of the collector of Q18.

4-102 Latching Flip-Flop. Transistors Q19 and Q20 are connected in a bi-stable multivibrator configuration. When the DVS is not in a current latch condition, the flip-flop is in the reset state with Q19 off and Q20 on. Reset is initiated by a short duration negative pulse applied to the base of Q20 by reset amplifier Q24. The reset pulse is generated 3 μ sec after the application of a gate input from the computer. The leading edge of the 50 μ sec wide input from input board A1 cuts off Q22. The output of Q22 is differentiated by A6C4 and A6R52 and the positive going spike that occurs at the leading edge of the input is inverted by Q24 and then used to turn on Q20.

4-103 A current latch condition is initiated by a positive going transition applied to the base of Q20 from the collector of Q18. This sets the flip-flop by turning Q20 off causing Q19 to turn on. The flip-flop remains in the set state until a gate pulse is received from the computer and a reset pulse is generated by Q24.

4-104 The latching flip-flop is also set when the shorting relay (A4K1) is deenergized (Figure 7-2, Sheet 3). This ensures that the power amplifier is turned off when the output terminals are shorted by contacts of relay A4K1.

4-105 Buffer and Current Latch Status Circuits. The buffer amplifier (A6Q21) inverts the negative going latch signal from Q20 and applies it to the power amplifier (Figure 7-2, Sheet 3) and to the

latch status isolator/output amplifier (A6A5). The isolator (A6A5Z1, Q1, Q2) is similar to the input isolators previously described. The latch status isolator provides a LO output to indicate latched status and a HI output for normal condition. The output amplifier stages A6A5Q3 and A6A5Q4 that follow A6A5Q2 provide sufficient current drive and proper signal inversion to interface with the computer. Circuit details depend on interface requirements. Refer to the appropriate Option Appendix or the Instrument Modification Sheet for this unit.

4-106. Current Overload Circuits. The current overload circuits consist of an overload flag generator, isolator, output inverter, and a overload status isolator/output amplifier circuit. If the current latch value is exceeded, the negative going overload signal at TP17 is applied to the overload flag generator and to the overload status isolator and output amplifier circuit.

4-107. Overload Flag Generator. The overload flag generator consists of two emitter coupled amplifier stages A6Q29 and A6Q30. The collector stage of each amplifier contains a differentiating network (C13, R95 and C14, R94) and a limiting diode (CR14 and CR15). The limiting diodes conduct only the positive excursion of the differentiated waveform from the respective collector. These diodes also serve as part of the flag enable OR gate along with A6CR16 which receives the voltage range flag. The first output pulse from the overload flag generator is obtained from the collector of Q29. It is initiated by the negative going overload signal (begin current overload) which turns off Q29 turns Q30 on. This causes a negative voltage change at the collector of Q30 and a positive change at the collector of Q29. The positive portion of the differentiated Q29 output is conducted by CR14 while the negative portion of this waveform and the output of Q30 are blocked. The component values of the differentiating network determine the 10 μ sec width of the conducted pulse. The trailing edge (begin current latch) of the overload signal turns Q29 on and Q30 off resulting in a second 10 μ sec pulse at TP33 through CR15. This pulse is obtained from the collector of Q30 and is a replica of the first overload pulse.

4-108. Figure 4-7 illustrates the output pulses obtained from the flag generator (TP33) for a current latch delay of 20 μ sec. Because the output pulses from the flag generator have a fixed width of 10 μ sec, the output waveforms at TP33 will merge if the current latch delay is less than approximately 10 μ sec. For example, if the current latch is 10 μ sec, the waveform at TP33 consists of a single pulse having a width of approximately 20 μ sec.

4-109. Overload/Range Flag Isolator and Inverter. The positive (high) output from the OR gate (TP33)

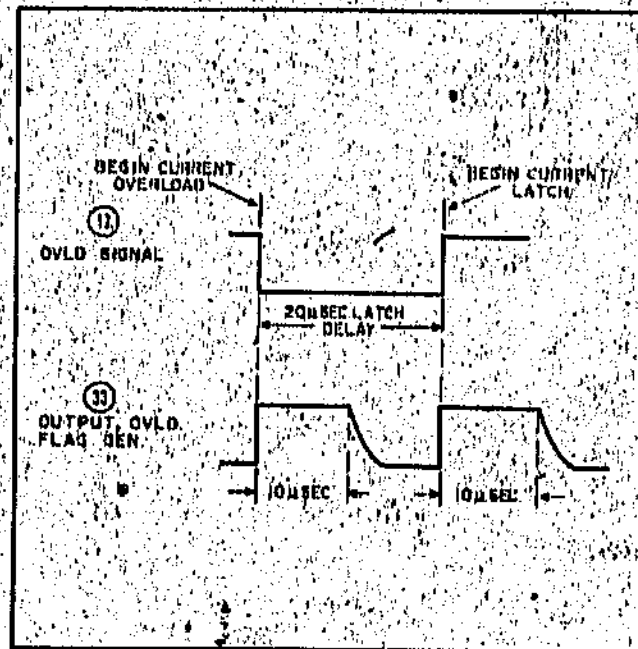


Figure 4-7. Overload Flag Generator Output With 20 μ sec Latch Delay

is applied to the overload/range flag isolator and inverter circuit. The photo-isolator circuit (A6Q31, Z5, Q32) is identical to those previously described. The low output at the collector of Q32 is applied to the base of inverter Q33. A high at the collector of Q33 which is conducted through A6OR20. Diode A6CR20 along with diode A1CR1 comprise an OR gate input to the flag isolator and output amplifier/inverter circuit (Figure 7-2, sheet 1).

4-110. Overload Status Isolator and Output Amplifier. The overload status isolator and output amplifier (A6A6) is similar to the latch status isolator and output amplifier (A6A5), described in paragraph 4-105. For a latch condition, the input to A6A5 is positive causing A6A5Q2 to conduct. For an overload condition, the input to A6A5 is negative causing A6A5Q2 to cutoff. Inverter A6A6Q3 provides a LO output to indicate an overload status. Stage A6A6Q4 is omitted for the standard options.

4-111. Voltage Range Circuits. The voltage range circuits energize or deenergize the voltage range relays in the power amplifier and also provide a 2msec wide flag output to the computer whenever the voltage range is changed. For the X10 range, the range input bit is a positive level causing the range storage flip-flop to provide a negative input to the base of Q25 (range pulse generator). This holds Q25 off, opening the collector load which is connected to the range relay coils (Sheet

3) via A510, pin D. Hence, in the X10 range the relay is demagnetized.

4-112 For the X1 range, the range input bit is a negative level causing the range storage flip-flop to provide a positive input causing Q25 to conduct coupling 2 common to the range relay coils to energize them. Differentiating networks and limiting diodes (C8, R74, CR12 and C9, R75, CR13) in the base and collector circuits of Q25 couple positive going transitions to the base of Q24 in the 2msec delay circuit whenever a change in range occurs.

4-113 The 2msec delay circuit is composed of transistors Q26 and Q28, connected in a type of one-shot multivibrator configuration, and transistor Q27 which provides current gain between the one-shot stages. In the stable state, transistors Q28 and Q27 are conducting and Q26 is held off due to the voltage drop across common emitter resistor, R81. Coupling capacitor C11 charges up to nearly +15V through conducting transistor Q27. When a range change occurs, a positive going transition is received from the range pulse generator. The multivibrator now is driven into its unstable state with Q26 on and Q27, Q28 off. It remains in the unstable state for approximately 2msec until C11 discharges (through R82 and R83) sufficiently to allow the conduction of Q28. The range flag enable output is coupled to the flag output circuit (Sheet 1) via OR gate diode A6CR16.

4-114 POWER AMPLIFIER (See Figure 7-2, Sheet 3)

4-115 Feedback Differential Amplifier. This circuit consists of three differential amplifier stages followed by a single-ended stage. The first two stages (A7Q1 and A7Q2) each consist of two silicon transistors housed in a single package. The transistors have matched characteristics to minimize differential voltages due to mismatching or thermal drift.

4-116 Diodes A7CR3 and A7CR4 protect the input stage, Q1A, from being overdriven by excessive inputs from the D/A Converter and/or the external analog input. Voltage divider A7R1, R2, and R3, connected to the base of the input stage, provides a zero reference bias with no applied input signal. The voltage magnitude input from the D/A converter is summed with the external analog input and the resultant analog current applied to the base of the differential amplifier input stage. The collector circuits of each of the first three differential amplifiers contain RC networks (C1, R6-C2, R16-C4, R25) which help prevent amplifier oscillations. Potentiometer A7R9, in the base circuit of Q1B, can be adjusted to compensate for slight differences between the two base voltages of the input stage,

thus zeroing the output voltage.

4-117 The output of the feedback differential amplifier is taken from the collector of A7Q5 and applied to the coupling amplifier, A7Q6. Negative feedback is employed, from the collector of Q5 to the base of Q1A, for equalization purposes. Zener diode VR7 improves the response time of the feedback amplifier by its clamping action at the collector of Q5.

4-118 Range relay A7K2 switches in the proper value equalizing network for each range: C22 and R88 in the X10 range, or these components in parallel with C23 and R89 in the X1 range. Relay A1K1 changes the range by changing the overall feedback resistance by a factor of 10. The overall feedback line, from the high sensing terminal to the base of Q1A, contains resistors R85, R86, and R87. In the X10 range, in the X1 range, the relay is energized thus shorting out R85 and R86.

4-119 The normal output voltage swing at the collector of Q5 is between +1 volt and -6 volts. Those two extremes represent output voltages +50V and -50V, respectively. Q5 provides an output of approximately -3V when the output voltage is zero.

4-120 Coupling Amplifier. Inverter Q6 serves as a "level changing" transistor, coupling the relatively small negative output level of Q5 to the considerably higher output levels used in the power amplifier output circuits. The gain of the coupling amplifier is small, only slightly greater than one. If the gross current limit is exceeded, the coupling amplifier receives a turn-down signal from Q23 (if positive output voltage gross current limit is exceeded) or Q20 (if negative output voltage gross current limit is exceeded). The operation of the positive and negative gross current limit circuits is described in subsequent paragraphs. Notice that the supply voltages for the coupling amplifier input circuits are low level ($\pm 15V$) and referenced to $\textcircled{2}$ common. The power amplifier output stages, on the other hand, use high-level supply voltages ($\pm 75V$ and $\pm 95V$) that are referenced to $\textcircled{1}$ common. Transistor Q31 in the emitter circuit of coupling amplifier Q6, serves to minimize unwanted ground current from flowing in the low sense output terminal and causing erroneous DVS output monitoring at the low sense terminal. If Q31 were not included and the emitter of Q6 were returned directly to $\textcircled{2}$ common, only a portion of the emitter current of Q6 would return to $\textcircled{2}$ by way of the base (and input circuits) current flow. A significant amount of Q6 emitter current would flow in its collector circuit which is, of course, referenced to $\textcircled{1}$. A return path to $\textcircled{2}$ for this current would be required with collector current flowing through $\textcircled{1}$ current sampling resistor A5R5, the low output

terminal (as well as the protection diodes across the low output and low sense terminals), through the low sense terminal (externally connected to the low output terminal) and on to Q_6 (internally connected to the low sense terminal). Thus, a possibly significant offset voltage could be produced at the low sense terminal particularly if the low sense lead resistance is large. Transistor Q_{31} , however, returns most of the high-level supply current through its collector circuit with only the difference between the base-emitter current of Q_6 and the base-emitter current of Q_{31} required to return to Q_6 through the low sense terminal circuit. This return current is relatively insignificant so that the accuracy of monitoring DVS operation at the low sense terminal is not impaired.

4-121 Power Amplifier. The power amplifier consists of three push-pull stages which are of complementary symmetry design. The input stages Q_{10} and Q_{12} , is driven by a single-ended stage, Q_7 . For positive output currents the positive section of the amplifier (NPN transistors Q_{10} , Q_{11} , Q_2 , Q_1 , Q_{14} , and Q_{15}) is conducting while the negative section (PNP transistors Q_{12} , Q_{13} , Q_3 , Q_4 , Q_{16} , and Q_{17}) is cutoff. The reverse is true for negative output currents. At zero output current, both halves of the power amplifier are conducting a slightly with Q_{30} providing the drive and diodes CR_{17} and CR_{18} providing the voltage drop necessary to forward bias Q_{10} and Q_{12} simultaneously. This eliminates "dead spots" when the unit is programmed away from zero.

4-122 Transistor Q_7 is a voltage amplifier, having a gain of approximately 20, while the three emitter-coupled push-pull stages provide most of the total current gain of the power amplifier. Hence, the voltage at the bases of the push-pull input stage (Q_{10} and Q_{12}) is essentially equal to the output voltage of the unit. Q_7 , together with R_{36} , CR_{16} , CR_{18} , CR_{21} , and R_{38} form a voltage divider network in the base circuit of the input stage. The conduction of Q_7 controls the current flowing in the voltage divider and, thus, the bias at the bases of the input transistors. Zener diodes VR_3 and VR_4 prevent the output voltage from exceeding approximately ± 55 volts.

4-123 Diodes CR_{30} through CR_{34} and resistors R_{108} and R_{109} are included in the Q_{10} and Q_{12} circuits to speed up the gross current limit operation of the DVS. Normally diodes CR_{30} through CR_{32} are reversed biased. However, if the output current exceeds approximately 1.8A, these diodes conduct and limit the output current to less than 2A (approximately 1.8A). This circuit limits the output current in approximately 2 μ sec thereby protecting the DVS circuits until the gross current

limit comparators react (in approximately 25 μ sec) to limit output current to 1.1A. Operation of the gross current limit comparators is described in subsequent paragraphs.

4-124 Under current latch conditions, transistors Q_{10} and Q_{12} are biased below cutoff due to the conduction of Q_8 and Q_9 , part of the current latch switch circuit. The conduction of these transistors effectively shorts the bases of Q_{10} and Q_{12} to the high output terminal, reducing the bias current to zero. The current latch switch and isolator circuits are described in succeeding paragraphs.

4-125 The second push-pull stage (Q_{11} and Q_{13}) on the A7 amplifier board drives the power output transistors (Q_1 through Q_4) which are mounted on the rear heat sink. These transistors are connected in series between the +75V and -75V supplies. The conduction of Q_2 or Q_3 is controlled directly by the output of Q_{11} or Q_{13} , depending on which half of the amplifier is active at the time. The conduction of the other series transistor (Q_1 or Q_4) is controlled by the positive or negative bias transistors (Q_{14} and Q_{15} or Q_{16} and Q_{17}). The base of each bias output transistor (Q_{14} or Q_{16}) is connected to the center tap of a voltage divider (R_{45} and R_{46} or R_{49} and R_{50}) which, in turn, is connected between the ± 25 volt supply and the high output terminal. With this arrangement, variations in the output voltage are felt at the base of Q_{14} or Q_{16} and thus cause output transistor Q_1 or Q_4 to follow its series partner (Q_2 or Q_3). Resistors R_{45} - R_{46} and R_{49} - R_{50} are selected so the base of appropriate bias transistor (Q_{14} and Q_{16}) rests at approximately half of the difference between the output voltage and the ± 25 volt supply voltage. This has the effect of equally dividing the voltage drops (and thus the power dissipation) between the two conducting output transistors.

4-126 Gross Current Limit Comparators. The positive and negative current limit comparators protect the output transistors of the power amplifier by limiting the maximum output current to a safe level for both source and sink conditions. The output current for normal source conditions is limited to a fixed maximum of 1.1A; for sink conditions the maximum current is a linear variable ranging from 0.25A at 50V (at HI output terminal) to 1.1A at 0V. Because the two current limiters are so similar only one, the positive, limiter, is described in detail.

4-127 When the output current is within specified limits, transistor Q_{21} is biased on, Q_{22} and Q_{23} are cutoff, and diode CR_{29} is reversed biased. Under these conditions the limiter has no effect on the output current. Zener diode VR_{11} together with resistors R_{115} , R_{116} , and R_{120} form a bias

network that holds the base voltage of Q22 slightly more positive than the base voltage of Q21 and thus establishes a positive current limit switching level. If the output current starts to exceed the source current limit of 1.1A, the voltage drop across sampling resistor A5R5 increases and produces a voltage level at the base of Q21 equal to the base voltage of Q22. With zero differential voltage between Q21 and Q22, Q22 comes out of cutoff switching on Q23 and forward biases CR29. The negative voltage coupled through CR29 clamps the power amplifier output current at a maximum of 1.1A. Diodes CR38 and CR39 protect the base emitter junction of Q22 from voltage transients caused by surge currents through A5R5.

4-128 During sinking conditions the normally positive output voltage becomes negative. This negative voltage is fed back through diode CR40 and influences the positive current limit switching level at the base of Q22. As the output voltage becomes increasingly negative, the positive current limit switching level decreases so that Q22 will switch on and initiate current limiting at an output current level less than 1.1A.

4-129 Current Latch Isolator and Switch. These two circuits operate in conjunction with the current latch circuits on the A6 Control Board. The current latch isolator circuit consists of switching transistor A7Q25 and tuned-collector oscillator A7Q24. A positive going transition at the current latch input at the base of A7Q25 causes it to conduct. The resultant output at its collector, is fed to the emitter of A7Q24 via swamping resistor A7R70. This allows A7Q24 to conduct through the 10MHz tank circuit (T1 primary winding and capacitor C20) in its collector circuit. Voltage divider resistors R68 and R69 establish the base bias. Regeneration for sustained oscillation is coupled from the collector winding of T1 to the base winding. Each end of the T1 output winding contains a rectifier-filter network in order to drive the push-pull current latch switch, A7Q8 and A7Q9. Rectifiers CR7 and CR8 conduct on the positive half cycles; rectifier diodes CR11 and CR12 conduct on the negative half cycles. Under latch conditions, both, Q8 and Q9 conduct to zero bias the power amplifier push-pull input stage (A7Q10 and A7Q12).

4-130 Disconnect Interlock. Relay A4K1 and driver transistor A4Q1 protect the load by shorting the output terminals of the DVS under certain conditions. The output terminals are shorted when K1 is deenergized. This occurs if the (3) common input from the computer is removed or the -12V DELAYED is not present. When the unit is first turned on, K1 is also deenergized because the -12V bias input is delayed for approximately 0.2 seconds after turn-on. Notice that the current latch circuits are activated at this time and, thus, must be reset with a gate input before the unit can be restored to normal operation. The output is also shorted at turn off of the unit because the -12V bias input collapses rapidly causing K1 to deenergize.

4-131 POWER DISTRIBUTION (See Figure 7-2, Sheet 4)

4-132 The $\pm 12V$, $\pm 26V$, $\pm 75V$, and $\pm 95V$ bias and supply voltages are obtained from power supply board A4. The +5V is obtained from chassis mounted +5 volt regulator Z1. Note that the +5V supply is referenced to (4) which is at -26V with respect to (2), the common potential for the $\pm 26V$ supply. The $\pm 12V$ supply is referenced to (3) which is connected to the computer ground. The $\pm 12V$, $\pm 26V$, $\pm 75V$, and $\pm 95V$ supplies are simple networks containing rectifier diodes, filter capacitors, and bleeder resistors.

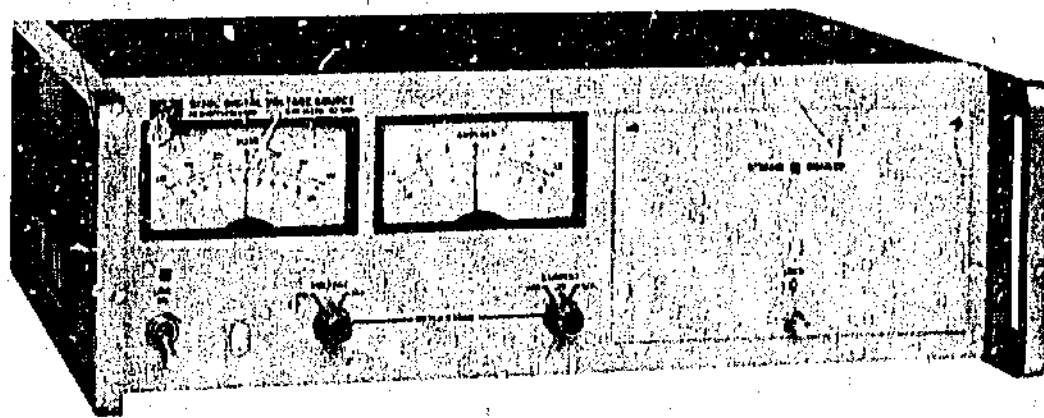
4-133 Amplifier board A7 contains two regulator circuits for deriving $\pm 15V$ outputs from the $\pm 26V$ inputs. Each circuit is composed of a series regulator (Q26 or Q28) and an input comparator stage (Q27 or Q29). The input stage compares a portion of the output voltage with a fixed reference voltage (across VR5 or VR6). If a difference exists, it generates an error voltage which is of the correct amplitude to counteract this difference.

4-134 Boards A1, A2, A3, and A6 contain filter capacitors for various supply voltages. In addition, board A1 contains zener diodes and resistors to develop +5V referenced to (3) and board A6 contains a series regulator A6Q34, resistors, and a zener diode to provide +4.99V referenced to (2). Series regulator A6Q34 also provides a +14.5V output referenced to (2).

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SECTION I GENERAL INFORMATION

1-1 DESCRIPTION

1-2 The Digital Voltage Source (DVS) is a complete digital-to-analog link between a computer (or other digital source) and any application requiring a fast accurately settable source of dc or low frequency ac power.

1-3 A constant voltage/current limiting source, the DVS will furnish full rated output voltage at the maximum rated output current or can be continuously programmed throughout two output voltage ranges. The output is bipolar, and is programmable on either side of, or through, zero without output polarity switches or "notch" effects. In addition, the DVS has low output impedance—the load does not degrade the accuracy specification. The DVS analog output is floating and fully isolated from the digital inputs, thus avoiding ground loops between the output ground and the computer ground.

1-4 The output voltage is controlled by digital data inputs applied to the DVS via a ribbon connector on the rear panel.

1-5 Overcurrent protection is provided by a current "latch" circuit which can be externally or internally programmed to one of eight values between 2% and 100% of the units rated output current. When activated, the current latch circuit turns off the output power amplifier reducing the output current to less than 10mA. The reaction time of the current latch circuit (time between the start of a current overload and turn off of the power amplifier) can be adjusted by adding an external capacitor at the rear terminals. The upper current limit is safeguarded by a separate fixed current limit circuit that prevents the output current from exceeding 110% of the current rating. The computer is continuously informed of possible current overload or current latch conditions by status outputs which are fed back to the user's source.

1-6 For maximum reliability and minimum size and weight, the DVS utilizes all solid state circuitry. Most of the DVS circuitry is contained on five removable plug-in circuit boards, accessible from the front of the unit through an access door.

1-7 Output voltage and current are continuously displayed on two front panel meters. The front

panel METER RANGE switches select the desired voltage and current ranges.

1-8 The DVS also limits sink current (resulting from an active load forcing energy back into the DVS) to a value between 0.25A and 1.1A as a function of sink voltage magnitude.

1-9 Terminals for High Output, High Sensing, Low Output, Low Sensing, Chassis Ground, Current Latch Delay, Analog Input, and Current Monitor are included on a rear barrier strip. The Low Output terminal may be connected to the ground terminal, or the output may be floated up to 300 volts above ground. The output terminals are automatically shorted if the digital input cable is disconnected or if the input power is removed. The Sensing terminals may be used when the load is remotely located from the DVS in order to avoid degradation in regulation at the load due to voltage drop in the load leads.

1-10 INTERFACING

1-11 Each DVS is pre-interfaced with its controlling computer, or other digital device, by modifying three of the plug-in boards. Five standard sets of these boards (Option J20 and Options 061 through 064) satisfy the majority of interfacing requirements. Each instrument must have either an Option number or a "Special" modification number (e. g., J01, J02, etc.) for identification. The Jxx numbers are used for instruments which do not fit into the standard option category. Detailed descriptions of the different options are included in Appendixes at the rear of each manual while descriptions of special options are included on blue modification sheets in the front of applicable manuals. The option number for each instrument appears on an identification tag at the rear of the unit.

1-12 As supplied from the factory, the DVS can be operated from a 115Vac $\pm 10\%$, 48-440Hz power source. In addition, the DVS can be operated from a 230Vac $\pm 10\%$ single phase input when the unit is equipped with Option 28 (see Paragraph 1-15). This versatility makes the instrument compatible with the European power system.

1-13 SPECIFICATIONS

1-14 Complete specifications for the Digital Volt-

age Source are given in Table 1-1.

1-15 OPTIONS

1-16 As mentioned previously all DVS's are pre-interfaced at the factory. There is no standard instrument; each unit has an option number for identification. There are five "standard" options which satisfy the majority of interfacing requirements. Two of these options (061 and 063) are for BCD instruments while the other three (J20, 062, and 064) are for binary units. Detailed coverage of these options is included in Appendixes at the rear of the manual.

<u>Option No.</u>	<u>Description</u>
020	<u>Rewire for 230Vac Input:</u> Consists of reconnecting the input transformers for 230 volt operation and changing the fuse. (Refer to Section II for details.)
J20	<u>Binary Interface for μ 12661A DVS Program Card:</u> Input/output circuits on P.C. boards A1, A2 and A6 are modified to interface with μ computer. (Refer to proper Appendix for details.)
061	<u>BCD Interface for NPN Open Collector Circuits:</u> Input/output circuits on P.C. boards A1, A2 and A6 are modified to interface with a BCD digital source employing "open collector" drivers. (Refer to proper Appendix for details.)
062	<u>Binary Interface for NPN Open Collector Circuits:</u> Input/output circuits on P.C. boards A1, A2, and A6 are modified to interface with a binary source employing "open collector" drivers. (Refer to proper Appendix for details.)
063	<u>BCD Interface for Microcircuit Logic Levels:</u> Input/output circuits on P.C. boards A1, A2, and A6 are modified

to interface with a BCD source employing microcircuit logic of the TTL or DTL family. (Refer to proper Appendix for details.)

064

Binary Interface for Microcircuit Logic Levels: Input/output circuits on P.C. boards A1, A2, and A6 are modified to interface with a binary source employing microcircuit logic of the TTL or DTL family. (Refer to proper Appendix for details.)

1-17 INSTRUMENT IDENTIFICATION

1-18 Hewlett-Packard instruments are identified by a three-part serial number. The first part is the power supply model number. The second part is the serial number prefix, consisting of a number-letter combination denoting the date of a significant design change. The first digits indicate the year (10 = 1970, 11 = 1971, etc.); the second two digits indicate the week; and the letter "A" designates the U.S.A. as the country of manufacturer. The third part is the power supply serial number; a different 5-digit sequential number is assigned to each power supply, starting with 00101.

1-19 If the serial number on your instrument does not agree with those on the title page of the manual, Change Sheets supplied with the manual or Manual Backdating Changes define the differences between your instrument and the instrument described by this manual.

1-20 ORDERING ADDITIONAL MANUALS

1-21 One manual is shipped with each power supply. Additional manuals may be purchased from your local Hewlett-Packard field office (see list at rear of this manual for addresses). Specify the model number, serial number prefix, and HP Part number shown on the title page.

Table 1-1. Specifications

INPUT AND OUTPUT POWER

Input:

115Vac $\pm 10\%$, 48-440Hz, 1.2A, 100W
(Standard)

230Vac $\pm 10\%$, 48-440Hz, 0.6A, 100W
(Option 28 only)

Output:

X1 Range: -16.384 to +16.383Vdc
@ 1.0A Source.

X10 Range: -50 to +50Vdc @ 1.0A Source.

Sink Current Compliance:

A sink condition results from an active load attempting to force energy back into the DVS. This can appear as current flow into the HI output terminal when the terminal is positive, or current flow out of the terminal when it is negative. In either case the current is limited to a value ranging linearly from 0.25A at 50V to 1.1A at 0V.

ACCURACY

Basic Accuracy:

DC voltage accuracy at 23°C $\pm 3^\circ\text{C}$,
115Vac input, no load, following 30 minutes
warm-up.

X1 Range: 1mV

X10 Range: 10mV

Source Effect (Line Regulation):

Change in output voltage for any change
in line voltage from 104 to 126Vac (or 208 to
254V ac).

X1 Range: 500 μV

X10 Range: 5mV.

Load Effect (Load Regulation):

Change in output voltage for any change
in load current within rating.

X1 Range: 150 μV

X10 Range: 500 μV

Temperature Coefficient:

Change in output voltage per degree
Centigrade change in ambient temperature.

X1 Range: 160 $\mu\text{V}/^\circ\text{C}$

X10 Range: 800 $\mu\text{V}/^\circ\text{C}$

PERIODIC AND RANDOM VOLTAGE DEVIATIONS

Drift (Stability):

DC output voltage drift under constant
line, load, and ambient temperature for
8 hours after 30 minutes warm-up.

X1 Range: 500 μV

X10 Range: 2.5mV.

PARD (Ripple and Noise):

p-p/rms (dc to 50MHz), at any line voltage

and under any load condition within rating.

X1 Range: 2mV p-p/0.5mV rms

X10 Range: 7mV p-p/1.5mV rms

Load Transient Recovery Time:

Time required for the output voltage to recover
within 0.1% of full range voltage following a full
load current change.

X1 or X10 Range: 150 μsec .

SPEED

Programming Time:

Maximum time required for the output volt-
age to settle within 0.1% of the programmed
voltage change after simultaneous receipt of
data and gate signals with a resistive load
connected across the output terminals.

X1 or X10 Range: 300 μsec . Voltage range
change required 2msec.

ANALOG INPUT

Impedance: 10k Ω $\pm 1\%$.

Maximum Input Voltage (Full Range):

X1 Range: $\pm 20\text{V}$

X10 Range: $\pm 5.0\text{V}$

Bandwidth (to -3dB Point): Approx. 25kHz.

DC Gain: X1 Range: $-1 \pm 0.2\%$

X10 Range: $-10 \pm 0.2\%$.

Stability (8 hours):

X1 Range: Same as stability of input signal
+ 500 μV .

X10 Range: Same as stability of input sig-
nal + 5mV.

CURRENT SENSING

Impedance: 800 Ω

Coefficient: 1 Volt/Amp.

Accuracy: 3% $\pm 2\text{mA}$

TEMPERATURE RATINGS

Operating: 0°C to +55°C.

Storage: -40°C to +75°C.

COOLING

Convection cooling is employed.

ACCESSORIES FURNISHED

50-Contact Rear Plug, HP Part No. 1251-0085,

Rack Mounting Kit, HP Part No. 5060-8740

Plug-in Extender Board, HP Part No. 5060-7948

ACCESSORIES AVAILABLE

Pocket Programmer, Model 14533B. This ac-
cessory permits manual programming of all in-
put functions by switch closures.

3-Foot Extension Cable for Pocket Programming,

Model 14534A. This accessory may be used
with the Pocket Programmer for maximum con-
venience.

SECTION II INSTALLATION

2-1 INITIAL INSPECTION

2-2 Before shipment, this instrument was inspected and found to be free of mechanical and electrical defects. As soon as the instrument is received, proceed as instructed in the following paragraphs.

2-3 MECHANICAL CHECK

2-4 If external damage to the shipping carton is evident, ask the carrier's agent to be present when the instrument is unpacked. Check the instrument for external damage such as broken controls or connectors, and dents or scratches on the panel surfaces. If the instrument is damaged, file a claim with the carrier's agent and notify Hewlett-Packard Sales and Service Office as soon as possible. If the instrument appears undamaged, perform the electrical check given in the following paragraph.

2-5 ELECTRICAL CHECK

2-6 Check the electrical performance of the instrument as soon as possible after receipt. Section V of this manual contains performance check procedures which will verify instrument operation within the specifications stated in Table 1-1. This check is also suitable for incoming quality control inspection. Refer to the inside front cover of the manual for the Certification and Warranty statements.

2-7 REPACKING FOR SHIPMENT

2-8 When shipping the entire instrument, it is recommended that the package designed for the instrument be used. The original packaging material is reusable. If it is not available, contact your local Hewlett-Packard field office to obtain the materials. This office will also furnish the address of the nearest service office to which the instrument can be shipped. Be sure to attach a tag to the instrument specifying the owner, model number, full serial number, and service required, or a brief description of the trouble.

2-9 INSTALLATION DATA

2-10 The instrument is shipped ready for bench operation. Power connections are made through the power cable supplied with the unit. The digit-

tal inputs to control the output voltage, current limit, etc., must be supplied through the data input plug (P1) at the rear of the unit. Section III of this manual provides a complete description of the interfacing requirements.

2-11 LOCATION

2-12 This instrument is convection cooled. Sufficient space should be allotted so that a free flow of air can reach the rear of the instrument when it is in operation. It should be used in an area where the ambient temperature remains between 0°C and +55°C.

2-13 OUTLINE DIAGRAM

2-14 Figure 2-1 shows the outline and dimension information for the instrument which can be used to plan a specific installation.

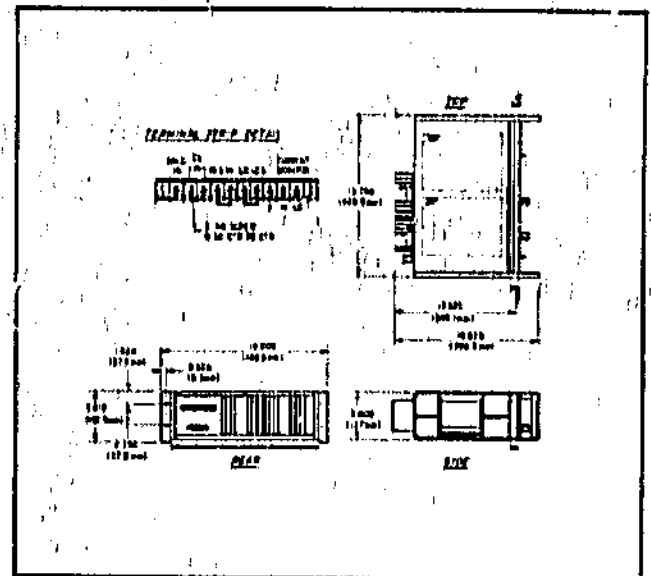


Figure 2-1. Outline Diagram

2-15 RACK MOUNTING

2-16 To mount the unit in a standard rack panel, proceed as follows:

- Remove gray plastic trim strips (glued on) at each side of unit by inserting a thin screwdriver

at edge or top of strip and prying gently away from unit.

b. Attach rack ears (furnished with each unit) to side of unit using screws supplied with ears.

c. Mount unit in rack, using standard mounting screws.

2-17 INPUT POWER REQUIREMENTS

2-18 POWER REQUIREMENTS

2-19 This instrument may be operated continuous-

ly from either a nominal 115 volt or 230 volt, 48-440Hz power source. The unit as shipped from the factory is wired for 115 volt operation. The input power required when operated from a 115 volt power source at full load is 1.2 amperes, 100 watts.

2-20 CONNECTIONS FOR 230 VOLT OPERATION (Figure 2-2)

2-21 Normally, the primary windings of input transformers T2 and T3 are connected in parallel for operation from a 115 volt source. To convert the unit to operate from a 230 volt source, the primary windings of each transformer must be connected in series as follows:

a. Unplug line cord and remove top cover.

b. Looking from the rear of unit, locate the 115Vac jumpers between terminals 1,3, and 2,4 of transformer T3 (see Figure 2-2).

c. Remove both 115Vac jumpers and solder the 230Vac jumper between terminals 2 and 3 of transformer T3 as shown in Figure 2-2.

d. Replace existing fuse (on rear panel) with 1 ampere, 230V fuse.

2-22 POWER CABLE

2-23 To protect operating personnel, the National Electrical Manufacturers' Association (NEMA) recommends that the instrument panel and cabinet be grounded. This instrument is equipped with a three conductor power cable. The third conductor is the ground conductor and when the cable is plugged into an appropriate receptacle, the instrument is grounded. The offset pin on the power cable's three prong connector is the ground connection.

2-24 To preserve the protection feature when operating the instrument from a two-contact outlet, use a three-prong to two-prong adapter and connect the ground lead on the adapter to ground.

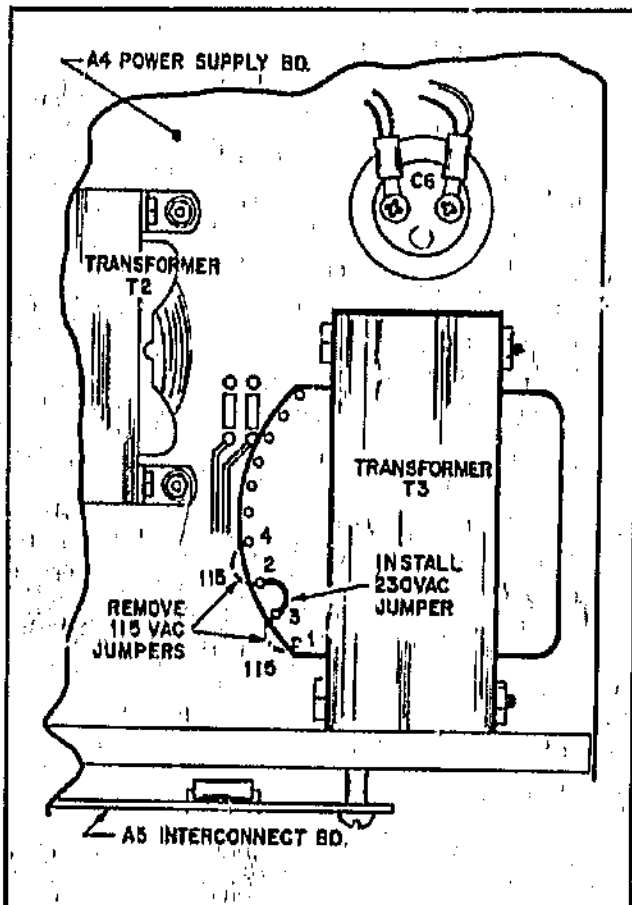


Figure 2-2. Primary Connection for 230Vac Operation

SECTION III OPERATING INSTRUCTIONS

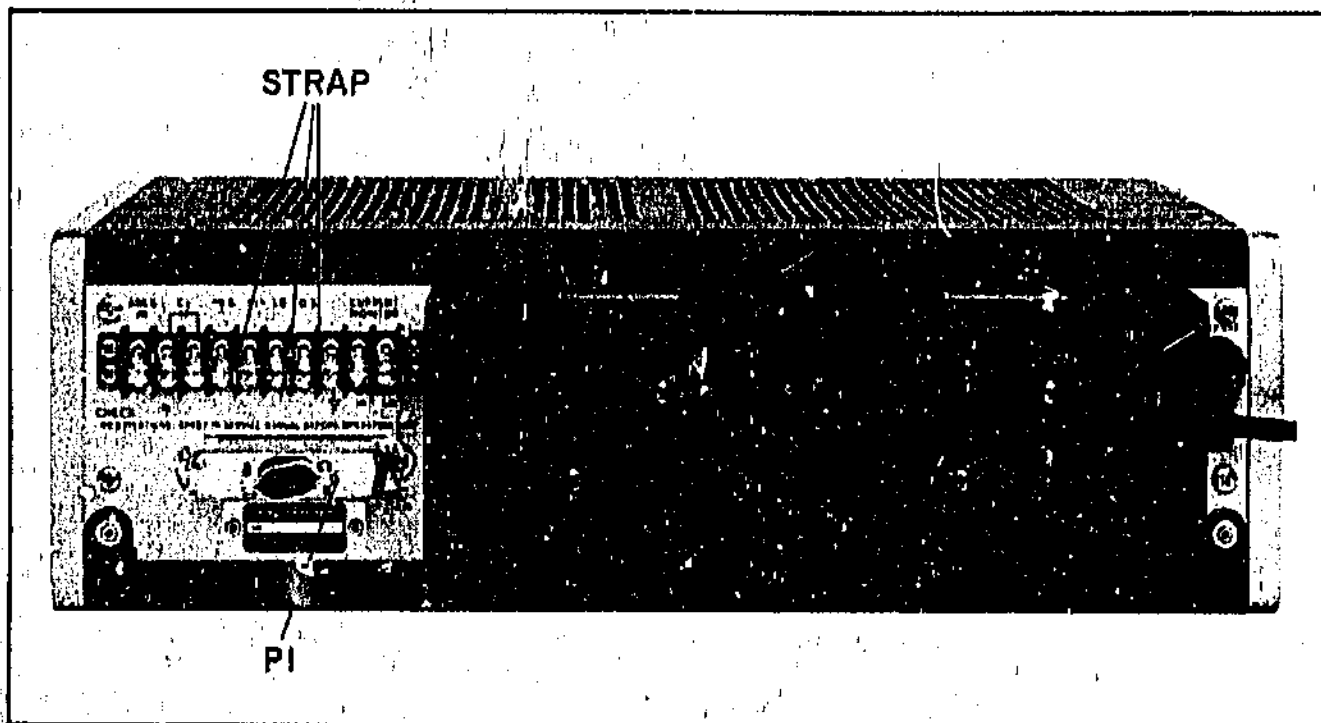


Figure 3-1. Model 6130C, Rear View

3-1 DATA INPUT CONNECTOR

3-2 Before output voltage can be obtained, data input plug P1 must be in place as shown in Figure 3-1. A connection must be made between the cable continuity interlock pin 25 and the computer common (relay A4K1 must be energized; see Figure 7-2, Sheet 3). If this connection is not present or if the input connector is removed, the output terminals will be shorted and the output current will be reduced to less than 10mA. This protects any loads connected to the DVS in the event that the cable is inadvertently disconnected. Note also that the output is shorted when ac power is removed.

3-3 AC INPUT

3-4 To turn on the unit, set the LINE switch (Item ① in Figure 3-2) to ON. The pilot light directly above the LINE switch should light. Fuse 1 (2A at 115Vac or 1A at 230Vac) protects the main power supply.

NOTE

Any deflection of the current meter after turn-off does not represent current flowing in the load but rather is current flowing through the internal shorting relay.

3-5 VOLTMETER RANGES

3-6 The VOLTAGE control ② selects either the 50V or 10V range, which corresponds to the upper and lower scales on the voltmeter. The shaded area on the front panel meter face indicates the amount of output voltage that is available (5V) in excess of the normal rated output. Although the instrument will operate in this shaded region without being damaged, it is not guaranteed to meet all of its performance specifications.

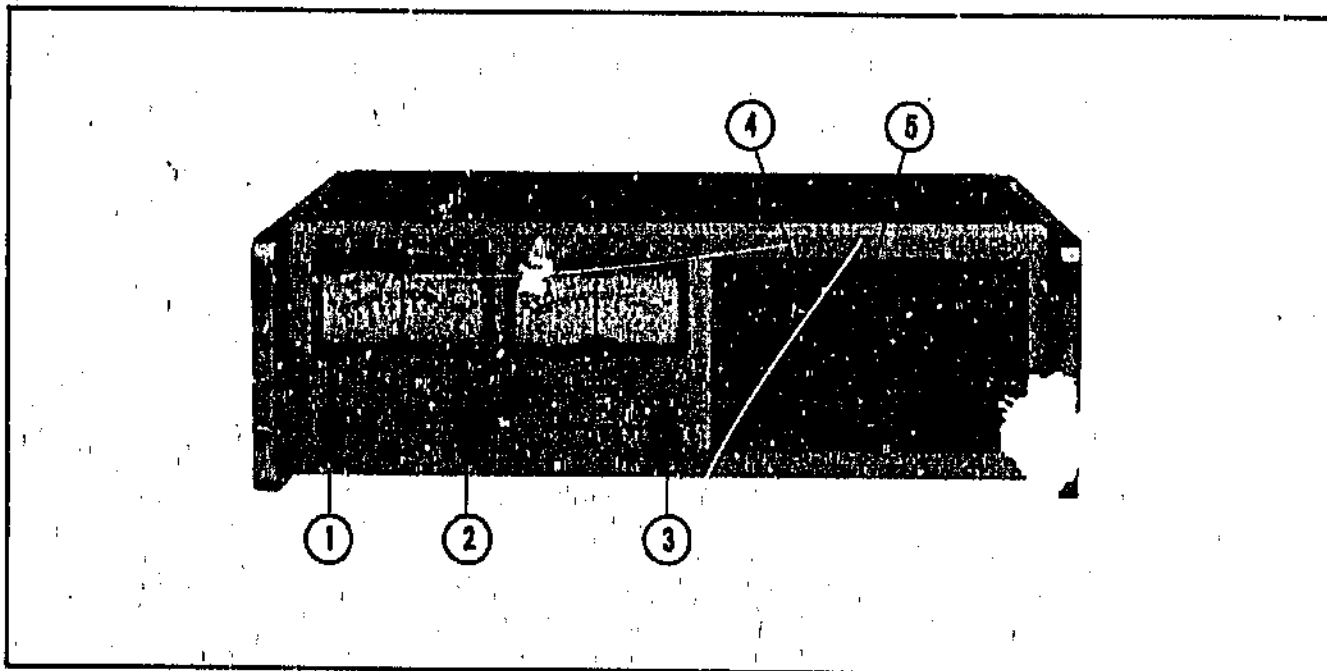


Figure 3-2. Operating Controls and Indicators

3-7. AMMETER RANGES

3-8 The CURRENT control, ③ selects the current range on the front panel meter, 0.12, 0.3, or 1.2A. A 2-amp slo-blo fuse is used as shown on the rear of the unit.

3-9 PROGRAMMING

3-10 Input/output data is connected from a digital computer to P1/J1 on the rear of the DVS as shown in Figure 3-3. A substitute for the computer is HP Pocket Programmer. This accessory plugs into J1 and manually programs all the input to the DVS by switch closures. An extension cable, with connectors on both ends, is also available to mate with J1 and the Programmer plug. Pocket Programmers can be purchased from your local Hewlett-Packard Sales Office.

3-11 The coding, voltage levels, and polarity of the input/output data are selected by the customer to fit his application. Three plug-in boards, A1 Input, A2 Logic, and A6 Control, are modified at the factory to fit these requirements. Most customer requirements can be satisfied by one of the standard options for this instrument. For requirements beyond the scope of the standard options, special modifications are made to the A1, A2, and A6 boards. Either an option number or a special (J) number is assigned to each instrument and is printed on an identification tag on the rear heat sink of the unit. Options are described in Appendixes located at the rear of the manual while special changes are described in an "Instrument

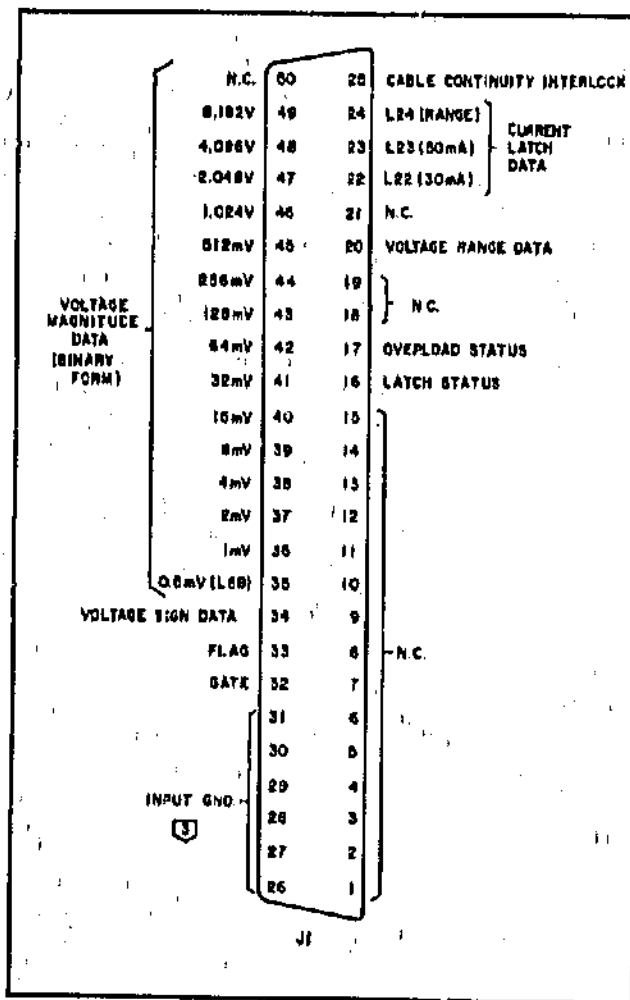


Figure 3-3. Input/Output Data Connector

Modification sheet which is inserted in the front of any applicable manual.

3-12 The following paragraphs describe the input/output data that is transferred between the computer and the DVS. Sufficient detail to operate the instrument is included; more detailed information is included in Section IV.

3-13 VOLTAGE MAGNITUDE AND VOLTAGE SIGN DATA INPUTS

3-14 Fifteen lines designated according to their positive analog equivalent value in millivolts (0.5, 1, 2, 4, 8, ..., 4096 and 8192) comprise the voltage magnitude input. This input is received from the computer, or other programming source, in a "computer binary" code. Positive numbers are received in straight binary form while negative numbers are received in negative 2's complement form; that is, the equivalent positive number is complemented (all ones become zeros, all zeros becomes ones) and a binary one is added to the least significant bit. Notice that because of the nature of negative 2's complementing, it is impossible to program for "negative zero" volts output. The lowest negative number that can be programmed is -0.5mV . Hence, to obtain an output of zero volts, the sign must be positive.

3-15 The voltage magnitude and sign data are stored in the DVS upon the receipt of a gate input from the computer. As shown in Figure 3-4, the voltage magnitude and sign data bits must remain for at least $10\mu\text{sec}$ after the triggering edge of the Gate. Once the $10\mu\text{sec}$ period is expired, the voltage program and sign can be changed to prepare for the next gate. The gate must reset for at least $2\mu\text{sec}$ before starting a new gate, and the time between the leading edges of two consecutive gates must be at least $55\mu\text{sec}$.

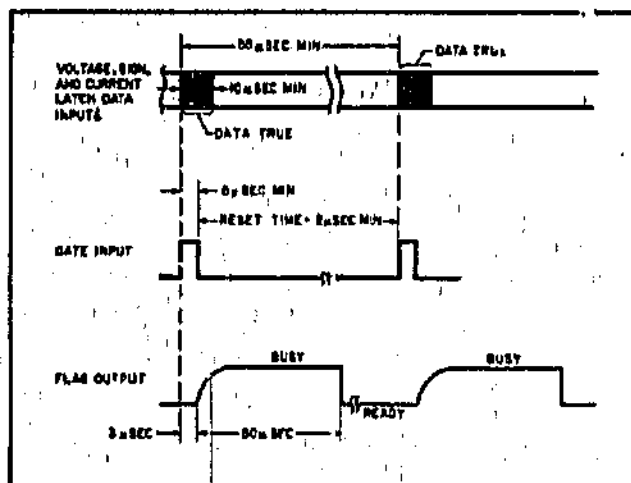


Figure 3-4. Timing Diagram, No Range Change

3-16 Notice that in addition to initiating the storage and processing of voltage and sign data, the Gate also stores the voltage range and current latch data which are discussed in subsequent paragraphs. It should be noted, though, that the trailing edge of the Flag indicates to the computer that the voltage processing is complete and will occur $55\mu\text{sec}$ after the leading edge of the Gate provided the voltage range of the DVS has not been changed. If a voltage range change is programmed, the trailing edge of the Flag is delayed to 2msec from the leading edge of the Gate (refer to Paragraph 3-21).

3-17 STORAGE

3-18 With the STORAGE switch (4) (Figure 3-2) in the STORE position, the voltage, sign, range, and current latch program data are stored when the gate is received from the computer. In the DISABLE position, indicator DS1 (5) lights and the data are processed as soon as they are received.

3-19 Storage can be disabled in cases where a manual programmer is used or where the computer has internal storage for the voltage magnitude and sign data.

3-20 VOLTAGE RANGE

3-21 The voltage range data input from the computer multiplies the voltage magnitude data X1 for the lower range or X10 for the higher range. In the X1 range, the maximum output voltage swing is from -16.384 to $+16.3835$ volts. In the X10 range, the output voltage swing is from -50.00 to $+50.00$ volts. The range of the DVS is controlled by the voltage range data bit from the computer which is stored (along with the voltage magnitude, sign, and current latch data) in the DVS when the Gate input is received. As shown in Figure 3-5, the voltage range data bit must remain for at least $10\mu\text{sec}$ after the triggering edge of the gate. Once the $10\mu\text{sec}$ period is expired the voltage range input can be removed. The gate must reset for at least $2\mu\text{sec}$ before starting a new gate, and the time between the leading edges of two consecutive gates must be at least 2msec .

3-22 If a range change is programmed, then, the trailing edge of the Flag sent to the computer is delayed 2msec after the leading edge of the Gate. If a range change is not programmed, the DVS Flag is returned $55\mu\text{sec}$ after the Gate as indicated in Figure 3-4 and discussed in paragraph 3-15.

3-23 Voltage Range Programming. The voltage range bit from the computer has two states, X1 and X10. In the X1 range, the voltage magnitude data input is multiplied by 1 so that the output voltage can be varied (in 0.5mV or greater steps) between 0.000 and $+16.3835$ volts (positive sign

bit) or $-0.000F$ and -16.384 volts (negative sign bit). In the X10 range, the voltage magnitude data input is multiplied by 10 so that the output voltage can be varied (in 5mV steps or greater) between -50.00 and $+50.00$ volts.

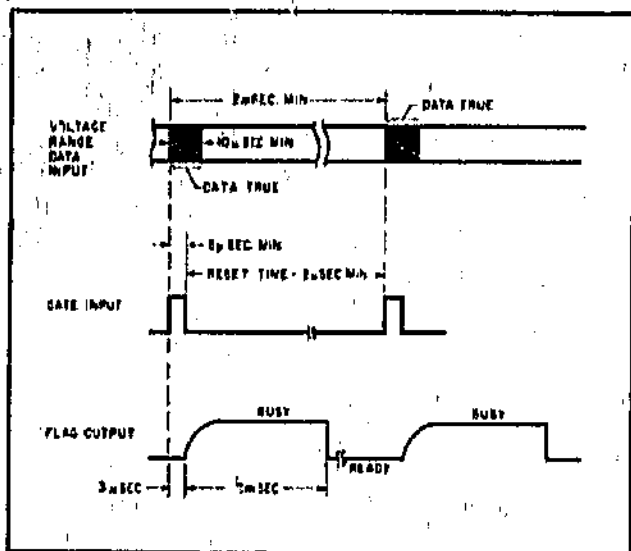


Figure 3-5. Timing Diagram, Range Change

3-24 CURRENT LIMIT

3-25 The DVS provides a maximum (gross) limit and a programmable current limit (referred to as current latch on this unit). Each current limit is controlled independently by a separate circuit. The gross current limit circuit is fixed to activate at approximately 110% of the rated output current (approximately 1.1A). The adjustable current latch circuit can be programmed to 20, 50, 70, 100, 200, 500, 700, or 1000mA. Current latch input data consist of three lines: L22 (30mA), L23 (50mA), and L24 (range, X1 or X10). All three inputs are stored in the DVS when the gate signal is received. As shown in Figure 3-4, the current latch data must remain for at least 10µsec after the triggering edge of the gate. The flag signal is sent to the computer 55µsec after the gate to indicate that current latch processing is complete.

3-26 If the overload condition persists for a certain variable delay period, the current latch circuit is activated, and the output current is reduced to from 0 to 10mA, depending on the type of load connected to the unit. The output voltage, under current latch conditions, depends on the programmed output voltage and the type of load. With a full resistive load connected to the unit, the output voltage (and current) are reduced to nearly zero. At no load, the output voltage will correspond to the programmed voltage; up to a maximum of 40

volts. After the load current is reduced or the current latch increased, the next gate that is received will reset the current latch circuit and return the unit to normal operation.

3-27 In addition to the current limits described above, the current limit circuits also protect the DVS from active loads that force energy back into the DVS (sink condition). This can appear as current flow into the HI output terminal when the terminal is positive, or current flow out of the terminal when it is negative. Figure 3-6 shows the normal operating locus of the DVS. As shown, the DVS will limit the sink current to a value ranging linearly from 0.25A at 50V to 1.1A at 0V.

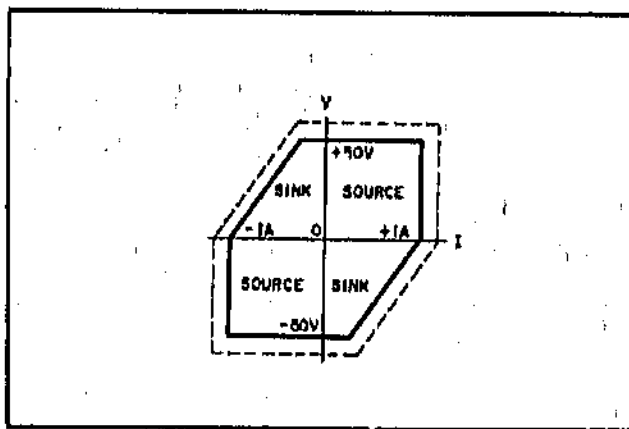


Figure 3-6. 6130C Output Ranges

CAUTION

Externally applied terminal -to- terminal voltage in excess of 55V will damage the DVS.

3-28 Current Latch Programming. The current latch data bits L22 (30mA), L23 (50mA), and L24 (range) from the computer form a 3-bit binary code to program the DVS current latch value. The states of the 30mA and 50mA bits determine the basic value; the state of the range bit multiplies that value by 1 or 10. The following chart illustrates the code for each current latch value in standard option (NPN) units. The three current latch bits provide a maximum of eight possible combinations as shown in the chart. If the pocket programmer is used to program the current latch, refer to the associated manual.

3-29 CURRENT OVERLOAD AND LATCH

3-30 If the output current exceeds the value of the programmed current latch a 10µsec flag signal and the overload status signal are sent to the computer

NPN CURRENT LATCH CODING

CURRENT LATCH (mA)	L24 (RANGE)	L23 (50mA)	L22 (30mA)
20	HI	HI	HI
50	HI	HI	LO
70	HI	LO	HI
100	HI	LO	LO
200	LO	HI	HI
500	LO	HI	LO
700	LO	LO	HI
1000	LO	LO	LO

HI = more positive voltage
LO = more negative voltage

as shown in Figure 3-7. If the overload condition still exists after a variable delay period, (refer to next paragraph) the unit commences current latch operation and the latch status signal changes state. The current overload status signal switches to the normal state when the current latch mode commences. A second 10- μ sec wide flag signal is produced when current latch begins.

NOTE

For standard Option J20, the two 10 μ sec Flag outputs corresponding to the leading and trailing edges of the Overload status output are disabled and not transmitted to the computer.

3-31 Current Latch Delay. Two terminals, C_T , on the rear barrier strip are provided for connection of a capacitor to delay the current latch circuit. Capacitor C_T determines the delay between detection of an over-current condition (current overload status) and the time that current latch begins (the current latch status signal switches to the overload state). Some delay is desirable when driving a capacitive load, since current surges higher than the current latch setting would activate the current latch circuitry. If the C_T terminals are open, a natural delay period of from 3 to 10 μ sec (approximate) will result. If capacitor C_T is utilized, the delay is adjustable between 5 μ sec and 2msec at the rate of approximately 1 μ F per msec.

3-32 The current latch status signal will switch from overload to normal state approximately 10 μ sec after the next gate providing that the overload condition no longer exists. Therefore, to program the DVS out of the current latch condition and back to normal operation, the overload must be removed or the current latch increased; and then a new gate must be issued. The flag will switch to busy 5 μ sec after the gate is received and remain in that state for 50 μ sec.

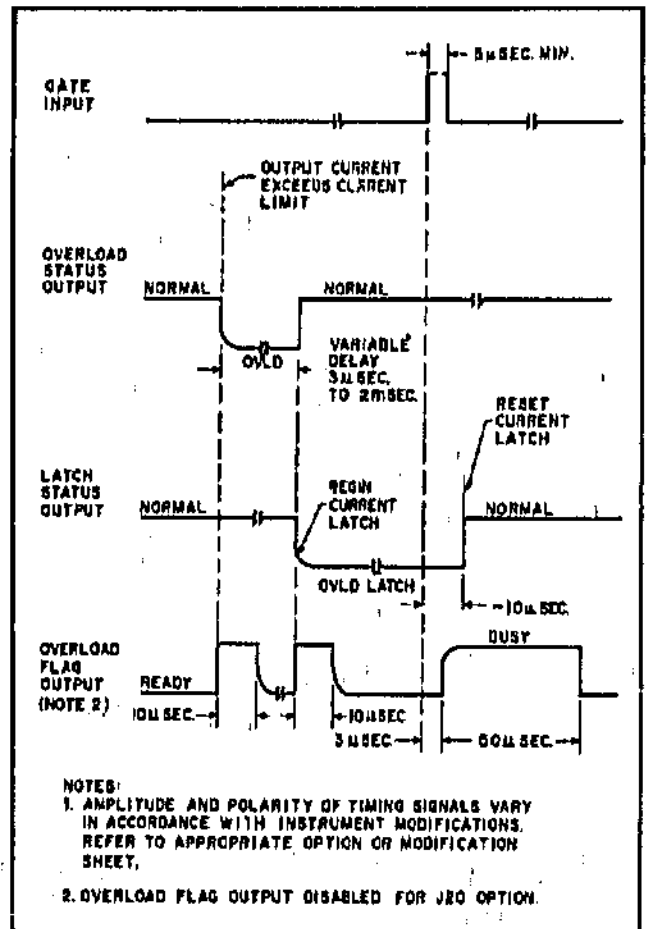


Figure 3-7. Current Latch Overload Timing Diagram

3-33 Current Latch Disable. The current latch circuit within the DVS can be disabled by shorting the C_T terminals at the rear of the unit. Under these conditions, the current limit is governed solely by the gross current limit circuit which fixes the current limit at about 1.1 amperes. Although the current latch status signal is not generated, the overload status signal is switched to the overload state if the output current exceeds the programmed current latch value. Shorting the C_T terminals is useful during calibration or troubleshooting when it is desirable to keep the unit out of the current latch mode. Ensure that the shorting wire(s) across the C_T terminals is short (less than six inches long). The inductance of long wires could cause the current latch circuit to become activated.

3-34 Current Latch At Turn On. At turn on, the output terminals are shorted for approximately 0.2 second. This will activate the current latch circuitry reducing the output current accordingly. After the short is removed from the output terminals, a gate input must be received from the computer to reset the latch circuit and return the unit to normal operation.

3-35 CONNECTING THE LOAD

3-36 Low sense (LO S) and high senses (HI S) should be connected to LO and HI respectively, as shown in Figure 3-1.

3-37 Remote Sensing is used to maintain good regulation at the load and reduce the degradation of regulation which would occur due to the voltage drop in the leads between the power supply and the load. Remote sensing is accomplished by utilizing the strapping pattern shown in Figure 3-8. The power supply should be turned off before changing strapping patterns. The leads from the sensing terminals to the load will carry much less current than the load leads and it is not required that these leads be as heavy as the load leads. However, they should be twisted or shielded to minimize noise pickup. Remote sensing leads longer than 15 feet may have high frequency resonances which can cause the power supply to oscillate. If long leads are anticipated consult your local Hewlett-Packard Sales Engineer for techniques to eliminate oscillation.

3-38 Note that it is desirable to minimize the voltage drop in the load leads and it is recommended that the drop not exceed 1 volt per lead if the power supply is to meet its dc specifications. If a larger drop must be tolerated, please consult an HP Sales Engineer.

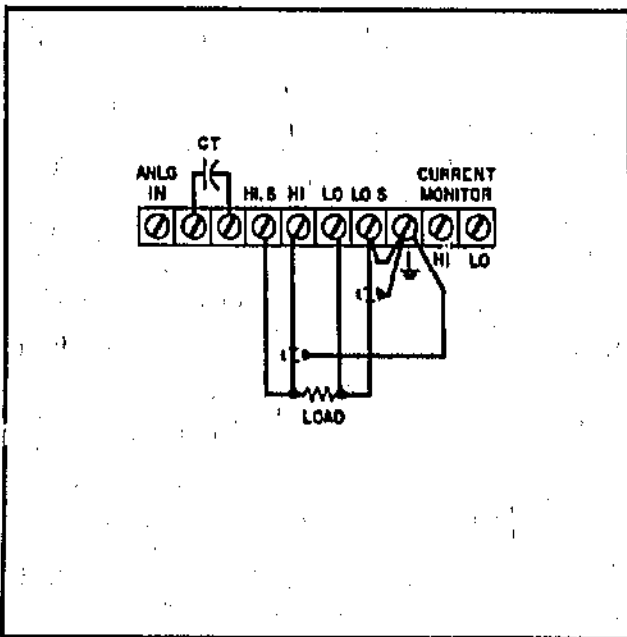


Figure 3-8. Remote Sensing, Strapping Pattern

3-39 Grounding. Proper grounding will greatly reduce output ripple and noise. It is recommended that the LO output terminal be connected to the

GND terminal. The HI output terminal should not be connected to GND during normal operation.

3-40 If the output terminals must be floated at some dc potential, a capacitor (between 0.05 and 0.1 μ F) should be connected between the LO and GND terminals. If the above capacitor is not connected, a common-mode noise signal will be induced in the output leads. Since this noise signal will have an amplitude of approximately 100mV, it is recommended that the above capacitor be utilized.

3-41 CURRENT MONITOR

3-42 The CURRENT MONITOR terminals (Figure 3-8) can be used to monitor the output current of the DVS without affecting the output voltage. To monitor the output current, a DVM is connected across the CURRENT MONITOR HI and LO terminals. The output voltage reading is proportional to the current output in the ratio of 1 volt/1 ampere output current. With a positive output programmed through a resistive load, the LO terminal is positive with respect to the HI terminal. The accuracy of the CURRENT MONITOR reading is $\pm 3\%$. For example, a reading of 250mV indicates that the DVS output current is 250 ± 7.5 mA.

3-43 ANALOG INPUT

3-44 The ANALG IN terminal (Figure 3-8) can be used to program the output of the DVS with an analog input. The analog input signal can be a dc level or a variable signal (a sine wave, for instance). The analog input signal is connected between the ANALG IN and LO S terminals.

3-45 The analog input is summed with the digital voltage magnitude data (after it is converted to its equivalent analog current) at the input to the DVS power amplifier. The result of the summation is used to drive the power amplifier which produces the specified output voltage. Since the power amplifier inverts its input, the analog input voltage must be of opposite polarity with respect to the polarity of the desired output voltage. The power amplifier amplifies the input signal by 1 in the X1 range and by 10 in the X10 range.

CAUTION

To protect the DVS from damage, the combination of digital voltage magnitude data and analog input should not cause the DVS to exceed its rated limits (± 50 Vdc). Further, regardless of the digital voltage input, the analog input in the X1 range should not be greater than ± 20 V nor greater than ± 5.0 V in the X10 range.

3-46 The DVS output voltage can be determined by the following formula: $V_{OUT} = -\text{Range} \times \text{Analog Input} + \text{Digital Program Voltage}$. For example if a +5.000Vdc output is desired with no digital voltage program input, a -5.000Vdc input can be applied to the ANALG IN terminal with the DVS set to the X1 range. The equation is: $V_{OUT} = -1 \times (-5.000) + 0 = +5.000\text{Vdc}$. This same output, of course, could also be obtained by applying a

-0.500Vdc input with the DVS in the X10 range. Negative DVS output is obtained in a similar manner; that is, by applying a positive analog input at the ANALG IN terminal. The bandwidth of the analog input (measured at the -3dB point) is approximately 25kHz. In other words, the gain of the power amplifier falls off if the analog input frequency exceeds 25kHz with the amplifier approaching unity gain at 100kHz.

SECTION IV PRINCIPLES OF OPERATION

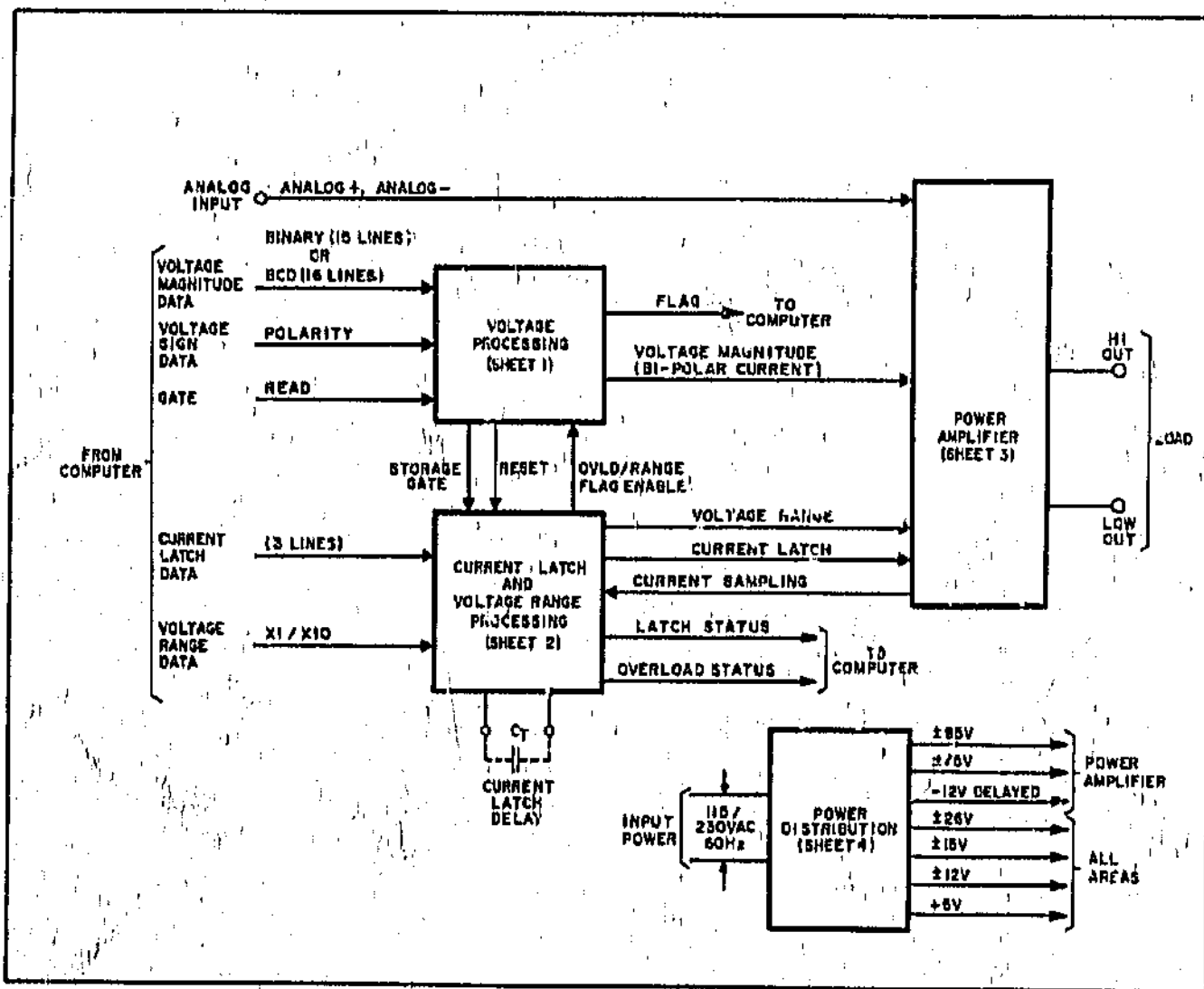


Figure 4-1. Basic Block Diagram

4-1 INTRODUCTION

4-2 This section contains the principles of operation for the Digital Voltage Source (DVS). The section is divided into three main paragraphs: a basic block diagram discussion, a detailed block diagram discussion, and a detailed circuit analysis. The depth of coverage increases with each level of discussion until, in the detailed circuit analysis, the function of each major component is described using the schematic diagrams of Figure 7-2.

4-3 BASIC BLOCK DIAGRAM DISCUSSION

4-4 Figure 4-1 is a basic block diagram of the DVS showing its four major circuits, together with the principle input/output signals of each circuit. Each major circuit has an associated sheet number for correlation of this diagram with the schematic sheets at the rear of the manual.

4-5 The Digital Voltage Source is a digital-to-analog "link" capable of providing an accurately

adjustable source of dc or low frequency ac power. It provides -16.384 to +16.385 volts (in 0.5mV steps) or -50 to +50 volts (in 5mV steps) at 0 to 1A, from dc to 25kHz. Current limit protection is provided by a current "latch" circuit which can be programmed to activate at one of eight values; ranging from 20mA to 1000mA. Back-up protection is provided by a gross current limit circuit which prevents the output current from exceeding 110% (maximum) of the rated output current.

4-6 VOLTAGE PROCESSING

4-7 The voltage processing circuits interface, isolate, store, and convert to analog form the digital input data representing the magnitude and sign of the required output voltage. The input circuits adapt the DVS to the requirements of the driver circuits to be used and provide dc isolation between the computer ground and the DVS output. Integrated circuits store the received data and a digital-to-analog converter translates the stored data to a bi-polar analog current. This bi-polar analog current signal controls the output of the power amplifier.

4-8 The input gate signal initiates timing and storage functions for both the voltage processing and current latch and voltage range processing circuits. The storage function allows the voltage processing circuits to continuously provide a voltage magnitude output without the need for repeated voltage magnitude and sign inputs from the computer. Each time the input gate is received, a storage gate reset signal and a flag are generated. The storage gate signal initiates the storage function within the current latch and voltage range processing circuits. The reset output signal resets the current latch circuit if (1) the circuit is in the latch condition; and (2) if the condition that originally caused the latch has been corrected. The reset signal is ignored if these two conditions have not been satisfied.

4-9 The flag output provides timing information to the computer concerning the status of the voltage processing and current latch and voltage range processing circuits. It is generated in response to the gate input or the overload/range enable inputs from the current latch and voltage range circuits.

4-10 CURRENT LATCH AND VOLTAGE RANGE PROCESSING

4-11 Current latch and voltage range processing circuits interface, isolate, store, and process input digital information to provide the current latch and voltage range output signals to the power amplifier. Input circuits, similar to those used in voltage processing, adapt the DVS to the com-

puter circuits and provide dc isolation. Integrated circuits store the information when the storage gate is received from voltage processing. The stored current latch and voltage range data is then processed by separate circuits as will be described in subsequent paragraphs.

4-12 Current Latch Processing. The three lines of current latch data are decoded and are used to establish a reference current limit which is compared with a sample of the output current (current sampling input from the power amplifier). If the current sampling input equals, or exceeds, the reference current limit, a current overload status signal is immediately sent to the computer informing it that an overload condition exists. If the overload condition still exists after a variable delay period, the current latch and current latch status output signals are simultaneously generated. The current latch delay period is approximately 3 to 10µsec with the C_T terminals open and with added capacitance can be extended to 2msec. The time delay should be extended for applications involving capacitive loads to prevent surge currents from initiating premature current latch action. When the C_T terminals are shorted, the current latch circuitry is disabled inhibiting the generation of the current latch and latch status output signals. If generated, the current latch output signal turns off the power amplifier so that the output current is reduced to a safe value (less than 10mA). The latch status signal informs the computer of the current latch status of the DVS.

4-13 Whenever a current overload or latch condition occurs, an overload flag enable signal is sent to the voltage processing circuits which, in turn, issues a flag output to the computer.

4-14 Voltage Range Processing. The voltage range data input is stored, and then sent as a voltage range select signal to control the power amplifier range relays. With the relays energized, the voltage program input signal is multiplied by 1 (X1 range). With the relays deenergized, the voltage magnitude is multiplied by 10 (X10 range). Similar to current overload condition, a range flag enable, and then a flag signal is issued whenever a voltage range change occurs.

4-15 POWER AMPLIFIER

4-16 The power amplifier amplifies the bi-polar voltage magnitude input current to provide a bi-polar output voltage across the load connected between the HI and LO output terminals. An external analog input signal can also be applied to the power amplifier. A signal applied to the analog input terminal is summed with the voltage magnitude signal from voltage processing. For this condition, the power amplifier amplifies the sum

of these signals. Shunt feedback is employed to prevent changes in the output voltage without a change in the input signal. Additional feedback networks are used within the amplifier stages for stability purposes.

4-17 As mentioned previously, the amplifier circuits multiply the current input signal by X1 or X10, depending on the status of the voltage range input from the voltage range processing circuit.

4-18 The power amplifier includes a self-contained, gross current limit circuit which is fixed to activate at 110% (maximum) of the rated output current. When activated, the gross current limit circuit limits the conduction of the power amplifier preventing the output current from exceeding the maximum current limit value.

4-19 Additional protection for the load is provided by a circuit which shorts the output of the amplifier whenever input power is interrupted or the input cable from the computer is disconnected.

4-20 POWER DISTRIBUTION

4-21 Power distribution circuits accept 115 volts or 230 volts, single phase, 60Hz input power and provide unregulated dc bias voltage outputs to the three major circuits. Additional regulated bias voltages are generated by reference supplies and voltage regulators in voltage processing and the power amplifier. Overload protection is provided by a fuse in the input circuit. The delayed -12 volt output to the power amplifier provides protection of the output load by keeping the amplifier output shorted until the internal bias supplies within the DVS have stabilized.

4-22 DETAILED BLOCK DIAGRAM DISCUSSION

4-23 Figure 7-1 is a detailed block diagram of the Digital Voltage Source showing each stage, or group of stages, within each of the three major circuits. The major circuits are bracketed by heavy-weight lines and sheet numbers are provided to correlate this drawing with the overall schematics of Figure 7-2. For the sake of simplicity the bias supplies and regulators are not included on Figure 7-1; but are discussed in the detailed circuit analysis.

4-24 The detailed block diagram discussion describes, in block diagram terms, the operation of each major circuit. Details concerning the components inside the many circuit blocks are given in the detailed circuit analysis which also includes information on the internal adjustments and controls. Waveforms and timing diagrams are included throughout to supplement the text. For ease of un-

derstanding, the waveforms are idealized. The waveforms are keyed to various points on Figure 7-1 by means of encircled test point numbers.

4-25 VOLTAGE PROCESSING

4-26 The voltage processing circuits consist of an input board, logic board, and a digital-to-analog converter board. The circuits will be explained functionally based on signal flow from board-to-board. A timing diagram for the voltage processing circuits is included on Figure 7-1.

4-27 Voltage Magnitude Input Data. Incoming voltage magnitude data (TP10) is in "computer binary" form—where positive numbers are received from the computer in straight binary and negative numbers are received in the negative 2's complement code. Negative 2's coding consists of complementing the corresponding positive number (changing all logical zeros to ones and all ones to zeros) and adding binary "1" to the least significant bit. (Examples of positive and negative input numbers will be given later.)

4-28 Input Isolators. Voltage magnitude and voltage sign data input isolators provide the logic interface and dc isolation required between the user's computer and the DVS. Incoming voltage magnitude data is applied first to a resistive voltage divider which establishes voltage levels that can be readily utilized by the DVS. DC isolation is provided by a photo-isolator. The input isolator circuit inverts the polarity of the input data, and, in the case of PNP driver circuit, converts it to signal levels appropriate to the NPN logic circuits of the DVS.

4-29 Gate Input and Timing. The gate input (TP1) initiates storage and other timing functions within the DVS. As described in Section III (Figure 3-4) the leading edge of the gate must be received at least 10μsec before the voltage magnitude (data) and sign bits are terminated.

4-30 The input gate signal is first level-set by a resistive voltage divider and then inverted, if necessary, to ensure that the 3-microsecond delay circuit receives a positive-going input transition. The 3-microsecond delay circuit produces a 3-microsecond negative pulse (TP4) whose trailing edge activates the 50-microsecond delay circuit. The two complementary outputs of the 50-microsecond delay are 50-microsecond pulses delayed from the input gate by 3-microseconds. The 3-microsecond delay ensures that the resulting storage gate occurs after the start of the incoming data pulses. The negative 50-microsecond gate pulse (TP6) serves as the input to the gate pulse isolator while the positive output is the input to

the flag isolator.

4-31 The flag output to the computer (TP16) is produced by an OR gate whose inputs are the 50-microsecond pulse (TP40), a pair of pulses occurring at the beginning and end of a current overload, and a 2-millisecond pulse which occurs during a change in voltage range. Waveforms for the flag output signals may be found in Figures 3-4, 3-5, and 3-7. The isolator for the flag signal output permits the output amplifier/inverter to be biased and configured to interface with the computer's receiver circuit. The trailing edge of the 50-microsecond flag produced by a gate input informs the computer that voltage processing is complete and the unit should be producing the requested output. The gate pulse isolator provides dc isolation. The isolator output (TP7) triggers the gate pulse generator and also resets the current latching flip-flop. The gate pulse generator produces a 2-microsecond positive pulse (TP8) with its leading edge delayed by 3-microseconds from that of the input gate.

4-32 With the storage disable switch in the STORE position, the gate pulse generator output pulse is the input to an OR gate whose output (TP9) is the storage gate for voltage magnitude and voltage sign bits. Putting the storage disable switch in the DISABLE position substitutes a fixed positive voltage for this pulse. This permits the bits to pass directly through the storage flip-flops. The output of the OR gate either gates or disables the current latch and voltage range storage flip-flops in the same manner.

4-33 As the unit is turned on, the initial gate pulse generator produces a storage gate input to the OR gate that assures that the storage flip-flops are in the desired initial state.

4-34 Storage. Having storage capability permits the DVS to provide a continuous output after initial data is no longer present. Fifteen latching flip-flops are provided for the voltage magnitude bits and one for voltage sign storage. A storage gate (TP9) strobes the flip-flops, allowing the magnitude and sign inputs to either set or reset them. If the data source is either NPN positive logic or PNP positive logic, the non-inverting outputs of the voltage storage flip-flops are connected. For negative logic inputs, the inverting outputs are connected. The proper outputs are selected by locating the storage flip-flop packages at appropriate locations on the board. Since the data has already been inverted (complemented) once by the input isolators, the outputs of the flip-flops are low for the bits of the incoming data from the computer that are ones. The polarity of the sign bit

is adapted to the logic of the DVS circuits by means of a jumper at the output of the sign flip-flop. Storage can be disabled by the storage/disable switch on the logic board, in which case the outputs of the storage flip-flops follow the data inputs continuously. Voltage and sign data from storage is applied to the digital-to-analog converter.

4-35 Digital-To-Analog Converter. The digital-to-analog converter converts the digital data to either a positive polarity analog current (for negative voltage magnitude inputs) or a negative polarity analog current (for positive voltage magnitude inputs). The latter is accomplished by a negative reference current applied to the converter by the polarity offset switch whenever the input is positive. The magnitude of the D/A converter output current varies between plus and minus 1.6384mA according to the value of the incoming voltage and sign data.

4-36 The D/A converter contains a series of switches (transistors) which are activated by the input data bits from storage. These switches then act on a resistive ladder network which produces an output current (in milliamperes) which is proportional to the numerical value of the input data. The combined output of the ladder network and the polarity offset switch make up the voltage magnitude signal. This signal is applied to the power amplifier where it is summed with the current produced by the external analog input, if any. The algebraic sum of these currents is inverted by the power amplifier and appears at the output terminals as the programmed output voltage.

4-37 Polarity Offset Switch and -16.384V Reference. For input data bearing a negative sign, the polarity offset switch is held off by the sign input from storage and has no effect on the operation of the D/A converter. Under these conditions, the D/A converter supplies a positive output current which is proportional to the applied binary data. For positive input data, the sign input turns on the polarity offset switch and a negative reference current of 1.6384mA is applied to the D/A converter from the -16.384V reference source. The negative reference current is then summed (within the D/A converter) with a positive current which is numerically equivalent to the complemented value of the original input data. The resultant output then, is a negative analog current which has been restored to the original numerical value of the positive input data (prior to complementing) by the addition of the -1.6384mA reference current.

4-38 To better understand the processes which take place within the voltage processing circuits, refer to Figure 4-2. With +4 volts programmed

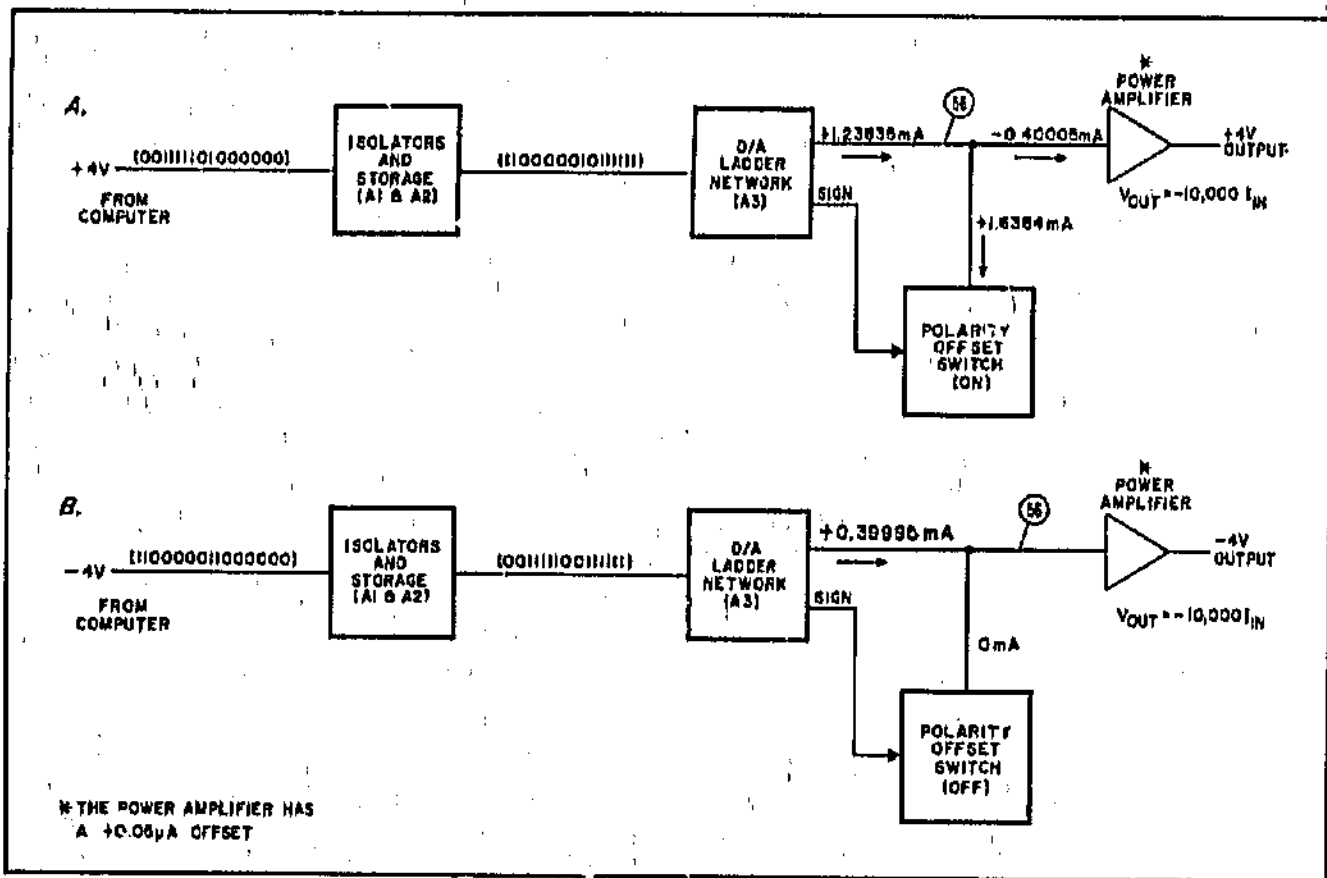


Figure 4-2. Voltage Processing Circuits, Simplified Schematic

into the DVS, the isolators/storage circuits invert the signal which is then changed into a programming current, the result of which is 1.23835mA flowing into TP56 on the D/A Board (A3). The polarity offset is turned on by the positive sign program bit. This draws a current of 1.6384mA from TP56 leaving -0.40005mA to be amplified and inverted by the amplifier section; the result of this will be +4 volts at the output terminals (the amplifier section has a +0.05µA offset).

4-39 If -4 volts (negative 2's complement) were programmed into the instrument (Figure 4-2B), again the isolators/storage circuits would invert the signal and the ladder network converts the resultant signal into a programming current, the value of which is +.39995mA. The polarity offset switch is turned off by the negative sign program input, thus no current is drawn from TP56. The +.39995mA is amplified and inverted by the power amplifier and the result of this will be -4 volts at the output terminal (again, the power amplifier has a +0.05µA offset).

4-40 POWER AMPLIFIER

4-41 The precision power amplifier consists basically of three major stages; a feedback differential amplifier, coupling amplifier, and power amplifier. Negative feedback is employed, from output to input, creating a near zero impedance summing junction at the input of the feedback differential amplifier. The amplifier provides an output of -1 volt for every 100µA of input current ($E_{OUT} = -10,000 \times I_{IN}$) in the X1 range or -10 volts for every 100µA of input current ($E_{OUT} = -100,000 \times I_{IN}$) in the X10 range. Hence, in the X1 range, the D/A converter supplies its maximum input current of approximately ±1638.4 microamperes to obtain a ±16.384 volt output. For the X10 range, however, the D/A converter need provide only ±500µA to attain the maximum rated output of ±50 volts. If a number larger than 50 is programmed in the X10 range, the additional D/A input current has little effect on the output because the output of the amplifier is internally limited to approximately (110%) 55 volts.

4-42 Feedback Differential Amplifier. This circuit amplifies and inverts the D/A output and/or analog input signal before applying it to the coupling amplifier. It provides most of the voltage gain of the overall amplifier. Negative feedback is employed with an equalizing network which shapes the high frequency responses for stability purposes.

4-43 Voltage Range. A range input from the voltage range processing circuits controls the operation of the range relays which, in turn, determine the impedance of both the equalizing and main feedback networks. In the X1 range, the relays are energized reducing the impedance of the feedback networks and thus increasing the amount of negative feedback through both networks. In the X1 range the overall amplification is multiplied by a factor of 1. In the X10 range, the relays are deenergized, multiplying the amplification by 10.

4-44 Coupling Amplifier. This inverting stage couples the input stage of the overall amplifier to the power amplifier stages which are at a much higher power level. The voltage and current gain of the coupling amplifier is minimal.

4-45 Power Amplifier. The power amplifier stage furnishes most of the current gain of the overall amplifier. The output stage is a class AB, push-pull complementary connected amplifier which produces the positive or negative output voltage. The output, at the high sense terminal, is fed back to the input of the overall amplifier resulting in a constant output voltage which is independent of load variations.

4-46 Current Latch Input. The current latch signal is received from the latch processing circuits if the preselected current latch value is exceeded. An isolating oscillator first isolates the power amplifier from the current latch circuit. The isolator output then activates the current latch switch which turns off the power amplifier.

4-47 Under current latch conditions, the non-conducting power amplifier presents an impedance of approximately 20K Ω in series with the high output terminal. The output current is limited to between 0 and approximately 10mA, depending on the programmed output voltage and the type of load.

4-48 Gross Current Limit. The positive and negative gross current limit comparators provide additional current limit protection. They are fixed to operate at the maximum current limit of approximately $\pm 1.1A$ providing protection for the DVS and the load during the variable current latch delay period or in the event of failures in the current latch circuit.

4-49. The comparators each monitor the voltage

drop across the current sampling resistor. Since the IR drop across the sampling resistance varies in proportion to the output current, both comparators effectively monitor the output current of the DVS. The use of two comparators allows sampling of output current flowing in either direction; with the negative gross current limit comparator monitoring negative output currents, and the positive comparator monitoring positive output currents. For normal source currents (below the $\pm 1.1A$ threshold) the comparators are biased below cutoff and do not influence amplifier operation. However, if the gross current limit threshold is exceeded, the appropriate comparator conducts sending a gross current limit signal to the coupling amplifier. This signal turns down the coupling amplifier, and hence the power amplifier, preventing the output current from exceeding the maximum current limit. For sink currents, the trip point is reduced.

4-50 Disconnect Interlock. A disconnect interlock relay provides load protection by shorting the output of the DVS whenever the computer cable is disconnected or source power is interrupted. Under these conditions, the relay is deenergized (as shown on Figure 7-1) and contacts of the relay short the output terminals. The output is also shorted at turn-on (for approximately 0.2 seconds) and turn-off of the unit which protects the load from possible transients during these times. For normal operating conditions, the relay is energized removing the short between the output terminals and connecting the interlock signal (Z) to the current latch and voltage processing circuits.

4-51 Metering Circuits. The metering circuits provide continuous indications of output voltage and current on the front panel meters. The meters operate in conjunction with front panel range switches and appropriate resistive voltage dividers to permit voltage display in one of two ranges and current indications in one of three ranges.

4-52 CURRENT LATCH AND VOLTAGE RANGE PROCESSING

4-53 These circuits are located on the control board A6. They consist of input isolating circuits, storage, decoding, current sampling and current overload circuits. The circuits will be described functionally based on signal flow from input to output.

4-54 Input Data. The current latch data input from the computer consists of a three bit binary code which is shown in Section III of this manual. This code establishes the point at which the DVS will current latch. The voltage range data input is a single binary bit which determines the voltage range, X1 or X10.

4-55 Input Isolators. Four input isolator circuits, identical to the voltage magnitude input isolators described above, are utilized. They provide the logic interface and dc isolation for the current latch and voltage range data signals from the computer.

4-56 Storage and Storage Disable. In store mode, the three bits of current latch data (TP74) are stored in flip-flops along with the one bit of voltage range data (TP76). These storage flip-flops are enabled by the storage gate and are identical to the ones used in the voltage processing storage circuit. If the storage disable switch in the voltage processing circuit is in the DISABLE position, these flip-flops as well as those in voltage processing are disabled and pass data directly through without storing it. The three current latch data output lines from storage (TP75) are applied to the current latch decoder and the voltage range storage output (TP73) to the range pulse generator.

4-57 Current Latch Decoder. The current latch decoder generates a reference voltage for each of the eight current latch bit combinations. As just mentioned, the current latch bits are received from storage. The incoming bits are first converted to an analog reference current which is then used to develop the negative reference voltage. This voltage is fed directly to the negative current comparator and to the negative reference inverter which provides an equal amplitude, opposite polarity reference voltage to the positive current comparator.

4-58 Current Comparators. The positive and negative current comparators compare a sample of the output current (voltage drop across the current sampling resistance) with the negative or positive reference. If the IR drop across the sampling resistance equals, or exceeds, the reference voltage, an overload signal (TP17-Figure 4-3) is generated. The polarity of the output current determines which of the comparators is activated. The overload signal is fed both to the current overload circuits (isolator and overload flag generator) and the current latch circuit (variable delay). Once the unit switches to the current latch mode, the output current is reduced to under 10mA and the current overload signal at TP17 reverts to its normal state.

4-59 Current Overload Circuits. The current overload circuits comprise an isolator, output amplifier, and overload flag generator. The isolator, a photo isolator of the type used throughout the DVS, provides dc isolation between the computer and the DVS. The output amplifier interfaces the DVS overload circuits with the computer receiver circuits by providing an overload status signal (TP25) of the proper magnitude and

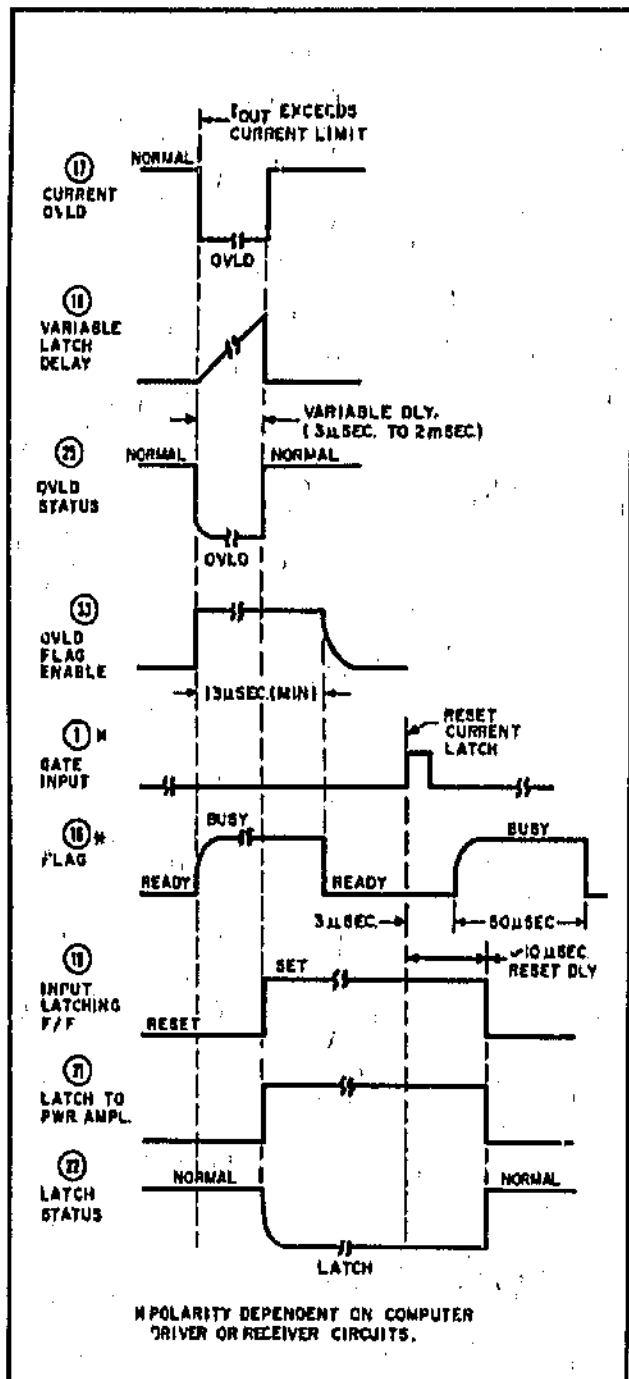


Figure 4-3. Current Overload and Latch Circuits, Timing Diagram.

polarity.

4-60 The overload flag generator provides a 10µsec wide flag enable output signal (TP33) at both the leading and trailing edges of the current overload signal at TP17. The first trip signal indicates the start of an overload while the second denotes that current latch has occurred. If the variable delay period is less than 10µsec, note that the trip signals at TP33 will overlap and

appear as one signal. Since the minimum latch delay is approximately 3 μ sec, the minimum trip signal width is 13 μ sec. The overload flag trip signals are OR'ed with the voltage range flag signal and then applied through a photo-isolator and an output amplifier to the voltage processing circuits. This signal (overload/range flag enable) is applied to an OR circuit in the voltage processing circuits which in turn generates the flag signal which is applied to the computer through another photo-isolator and an output amplifier/inverter circuit.

4-61 Current Latch Circuits. These circuits are composed of a variable delay, level detector, latching flip-flop, reset amplifier, isolator, and output amplifier. If a current overload condition persists for a certain preset delay period, these circuits generate a current latch signal. The current latch signal ultimately biases the power amplifier to cut-off, or near cutoff, limiting the output current to less than 10mA. A current latch indicator signal is also generated if a current latch condition occurs.

4-62 The variable delay circuit delays the fall time of the current overload input (TP17). The degree by which the leading edge of this signal is retarded, determines the current latch delay period. The variable delay circuit operates in conjunction with the C_T terminals on the rear of the unit. As mentioned previously, the condition of these C_T terminals determines the current latch delay. With the C_T terminals open, a natural delay period of from 3 μ sec to 10 μ sec results. If the user connects a capacitor across the C_T terminals, the current latch delay period can be extended from 5 μ sec to 2msec at the rate of approximately 1 μ F per msec. The user can also disable the current latch circuits by shorting the C_T terminals. This disables the variable delay circuit preventing the generation of the current latch signals to the power amplifier and computer. The user could employ this method during testing or troubleshooting when the unit is "off line", or in any case where programmable latching is not desired.

4-63 When the input at TP18 (Figure 4-3) becomes sufficiently positive the level detector (a Schmitt trigger) is activated. The positive going output (TP19) sets the latching flip-flop which, in turn, provides a current latch signal (TP21) to the power amplifier and a latch status signal (TP22) to the computer via an isolator and output amplifier. Similar to the other output circuits in the DVS, this amplifier issues a latch status output signal which is of the polarity and amplitude necessary to interface with the computer receiver circuits.

4-64 The latching flip-flop remains set until approximately 10 μ sec after the next gate input (TP1) is received from the computer. The leading edge

of the 50 μ sec delayed signal (TP7) is amplified and used to reset the flip-flop. Notice that if the current overload still exists after the latch is reset, the entire current overload and current latch process is repeated and the unit will again revert to the current latch state.

4-65 Voltage Range. The voltage range circuits consist of a range pulse generator and a 2msec delay circuit. The voltage range, similar to the current latch, is established by the voltage range data bit from the computer. The range pulse generator provides two outputs; one for the range relays in the power amplifier and the other for the generation of a voltage range flag signal to the computer. If the input voltage range bit calls for the X1 range, the range pulse generator connects a common to the power amplifier range relays to energize them. In the X10 range, the range relay lead is open and the relays are deenergized. The range pulse generator also provides a negative output pulse for each positive or negative transition of the voltage range input. The positive going output triggers a 2msec delay circuit which provides the voltage range flag signal. This signal is OR'ed with the overload flag signal and applied to the voltage processing circuits through a photo-isolator and an output amplifier. The overload/range flag enable output signal drives the flag OR circuit in the voltage processing circuits. An example of a voltage range flag is shown on Figure 3-5. The 2msec delay period allows time for operation of the range relays and for processing of the voltage range input bit.

4-66 DETAILED CIRCUIT ANALYSIS

4-67 VOLTAGE PROCESSING (See Figure 7-2, Sheet 1)

4-68 Input Isolator Circuits. The input isolator circuits (A1-A15) for the fifteen voltage data bits and for the sign bit (A17) are all identical. They employ light-emitting-diode/phototransistor isolators to eliminate dc paths between the computer and the DVS output. A biased attenuator network (R1, R2, and R3) makes it possible, by selecting appropriate values, to adapt to any of the three standard binary interface options, or, through resistor choice and/or resistor bias polarity, to adapt to other driver circuits as required, whether NPN or PNP. The logic convention of the source may either be positive true or negative true (See Figure 4-4). The voltage levels and circuit details for the inputs (and outputs) of instruments having any of the standard options are given in the appropriate Option Appendix in the back of this manual. Interface information for other instruments is given on the Instrument Modification Sheet included with the instrument.

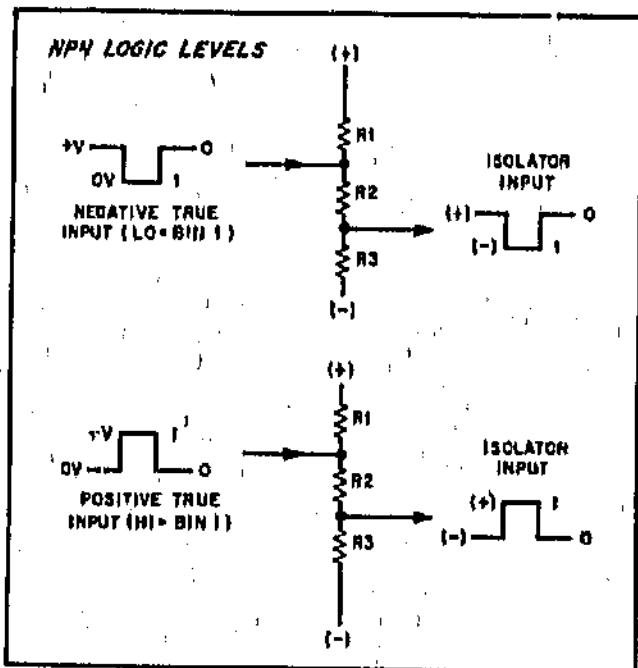


Figure 4-4. Input Voltage Divider Networks

4-69 When the input (TP10) is at its more positive level, Q1 is turned on and energizes the LED in photo-isolator assembly Z1. The photons emitted by the diode cause the phototransistor to conduct, turning on Q2 to apply a low to the data input (TP13) of the storage flip-flop for that data bit. CR1 and R5 form a low impedance lead for the photo-transistor to minimize its switching time. A more negative level from the computer produces a high input to the flip-flop. Note that a signal level inversion occurs between the isolator input and output.

4-70 Storage. When a high level is present at the clock inputs of the storage circuits, the level present at the data inputs appears at the Q outputs and the complement of that data at the \bar{Q} outputs. Whatever data is present when the clock input becomes low is stored in the flip-flops and continues to appear at the outputs until the next high clock input occurs. In STORAGE DISABLE mode, the clock input remains high. The logic board has two sets of four sockets for these IC packages. One set is designated Z1 through Z4 and connects the inverting (\bar{Q}) outputs. The other, Z9 through Z12, connects the non-inverting (Q) outputs. The proper choice of sockets for these IC's depends on the interface requirements of the DVS and whether an inversion of the voltage magnitude bits is needed. The fifteen voltage magnitude outputs from storage to the D/A converter must be low for those bits that are true. The voltage sign output from storage must be low for

a positive output voltage and high for a negative one. Since one inversion occurs at the input isolators, negative true voltage magnitude inputs from the computer require the use of the inverting Z1 through Z4 sockets and positive true inputs require the non-inverting Z9 through Z12 sockets to be used. The proper polarity of the sign bit is obtained by positioning jumper W1 in the B position for positive = HI inputs and the A position if the input is positive = LO.

4-71 Gate Input and Timing. In instruments equipped with one of the standard options, the gate input from the computer (TP1) is a negative-going transition. A biased attenuator network (R1, R2, and R3) identical to those of the voltage and sign bit inputs adapts the gate input to the interface requirements of the driver circuit. Inverter Q2 provides the positive-going transition needed at the input (TP3) of one-shot multivibrator Z3, which has a Schmitt trigger input sensitive to positive levels. For special modifications, an additional inverting stage that is normally jumpered out may be added ahead of Q2 to accommodate a positive-going input gate. The 3-microsecond duration of the negative pulse at the output of Z3 (TP4) is determined by the values of R7 and C5. The trailing edge of the negative 3-microsecond pulse triggers another one-shot multivibrator identical to the first except that its timing components, R8 and C6, cause it to produce an output pulse 50-microseconds long. Multivibrator Z4 produces a negative 50-microsecond pulse at its Q output (TP6) and a positive 50-microsecond pulse at its \bar{Q} output (TP40). Both of these pulses start 3-microseconds after the start of the incoming gate. The negative output (TP6) drives the light-emitting diode of the gate pulse isolator circuit. This isolator circuit, similar to those used for the voltage magnitude inputs lines, produces a negative output pulse (TP7). This pulse is inverted by part of A225 in order to obtain the positive-going transition (TP43) needed to drive another one-shot multivibrator, A226-A226 is identical A123 and A124 except that its timing components are chosen for a 2-microsecond output pulse (TP8).

4-72 If the storage disable switch is in the STORAGE position, this 2-microsecond positive pulse is applied to one of the inputs of the OR gate composed of Q1, Q2, and Q3. The output of the OR gate (TP9) is a positive 2-microsecond storage gate to the clock inputs of the voltage magnitude and sign flip-flops. This output is also inverted by another section of A225 and sent to the current latch and voltage range processing circuits to control the storage flip-flops there. The other input of the OR gate is connected to an r-c

differentiating network that produces a 20-millisecond pulse when the instrument is energized. This pulse assures that the A2 and A6 storage flip-flops are in the desired initial state.

4-73 If the storage disable switch is in the STORAGE DISABLE position, an input gate does not produce a storage gate. The pulse input to the OR gate is disconnected by the switch and Q1 is saturated by the current through R6. The continuously high output from Q2 keeps all of the storage flip-flops enabled so that data inputs are reflected at the flip-flop outputs continuously. Placing the switch in STORAGE DISABLE also lights the STORAGE DISABLE lamp.

4-74 The other output of multivibrator A1Z4, the 50-microsecond positive pulse (TP40) mentioned above, is one of two input signals to an OR gate consisting of A1CR1 and A6CR20. The other input will be discussed under current latch and voltage range processing. The output of this OR gate (TP31) feeds the flag isolator, which is similar to the input isolators described above. In this instance, the isolator is not used to isolate the computer from the DVS output, since the input and output are both referenced to common (3). Here it is used to make it possible to shift the dc level of the output stage so that it can interface with either an NPN or a PNP receiver circuit.

4-75 Following Q5 of the flag isolator are two optional amplifier/inverter stages, Q6 and Q7. The standard options either include an NPN Q6 stage as an inverter, if that option requires a ready = LO and busy = HI output, or else leave Q6 out if the reverse logic sense is required. Other instrument modifications may require an NPN or a PNP output of either logic sense. To provide an PNP output, jumpers W1, W2, and W3 are connected so that the entire output side of the isolator is connected between -12 volts and common (3) and PNP transistors are used for Q6 and Q7. Circuit details depend on interface requirements. Refer to the appropriate Option Appendix or the Instrument Modification Sheet for this unit.

4-76 Digital-To-Analog Converter. The digital-to-analog circuits consist of bit switches and ladder networks, a polarity offset switch and two reference voltage circuits. The D/A converter provides discrete output currents as determined by the voltage magnitude input bits from the storage flip-flops.

4-77 D/A Bit Switches and Ladder Networks. This circuit is composed of four similar sets of bit

switches and resistive ladder networks (one per bit). The switching circuits consist of transistors A3A2Q1-3 through A3A16Q1-3 while the analog ladder networks consist of resistors A3R50 through A3R96. Since all four networks are similar, only the network for the four most significant digits is described in the following paragraphs.

4-78 The bit switch network consists of a driver, Q1, and two low-saturation switching transistors, Q2 and Q3. With a voltage program input of +4 volts (00111101000000), the D/A Board switching circuits receive the complemented input of 12.3835 (11000001011111). The high inputs (the digits which have a value of binary 1; A16, A15, A9, etc.), at the base of Q1, are inverted and, through steering diode CR1, cause Q2 to turn on placing a +16.384V on the input line to the ladder network. The low inputs (the digits which have a value of binary 0; A14, A13, A12, etc.), at the base of Q1, are inverted and, through steering diode CR2, cause Q3 to turn on placing 0V (ground) on the input line to the ladder network.

4-79 In the simplified schematic of Figure 4-5, the switching transistors are represented by mechanical switches connecting each of the four rungs in the analog ladder network to either 16.384V or ground (2). Again, the switch positions represent the binary input of 1100, the four most significant bits of the inverted input of 4 volts.

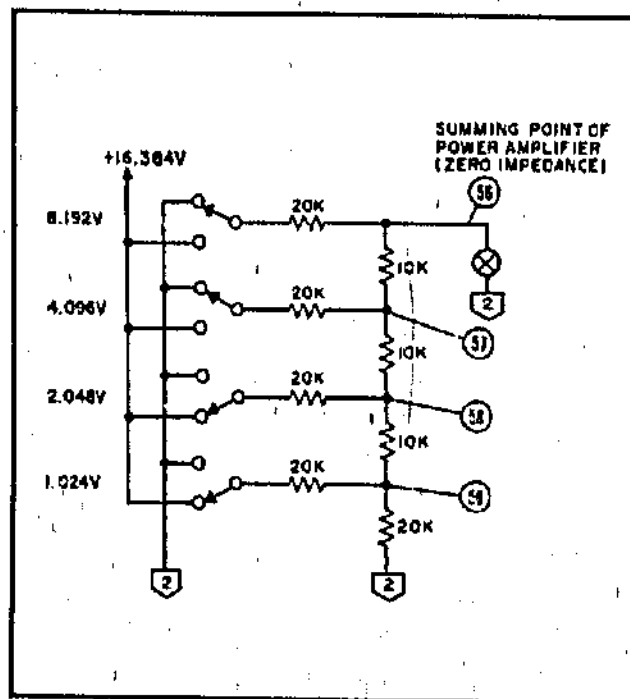


Figure 4-5. Ladder Network, Simplified Schematic

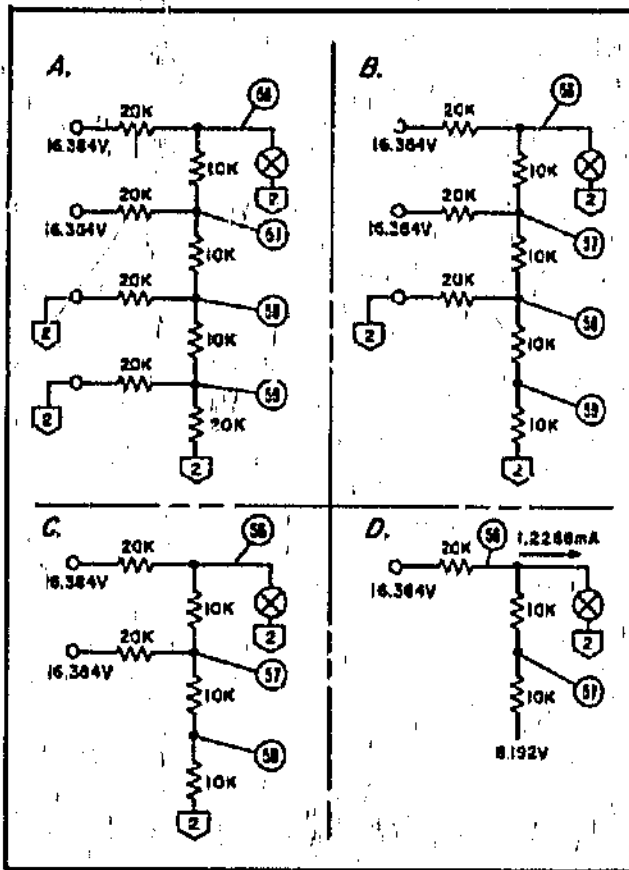


Figure 4-6. Ladder Network Thevenin Equivalents

4-80 Figure 4-6A shows the voltages at the input of each rung. To determine the current flowing into the summing point (X) from the ladder network, a Thevenin Equivalent can be constructed for each rung. If the circuit is broken above TP59, the open circuit voltage at TP59 is 0V and the impedance looking into TP59 is 20K in parallel with 20K or 10K. Thus, the Thevenin Equivalent is 0V (ground) in series with 10K, as shown in Figure 4-6B. Breaking the circuit at TP58 and replacing this portion by its Thevenin Equivalent, we have the circuit shown in Figure 4-6C. Now, breaking the circuit at TP57 and solving for the voltage at this point ($16.384 \times \frac{20K}{40K} = 8.192V$), we are left with the circuit shown in Figure 4-6D. This figure shows that the current flowing into the summing point (TP56) is 1.2288mA.

4-81 The currents flowing into the summing point from the other three ladder networks may be solved in the same manner and the results will be 0.0064-milliamperes, 0.0028mA and 0.0035mA. Summing all four currents together yields a final result of 1.23835mA total flowing into TP56 from the ladder network. As described previously, the +1.23835mA output of the ladder network is summed with -1.6384mA from the polarity switch yielding a net

input to the power amplifier of -0.40005mA. A continuous offset current of +0.05mA at the operational amplifier input yields an effective power amplifier input of -0.40000mA. The power amplifier amplifies this current to produce a +4V DVS output voltage.

4-82 Potentiometers A3R52 through A3R59 are adjusted to compensate for the conducting resistances of Q2-Q3 and resistance tolerances within the network. With these controls properly adjusted, the total series resistances in each rung are 20K Ω as shown in Figures 4-5 and 4-6. Notice that the output current of each of the four ladder networks are weighted in powers of 16. Thus, resistor A3R92 divides the output current of that rung by 16, resistors A3R93, R94 divide the next rung output current by 256 and resistors A3R95, R96 divide the output current of the remaining rung by 4096.

4-83 Polarity Offset Switch Circuit. This circuit consists of amplifier A3Q13 and switch A3Q14. A constant reference of -16.384V is supplied to the emitter of switch Q14. With a negative sign input A3Q13 receives a high level input signal and switch A3Q14 does not conduct. With positive input sign, however, Q13 receives a low input causing Q14 to saturate. A path for the offset current of 1.6384mA is now completed to the summing point. Potentiometer A3R100 provides a means of adjusting the offset current.

4-84 D/A Converter, +16.384 Volt Reference Circuit. This circuit provides a regulated output voltage of +16.384Vdc. To maintain the output voltage constant, a series regulating feedback loop is employed. A reference comparator circuit, AR-Z1, compares a portion of the output voltage (across divider R34, R36, and AR-R3) with an internal zener diode reference voltage. If a difference exists, the comparator sends an error signal to series regulator Q31 via driver Q32. This error signal is of the phase and amplitude necessary to counteract the original difference. Transistor Q30 provides a constant biasing current to Q32 and AR-Z1. Potentiometer R36 can be adjusted to alter the voltage divider resistance and thus, the +16.384V output. Output capacitor C30 stabilizes the feedback loop.

4-85 D/A Converter, -16.384 Volt Reference Circuit. This regulator circuit is similar to the +16.384V reference supply except that the -16.384V reference supply utilizes the regulated +16.384V as one of its dc inputs in a kind of "Auto-Tracking" configuration. With this technique, any change in the +16.384V output causes an equal percentage change in the -16.384V output thereby minimizing inaccuracies in the D/A converter due to drift or other disturbances.

4-86 The -16.384V reference supply contains a series regulating feedback loop composed of: comparison amplifier Q11, error amplifiers Q12 and Q15, and series regulator Q10. Incipient changes in the -16.384V output are detected by Q11B, amplified by Q12 and Q15 and applied to the series regulator. Feedback loop stability is maintained by output capacitor C13 and feedback network C12, R21.

4-87 +21.5 Volt Regulator. A regulated +21.5 volts is obtained from series regulator AJC40 and zener diode VR40 which keeps the base voltage of Q40 at a constant level.

4-88 CURRENT LATCH AND VOLTAGE RANGE PROCESSING (See Figure 7-2, Sheet 2)

4-89 Input Isolator Circuits. The four input isolators (A6A) through A6A4) for the latch bits (range, 50mA, and 30mA) and the voltage range bit are identical to those used in voltage processing (refer to paragraph 4-68). The current latch range (X1 or X10) input bit (L24) is at a positive level for the X1 range and a more negative level for the X10 range. The 30mA and 50mA bits (L22 and L23) of current latch data must be in LO = true, negative logic form. For example, when the 30mA input (L22) is LO (more negative level), the 30mA bit is present, and when the 30mA input is HI (more positive level), the 30mA bit is absent. The voltage range input bit is at a more negative level for the X1 range and a positive level for the X10 range. The input isolators invert these input levels.

4-90 Storage. The current latch and voltage range storage flip-flops (A6Z2) are identical to those used on board A2 in voltage processing. When a high storage gate level is present at the clock inputs to the storage flip-flops, the levels present at the data inputs appear at the Q outputs and the complement of that data at the \bar{Q} outputs. Whatever data is present when the storage gate (clock) input becomes low is stored in the flip-flops and continues to appear until the next high clock input occurs. In the storage disable mode, the clock input remains high, and the flip-flops pass the data bits directly through to the current latch decoder and range pulse generator without storing them.

4-91 Storage Gate. The storage gate circuit develops the clock signals for the storage flip-flops. The storage gate signal is received from the logic board in the voltage processing circuits and is applied to the base of Q4 through speed up network (C) and R62). Q4 and R63 comprise a level setting circuit to provide the proper interface with the logic board. Note that the emitter of Q4 is returned to (4) (-26V) while the emitters of Q5

and Q6 are connected to (2) The storage gate signal is inverted by Q5 and again by Q6 to provide the proper clock level to the storage flip-flops.

4-92 Current Latch Decoder. This circuit converts the three coded current latch bits to an analog output current. Eight possible analog output currents can be obtained; one for each of the eight current latch bit combinations. The output current of the current latch decoder appears at a current summing junction (collectors of A6Q11, Q12, and Q13) and is determined by the conduction of these transistors. The resultant current at the junction flows through A6R30 and A6R37 to develop negative and positive reference voltages, respectively, for the comparators.

4-93 Current latch range is determined by the range bit which turns on A6Q1 in the X1 range and turns off A6Q1 in the X10 range. With Q1 on, (X1 range) a path is completed for the voltage divider network (R8-R13) in its collector circuit. Bias voltages which are less positive now permit transistors Q8, Q9 and Q10 to conduct effectively shorting out resistors R16, R17, and R18, respectively, in the base circuits of Q11, Q12, and Q13. This action insures that the conduction of Q11 is decreased by a factor of 10. If transistors Q12 and/or Q13 are conducting, their conduction is likewise 10x less than that of the X10 current latch range.

4-94 Transistor Q11 is biased in its active region and always conducts one of two fixed amounts of reference current to the summing junction. As just described, the two fixed currents vary by a factor of 10 and depend on the status of the current latch range bit.

4-95 Transistors Q12 and Q13 may, or may not, be conducting depending on the status of the 50mA and 30mA current latch input bits. If transistor Q2 is conducting, Q14 is cut off and Q12 (50mA stage) does not conduct. Under these conditions, no reference current is supplied to the summing junction by Q12. Conversely, when Q2 is cut off, Q12 is allowed to conduct one of two fixed amounts of current as determined by the current latch range bit. Transistor Q13 (30mA stage) is controlled in a similar manner by the 30mA bit and the range bit.

4-96 To better illustrate the action of this circuit, assume that the programmed current latch is 20mA (the three current latch data inputs are all HI). In this case, transistor Q12 and Q13 are not conducting because of high level inputs to Q2 and Q3. Transistors Q1 and Q8 are conducting thus limiting the conduction of Q11 to its X1 range value. If a 200mA current latch is programmed (same as above except current latch range data input is LO),

transistors Q12 and Q13 are cut off, as before, but range transistor Q1 is not conducting. This cuts off Q8 and the conduction of Q11 is increased to its X10 value.

4-97 Negative and Positive Current Comparators. The current comparators compare the voltage drop across current sampling resistor A5R5 (proportional to the output current) with the voltage drop across A6R30 or A6R37 (proportional to the current latch value). If the output current equals or exceeds the current latch reference value, one of the 24 comparators (positive or negative) generates a negative going current overload signal to turn on the appropriate OR gate diode (CR1 or CR2). The polarity of the output current determines which of the comparators is activated. The positive current comparator (Z4, R32, R34, R43) is activated for positive output currents to monitor the difference between the output and latch reference current. The current sampling signal (J6-N) is one input to the positive current comparator and the positive reference signal is the other input. The positive reference signal is developed by the negative reference inverter (Z3 and Q23). For excessive positive output currents, the positive current comparator generates a negative going output signal causing CR2 to conduct. The negative current comparator (Z4, R31, R33, R39) is activated for negative output currents to monitor the difference between the output and latch reference currents. The current sampling signal is one input to the negative current comparator and the negative reference signal is the other input. For excessive negative output currents, the negative current comparator generates a negative going signal causing CR1 to conduct. With CR1 or CR2 conducting, an overload signal is passed to the current latch and current overload circuits.

4-98 Current Latch Circuits. If a current overload signal is generated, these circuits generate a current latch signal which turns off the power amplifier. The latch output signal is not generated until after variable delay period has elapsed. The delay ranges from approximately 3 μ sec to 2msec. Variable delay stage, 16, receives the overload signal and, if the C_T terminals are open, passes the inverted signal on to Q17 with a minimal delay (less than 1 μ sec). Under these conditions, the latch delay period is dependent solely on the natural circuit delays of the level detector, latching flip-flop, current latch switch, and the power amplifier (see Sheet 3). The time required to initiate turn-off at the power amplifier with the C_T terminals open is approximately 3 to 10 μ sec.

4-99 For greater latch delays, a capacitor can be connected across the C_T terminals. When Q16 is cut off by the negative going overload signal, the

positive going slope on its collector is now determined by the time taken by capacitor C_T to charge through R42. Hence, increasing the value of C_T increases the latch delay period.

4-100 Shorting the C_T terminals places the collector of Q16 at 0 potential preventing Q17 from conducting. This prevents the unit from operating in the current latch mode. Note that if the unit is already in the current latch mode shorting the C_T terminals will not transfer it out of current latch.

4-101 Level Detector. Transistors Q17 and Q18 form a Schmitt trigger circuit which switches state when the positive going input signal reaches the threshold level. Transistor Q17 conducts when the threshold is reached biasing Q18 below cutoff. The positive going rise on the collector of Q18 is then coupled through limiting diode CR9 to set the latching flip-flop. When current latch commences, the Schmitt trigger input goes negative cutting off Q17 and returning the circuit to its original state. The latching flip-flop remains in the set state, however, because diode CR9 blocks the negative going excursion of the collector of Q18.

4-102 Latching Flip-Flop. Transistors Q19 and Q20 are connected in a bi-stable multivibrator configuration. When the DVS is not in a current latch condition, the flip-flop is in the reset state with Q19 off and Q20 on. Reset is initiated by a short duration negative pulse applied to the base of Q20 by reset amplifier Q24. The reset pulse is generated 3 μ sec after the application of a gate input from the computer. The leading edge of the 50 μ sec wide input from input board A1 cuts off Q22. The output of Q22 is differentiated by A6C4 and A6R52 and the positive going spike that occurs at the leading edge of the input is inverted by Q24 and then used to turn on Q20.

4-103 A current latch condition is initiated by a positive going transition applied to the base of Q20 from the collector of Q18. This sets the flip-flop by turning Q20 off causing Q19 to turn on. The flip-flop remains in the set state until a gate pulse is received from the computer and a reset pulse is generated by Q24.

4-104 The latching flip-flop is also set when the shorting relay (A4K1) is deenergized (Figure 7-2, Sheet 3). This ensures that the power amplifier is turned off when the output terminals are shorted by contacts of relay A4K1.

4-105 Buffer and Current Latch Status Circuits. The buffer amplifier (A6Q21) inverts the negative going latch signal from Q20 and applies it to the power amplifier (Figure 7-2, Sheet 3) and to the

latch status isolator/output amplifier (A6A5). The isolator (A6A21, Q1, Q2) is similar to the input isolators previously described. The latch status isolator provides a LO output to indicate latched status and a HI output for normal condition. The output amplifier stages A6A5Q3 and A6A5Q4 that follow A6A5Q2 provide sufficient current drive and proper signal inversion to interface with the computer. Circuit details depend on interface requirements. Refer to the appropriate Option Appendix or the Instrument Modification Sheet for this unit.

4-106 Current Overload Circuit. The current overload circuits consist of an overload flag generator, isolator, output inverter, and a overload status isolator/output amplifier circuit. If the current latch value is exceeded, the negative going overload signal at TP17 is applied to the overload flag generator and to the overload status isolator and output amplifier circuit.

4-107 Overload Flag Generator. The overload flag generator consists of two emitter coupled amplifier stages A6Q29 and A6Q30. The collector stage of each amplifier contains a differentiating network (C13, R95 and C14, R94) and a limiting diode (CR14 and CR15). The limiting diodes conduct only the positive excursion of the differentiated waveform from the respective collector. These diodes also serve as part of the flag enable OR gate along with A6CR16 which receives the voltage range flag. The first output pulse from the overload flag generator is obtained from the collector of Q29. It is initiated by the negative going overload signal (begin current overload) which turns off Q29 turns Q30 on. This causes a negative voltage change at the collector of Q30 and a positive change at the collector of Q29. The positive portion of the differentiated Q29 output is conducted by CR14 while the negative portion of this waveform and the output of Q30 are blocked. The component values of the differentiating network determine the 10 μ sec width of the conducted pulse. The trailing edge (begin current latch) the overload signal turns Q29 on and Q30 off resulting in a second 10 μ sec pulse at TP33 through CR15. This pulse is obtained from the collector of Q30 and is a replica of the first overload pulse.

4-108 Figure 4-7 illustrates the output pulses obtained from the flag generator (TP33) for a current latch delay of 20 μ sec. Because the output pulses from the flag generator have a fixed width of 10 μ sec, the output waveforms at TP33 will merge if the current latch delay is less than approximately 10 μ sec. For example, if the current latch is 10 μ sec, the waveform at TP33 consists of a single pulse having a width of approximately 20 μ sec.

4-109 Overload/Range Flag Isolator and Inverter. The positive (high) output from the OR gate (TP33)

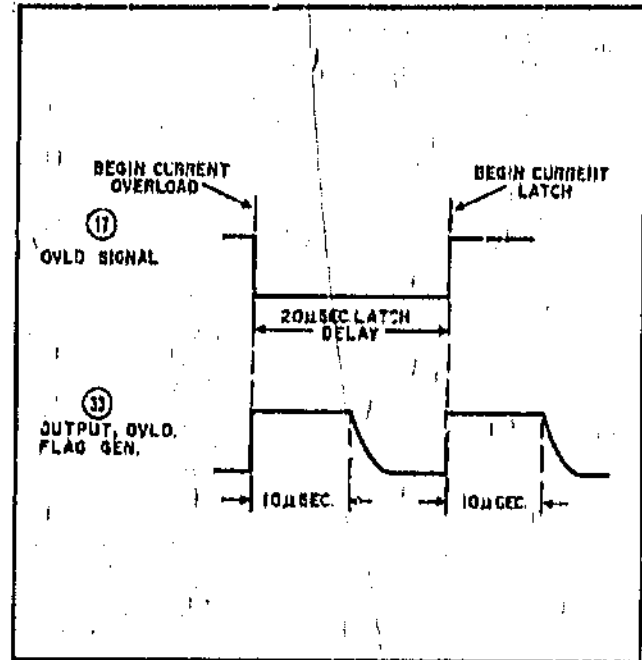


Figure 4-7. Overload Flag Generator Output With 20 μ sec Latch Delay

is applied to the overload/range flag isolator and inverter circuit. The photo-isolator circuit (A6Q31, Z5, Q32) is identical to those previously described. The low output at the collector of Q32 is applied to the base of inverter Q33 which produces a high at the collector of Q33 which is conducted through A6CR20. Diode A6CR20 along with diode A1CR1 comprise an OR gate input to the flag isolator and output amplifier/inverter circuit (Figure 7-2, sheet 1).

4-110 Overload Status Isolator and Output Amplifier. The overload status isolator and output amplifier (A6A6) is similar to the latch status isolator and output amplifier (A6A5), described in paragraph 4-105. For a latch condition, the input to A6A5 is positive causing A6A5Q2 to conduct. For an overload condition, the input to A6A6 is negative causing A6A6Q7 cutoff. Inverter A6A6Q3 provides a LO output to indicate an overload status. Stage A6A6Q4 is omitted for the standard options.

4-111 Voltage Range Circuits. The voltage range circuits energize or deenergize the voltage range relays in the power amplifier and also provide a 2msec wide flag output to the computer whenever the voltage range is changed. For the X10 range, the range input bit is a positive level causing the range storage flip-flop to provide a negative input to the base of Q25 (range pulse generator). This holds Q25 off, opening the collector lead which is connected to the range relay coils (Sheet

3) via A5J6, pin D. Hence, in the X10 range the relays are deenergized,

4-112 For the X1 range, the range input bit is a negative level causing the range storage flip-flop to provide a positive input causing Q25 to conduct coupling 2 common to the range relay coils to energize them. Differentiating networks and limiting diodes (Q8, R74, CR12 and Q9, R75, CR13) in the base and collector circuits of Q25 couple positive going transitions to the base of Q26 in the 2msec delay circuit whenever a change in range occurs.

4-113 The 2msec delay circuit is composed of transistors Q26 and Q28, connected in a type of one-shot multivibrator configuration, and transistor Q27 which provides current gain between the one-shot stages. In the stable state, transistors Q28 and Q27 are conducting and Q26 is held off due to the voltage drop across common emitter resistor, R81. Coupling capacitor C11 charges up to nearly +15V through conducting transistor Q27. When a range change occurs, a positive going transition is received from the range pulse generator. The multivibrator now is driven into its unstable state with Q26 on and Q27, Q28 off. It remains in the unstable state for approximately 2msec until C11 discharges (through R82 and R83) sufficiently to allow the conduction of Q28. The range flag enable output is coupled to the flag output circuit (Sheet 1) via OR gate diode A6CR16.

4-114 POWER AMPLIFIER (See Figure 7-2, Sheet 3)

4-115 Feedback Differential Amplifier. This circuit consists of three differential amplifier stages followed by a single-ended stage. The first two stages (A7Q1 and A7Q2) each consist of two silicon transistors housed in a single package. The transistors have matched characteristics to minimize differential voltages due to mismatching or thermal drift.

4-116 Diodes A7OR3 and A7OR4 protect the input stage, Q1A, from being overdriven by excessive inputs from the D/A Converter and/or the external analog input. Voltage divider A7R1, R2, and R3, connected to the base of the input stage, provides a zero reference bias with no applied input signal. The voltage magnitude input from the D/A converter is summed with the external analog input and the resultant analog current applied to the base of the differential amplifier input stage. The collector circuits of each of the first three differential amplifiers contain RC networks (C1, R6-C2, R16-C4, R25) which help prevent amplifier oscillations. Potentiometer A7R9, in the base circuit of Q1B, can be adjusted to compensate for slight differences between the two base voltages of the input stage,

thus zeroing the output voltage.

4-117 The output of the feedback differential amplifier is taken from the collector of A7Q5 and applied to the coupling amplifier, A7Q6. Negative feedback is employed, from the collector of Q5 to the base of Q1A, for equalization purposes. Zener diode VR7 improves the response time of the feedback amplifier by its clamping action at the collector of Q5.

4-118 Range relay A7K2 switches in the proper value equalizing network for each range; C22 and R88 in the X10 range, or these components in parallel with Q23 and R89 in the X1 range. Relay A1K1 changes the range by changing the overall feedback resistance by a factor of 10. The overall feedback line, from the high sensing terminal to the base of Q1A, contains resistors R85, R86, and R87. In the X10 range, in the X1 range, the relay is energized thus shorting out R85 and R86.

4-119 The normal output voltage swing at the collector of Q5 is between +1 volt and -6 volts. These two extremes represent output voltages +50V and -50V, respectively. Q5 provides an output of approximately -3V when the output voltage is zero.

4-120 Coupling Amplifier. Inverter Q6 serves as a "level changing" transistor, coupling the relatively small negative output level of Q5 to the considerably higher output levels used in the power amplifier output circuits. The gain of the coupling amplifier is small, only slightly greater than one. If the gross current limit is exceeded, the coupling amplifier receives a turn-down signal from Q23 (if positive output voltage gross current limit is exceeded) or Q20 (if negative output voltage gross current limit is exceeded). The operation of the positive and negative gross current limit circuits is described in subsequent paragraphs. Notice that the supply voltages for the coupling amplifier input circuits are low level ($\pm 15V$) and referenced to $\textcircled{2}$ common. The power amplifier output stages, on the other hand, use high-level supply voltages ($\pm 75V$ and $\pm 95V$) that are referenced to $\textcircled{1}$ common. Transistor Q31 in the emitter circuit of coupling amplifier Q6, serves to minimize unwanted ground current from flowing in the low sense output terminal and causing erroneous DVS output monitoring at the low sense terminal. If Q31 were not included and the emitter of Q6 were returned directly to $\textcircled{2}$ common, only a portion of the emitter current of Q6 would return to $\textcircled{2}$ by way of the base (and input circuits) current flow. A significant amount of Q6 emitter current would flow in its collector circuit which is, of course, referenced to $\textcircled{1}$. A return path to $\textcircled{2}$ for this current would be required with collector current flowing through $\textcircled{1}$, current sampling resistor A5R5, the low output

terminal (as well as the protection diodes across the low output and low sense terminals), through the low sense terminal (externally connected to the low output terminal) and on to Q (internally connected to the low sense terminal). Thus, a possibly significant offset voltage could be produced at the low sense terminal particularly if the low sense lead resistance is large. Transistor Q31, however, returns most of the high-level supply current through its collector circuit with only the difference between the base-emitter current of Q6 and the base-emitter current of Q31 required to return to Q through the low sense terminal circuit. This return current is relatively insignificant so that the accuracy of monitoring DVS operation at the low sense terminal is not impaired.

4-121 Power Amplifier. The power amplifier consists of three push-pull stages which are of complementary symmetry design. The input stage Q10 and Q12, is driven by a single-ended stage, Q7. For positive output currents the positive section of the amplifier (NPN transistors Q10, Q11, Q2, Q1, Q14, and Q15) is conducting while the negative section (PNP transistors Q12, Q13, Q3, Q4, Q16, and Q17) is cutoff. The reverse is true for negative output currents. At zero output current, both halves of the power amplifier are conducting a slightly with Q30 providing the drive and diodes CR17 and CR18 providing the voltage drop necessary to forward bias Q10 and Q12 simultaneously. This eliminates "dead spots" when the unit is programmed away from zero.

4-122 Transistor Q7 is a voltage amplifier, having a gain of approximately 20, while the three emitter-coupled push-pull stages provide most of the total current gain of the power amplifier. Hence, the voltage at the bases of the push-pull input stage (Q10 and Q12) is essentially equal to the output voltage of the unit. Q7, together with R36, CR16, CR18, CR21, and R38 form a voltage divider network in the base circuit of the input stage. The conduction of Q7 controls the current flowing in the voltage divider and, thus, the bias at the bases of the input transistors. Zener diodes VR3 and VR4, prevent the output voltage from exceeding approximately ± 55 volts.

4-123 Diodes CR30 through CR34 and resistors R108 and R109 are included in the Q10 and Q11 circuits to speed up the gross current limit operation of the DVS. Normally diodes CR30 through CR32 are reversed biased. However, if the output current exceeds approximately 1.8A, these diodes conduct and limit the output current to less than 2A (approximately 1.8A). This circuit limits the output current in approximately 2 μ sec thereby protecting the DVS circuit until the gross current

limit comparators react (in approximately 25 μ sec) to limit output current to 1.1A. Operation of the gross current limit comparators is described in subsequent paragraphs.

4-124 Under current latch conditions, transistors Q10 and Q12 are biased below cutoff due to the conduction of Q8 and Q9, part of the current latch switch circuit. The conduction of these transistors effectively shorts the bases of Q10 and Q12 to the high output terminal, reducing the bias current to zero. The current latch switch and isolator circuits are described in succeeding paragraphs.

4-125 The second push-pull stage (Q11 and Q13) on the A7 amplifier board drives the power output transistors (Q1 through Q4) which are mounted on the rear heat sink. These transistors are connected in series between the +75V and -75V supplies. The conduction of Q2 or Q3 is controlled directly by the output of Q11 or Q13; depending on which half of the amplifier is active at the time. The conduction of the other series transistor (Q1 or Q4) is controlled by the positive or negative bias transistors (Q14 and Q15 or Q16 and Q17). The base of each bias output transistor (Q14 or Q16) is connected to the center tap of a voltage divider (R45 and R46 or R49 and R50) which, in turn, is connected between the ± 95 volt supply and the high output terminal. With this arrangement, variations in the output voltage are felt at the base of Q14 or Q16 and thus cause output transistor Q1 or Q4 to follow its series partner (Q2 or Q3). Resistors R45-R46 and R49-R50 are selected so the base of appropriate bias transistor (Q14 and Q16) rests at approximately half of the difference between the output voltage and the ± 95 volt supply voltage. This has the effect of equally dividing the voltage drops (and thus the power dissipation) between the two conducting output transistors.

4-126 Gross Current Limit Comparators. The positive and negative current limit comparators protect the output transistors of the power amplifier by limiting the maximum output current to a safe level for both source and sink conditions. The output current for normal source conditions is limited to a fixed maximum of 1.1A; for sink conditions the maximum current is a linear variable ranging from 0.25A at 50V (at HI output terminal) to 1.1A at 0V. Because the two current limiters are so similar only one, the positive, limiter, is described in detail.

4-127 When the output current is within specified limits transistor Q21 is biased on, Q22 and Q23 are cutoff, and diode CR29 is reversed biased. Under these conditions the limiter has no effect on the output current. Zener diode VR11 together with resistors R115, R116, and R120 form a bias

network that holds the base voltage of Q22 slightly more positive than the base voltage of Q21 and thus establishes a positive current limit switching level. If the output current starts to exceed the source current limit of 1.1A, the voltage drop across sampling resistor A5R5 increases and produces a voltage level at the base of Q21 equal to the base voltage of Q22. With zero differential voltage between Q21 and Q22, Q22 comes out of cutoff switching on Q23 and forward biases CR29. The negative voltage coupled through CR29 clamps the power amplifier output current at a maximum of 1.1A. Diodes CR38 and CR39 protect the base emitter junction of Q22 from voltage transients caused by surge currents through A5R5.

4-128 During sinking conditions the normally positive output voltage becomes negative. This negative voltage is fed back through diode CR40 and influences the positive current limit switching level at the base of Q22. As the output voltage becomes increasingly negative, the positive current limit switching level decreases so that Q22 will switch on and initiate current limiting at an output current level less than 1.1A.

4-129 Current Latch Isolator and Switch. These two circuits operate in conjunction with the current latch circuits on the A6 Control Board. The current latch isolator circuit consists of switching transistor A7Q25 and tuned-collector oscillator A7Q24. A positive going transition at the current latch input at the base of A7Q25 causes it to conduct. The resultant output at its collector, is fed to the emitter of A7Q24 via swamping resistor A7R70. This allows A7Q24 to conduct through the 10MHz tank circuit (T1 primary winding and capacitor C20) in its collector circuit. Voltage divider resistors R68 and R69 establish the base bias. Regeneration for sustained oscillation is coupled from the collector winding of T1 to the base winding. Each end of the T1 output winding contains a rectifier-filter network in order to drive the push-pull current latch switch, A7Q8 and A7Q9. Rectifiers CR7 and CR8 conduct on the positive half cycles; rectifier diodes CR11 and CR12 conduct on the negative half cycles. Under latch conditions, both, Q8 and Q9 conduct to zero bias the power amplifier push-pull input stage (A7Q10 and A7Q12).

4-130 Disconnect Interlock. Relay A4K1 and driver transistor A4Q1 protect the load by shorting the output terminals of the DVS under certain conditions. The output terminals are shorted when K1 is deenergized. This occurs if the ③ common input from the computer is removed or the -12V DELAYED is not present. When the unit is first turned on, K1 is also deenergized because the -12V bias input is delayed for approximately 0.2 seconds after turn-on. Notice that the current latch circuits are activated at this time and, thus, must be reset with a gate input before the unit can be restored to normal operation. The output is also shorted at turn off of the unit because the -12V bias input collapses rapidly causing K1 to deenergize.

4-131 POWER DISTRIBUTION (See Figure 7-2, Sheet 4)

4-132 The $\pm 12V$, $\pm 26V$, $\pm 75V$, and $\pm 95V$ bias and supply voltages are obtained from power supply board A4. The +5V is obtained from chassis mounted +5 volt regulator Z1. Note that the +5V supply is referenced to ④ which is at -26V with respect to ②, the common potential for the $\pm 26V$ supply. The $\pm 12V$ supply is referenced to ③ which is connected to the computer ground. The $\pm 12V$, $\pm 26V$, $\pm 75V$, and $\pm 95V$ supplies are simple networks containing rectifier diodes, filter capacitors, and bleeder resistors.

4-133 Amplifier board A7 contains two regulator circuits for deriving $\pm 15V$ outputs from the $\pm 26V$ inputs. Each circuit is composed of a series regulator (Q26 or Q28) and an input comparator stage (Q27 or Q29). The input stage compares a portion of the output voltage with a fixed reference voltage (across VR5 or VR6). If a difference exists, it generates an error voltage which is of the correct amplitude to counteract this difference.

4-134 Boards A1, A2, A3, and A6 contain filter capacitors for various supply voltages. In addition, board A1 contains zener diodes and resistors to develop +5V referenced to ③ and board A6 contains a series regulator A6Q34, resistors, and a zener diode to provide +4.99V referenced to ②. Series regulator A6Q34 also provides a +14.5V output referenced to ②.

SECTION V MAINTENANCE

5-1 INTRODUCTION

5-2 Upon receipt of the power supply, the performance test (Paragraph 5-6) should be made. This check is suitable for incoming inspection. If a fault is detected in the power supply while making the performance check or during normal operation, proceed to the troubleshooting procedures (Paragraph 5-37). After troubleshooting and repair, perform any necessary adjustments and calibrations (Paragraph 5-69). Before returning the power supply to normal operation, repeat the performance test to ensure that the fault has been properly corrected and that no other faults exist. Before performing any maintenance checks, turn on the power supply and allow a 30-minute warm-up.

5-3 TEST EQUIPMENT REQUIRED

5-4 Table 5-1 lists the test equipment required to perform the various procedures described in this section.

NOTE

In certain maintenance procedures (including troubleshooting), DVS plug-in boards are required to be mounted on the Extender Board (supplied with the DVS). The extender board includes an epoxy plate that is positioned with screws on either side of the extender board printed circuit board to interface with the particular plug-in board being extended. The following extender board screw positions (for the epoxy board) are to be used for extending the associated plug-in board:

	Extender Board Position	Associated Plug-In Board
Side A	A	D/A (A3)
	B	Logic (A2)
	C	Input (A1)
	D	Control (A6) and Power Amplifier (A7)
Side B	E	Not Used
	F	Not Used
	G	Not Used
	H	Not Used

Note further that when a board is extended, the front panel cover should be completely removed to avoid any possibility of inadvertently touching the plug-in board to the front panel cover.

5-5 To conveniently program the DVS, the Hewlett-Packard Pocket Programmer Model 14533B is recommended. A three-foot 50-conductor extension cable (Model 14534A) is available for convenience in attaching the Pocket Programmer to the rear panel data input connector. If the Pocket Programmer is to be used, read the operating instructions in the Programmer manual before proceeding.

5-6 PERFORMANCE TEST

5-7 The following tests can be used as an incoming inspection check and appropriate portions of the test can be repeated either to check the operation of the instrument after repairs or for periodic maintenance tests. The tests are performed using a nominal 115-volt 60-Hz single-phase input supply to the unit. If the correct result is not obtained for a particular check, do not adjust any controls; proceed to the troubleshooting procedures.

5-8 PRE-OPERATION CHECKOUT

5-9 This procedure checks the basic operation of the DVS to assure that all programming functions are operating satisfactorily.

INITIAL CONDITIONS

1. Check that the rear terminal strip is connected as shown in Figure 3-1. III should be strapped to HI S (high sense) and LO to LO S (low sense).
2. Connect a digital voltmeter in parallel with a $50\Omega \pm 1\%$ 50 watt resistor across the III and LO terminals on the rear of the DVS.
3. Connect the Pocket Programmer to the data input connector and set its switches as follows:
 - a. Set the INPUT LEVEL REF switch to DATA COM.
 - b. Set the MP/DCPS switch to DCPS.
 - c. Set the SOURCE SELECT switch to EXT.

(The above three switches remain in these positions

Table 5-1. Test Equipment Required

TYPE	REQUIRED CHARACTERISTICS	USE	RECOMMENDED MODEL
Diff. or Dig. Voltmeter	Sensitivity: 100 μ V full scale (min.). Accuracy: 0.004%	Measure dc voltages; calibration procedures	HP 3462, 3490, or 3420
Variable Voltage Transformer	Current Rating: 2A. Range: 90-130Vac. Equipped with voltmeter accurate within 1V.	Vary ac input	---
Oscilloscope	Differential input; dc to 50MHz	Display transient response waveforms and p-p noise	HP 180A plus 1801A, 1806A, and 1821A Plug-Ins
DC Voltmeter	Accuracy: 1%. Input resistance: 20,000 ohms/volt (min.).	Measure dc voltages	HP 412A
Repetitive Load Switch	Rate: 60-400Hz; 2 μ sec rise and fall time.	Measure transient response	See Figure 5-5.
Resistive Loads	50 Ω , 50W \pm 5%; 17 Ω , 17W \pm 5%	Power supply load resistors	---
Resistor	Value: 50 Ω , \pm 1%, 50 watts.	Check current latch performance	---
Function Generator	0.0005Hz - 5MHz	Measure programming time.	HP 3310A/B
DC Power Supply	0-25Vdc, 0-400mA	Provide input to ANLG IN terminals on DVS.	HP 6215A
Rms Voltmeter	10Hz-10MHz	Measure rms ripple and noise	HP 3400A
Programming Device		Supply digital program inputs	HP Pocket Programmer 1433B

throughout all of the following procedures.)

- d. Set the RANGE switch to X10.
- e. Set the data and sign bit switches for an output of +0.00 volts. The proper coding for Pocket Programmer data and sign bit switches depends on the instrument being programmed. The voltage magnitude switches might either be up (open circuit) or down (grounded) to program zeros. Similarly, the OUTPUT SIGN switch might be up or down to program a positive output. Refer to the appropriate Option Appendix or the Instrument Modification Sheet supplied with the instrument being programmed for digital input coding information.)
- f. Set the I LIMIT switches for a 1000mA

current limit. (all three switches will be down.)

4. Open the front access door and put the STORAGE DISABLE switch on the A2 board in the STORAGE DISABLE position.
5. Connect the line cord and switch the LINE switch to ON. The STORAGE DISABLE light will come on and the front panel meters will both indicate zero. (Select the 10V and 12A meter ranges.)

CURRENT LATCH RESET AND DISCONNECT INTERLOCK CHECK

6. On the Pocket Programmer, switch on the 4096 bit. Observe that the digital voltmeter indi-

reads approximately 0.3 volts (not +40.96V) and the DVS CURRENT meter reads less than 10mA. The error is because the over current latch circuit activated when the DVS was turned-on.

NOTE

Whenever the DVS is turned on the Gate switch must be toggled to reset the over-current latch circuit.

7. Press the Pocket Programmer GATE switch. The digital voltmeter should indicate +40.96V and the DVS CURRENT meter 820mA (1.2A scale).

8. Disconnect the Pocket Programmer data input cable. The meters will indicate 0V and less than 10mA. The instrument is in the disconnect interlock and overcurrent latch status mode.

9. Reconnect the data input cable. The meters will indicate 0V and less than 10mA. The instrument is still in the overcurrent status.

10. Press the Pocket Programmer GATE switch. The meters will indicate +40.96V and 820mA again.

VOLTAGE RANGE CHECK

11. Set the RANGE switch on the Pocket Programmer to X1. The digital voltmeter should read +4.096V.

VOLTAGE MAGNITUDE CHECK

12. On the Programmer, turn on all of the voltage magnitude bits. The digital voltmeter reading will be +16.3835V ±0.001V.

13. Turn off all of the voltage magnitude bits. The voltage reading will be 0 volts ±0.001 volts.

14. Turn on each voltage magnitude bit 0.5 through 8192, individually, and check the digital voltmeter readings in the following chart (all readings ±1mV).

NOTE

Turn each bit off after making check.

SWITCH	READING	SWITCH	READING
0.5	0.5mV	128	128mV
1	1mV	256	256mV
2	2mV	512	512mV
4	4mV	1024	1.024V
8	8mV	2048	2.048V
16	16mV	4096	4.096V
32	32mV	8192	8.192V
64	64mV		

15. Switch the STORAGE DISABLE switch on board A2 to the STORAGE position.

16. Repeat the sequence of Programmer switch operations of step (14) but press the Programmer GATE switch after each voltage magnitude bit change. Observe that the previously programmed voltage remains until the new value is gated into storage.

17. Switch the STORAGE DISABLE switch back to the STORAGE DISABLE position, set the OUTPUT SIGN switch on the Programmer to the negative position and turn off all voltage magnitude bits to obtain -0.5mV, ±1mV.

18. Repeat steps (14), (15), and (16), set voltage magnitude switches so that the input is received in the "negative 2's complement" code. To obtain any negative number, first complement the corresponding positive number and then add a binary "1" to the least significant digit. For example, to program the unit to a -0.5mV output, all switches (0.5 through 8192) must be set to their binary "1" position. To program the supply to -1mV, the 0.5 switch is set to binary "0" and the remaining switches are set to "1". As stated previously, the proper coding for the Pocket Programmer depends upon the instrument being programmed. The voltage magnitude switches may be up (open circuit) or down (grounded) to program ones or zeros. Refer to the appropriate Option Appendix or Modification Sheet supplied with the instrument being programmed.

GROSS CURRENT LIMIT

19. Turn off power to the DVS. Disconnect the 50 Ω load and connect the 17 Ω , 17W load across the HI and LO terminals.

20. On the DVS rear barrier strip, jumper the C₁ terminals. This disables the programmable current latch circuit.

21. Set the voltage magnitude switches and OUTPUT SIGN switch on the Programmer for an output voltage of +10 volts.

22. Set the CURRENT METER RANGE switch on the DVS front panel to 1.2A and the STORAGE DISABLE switch on board A2 to DISABLE.

23. Turn on power to the DVS and press the Programmer GATE switch. Observe that the DVS voltmeter reads +10V.

24. While observing the DVS ammeter, increase the voltage magnitude input in +1V steps (to a maximum of +20V) until the current no longer increases (limiting). The current at limiting should be between 1.1A and 1.2A.

25. Set the voltage magnitude switches and OUTPUT SIGN switch on the Programmer for an output voltage of -10V.

26. While observing the DVS ammeter, increase the voltage magnitude input in -1V steps (to a maximum of -20V) until the current no longer increases (limiting). The current at limiting should

be between 1.1A and 1.2A.

CURRENT OVERLOAD CHECK

27. Turn off power to the DVS. Disconnect the 17 Ω , 17W load and connect the 50 Ω , 1%, 50 watt (minimum) load resistor between the HI and LO terminals. The jumper remains connected between the G₁ terminals.

28. Check Option descriptions (Appendix A, B, or C) or, where applicable, the Modification Sheet in the manual, to determine the existence of output transistor "pull up" resistor A6A6R8. If A6A6R8 is used proceed to step 29. If A6A6R8 is not used, proceed to step 30.

29. Connect a dc voltmeter between 0 LOAD STATUS and DATA COM test points on the Pocket PROGRAMMER. Select a voltmeter range capable of reading 12 volts. Proceed to step 31.

30. Connect an ohmmeter between the 0 LOAD and DATA COM test points on the pocket programmer. The common lead should be connected to the DATA COM test point.

31. Program the current latch value for 20mA. The I LATCH (current latch) switch positions on the Programmer are listed below for the eight current latch values.

32. Set the voltage magnitude and OUTPUT SIGN on the Programmer for an output voltage of $\pm 0.75V$.

33. Turn on power to the DVS and press the Programmer GATE switch. Overload status signal should be normal (voltage meters should indicate the collector voltage at output stage or the ohmmeter should indicate an open circuit).

34. Increase the output voltage in 0.1V steps. Overload status signal should switch to the overload state between 0.95V and 1.05V output (voltage meter reads 0V or ohmmeter reads 0 ohms). See following chart:

CURRENT LATCH (mA)	I LATCH SWITCH POSITIONS			CURRENT OVERLOAD OCCURS BETWEEN (Volts)
	L24	L22	L23	
20	up	up	up	0.95 and 1.05
50	up	down	up	2.375 and 2.625
70	up	up	down	3.325 and 3.675
100	up	down	down	4.75 and 5.25
200	down	up	up	9.5 and 10.50
500	down	down	up	23.75 and 26.25
700	down	up	down	33.25 and 36.75
1000	down	down	down	47.50 and 52.50

35. Change the programmable current latch (I LATCH) value and output voltage at which current overload occurs to the values listed in the chart and repeat step (34).

36. Set the OUTPUT SIGN switch to negative and repeat steps (34) and (35).

CURRENT LATCH CHECK

37. Turn off power to the DVS and remove the jumper between the G₁ terminals. The 50 Ω load resistor remains connected between the HI and LO output terminals.

38. As in the current overload check step 28, determine the existence of the current latch output transistor "pull up" resistor A6A5R8. If A6A5R8 is used, connect a dc voltmeter between the I LATCH STATUS and DATA COM test points on the Programmer. If A6A5R8 is not used, connect an ohmmeter between these two test points.

39. On the Programmer, set the current latch (I LATCH) to 200mA and the voltage magnitude to 25V.

40. Turn on power to the DVS and press GATE on Programmer. Instrument should remain in current latch condition (voltage meter reads 0V or ohmmeter reads 0 ohms).

41. Remove the 50 Ω load resistor from the HI and LO output terminals. Unit should remain in latched condition until a GATE signal is applied.

5-10. CONSTANT VOLTAGE TESTS

5-11. For constant voltage measurements, the measuring device must be connected across the rear sensing terminals of the supply in order to achieve valid indications. A measurement made across the load includes the impedance of the leads to the load and such lead lengths can easily have an impedance several orders of magnitude greater than the supply impedance (10 milliohms at dc), thus invalidating the measurement.

5-12. To avoid mutual coupling effects, each monitoring device must be connected directly to the sensing terminals by separate pairs of leads. The load resistor is connected across the output terminals and must be selected according to the output voltage and current of the supply. When measuring the constant voltage performance specifications, the CURRENT LATCH should be programmed well above the maximum output current which the supply will draw, since the onset of current latch action will cause a drop in output voltage, increased ripple, and other performance changes not properly ascribed to the constant voltage operation of the supply.

5-13. Calibration Error

Definition: The maximum absolute voltage

accuracy deviation at constant room temperature, 115Vac input, no load, following a minimum warm-up time of 30 minutes. It is the ability of the instrument to accurately convert a digital input into an analog output voltage.

5-14 To measure the accuracy, proceed as follows:

- Connect a digital or differential voltmeter to the HI and LO sensing terminals on the rear of the unit.
- Program the output to 50.00V and gate the unit.
- The voltmeter should read 50.00V \pm 10mVdc.
- Set the range switch to X1.
- Program the output to -16.384 volts. Gate the input.
- The differential voltmeter should read -16.384V \pm 1mVdc.

5-15 Voltmeter Accuracy. To check the accuracy of the front panel voltmeter, proceed as follows:

- Connect a Digital or differential voltmeter to the HI and LO sensing terminals on the rear of the unit.
- Turn on supply and program the output voltage for 50.00V. Gate the unit.
- Record the reading on the voltmeter.
- The reading on the front panel meter should be the same as the reading in Step (c) \pm 1.5 volts.

5-16 Load Regulation

Definition: The change ΔE_{OUT} in the static value of dc output voltage resulting from a change in load resistance from open circuit to a value which yields maximum rated output current (or vice versa).

5-17 Load regulation should be checked in both the higher (X10) range with both negative and positive output voltages and the lower (X1) range with both positive and negative output voltages, since any one of these four conditions can yield an unsatisfactory result, which is not reflected under the other three conditions. To test the load regulation for all four conditions, proceed as follows:

- Connect test setup shown in Figure 5-1. Set the METER switch to the highest voltage and current ranges.
- Program the current latch to 1 ampere.
- Turn on supply.
- Program the output voltage to +50.00 volts, and gate the unit.
- Read and record voltage indicated on

voltmeter.

- Disconnect load (open) and gate the unit.
- Reading on voltmeter should not vary from reading recorded in Step (e) by more than 500 μ V.
- Reconnect load.
- Program the output to -50.00V and gate the unit.
- Repeat Steps (e) and (f).
- Reading on voltmeter should not change from reading recorded in Step (e) by more than 500 μ V.
- Program the output to +16.3835 volts, X1 range and gate the unit.
- Change load to 17 Ω , 17 watts.
- Repeat Steps (e) and (f).
- Reading on voltmeter should not change from the reading recorded in Step (e) by more than 150 μ V.
- Reconnect load (17 Ω , 17W).
- Program the output to -16.384 volts, X1 range and gate the unit.
- Repeat Steps (e) and (f).
- Reading on voltmeter should not change from reading recorded in Step (e) by more than 150 μ V.

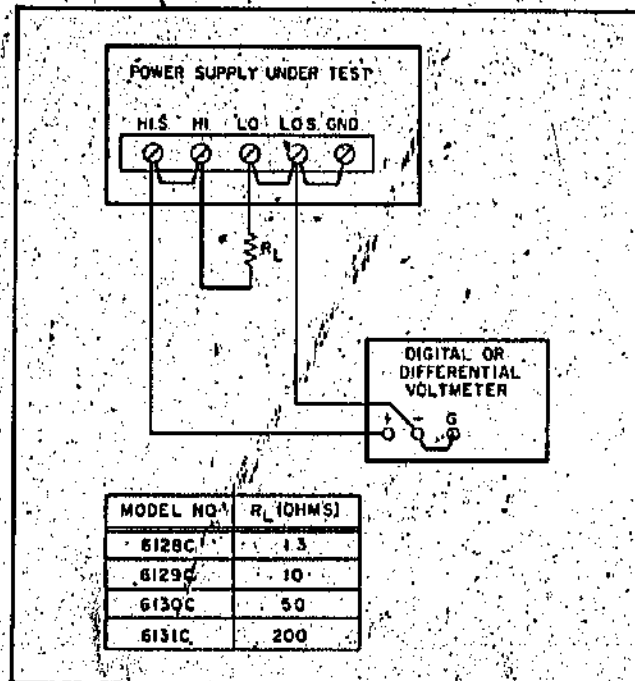


Figure 5-1. Constant Voltage Load Regulation Test Setup

5-18 Line Regulation.

Definition: The change, ΔE_{OUT} in the static value of dc output voltage resulting from a change in ac input volt-

age over the specified range from low line, 10% less than nominal, to high line, 10% more than nominal, or high line to low line.

5-19 Line regulation should be checked in both the higher (X10) range with both negative and positive output voltages and the lower (X1) range with both positive and negative output voltages, since any one of these four conditions can yield an unsatisfactory result, which is not reflected under the other three conditions. To test the line regulation for all four conditions, proceed as follows:

a. Connect test setup shown in Figure 5-1. Set the METER switch to the highest voltage and current ranges.

b. Connect variable auto transformer between input power source and power supply 115Vac input.

c. Program the current latch to 1 ampere.

d. Program the output voltage to 50.00 volts, X10 range.

e. Program the output voltage sign to positive (+).

f. Adjust variable auto transformer for low line (103.5Vac). Gate the unit.

g. Read and record voltage indicated on voltmeter.

h. Adjust variable auto transformer for high line (126.5Vac). Gate the unit.

i. Reading on differential voltmeter should not vary from reading recorded in Step (g) by more than 5mV.

j. Program the output voltage sign to negative (-). Perform Steps (f) through (i).

k. Program the output voltage to 16.3835Vdc, X1 range. Change R_L to 17 Ω , 17W.

l. Program the output voltage sign to positive (+). Perform Steps (f) through (h).

m. The reading on the voltmeter should not vary from the reading recorded in Step (g) by more than 500 μ V.

n. Program the output voltage sign to negative (-). Perform (f) through (h).

o. The reading on the voltmeter should not vary from the reading recorded in Step (g) by more than 500 μ V.

5-20 Temperature Coefficient

Definition: The change in output voltage per degree Centigrade change in the ambient temperature under conditions of constant input ac line voltage, output voltage setting, and load resistance.

5-21 The temperature coefficient of a power supply is measured by placing the power supply in an oven and varying the temperature over any span within its rating. (Most HP power supplies are

rated for operation from 0°C to 55°C). The power supply must be allowed to thermally stabilize for a sufficient period of time at each temperature of measurement, usually 1/2 hour.

5-22 To check the temperature coefficient, proceed as follows:

a. Connect test setup shown in Figure 5-1.

b. Strap C_T terminals and program the output voltage to 50.00 volts. Gate the unit.

c. Insert the power supply into the temperature-controlled oven (voltmeter and load resistance remain outside oven). Set the temperature to 30°C and allow 30 minutes warm-up.

d. Record the voltmeter indication.

e. Raise the temperature to 40°C and allow 30 minutes warm-up.

f. The voltmeter indication should change by less than 6mV from indication recorded in Step (d).

g. Program the output voltage to 16.3835 volts. Gate the unit. Change R_L to 17 Ω , 17W. Perform Steps (c) through (e).

h. The voltmeter indication should change by less than 1.6mV from indication recorded in Step (d).

5-23 Programming Time

Definition: Maximum time required for the output voltage to settle to within 0.1% of the programmed voltage change after simultaneous receipt of the data and gate commands as measured with a resistive load.

5-24 Equal positive and negative output voltages cannot be obtained by simple switching the position of the polarity switch; negative numbers must be programmed in the 2's complement form. For this reason, a computer or calculator would be the easiest means to obtain the equal positive and negative numbers necessary to perform this test. To perform this test for "worst case" result, use the test setup in Figure 5-2 employing the computer or calculator recommended. Program the computer or calculator so that it will program the DVS between +16.3835 and -16.384 volts and between +50 and -50 volts. The observed waveform should be within the tolerance of Figure 5-3. If the computer or calculator is not available, use the Pocket Programmer and Function Generator (see Figure 5-2) as the programming device and proceed as follows:

CONTROL SETTINGS

- a. Set switches on HP 3490A as follows:
 1. FUNCTION: DC
 2. RANGE: /As needed 10V or 100V
 3. SAMPLE RATE: HOLD

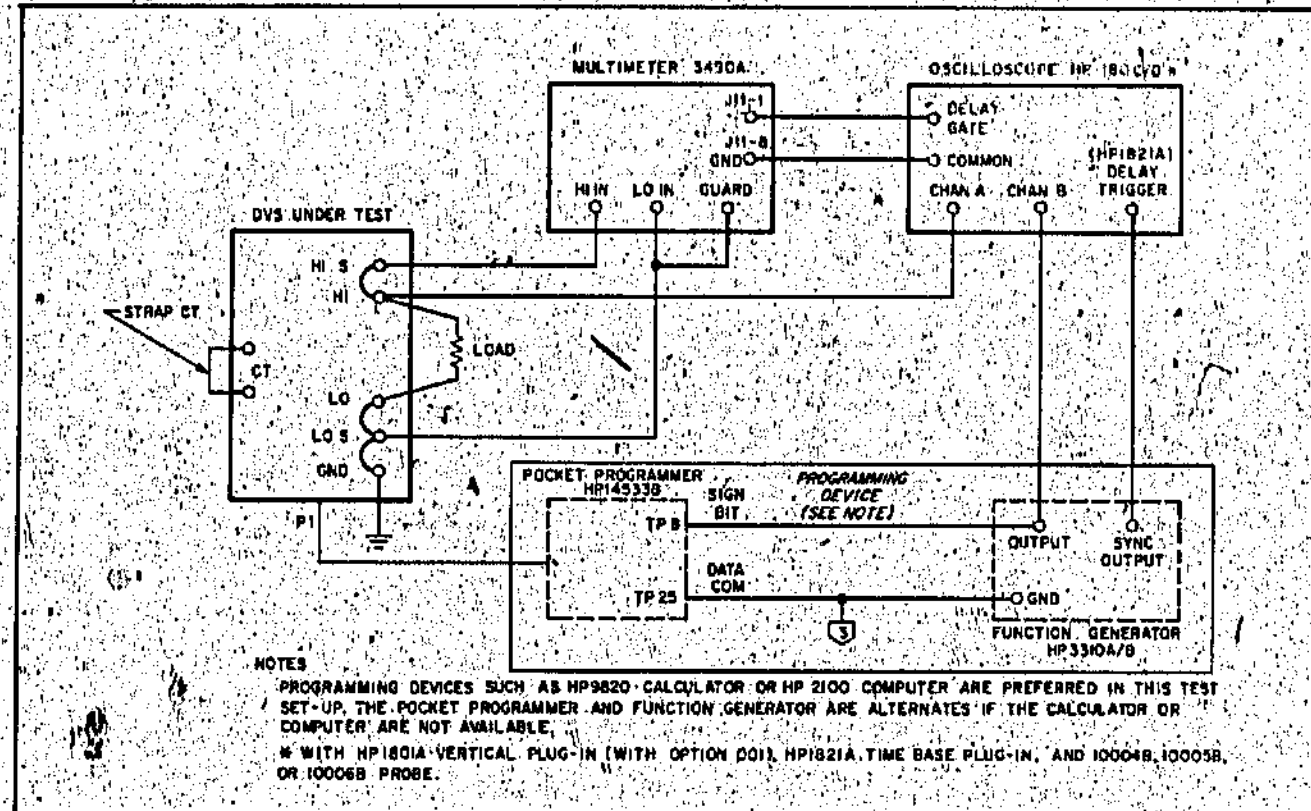


Figure 5-2. Programming Time Test Setup

4. **SAMPLE/HOLD: TRACK/HOLD**
 - b. Set switches on HP 1821A Delay Section of HP 180 C/D as follows:
 1. AC or ACE; SLOPE + or -; AUTO
 2. TRIGGER LEVEL: Adjust for stable display
 3. TIME/DIV: Delayed to 0.1 to 0.5 μ sec
 - c. Set HP 1821A Main Section of HP 180 C/D as follows:
 1. SWEEP MODE: AUTO
 2. INT: SLOPE + or -; AC
 3. TIME/DIV: 1msec with X10 magnifier
 4. Set sweep to MAIN
 - d. Set switches on HP 3310 A/B as follows:
 1. FREQUENCY: 100Hz
 2. FUNCTION: Squarewave
 3. OUTPUT LEVEL: Value specified in DVS Appendix for data and sign bits.
 - e. Set switches on HP 14533B as follows:
 1. SOURCE SELECT: EXT
 2. MP/DCPS: DCPS
 3. LATCH: All bits down (maximum L-LATCH)
 4. INPUT LEVEL REF: DATA COM
 5. RANGE: X1
 - f. On DVS A2 board, set switch to STORAGE DISABLE (only if Pocket Programmer is used).

PROCEDURE

- a. Connect 50 Ω , 50W load between HI and LO

- b. Connect 3310 A/B output (after adjusting to proper levels to 14533B.

Example: Program all but the 8192 bit to the down (shorted to Data com.) position. Program the sign bit to the up (not shorted to Data com.) position. Connect the 3310 A/B output to the sign bit and DATA com to the 3310 A/B ground. The output will now program between -8.1925 volts and +8.192 volts, for a $\Delta V_{OUT} = 16.3845$ volts. In this example, 0.1% of $\Delta V_{OUT} = 16.3845mV$. The output voltage should read within 16mV of final value within 300 μ sec.

- c. Obtain a stable display on oscilloscope. While adjusting DELAY (DIV) control on 1821A, look for the bright spot on the CRT trace. The beginning of the bright spot indicates where the 3490A will be triggered.
- d. To calibrate system delay, adjust bright spot on CRT display (using DELAY control) to the position where the 3490A indicates approximately zero volts. The time between the actual zero crossing of the DVS output (channel A) and the start of the bright spot indicates system delay (T_d).
- e. Measure the voltage just prior to the waveform transitions (see Figure 5-3). Voltage reading should be within 0.1% of ΔV_{OUT} .

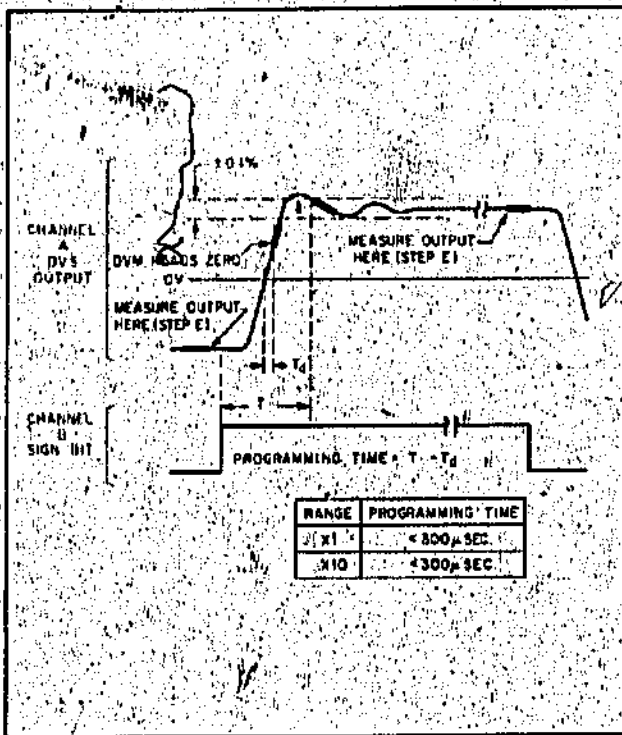


Figure 5-3. Programming Time Waveforms

Example: as before $\Delta V_{OUT} = 16.3845$ volts; 0.1% of $\Delta V_{OUT} = 16\text{mV}$. For a -8.1925 volt to +8.192 volt transition, look for a reading of +8.176 volts on the 3490A.

f. Using the DELAY control on the 1821A, start at the zero crossing and sweep until the voltage in step e. is reached. Determine the time (T) from the transition time of channel B trace to the beginning of the bright spot. DVS programming time will then be:

$$\text{Programming Time} = T - T_d$$

5-25 Ripple and Noise

Definition: The residual ac voltage which is superimposed in the dc output of a regulated power supply.

Ripple and noise may be specified and measured in terms of its RMS or (preferable) peak-to-peak value.

Ripple and noise measurement can be made at any input ac line voltage combined with any dc output voltage and load current within rating.

5-26 The amount of ripple and noise that is present on the power supply output is measured either in terms of the RMS or (preferable) peak-to-peak value. The peak-to-peak measurement is particularly important for applications where noise spikes could be detrimental to a sensitive load, such as logic circuitry. The RMS measurement

is not an ideal representation of the noise, since fairly high output noise spikes of short duration could be present in the ripple and not appreciably increase the RMS value.

5-27 RMS Measurement. To check the rms value of ripple and noise, proceed as follows:

- Connect 50 Ω , 50W load across HI and LO terminals.
- Using coax cable, connect rms voltmeter (HP 3400A is recommended) to the DVS HI and LO terminals. On the DVS end, connect the coax inner conductor to the HI terminal and the coax shield lead to the LO terminal (which is also connected to DVS ground).
- Strap C_T terminals together.
- Program the output voltage for 50.0 volts and the voltage range to X10.
- The voltmeter should read less than 1.5mV rms.
- Program the voltage range to X1 and output voltage to +16.3835 volts. Change load to 17 Ω , 17W.
- The voltmeter should read less than 0.5mV rms.

5-28 Note that a continuous ground loop exists from the third wire of the input power cord of the rms meter via the grounded power supply case, the wire between the negative output terminal of the power supply and the input of the meter, and the grounded meter case. Any ground current circulating in this loop as a result of the difference in potential E_G between the two ground points causes an IR drop which is in series with the meter input. This IR drop, normally having a 60Hz line frequency fundamental, plus any pickup on the leads interconnecting the power supply and meter, appears in the meter reading. The magnitude of this resulting noise signal can easily be much greater than the true ripple developed between the output terminals of the power supply, and can completely invalidate the measurement. To minimize the effects of ground current flow, the DVS and test instruments in all ripple and noise measurements should be plugged into the same ac power buss whenever possible.

5-29 Peak-to-Peak Measurements. The same ground current and pickup problems exist if an oscilloscope is substituted in place of the rms voltmeter in the peak-to-peak measurements. However, the oscilloscope display, unlike the true rms meter reading, tells the observer immediately whether the fundamental period of the signal displayed is 8.3 milliseconds (1/120Hz) or 16.7 milliseconds (1/60Hz). Since the fundamental ripple frequency present on the output of an HP supply is 120Hz (due to full-wave rectification), an oscilloscope display showing a 120Hz fundamental com-

ponent is indicative of a "clean" measurement setup, while the presence of a 60Hz fundamental usually means that an improved setup will result in a more accurate (and lower) value of measured ripple. To verify that the oscilloscope is not displaying ripple that is induced in the leads or picked up from the grounds, the (+) scope lead should be shorted to the (-) scope lead at the power supply terminals. The ripple value obtained when the leads are shorted should be subtracted from the actual ripple measurement.

5-30 The simple, direct test equipment connection of the rms measurement is normally not adequate to measure the high-frequency components of the peak-to-peak ripple and noise. Figure 5-4A shows a technique using a 50 Ω coaxial cable between the DVS and oscilloscope that is terminated in its characteristic impedance. Note that the terminating network is placed across the DVS output to avoid attenuating the low-frequency (60Hz) component of the ripple and noise. Further, the impedance matching network eliminates standing waves and cable ringing which might introduce erroneous values in the measurement.

5-31 In most cases, the single-ended scope method of Figure 5-4A will be adequate to eliminate non-real components of ripple so that a satisfactory measurement may be obtained. However, if the DVS and oscilloscope cannot be plugged into the same ac power buss or the peak-to-peak reading obtained with a single ended scope exceeds the specifications due to I_g , it will be necessary to use a differential scope with properly terminated floating inputs as shown in Figure 5-4B. Note that the coax connectors are not connected to ground on the DVS end. Because of its common mode rejection, a differential oscilloscope displays only the difference in signal between its two vertical input terminals, thus ignoring the effects of any common mode signal produced by the difference in the ac potential between the power supply case and scope case. Before using a differential input scope in this manner, however, it is imperative that the common mode rejection capability of the scope be verified by shorting together its two input leads at the power supply and observing the trace on the CRT. If this trace is a straight line, then the scope is properly ignoring any common mode signal present. If this trace is not a straight line, then the scope is not rejecting the ground signal and must be realigned in accordance with the manufacturer's instructions until proper common mode rejection is attained.

5-32 To check the peak-to-peak ripple and noise output, proceed as follows:

a. Connect 50 Ω , 50W load, impedance matching network(s), and oscilloscope as shown

in Figures 5-4A or 5-4B.

b. Strap together C₁ terminals.

c. Program the output voltage for 30.0 volts.

d. The observed ripple should be less than 7mV p-p.

e. Program the voltage range to X1, the output voltage to +16.3835 volts, and change load to 17 Ω , 17W. The observed ripple should be less than 2mV p-p.

5-33 Transient Recovery Time

Definition: The time "X" for output voltage recovery to within "Y" millivolts of the nominal output voltage following a "Z" amp step change in load current—where: "Y" is specified as 0.1% of full range voltage. The nominal output voltage is defined as the dc level half way between the static output voltage before and after the imposed load change, and "Z" is the specified load current change, which is equal to the rated output current.

5-34 A mercury-wetted relay, as connected in the load switching circuit of Figure 5-5 should be used for loading and unloading the supply. When this

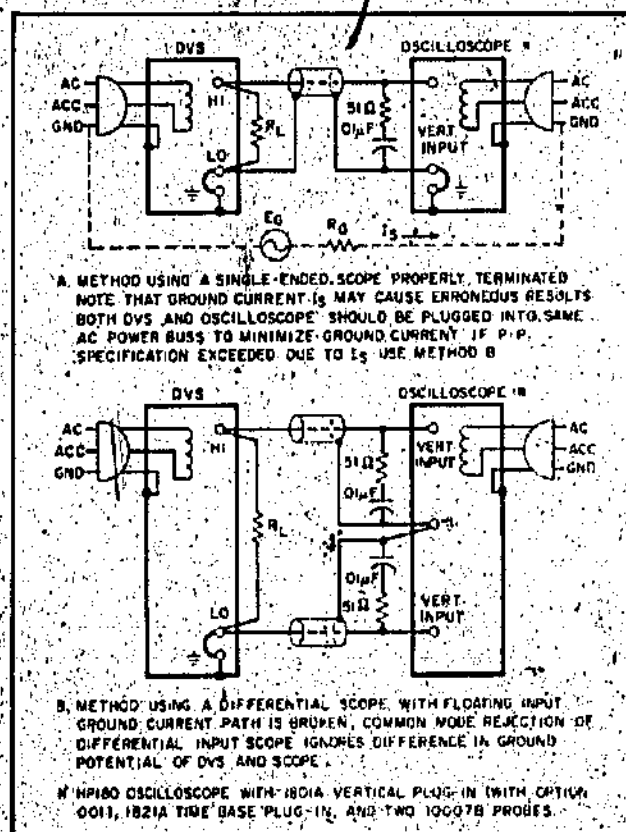


Figure 5-4. Peak-to-Peak Ripple and Noise Test Setup

load switch is connected to a 60Hz ac input, the mercury-wetted relay will open and close 60 times per second. Adjustment of the 25K control permits adjustment of the duty cycle of the load current switching and reduction in jitter of the oscilloscope display.

5-35 The maximum load ratings listed in Figure 5-5 must be observed in order to preserve the mercury-wetted relay contacts. Switching of larger load currents can be accomplished with mercury pool relays; with this technique fast rise times can still be obtained, but the large inertia of mercury pool relays limits the maximum repetition rate of load switching and makes the clear display of the transient recovery characteristic on an oscilloscope more difficult.

5-36 The transient recovery time is checked in both the X10 and X1 ranges as follows:

- Connect test setup shown in Figure 5-5.
- Strap C_T terminals together.

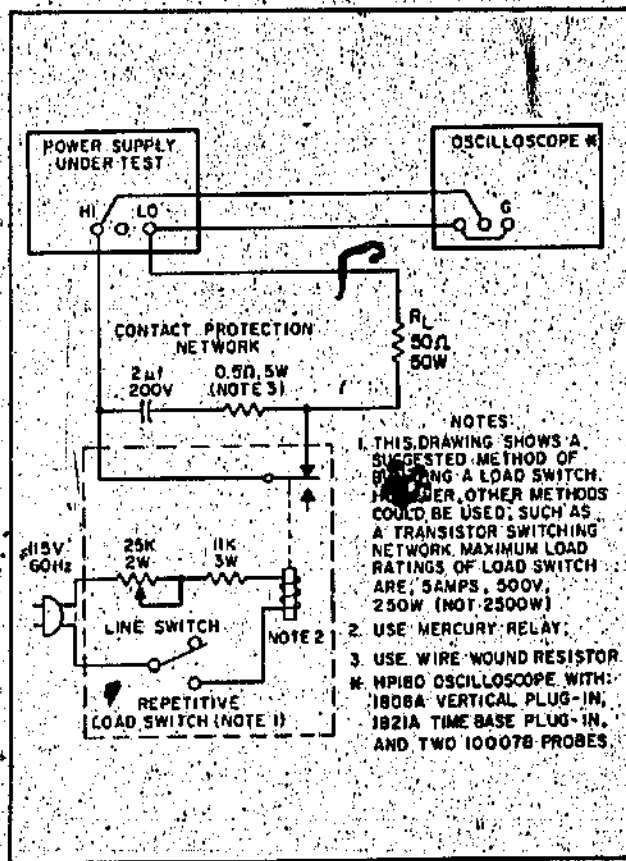


Figure 5-5. Transient Recovery Time, Test Setup

c. Turn on supply and program the output voltage to +50.00 volts and voltage range to X10 (50V).

d. Close the line switch on the repetitive

load switch setup.

e. Set the oscilloscope for internal sync and lock on either the positive or negative transient spike.

f. Set the vertical input of the oscilloscope for ac coupling so that small dc level changes the output voltage of the power supply will not cause the display to shift.

g. Adjust the sync controls separately for the positive and negative going transients so that not only the recovery waveshape but also as much as possible of the rise time of the transient is displayed.

h. Starting from the major graticule division representative of time zero, count to the right 150 μsec and vertically 50mV. Recovery should be within these tolerances as illustrated in Figure 5-6.

i. Program the output voltage to +15.3835 volts, change R_L to 17Ω, 17W and the voltage range to X1.

j. The transient recovery should be within 16mV at 150μsec as illustrated in Figure 5-6.

5-37 TROUBLESHOOTING

5-38 Before attempting to troubleshoot this instrument, make certain that the trouble lies within the instrument and not in any associated equipment. In order to isolate the DVS from the system in which it is being used, the HP Pocket Programmer 14533B is recommended. This device permits the operator to manually program all functions of the DVS and thus isolate it from other possible sources of trouble within the system, such as computer interfacing or a programming error.

5-39 A good understanding of the principles of operation of the instrument is essential to an efficient approach to troubleshooting. For this

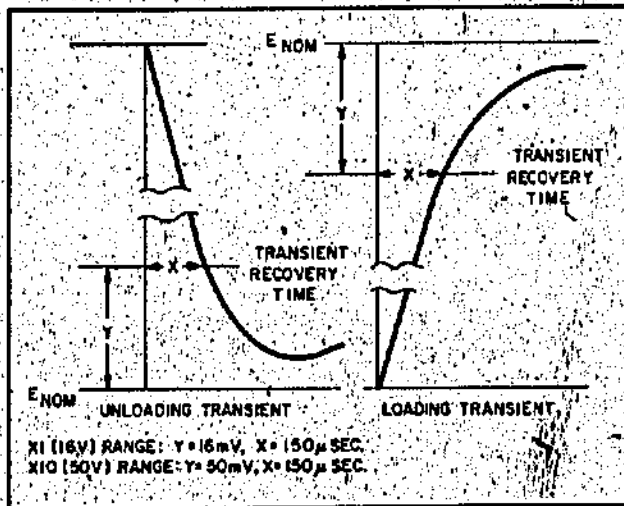


Figure 5-6. Transient Recovery Time, Waveforms

reason, it is recommended that Section IV, Principles of Operation be reviewed before attempting to troubleshoot the unit. Once the principles of operation are understood, follow the steps of the Overall Trouble Isolation Procedure in paragraphs 5-43 through 5-46 in the given order to establish which circuit areas are functional and which are not. References to more detailed troubleshooting guides are given in that procedure.

5-40 The four sheets of schematic diagrams of Figure 7-2 are based on the functional organization of the unit. Figure 7-1 provides an overall block diagram of the unit, except for its power distribution, and is especially convenient for tracing signal flow through the entire instrument. The circled test point numbers on Figures 7-1 and 7-2 are also marked on the component location diagrams which accompany the schematics. References are made to these test points in the Principles of Operation section of the manual, as well.

5-41 Before proceeding with the trouble isolation procedure, check for obvious troubles such as an open fuse, a defective power cord, an input power failure, a defective meter or a loosely connected board. Next visually inspect the boards for mechanical damage, discolored or charred components, etc. If the source of trouble cannot be detected by visual inspection perform the Overall Trouble Isolation Procedure given below. Throughout the course of troubleshooting the instrument, do not neglect the possibility of two or more faults being present.

CAUTION

Trouble isolation by exchanging a known good board for a suspected faulty one is allowed only for the A1, A2, and A3 boards. Exchanging a good board for a faulty one in any of the other card slots will often result in causing damage to the good board.

5-42 OVERALL TROUBLE ISOLATION PROCEDURE

5-43 Trouble Isolation — Power Distribution. Almost any trouble symptom could be caused by an incorrect power supply or reference voltage, thus it is good practice to routinely check all of the most important power supply voltages before attempting to isolate a problem to a particular circuit. The tests described in Table 5-2 provide a relatively fast check for trouble in this area. In many cases these checks can save hours that might be spent troubleshooting circuits which are not themselves defective. The A4 power supply board test points are accessible by removing the top cover; the A7 power amplifier test points are accessible by installing the extender board/A7 combination in the A7 slot. The test points are located by referring to the component location diagrams.

5-44 Notice that there are four separate power supply common return systems in the DVS, designated common ①, common ②, common ③ and common ④. When making any voltage or waveform measurements, be sure to use the appropriate power supply common reference point. The appropriate common point can be determined by referring to the circuit schematics of Figure 7-2. If the supply voltages are correct or if the supply voltages are incorrect but the components in that supply are not defective, proceed to paragraph 5-45.

5-45 Overall Troubleshooting Table. After checking the power supplies, disconnect the load and examine Table 5-3. This table contains a list of symptoms and probable causes that may cut down on troubleshooting time. For each trouble symptom, Table 5-3 isolates the fault to a component or group of components or directs the reader to additional procedures if further isolation of the trouble is necessary.

Table 5-2. Power Supply Troubleshooting

METER COMMON	METER POSITIVE	NORMAL READING	MAXIMUM RIPPLE P-P	PROBABLY DEFECTIVE COMPONENT
③	TP84	12 ± 1.5Vdc	0.2V	A4C1, CR2, CR3 or R1
TP85	③	12 ± 1.5Vdc	0.6V	A4C2, CR1, CR4, or R2
TP86	③	10 ± 2.0Vdc	0.6V	A4C10, CR22, CR5, CR6 or R27
TP87	④	5.0 ± .25Vdc	5mV	A4C3, CR8, CR9, R3, A5C1, C2, or Z1
TP88	②	26 ± 4Vdc	1.2V	A4C4, C19, C21, CR10, CR12 or R4
②	TP89	26 ± 4Vdc	0.8V	A4C5, C20, C22, CR11, CR13 or R5
①	TP90	95 ± 19Vdc	0.12V	A4C8, C12, C13, CR15, CR20, or R8
TP93	①	95 ± 19Vdc	0.25V	A4C9, C11, C14, CR14, CR21 or R9
①	TP91	75 ± 7.5Vdc	0.6V	A4C6, C15, C18, CR16, CR19 or R6
TP92	①	75 ± 7.5Vdc	0.8V	A4C7, C16, C17, CR17, CR18 or R7
NOTE: Test points 94 and 95 are on A7.				
②	TP94	15 ± 0.2V	0.0015V	A7C25, Q26, Q27, VR5 or CR24
TP95	②	15 ± 0.2V	0.0015V	A7C24, Q28, Q29, CR6 or CR25

Table 5-3. Overall Troubleshooting

SYMPTOM	PROBABLE CAUSE
Zero or Low Output Voltage	<ul style="list-style-type: none"> a. Fuse blown. Check output power transistors. b. Defective meter. c. Board(s) loosely connected. d. A4Q1 open or A4K1 defective. A4CR7 shorted. e. Short circuit load. f. Interconnect board A5 open.

Table 5-3. Overall Troubleshooting (Continued)

SYMPTOM	POSSIBLE CAUSE
Zero or Low Output Voltage (Continued)	<ul style="list-style-type: none"> g. Input connector P1 loosely connected h. Defective board or unit-in-latch (paragraph 5-46).
Unable to program output voltage or actual output does not coincide with programmed input.	<ul style="list-style-type: none"> a. Meter circuit defective. b. Flag or gate pulse not generated (paragraph 5-47). c. Voltage bits out of calibration (paragraph 5-71). d. Defective board (paragraph 5-46).
Able to program only a few voltages of each polarity	<ul style="list-style-type: none"> a. Defective board (paragraph 5-46).
Able to program at least some negative output voltages within the rating of the supply but no positive output voltages	<ul style="list-style-type: none"> a. Sign bit circuit defective (paragraph 5-47).
Able to program at least some positive output voltages within the rating of the supply but no negative output voltages	<ul style="list-style-type: none"> a. Sign bit circuit defective (paragraph 5-47).
Able to program all but a few voltages of each polarity	<ul style="list-style-type: none"> a. Voltage Processing circuits defective (paragraph 5-47).
Programmable current latch defective or unable to get unit out of current latch	<ul style="list-style-type: none"> a. A6 or A7 boards defective (paragraph 5-46).
Unit locked up (high positive output) or locked-down (high negative output)	<ul style="list-style-type: none"> a. Defective A7 board (paragraph 5-64).
Flag or gate pulse not being generated	<ul style="list-style-type: none"> a. Defective A1 board (paragraph 5-47).
Unable to program voltage range	<ul style="list-style-type: none"> a. A7K1 defective b. Defective A6 board (paragraph 5-55).
Programmable current latch defective (unable to program some values)	<ul style="list-style-type: none"> a. Defective A6 board (paragraph 5-55).
Unable to get unit out of current latch or unable to get unit into current latch	<ul style="list-style-type: none"> a. Defective A6 or A7 boards (paragraph 5-46).

Table 5-3 Overall Troubleshooting (Continued)

SYMPTOM	PROBABLE CAUSE
Poor Line Regulation	a. Power supplies faulty b. Marginal photo-isolators on board A1 (paragraph 5-53).
Poor Load Regulation	a. Power Supplies faulty b. Excessive voltage drop in sensing leads.

5-46. **Board Isolation Procedure.** The board isolation procedure describes how to isolate trouble to the power amplifier board A7, the control board A6, or to the voltage processing boards A1, A2, and A3. When the defective board(s) is located, further isolation is necessary before the trouble can be traced down to a particular circuit or component. Paragraphs 5-47 through 5-58 describe troubleshooting procedures on individual boards which isolate the trouble down to a component or circuit. The board isolation procedure assumes that an output voltage problem (zero or incorrect output voltage) exists. To isolate troubles to the defective board(s) proceed as follows:

1. Remove boards A2 and A3 from the DVS.
2. Remove load and connect voltmeter across HI and LO output terminals.
3. Connect Pocket Programmer to the data input connector and set its switches as follows:
 - a. Set the INPUT LEVEL REF switch to DATA COM.
 - b. Set the SOURCE SELECT switch to EXT.
 - c. Set the MP/DCPS switch to DCPS.
 - d. Set the RANGE switch to X1.
 - e. The voltage magnitude bit switches (0.5 through 8192), OUTPUT SIGN switch and I LATCH switches (L24, L22, and L23) may be left on either position (up or down) at this point in the procedure.
4. Turn on power apply a GATE pulse to the DVS and measure output voltage. Output should be 0 volts \pm 10mV. If output is not correct, troubleshoot the power amplifier board A7 (paragraph 5-64).
5. Connect a negative dc voltage ($-V_x$) between the ANLG IN and LO S terminals on the rear of the DVS. Connect (-) polarity to the ANLG IN terminal and (+) polarity to the LO S terminal as shown in Figure 5-7A. Note that the power amplifier in the DVS inverts this voltage and amplifies it by 1 in the X1 range and by 10 in the X10 range. The magnitude of the V_x input (maximum of 5V in

the X10 range) depends upon the trouble encountered. For example, if a high range output voltage cannot be programmed, apply a high range voltage to the analog input.

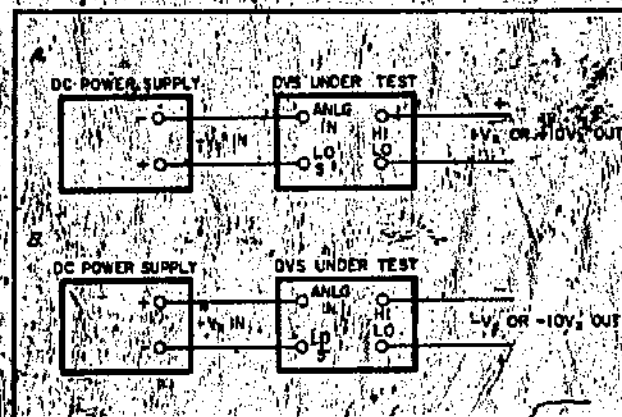


Figure 5-7. DVS Analog Input Connections

6. Measure the output voltage. Output should be $\pm 10V_x \pm 0.2\%$. If output is $+10V_x \pm 0.2\%$, proceed to step 7. If output is $+V_x \pm 0.2\%$, the problem is in the range circuits on board A6 (paragraph 5-61) or the range relay A7K1 is defective. If the output is not $+10V_x \pm 0.2\%$ or $+V_x \pm 0.2\%$ troubleshoot the A7 board (paragraph 5-64).

7. Connect a positive dc voltage ($+V_x$) between the ANLG IN and LO S terminals as shown in Figure 5-7B. Set the RANGE switch on the Programmer to X1.

8. Measure the output voltage. Output should be $-V_x \pm 0.2\%$. If output is $-V_x \pm 0.2\%$, proceed to step 9. If output is $-10V_x \pm 0.2\%$, the problem is in the range circuits on board A6 (paragraph 5-61) or the range relay A7K1 is defective. If output is not $-V_x \pm 0.2\%$ or $-10V_x \pm 0.2\%$, troubleshoot the A7 board (paragraph 5-64).

9. Turn off DVS and make the following test setup changes:

- a. Remove the A7 board and install it with the extender board (side A, position D) in the A7 slot.
- b. Connect a 50 Ω load in parallel with the voltmeter across the HI and LO output terminals.
- c. Connect $-V_X$ to ANLG IN as shown in Figure 5-7A.

10. Turn on DVS and measure output. Output should be less than 1 volt because the DVS should be in the latch condition. If output is less than 1V, proceed to step 12. If output is $+V_X$ (DVS is not in latch condition), proceed to step 11.

11. Measure the voltage across A7B92 (connect positive probe to base of A7Q25 and negative probe to Q^2) see Figure 7-B, sheet 3. If meter reads approximately $+0.7$ volts (one V_{BE} drop), the A7 latch circuit is defective (see paragraph 5-67). If meter reads less than one V_{BE} voltage drop, the A6 latch circuit is defective (see paragraph 5-58) provided A7Q25 is not shorted from base to emitter.

12. Apply a GATE pulse via the Pocket Programmer (14533B) to get the DVS out of the latch condition.

13. Measure output voltage. Output voltage should be $+V_X$. If output is not $+V_X$, the A7 latch circuits are defective (see paragraph 5-67).

14. Connect $+V_X$ to ANLG IN as shown in Figure 5-7B and measure the output voltage. Output voltage should be $-V_X$. If not $-V_X$, the A7 latch circuits are defective (see paragraph 5-67).

15. Turn off the DVS and make the following test setup changes:

- a. Remove A7/extender board and return A7 to its slot.
- b. Insert the A2 board in its slot.
- c. Install A3 with extender board (side A, positive A) in the A3 slot.
- d. Remove the input from the ANLG IN and LOS terminals.
- e. On the Pocket Programmer, set all voltage magnitude bits to the on position.

16. On the A3 board, check voltages at TP52 ($+16.384V \pm 1\%$), TP53 ($-16.384V \pm 1\%$), and TP55 ($21.5V \pm 5\%$). All voltages should be within tolerance. If not, check the associated regulating circuit on the A3 board.

17. On the Pocket Programmer, set all voltage magnitude bits to the off position.

18. Check voltages at TP52, TP53, and TP55 on the A3 board. Voltage changes should be as indicated below. If not, check associated regulating circuit on the A3 board. If voltages check out, perform the troubleshooting procedures for the voltage processing circuits (paragraph 5-47).

TP	ΔV
TP52	$\pm 0.5mV$
TP53	$\pm 0.5mV$
TP55	$\pm 100mV$

5-47. VOLTAGE PROCESSING CIRCUIT TROUBLESHOOTING

5-48. The following paragraphs should be helpful in locating any circuit failures on the A1, A2, or A3 boards. Paragraph 5-49 traces the voltage magnitude and sign bits through the three boards to locate data bit problems on the A1 and A2 boards or to isolate them to the A3 board. Paragraph 5-50 troubleshoots the A3 board in detail. Paragraph 5-51 troubleshoots the gate, flag, and storage strobe circuits on the A1 and A2 boards. Refer to Figure 7-2, sheet 1 when troubleshooting circuit failures on the A1, A2, or A3 circuit boards. Use the extender board (paragraph 5-4) to gain access to circuit board test points.

NOTE

For convenience, it is best to leave the A6 and A7 boards out of the unit while troubleshooting the voltage processing circuits.

5-49. A1 and A2 Board Troubleshooting. Assuming that the sign bit or one or more voltage magnitude bits do not affect the output of the D/A converter, the following steps will isolate the problem to a particular board.

a. Observe the voltage between common Q^3 and A1TP10 of the bit to be tested. Toggle the input bit. There should be two logic levels at TP10. If there are not, look for a problem in the programming source or its connector, in the A1 board connector, or in the input bias circuit.

b. Toggle the input bit while observing the voltage between common Q^4 and A1TP13. There should be two logic levels. If the voltage is zero, check for an open A1 or A2 board connector or an open resistor in A227 or A228. If the voltage remains near zero or about 5 volts, the problem is on the A1 board, either in the input bias circuit or the isolator circuit. For isolator circuit troubleshooting instructions, see paragraph 5-53.

c. To check for problems on the A2 board, switch to STORAGE DISABLE and check the voltage between A2TP97 (or A2TP51 for the sign bit) and common Q^4 while toggling the input bit. If there are not two logic levels, the storage IC is probably defective. But first check for a high logic level at A2TP9. If this level is low a storage disable circuit fault is indicated; see paragraph 5-51. If TP97 does exhibit two logic levels, the fault has been isolated to the A3 board. See paragraph 5-50 for A3 board troubleshooting instructions.

5-50. A3 Board Troubleshooting. If a problem has been isolated to the A3 board, first check the three voltages that are regulated on that board. (All

voltage measurements on A3 are referenced to common (2).

a. Measure the outputs of the +21.5-volt, +16.384-volt, and -16.384-volt supplies at test points TP55, TP52, and TP53. If any of these voltages is not within tolerance, check the regulating circuit for that particular voltage. Note that a shorted switching transistor (Q2 or Q3) can affect the +16.384-volt reference. If one of these two switching transistors is shorted, either a high or low, input respectively to Q1 will load down the positive reference through Q2 and Q3 in series. A Q2 or Q3 short can be detected by monitoring the +16.384-volt regulator output while toggling each input bit.

b. Program all voltage magnitude input bits to produce low inputs at the base of Q1 and measure the voltage at TP54 of each bit. The voltage at TP54 should be between zero and +8mV. If any bit is higher than +8mV, check Q1 and Q3.

c. Now program for high inputs at the base of Q1 and again measure the voltage at TP54 of each bit. All bits should be within 8mV of TP52 voltage. If any are lower than this voltage, check Q1 and Q2.

d. If all ladder network switching circuits are now operating properly, the voltage at TP54 of each bit can be alternated between the values specified above by toggling the input bit.

e. If the sign bit tested good at A2TP51 but does not affect the output of the A3 board, check transistors A3Q13 and A3Q14 in the polarity offset switch. A failure either here or in the -16.384-volt reference supply is likely.

NOTE

If any repair or adjustment of the power amplifier is required, that will have to be completed before the D/A converter can be performance tested or calibrated.

f. If steps (a) through (e) above confirm the proper operation of the A3 board voltage regulators, bit switches, and polarity offset switch, the only possible trouble area remaining on the D/A board is the resistive ladder network. An out-of-tolerance resistor in the ladder network will be detected only by attempting to calibrate the unit. Perform the calibration procedure of paragraph 5-71. If one or more bits cannot be calibrated, their identity should pinpoint the faulty resistor(s). If the -16.384-volt reference supply and polarity offset switch are operating but the polarity offset current adjustment (A3R18) will not bring the DVS output voltage to zero in step (p) of paragraph 5-72, A3R19 or A3Q14 is likely to be at fault.

5-51 Gate, Flag, and Storage Strobe Troubleshooting

The simplest method of troubleshooting these circuits is to trace signals with an oscilloscope while providing a gate input from a pulse generator. The pulse generator may be connected between common (3) and either the GATE input jack on the Pocket Programmer or A1TP1. The required pulse amplitude and polarity will depend on the instrument being tested. See the appropriate Option Appendix or the Instrument Modification sheet supplied with the instrument for this information. The minimum pulse width is 5 microseconds; a repetition rate of 400Hz or less is suitable. In the STORAGE mode, check waveforms at test points in the following order: TP2, 3, 4, 6, 7, 40, 31, 41, 42, 16, 43, 8, 9, and 28. In the STORAGE DISABLE mode, check voltages at TP9 and TP28. TP9 should be $\geq 2.4V$. TP28 should be $\leq 0.6V$ referenced to (4).

NOTE

When tracing signals at each test point, make certain to connect oscilloscope to proper common reference point, either common (3) or common (4).

CAUTION

(4) common is -26 volts off ground (2).

5-52 If the signal is lost at TP4, or TP40, one of the delay multivibrators (A1Z3 or A1Z4) or its power supply is at fault. The +5V₁ and +5V₂ supply voltages for A1Z3 and A1Z4 are derived from the +12V source supply and components on board A1 (see Figure 7-2, sheet 4). If the gate pulse isolator or flag isolator is at fault, see Paragraph 5-53 for isolator troubleshooting instructions.

5-53 PHOTO-ISOLATOR CIRCUIT TROUBLESHOOTING

5-54 Once a trouble has been localized to a particular photo-isolator circuit, following the steps of Table 5-4 or 5-5 will troubleshoot its three main semiconductor components without requiring the removal of any parts from the board. Although some of the photo-isolator circuits in the DVS differ in the means of input drive and some are followed by one or more stages of amplification or inversion, all are generally similar to the circuit, first make sure that all of the two or three dc supplies to the circuit are present. When this has been established, toggle the input bit and observe the collector voltage of the transistor that immediately follows the photo-isolator package (Q2 of Figure 5-8). The

choice of which table should be used depends on the results of that test. If the collector of that transistor remains at a logical high when the input bit is toggled, begin at step (1) of Table 5-4. If that collector remains at a logical low, begin at step (1) of Table 5-5.

NOTE

Marginal photo-isolators in the input circuits on the A1 and A6 boards can cause erroneous output voltage readings and current latch values when operating in the low or high limits of ac input voltage (see paragraph 5-16). This can be detected by programming all photo-isolators to turn-on then turn-on power to the DVS (at low line) and check the output of each storage flip-flop. Thus, the marginal photo-isolation can be detected and replaced.

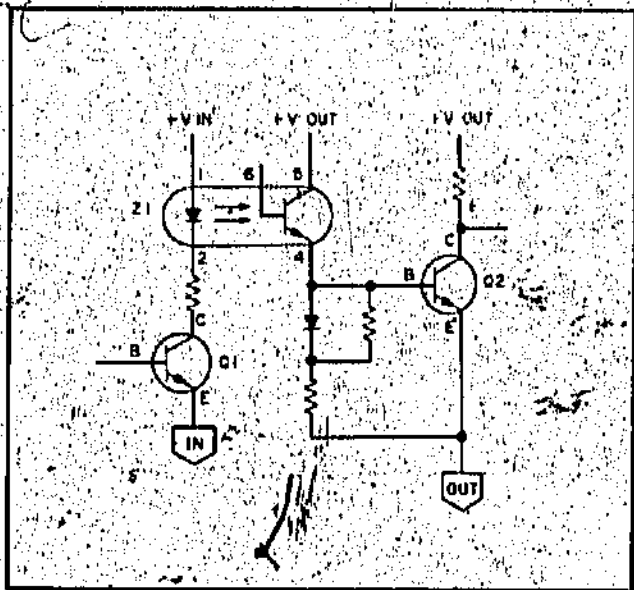


Figure 5-8. Representative Isolator Circuit

Table 5-4. Photo-Isolator Troubleshooting -- Output Remains High

NOTE: Refer to Figure 5-8 for component reference designations used in this table.

STEP	ACTION	RESPONSE	PROBABLE CAUSE
1.	Observe voltage between Q2 collector and OUT common. Shunt Z1 pin 4 to pin 5 momentarily with 1K Ω resistor.	a. Two logic levels present. b. Q2 collector still remain high.	a. Proceed to Step 2. b. Q2 opened. Replace Q2 and retest entire isolator stage. If output now remains low, proceed to Table 5-5.
2.	Observe voltage between Q1 collector and IN common. Toggle input bit.	a. Two logic levels present. b. High logic level only. c. Zero or low logic level only.	a. Z1 failure. b. Proceed to Step 3. c. Proceed to Step 4.
3.	Observe voltage between Q2 collector and OUT common. Short Q1 collector to emitter.	a. Q2 collector goes low. b. Q2 collector remains high.	a. Q1 opened. b. Q1 opened and Z1 failure.
4.	Connect short from Z1 pin 1 to pin 2. Observe voltage between Q1 collector and IN common. Toggle input bit.	a. Two logic levels present. b. Zero or low logic level only.	a. Z1 failure. b. Q1 shorted and Z1 failure.
NOTE: If failure persists, check for bridged or open P.C. conductors.			

Table 5-5. Photo-Isolator Troubleshooting — Output Remains Low

NOTE: Refer to Figure 5-8 for component reference designations used in this table.

STEP	ACTION	RESPONSE	PROBABLE CAUSE
1.	Observe voltage between Q2 collector and OUT common. Short Q2 base to emitter momentarily.	a. Two logic levels present. b. Q2 collector still remains low or zero.	a. Proceed to Step 2. b. Q2 shorted. Replace Q2 and retest entire Isolator stage. If output now remains high, proceed to Table 5-4.
2.	Observe voltage between Q2 collector and OUT common. Short Z1 pin 4 to pin 6 momentarily.	a. Two logic levels present. b. Q2 collector still remains low or zero. c. High logic level only.	a. Q1 shorted. Replace Q1 and proceed to Step 3. b. Z1 shorted. Replace Z1 and proceed to Step 3. c. Proceed to Table 5-4.
3.	Observe voltage between Q2 collector and OUT common. Toggle input bit.	a. Two logic levels present. b. Q2 collector remains low or zero. c. High logic level only.	a. Repair completed. b. Q1 shorted. Replace Q1 and repeat Step 3. c. Proceed to Table 5-4.
NOTE: If failure persists check for bridged or open P.C. conductors.			

5-55 A6 CONTROL BOARD TROUBLESHOOTING

5-56 Since the A6 Board handles many different signals, the troubleshooting for this board has been broken down according to input and output signals. Table 5-6 lists the possible trouble symptoms and directs the reader to the correct paragraph or table for further isolation. Before proceeding to Table 5-6 for the paragraph or table applicable to the trouble present, the following procedure should be used to determine if the trouble lies within the input circuits:

- a. Remove the A6 board and install it in the extender board. Install the extender board/A6 combination in the A6 board slot.
- b. Connect a voltmeter or logic probe between (2) common and TP75 of the bit to be tested.
- c. Set the STORAGE/DISABLE switch to DISABLE.
- d. Toggle bit to be tested. If two logic levels can be obtained proceed to Table 5-6. If only one logic level is present, proceed to Paragraphs 5-57, 5-58, and 5-59.

5-57 Current Latch Data Input Circuits Troubleshooting. The following procedure describes the process by which troubles in the current latch data input circuits may be isolated. The process consists of a series of fast checks of the input circuits up to and including the storage flip-flops A622.

5-58 To isolate troubles in the input circuits, proceed as follows:

1. Connect the common lead of an oscilloscope or logic probe to (3) common.
2. Connect the other lead to TP64 of each of the current latch input bits, and look for the presence of two logic levels as the switch for that bit is toggled. If only one logic level is found at TP64 for any of the bits, check the programming source for defect.
3. Disconnect the leads at TP64 and (3) and connect them to TP74 of each bit and (2). Check for the two logic levels as described in Step 2. If only one logic level is present for any of the bits, check the associated pull-up resistor (A621) and photo-isolator circuit (paragraph 5-53).

4. Disconnect the lead of the monitoring device of TP74 and connect it to TP75 of each bit. Check for the presence of two logic levels as described in Step 2. If two logic levels are not present for any of the bits, A6Z1 may be defective. See Paragraph 5-59 and 5-60.

5-59 Storage Gate Pulse Troubleshooting. First determine if the A2 STORAGE DISABLE switch and associated circuits are working by monitoring TP30 (Ref. ②) while switching from STORAGE to STORAGE DISABLE. If two logic levels are present these circuits are working on a "static" level; otherwise check the Interconnect Board (A5) and Logic Board (A2) and A6Q4, Q5, Q6 as follows. With A2S1 in the STORAGE position, apply a pulse train to the GATE input terminal J1 pin 32. Check for the presence of a pulse by connecting an oscilloscope or logic probe to ② common and TP's 28, 69, 70 and 30 in order. Note that TP28 is approximate -26 volts with respect to ② and ② is connected to the Low Sense terminal on the rear barrier block. Low Sense is typically connected to chassis ground ($\frac{1}{2}$). If a point is reached at which the pulse is not present, it may be assumed that the transistor (or related components) just before this point is defective. If the gate pulse is traced through to TP30, it is likely that A6Z2 is defective and must be replaced. Before replacing A6Z2 ensure that +4.99V supply voltage is present at A6Z2, pin 5. If not, check the +4.99V supply components (see Figure 7-2, sheet 4).

5-60 Voltage Range Troubleshooting. To troubleshoot the voltage range circuits, the following procedure is recommended:

1. Connect the common lead of oscilloscope or logic probe to ③ common.
2. Connect the other lead of TP65 and check, by toggling the appropriate switch, for the presence of two logic levels. If only one logic level is present, check the Interconnect board for continuity and ensure that the programming device is connected properly.
3. Disconnect the leads of the monitoring device at TP65 and ③ and connect to TP76 and ② respectively observing the presence of two logic levels as described in Step 2. If only one logic level is present, check the A6A4 photo-isolator circuit (paragraph 5-53). Also check network A6Z1.
4. Disconnect the lead of the monitoring device from TP76 and connect to TP73 checking for the presence of two logic levels as in Step 2. If only one logic level is present, it is likely that A6Z1 or A6Z2 is defective.
5. Disconnect the lead of the monitoring device from TP73 and connect to TP77 observing the presence of two logic levels as in Step 2. If only one logic level is present, check A6Q25 for an open or short circuit. If 2 logic levels are present, the

trouble lies within the A7 board (A7K1 or A7K2).

5-61 Negative Programmable Output Current Latch Defective. If the unit will current latch for positive output currents, but not for negative output currents; or, if the unit is in current latch for all values of negative output current and works correctly for positive output current latch settings, the cause of trouble must be in a circuit which handles the flow of the negative current latch signal. There are two stages which handle the negative output current latch signal, A6Z4 and A6CR1.

5-62 Positive Programmable Output Current Latch Defective. If the unit will current latch for negative output currents, but not for positive output currents; or, if the unit is in current latch for all values of positive output current and works correctly for negative output current latch settings, the cause of trouble must be in a circuit which handles the flow of the positive current latch signal only. There are three stages which handle only the positive output current latch signals, A6Z4, A6CR2 and the Negative Reference Inverter (A5Z3, A6Q23, and associated components). Check A6Z4 and A6CR2 first. If these two components are operative, the trouble probably lies in the negative reference inverter. Check A6Z4 and A6CR2 for open or shorted junctions.

5-63 Current Latch Decoder Troubleshooting. To troubleshoot the current latch decoder circuit, the following procedure is recommended:

1. Connect voltmeter positive lead to the NEG REF (TP100) on board A6 and the common lead to TP99. Turn unit on and GATE unit. Set the STORAGE DISABLE switch on A2 to DISABLE.
2. Set the current latch to each value and check that the associated voltage reading is as indicated below:

Current Latch Value (mA)	Voltage Reading (mV) $\pm 10\%$, $\pm 17mV$
20	+25
50	+62.5
70	+87.5
100	+125
200	+250
500	+625
700	+875
1000	+1250

3. If all voltages are incorrect, check current latch decoder stage A6Q1 and the negative reference resistor A6R30. If any voltage reading or combination of voltage readings are incorrect, refer to Table 5-7. Also, check the current latch calibration (paragraph 5-79).
4. Connect voltmeter positive lead to the

3 RTT (TP101) on board A6 and the common lead to TP99.

5. Set the current latch to a value of 1000mA and check that voltmeter reads -1.250V \pm 10%. If

reading is incorrect, check the negative reference inverter (A6Q23, Z3) and the positive reference resistor A6R37. Also, check the current latch calibration (paragraph 5-79).

Table 5-6. A6 Troubleshooting Guide

SYMPTOM	A6 TROUBLESHOOTING SECTION
Unit always in current latch	Proceed to Table 5-8
Unable to current latch at turn-on	Proceed to Table 5-9
Unable to current latch at latch setting	Proceed to Table 5-10
Current latch operating properly but latch status is always in the same state (on or off)	Proceed to Table 5-11
Current latch operating properly but overload status is always in the same state (on or off)	Proceed to Table 5-12
Storage gate pulse defective	Proceed to paragraph 5-59
Voltage range defective	Proceed to paragraph 5-60
Positive output current latch defective	Proceed to paragraph 5-62
Negative output current latch defective	Proceed to paragraph 5-61
Flag is not generated for both range switching and overload conditions *	Check the overload/range flag isolator (A6Q31, Q32, Q33, and Z5).
Flag is not generated when range is switched but is generated for an overload condition *	Check 2 millisecond delay circuit (A6CR12, CR13, CR16, Q26, Q27, Q28).
Flag is not generated for an overload condition but is generated when range is switched *	Check overload flag generator (A6CR14, CR15, Q29, Q30).

* Overload Flag is disabled for J20 Option

Table 5-7. Current Latch Decoder Troubleshooting Guide

SYMPTOM	PROBABLE CAUSE
Current latch defective for all values	A6Q1, Q8-Q15, or Z2 defective.
Current latch defective only for the following values: 20, 70, 200, 700mA	A6Q3 opened, Q13 or Q15 shorted.
Current latch defective only for the following values: 50, 100, 500, 1000mA	A6Q3 shorted, Q13 or Q15 opened.

Table 5-7. Current Latch Decoder Troubleshooting Guide (Continued)

SYMPTOM	PROBABLE CAUSE
Current latch defective only for the following values: 20, 50, 200, 500mA	A6Q2 opened, Q12 or Q14 shorted
Current latch defective only for the following values: 70, 100, 700, 1000mA	A6Q2 shorted, Q12 or Q14 opened
Current latch works for 20 or 200mA but does not work for both.	A6Q8 defective
Current latch works for 50 or 500mA but does not work for both.	A6Q10 defective
Current latch works for 70 or 700mA but does not work for both.	A6Q9 defective
Current latch works for 100 or 1000mA but does not work for both.	A6Q8, Q9, Q10 defective

Table 5-8. Unit Always In Current Latch

NOTE: Logic level "1" equals a positive voltage, logic level "0" equals approximately 0V.

STEP	ACTION	RESPONSE	CONCLUSION
1	Connect voltmeter common to Ⓜ . Remove load and ensure that output terminals are not shorted. Turn unit on and Gate unit. Check TP21.	a. Logic level "0" b. Logic level "1"	a. Current latch circuit on A6 board operating properly, check current latch circuit on A7 board (paragraph 5-67). b. Ensure that input plug P1 is connected. Proceed to Step 2.
2	Check TP20.	a. Voltage magnitude equals approximately -5V. b. Logic level "1"	a. Buffer stage A6Q21 probably working, go to Step 3. b. Check A6Q21 for open.
3	Check TP14.	a. Logic level "1" b. Logic level "0"	a. Reset amplifier working, check A6Q20 for open. If A6Q20 not open, go to Step 4. b. Check Reset Amplifier A6Q24 for short.

Table 5-8. Unit Always in Current Latch (Continued)

STEP	ACTION	RESPONSE	CONCLUSION
4	Check TP98	a. Logic level "0" b. Logic level "1"	a. Relay A4K1 probably working, go to Step 5. b. Relay A4K1 defective causing false setting of latching flip-flop A6Q19, Q20.
5	Connect voltmeter common to $\textcircled{2}$. Check TP19	a. Logic level "1" b. Logic level "0"	a. Latching flip-flop probably working, go to Step 6. b. Check A6Q19 for short.
6	Check TP18	a. Logic level "1" b. Logic level "0"	a. Level detector A6Q17 and A6Q18 probably good, go to Step 7. b. Check A6Q17 for short and A6Q18 for open.
7	Check TP17	a. Voltage magnitude $+0.5V$ b. Logic level "1"	a. Variable delay A6Q16 probably operating, go to Step 8. b. Check A6Q16 for open.
8	Connect voltmeter common to TP99 and check TP15	a. Voltage magnitude is less than 20mV. b. Voltage magnitude is more than 20mV	a. Current sampling circuit operating properly, go to Step 9. b. Check current sampling resistor and interconnect wires.
9	Connect voltmeter common to $\textcircled{2}$. Check TP35	a. Logic level "1" b. Voltage magnitude equals approximately $-13V$.	a. Negative current comparator is operating properly, go to Step 10. b. Check current latch decoder (see para. 5-63). If current latch decoder circuits are operating properly check the negative current comparator circuit (A6Z4, R39, R33, R31).
10	Check TP36	a. Logic level "1"	a. Positive current comparator is operating properly, check OR gate (A6CR1, CR2) for shorts.

Table 5-8. Unit Always in Current Latch (Continued)

STEP	ACTION	RESPONSE	CONCLUSION
10	Check TP36 (Continued)	b. Voltage magnitude equals approximately -13V.	b. Check current latch decoder (see para. 5-63). If current latch decoder circuits are operating properly, check the positive current comparator (A6Z1, R32, R34, R43) and the negative reference inverter (A6Q3, Z3).

Table 5-9. Unable to Current Latch at Turn-On

NOTE: Positive voltage equals logic level "1"; logic level "0" equals approximately 0V.

STEP	ACTION	RESPONSE	CONCLUSION
1	Turn unit off. Measure impedance between $\textcircled{2}$ and TP98.	a. Impedance $\geq 5K\Omega$ b. Impedance $< 5K\Omega$	a. Relay A4K1 probably working, go to Step 2. b. Relay A4K1 defective causing false resetting of latching flip-flop.
2	Connect voltmeter common to $\textcircled{2}$. Turn unit on (Do not GATE). Check TP21.	a. Logic level "0" b. Logic level "1"	a. No latch, go to Step 3. b. Latch circuit on A6 board is operating, check latch circuit on A7 board (paragraph 5-67).
3	Check TP20	a. Logic level "1" b. Voltage magnitude equals approximately -5V.	a. Buffer stage A6Q21 probably working, go to Step 4. b. Buffer stage A6Q21 not working, check A6Q21 for short.
4	Check TP14	a. Logic level "0" b. Logic level "1"	a. A6Q20 probably working. Reset amplifier may be defective. Check A6 Q24 for short and A6Q22 for open. If reset amplifier is working properly, go to Step 5. b. Check A6Q20 for short.
5	With an oscilloscope, observe operation of A4K1 (TP98) and turn-on of power (TP88). Both referenced to $\textcircled{2}$.	a. TP98 goes low $\approx 200\text{ms}$ after power on. b. TP98 goes low $< 200\text{ms}$ after power on.	a. Delay for A4K1 working; check complete. b. Check -12V delayed circuit especially A6C10, CR22 for shorts (see Figure 7-2, sheet A).

Table 5-10. Unable to Current Latch at Latch Settings

NOTE: Logic level "1" equals a positive voltage, logic level "0" equals approximately 0V.

STEP	ACTION	RESPONSE	CONCLUSION
1	Turn unit off. Measure impedance from TP18 to (2) (connect positive meter lead to TP18)	a. Impedance > 1K b. Impedance < 1K	a. Go to Step 2 b. CT terminals on barrier strip are shorted or electrolytic capacitor used is connected with reverse polarity.
2	Short the output terminals and turn unit on. Program the current latch and voltage magnitude values in question then Gate unit.	a. Output current < 20mA b. Output current $\geq 100\%$ of rated output	a. Check completed. Problem caused by improper setting of current latch value or current latch not calibrated (see paragraph 5-79) b. Latch circuits not working, go to Step 3.
3	Connect meter common to (2) and check TP21.	a. Logic level "1" b. Logic level "0"	a. Current latch circuits on A6 board operating properly, check current latch circuit on A7 board (see paragraph 5-67) b. A6 latch circuits not working, go to Step 4.
4	Check TP20.	a. Logic level "1" b. Voltage magnitude equals approximately -5V	a. Buffer stage A6Q21 probably working, go to Step 5. b. Check Buffer Stage A6Q21 for short.
5	Check TP19.	a. Logic level "0" b. Logic level "1"	a. Latching flip-flop probably working, go to Step 6. b. Check latching flip-flop transistor A6Q20 for short and A6Q5 for open.
6	Check TP18.	a. Logic level "0" b. Logic level "1"	a. Level detector (A6Q17, Q18) probably working, go to Step 7. b. Level detector not working, Check A6Q17 for open and A6Q18 for short.
7	Check TP17.	a. Logic level "1" b. Voltage magnitude < +0.5V	a. Variable delay A6Q16 probably working, go to Step 8. b. Check A6Q16 for short.

Table 5-10. Unable to Current Latch at Latch Settings (Continued).

NOTE: Logic level "1" equals a positive voltage, logic level "0" equals approximately 0V.

STEP	ACTION	RESPONSE	CONCLUSION
8	Check TP35 and TP36	a. Both logic level "1" b. Either equals approximately -13V. c. Both equal approximately -13V.	a. Go to Step 9 b. CR1, CR2, or VR2 open c. CR1 and CR2 open, go to Step 9.
9	Connect voltmeter common to TP99 and check TP15	a. Voltage magnitude equals 1.25V $\pm 10\%$ b. Voltage magnitude does not equal 1.25V $\pm 10\%$	a. Current sampling circuit operating properly, go to Step 10. b. Check current sampling resistor and interconnections.
10	Set current latch to 1000mA. With voltmeter common connected to TP99, check the NEG REF (TP100).	a. Voltage equals $+1.25V \pm 10\%$ b. Voltage does not equal $+1.25V \pm 10\%$	a. Current latch decoder operating properly. Check the negative current comparator (A624, R31, R33, R32). Proceed to Step 11. b. Check current latch decoder (see paragraph 5-63).
11	Check POS REF (TP101) with meter common connected to TP99	a. Voltage equals $-1.25V \pm 10\%$ b. Voltage does not equal $-1.25V \pm 10\%$	a. Negative reference inverter operating properly. Check positive current comparator (A624, R32, R34, and R43). b. Check negative reference inverter (A623, Q23).

Table 5-11. Latch Status Troubleshooting

STEP	ACTION	RESPONSE	CONCLUSION
1	Check the operation of A6A5Q4 by first shorting A6A5Q3 emitter to base and then emitter to collector. Monitor the output with a voltmeter *connected between TP22 and (3) common.	a. Only one logic level present b. Two logic levels present	a. A6A5Q4 defective or A6A5Q3 shorted b. Remove short and proceed to Step 2.

*If there is no pull-up resistor (A6A5R8), use an ohmmeter.

Table 5-11. Latch Status Troubleshooting (Continued)

STEP	ACTION	RESPONSE	CONCLUSION
2	Check the operation of A6A5Q3 by shorting A6A5Q2 first emitter to collector and then emitter to base. Monitor the output after each operation as described in Step 1.	a. One logic level present b. Two logic levels present	a. A6A5Q3 defective or A6A5Q2 shorted b. Remove short and check the operation of the latch status photo isolator circuit (see paragraph 5-53).

Table 5-12. Overload Status Troubleshooting

STEP	ACTION	RESPONSE	CONCLUSION
1	If A6A6Q4 is in the circuit (see modifications sheet) test its operation by first shorting A6A6Q3 emitter to base. Monitor the output with a voltmeter * connected between TP25 and (3) common after each operation.	a. Only one logic level present b. Two logic levels present	a. A6A6Q4 defective or A6A6Q3 shorted. b. Remove short and proceed to Step 2.
2	Check the operation of A6A6Q3 by shorting A6A6Q2 first emitter to collector and then emitter to base. Monitor the output after each operation as described in Step 1.	a. One logic level present b. Two logic levels present	a. A6A6Q3 defective or A6A6Q2 shorted. b. Remove short and check the operation of the overload status photo-isolator circuit (see paragraph 5-53).

* If there is no pull-up resistor (A6A6R8), use an ohmmeter.

5-64 A7 POWER AMPLIFIER BOARD TROUBLESHOOTING

5-65 Before attempting to troubleshoot the power amplifier, it is important to classify the kind of trouble present according to the trouble symptoms. Generally, troubles in the A7 board generate two broad categories of symptoms: current latch problems and output voltage problems. For example, if output voltages can be programmed with no load but no current can be drawn when a load is added, the problem is most likely a current latch type. However, if output voltages cannot be programmed without a load, the problem is probably an output voltage type.

5-66 The A7 troubleshooting procedures thus, are divided into two categories according to fault symptoms. The symptoms listed in Table 5-3 can be related to these two categories.

5-67 Current Latch Troubleshooting. Current latch problems on the A7 board can be caused by the current latch circuits themselves (the current latch isolators and switch circuits) or subsequent circuits including the power amplifier, power output, or positive and negative bias circuits. Figure 5-9A presents a procedure for dividing the fault path between either the A7 current latch circuits or the power circuits. If this procedure indicates the fault is in the current latch circuits, Figure

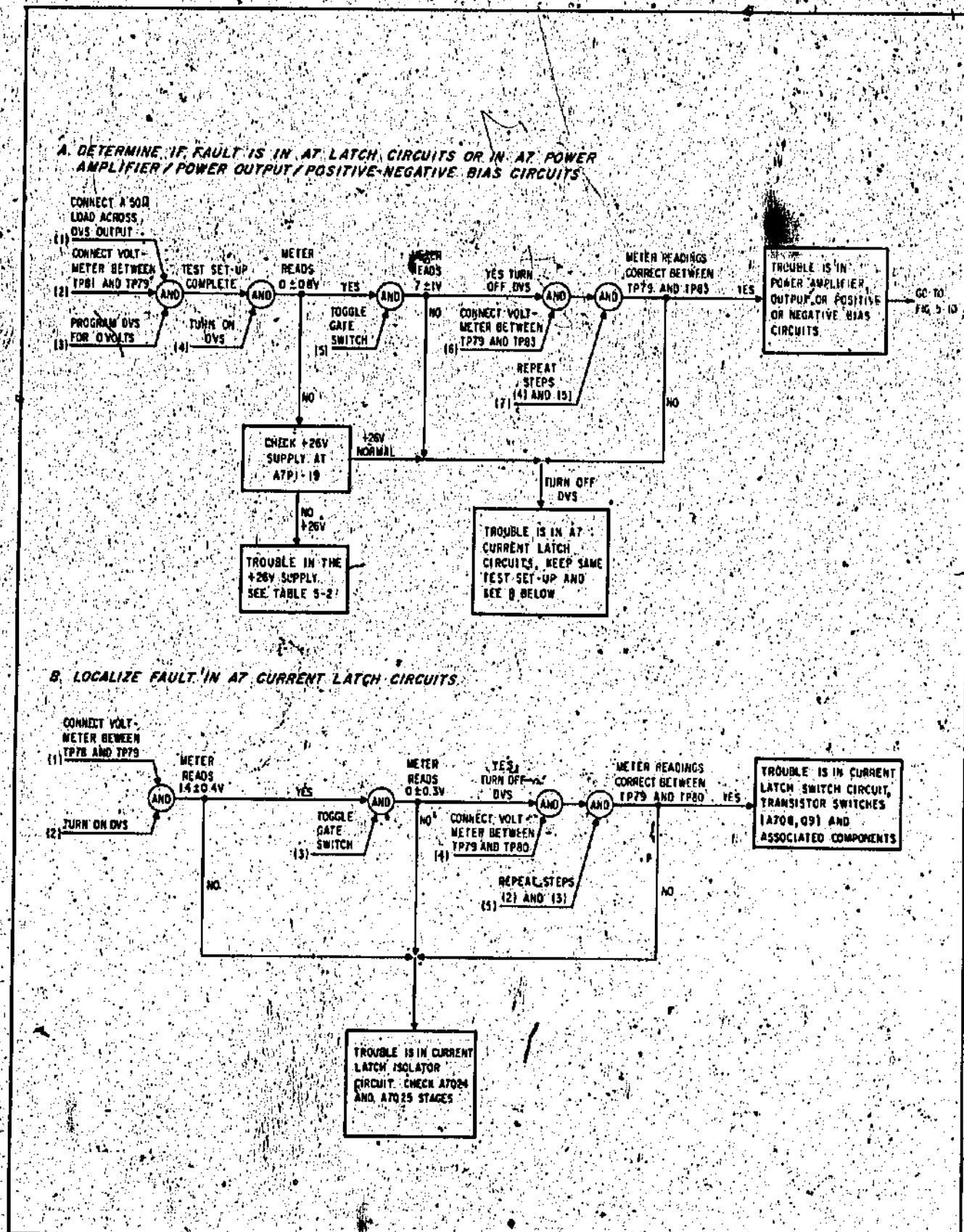


Figure 5-9. A7 Power Amplifier Current Latch Troubleshooting

5-9B provides a procedure for localizing the fault to either the current latch isolator or the current latch switch stages. If the procedure of Figure 5-9A indicates that the fault is in the power circuits, the procedure given in Figure 5-10 can be used to localize the fault to the defective stage within the power circuits.

5-68 Output Voltage Troubleshooting. The power amplifier contains four functional circuits (current latch, gross current limit, feedback differential amplifier, and power amplifier), any one of which can cause a failure in output voltage (the failure being that output voltage is locked up or down—full positive or full negative or zero). The first step in troubleshooting then, is to isolate the trouble to one of the four circuit groups. Once this is accomplished, the defective part of the faulty circuit can be located by more detailed troubleshooting. The following procedures will isolate trouble to one of the four circuit groups by systematically eliminating each circuit from the loop, one at a time, and noting if the output voltage returns to normal after each circuit isolation.

1. Disconnect the load and insure that the output terminals are not short circuited.
2. Program for 0V output.
3. Isolate the gross current limiters from the loop by opening the connection from A7CR28 and CR29 to the base of A7Q6.
4. Program the output voltage 50 volts

above and below 0 volts, in 5 volt steps.

5. If the original trouble still exists, reconnect the gross current limiters and proceed to Step (6). If the original trouble is eliminated, turn the DVS off and troubleshoot the gross current limiters (Table 5-13).
6. Isolate the current latch circuits by opening the connection from diodes A7CR15 and CR20 to the power amplifier.
7. Repeat Step (4).
8. If the original trouble still exists, reconnect the current latch circuits and proceed to Step (9). If the original trouble is eliminated, turn the DVS off and troubleshoot the current latch circuits (Paragraph 5-67).
9. Strap A7Q6 emitter to base. Connect a 25K Ω resistor between emitter and collector of A7Q6. Make sure programming source is connected.
10. Program for 0V output.
11. Read and record output voltage.
12. Remove strap and resistor from A7Q6.
13. If the output reading in Step 11 was 0 ± 10 volts and the unit is locked down, proceed to Table 5-14. If reading in Step 11 was 0 ± 10 volts and the unit is locked up, proceed to Table 5-15. If the reading in Step 11 was greater than 0 ± 10 volts proceed to Step 14.
14. Remove input power. Check A7Q7 and Q18 through Q17 for defect.
15. Check power output transistors Q1 through Q4 for defect.

Table 5-13. Gross Current Limiters Troubleshooting

STEP	ACTION	RESPONSE	CONCLUSION
1	With the load removed from the DVS, the output programmed for 0V, and the gross current limiters disconnected from the base of A7Q6, monitor the voltage at the anode of A7CR28.	$-7 \pm 1Vdc$	If the monitored voltage is positive, the negative gross current limiter is locked in the limiting state. Check A7Q18-20.
2	Monitor the voltage at the cathode of A7CR29.	$-3 \pm 1Vdc$	If the monitored voltage is excessively negative, the positive gross current limiter is locked in the limiting state. Check A7Q21-23.
3	Again monitor the voltage at the anode A7CR28, but this time connect a 50 Ω , 50 watt load and increase output to a positive level sufficient to draw + 1.1A.	Monitored voltage switches to $+12 \pm 1Vdc$	If the voltage does not switch, the negative gross current limiter is not limiting. Check A7Q18-20.

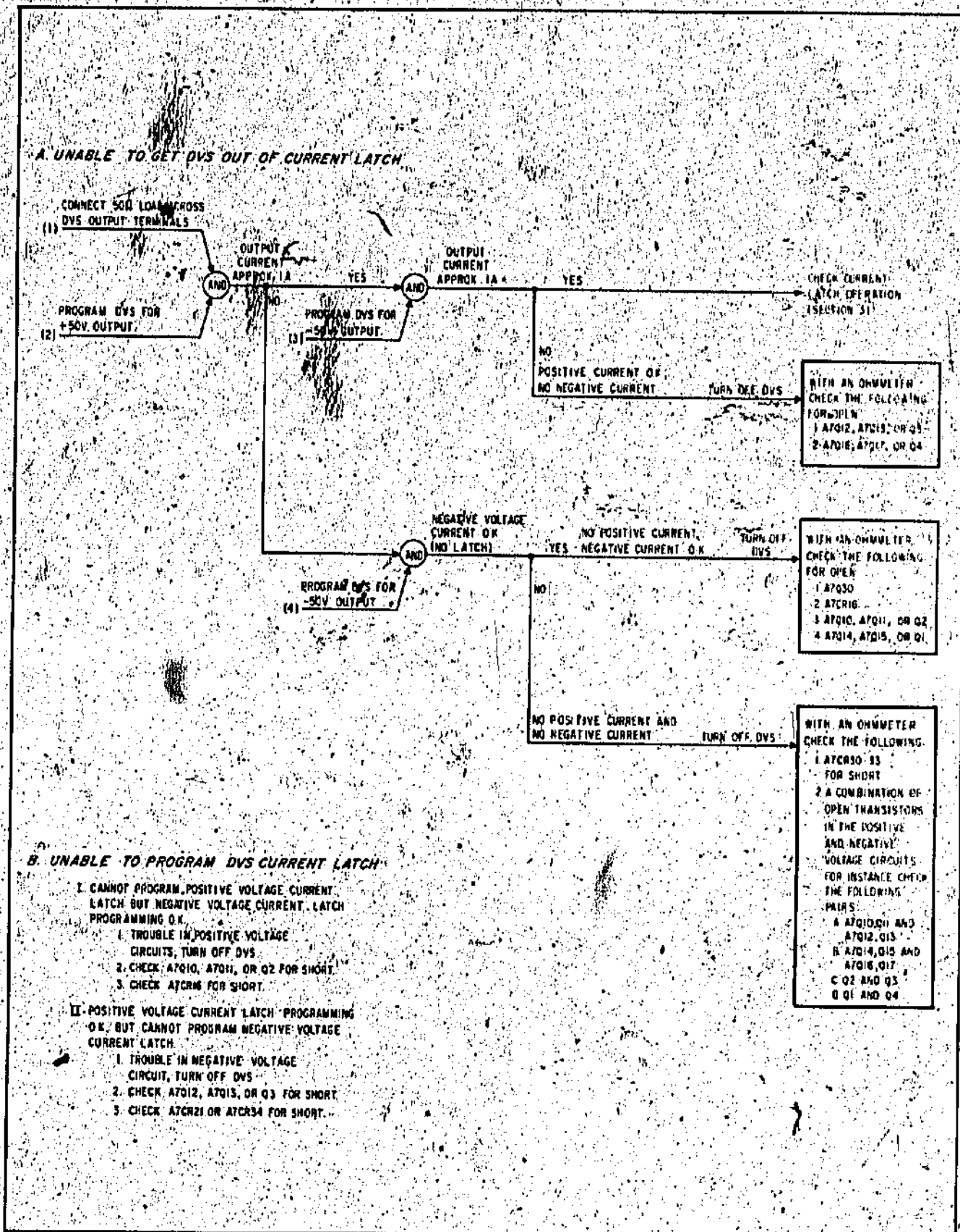


Figure 5-10. Localize Current Latch Trouble

Table 5-13. Gross Current Limiters Troubleshooting (Continued)

STEP	ACTION	RESPONSE	CONCLUSION
4	Repeat Step 3, expect monitor the voltage at the cathode of CR29 and increase negative output voltage to draw -1.1A.	Monitored voltage switches to $-12 \pm 1Vdc$.	If the voltage does not switch, the positive gross current limiter is not limiting. Check A7Q21-23.

Table 5-14. Feedback Differential Amplifier Troubleshooting, Unit Locked Down (Full Negative)

STEP	ACTION	RESPONSE	CONCLUSION
1	Short A7Q5 emitter to collector	a. Output voltage remains low b. Output voltage increases	a. A7Q6 shorted. b. Remove short and proceed to Step 2.
2	Short A7Q4 emitter to collector	a. Output voltage remains low b. Output voltage increases	a. A7Q5 opened. b. Remove short and proceed to Step 3.
3	Short A7Q3 base to emitter	a. Output voltage remains low b. Output voltage increases	a. A7Q4 opened, A7Q3 shorted. b. Remove short and proceed to Step 4.
4	Short A7Q1B emitter to collector	a. Output voltage remains low b. Output voltage increases	a. A7Q2 defective b. Remove short. Check A7Q1A for short and Q1B for open.

Table 5-16. Feedback Differential Amplifier Troubleshooting, Unit Locked Up (Full Positive)

STEP	ACTION	RESPONSE	CONCLUSION
1	Short A7Q31 base to emitter.	a. Output voltage remains high. b. Output voltage decreases.	a. A7Q31 probably good. Go to Step 2. b. A7Q31 open.
2	Short A7Q5 emitter to base.	a. Output voltage remains high. b. Output voltage decreases.	a. A7Q5 opened; A7Q5 shorted. b. Remove Q5 short and proceed to Step 3.
3	Short A7Q2B emitter to collector and A7Q24 emitter to base.	a. Output voltage remains high. b. Output voltage decreases.	a. A7Q4 shorted; A7Q3 opened, or A7Q2A shorted. b. Remove Q2 shorts and proceed to Step 4.
4	Short A7Q1A emitter to collector; A7Q1B emitter to base.	a. Output voltage remains high. b. Output voltage decreases.	a. A7Q2B opened or A7Q1B shorted. b. Remove shorts. Check A7Q1 for defects.

5-69 ADJUSTMENT AND CALIBRATION

5-70 Adjustment and calibration may be required after performance testing, troubleshooting or repair and replacement. Perform only those adjustments that affect the operation of the faulty circuit and no others. All the controls referred to in these adjustments are shown on the component location diagrams in Section VII.

5-71 OUTPUT VOLTAGE ADJUSTMENT

5-72 Before proceeding to the following adjustment procedures, make the following preparations:

1. Strap the following terminals on the rear terminal strip of the DVS:

- a. LO to LO S to GND
- b. HI to HI S

2. Connect the Pocket Programmer to the data input connector and set its switches as follows:

- a. Set the INPUT LEVEL REF switch to DATA COM.
- b. Set the MP/DCPS switch to DCPS.
- c. Set the SOURCE SELECT switch to EXT.
- d. Set the RANGE switch to X1.
- e. Set the data and sign bit switches for an output of -0.5mV. (Refer to the appropriate Option Appendix for the correct data and sign bit coding).

- f. Set the LIMIT switches for a 100mA limit (all three switches down).
- g. Set the switch on the A2 board to the STORAGE DISABLE position.
- h. Connect a digital voltmeter across the HI S and LO S output terminals.
- i. Turn on DVS and momentarily depress GATE switch on Pocket Programmer to deactivate the current latch circuit.
- j. With the DVS programmed for an output of -0.5mV, test the voltage processing circuits by individually turning on each bit and observing the relative change in output voltage associated with each bit value. If any voltage bits are not functioning, calibration can not be accomplished (refer to troubleshooting procedures, paragraph 5-37). If all voltage bits are functioning, proceed as follows:

-0.5 MILLIVOLT CALIBRATION

- a. Turn DVS off. Remove bottom cover in order to gain access to potentiometer A7 R9. Note that if the DVS is installed in a system, both the A3 and A7 boards must be placed in extender boards to perform this calibration.
- b. Set all of the potentiometers on the A3 board (A3R18, A3R36, A3R52 through A3R59, and A3R100) to midrange.
- c. Set the data and sign bit switches on the Programmer for an output of -0.5mV.
- d. Turn on DVS and momentarily depress GATE switch on the programmer. Allow a 30-minute DVS warm-up period.

CAUTION

High voltages are present on the amplifier board A7.

- e. Set the RANGE switch on the Programmer to the X10 position and measure the output voltage.
- f. Set the RANGE switch to the X1 position and adjust A7R9 until a reading 1/10 the reading in step (e) is obtained.
- g. Repeat steps (e) and (f) until no further adjustments are needed.
- h. Set the RANGE switch to the X10 position and adjust A3R100 for a reading of -5mV \pm 1mV.
- i. Repeat steps (e) through (h) until no further adjustments are needed.

POSITIVE 16.384 VOLT REFERENCE ADJUST

- j. On the Programmer, set the RANGE switch to X1 and the OUTPUT SIGN switch for negative

polarity.

- k. Connect a digital voltmeter across capacitor A3C30.
- l. Adjust A3R36 for a reading of 16.396 \pm .003V.

INDIVIDUAL BIT CALIBRATION

m. The individual bits are adjusted in two groups (8192, 4096, 2048, 1024, and 512, 256, 128, 64) according to the table below. The adjustment of all bits in the first group should be completed before proceeding to the second group. If any potentiometer in a group is adjusted to its end stop, continue adjusting the remaining potentiometers in the group and then back off 10% on the potentiometer that reached its end stop. Reprogram the bit associated with the potentiometer that was adjusted to its end stop and then adjust A3R36 for the correct output voltage level. If A3R36 must be adjusted, the entire bit calibration procedure must be repeated.

Voltage Bit	Meter Reading	Potentiometer
8192	-8192.5mV \pm 100 μ V	A3R52
4096	-4096.5mV \pm 100 μ V	A3R53
2048	-2048.5mV \pm 100 μ V	A3R54
1024	-1024.5mV \pm 100 μ V	A3R55
512	-512.5mV \pm 30 μ V	A3R56
256	-256.5mV \pm 30 μ V	A3R57
128	-128.5mV \pm 30 μ V	A3R58
64	-64.5mV \pm 30 μ V	A3R59

- n. Check each of the remaining bits (32mV, 16mV, 8mV, 4mV, 2mV, 1mV, and 0.5mV) to insure that they are within \pm 200 μ V. If not, check the associated switching transistors and ladder network on the A3 board (see Figure 7-2, sheet 1).

POSITIVE ZERO VOLTAGE AND X10 FEEDBACK RESISTOR ADJUSTMENT CALIBRATION

- o. Set the data and sign bits on the Programmer for an output of 0 volts.
- p. Adjust A3R18 for 0V \pm 100 μ V.
- q. Turn on the 4096 bit and observe the voltage reading.
- r. Set the Programmer RANGE switch to X10 and adjust A7R85 for 10 times and the reading in Step (q) \pm 1mV.
- y. Repeat Steps (p) through (r) until no further adjustments are necessary.
- t. Turn off DVS and replace bottom cover or remove extender boards and replace boards as applicable.

5-73 METER ZERO

5-74 To zero-set either the voltmeter or ammeter, proceed as follows:

- a. Turn the instrument off. Wait one minute for power supply capacitors to discharge completely.
- b. Insert sharp object (pen point or awl) into the small indentation near the top of the round black plastic disc located directly below the meter face.
- c. Rotate the disc until meter reads exactly zero.

5-75 VOLTMETER ADJUSTMENT

5-76 To adjust the calibration of the DVS voltmeter, proceed as follows:

- a. On the Pocket Programmer, set the data bits, OUTPUT SIGN, and RANGE switches for a voltage output of +10V.
- b. Turn on DVS and press GATE switch on Programmer.
- c. Set the DVS front panel VOLTAGE control to the 10V position and adjust A4R14 until meter reads +10V.
- d. Set the data bit, OUTPUT SIGN, and RANGE switches for an output voltage of -10V. The voltmeter should read -10V.
- e. If it does not, halve the error and adjust A4R14 accordingly.

5-77 AMMETER ADJUSTMENT

5-78 To adjust the calibration of the DVS Ammeter proceed as follows:

- a. Connect a 10 ohm, 10 watt, 1% resistor across the HI and LO output terminals.
- b. On the Programmer set the data bit, OUTPUT SIGN, and RANGE switches for an output voltage of +10V.
- c. Turn on DVS and press GATE switch on Programmer.
- d. Set the DVS front panel CURRENT switch

to 1.2A and adjust A1R24 until ammeter reads +1A.

- e. Set the data bit, OUTPUT SIGN, and RANGE switches for an output voltage of -10V. The meter should read -1A.
- f. If it does not, halve the error and adjust A1R24 accordingly.

5-79 CURRENT LATCH ADJUSTMENT

5-80 To calibrate the accuracy of the current latch circuit, proceed as follows:

- a. Remove the A6 control board and using the extender board, place A6 in the extended position. Short the C_T terminals (rear barrier strip).
- b. Connect a voltmeter across A6A6Q3 (Figure 7-2, Sheet 2). Connect meter positive to collector and common to emitter of A6A6Q3. When current latch occurs, the voltmeter will read approximately 0.7 volts.
- c. Attach a 50 ohm, 50 watt, 1% load resistor across the HI and LO output terminals.
- d. Set the switches on the Pocket Programmer for an output voltage of -1.00V and a current latch of 20mA.
- e. Adjust potentiometers A6R19, R20, R21, and R108 fully clockwise.
- f. Turn on DVS and press GATE switch on Pocket Programmer. Allow a 30-minute DVS warm-up period.
- g. Adjust A6R19 ccw until the voltmeter indicates approximately 0.7V.
- h. Program the voltage to -02.50V and the current latch to 50mA.
- i. Adjust A6R21 ccw until the voltmeter indicates approximately 0.7V.
- j. Program the voltage to -03.50V and the current latch to 70mA.
- k. Adjust A6R20 until the voltmeter indicates approximately 0.7V.
- l. Program the voltage to +01.00V and the current latch to 20mA.
- m. Adjust A6R108 until voltmeter indicates approximately 0.7V.

SECTION VI REPLACEABLE PARTS

6-1 INTRODUCTION

6-2 This section contains information for ordering replacement parts. Table 6-4 lists parts in alpha-numeric order by reference designators and provides the following information:

- a. Reference Designators. Refer to Table 6-1.
- b. Description. Refer to Table 6-2 for abbreviations.
- c. Total Quantity (TQ). Given only the first time the part number is listed except in instruments containing many sub-modular assemblies. In which case the TQ appears the first time the part number is listed in each assembly.
- d. Manufacturer's Part Number or Type.
- e. Manufacturer's Federal Supply Code Number. Refer to Table 6-3 for manufacturer's name and address.

- f. Hewlett-Packard Part Number.
- g. Recommended Spare Parts Quantity (RS) for complete maintenance of one instrument during one year of isolated service.
- h. Parts not identified by a reference designator are listed at the end of Table 6-4 under Mechanical and/or Miscellaneous. The former consists of parts belonging to and grouped by individual assemblies; the latter consists of all parts not immediately associated with an assembly.

6-3 ORDERING INFORMATION

6-4 To order a replacement part, address order or inquiry to your local Hewlett-Packard sales office (see lists at rear of this manual for addresses). Specify the following information for each part: Model; complete serial number, and any Option or special modification (J) numbers of the instrument; Hewlett-Packard part number; circuit reference designator; and description. To order a part not listed in Table 6-4, give a complete description of the part, its function, and its location.

Table 6-1. Reference Designators

A	= assembly	E	= miscellaneous electronic part
B	= blower (fan)	F	= fuse
C	= capacitor	J	= Jack, Jumper
CB	= circuit breaker	K	= relay
CR	= diode	L	= inductor
DS	= device, signaling (lamp)	M	= meter

Table 6-1. Reference Designators (Continued)

P	= plug	V	= vacuum tube, neon bulb, photocell, etc.
Q	= transistor	VR	= zener diode
R	= resistor	X	= socket
S	= switch	Z	= integrated circuit or network
T	= transformer		
TB	= terminal block		
TS	= thermal switch		

Table 6-2. Description Abbreviations

A	= ampere	mfr	= manufacturer
ac	= alternating current	mod.	= modular or modified
assy.	= assembly	mtg	= mounting
bd	= board	n	= nano = 10^{-9}
bkt	= bracket	NC	= normally closed
OC	= degree Centigrade	NO	= normally open
cd	= card	NP	= nickel-plated
coef	= coefficient	Ω	= ohm
comp	= composition	obd	= order by description
CRT	= cathode-ray tube	OD	= outside diameter
CT	= center-tapped	p	= pic = 10^{-12}
dc	= direct current	P.C.	= printed circuit
DPDT	= double pole, double throw	pot.	= potentiometer
DPST	= double pole, single throw	p-p	= peak-to-peak
elect	= electrolytic	ppm	= parts per million
encap	= encapsulated	pvr	= peak reverse voltage
F	= farad	root	= rectifier
OF	= degree Fahrenheit	rms	= root mean square
fxd	= fixed	Si	= silicon
Ge	= germanium	SPDT	= single pole, double throw
H	= Henry	SPST	= single pole, single throw
Hz	= Hertz	SS	= small signal
IC	= integrated circuit	T	= slow-blow
ID	= inside diameter	tan.	= tantalum
Incnd	= incandescent	Ti	= titanium
k	= kilo = 10^3	V	= volt
m	= milli = 10^{-3}	var	= variable
M	= mega = 10^6	ww	= wirewound
μ	= micro = 10^{-6}	W	= Watt
met.	= metal		

Table 6-3. Code List of Manufacturers

CODE NO.	MANUFACTURER	ADDRESS	CODE NO.	MANUFACTURER	ADDRESS
00629	EBY Sales Co., Inc.	Jamaica, N. Y.	07138	Westinghouse Electric Corp.	
00656	Aerovox Corp.	New Bedford, Mass.		Electronic Tube Div.	Elmira, N. Y.
00853	Sangamo Electric Co.		07263	Falchlid Camera and Instrument Corp.	Semiconductor Div.
	S. Carolina Div.	Pickens, S. C.			Mountain View, Calif.
01121	Allen Bradley Co.	Milwaukee, Wis.	07387	Bircher Corp., The	Log Angeles, Calif.
01255	Litton Industries, Inc.	Beverly Hills, Calif.	07397	Sylvania Electric Prod., Inc.	
				Sylvania Electronic Systems	
01281	TRW Semiconductors, Inc.	Lawndale, Calif.		Western Div.	Mountain View, Calif.
01295	Texas Instruments, Inc.		07716	IRC Div. of TRW Inc.	Burlington Plant
	Semiconductor-Components Div.				Burlington, Iowa
		Dallas, Texas	07910	Continental Device Corp.	
01686	RCL Electronics, Inc.	Manchester, N. H.			Hawthorne, Calif.
01930	Amerock Corp.	Rockford, Ill.	07933	Raytheon Co. Components Div.	
02107	Sparta Mfg. Co.	Dover, Ohio		Semiconductor Operation	
02114	Ferroxcube Corp.	Saugerties, N. Y.			Mountain View, Calif.
02606	Fenwal Laboratories	Morton Grove, Ill.	08484	Breeze Corporations, Inc.	Union, N. J.
02660	Amphenol Corp.	Broadview, Ill.	08530	Reliance Mica Corp.	Brooklyn, N. Y.
02735	Radio Corp. of America	Solid State	08717	Sloan Company, The	Sun Valley, Calif.
	and Receiving Tube Div.	Somerville, N. J.	08730	Vemaline Products Co., Inc.	Wyckoff, N. J.
03508	G. E. Semiconductor Products Dept.		08806	General Elect. Co. Minia-	
		Syracuse, N. Y.		ture Lamp Dept.	Cleveland, Ohio
03797	Eidema Corp.	Compton, Calif.	08863	Nylomatic Corp.	Norrisville, Pa.
03877	Transitron Electronic Corp.		08919	RCH Supply Co.	Vernon, Calif.
		Wakefield, Mass.	09021	Airco Speer Electronic Components	
03888	Pyrofilm Resistor Co., Inc.				Bradford, Pa.
		Cedar Knolls, N. J.	09182	*Hewlett-Packard Co. New Jersey Div.	
04009	Arrow, Hart and Hegeman Electric Co.				Rockaway, N. J.
		Hartford, Conn.	09213	General Elect. Co. Semiconductor	
04072	ADC Electronics, Inc.	Harbor City, Calif.		Prod. Dept.	Buffalo, N. Y.
04213	Caddell & Burns Mfg. Co., Inc.		09214	General Elect. Co. Semiconductor	
		Mineola, N. Y.		Prod. Dept.	Auburn, N. Y.
04404	*Hewlett-Packard Co. Palo Alto Div.		09353	C & K Components Inc.	Newton, Mass.
		Palo Alto, Calif.	09922	Burndy Corp.	Norwalk, Conn.
04713	Motorola Semiconductor Prod. Inc.		11115	Wagner Electric Corp.	
		Phoenix, Arizona		Tung-Sol Div.	Bloomfield, N. J.
05277	Westinghouse Electric Corp.		11236	CTS of Berne, Inc.	Berne, Ind.
	Semiconductor Dept.	Youngwood, Pa.	11237	Chicago Telephone of Cal., Inc.	
05347	Ultronix, Inc.	Grand Junction, Colo.			So. Pasadena, Calif.
05820	Wakefield Engr. Inc.	Wakefield, Mass.	11502	IRC Div. of TRW Inc.	Boone Plant
06001	General Elect. Co. Electronic				Boone, N. C.
	Capacitor & Battery Dept.	Irmo, S. C.	11711	General Instrument Corp.	
06004	Basic Div. Stewart-Wornor Corp.			Rectifier Div.	Newark, N. J.
		Bridgport, Conn.	12136	Philadelphia Handle Co., Inc.	
06486	IRC Div. of TRW Inc.				Camden, N. J.
	Semiconductor Plant	Lynn, Mass.	12615	U. S. Terminals, Inc.	Cincinnati, Ohio
06540	Amatom Electronic Hardware Co., Inc.		12617	Hamlin Inc.	Lake Mills, Wisconsin
		New Rochelle, N. Y.	12697	Clarostat Mfg. Co., Inc.	Dover, N. H.
06555	Beeda Electrical Instrument Co.		13103	Thermalloy Co.	Dallas, Texas
		Penacook, N. H.	14493	*Hewlett-Packard Co.	Loveland Div.
06666	General Devices Co., Inc.				Loveland, Colo.
		Indianapolis, Ind.	14655	Cornell-Dubilier Electronics Div.	
06751	Semcor Div. Components, Inc.			Federal Pacific Electric Co.	
		Phoenix, Arizona			Newark, N. J.
06776	Robinson Nugent, Inc.	New Albany, Ind.	14936	General Instrument Corp. Semicon-	
06812	Torrington Mfg. Co., West Div.			ductor Prod. Group	Hicksville, N. Y.
		Van Nuys, Calif.	15801	Fenwal Elect.	Framingham, Mass.
07137	Transistor Electronics Corp.		16299	Coming Glass Works, Electronic	
		Minneapolis, Minn.		Components Div.	Raleigh, N. C.

*Use Code 28480 assigned to Hewlett-Packard Co., Palo Alto, California

Table 6-3, Code List of Manufacturers (Continued)

CODE NO.	MANUFACTURER	ADDRESS	CODE NO.	MANUFACTURER	ADDRESS
16750	Delco Radio Div. of General Motors Corp.	Kokomo, Ind.	70563	Amperite Co. Inc.	Union City, N.Y.
17545	Atlantic Semiconductors, Inc.	Asbury Park, N.J.	70901	Boomer Engrg. Co.	Fort Washington, Pa.
17803	Fairchild Camera and Instrument Corp.	Mountain View, Calif.	70903	Belden Corp.	Chicago, Ill.
17870	Daven Div. Thomas A. Edison Industries	Orange, N.J.	71218	Bud Radio, Inc.	Willoughby, Ohio
18324	Signetics Corp.	Sunnyvale, Calif.	71279	Cambridge Thermionic Corp.	Cambridge, Mass.
19315	Bendix Corp. The Navigation and Control Div.	Teterboro, N.J.	71400	Rusmann Mfg. Div. of McGraw & Edison Co.	St. Louis, Mo.
19701	Electra/Midland Corp.	Mineral Wells, Texas	71450	CTS Corp.	Elkhart, Ind.
21520	Fansteel Metallurgical Corp.	No. Chicago, Ill.	71468	I. T. T. Cannon Electric Inc.	Los Angeles, Calif.
22229	Union Carbide Corp. Electronics Div.	Mountain View, Calif.	71590	Globe-Union Inc.	Milwaukee, Wis.
22753	UID Electronics Corp.	Hollywood, Fla.	71700	General Cable Corp. Cornish Wire Co. Div.	Williamstown, Mass.
23936	Pamotor, Inc.	Pampa, Texas	71707	Coto Coll Co. Inc.	Providence, R.I.
24446	General Electric Co.	Schenectady, N.Y.	71744	Chicago Miniature Lamp Works	Chicago, Ill.
24456	General Electric Co. Lamp Div. of Consumer Prod. Group	Nela Park, Cleveland, Ohio	71785	Cinch Mfg. Co. and Howard B. Jones Div.	Chicago, Ill.
24655	General Radio Co.	West Concord, Mass.	71984	Dow Corning Corp.	Midland, Mich.
24881	LTV ElectroSystems Inc Memcor/Components Operations	Huntington, Ind.	72136	Electro Motive Mfg. Co. Inc.	Willimantic, Conn.
26982	Dynacool Mfg. Co. Inc.	Saugerties, N.Y.	72619	Dialight Corp.	Brooklyn, N.Y.
27014	National Semiconductor Corp.	Santa Clara, Calif.	72699	General Instrument Corp.	Newark, N.J.
28480	Hewlett-Packard Co.	Palo Alto, Calif.	72755	Drake Mfg. Co.	Harwood Heights, Ill.
28520	Heyman Mfg. Co.	Kenilworth, N.J.	72952	Elastic Stop Nut Div. of Amerace Esna Corp.	Union, N.J.
28875	IMC Magnetics Corp.	Rochester, N.H.	72982	Erie Technological Products Inc.	Erie, Pa.
31514	SAE Advance Packaging, Inc.	Santa Ana, Calif.	73096	Hart Mfg. Co.	Hartford, Conn.
31827	Budwig Mfg. Co.	Ramona, Calif.	73138	Beckman Instruments Inc.	Fullerton, Calif.
3173	G. E. Co. Tube Dept.	Owensboro, Ky.	73168	Fenwal, Inc.	Ashland, Mass.
35434	Lectrohm, Inc.	Chicago, Ill.	73293	Hughes Aircraft Co. Electron Dynamics Div.	Torrance, Calif.
37942	P. R. Mallory & Co. Inc.	Indianapolis, Ind.	73445	Amperex Electronic Corp.	Hicksville, N.Y.
42190	Mutor Co.	Chicago, Ill.	73506	Bradley Semiconductor Corp.	New Haven, Conn.
43334	New Departure-Hyatt Bearings Div. General Motors Corp.	Sandusky, Ohio	73559	Carling Electric, Inc.	Hartford, Conn.
44655	Ohmite Manufacturing Co.	Stokely, Ill.	73734	Federal Screw Products, Inc.	Chicago, Ill.
46384	Penn Engr. and Mfg. Corp.	Doylestown, Pa.	74193	Heinemann Electric Co.	Trenton, N.J.
47904	Polaroid Corp.	Cambridge, Mass.	74545	Hubbell Harvey Inc.	Bridgeport, Conn.
48956	Raytheon Co.	Lexington, Mass.	74868	Amphenol Corp. Amphenol RF Div.	Danbury, Conn.
55026	Simpson Electric Co. Div. of American Gage and Machine Co.	Chicago, Ill.	74970	E. F. Johnson Co.	Waseca, Minn.
56289	Sprague Electric Co.	North Adams, Mass.	75042	IRC Div. of TRW, Inc.	Philadelphia, Pa.
58474	Superior Electric Co.	Bristol, Conn.	75183	*Howard B. Jones Div. of Cinch Mfg. Corp.	New York, N.Y.
58849	Syntrotron Div. of FMC Corp.	Homer City, Pa.	75376	Kurz and Kasch, Inc.	Dayton, Ohio
59730	Thomas and Betts Co.	Philadelphia, Pa.	75382	Kilka Electric Corp.	Mt. Vernon, N.Y.
61537	Union Carbide Corp.	New York, N.Y.	75915	Littlefuse, Inc.	Des Plaines, Ill.
63743	Ward Leonard Electric Co.	Mt. Vernon, N.Y.	76381	Minnesota Mining and Mfg. Co.	St. Paul, Minn.
			76385	Minor Rubber Co. Inc.	Bloomfield, N.J.
			76487	James Millen Mfg. Co. Inc.	Malden, Mass.
			76493	J. W. Miller Co.	Compton, Calif.

*Use Code 71785 assigned to Cinch Mfg. Co., Chicago, Ill.

Table 6-3. Code List of Manufacturers (Continued)

CODE NO.	MANUFACTURER	ADDRESS	CODE NO.	MANUFACTURER	ADDRESS
76530	Cinch	City of Industry, Calif.	83508	Grant Pulley and Hardware Co.	West Nyack, N. Y.
76854	Oak Mfg. Co. Div. of Oak	Crystal Lake, Ill.	83594	Burdoughs Corp. Electronic	Plainsfield, N. J.
77068	Electro/Netics Corp.	Crystal Lake, Ill.	83835	Components Div.	Morristown, N. J.
	Bendix Corp., Electrodynamics Div.	No. Hollywood, Calif.	83877	U. S. Radium Corp.	New York, N. Y.
77122	Palnut Co.	Mountainside, N. J.	84171	Yardeny Laboratories, Inc.	Great Neck, N. Y.
77147	Patton-MacGuyar Co.	Providence, R. I.	84411	Arco Electronics, Inc.	Ogallala, Neb.
77221	Phaostron Instrument and Electronic Co.	South Pasadena, Calif.	85684	TRW Capacitor Div.	Harrison, N. J.
77252	Philadelphia Steel and Wire Corp.	Philadelphia, Pa.	85688	RCA Corp. Electronic Components	Newark, N. J.
77342	American Machine and Foundry Co.	Princeton, Ind.	87034	Rummel Fibre Co.	Anaheim, Calif.
77630	Potter and Drumfield Div.	Camden, N. J.	87216	Marco & Oak Industries a Div. of Oak	Lansdale, Pa.
77764	TRW Electronic Components Div.	Harrisburg, Pa.	87585	Electro/netics Corp.	Philadelphia, Pa.
78189	Resistance Products Co.	Elgin, Ill.	87929	Philco Corp. Lansdale Div.	Bridgport, Conn.
78452	Illinois Tool Works Inc. Shakeproof Div.	Chicago, Ill.	88140	Stockwell Rubber Co. Inc.	Lincoln, Ill.
78488	Everlock Chicago, Inc.	St. Marys, Pa.	88245	Tower-Olschan Corp.	Van Nuys, Calif.
78526	Stackpole Carbon Co.	San Fernando	90634	Cutler-Hammer Inc. Polymer Distribution	Metuchen, N. J.
78553	Stanwyck Winding Div.	Newburgh, N. Y.	90763	and Control Div. Lincoln Plant	Chicago, Ill.
78584	Electric Mfg. Co. Inc.	Cleveland, Ohio	91345	Litton Precision Products Inc. USECO	El Monte, Calif.
79136	Tinnerman Products, Inc.	Yonkers, N. Y.	91418	Div. Litton Industries	Chicago, Ill.
79307	Stewart Stamping Corp.	L. I. C., N. Y.	91506	Gulton Industries Inc.	Attleboro, Mass.
79727	Waldes Kohincor, Inc.	New York, N. Y.	91637	United-Car Inc.	Columbus, Ohio
	Whitehead Metals Inc.	Philadelphia, Pa.	91662	Miller Dial and Nameplate Co.	Willow Grove, Pa.
	Continental-Wirt Electronics Corp.	Mt. Kisco, N. Y.	91929	Radio Materials Co.	Freeport, Ill.
79963	Zierick Mfg. Co.	Morristown, N. J.	92825	Honeywell Inc. Div. Micro Switch	Schiller Pk., Ill.
80031	Mepco Div. of Sessions Clock Co.	Riverside, Calif.	93332	Whitso, Inc.	Woburn, Mass.
80294	Bourns, Inc.	Racine, Wisc.	93410	Sylvania Electric Prod. Inc. Semi-	Manassas, Ohio
81042	Howard Industries Div. of Mal Ind. Inc.	La Grange, Ill.	94144	conductor Prod. Div.	Quincy, Mass.
81073	Grayhill, Inc.	El Segundo, Calif.	94154	Essex Wire Corp. Stemco	Livingston, N. J.
81483	International Rectifier Corp.	Yonkers, N. Y.	94222	Controls Div.	Lester, Pa.
81751	Columbus Electronics Corp.	New York, N. Y.	95263	Raytheon Co. Components Div.	L. I. C., N. Y.
82099	Goodyear Sundries & Mechanical Co. Inc.	Du Bois, Pa.	95354	Ind. Components Oper.	Rolling Meadows, Ill.
82142	Airco Spear Electronic Components	Emporium, Pa.	95712	Wagner Electric Corp.	Franklin, Ind.
82219	Sylvania Electric Products Inc.	Chicago, Ill.	95987	Tung-Sol Div.	Chicago, Ill.
	Electronic Tube Div. Receiving	Attleboro, Mass.	96791	Southco Inc.	Janesville, Wis.
82389	Tube Operations	Madison, Wis.	97464	Leocraft Mfg. Co. Inc.	Irvington, N. J.
82647	Switchcraft, Inc.	Woodstock, N. Y.	98291	Method Mfg. Co.	Westbury, N. Y.
	Metals and Controls Inc. Control	Glendale, Calif.	98410	Bendix Corp. Microwave	Mamaroneck, N. Y.
	Products Group	Cambridge, Mass.	98978	Devices Div.	Cleveland, Ohio
82866	Research Products Corp.	Springfield, N. J.		Weckesser Co. Inc.	Burbank, Calif.
82877	Retron Inc.	Eatontown, N. J.		Amphenol Corp. Amphenol	Boston, Mass.
82893	Vector Electronic Co.	Brooklyn, N. Y.		Controls Div.	
83058	Carr Fastener Co.	Chicago, Ill.		Industrial Retaining Ring Co.	
83186	Victory Engineering Corp.	Brookfield, Mass.			
83298	Bendix Corp. Electric Power Div.				
83330	Herman H. Smith, Inc.				
83385	Central Screw Co.				
83501	Gavitt Wire and Cable Div. of				
	Amerace Esna Corp.				

Table G-4. Replaceable Parts

REF. DESIGN.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A1	Input Board		Refer to proper Option Appendix			
A1A1	Isolator circuit					
CR1,2	Diode, Si 200mA 75V	2		28480	1901-0050	2
Q1,2	SS NPN SI	2		28480	1854-0071	2
R1,2,3			Refer to proper Option Appendix			
R4	fxd, comp 750 Ω \pm 5%, 1/2W	1	EB-7515	01121	0686-7515	1
R5	fxd, comp 82 Ω \pm 5%, 1/4W	1	CB-8205	01121	0683-8205	1
R6	fxd, comp 750 Ω \pm 5%, 1/4W	1	CB-7515	01121	0683-7515	1
Z1	Photo-Isolator	1		28480	1990-0407	1
A1A2 through A1A7	Same as A1A1	16				
A1C1-3	fxd, ceramic .47 μ F 25Vdc	3		28480	0160-0174	1
C4	fxd, ceramic .1 μ F 50Vdc	2		28480	0150-0121	1
C5	fxd, mica 390pF 300Vdc	1	RDM15F39153C	72136	0140-0200	1
C6	fxd, mylar .01 μ F 200Vdc	1	292P10352-PTS	56289	0160-0207	1
C7	fxd, ceramic .1 μ F 50Vdc			28480	0150-0121	
CR1-4	Diode, Si 200mA 75V	4		28480	1901-0050	4
Q1			Refer to Instrument Modification Sheet			
Q2-Q5	SS NPN SI	4		28480	1854-0071	4
Q6			Refer to proper Option Appendix			
Q7			Refer to Instrument Modification Sheet			
R1,2,3			Refer to proper Option Appendix			
R4			Refer to Instrument Modification Sheet			
R5	fxd, comp 1K Ω \pm 5%, 1/4W	3	CB-1025	01121	0683-1025	1
R6	fxd, ww 100 Ω \pm 5%, 3W	2	242E	56289	0813-0050	1
R7	fxd, met film 11K Ω \pm 2%, 1/8W	1	MF4C TD	30983	0757-0949	1
R8	fxd, met film 7.5K Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0757-0440	1
R9	fxd, comp 1K Ω \pm 5%, 1/4W		CB-1025	01121	0683-1025	
R10	fxd, ww 100 Ω \pm 5%, 3W		242E	56289	0813-0050	
R11	fxd, comp 3K Ω \pm 5%, 1/4W	1	CB-3025	01121	0683-3025	1
R12	fxd, comp 910 Ω \pm 5%, 1/2W	1	EB-9115	01121	0686-9115	1
R13	fxd, comp 750 Ω \pm 5%, 1/2W	1	EB-7515	01121	0686-7515	1
R14	fxd, comp 750 Ω \pm 5%, 1/4W	2	CB-7515	01121	0683-7515	1
R15			Refer to proper Option Appendix			
R16	fxd, comp 82 Ω \pm 5%, 1/4W	2	CB-8205	01121	0683-8205	
R17,18,19			Refer to proper Option Appendix			
R20	fxd, comp 1K Ω \pm 5%, 1/4W		CB-1025	01121	0683-1025	
R21	fxd, comp 750 Ω \pm 5%, 1/4W		CB-7515	01121	0683-7515	
R22	fxd, comp 82 Ω \pm 5%, 1/4W		CB-8205	01121	0683-8205	
R23	fxd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
VR1	Diode, zener 4.22V 400mW	2		28480	1902-3070	2
VR2,3	Diode, zener 4.99V	2	SZ11213-54	04713	1902-0533	2
VR4	Diode, zener 4.22V 400mW			28480	1902-3070	
VR5			Refer to proper Option Appendix			
Z1,2	Photo-Isolator	2		28480	1990-0407	2
Z3,4	Monostable Multivibrator, IC	2	SN13617	01295	1820-0261	2
A2	Logic Plug-In Board		Refer to proper Option Appendix			
C1	fxd, ceramic .47 μ F 25Vdc	6		28480	0160-0174	2
C2	fxd, Mica 150pF 300Vdc	1	RDM15F151J3C	72136	0140-0196	1
C4-8	fxd, ceramic .47 μ F 25Vdc			28480	0160-0174	
C9	fxd, tant. 4.7 μ F 6Vdc	1	150D475X5006A2-DYS	56289	0180-1954	1

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	HIP PART NO.	RS
AZDS1	Lamp, 6Vdc incandescent	1	2305WA	11115	2140-0324	1
Q1-3	SS NPN SI	3		28480	1854-0071	3
R1	fxd, comp 1K Ω \pm 5%, 1/4W	4	CB-1025	01121	0683-1025	1
R2	fxd, comp 4.7K Ω \pm 5%, 1/4W	1	CB-4725	01121	0683-4725	1
R3	fxd, comp 1K Ω \pm 5%, 1/4W	1	CB-1025	01121	0683-1025	1
R4	fxd, comp 200 Ω \pm 5%, 1/4W	1	CB-2015	01121	0683-2015	1
R5	fxd, film 30.1K Ω \pm 1%, 1/8W	1		28480	0757-0453	1
R6	fxd, comp 5.1K Ω \pm 5%, 1/4W	1	CB-5125	01121	0683-5125	1
R7	fxd, comp 510 Ω \pm 5%, 1/4W	1	CB-5115	01121	0683-5115	1
R8	fxd, comp 2K Ω \pm 5%, 1/4W	1	CB-2025	01121	0683-2025	1
R9, 10	fxd, comp 1K Ω \pm 5%, 1/4W	1	CB-1025	01121	0683-1025	1
S1	Switch, slide DPDT	1		28480	3101-0932	1
Z1-4			Refer to proper Option Appendix			
Z5	4-2 Input NAND Gate; IC	1		28480	1820-0054	1
Z6	Monostable Multivibrator; IC	1	SN13617	01295	1820-0261	1
Z7, 8	Hybrid Resistive Network; IC	2		28480	1810-0041	2
Z9-12			Refer to proper Option Appendix			
A3	D to A Converter Plug-In Board	1		28480	5060-6192	
A3A1	NOT USED	-				
A3A2C1	fxd, ceramic .001 μ F 500Vdc	1		28480	0160-3398	1
C2	fxd, ceramic .005 μ F 100V	1		28480	0160-2639	1
CR1-3	Diode, SI 200mA 75V	3		28480	1901-0050	3
Q1	SS NPN SI	1		28480	1854-0087	1
Q2	SS PNP SI	1		28480	1853-0078	1
Q3	SS NPN SI	1		28480	1854-0317	1
R1	fxd, comp 3.3K Ω \pm 5%, 1/2W	1	EB-3325	01121	0686-3325	1
R2	fxd, comp 12K Ω \pm 5%, 1/2W	1	EB-1235	01121	0686-1235	1
R3	fxd, comp 2.2K Ω \pm 5%, 1/2W	1	EB-2225	01121	0686-2225	1
R4, 5	fxd, comp 10K Ω \pm 5%, 1/2W	2	EB-1035	01121	0686-1035	1
A3A3 through A3A15	Same as A3A2	13				
A3A16C1	fxd, ceramic .001 μ F 500Vdc	1		28480	0160-3398	1
C2	fxd, ceramic .005 μ F 100V	1		28480	0160-2639	1
CR1-3	Diode, SI 200mA 75V	3		28480	1901-0050	3
Q1	SS NPN SI	1		28480	1854-0087	1
Q2	SS PNP SI	1		28480	1853-0078	1
Q3	SS NPN SI	1		28480	1854-0317	1
A3A16R1	fxd, comp 3.3K Ω \pm 5%, 1/2W	1	EB-3325	01121	0686-3325	1
R2	fxd, comp 10K Ω \pm 5%, 1/2W	3	EB-1035	01121	0686-1035	1
R3	fxd, comp 2.2K Ω \pm 5%, 1/2W	1	EB-2225	01121	0686-2225	1
R4, 5	fxd, comp 10K Ω \pm 5%, 1/2W	2	EB-1035	01121	0686-1035	1
R6	fxd, comp 33K Ω \pm 5%, 1/2W	1	EB-3335	01121	0686-3335	1
AJAR-Z1	Ref. Amp. 6.8V \pm 5% TC \pm .0005%	1		28480	5080-7139	1
AR-R1	fxd, ww - Part of 5080-7139	1				
AR-R2	fxd, film - Part of 5080-7139	1				
AR-R3	fxd, film - Part of 5080-7139	1				
AR-R4	fxd, film - Part of 5080-7139	1				

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A3C5	fxd, mica 330pF 500Vdc	1	RCM15331J	00853	0140-0168	1
C11	fxd, ceramic .001 μ F 500Vdc	1		28480	0160-3398	1
C12	fxd, mylar .01 μ F 200V	1	192P10392	56289	0160-0161	1
C13, 30	fxd, elect, 22 μ F 35V	2	150D226X0035R2	56289	0180-0160	1
C40, 41	fxd, elect, 1 μ F 35Vdc	2	150D105X9035A2	56289	0180-0291	1
CR10-14	Diode, SI 200mA 75V	5		28480	1901-0050	5
L1	Ferrite Bead	1		28480	9170-0847	1
Q10	SS PNP SI	3		28480	1853-0099	3
Q11	Dual NPN SI	1		28480	1854-0221	1
Q12	SS NPN SI	2		28480	1854-0071	2
Q13	SS NPN SI	1		28480	1854-0087	1
Q14	SS NPN SI	1		28480	5080-7132	1
Q15, 30	SS PNP SI	2		28480	1853-0099	2
Q31	SS NPN SI	2		28480	1854-0244	2
Q32	SS NPN SI	1		28480	1854-0071	1
Q40	SS NPN SI	1		28480	1854-0244	1
R10	fxd, comp 43K Ω \pm 5%, 1/2W	1	EB-4335	01121	0686-4335	1
R11	fxd, comp 3K Ω \pm 5%, 1/2W	1	EB-3025	01121	0686-3025	1
R12	fxd, met. film 1K Ω \pm 1%, 1/4W	1	Type CCA T-0	07716	0757-0338	1
R13	fxd, comp 2.4K Ω \pm 5%, 1/2W	1	EB-2425	01121	0686-2425	1
R14	fxd, met. film 200K Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0757-0472	1
R15	fxd, met. film 160K Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0698-5092	1
R16	fxd, ww 297 Ω \pm 1%, 1/4W 20ppm	1	Type R303B	01686	0811-1929	1
R17	fxd, ww 243 Ω \pm 1%, 1/4W 20ppm	1	Type R303B	01686	0811-2075	1
R18	var. ww 500 Ω (Type 100)	1	Model 100	11502	2100-0898	1
R19	fxd, ww 10K Ω \pm 0.1%, TC \pm 2ppm	1	Type 7007	01686	0811-2577	1
R20A	fxd, ww 16K Ω \pm 0.1% (Matched to R20B)	1	Type 7007	01686	0811-2757	1
R20B	fxd, ww 15.82K Ω \pm 0.1%	1	Type 7007	01686	0811-2757	1
R21	fxd, comp 1.8K Ω \pm 5%, 1/2W	1	EB-1825	01121	0686-1825	1
R22	fxd, met. film 7.5K Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0757-0440	1
R23	fxd, met. film 12K Ω \pm 1%, 1/8W	2	Type CEA T-0	07716	0698-5088	1
R24	fxd, comp 2.2K Ω \pm 5%, 1/2W	2	EB-2225	01121	0686-2225	1
R25	fxd, met. film 12K Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0689-5088	1
R26	fxd, comp 2K Ω \pm 5%, 1/2W	1	EB-2025	01121	0686-2025	1
R27	fxd, met. film 600 Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0757-1100	1
R30	fxd, met. film 2K Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0757-0283	1
R31	fxd, comp 51 Ω \pm 5%, 1/2W	1	EB-5105	01121	0686-5105	1
R34A	fxd, ww 2350 Ω \pm 0.1% (Match to R34B)	1	Type 7007	01686	0811-1167	1
R34B	fxd, ww 1940 Ω \pm 0.1%	1	Type 7007	01686	0811-1167	1
R36	var. ww 100 Ω \pm 5%	9	Model 100	11502	2100-1450	2
R40	fxd, comp 1.2K Ω \pm 5%, 1/2W	1	EB-1225	01121	0686-1225	1
R50	fxd, met. film 196 Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0698-3440	1
R51	fxd, comp 18 Ω \pm 5%, 1/2W	1	EB-1805	01121	0686-1805	1
R52-59	var. ww 100 Ω \pm 5%	1	Model 100	11502	2100-1450	1
R60	fxd, ww 19.96K Ω \pm 1%, TC \pm 2ppm	1	Type 7007	01686	0811-2574	1
R61-67	fxd, ww 19.96K Ω \pm 1%, TC \pm 5ppm	7	Type 7007	01686	0811-2575	2
R68-76	fxd, ww 10K Ω \pm 1%, TC \pm 5ppm	9	Type E30	01686	0811-1994	2
R77, 78	fxd, met. film 10K Ω \pm 1%, 1/8W	2	Type CEA T-0	07716	0757-0442	1
R79	JUMPER	-				-
R80-86	fxd, ww 20K Ω \pm 1% TC \pm 5ppm	7	Type 7007	01686	0811-2609	2
R87-89, 91	fxd, met. film 20K Ω \pm 1%, 1/8W	4	Type CEA T-0	07716	0757-0449	1
R92	fxd, ww 150K Ω \pm 1% TC \pm 5ppm	1	Type 7007	01686	0811-2763	1

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	TO	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A3R93	fxd, ww 100K Ω \pm 1%, TC \pm 5ppm	1	Type 7010	016HG	0811-1997	1
R94	fxd, ww 408.2 Ω \pm 1%, TC \pm 5ppm	1	Type 7007	016HG	0811-2762	1
R95	fxd, met, film 562K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0482	1
R96	fxd, met, film 139 Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-4099	1
R97	fxd, met, film 11K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0443	1
R98	fxd, met, film 1M Ω \pm 1%, 1/4W	1	Type CEB T-O	07716	0757-0344	1
R99	fxd, met, film 390K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-5093	1
R100	var, ww 15K Ω \pm 5%	1	Model 100	11502	2100-0896	1
R102	NOT ASSIGNED	-	-	-	-	-
R103	fxd, comp 5.6K Ω \pm 5%, 1/2W	1	EB-5625	01121	0686-5625	1
VR30	Diode, zener 4.22V 400mW	1		28480	1902-3070	1
VR31	Diode, zener 12.4V 400mW	1		28480	1902-3105	1
VR40	Diode, zener 5.62V 400mW	1		28480	1902-3104	1
A4	Power Supply Board	1		28480	06130-60025	
C4,5	fxd, elect, 1.450 μ F 45Vdc	2		28480	0180-1893	1
C8,9	fxd, elect, 400 μ F 100Vdc	2		28480	0180-1807	1
C10	fxd, elect, 100 μ F 25Vdc	2	30D107G025DD2	56289	0180-0094	1
G11-22	fxd, ceramic .05 μ F 400V	12	33C 17A CDII	56289	0150-0052	2
C23	fxd, elect, 100 μ F 25Vdc		30D107G025DD2	56289	0180-0094	1
CR1-4	Rect. Si 1A 400prv	18		28480	1901-0328	8
CR5,6,7	Rect. Si 250mW 200prv	4		28480	1901-0033	4
CR8-21	Rect. Si 1A 400prv			28480	1901-0328	
CR22	Rect. Si 250mW 200prv			28480	1901-0033	
K1	Relay, 6Vdc	1	643-6V	09023	0490-0513	1
Q1	SS PNP Si	1		28480	1853-0099	1
R1-R3	fxd, comp 560 Ω \pm 5%, 1/2W	3	EB-5615	01121	0686-5615	1
R4,5	fxd, comp 3.6K Ω \pm 5%, 1/2W	3	EB-3625	01121	0686-3625	1
R6,7	fxd, met, oxide 5.1K Ω \pm 5%, 2W	2	Type C42S	16299	0698-3644	1
R8,9	fxd, comp 20K Ω \pm 5%, 1W	2	GB-2035	01121	0689-2035	1
R10	fxd, comp 3K Ω \pm 5%, 1/2W	1	EB-3025	01121	0686-3025	1
R11	fxd, comp 3.6K Ω \pm 5%, 1/2W		EB-3625	01121	0686-3625	
R12	fxd, comp 9.1K Ω \pm 5%, 1/2W	1	EB-9125	01121	0686-9125	1
R13	fxd, comp 33K Ω \pm 5%, 1/2W	1	EB-3335	01121	0686-3335	1
R14	var, ww 5K Ω \pm 5%	1	Type CT-100-4	06486	2100-0741	1
R15	fxd, film 9.09K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0288	1
R16	fxd, film 5.2K Ω \pm 1%, 1/4W	1	Type CEB T-O	07716	0698-5148	1
R17	fxd, film 10.0K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0442	1
R18	fxd, film 68.1K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0461	1
R19	fxd, film 2K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0283	1
R20	fxd, film 392 Ω \pm 1%, 1/2W	1	Type CEC T-O	07716	0757-0811	1
R21	fxd, film 121 Ω \pm 1%, 1/4W	1	Type CEB T-O	07716	0757-0316	1
R22	fxd, film 42.2 Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0757-0069	1
R23	Thermistor 64 Ω \pm 10%	1	LB16J1	02606	0837-0023	1
R24	var, ww 10 Ω \pm 5%	1	Type CT-100-4	06486	2100-1767	1
R25	fxd, film 42.2 Ω \pm 1%, 1/8W		Type CEA T-O	07716	0757-0316	
R26	fxd, comp 200 Ω \pm 5%, 1/2W	1	EB-2015	01121	0686-2015	1
R27	fxd, comp 2K Ω \pm 5%, 1/2W	1	EB-2025	01121	0686-2025	1
T2	Bias Transformer	1		28480	5080-1773	1
A5	Interconnect Board	1		28480	06130-60026	
C1	fxd, mylar, .033 μ F 200Vdc	1	192P33392	56289	0160-0163	1
C2	fxd, tant, 4.7 μ F 35Vdc	1	150D475X9035B2-DYS	56289	0180-Q108	1
C3	fxd, ceramic 0.1 μ F 50Vdc	1	5C50B1-CML	56289	0150-0121	1

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A5CR1-B	Rect. SI 1A 200prv	8		28480	1901-0327	6
J1-6	P. C. Board Edge Connectors	6	262-22-30-340	16630	1251-1887	2
L1	Inductor 1mH	1		28480	9100-2198	1
R3-5	fxd, ww 1.25 Ω \pm 1%, 4W	3	NS-2-18	91637	0811-2556	1
R8	fxd, comp 10 Ω \pm 5%, 1/2W	1	EB-1000	01121	0686-1000	1
R9	JUMPER					
R10	fxd, film 4K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0688-5808	1
R11	fxd, film 1K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0280	1
R12	fxd, ww 10K Ω \pm 0.1%, 1/4W	1	Type E30	01686	0811-1994	1
A6	Control Board		Refer to proper Option Appendix			
A6A1	Input Isolator Circuit					
CR1,2	Diode, SI 200mA 75V	2		28480	1901-0050	2
Q1,2	SS NPN SI	2		28480	1854-0071	2
R1,2,3			Refer to proper Option Appendix			
R4	fxd, comp 750 Ω \pm 5%, 1/2W	1	EB-7515	01121	0686-7515	1
R5	fxd, comp 82 Ω \pm 5%, 1/4W	1	CB-8205	01121	0683-8205	1
R6	fxd, comp 750 Ω \pm 5%, 1/4W	1	CB-7515	01121	0683-7515	1
Z1	Photo-Isolator	1		28480	1990-0407	1
A6A2 through A6A4	Same as A6A1					
A6A5	Latch Status Isolator and Output Amplifier					
CR1,2	Diode, SI 200mA 75V	2		28480	1901-0050	2
Q1-4	SS NPN SI	4		28480	1854-0071	4
R1	fxd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
R2	fxd, comp 1.3K Ω \pm 5%, 1/2W	1	EB-1325	01121	0686-1325	1
R3	fxd, comp 750 Ω \pm 5%, 1/2W	1	EB-7515	01121	0683-7515	1
R4	fxd, comp 82 Ω \pm 5%, 1/4W	1	CB-8205	01121	0683-8205	1
R5	fxd, comp 12K Ω \pm 5%, 1/4W	1	CB-1235	01121	0683-1235	1
R6	fxd, comp 100 Ω \pm 5%, 1/4W	1	CB-1015	01121	0683-1015	1
R7	fxd, comp 5.6K Ω \pm 5%, 1/2W	1	EB-5625	01121	0686-5625	1
R8			Refer to proper Option Appendix			
VR1			Refer to proper Option Appendix			
Z1	Photo-Isolator	1		28480	1900-0407	1
A6A6	Overload Status Isolator and Output Amplifier					
CR1,2	Diode, SI 200ma 75V	2		28480	1901-0050	2
Q1-3	SS NPN SI	3		28480	1854-0071	3
Q4			Refer to Instrument Modification Sheet			
R1	fxd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
R2	fxd, comp 1.3K Ω \pm 5%, 1/2W	1	EB-1325	01121	0686-1325	1
R3	fxd, comp 750 Ω \pm 5%, 1/2W	1	EB-7515	01121	0683-7515	1
R4	fxd, comp 82 Ω \pm 5%, 1/4W	1	CB-8205	01121	0683-8205	1
R5	fxd, comp 12K Ω \pm 5%, 1/4W	1	CB-1235	01121	0683-1235	1
R6	fxd, comp 100 Ω \pm 5%, 1/4W	1	CB-1015	01121	0683-1015	1
R7			Refer to Instrument Modification Sheet			
R8			Refer to proper Option Appendix			
VR1			Refer to proper Option Appendix			
Z1		1		28480	1900-0407	1
A6C1	fxd, mica 240pF 300Vdc	4	RDM15F241J3C	00853	0140-0199	1

Table 6-1. Replaceable Parts

REF. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	IMP. PART NO.	PKS.
AGC2	fxd, ceramic .47 μ F 25Vdc	2	5C11B7	56289	0160-0174	1
C3	fxd, mica 30pF 300Vdc	1	RDM15C300J3C	00853	0160-2109	1
C4	fxd, mylar .001 μ F 200Vdc	3	192P10292	56289	0160-0153	1
C5, 6, 7	fxd, mica 240pF 300Vdc		RDM15P241J3C	00853	0140-0199	
C8	fxd, mylar 2200pF 200Vdc	1	192P22202	56289	0160-0154	1
C9, 10	fxd, mylar .001 μ F 200Vdc		192P10292	56289	0160-0153	
C11	fxd, mylar .033 μ F 200Vdc	1	192P33392	56289	0160-0163	1
C12	fxd, mica 150pF 300Vdc	1	RDM15P151J3C	00853	0140-0196	1
C13, 14	fxd, mica 390pF 300Vdc	2	RDM15P391J3C	00853	0140-0200	1
C15	fxd, ceramic .1 μ F 50Vdc	1	5C50B1-CML	56289	0150-0121	1
C16	fxd, tant. 4.7 μ F 35Vdc	1	150D475X9035B2-DYS	56289	0180-0100	1
C17	fxd, ceramic .47 μ F 25Vdc		5C11B7	56289	0160-0174	
CR1, 2	Diode, Si 200mA 75V	17		28480	1901-0050	H
CR5-13	Diode, Si 200mA 75V			28480	1901-0050	
CR14, 15			Refer to proper Option Appendix			
CR16-18	Diode, Si 200mA 75V			28480	1901-0050	
CR19	Stabistor, Si 10prv 400mW	1		28480	1901-0460	1
CR20	Diode, Si 200mA 75V			28480	1901-0050	
AGQ1, 2, 3	SS NPN SI	17		28480	1854-0071	H
Q4	SS NPN SI	6	2N3417	03500	1854-0087	5
Q5, 6	SS NPN SI			28480	1854-0071	
Q8-13	SS PNP SI	9		28480	1853-0099	5
Q14, 15	SS NPN SI			28480	1854-0071	
Q16-18	SS NPN SI		2N3417	03500	1854-0087	
Q19, 20	SS PNP SI			28480	1853-0099	
Q21, 22	SS NPN SI		2N3417	03500	1854-0087	
Q23	SS PNP SI			28480	1853-0099	
Q24-33	SS NPN SI			28480	1854-0071	
Q34	Power NPN SI	1	2N1711	17803	1854-0003	1
R1-3	fxd, comp 3.9K Ω \pm 5%, 1/4W	3	CB-3925	01121	0683-3925	1
R4-6	fxd, comp 39K Ω \pm 5%, 1/4W	3	CB-3935	01121	0683-3935	1
R7	fxd, ww 220 Ω \pm 5%, 2W	1	Type DWII	07716	0811-1763	1
R8-10	fxd, comp 5.1K Ω \pm 5%, 1/4W	9	CB-5125	01121	0683-5125	1
R11-13	fxd, comp 9.1K Ω \pm 5%, 1/4W	3	CB-9125	01121	0683-9125	1
R14, 15	fxd, comp 20K Ω \pm 5%, 1/4W	12	CB-2035	01121	0683-2035	2
R16-18	fxd, film 19.6K Ω \pm 1%, 1/8W	3	Type CEA T-O	07716	0698-3157	1
R19	var, cermet 1K Ω \pm 10%	1	62-224-1	73138	2100-2633	1
R20-21	var, cermet 200 Ω \pm 10%	2	62-222-1	73138	2100-2413	1
R22-24	fxd, film 3.57K Ω \pm 1%, 1/8W	3	Type CEA T-O	07716	0698-3496	1
R25, 26	fxd, comp 200 Ω \pm 5%, 1/4W	2	CB-2015	01121	0683-2015	1
R27	fxd, film 6K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-3476	1
R28	fxd, film 2.37K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-3150	1
R29	fxd, film 4K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-5808	1
R30	fxd, film 121 Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0757-0069	1
R31, 32	fxd, film 432K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0757-0480	1
R33, 34	fxd, film 1K Ω \pm 1%, 1/8W	4	Type CEA T-O	07716	0757-0280	1
R35, 36	fxd, film 10K Ω \pm 1%, 1/8W	3	Type CEA T-O	07716	0757-0442	1
R37	fxd, film 121 Ω \pm 1%, 1/8W		Type CEA T-O	07716	0757-0069	
R38	fxd, film 750 Ω \pm 5% 1/4W	2	CB-7515	01121	0683-7515	1
R39	fxd, film 1K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0757-0280	
R40	fxd, comp 2.4K Ω \pm 5%, 1/4W	1	CB-2425	01121	0683-2425	1
R41	fxd, comp 5.1K Ω \pm 5%, 1/4W		CB-5125	01121	0683-5125	
R42	fxd, film 8.2K Ω \pm 2%, 1/8W	2	Type CEA T-O	07716	0757-0946	1

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
R43	fxd, film 1K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0757-0280	
R44	fxd, film 102 Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0406	1
R45	fxd, film 0.2K Ω \pm 2%, 1/8W		Type CEA T-O	07716	0757-0946	
R46	fxd, film 11K Ω \pm 1% 1/8W	1	Type CEA T-O	07716	0757-0443	1
R47	fxd, film 1.3K Ω \pm 1%, 1/4W	1	Type CEB T-O	07716	0757-0735	1
R48	fxd, film 1.21K Ω \pm 1%, 1/4W	1	Type CEB T-O	07716	0757-0734	1
R49	fxd, comp 51K Ω \pm 5%, 1/4W		CB-5125	01121	0683-5125	
R50-52	fxd, comp 10K Ω \pm 5%, 1/4W	9	CB-1035	01121	0683-1035	1
R53, 54	fxd, comp 20K Ω \pm 5%, 1/4W		CB-2035	01121	0683-2035	
R55, 56	fxd, comp 10K Ω \pm 5%, 1/4W		CB-1035	01121	0683-1035	
R57, 58	fxd, comp 2K Ω \pm 5%, 1/4W	3	CB-2025	01121	0683-2025	1
R59	fxd, comp 51K Ω \pm 5%, 1/4W		CB-5125	01121	0683-5125	
R60	fxd, comp 10K Ω \pm 5%, 1/4W		CB-1035	01121	0683-1035	
R61-63	fxd, comp 20K Ω \pm 5%, 1/4W		CB-2035	01121	0683-2035	
R64, 66	fxd, comp 51K Ω \pm 5%, 1/4W		CB-5125	01121	0683-5125	
R66	fxd, comp 100 Ω \pm 5%, 1/4W	1	CB-1015	01121	0683-1015	1
R67	fxd, comp 1K Ω \pm 5%, 1/4W	2	CB-1025	01121	0683-1025	1
R73	fxd, comp 4.7K Ω \pm 5%, 1/4W	2	CB-4725	01121	0683-4725	1
R74	fxd, comp 20K Ω \pm 5%, 1/4W		CB-2035	01121	0683-2035	
R75	fxd, comp 6.2K Ω \pm 5%, 1/4W	3	CB-6225	01121	0683-6225	1
R76	fxd, comp 100K Ω \pm 5%, 1/4W	2	CB-1045	01121	0683-1045	1
R77	fxd, comp 5.6K Ω \pm 5%, 1/4W	1	CB-5625	01121	0683-5625	
R78	fxd, comp 4.7K Ω \pm 5%, 1/4W		CB-4725	01121	0683-4725	
R79	fxd, comp 2K Ω \pm 5%, 1/4W		CB-2025	01121	0683-2025	
R80	fxd, comp 20K Ω \pm 5%, 1/4W		CB-2035	01121	0683-2035	
R81	fxd, comp 2.7K Ω \pm 5%, 1/4W	1	CB-2725	01121	0683-2725	1
R82	fxd, comp 1K Ω \pm 5%, 1/4W		CB-1025	01121	0683-1025	
R83	fxd, comp 200K Ω \pm 5%, 1/4W	1	CB-2045	01121	0683-2045	1
R84	fxd, comp 5.1K Ω \pm 5%, 1/4W		CB-5125	01121	0683-5125	
R85	fxd, comp 33K Ω \pm 5%, 1/4W	1	CB-3335	01121	0683-3335	1
R86	fxd, comp 82K Ω \pm 5%, 1/4W	1	CB-8235	01121	0683-8235	1
R87	fxd, comp 3.6K Ω \pm 5%, 1/4W	1	CB-3625	01121	0683-3625	1
R88	fxd, comp 9.1K Ω \pm 5%, 1/4W	1	CB-9125	01121	0683-9125	1
R89, 90	fxd, comp 6.2K Ω \pm 5%, 1/4W		CB-6225	01121	0683-6225	
R91	fxd, comp 100K Ω \pm 5%, 1/4W		CB-1045	01121	0683-1045	
R92	fxd, comp 12K Ω \pm 5%, 1/4W	1	CB-1235	01121	0683-1235	1
R93, 94, 95	fxd, comp 20K Ω \pm 5%, 1/4W		CB-2035	01121	0683-2035	
R96	fxd, comp 1.3K Ω \pm 5%, 1/2W		EB-1325	01121	0686-1325	
R97	fxd, comp 51K Ω \pm 5%, 1/4W	1	CB-5135	01121	0683-5135	1
R98	fxd, comp 750 Ω \pm 5%, 1/4W		CB-7515	01121	0683-7515	
R99	fxd, comp 82 Ω \pm 5%, 1/4W		CB-8205	01121	0683-8205	
R100, 101	fxd, comp 10K Ω \pm 5%, 1/4W		CB-1035	01121	0683-1035	
R102	fxd, ww 390 Ω \pm 5%, 3W	1	242E	56289	0811-1799	1
R103	fxd, comp 10K Ω \pm 5%, 1/4W		CB-1035	01121	0683-1035	
R105	fxd, comp 10Meg \pm 5%, 1/4W	1	CB-1065	01121	0683-1065	1
R106	fxd, film 10K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0757-0442	
R107	fxd, comp 5.6Meg \pm 5%, 1/4W	1	CB-5655	01121	0683-5655	1
R108	var, cermet 20K Ω \pm 10%	1	62-228-1	73138	2100-2514	1
R109	fxd, ww 75 Ω \pm 5%, 5W	1	243E	56289	0812-0097	1
VR1	Diode, zener 4.99V 400mW	1		28480	1902-3092	1
VR2	Diode, zener 12.4V 400mW	1		28480	1902-3185	1
VR4-6	Diode, zener 4.22V 400mW	3		28480	1902-3070	3
Z1	Hybrid Resistive Network IC	1		28480	1810-0041	1
Z2	Quad 4-Bit Dstaple Latch IC	1	SN7475	01295	1820-0876	1

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A6Z3	Operational Amplifier IC	1	SL8641	27014	1820-0223	1
Z4	Dual Operational Amp IC	1		28480	1820-0092	1
A7	Amplifier Plug-In Board	1		28480	06130-60024	
C1	fxd, mica 330pF 500Vdc	2	RCM15E33IJ	04062	0140-0168	1
C2,3	fxd, mylar .22 μ F 80Vdc	2	192P2249R8	56289	0160-2453	1
C4	fxd, elect. 1 μ F 35Vdc	1	150D105X9035A2	56289	0180-0291	1
C5,6	fxd, mylar .0022 μ F 200V	2	192P22292	56289	0160-0154	1
C7,8	fxd, mylar .1 μ F 200Vdc	2	192P10492	56289	0160-0168	1
C9	fxd, mica 330pF 500Vdc	1	RCM15E33JJ	04062	0140-0168	1
C10,11	fxd, mica 82pF 300Vdc	2	RDM15E820J3C	04062	0140-0193	1
C12	fxd, ceramic .001 μ F 500Vdc	5	40C88A1CDH	56289	0160-3398	1
C14	fxd, mylar .01 μ F 200Vdc	3	192P10392	56289	0160-0161	1
C15	fxd, ceramic .001 μ F 500Vdc		40C88A1CDH	56289	0160-3398	
C17	fxd, mylar .01 μ F 200Vdc		192P10392	56289	0160-0161	
C18	fxd, tant. .47 μ F 35Vdc	1	150D474X9035A2-DYS	56289	0180-0376	1
C19	fxd, ceramic .001 μ F 500Vdc		40C88A1CDH	56289	0160-3398	
C20	fxd, ceramic 100pF 1KVdc	1	DD-101	71590	0160-2061	1
C21,22	fxd, ceramic .001 μ F 500Vdc		40C88A1CDH	56289	0160-3398	
C23	fxd, mylar .01 μ F 200Vdc		192P10392	56289	0160-0161	
C24,25	fxd, ceramic .47 μ F 25Vdc	2	5C11B7	56289	0160-0174	1
C26	fxd, ceramic 0.001 μ F 1KVdc	1	C067B102E102ZS26	56289	0150-0050	1
CR1-15	Diode, Si 15V 400mW	24		28480	1901-0461	2
CR16,17	Stabistor, Si 10prv 400mW	5		28480	1901-0460	5
CR18-20	Diode, Si 15V 400mW			28480	1901-0461	
CR21	Stabistor, Si 10prv 400mW			28480	1901-0460	
CR22,23	Diode, Si 200V 250mW	2		28480	1901-0033	2
CR24-27	Diode, Si 15V 400mW			28480	1901-0461	
CR28,29	Diode, Si 200mA 75V	8		28480	1901-0050	5
CR30,31	Diode, Si 15V 400mW			28480	1901-0461	
CR32,33	Stabistor, Si 10prv 400mW			28480	1901-0460	
CR34	Diode, Si 15V 400mW			28480	1901-0461	
CR35-40	Diode, Si 200mA 75V			28480	1901-0050	
K1	Reed Relay and Coil Assembly Reed Relay (Part of A7K1) Coil (Part of A7K1)	1		28480	5080-7127	1
		1	DRS-2	12617	0490-0727	1
		1	SF-125	71707	0490-0728	1
K2	Reed Relay	1		28480	0490-0399	1
Q1	Diff. Amp, NPN	1		28480	1854-0221	1
Q2	Diff. Amp, NPN	1		28480	1854-0229	1
Q3,4	SS NPN Si	4	2N3417	03508	1854-0087	4
Q5	SS PNP Si	1		28480	1853-0010	1
Q6	SS PNP Si	5		28480	1853-0037	5
Q7	Power NPN Si	7		28480	1854-0095	5
Q8	SS NPN Si	5		28480	1854-0071	5
Q9	SS PNP Si	5		28480	1853-0099	5
Q10,11	Power NPN Si			28480	1854-0095	
Q12,13	SS PNP Si			28480	1853-0037	
Q14,15	Power NPN Si			28480	1854-0095	
Q16,17	SS PNP Si			28480	1853-0037	
Q18,19	SS NPN Si			28480	1854-0071	
Q20-22	SS PNP Si			28480	1853-0099	
Q23	SS NPN Si			28480	1854-0071	
Q24,25	SS NPN Si		2N3417	03508	1854-0087	
Q26	SS PNP Si	1		28480	1853-0041	1
Q27	SS NPN Si			28480	1854-0071	

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A7028	SS NPN-SI	1		28480	1854-0244	1
Q29	SS PNP-SI			28480	1853-0099	1
Q30, 31	Power NPN-SI			28480	1854-0095	1
R1	fxd, film 1M Ω \pm 1%, 1/4W	1	Type CEB T-O	07716	0757-0344	1
R2	fxd, film 45K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-5091	1
R3	fxd, film 619 Ω \pm 1%, 1/4W	1	Type CEB T-O	07716	0757-0728	1
R4, 5	fxd, film 200K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0757-0472	1
R6	fxd, comp 1K Ω \pm 5%, 1/2W	6	EB-1025	01121	0686-1025	2
R7	fxd, film 4.75K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0437	1
R8	fxd, film 118K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-3265	1
R9	var. ww 100 Ω \pm 5%	1	Type 100	11502	2100-1450	1
R10, 11	fxd, film 21.5 Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0698-3430	1
R12, 13	fxd, film 43K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0698-5090	1
R14, 15	fxd, film 12K Ω \pm 1%, 1/8W	3	Type CEA T-O	07716	0698-5088	1
R16	fxd, comp 1K Ω \pm 5%, 1/2W	1	EB-1025	01121	0686-1025	1
R17, 18	fxd, film 510 Ω \pm 1%, 1/4W	2	Type CEB T-O	07716	0698-5145	1
R19	fxd, comp 100 Ω \pm 5%, 1/2W	3	EB-1015	01121	0686-1015	1
R20	fxd, film 12K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0698-5088	1
R21	fxd, comp 1.3K Ω \pm 5%, 1/2W	3	EB-1325	01121	0686-1325	1
R22, 23	fxd, comp 51 Ω \pm 5%, 1/2W	2	EB-5105	01121	0686-5105	1
R24	fxd, comp 5.6K Ω \pm 5%, 1/2W	1	EB-5625	01121	0686-5625	1
R25	fxd, comp 560 Ω \pm 5%, 1/2W	3	EB-5615	01121	0686-5615	1
R26	fxd, comp 510 Ω \pm 5%, 1/2W	1	EB-5115	01121	0686-5115	1
R27	fxd, comp 3K Ω \pm 5%, 1/2W	1	EB-3025	01121	0686-3025	1
R28	fxd, comp 5.1K Ω \pm 5%, 1/2W	4	EB-5125	01121	0686-5125	1
R29	fxd, comp 1.5K Ω \pm 5%, 1/2W	3	EB-1525	01121	0686-1525	1
R30	fxd, comp 2.2K Ω \pm 5%, 1/2W	1	EB-2225	01121	0686-2225	1
R31	fxd, comp 2K Ω \pm 5%, 1/2W	4	EB-2025	01121	0686-2025	1
R32	fxd, comp 8.2K Ω \pm 5%, 1/2W	2	EB-8225	01121	0686-8225	1
R33	fxd, comp 2K Ω \pm 5%, 1/2W		EB-2025	01121	0686-2025	1
R34	fxd, comp 8.2K Ω \pm 5%, 1/2W		EB-8225	01121	0686-8225	1
R35	fxd, comp 120K Ω \pm 5%, 1/2W	2	EB-1245	01121	0686-1245	1
R36	fxd, comp 910 Ω \pm 5%, 1/2W	1	EB-9115	01121	0686-9115	1
R37	fxd, comp 120K Ω \pm 5%, 1/2W		EB-1245	01121	0686-1245	1
R38	fxd, met. oxide 18K Ω \pm 5%, 2W	1	Type C42S	16299	0764-0006	1
R39	fxd, comp 200 Ω \pm 5%, 1/2W	6	EB-2015	01121	0686-2015	1
R40	fxd, comp 12K Ω \pm 5%, 1/2W	1	EB-1235	01121	0686-1235	1
R41	fxd, comp 18 Ω \pm 5%, 1/2W	2	EB-1805	01121	0686-1805	1
R42	fxd, comp 1K Ω \pm 5%, 1/2W		EB-1025	01121	0686-1025	1
R43	fxd, comp 200 Ω \pm 5%, 1/2W		EB-2015	01121	0686-2015	1
R44	fxd, comp 18 Ω \pm 5%, 1/2W		EB-1805	01121	0686-1805	1
R45	fxd, comp 82K Ω \pm 5%, 1/2W	2	EB-8235	01121	0686-8235	1
R46	fxd, comp 62K Ω \pm 5%, 1/2W	2	EB-6235	01121	0686-6235	1
R47	fxd, comp 200 Ω \pm 5%, 1/2W		EB-2015	01121	0686-2015	1
R48	fxd, met. oxide 15K Ω \pm 5%, 2W	1	Type C42S	16299	0686-3647	1
R49	fxd, comp 62K Ω \pm 5%, 1/2W		EB-6235	01121	0686-6235	1
R50	fxd, comp 82K Ω \pm 5%, 1/2W		EB-8235	01121	0686-8235	1
R51, 53	fxd, comp 200 Ω \pm 5%, 1/2W		EB-2015	01121	0686-2015	1
R54	fxd, comp 5.1K Ω \pm 5%, 1/2W		EB-5125	01121	0686-5125	1
R55	fxd, comp 100 Ω \pm 5%, 1/2W		EB-1015	01121	0686-1015	1
R56	fxd, film 1.50K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0757-0427	1
R57	fxd, comp 15K Ω \pm 5%, 1/2W	2	EB-1535	01121	0686-1535	1
R58	fxd, comp 2K Ω \pm 5%, 1/2W		EB-2025	01121	0686-2025	1
R59	fxd, comp 1.5K Ω \pm 5%, 1/2W	2	EB-1525	01121	0686-1525	1

Table 6-4. Replaceable Parts

REP. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	PIP PART NO.	RS
A7R60	fxd, film 1.50K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0757-0427	
R61	fxd, comp 15K Ω \pm 5%, 1/2W		EB-1535	01121	0686-1535	
R62	fxd, comp 1K Ω \pm 5%, 1/2W		EB-1025	01121	0686-1025	
R64	fxd, comp 200 Ω \pm 5%, 1/2W		EB-2015	01121	0686-2015	
R65	fxd, comp 5.1K Ω \pm 5%, 1/2W		EB-5125	01121	0686-5125	
R66	fxd, comp 100 Ω \pm 5%, 1/2W		EB-1015	01121	0686-1015	
R67	fxd, comp 1.5K Ω \pm 5%, 1/2W		EB-1525	01121	0686-1525	
R58	fxd, comp 27K Ω \pm 5%, 1/2W	1	EB-2735	01121	0686-2735	1
R69	fxd, comp 39K Ω \pm 5%, 1/2W	1	EB-3935	01121	0686-3935	1
R70	fxd, comp 150 Ω \pm 5%, 1/2W	1	EB-1515	01121	0686-1515	1
R71	fxd, comp 4.3K Ω \pm 5%, 1/2W	3	EB-4325	01121	0686-4325	1
R72	fxd, comp 10K Ω \pm 5%, 1/2W	2	EB-1035	01121	0686-1035	1
R73	fxd, comp 4.3K Ω \pm 5%, 1/2W		EB-4325	01121	0686-4325	
R74	fxd, comp 750 Ω \pm 5%, 1/2W	2	EB-7515	01121	0686-7515	1
R75	fxd, comp 7.5K Ω \pm 5%, 1/2W	2	EB-7525	01121	0686-7525	1
R76	fxd, comp 560 Ω \pm 5%, 1/2W		EB-5615	01121	0686-5615	
R77	fxd, film 6.2K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0698-5087	1
R78	fxd, film 4.53K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0698-4443	1
R79	fxd, comp 4.3K Ω \pm 5%, 1/2W		EB-4325	01121	0686-4325	
R80	fxd, comp 750 Ω \pm 5%, 1/2W		EB-7515	01121	0686-7515	
R81	fxd, comp 7.5K Ω \pm 5%, 1/2W		EB-7525	01121	0686-7525	
R82	fxd, comp 560 Ω \pm 5%, 1/2W		EB-5615	01121	0686-5615	
R83	fxd, film 6.2K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0698-5087	
R84	fxd, film 4.53K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0698-4443	
R85	var. ww 200 Ω \pm 10%	1	Type 500	11502	2100-1771	1
R86	fxd, ww 89.90K Ω \pm 1%, 5ppm	1	Type 7009	01686	0811-2578	1
R87	fxd, ww 10.0K Ω \pm 1%, 5ppm	1	Type E30	01686	0811-1094	1
R88	fxd, comp 9.1K Ω \pm 5%, 1/2W	1	EB-9125	01121	0686-9125	1
R89	fxd, comp 1.6K Ω \pm 5%, 1/2W	1	EB-1625	01121	0686-1625	1
R90	fxd, comp 5.1K Ω \pm 5%, 1/2W		EB-5125	01121	0686-5125	
R92	fxd, comp 10K Ω \pm 5%, 1/2W		EB-1035	01121	0686-1035	
R93	fxd, comp 3.9K Ω \pm 5%, 1/2W	1	EB-3925	01121	0686-3925	1
R94	fxd, comp 13K Ω \pm 5%, 1/2W	1	EB-1335	01121	0686-1335	1
R108, 109	fxd, comp 1K Ω \pm 5%, 1/2W		EB-1025	01121	0686-1025	
R110	fxd, film 7.5K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0757-0440	1
R111	fxd, film 1.69K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0698-4428	1
R112	fxd, comp 2K Ω \pm 5%, 1/2W		EB-2025	01121	0686-2025	
R113	fxd, film 249K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0757-0270	1
R114, 115	fxd, comp 1.3K Ω \pm 5%, 1/2W		EB-1325	01121	0686-1325	
R116	fxd, film 1.69K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0698-4428	
R117	fxd, film 249K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0757-0270	
R118, 119	fxd, film 110K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0757-0466	1
R120	fxd, film 7.5K Ω \pm 1% 1/8W		Type CEA T-O	07716	0757-0440	
R121	fxd, met. oxide 180 Ω \pm 5%, 2W	1	RG-42	07716	0698-3626	1
T1	Toroidal Transformer 1:1:1	1		28480	9100-2185	1
VR1, 2	Diode, zener 6.8V 400mW	4		28480	1902-0048	4
VR3	Diode, zener 56.2V \pm 5%, 1W	1		28480	1902-0597	1
VR4	Diode, zener 61.9V \pm 5%, 1W	2		28480	1902-0660	2
VR5, 6	Diode, zener 9.4V 500mW	2	1N2163A	04713	1902-0763	2
VR7	Diode, zener 7.5V 400mW	1		28480	1902-0064	1
VR8	Diode, zener 5.62V 400mW	1		28480	1902-3104	1
VR9	Diode, zener 61.9V \pm 5%, 1W			28480	1902-0660	
VR10, 11	Diode, zener 6.8V 400mW			28480	1902-0048	

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
	CHASSIS ELECTRICAL PARTS					
C1, 2	fxd, elect, 5,000 μ F 25Vdc	2	32D40010	56289	0180-1921	1
C3	fxd, elect, 4,000 μ F 15Vdc	1	602D402G015AA2A	56289	0180-2305	1
C6, 7	fxd, elect, 3,000 μ F 80Vdc	2	36D302G08AC2	56289	0180-2193	1
C8	fxd, mylar 0,01 μ F 200Vdc	1	192P10392	56289	0160-0161	1
DS1	Lamp, glow 115V	1	NE-2H	03508	2140-0015	1
F1	Fuse, 2A 250V, T	1	MDX-2A	71400	2110-0303	5
J1	Jack, Input	1		28480	1251-0087	1
M1	Voltmeter, Dual, 0- \pm 60V, 0- \pm 10V	1		28480	1120-1143	1
M2	Ammeter, Dual 0- \pm 1.2A, 0- \pm 0.3A	1		28480	1120-1145	1
P1	Plug, Input	1		28480	1251-0086	1
Q1, 2	Power NPN SI	2	2N3714	04713	1054-0338	2
Q3, 4	Power PNP SI	2	2N3790	04713	1053-0095	2
S1	Switch, AC Line	1		28480	3101-1055	1
S2	Switch, Range, Current	1		28480	3100-1916	1
S3	Switch, Range, Voltage	1		28480	3100-1919	1
T3	Power Transformer	1		28480	06130-80091	1
Z1	+5V Regulator, IC	1	SL10236	27014	1820-0430	1
	MECHANICAL					
	A1 Input Board					
	Card Extractor Handle	1		28480	5081-4901	
	Roll Pin	1	52012062-250	72962	1480-0059	1
	A2 Logic Board					
	Card Extractor Handle	1		28480	5081-4903	
	Roll Pin	1	52012062-250	72962	1480-0059	1
	IC Socket, 16-pin (Z1-4 or Z9-12)	4	316-AG5D-3R	91506	1200-0767	1
	IC Socket, 14-pin (Z5, Z6)	2	314-AG5D-3R	91506	1200-0768	1
	A3 D/A Board					
	Card Extractor Handle	1		28480	5081-4905	
	Roll Pin	1	52012062-250	72962	1480-0059	1
	Heat Dissipator, Q31	1	NF-207	05820	1205-0033	1
	A6 Control Board					
	Card Extractor Handle	1		28480	5081-4906	
	Roll Pin	1	52012062-250	72962	1480-0059	1
	Heat Dissipator (Q34)	1	NF-207	05820	1205-0033	1
	A7 Amplifier Board					
	Card Extractor Handle	1		28480	06130-80001	
	Roll Pin	1	52012062-250	72962	1480-0059	1
	Heat Dissipator (Q6, 7, 11, 13, 15, 17, 26, 28)	8	NF-207	05820	1205-0033	1
	Front Panel Assembly					
	Front Panel (loaded)	1		28480	06130-60011	
	Front Panel (lettering)	1		28480	06130-60010	
	Meter Bezel	2		28480	4040-0297	1
	Meter Spring	8		28480	1460-0256	2
	Base, Indicator DS1	1		28480	5040-0305	1
	Lens, Indicator DS1	1		28480	5040-0234	1
	Knob, Black, Pointer	2		28480	0370-1099	1

Table 6-4. Replaceable Parts.

REF. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	HP. PART NO.	RS
	MECHANICAL					
	Front Door Assembly	1		28480	06130-60009	
	Door, Blank (Lettering Only)	1		28480	06130-00012	
	Spring, Door	1		28480	06130-00011	1
	Lens, Door	1		28480	5040-0234	1
	Latch, Door	1	27-10-301-10	94222	1390-0037	1
	Rear Panel Assembly	1		28480	5060-7992	
	Rear Panel	1		28480	5000-9490	
	Barrier Strip, 10-Terminal	1		75382	0360-1156	1
	Jumper, Barrier Strip	3		28480	0360-1143	1
	Heat Sink, Rear	2		28480	5020-8068	
	Cover, Heat Sink	2		28480	5000-9442	
	Spacer, Heat Sink Cover, Hex, 8-32 x 5/8 long	4		28480	0380-0719	
	AC Line Cord	1		28480	0120-0050	1
	Strain Relief Bushing, Line Cord	1		28480	0400-0013	1
	Shoulder Washer, Gray, Q1-Q4, Mounting Screws,	8		28480	2190-0491	6
	Bushing, Transistor Pins, Q1-Q4	8		28480	0340-0166	6
	Bushing, Transistor Screws, Q1-Q4	8		28480	0340-0168	6
	Insulator, Misc. Q1-Q4	4		28480	0340-0174	4
	Hinge, Plastic	2		28480	5040-1449	
	Bracket, Hinge	2		28480	5000-6208	
	Fuse Holder	1	342.014	75915	1400-0084	1
	Hex Nut, Fuse Holder	1		20480	2950-0038	1
	Lockwasher, Fuse Holder	1		28480	2190-0037	1
	Neoprene Washer, Fuse Holder	1		28480	1400-0090	1
	Rear Chassis	1		28480	5000-6206	
	Spacer, Rear Chassis, Hex, 8-32 x 7/8 long	4		28480	0380-0392	
	Cover, Bottom	1		28480	5000-9805	
	Cover, Top	1		28480	5000-9806	
	Side Frame	2		28480	5060-0731	
	Side Cover, Front	2		28480	5000-0703	
	Side Cover, Rear	2		28480	5000-0701	
	Side Trim, Fluted, Adhesive Back	2		28480	5000-0051	
	Handle Assembly, Side	2		28480	5060-0222	1
	Retainer, Side Handle, Sheet Metal	2		28480	5060-0766	1
	Chassis, Power Supply, U- Shape, Aluminum Sheet Metal	1		28480	5000-6205	
	Chassis, Plug-In Card, Aluminum Sheet Metal	1		28480	5000-6204	
	Guide Rail, Plug-In Card, Plastic, Right	5		28480	5040-1419	
	Guide Rail, Plug-In Card, Plastic, Left	5		28480	5040-1420	

Table 6-4. Replaceable Parts

REF. DRWG.	DESCRIPTION	TO	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
	MECHANICAL					
	Shoulder Washer, Plug-In Card Chassis	8		28480	2190-0492	
	Spacer, P.C. Guide 3/8" O.D., #20 C.L.	12	9319-A-19A	06540	Q380-0471	
	Clamp Tube, C1, C2	2		28480	5000-6276	
	MISCELLANEOUS					
	Clamp, 1/4" Dia.	3	T4-4	79307	1400-0330	1
	Clamp, 2" Dia., C3	1	4586-2D	56289	0180-8078	1
	Clamp, 1-3/8" Dia., C6, C7	2	4586-97A	56289	0160-2149	1
	Foot Assembly	5		28480	5060-0767	1
	Stand, Tilt	1		28480	1490-0030	1
	Fastener	4	C17859632-24D	89032	0590-0053	1
	Fastener	9	C8022632-24B	89032	0590-0710	2
	Rack Mounting Kit (Includes Rack Ears, Trim, and Screws)	1		28480	5060-0740	
	Packing Carton	1		28480	9211-1180	
	Floater Pad, Packing Carton	2		28480	9220-1400	
	Extender Assembly, Plug-In Board	1		28480	5060-7948	
	Printed Circuit Board	1		28480	5020-8049	
	Printed Circuit Board Connector	1	251-20-30-390	71785	1251-0495	
	Epoxy Plate	1		28480	5020-5728	

SECTION V MAINTENANCE

5-1 INTRODUCTION

5-2 Upon receipt of the power supply, the performance test (Paragraph 5-6) should be made. This check is suitable for incoming inspection. If a fault is detected in the power supply while making the performance check or during normal operation, proceed to the troubleshooting procedures (Paragraph 5-37). After troubleshooting and repair, perform any necessary adjustments and calibrations (Paragraph 5-69). Before returning the power supply to normal operation, repeat the performance test to ensure that the fault has been properly corrected and that no other faults exist. Before performing any maintenance checks, turn on the power supply and allow a 30-minute warm-up.

5-3 TEST EQUIPMENT REQUIRED

5-4 Table 5-1 lists the test equipment required to perform the various procedures described in this section.

NOTE

In certain maintenance procedures (including troubleshooting), DVS plug-in boards are required to be mounted on the Extender Board (supplied with the DVS). The extender board includes an epoxy plate that is positioned with screws on either side of the extender board printed circuit board to interface with the particular plug-in board being extended. The following extender board screw positions (for the epoxy board) are to be used for extending the associated plug-in board:

	Extender Board Position	Associated Plug-In Board
Side A	A	D/A (A3)
	B	Logic (A2)
	C	Input (A1)
	D	Control (A6) and Power Amplifier (A7)
Side B	E	Not Used
	F	Not Used
	G	Not Used
	H	Not Used

Note further that when a board is extended, the front panel cover should be completely removed to avoid any possibility of inadvertently touching the plug-in board to the front panel cover.

5-5 To conveniently program the DVS, the Hewlett-Packard Pocket Programmer Model 14533B is recommended. A three-foot 50-conductor extension cable (Model 14534A) is available for convenience in attaching the Pocket Programmer to the rear panel data input connector. If the Pocket Programmer is to be used, read the operating instructions in the Programmer manual before proceeding.

5-6 PERFORMANCE TEST

5-7 The following tests can be used as an incoming inspection check and appropriate portions of the test can be repeated either to check the operation of the instrument after repairs or for periodic maintenance tests. The tests are performed using a nominal 115-volt 60-Hz single-phase input supply to the unit. If the correct result is not obtained for a particular check, do not adjust any controls; proceed to the troubleshooting procedures.

5-8 PRE-OPERATION CHECKOUT

5-9 This procedure checks the basic operation of the DVS to assure that all programming functions are operating satisfactorily.

INITIAL CONDITIONS

1. Check that the rear terminal strip is connected as shown in Figure 3-1. HI should be strapped to HI S (high sense) and LO to LO S (low sense).
2. Connect a digital voltmeter in parallel with a $50\Omega \pm 1\%$ 50 watt resistor across the HI and LO terminals on the rear of the DVS.
3. Connect the Pocket Programmer to the data input connector and set its switches as follows:
 - a. Set the INPUT LEVEL REF switch to DATA COM.
 - b. Set the MP/DCPS switch to DCPS.
 - c. Set the SOURCE SELECT switch to EXT.

(The above three switches remain in these positions)

Table 5-1. Test Equipment Required

TYPE	REQUIRED CHARACTERISTICS	USE	RECOMMENDED MODEL
Diff. or Dig. Voltmeter	Sensitivity: 100 μ V full scale (min.). Accuracy: 0.004%	Measure dc voltages; calibration procedures	HP 3462, 3490, or 3420
Variable Voltage Transformer	Current Rating: 2A. Range: 90-130Vac. Equipped with voltmeter accurate within 1V.	Vary ac input	---
Oscilloscope	Differential input; dc to 50MHz	Display transient response waveforms and p-p noise	HP 180A plus 1801A, 1806A, and 1821A Plug-ins
DC Voltmeter	Accuracy: 1%, Input resistance: 20,000 ohms/volt (min.).	Measure dc voltages	HP 412A
Repetitive Load Switch	Rate: 60-400Hz, 2 μ sec rise and fall time.	Measure transient response	See Figure 5-5.
Resistive Loads	50 Ω , 50W \pm 5%, 17 Ω , 17W \pm 5%.	Power supply load resistors	---
Resistor	Value: 50 Ω , \pm 1%, 50 watts.	Check current latch performance	---
Function Generator	0.0005Hz - 5MHz	Measure programming time	HP 3310A/B
DC Power Supply	0-25Vdc, 0-400mA	Provide input to ANLG IN terminals on DVS.	HP 6215A
Rms Voltmeter	10Hz-10MHz	Measure rms ripple and noise	HP 3400A
Programming Device		Supply digital program inputs	HP Pocket Programmer 1433B

throughout all of the following procedures.)

d. Set the RANGE switch to X10.

e. Set the data and sign bit switches for an output of +0.00 volts. The proper coding for Pocket Programmer data and sign bit switches depends on the instrument being programmed. The voltage magnitude switches might either be up (open circuit) or down (grounded) to program zeros. Similarly, the OUTPUT SIGN switch might be up or down to program a positive output. Refer to the appropriate Option Appendix or the Instrument Modification Sheet supplied with the instrument being programmed for digital input coding information.)

f. Set the I LIMIT switches for a 1000mA

current limit. (all three switches will be down.)

4. Open the front access door and put the STORAGE DISABLE switch on the A2 board in the STORAGE DISABLE position.

5. Connect the line cord and switch the LINE switch to ON. The STORAGE DISABLE light will come on and the front panel meters will both indicate zero. (Select the 10V and .1A meter ranges.)

CURRENT LATCH RESET AND DISCONNECT INTERLOCK CHECK

6. On the Pocket Programmer, switch on the 4096 bit. Observe that the digital voltmeter indi-

reads approximately 0.3 volts (not +40.96V) and the DVS CURRENT meter reads less than 10mA. The error is because the over current latch circuit activated when the DVS was turned-on.

NOTE

Whenever the DVS is turned on the Gate switch must be toggled to reset the over-current latch circuit.

7. Press the Pocket Programmer GATE switch. The digital voltmeter should indicate +40.96V and the DVS CURRENT meter 820mA (1.2A scale).

8. Disconnect the Pocket Programmer data input cable. The meters will indicate 0V and less than 10mA. The instrument is in the disconnect interlock and overcurrent latch status mode.

9. Reconnect the data input cable. The meters will indicate 0V and less than 10mA. The instrument is still in the overcurrent status.

10. Press the Pocket Programmer GATE switch. The meters will indicate +40.96V and 820mA again.

VOLTAGE RANGE CHECK

11. Set the RANGE switch on the Pocket Programmer to X1. The digital voltmeter should read +4.096V.

VOLTAGE MAGNITUDE CHECK

12. On the Programmer, turn on all of the voltage magnitude bits. The digital voltmeter reading will be +16.3835V \pm 0.001V.

13. Turn off all of the voltage magnitude bits. The voltage reading will be 0 volts \pm 0.001 volts.

14. Turn on each voltage magnitude bit 0.5 through 8192, individually, and check the digital voltmeter readings in the following chart (all readings \pm 1mV).

NOTE

Turn each bit off after making check.

SWITCH	READING	SWITCH	READING
0.5	0.5mV	128	128mV
1	1mV	256	256mV
2	2mV	512	512mV
4	4mV	1024	1.024V
8	8mV	2048	2.048V
16	16mV	4096	4.096V
32	32mV	8192	8.192V
64	64mV		

15. Switch the STORAGE DISABLE switch on board A2 to the STORAGE position.

16. Repeat the sequence of Programmer switch operations of step (14) but press the Programmer GATE switch after each voltage magnitude bit change. Observe that the previously programmed voltage remains until the new value is gated into storage.

17. Switch the STORAGE DISABLE switch back to the STORAGE DISABLE position, set the OUTPUT SIGN switch on the Programmer to the negative position and turn off all voltage magnitude bits to obtain -0.5mV, \pm 1mV.

18. Repeat steps (14), (15), and (16), set voltage magnitude switches so that the input is received in the "negative 2's complement". To obtain any negative number, first complement the corresponding positive number and then add a binary "1" to the least significant digit. For example, to program the unit to a -0.5mV output, all switches (0.5 through 8192) must be set to their binary "1" position. To program the supply to -1mV, the 0.5 switch is set to binary "0" and the remaining switches are set to "1". As stated previously, the proper coding for the Pocket Programmer depends upon the instrument being programmed. The voltage magnitude switches may be up (open circuit) or down (grounded) to program ones or zeros. Refer to the appropriate Option Appendix or Modification Sheet supplied with the instrument being programmed.

GROSS CURRENT LIMIT

19. Turn off power to the DVS. Disconnect the 50A load and connect the 17A, 17W load across the HI and LO terminals.

20. On the DVS rear barrier strip, jumper the C_T terminals. This disables the programmable current latch circuit.

21. Set the voltage magnitude switches and OUTPUT SIGN switch on the Programmer for an output voltage of +10 volts.

22. Set the CURRENT METER RANGE switch on the DVS front panel to 1.2A and the STORAGE DISABLE switch on board A2 to DISABLE.

23. Turn on power to the DVS and press the Programmer GATE switch. Observe that the DVS voltmeter reads +10V.

24. While observing the DVS ammeter, increase the voltage magnitude input in +1V steps (to a maximum of +20V) until the current no longer increases (limiting). The current at limiting should be between 1.1A and 1.2A.

25. Set the voltage magnitude switches and OUTPUT SIGN switch on the Programmer for an output voltage of -10V.

26. While observing the DVS ammeter, increase the voltage magnitude input in -1V steps (to a maximum of -20V) until the current no longer increases (limiting). The current at limiting should

be between 1.1A and 1.2A.

CURRENT OVERLOAD CHECK

27. Turn off power to the DVS. Disconnect the 17 Ω , 17 W load and connect the 50 Ω , 1%, 50 watt (minimum) load resistor between the HI and LO terminals. The jumper remains connected between the C_T terminals.

28. Check Option descriptions (Appendix A, B, or C) or, where applicable, the Modification Sheet in the manual to determine the existence of output transistor "pull up" resistor A6A6R8. If A6A6R8 is used proceed to step 29. If A6A5R8 is not used, proceed to step 30.

29. Connect a dc voltmeter between 0 LOAD STATUS and DATA COM test points on the Pocket PROGRAMMER. Select a voltmeter range capable of reading 12 volts. Proceed to step 31.

30. Connect an ohmmeter between the 0 LOAD and DATA COM test points on the pocket programmer. The common lead should be connected to the DATA COM test point.

31. Program the current latch value for 20mA. The I LATCH (current latch) switch positions on the Programmer are listed below for the eight current latch values.

32. Set the voltage magnitude and OUTPUT SIGN on the Programmer for an output voltage of +0.75V.

33. Turn on power to the DVS and press the Programmer GATE switch. Overload status signal should be normal (voltmeters should indicate the collector voltage at output stage or the ohmmeter should indicate an open circuit).

34. Increase the output voltage in 0.1V steps. Overload status signal should switch to the overload state between 0.95V and 1.05V output (voltmeter reads 0V or ohmmeter reads 0 ohms). See following chart:

CURRENT LATCH (mA)	I LATCH SWITCH POSITIONS			CURRENT OVERLOAD OCCURS BETWEEN (Volts)
	L24	L22	L23	
20	up	up	up	0.95 and 1.05
50	up	down	up	2.375 and 2.625
70	up	up	down	3.325 and 3.675
100	up	down	down	4.75 and 5.25
200	down	up	up	9.5 and 10.50
500	down	down	up	23.75 and 26.25
700	down	up	down	33.25 and 36.75
1000	down	down	down	47.50 and 52.50

35. Change the programmable current latch (I LATCH) value and output voltage at which current overload occurs to the values listed in the chart and repeat step (34).

36. Set the OUTPUT SIGN switch to negative and repeat steps (34) and (35).

CURRENT LATCH CHECK

37. Turn off power to the DVS and remove the jumper between the C_T terminals. The 50 Ω load resistor remains connected between the HI and LO output terminals.

38. As in the current overload check step 28, determine the existence of the current latch output transistor "pull up" resistor A6A5R8. If A6A5R8 is used, connect a dc voltmeter between the I LATCH STATUS and DATA COM test points on the Programmer. If A6A5R8 is not used, connect an ohmmeter between these two test points.

39. On the Programmer, set the current latch (I LATCH) to 200mA and the voltage magnitude to 25V.

40. Turn on power to the DVS and press GATE on Programmer. Instrument should remain in current latch condition (voltmeter reads 0V or ohmmeter reads 0 ohms).

41. Remove the 50 Ω load resistor from the HI and LO output terminals. Unit should remain in latched condition until a GATE signal is applied.

5-10 CONSTANT VOLTAGE TESTS

5-11 For constant voltage measurements, the measuring device must be connected across the rear sensing terminals of the supply in order to achieve valid indications. A measurement made across the load includes the impedance of the leads to the load and such lead lengths can easily have an impedance several orders of magnitude greater than the supply impedance (10 milliohms at dc), thus invalidating the measurement.

5-12 To avoid mutual coupling effects, each monitoring device must be connected directly to the sensing terminals by separate pairs of leads. The load resistor is connected across the output terminals and must be selected according to the output voltage and current of the supply. When measuring the constant voltage performance specifications, the CURRENT LATCH should be programmed well above the maximum output current which the supply will draw, since the onset of current latch action will cause a drop in output voltage, increased ripple, and other performance changes not properly ascribed to the constant voltage operation of the supply.

5-13 Calibration Error

Definition: The maximum absolute voltage

accuracy deviation at constant room temperature, 115Vac input, no load, following a minimum warm-up time of 30 minutes, it is the ability of the instrument to accurately convert a digital input into an analog output voltage.

5-14 To measure the accuracy, proceed as follows:

- Connect a digital or differential voltmeter to the HI and LO sensing terminals on the rear of the unit.
- Program the output to 50.00V and gate the unit.
- The voltmeter should read 50.00V \pm 10mVdc.
- Set the range switch to X1.
- Program the output to -16.384 volts. Gate the input.
- The differential voltmeter should read -16.384V \pm 1mVdc.

5-15 Voltmeter Accuracy. To check the accuracy of the front panel voltmeter, proceed as follows:

- Connect a Digital or differential voltmeter to the HI and LO sensing terminals on the rear of the unit.
- Turn on supply and program the output voltage for 50.00V. Gate the unit.
- Record the reading on the voltmeter.
- The reading on the front panel meter should be the same as the reading in Step (c) \pm 1.5 volts.

5-16 Load Regulation

Definition: The change ΔE_{OUT} in the static value of dc output voltage resulting from a change in load resistance from open circuit to a value which yields maximum rated output current (or vice versa).

5-17 Load regulation should be checked in both: the higher (X10) range with both negative and positive output voltages and the lower (X1) range with both positive and negative output voltages, since any one of these four conditions can yield an unsatisfactory result, which is not reflected under the other three conditions. To test the load regulation for all four conditions, proceed as follows:

- Connect test setup shown in Figure 5-1. Set the METER switch to the highest voltage and current ranges.
- Program the current latch to 1 ampere.
- Turn on supply.
- Program the output voltage to +50.00 volts, and gate the unit.
- Read and record voltage indicated on

voltmeter.

- Disconnect load (open) and gate the unit.
- Reading on voltmeter should not vary from reading recorded in Step (e) by more than 500 μ V.
- Reconnect load.
- Program the output to -50.00V and gate the unit.
- Repeat Steps (e) and (f).
- Reading on voltmeter should not change from reading recorded in Step (e) by more than 500 μ V.
- Program the output to +16.3835 volts. X1 range and gate the unit.
- Change load to 17 Ω , 17 watts.
- Repeat Steps (e) and (f).
- Reading on voltmeter should not change from the reading recorded in Step (e) by more than 150 μ V.
- Reconnect load (17 Ω , 17W).
- Program the output to -16.384 volts. X1 range and gate the unit.
- Repeat Steps (e) and (f).
- Reading on voltmeter should not change from reading recorded in Step (e) by more than 150 μ V.

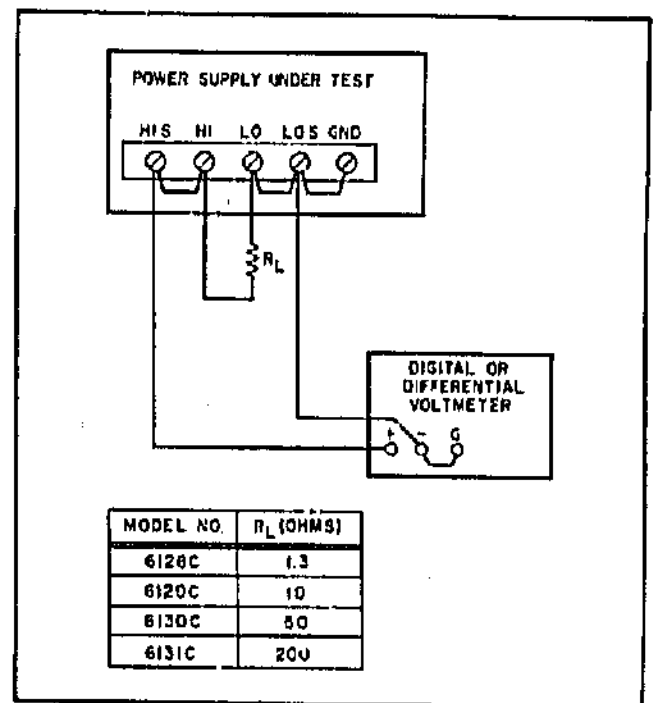


Figure 5-1. Constant Voltage Load Regulation Test Setup

5-18 Line Regulation

Definition: The change, ΔE_{OUT} in the static value of dc output voltage resulting from a change in ac input volt-

age over the specified range from low line, 10% less than nominal, to high line, 10% more than nominal, or high line to low line.

5-19 Line regulation should be checked in both the higher (X10) range with both negative and positive output voltages and the lower (X1) range with both positive and negative output voltages, since any one of these four conditions can yield an unsatisfactory result, which is not reflected under the other three conditions. To test the line regulation for all four conditions, proceed as follows:

a. Connect test setup shown in Figure 5-1. Set the METER switch to the highest voltage and current ranges.

b. Connect variable auto transformer between input power source and power supply 115Vac input.

c. Program the current latch to 1 ampere.

d. Program the output voltage to 50.00 volts, X10 range.

e. Program the output voltage sign to positive (+).

f. Adjust variable auto transformer for low line (103.5Vac). Gate the unit.

g. Read and record voltage indicated on voltmeter.

h. Adjust variable auto transformer for high line (126.5Vac). Gate the unit.

i. Reading on differential voltmeter should not vary from reading recorded in Step (g) by more than 5mV.

j. Program the output voltage sign to negative (-). Perform Steps (f) through (i).

k. Program the output voltage to

16.3835Vdc, X1 range. Change R_L to 17 Ω , 17W.

l. Program the output voltage sign to positive (+). Perform Steps (f) through (h).

m. The reading on the voltmeter should not vary from the reading recorded in Step (g) by more than 500 μ V.

n. Program the output voltage sign to negative (-). Perform (f) through (h).

o. The reading on the voltmeter should not vary from the reading recorded in Step (g) by more than 500 μ V.

5-20 Temperature Coefficient

Definition: The change in output voltage per degree Centigrade change in the ambient temperature under conditions of constant input ac line voltage, output voltage setting, and load resistance.

5-21 The temperature coefficient of a power supply is measured by placing the power supply in an oven and varying the temperature over any span within its rating. (Most HP power supplies are

rated for operation from 0°C to 55°C.) The power supply must be allowed to thermally stabilize for a sufficient period of time at each temperature of measurement, usually 1/2 hour.

5-22 To check the temperature coefficient, proceed as follows:

a. Connect test setup shown in Figure 5-1.

b. Strap C_T terminals and program the output voltage to 50.00 volts. Gate the unit.

c. Insert the power supply into the temperature-controlled oven (voltmeter and load resistance remain outside oven). Set the temperature to 30°C and allow 30 minutes warm-up.

d. Record the voltmeter indication.

e. Raise the temperature to 40°C and allow 30 minutes warm-up.

f. The voltmeter indication should change by less than 8mV from indication recorded in Step (d).

g. Program the output voltage to 16.3835 volts. Gate the unit. Change R_L to 17 Ω , 17W. Perform Steps (c) through (e).

h. The voltmeter indication should change by less than 1.6mV from indication recorded in Step (d).

5-23 Programming Time

Definition: Maximum time required for the output voltage to settle to within 0.1% of the programmed voltage change after simultaneous receipt of the data and gate commands as measured with a resistive load.

5-24 Equal positive and negative output voltages cannot be obtained by simple switching the position of the polarity switch; negative numbers must be programmed in the 2's complement form. For this reason, a computer or calculator would be the easiest means to obtain the equal positive and negative numbers necessary to perform this test. To perform this test for "worst case" result, use the test setup in Figure 5-2 employing the computer or calculator recommended. Program the computer or calculator so that it will program the DVS between +16.3835 and -16.384 volts and between +50 and -50 volts. The observed waveform should be within the tolerance of Figure 5-3. If the computer or calculator is not available, use the Pocket Programmer and Function Generator (see Figure 5-2) as the programming device and proceed as follows:

CONTROL SETTINGS

a. Set switches on HP 3490A as follows:

1. FUNCTION: DC
2. RANGE: As needed 10V or 100V
3. SAMPLE RATE: HOLD

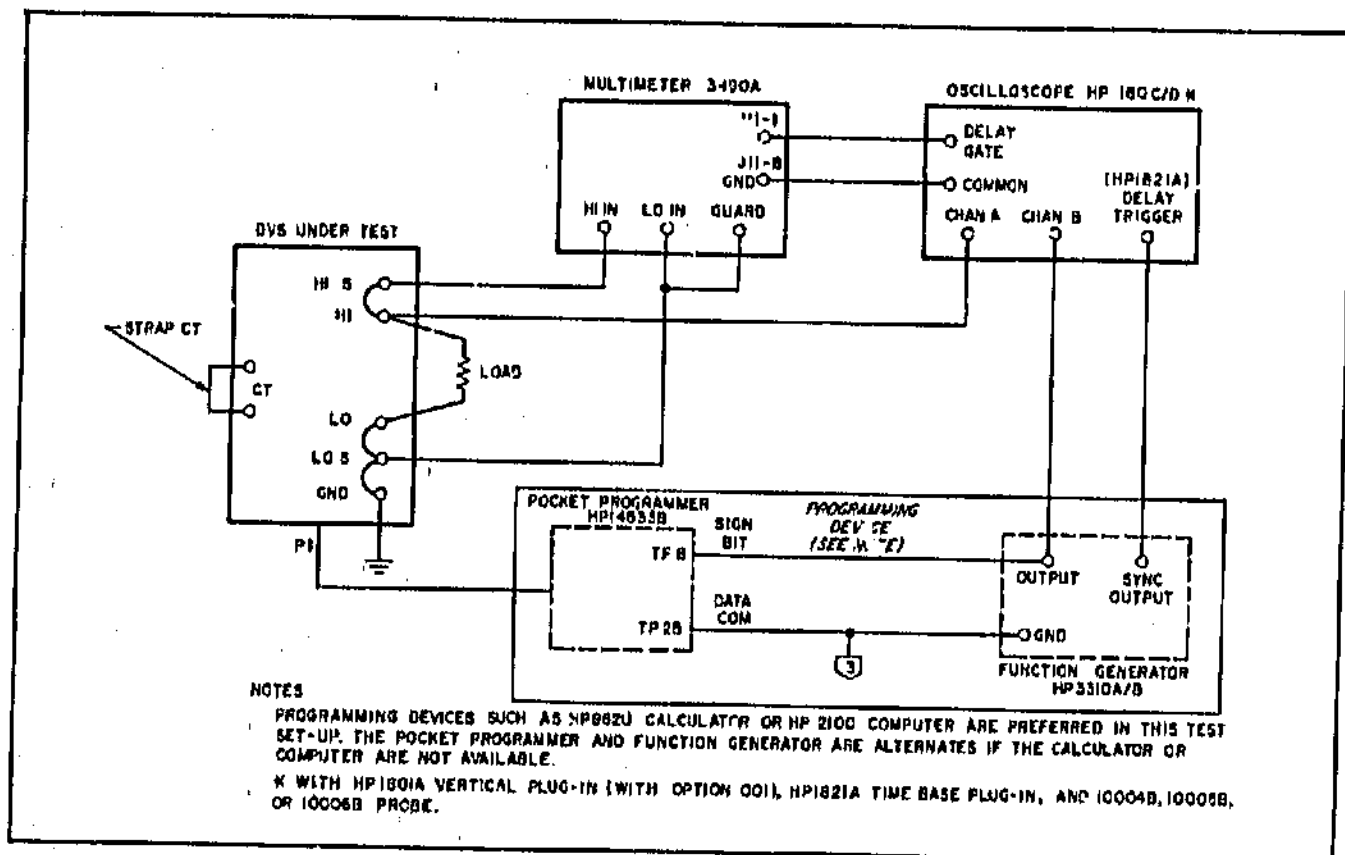


Figure 5-2. Programming Time Test Setup

4. SAMPLE/HOLD: TRACK/HOLD
 - b. Set switches on HP 1821A Delay Section of HP 180 C/D as follows:
 1. AC or ACF; SLOPE + or -; AUTO
 2. TRIGGER LEVEL; Adjust for stable display
 3. TIME/DIV; Delayed to 0.1 to 0.5 μ sec
 - c. Set HP 1821A Main Section of HP 180 C/D as follows:
 1. SWEEP MODE: AUTO
 2. INT; SLOPE + or -; AC
 3. TIME/DIV; 1msec with X10 magnifier
 4. Set sweep to MAIN
 - d. Set switches on HP 3310 A/B as follows:
 1. FREQUENCY; 100Hz
 2. FUNCTION; Squarwave
 3. OUTPUT LEVEL; Value specified in DVS Appendix for data and sign bits.
 - e. Set switches on HP 14533B as follows:
 1. SOURCE SELECT; EXT
 2. MP/DCPS; DCPS
 3. I LATCH; All bits down (maximum I LATCH)
 4. INPUT LEVEL REF; DATA COM
 5. RANGE; X1
 - f. On DVS A2 board, set switch to STORAGE DISABLE (only if Pocket Programmer is used).

PROCEDURE

- a. Connect 50 Ω , 50W load between HI and LO

- b. Connect 3310 A/B output (after adjusting to proper levels) to 14533B.

Example: Program all but the 8192 Bit to the down (shorted to Data com.) position. Program the sign bit to the up (not shorted to Data com.) position. Connect the 3310 A/B output to the sign bit and DATA com to the 3310 A/B ground. The output will now program between -8.1925 volts and +8.192 volts, for a $\Delta V_{OUT} = 16.3845$ volts. In this example 0.1% of $\Delta V_{OUT} = 16.3845$ mV. The output voltage should read within 16mV of final value within 300 μ sec.

- c. Obtain a stable display on oscilloscope. While adjusting DELAY (DIV) control on 1821A, look for the bright spot on the CRT trace. The beginning of the bright spot indicates where the 3490A will be triggered.

- d. To calibrate system delay, adjust bright spot on CRT display (using DELAY control) to the position where the 3490A indicates approximately zero volts. The time between the actual zero crossing of the DVS output (channel A) and the start of the bright spot indicates system delay (T_d).

- e. Measure the voltage just prior to the waveform transitions (see Figure 5-3). Voltage reading should be within 0.1% of ΔV_{OUT} .

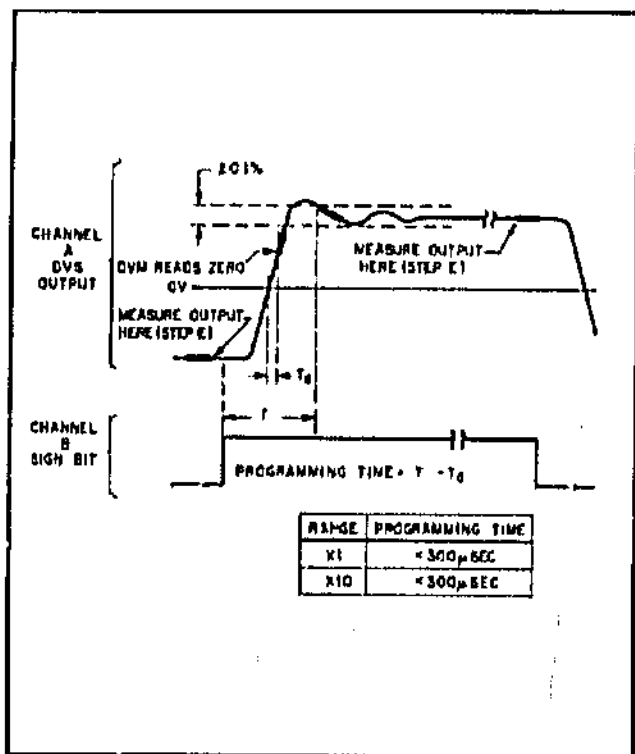


Figure 5-3. Programming Time Waveforms

Example: as before $\Delta V_{OUT} = 16.3845$ volts; 0.1% of $\Delta V_{OUT} = 16\text{mV}$. For a -8.1925 volt to $+8.192$ volt transition, look for a reading of $+8.176$ volts on the 3490A.

f. Using the DELAY control on the 1821A, start at the zero crossing and sweep until the voltage in step e is reached. Determine the time (T) from the transition time of channel B trace to the beginning of the bright spot. DVS programming time will then be:

$$\text{Programming Time} = T - T_d$$

5-25 Ripple and Noise

Definition: The residual ac voltage which is superimposed in the dc output of a regulated power supply.

Ripple and noise may be specified and measured in terms of its RMS or (preferable) peak-to-peak value.

Ripple and noise measurement can be made at any input ac line voltage combined with any dc output voltage and load current within rating.

5-26 The amount of ripple and noise that is present on the power supply output is measured either in terms of the RMS or (preferable) peak-to-peak value. The peak-to-peak measurement is particularly important for applications where noise spikes could be detrimental to a sensitive load, such as logic circuitry. The RMS measurement

is not an ideal representation of the noise, since fairly high output noise spikes of short duration could be present in the ripple and not appreciably increase the RMS value.

5-27 RMS Measurement. To check the rms value of ripple and noise, proceed as follows:

- Connect 50Ω , 50W load across HI and LO terminals.
- Using coax cable, connect rms voltmeter (HP 3400A is recommended) to the DVS HI and LO terminals. On the DVS end, connect the coax inner conductor to the HI terminal and the coax shield lead to the LO terminal (which is also connected to DVS ground).
- Strap C_T terminals together.
- Program the output voltage for 50.0 volts and the voltage range to X10.
- The voltmeter should read less than 1.5mV rms.
- Program the voltage range to X1 and output voltage to $+16.3835$ volts. Change load to 17Ω , 17W.
- The voltmeter should read less than 0.5mV rms.

5-28 Note that a continuous ground loop exists from the third wire of the input power cord of the rms meter via the grounded power supply case, the wire between the negative output terminal of the power supply and the input of the meter, and the grounded meter case. Any ground current circulating in this loop as a result of the difference in potential E_G between the two ground points causes an IR drop which is in series with the meter input. This IR drop, normally having a 60Hz line frequency fundamental, plus any pickup on the leads interconnecting the power supply and meter, appears in the meter reading. The magnitude of this resulting noise signal can easily be much greater than the true ripple developed between the output terminals of the power supply, and can completely invalidate the measurement. To minimize the effects of ground current flow, the DVS and test instruments in all ripple and noise measurements should be plugged into the same ac power buss whenever possible.

5-29 Peak-to-Peak Measurements. The same ground current and pickup problems exist if an oscilloscope is substituted in place of the rms voltmeter in the peak-to-peak measurements. However, the oscilloscope display, unlike the true rms meter reading, tells the observer immediately whether the fundamental period of the signal displayed is 8.3 milliseconds ($1/120\text{Hz}$) or 16.7 milliseconds ($1/60\text{Hz}$). Since the fundamental ripple frequency present on the output of an HP supply is 120Hz (due to full-wave rectification), an oscilloscope display showing a 120Hz fundamental com-

ponent is indicative of a "clean" measurement setup, while the presence of a 60Hz fundamental usually means that an improved setup will result in a more accurate (and lower) value of measured ripple. To verify that the oscilloscope is not displaying ripple that is induced in the leads or picked up from the grounds, the (+) scope lead should be shorted to the (-) scope lead at the power supply terminals. The ripple value obtained when the leads are shorted should be subtracted from the actual ripple measurement.

5-30 The simple, direct test equipment connection of the rma measurement is normally not adequate to measure the high-frequency components of the peak-to-peak ripple and noise. Figure 5-4A shows a technique using a 50 Ω coaxial cable between the DVS and oscilloscope that is terminated in its characteristic impedance. Note that the terminating network is placed across the DVS output to avoid attenuating the low-frequency (60Hz) component of the ripple and noise. Further, the impedance matching network eliminates standing waves and cable ringing which might introduce erroneous values in the measurement.

5-31 In most cases, the single-ended scope method of Figure 5-4A will be adequate to eliminate non-real components of ripple so that a satisfactory measurement may be obtained. However, if the DVS and oscilloscope cannot be plugged into the same ac power buss or the peak-to-peak reading obtained with a single ended scope exceeds the specifications due to I_S , it will be necessary to use a differential scope with properly terminated floating inputs as shown in Figure 5-4B. Note that the coax connectors are not connected to ground on the DVS end. Because of its common mode rejection, a differential oscilloscope displays only the difference in signal between its two vertical input terminals, thus ignoring the effects of any common mode signal produced by the difference in the ac potential between the power supply case and scope case. Before using a differential input scope in this manner, however, it is imperative that the common mode rejection capability of the scope be verified by shorting together its two input leads at the power supply and observing the trace on the CRT. If this trace is a straight line, then the scope is properly ignoring any common mode signal present. If this trace is not a straight line, then the scope is not rejecting the ground signal and must be realigned in accordance with the manufacturer's instructions until proper common mode rejection is attained.

5-32 To check the peak-to-peak ripple and noise output, proceed as follows:

a. Connect 50 Ω , 50W load, impedance matching network(s), and oscilloscope as shown

in Figures 5-4A or 5-4B.

- b. Strap together C_T terminals.
- c. Program the output voltage for 50.0 volts.
- d. The observed ripple should be less than 7mV p-p.
- e. Program the voltage range to X1, the output voltage to +16,3835 volts, and change load to 17 Ω , 17W. The observed ripple should be less than 2mV p-p.

5-33 Transient Recovery Time

Definition: The time "X" for output voltage recovery to within "Y" millivolts of the nominal output voltage following a "Z" amp step change in load current—where: "Y" is specified as 0.1% of full range voltage. The nominal output voltage is defined as the dc level half way between the static output voltage before and after the imposed load change, and "Z" is the specified load current change, which is equal to the rated output current.

5-34 A mercury-wetted relay, as connected in the load switching circuit of Figure 5-5 should be used for loading and unloading the supply. When this

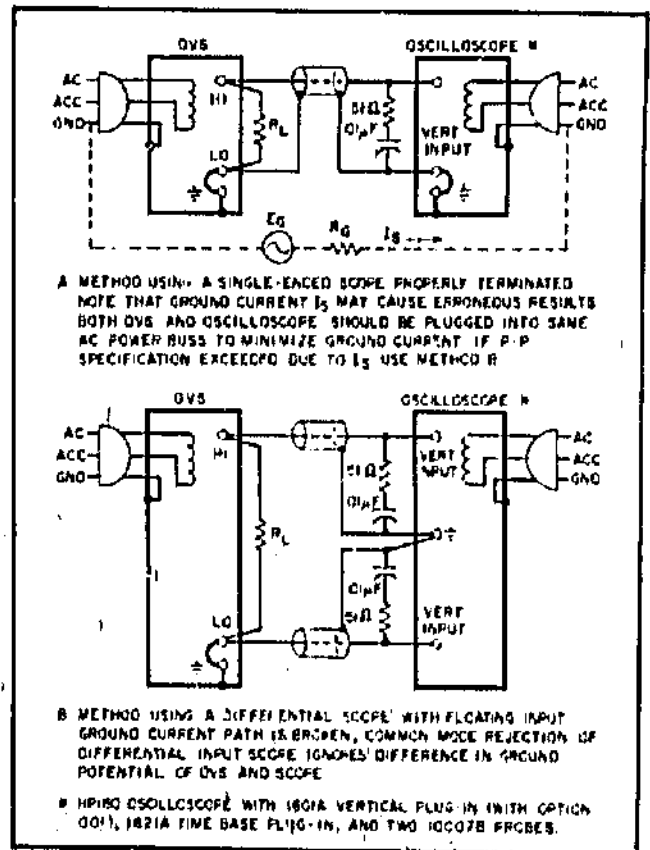


Figure 5-4. Peak-to-Peak Ripple and Noise Test Setup

load switch is connected to a 60Hz ac input, the mercury-wetted relay will open and close 60 times per second. Adjustment of the 25K control permits adjustment of the duty cycle of the load current switching and reduction in jitter of the oscilloscope display.

5-35 The maximum load ratings listed in Figure 5-5 must be observed in order to preserve the mercury-wetted relay contacts. Switching of larger load currents can be accomplished with mercury pool relays; with this technique fast rise times can still be obtained, but the large inertia of mercury pool relays limits the maximum repetition rate of load switching and makes the clear display of the transient recovery characteristic on an oscilloscope more difficult.

5-36 The transient recovery time is checked in both the X10 and X1 ranges as follows:

- Connect test setup shown in Figure 5-5.
- Strap C_T terminals together.

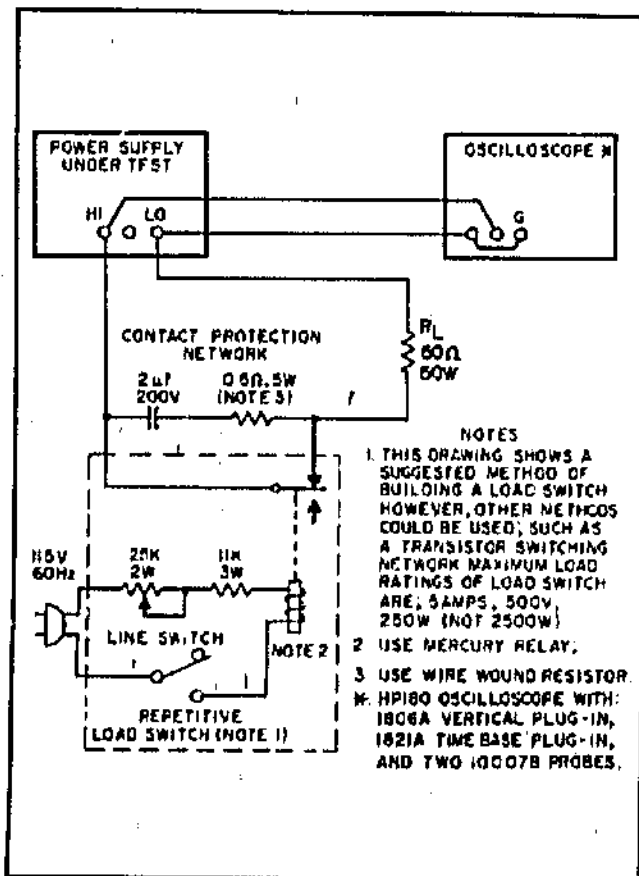


Figure 5-5. Transient Recovery Time, Test Setup

c. Turn on supply and program the output voltage to +50.00 volts and voltage range to X10 (50V).

d. Close the line switch on the repetitive

load switch setup.

e. Set the oscilloscope for internal sync and lock on either the positive or negative load transient spike.

f. Set the vertical input of the oscilloscope for ac coupling so that small dc level changes the output voltage of the power supply will not cause the display to shift.

g. Adjust the sync controls separately for the positive and negative going transients so that not only the recovery waveshape but also as much as possible of the rise time of the transient is displayed.

h. Starting from the major graticule division representative of time zero, count to the right 150 μ sec and vertically 50mV. Recovery should be within these tolerances as illustrated in Figure 5-6.

i. Program the output voltage to +16.3835 volts, change R_T to 17 Ω , 17W and the voltage range to X1.

j. The transient recovery should be within 16mV at 150 μ sec as illustrated in Figure 5-6.

5-37 TROUBLESHOOTING

5-38 Before attempting to troubleshoot this instrument, make certain that the trouble lies within the instrument and not in any associated equipment. In order to isolate the DVS from the system in which it is being used, the HP Pocket Programmer 14533B is recommended. This device permits the operator to manually program all functions of the DVS and thus isolate it from other possible sources of trouble within the system, such as computer interfacing or a programming error.

5-39 A good understanding of the principles of operation of the instrument is essential to an efficient approach to troubleshooting. For this

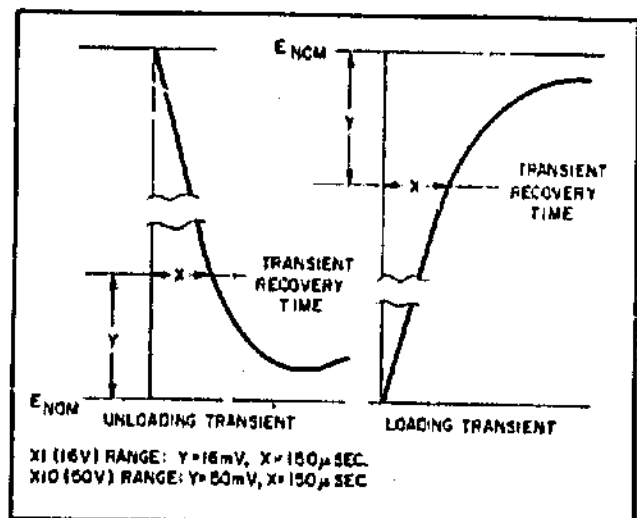


Figure 5-6. Transient Recovery Time, Waveforms

reason it is recommended that Section IV, Principles of Operation be reviewed before attempting to troubleshoot the unit. Once the principles of operation are understood, follow the steps of the Overall Trouble Isolation Procedure in paragraphs 5-43 through 5-46 in the given order to establish which circuit areas are functional and which are not. References to more detailed troubleshooting guides are given in that procedure.

5-40 The four sheets of schematic diagrams of Figure 7-2 are based on the functional organization of the unit. Figure 7-1 provides an overall block diagram of the unit, except for its power distribution, and is especially convenient for tracing signal flow through the entire instrument. The circled test point numbers on Figures 7-1 and 7-2 are also marked on the component location diagrams which accompany the schematics. References are made to these test points in the Principles of Operation section of the manual, as well.

5-41 Before proceeding with the trouble isolation procedure, check for obvious troubles such as an open fuse, a defective power cord, an input power failure, a defective meter or a loosely connected board. Next visually inspect the boards for mechanical damage discolored or charred components, etc. If the source of trouble cannot be detected by visual inspection perform the Overall Trouble Isolation Procedure given below. Throughout the course of troubleshooting the instrument, do not neglect the possibility of two or more faults being present.

CAUTION

Trouble isolation by exchanging a known good board for a suspected faulty one is allowed only for the A1, A2, and A3 boards. Exchanging a good board for a faulty one in any of the other card slots will often result in causing damage to the good board.

5-42 OVERALL TROUBLE ISOLATION PROCEDURE

5-43 Trouble Isolation - Power Distribution.

Almost any trouble symptom could be caused by an incorrect power supply or reference voltage, thus it is good practice to routinely check all of the most important power supply voltages before attempting to isolate a problem to a particular circuit. The tests described in Table 5-2 provide a relatively fast check for trouble in this area. In many cases these checks can save hours that might be spent troubleshooting circuits which are not themselves defective. The A4 power supply board test points are accessible by removing the top cover; the A7 power amplifier test points are accessible by installing the extender board/A7 combination in the A7 slot. The test points are located by referring to the component location diagrams.

5-44 Notice that there are four separate power supply common return systems in the DVS, designated common ①, common ②, common ③ and common ④. When making any voltage or waveform measurements, be sure to use the appropriate power supply common reference point. The appropriate common point can be determined by referring to the circuit schematics of Figure 7-2. If the supply voltages are correct or if the supply voltages are incorrect but the components in that supply are not defective, proceed to paragraph 5-45.

5-45 Overall Troubleshooting Table. After checking the power supplies, disconnect the load and examine Table 5-3. This table contains a list of symptoms and probable causes that may cut down on troubleshooting time. For each trouble symptom Table 5-3 isolates the fault to a component or group of components or directs the reader to additional procedures if further isolation of the trouble is necessary.

Table 5-2. Power Supply Troubleshooting

METER COMMON	METER POSITIVE	NORMAL READING	MAXIMUM RIPPLE P-P	PROBABLY DEFECTIVE COMPONENT
③	TP84	12 ± 1.5Vdc	0.2V	A4C1, CR2, CR3 or R1
TP85	③	12 ± 1.5Vdc	0.6V	A4C2, CR1, CR4, or R2
TP86	③	10 ± 2.0Vdc	0.6V	A4C10, CR22, CR5, CR6 or R27
TP87	④	5.0 ± .25Vdc	5mV	A4C3, CR8, CR9, R3, A5C1, C2, or Z1
TP88	②	26 ± 4Vdc	1.2V	A4C4, C19, C21, CR10, CR12 or R4
②	TP89	26 ± 4Vdc	0.8V	A4C5, C20, C22, CR11, CR13 or R5
①	TP90	95 ± 19Vdc	0.12V	A4C6, C12, C13, CR15, CR20, or R8
TP93	①	95 ± 19Vdc	0.25V	A4C9, C11, C14, CR14, CR21 or R9
①	TP91	75 ± 7.5Vdc	0.6V	A4C6, C15, C18, CR16, CR19 or R6
TP92	①	75 ± 7.5Vdc	0.6V	A4C7, C16, C17, CR17, CR18 or R7
NOTE: Test points 94 and 95 are on A7.				
②	TP94	15 ± 0.2V	0.0015V	A7C25, Q26, Q27, VR5 or CR24
TP95	②	15 ± 0.2V	0.0015V	A7C24, Q28, Q29, CR6 or CR25

Table 5-3. Overall Troubleshooting

SYMPTOM	PROBABLE CAUSE
Zero or Low Output Voltage	<ul style="list-style-type: none"> a. Fuse blown. Check output power transistors. b. Defective meter. c. Board(s) loosely connected. d. A4Q1 open or A4K1 defective. A4CR7 shorted. e. Short circuit load. f. Interconnect board A5 open.

Table 5-3. Overall Troubleshooting (Continued)

SYMPTOM	PROBABLE CAUSE
Zero or Low Output Voltage (Continued)	<ul style="list-style-type: none"> a. Input connector P1 loosely connected b. Defective board or unit in latch (paragraph 5-46)
Unable to program output voltage or actual output does not coincide with programmed input	<ul style="list-style-type: none"> a. Meter circuit defective. b. Flag or gate pulse not generated (paragraph 5-37). c. Voltage bits out of calibration (paragraph 5-71). d. Defective board (paragraph 5-46).
Able to program only a few voltages of each polarity	<ul style="list-style-type: none"> a. Defective board (paragraph 5-46).
Able to program at least some negative output voltages within the rating of the supply but no positive output voltages	<ul style="list-style-type: none"> a. Sign bit circuit defective (paragraph 5-47).
Able to program at least some positive output voltages within the rating of the supply but no negative output voltages	<ul style="list-style-type: none"> a. Sign bit circuit defective (paragraph 5-47).
Able to program all but a few voltages of each polarity	<ul style="list-style-type: none"> a. Voltage Processing circuits defective (paragraph 5-47).
Programmable current latch defective or unable to get unit out of current latch	<ul style="list-style-type: none"> a. A6 or A7 boards defective (paragraph 5-46).
Unit locked up (high positive output) or locked-down (high negative output)	<ul style="list-style-type: none"> a. Defective A7 board (paragraph 5-64)
Flag or gate pulse not being generated	<ul style="list-style-type: none"> a. Defective A7 board (paragraph 5-47).
Unable to program voltage range	<ul style="list-style-type: none"> a. A7K1 defective b. Defective A6 board (paragraph 5-55).
Programmable current latch defective (unable to program some values)	<ul style="list-style-type: none"> a. Defective A6 board (paragraph 5-55).
Unable to get unit out of current latch or unable to get unit into current latch	<ul style="list-style-type: none"> a. Defective A6 or A7 boards (paragraph 5-46).

Table 5-3. Overall Troubleshooting (Continued)

SYMPTOM	PROBABLE CAUSE
Poor Line Regulation	a. Power supplies faulty. b. Marginal photo-isolators on board A1 (paragraph 5-53).
Poor Load Regulation	a. Power Supplies faulty. b. Excessive voltage drop in sensing loads.

5-46 Board Isolation Procedure. The board isolation procedure describes how to isolate trouble to the power amplifier board A7, the control board A6, or to the voltage processing boards A1, A2, and A3. When the defective board(s) is located, further isolation is necessary before the trouble can be traced down to a particular circuit or component. Paragraphs 5-47 through 5-58 describe troubleshooting procedures on individual boards which isolate the trouble down to a component or circuit. The board isolation procedure assumes that an output voltage problem (zero or incorrect output voltage) exists. To isolate troubles to the defective board(s) proceed as follows:

1. Remove boards A2 and A3 from the DVS.
2. Remove load and connect voltmeter across HI and LO output terminals.
3. Connect Pocket Programmer to the data input connector and set its switches as follows:
 - a. Set the INPUT LEVEL REF switch to DATA COM.
 - b. Set the SOURCE SELECT switch to EXT.
 - c. Set the MP/DCPS switch to DCPS.
 - d. Set the RANGE switch to X10.
 - e. The voltage magnitude bit switches (0, 5 through 8192), OUTPUT SIGN switch and I LATCH switches (L24, L22, and L23) may be left on either position (up or down) at this point in the procedure.
4. Turn on power apply a GATE pulse to the DVS and measure output voltage. Output should be 0 volts \pm 10mV. If output is not correct, troubleshoot the power amplifier board A7 (paragraph 5-64).
5. Connect a negative dc voltage ($-V_x$) between the ANLG IN and LO S terminals on the rear of the DVS. Connect (-) polarity to the ANLG IN terminal and (+) polarity to the LO S terminal as shown in Figure 5-7A. Note that the power amplifier in the DVS inverts this voltage and amplifies it by 1 in the X1 range and by 10 in the X10 range. The magnitude of the V_x input (maximum of 5V in

the X10 range) depends upon the trouble encountered. For example, if a high range output voltage cannot be programmed, apply a high range voltage to the analog input.

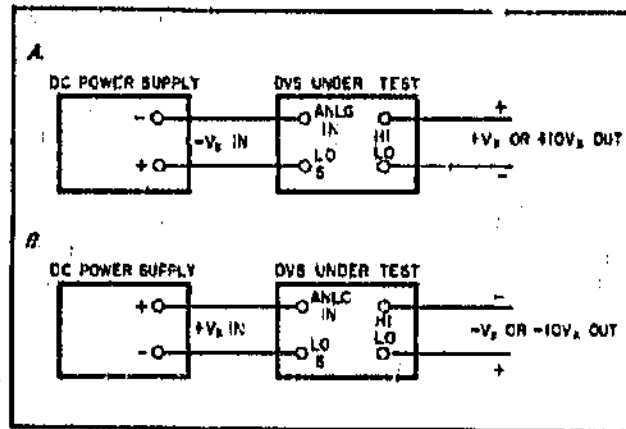


Figure 5-7. DVS Analog Input Connections

6. Measure the output voltage. Output should be $\pm 10V_x \pm 0.2\%$. If output is $+10V_x \pm 0.2\%$, proceed to step 7. If output is $+V_x \pm 0.2\%$, the problem is in the range circuits on board A6 (paragraph 5-61) or the range relay A7K1 is defective. If the output is not $+10V_x \pm 0.2\%$ or $+V_x \pm 0.2\%$ troubleshoot the A7 board (paragraph 5-64).

7. Connect a positive dc voltage ($+V_x$) between the ANLG IN and LO S terminals as shown in Figure 5-7B. Set the RANGE switch on the Programmer to X1.

8. Measure the output voltage. Output should be $-V_x \pm 0.2\%$. If output is $-V_x \pm 0.2\%$, proceed to step 9. If output is $-10V_x \pm 0.2\%$, the problem is in the range circuits on board A6 (paragraph 5-61) or the range relay A7K1 is defective. If output is not $-V_x \pm 0.2\%$ or $-10V_x \pm 0.2\%$, troubleshoot the A7 board (paragraph 5-64).

9. Turn off DVS and make the following test setup changes:

- a. Remove the A7 board and install it with the extender board (side A, position D) in the A7 slot.
- b. Connect a 50 Ω load in parallel with the voltmeter across the HI and LO output terminals.
- c. Connect $-V_x$ to ANLG IN as shown in Figure 5-7A.

10. Turn on DVS and measure output. Output should be less than 1 volt because the DVS should be in the latch condition. If output is less than 1V, proceed to step 12. If output is $+V_x$ (DVS is not in latch condition), proceed to step 11.

11. Measure the voltage across A7R92 (connect positive probe to base of A7Q25 and negative probe to $\textcircled{2}$) see Figure 7-2, sheet 3. If meter reads approximately +0.7 volts (one V_{BE} drop), the A7 latch circuit is defective (see paragraph 5-67). If meter reads less than one V_{BE} voltage drop, the A6 latch circuit is defective (see paragraph 5-58) provided A7Q25 is not shorted from base to emitter.

12. Apply a GATE pulse via the Pocket Programmer (14533B) to get the DVS out of the latch condition.

13. Measure output voltage. Output voltage should be $+V_x$. If output is not $+V_x$, the A7 latch circuits are defective (see paragraph 5-67).

14. Connect $+V_x$ to ANLG IN as shown in Figure 5-7B and measure the output voltage. Output voltage should be $-V_x$. If not $-V_x$, the A7 latch circuits are defective (see paragraph 5-67).

15. Turn off the DVS and make the following test setup changes:

- a. Remove A7/extender board and return A7 to its slot.
- b. Insert the A2 board in its slot.
- c. Install A3 with extender board (side A, positive A) in the A3 slot.
- d. Remove the input from the ANLG IN and LO S terminals.
- e. On the Pocket Programmer, set all voltage magnitude bits to the on position.

16. On the A3 board, check voltages at TP52 (+16.384V $\pm 1\%$), TP53 (-16.384V $\pm 1\%$), and TP55 (21.5V $\pm 5\%$). All voltages should be within tolerance. If not, check the associated regulating circuit on the A3 board.

17. On the Pocket Programmer, set all voltage magnitude bits to the off position.

18. Check voltages at TP52, TP53, and TP55 on the A3 board. Voltage changes should be as indicated below. If not, check associated regulating circuit on the A3 board. If voltages check out, perform the troubleshooting procedures for the voltage processing circuits (paragraph 5-47).

TP	ΔV
TP52	$\pm 0.5mV$
TP53	$\pm 0.5mV$
TP55	$\pm 100mV$

5-47 VOLTAGE PROCESSING CIRCUIT TROUBLESHOOTING

5-48 The following paragraphs should be helpful in locating any circuit failures on the A1, A2, or A3 boards. Paragraph 5-49 traces the voltage magnitude and sign bits through the three boards to locate data bit problems on the A1 and A2 boards or to isolate them to the A3 board. Paragraph 5-50 troubleshoots the A3 board in detail. Paragraph 5-51 troubleshoots the gate, flag, and storage strobe circuits on the A1 and A2 boards. Refer to Figure 7-2, sheet 1 when troubleshooting circuit failures on the A1, A2, or A3 circuit boards. Use the extender board (paragraph 5-4) to gain access to circuit board test points.

NOTE

For convenience, it is best to leave the A6 and A7 boards out of the unit while troubleshooting the voltage processing circuits.

5-49 A1 and A2 Board Troubleshooting. Assuming that the sign bit or one or more voltage magnitude bits do not affect the output of the D/A converter, the following steps will isolate the problem to a particular board.

a. Observe the voltage between common $\textcircled{3}$ and A1TP10 of the bit to be tested. Toggle the input bit. There should be two logic levels at TP10. If there are not, look for a problem in the programming source or its connector, in the A1 board connector, or in the input bias circuit.

b. Toggle the input bit while observing the voltage between common $\textcircled{4}$ and A1TP13. There should be two logic levels. If the voltage is zero, check for an open A1 or A2 board connector or an open resistor in A227 or A228. If the voltage remains near zero or about 5 volts, the problem is on the A1 board, either in the input bias circuit or the isolator circuit. For isolator circuit troubleshooting instructions, see paragraph 5-53.

c. To check for problems on the A2 board, switch to STORAGE DISABLE and check the voltage between A2TP97 (or A2TP51, for the sign bit) and common $\textcircled{4}$ while toggling the input bit. If there are not two logic levels, the storage IC is probably defective. But first check for a high logic level at A2TP9. If this level is low a storage disable circuit fault is indicated; see paragraph 5-51. If TP97 does exhibit two logic levels, the fault has been isolated to the A3 board. See paragraph 5-50 for A3 board troubleshooting instructions.

5-50 A3 Board Troubleshooting. If a problem has been isolated to the A3 board, first check the three voltages that are regulated on that board. (All

voltage measurements on A3 are referenced to common (2).

a. Measure the outputs of the +21.5-volt, +16.384-volt, and -16.384-volt supplies at test points TP55, TP52, and TP53. If any of these voltages is not within tolerance, check the regulating circuit for that particular voltage. Note that a shorted switching transistor (Q2 or Q3) can affect the +16.384-volt reference. If one of these two switching transistors is shorted, either a high or low, input respectively to Q1 will load down the positive reference through Q2 and Q3 in series. A Q2 or Q3 short can be detected by monitoring the +16.384-volt regulator output while toggling each input bit.

b. Program all voltage magnitude input bits to produce low inputs at the base of Q1 and measure the voltage at TP54 of each bit. The voltage at TP54 should be between zero and +8mV. If any bit is higher than +8mV, check Q1 and Q3.

c. Now program for high inputs at the base of A1 and again measure the voltage at TP54 of each bit. All bits should be within 8mV of TP52 voltage. If any are lower than this voltage, check Q1 and Q2.

d. If all ladder network switching circuits are now operating properly, the voltage at TP54 of each bit can be alternated between the values specified above by toggling the input bit.

e. If the sign bit tested good at A2TP51 but does not affect the output of the A3 board, check transistors A3Q13 and A3Q14 in the polarity offset switch. A failure either here or in the -16.384 volt reference supply is likely.

NOTE

If any repair or adjustment of the power amplifier is required, that will have to be completed before the D/A converter can be performance tested or calibrated.

f. If steps (a) through (e) above confirm the proper operation of the A3 board voltage regulators, bit switches, and polarity offset switch, the only possible trouble area remaining on the D/A board is the resistive ladder network. An out-of-tolerance resistor in the ladder network will be detected only by attempting to calibrate the unit. Perform the calibration procedure of paragraph 5-71. If one or more bits cannot be calibrated, their identity should pinpoint the faulty resistor(s). If the -16.384-volt reference supply and polarity offset switch are operating but the polarity offset current adjustment (A3R18) will not bring the DVS output voltage to zero in step (p) of paragraph 5-72, A3R19 or A3Q14 is likely to be at fault.

5-51 Gate, Flag, and Storage Strobe Troubleshooting. The simplest method of troubleshooting these circuits is to trace signals with an oscilloscope while providing a gate input from a pulse generator. The pulse generator may be connected between common (3) and either the GATE input jack on the Pocket Programmer or A1TP1. The required pulse amplitude and polarity will depend on the instrument being tested. See the appropriate Option Appendix or the Instrument Modification sheet supplied with the instrument for this information. The minimum pulse width is 5 microseconds; a repetition rate of 400Hz or less is suitable. In the STORAGE mode, check waveforms at test points in the following order: TP2, 3, 4, 6, 7, 40, 31, 41, 42, 16, 43, 8, 9, and 28. In the STORAGE DISABLE mode, check voltages at TP9 and TP28. TP9 should be $\geq 2.4V$, TP28 should be $\leq 0.6V$ referenced to (4).

NOTE

When tracing signals at each test point, make certain to connect oscilloscope to proper common reference point, either common (3) or common (4).

CAUTION

(4) common is -26 volts off ground (2).

5-52 If the signal is lost at TP4, or TP40, one of the delay multivibrators (A1Z3 or A1Z4) or its power supply is at fault. The +5V, and +5V₂ supply voltages for A1Z3 and A1Z4 are derived from the +12V source supply and components on board A1 (see Figure 7-2, sheet 4). If the gate pulse isolator or flag isolator is at fault, see paragraph 5-53 for isolator troubleshooting instructions.

5-53 PHOTO-ISOLATOR CIRCUIT TROUBLESHOOTING

5-54 Once a trouble has been localized to a particular photo-isolator circuit, following the steps of Table 5-4 or 5-5 will troubleshoot its three main semiconductor components without requiring the removal of any parts from the board. Although some of the photo-isolator circuits in the DVS differ in the means of input drive and some are followed by one or more stages of amplification or inversion, all are generally similar to the circuit, first make sure that all of the two or three dc supplies to the circuit are present. When this has been established, toggle the input bit and observe the collector voltage of the transistor that immediately follows the photo-isolator package (Q2 of Figure 5-8). The

choice of which table should be used depends on the results of that test. If the collector of that transistor remains at a logical high when the input bit is toggled, begin at step (1) of Table 5-4. If that collector remains at a logical low, begin at step (1) of Table 5-5.

NOTE

Marginal photo-isolators in the input circuits on the A1 and A6 boards can cause erroneous output voltage readings and current latch values when operating in the low or high limits of ac input voltage (see paragraph 5-16). This can be detected by programming all photo-isolators to turn-on then turn-on power to the DVS (at low line) and check the output of each storage flip-flop. Thus, the marginal photo-isolation can be detected and replaced.

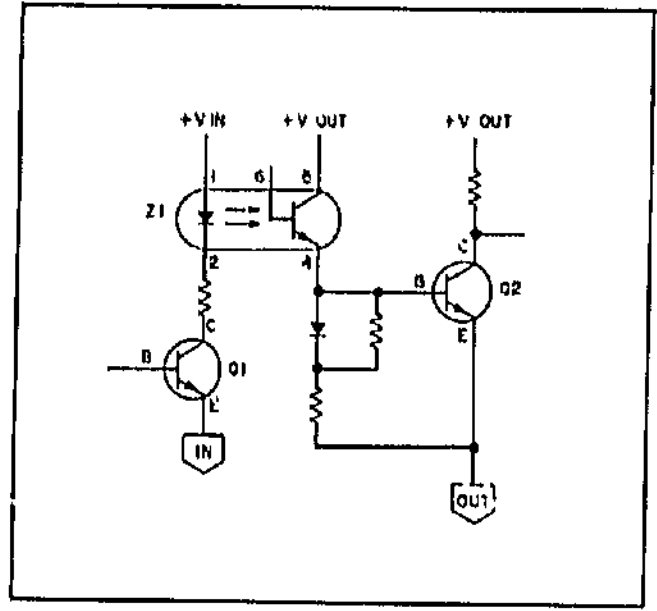


Figure 5-8. Representative Isolator Circuit

Table 5-4. Photo-Isolator Troubleshooting -- Output Remains High

NOTE: Refer to Figure 5-8 for component reference designations used in this table.

STEP	ACTION	RESPONSE	PROBABLE CAUSE
1.	Observe voltage between Q2 collector and OUT common. Shunt Z1 pin 4 to pin 5 momentarily with 1K Ω resistor.	<ul style="list-style-type: none"> a. Two logic levels present. b. Q2 collector still remain high. 	<ul style="list-style-type: none"> a. Proceed to Step 2. b. Q2 opened. Replace Q2 and retest entire isolator stage. If output now remains low, proceed to Table 5-5.
2.	Observe voltage between Q1 collector and IN common. Toggle input bit.	<ul style="list-style-type: none"> a. Two logic levels present. b. High logic level only. c. Zero or low logic level only. 	<ul style="list-style-type: none"> a. Z1 failure. b. Proceed to Step 3. c. Proceed to Step 4.
3.	Observe voltage between Q2 collector and OUT common. Short Q1 collector to emitter.	<ul style="list-style-type: none"> a. Q2 collector goes low. b. Q2 collector remains high. 	<ul style="list-style-type: none"> a. Q1 opened. b. Q1 opened and Z1 failure.
4.	Connect short from Z1 pin 1 to pin 2. Observe voltage between Q1 collector and IN common. Toggle input bit.	<ul style="list-style-type: none"> a. Two logic levels present. b. Zero or low logic level only. 	<ul style="list-style-type: none"> a. Z1 failure. b. Q1 shorted and Z1 failure.

NOTE: If failure persists, check for bridged or open P.C. conductors.

Table 5-5. Photo-Isolator Troubleshooting — Output Remains Low

NOTE: Refer to Figure 5-8 for component reference designations used in this table.

STEP	ACTION	RESPONSE	PROBABLE CAUSE
1.	Observe voltage between Q2 collector and OU1 common. Short Q2 base to emitter momentarily.	a. Two logic levels present. b. Q2 collector still remains low or zero.	a. Proceed to Step 2, b. Q2 shorted. Replace Q2 and retest entire isolator stage. If output now remains high, proceed to Table 5-4.
2.	Observe voltage between Q2 collector and OUT common. Short Z1 pin 4 to pin 6 momentarily.	a. Two logic levels present. b. Q2 collector still remains low or zero. c. High logic level only.	a. Q1 shorted. Replace Q1 and proceed to Step 3. b. Z1 shorted. Replace Z1 and proceed to Step 3. c. Proceed to Table 5-4.
3.	Observe voltage between Q2 collector and OUT common. Toggle input bit.	a. Two logic levels present. b. Q2 collector remains low or zero. c. High logic level only.	a. Repair completed b. Q1 shorted. Replace Q1 and repeat Step 3. c. Proceed to Table 5-4.
NOTE: If failure persists check for bridged or open P.C. conductors.			

5-55 A6 CONTROL BOARD TROUBLESHOOTING

5-56 Since the A6 Board handles many different signals, the troubleshooting for this board has been broken down according to input and output signals. Table 5-6 lists the possible trouble symptoms and directs the reader to the correct paragraph or table for further isolation. Before proceeding to Table 5-6 for the paragraph or table applicable to the trouble present, the following procedure should be used to determine if the trouble lies within the input circuits:

a. Remove the A6 board and install it in the extender board. Install the extender board/A6 combination in the A6 board slot.

b. Connect a voltmeter or logic probe between (2) common and TP75 of the bit to be tested.

c. Set the STORAGE/DISABLE switch to DIS-ABLE

d. Toggle bit to be tested. If two logic levels can be obtained proceed to Table 5-6. If only one logic level is present, proceed to Paragraphs 5-57, 5-58, and 5-59.

5-57 Current Latch Data Input Circuits Troubleshooting. The following procedure describes the process by which troubles in the current latch data input circuits may be isolated. The process consists of a series of fast checks of the input circuits up to and including the storage flip-flops A6Z2.

5-58 To isolate troubles in the input circuits, proceed as follows:

1. Connect the common lead of an oscilloscope or logic probe to (3) common.

2. Connect the other lead to TP64 of each of the current latch input bits, and look for the presence of two logic levels as the switch for that bit is toggled. If only one logic level is found at TP64 for any of the bits, check the programming source for defect.

3. Disconnect the leads at TP64 and (3) and connect them to TP74 of each bit and (2). Check for the two logic levels as described in Step 2. If only one logic level is present for any of the bits, check the associated pull-up resistor (A6Z1) and photo-isolator circuit (paragraph 5-53).

4. Disconnect the lead of the monitoring device of TP74 and connect it to TP75 of each bit. Check for the presence of two logic levels as described in Step 2. If two logic levels are not present for any of the bits, A6Z1 may be defective. See Paragraph 5-59 and 5-60.

5-59 Storage Gate Pulse Troubleshooting. First determine if the A2 STORAGE DISABLE switch and associated circuits are working by monitoring TP30 (Ref ②) while switching from STORAGE to STORAGE DISABLE. If two logic levels are present these circuits are working on a "static" level, otherwise check the Interconnect Board (A5) and Logic Board (A2) and A6Q4, Q5, Q6 as follows. With A2S1 in the STORAGE position, apply a pulse train to the GATE input terminal J1 pin 32. Check for the presence of a pulse by connecting an oscilloscope or logic probe to ② common and TP's 28, 69, 70 and 30 in order. Note that TP28 is approximate -26 volts with respect to ② and ② is connected to the Low Sense terminal on the rear barrier block. Low Sense is typically connected to chassis ground (⊕). If a point is reached at which the pulse is not present, it may be assumed that the transistor (or related components) just before this point is defective. If the gate pulse is traced through to TP30, it is likely that A6Z2 is defective and must be replaced. Before replacing A6Z2 ensure that +4.99V supply voltage is present at A6Z2, pin 5. If not, check the +4.99V supply components (see Figure 7-2, sheet 4).

5-60 Voltage Range Troubleshooting. To troubleshoot the voltage range circuits, the following procedure is recommended:

1. Connect the common lead of oscilloscope or logic probe to ③ common.
2. Connect the other lead of TP65 and check, by toggling the appropriate switch, for the presence of two logic levels. If only one logic level is present, check the interconnect board for continuity and ensure that the programming device is connected properly.
3. Disconnect the leads of the monitoring device at TP65 and ③ and connect to TP76 and ② respectively observing the presence of two logic levels as described in Step 2. If only one logic level is present, check the A6A4 photo-isolator circuit (paragraph 5-53). Also check network A6Z1.
4. Disconnect the lead of the monitoring device from TP76 and connect to TP73 checking for the presence of two logic levels as in Step 2. If only one logic level is present, it is likely that A6Z1 or A6Z2 is defective.
5. Disconnect the lead of the monitoring device from TP73 and connect to TP77 observing the presence of two logic levels as in Step 2. If only one logic level is present, check A6Q25 for an open or short circuit. If 2 logic levels are present, the

trouble lies within the A7 board (A7K1 or A7K2).

5-61 Negative Programmable Output Current Latch Defective. If the unit will current latch for positive output currents, but not for negative output currents; or, if the unit is in current latch for all values of negative output current and works correctly for positive output current latch settings, the cause of trouble must be in a circuit which handles the flow of the negative current latch signal. There are two stages which handle only the negative output current latch signal, A6Z4 and A6CR1.

5-62 Positive Programmable Output Current Latch Defective. If the unit will current latch for negative output currents, but not for positive output currents; or, if the unit is in current latch for all values of positive output current and works correctly for negative output current latch settings, the cause of trouble must be in a circuit which handles the flow of the positive current latch signal only. There are three stages which handle only the positive output current latch signals, A6Z4, A6CR2 and the Negative Reference Inverter (A6Z3, A6Q23, and associated components). Check A6Z4 and A6CR2 first. If these two components are operative, the trouble probably lies in the negative reference inverter. Check A6Z4 and A6CR2 for open or shorted junctions.

5-63 Current Latch Decoder Troubleshooting. To troubleshoot the current latch decoder circuit, the following procedure is recommended:

1. Connect voltmeter positive lead to the NEG REF (TP100) on board A6 and the common lead to TP99. Turn unit on and GATE unit. Set the STORAGE DISABLE switch on A2 to DISABLE.
2. Set the current latch to each value and check that the associated voltage reading is as indicated below:

Current Latch Value (mA)	Voltage Reading (mV) $\pm 10\%$, $\pm 17mV$
20	+25
50	+62.5
70	+67.5
100	+125
200	+250
500	+625
700	+875
1000	+1250

3. If all voltages are incorrect, check current latch decoder stage A6Q1 and the negative reference resistor A6R30. If any voltage reading or combination of voltage readings are incorrect, refer to Table 5-7. Also, check the current latch calibration (paragraph 5-79).

4. Connect voltmeter positive lead to the

POS REF (TP101) on board A6 and the common lead to TP99.

5. Set the current latch to a value of 1000mA and check that voltmeter reads $-1.250V \pm 10\%$. If

reading is incorrect, check the negative reference inverter (A6Q23, Z3) and the positive reference resistor A6R37. Also, check the current latch calibration (paragraph 5-79).

Table 5-6. A6 Troubleshooting Guide

SYMPTOM	A6 TROUBLESHOOTING SECTION
Unit always in current latch	Proceed to Table 5-8
Unable to current latch at turn-on	Proceed to Table 5-9
Unable to current latch at latch setting	Proceed to Table 5-10
Current latch operating properly but latch status is always in the same state (on or off).	Proceed to Table 5-11
Current latch operating properly but overload status is always in the same state (on or off).	Proceed to Table 5-12
Storage gate pulse defective	Proceed to paragraph 5-59
Vc range defective	Proceed to paragraph 5-60
Positive output current latch defective	Proceed to paragraph 5-62
Negative output current latch defective	Proceed to paragraph 5-61
Flag is not generated for both range switching and overload conditions *	Check the overload/range flag isolator (A6Q31, Q32, Q33, and Z5).
Flag is not generated when range is switched but is generated for an overload condition *	Check 2 millisecond delay circ (A6CR12, CR13, CR16, Q26, Q27, Q28).
Flag is not generated for an overload condition but is generated when range is switched *	Check overload flag generator (A6CR14, CR15, Q29, Q30).

* Overload Flag is disabled for J20 Option

Table 5-7. Current Latch Decoder Troubleshooting Guide

SYMPTOM	PROBABLE CAUSE
Current latch defective for all values.	A6Q1, Q8-Q15, or Z2 defective.
Current latch defective only for the following values: 20, 70, 200, 700mA	A6Q3 opened, Q13 or Q15 shorted
Current latch defective only for the following values: 50, 100, 500, 1000mA	A6Q3 shorted, Q13 or Q15 opened

Table 5-7. Current Latch Decoder Troubleshooting Guide (Continued)

SYMPTOM	PROBABLE CAUSE
Current latch defective only for the following values: 20, 50, 200, 500mA	A6Q2 opened, Q12 or Q14 shorted
Current latch defective only for the following values: 70, 100, 700, 1000mA	A6Q2 shorted, Q12 or Q14 opened
Current latch works for 20 or 200mA but does not work for both,	A6Q8 defective
Current latch works for 50 or 500mA but does not work for both,	A6Q10 defective
Current latch works for 70 or 700mA but does not work for both,	A6Q9 defective
Current latch works for 100 or 1000mA but does not work for both,	A6Q8, Q9, Q10 defective

Table 5-8. Unit Always in Current Latch

NOTE: Logic level "1" equals a positive voltage, logic level "0" equals approximately 0V.


STEP	ACTION	RESPONSE	CONCLUSION
1	Connect voltmeter common to  . Remove load and ensure that output terminals are not shorted. Turn unit on and Gate unit. Check TP21.	a. Logic level "0" b. Logic level "1"	a. Current latch circuit on A6 board operating properly, check current latch circuit on A7 board (paragraph 5-67). b. Ensure that input plug P1 is connected. Proceed to Step 2.
2	Check TP20	a. Voltage magnitude equals approximately -5V. b. Logic level "1"	a. Buffer stage A6Q21 probably working, go to Step 3. b. Check A6Q21 for open.
3	Check TP14	a. Logic level "1" b. Logic level "0"	a. Reset amplifier working, check A6Q20 for open. If A6Q20 not open, go to Step 4. b. Check Reset Amplifier A6Q24 for short.

Table 5-8. Unit Always in Current Latch (Continued)



STEP	ACTION	RESPONSE	CONCLUSION
4	Check TP98	a. Logic level "0" b. Logic level "1"	a. Relay MK1 probably working, go to Step 5. b. Relay MK1 defective causing false setting of latching flip-flop A6Q19, Q20.
5	Connect voltmeter common to  , Check TP19	a. Logic level "1" b. Logic level "0"	a. Latching flip-flop probably working, go to Step 6. b. Check A6Q19 for short.
6	Check TP18	a. Logic level "1" b. Logic level "0"	a. Level detector A6Q17 and A6Q18 probably good, go to Step 7. b. Check A6Q17 for short and A6Q18 for open.
7	Check TP17	a. Voltage magnitude $\pm 0.5V$ b. Logic level "1"	a. Variable delay A6Q16 probably operating, go to Step 8. b. Check A6Q16 for open.
8	Connect voltmeter common to TP99 and check TP15	a. Voltage magnitude is less than 20mV. b. Voltage magnitude is more than 20mV	a. Current sampling circuit operating properly, go to Step 9. b. Check current sampling resistor and interconnect wires.
9	Connect voltmeter common to  , Check TP36	a. Logic level "1" b. Voltage magnitude equals approximately -13V.	a. Negative current comparator is operating properly, go to Step 10. b. Check current latch decoder (see para. 5-63). If current latch decoder circuits are operating properly check the negative current comparator circuit (A6Z4, R39, R33, R31).
10	Check TP36	a. Logic level "1"	a. Positive current comparator is operating properly, check CIR gate (A6CR1, CR2) for shorts.

Table 5-8. Unit Always in Current Latch (Continued)

STEP	ACTION	RESPONSE	CONCLUSION
10	Check TP36 (Continued)	b. Voltage magnitude equals approximately -13V.	b. Check current latch decoder (see para. 5-63). If current latch decoder circuits are operating properly, check the positive current comparator (A624, R32, R34, R43) and the negative reference inverter (A6Q3, 23).

Table 5-9. Unable to Current Latch at Turn-On

NOTE: Positive voltage equals logic level "1"; logic level "0" equals approximately 0V.

STEP	ACTION	RESPONSE	CONCLUSION
1	Turn unit off. Measure impedance between 2 and TP98.	a. Impedance $\geq 5K\Omega$ b. Impedance $< 5K\Omega$	a. Relay A4K1 probably working, go to Step 2. b. Relay A4K1 defective causing false resetting of latching flip-flop.
2	Connect voltmeter common to 2 . Turn unit on (Do not GATE). Check TP21	a. Logic level "0" b. Logic level "1"	a. No latch go to Step 3. b. Latch circuit on A6 board is operating, check latch circuit on A7 board (paragraph 5-67).
3	Check TP26	a. Logic level "1" b. Voltage magnitude equals approximately -5V.	a. Buffer stage A6Q21 probably working, go to Step 4. b. Buffer stage A6Q21 not working, check A6Q21 for short.
4	Check TP14	a. Logic level "0" b. Logic level "1"	a. A6Q20 probably working. Reset amplifier may be defective. Check A6 Q24 for short and A6Q22 for open. If reset amplifier is working properly, go to Step 5. b. Check A6Q20 for short.
5	With an oscilloscope, observe operation of A4K1 (TP98) and turn-on of power (TP88). Both referenced to 2 .	a. TP98 goes low $\approx 200ms$ after power on. b. TP98 goes low $< 200ms$ after power on.	a. Delay for A4K1 working; check complete. b. Check -12V delayed circuit especially M4C10, CR22 for shorts (see Figure 7-2, sheet 4).

Table 5-10. Unable to Current Latch at Latch Settings

NOTE: Logic level "1" equals a positive voltage, logic level "0" equals approximately 0V.


STEP	ACTION	RESPONSE	CONCLUSION
1	Turn unit off. Measure impedance from TP18 to 2 (connect positive meter lead to TP18)	a. Impedance $>1K\Omega$ b. Impedance $<1K\Omega$	a. Go to Step 2 b. Or terminals on barrier strip are shorted or electrolytic capacitor used is connected with reverse polarity.
2	Short the output terminals and turn unit on. Program the current latch and voltage magnitude values in question then Gate unit.	a. Output current $<20mA$ b. Output current $\geq 100\%$ of rated output	a. Check completed. Problem caused by improper setting of current latch value or current latch not calibrated (see paragraph 5-79) b. Latch circuits not working, go to Step 3.
3	Connect meter common to 2 and check TP21	a. Logic level "1" b. Logic level "0"	a. Current latch circuits on A6 board operating properly, check current latch circuit on A7 board (see paragraph 5-67). b. A6 latch circuits not working, go to Step 4.
4	Check TP20	a. Logic level "1" b. Voltage magnitude equals approximately -5V	a. Buffer stage A6Q21 probably working, go to Step 5. b. Check Buffer Stage A6Q21 for short.
5	Check TP19	a. Logic level "0" b. Logic level "1"	a. Latching flip-flop probably working, go to Step 6. b. Check latching flip-flop transistor A6Q20 for short and A6C5 for open.
6	Check TP18	a. Logic level "0" b. Logic level "1"	a. Level detector (A6Q17, Q18) probably working, go to Step 7. b. Level detector not working, Check A6Q17 for open and A6Q18 for short.
7	Check TP17	a. Logic level "1" b. Voltage magnitude $<+0.5V$	a. Variable delay A6Q16 probably working, go to Step 8. b. Check A6Q16 for short

Table 5-10. Unable to Current Latch at Latch Settings (Continued)

NOTE: Logic level "1" equals a positive voltage, logic level "0" equals approximately 0V.

STEP	ACTION	RESPONSE	CONCLUSION
6	Check TP35 and TP36	a. Both logic level "1" b. Either equals approximately -13V. c. Both equal approximately -13V.	a. Go to Step 9 b. CR1, CR2, or VR2 open c. CR1 and CR2 open, go to Step 9.
9	Connect voltmeter common to TP99 and check TP15	a. Voltage magnitude equals 1.25V $\pm 10\%$ b. Voltage magnitude does not equal 1.25V $\pm 10\%$	a. Current sampling circuit operating properly, go to Step 10. b. Check current sampling resistor and interconnections.
10	Set current latch to 1000mA. With voltmeter common connected to TP99, check the NEG REF (TP100).	a. Voltage equals +1.25V $\pm 10\%$ b. Voltage does not equal +1.25V $\pm 10\%$	a. Current latch decoder operating properly. Check the negative current comparator (A624, R31, R33, R33). Proceed to Step 11. b. Check current latch decoder (see paragraph 5-63).
11	Check POS REF (TP101) with meter common connected to TP99	a. Voltage equals -1.25V $\pm 10\%$ b. Voltage does not equal -1.25V $\pm 10\%$	a. Negative reference inverter operating properly. Check positive current comparator (A624, R32, R34, and R43). b. Check negative reference inverter (A623, Q23).

Table 5-11. Latch Status Troubleshooting

STEP	ACTION	RESPONSE	CONCLUSION
1	Check the operation of A6A5Q4 by first shorting A6A5Q3 emitter to base and then emitter to collector. Monitor the output with a voltmeter *connected between TP22 and  common.	a. Only one logic level present b. Two logic levels present	a. A6A5Q4 defective or A6A5Q3 shorted b. Remove short and proceed to Step 2.

*If there is no pull-up resistor (A6A5R8), use an ohmmeter.

Table 5-11. Latch Status Troubleshooting (Continued)

STEP	ACTION	RESPONSE	CONCLUSION
2	Check the operation of A6A5Q3 by shorting A6A5Q2 first emitter to collector and then emitter to base. Monitor the output after each operation as described in Step 1.	a. One logic level present b. Two logic levels present	a. A6A5Q3 defective or A6A5Q2 shorted b. Remove short and check the operation of the latch status photo isolator circuit (see paragraph 5-53).

Table 5-12. Overload Status Troubleshooting

STEP	ACTION	RESPONSE	CONCLUSION
1	If A6A6Q4 is in the circuit (see modifications sheet) test its operation by first shorting A6A6Q3 emitter to base. Monitor the output with a voltmeter * connected between TP25 and ③ common after each operation.	a. Only one logic level present b. Two logic levels present	a. A6A6Q4 defective or A6A6Q3 shorted. b. Remove short and proceed to Step 2.
2	Check the operation of A6A6Q3 by shorting A6A6Q2 first emitter to collector and then emitter to base. Monitor the output after each operation as described in Step 1.	a. One logic level present b. Two logic levels present	a. A6A6Q3 defective or A6A6Q2 shorted. b. Remove short and check the operation of the overload status photo-isolator circuit (see paragraph 5-53).

* If there is no pull-up resistor (A6A6R8), use an ohmmeter.

5-64 A7 POWER AMPLIFIER BOARD TROUBLESHOOTING

5-65 Before attempting to troubleshoot the power amplifier, it is important to classify the kind of trouble present according to the trouble symptoms. Generally, troubles in the A7 board generate two broad categories of symptoms: current latch problems and output voltage problems. For example, if output voltages can be programmed with no load but no current can be drawn when a load is added, the problem is most likely a current latch type. However, if output voltages cannot be programmed without a load, the problem is probably an output voltage type.

5-66 The A7 troubleshooting procedures thus, are divided into two categories according to fault symptoms. The symptoms listed in Table 5-3 can be related to these two categories.

5-67 Current Latch Troubleshooting. Current latch problems on the A7 board can be caused by the current latch circuits themselves (the current latch isolators and switch circuits) or subsequent circuits including the power amplifier, power output, or positive and negative bias circuits. Figure 5-9A presents a procedure for dividing the fault path between either the A7 current latch circuits or the power circuits. If this procedure indicates the fault is in the current latch circuits, Figure

5-9B provides a procedure for localizing the fault to either the current latch isolator or the current latch switch stages. If the procedure of Figure 5-9A indicates that the fault is in the power circuits, the procedure given in Figure 5-10 can be used to localize the fault to the defective stage within the power circuits.

5-68 Output Voltage Troubleshooting. The power amplifier contains four functional circuits (current latch, gross current limit, feedback differential amplifier, and power amplifier) any one of which can cause a failure in output voltage (the failure being that output voltage is locked up or down-full positive or full negative-or zero). The first step in troubleshooting then, is to isolate the trouble to one of the four circuit groups. Once this is accomplished, the defective part of the faulty circuit can be located by more detailed troubleshooting. The following procedures will isolate trouble to one of the four circuit groups by systematically eliminating each circuit from the loop, one at a time, and noting if the output voltage returns to normal after each circuit isolation.

1. Disconnect the load and insure that the output terminals are not short circuited.
2. Program for 0V output.
3. Isolate the gross current limiters from the loop by opening the connection from A7CR28 and CR29 to the base of A7Q6.
4. Program the output voltage 50 volts

above and below 0 volts, in 5 volt steps.

5. If the original trouble still exists, reconnect the gross current limiters and proceed to Step (6). If the original trouble is eliminated, turn the DVS off and troubleshoot the gross current limiters (Table 5-13)

6. Isolate the current latch circuits by opening the connection from diodes A7CR15 and CR20 to the power amplifier.

7. Repeat Step (4).

8. If the original trouble still exists, reconnect the current latch circuits and proceed to Step (9). If the original trouble is eliminated, turn the DVS off and troubleshoot the current latch circuits (Paragraph 5-67).

9. Strap A7Q6 emitter to base. Connect a 25K Ω resistor between emitter and collector of A7Q6. Make sure programming source is connected.

10. Program for 0V output.

11. Read and record output voltage.

12. Remove strap and resistor from A7Q6.

13. If the output reading in Step 11 was 0 ± 10 volts and the unit is locked down, proceed to Table 5-14. If reading in Step 11 was 0 ± 10 volts and the unit is locked up, proceed to Table 5-15. If the reading in Step 11 was greater than 0 ± 10 volts proceed to Step 14.

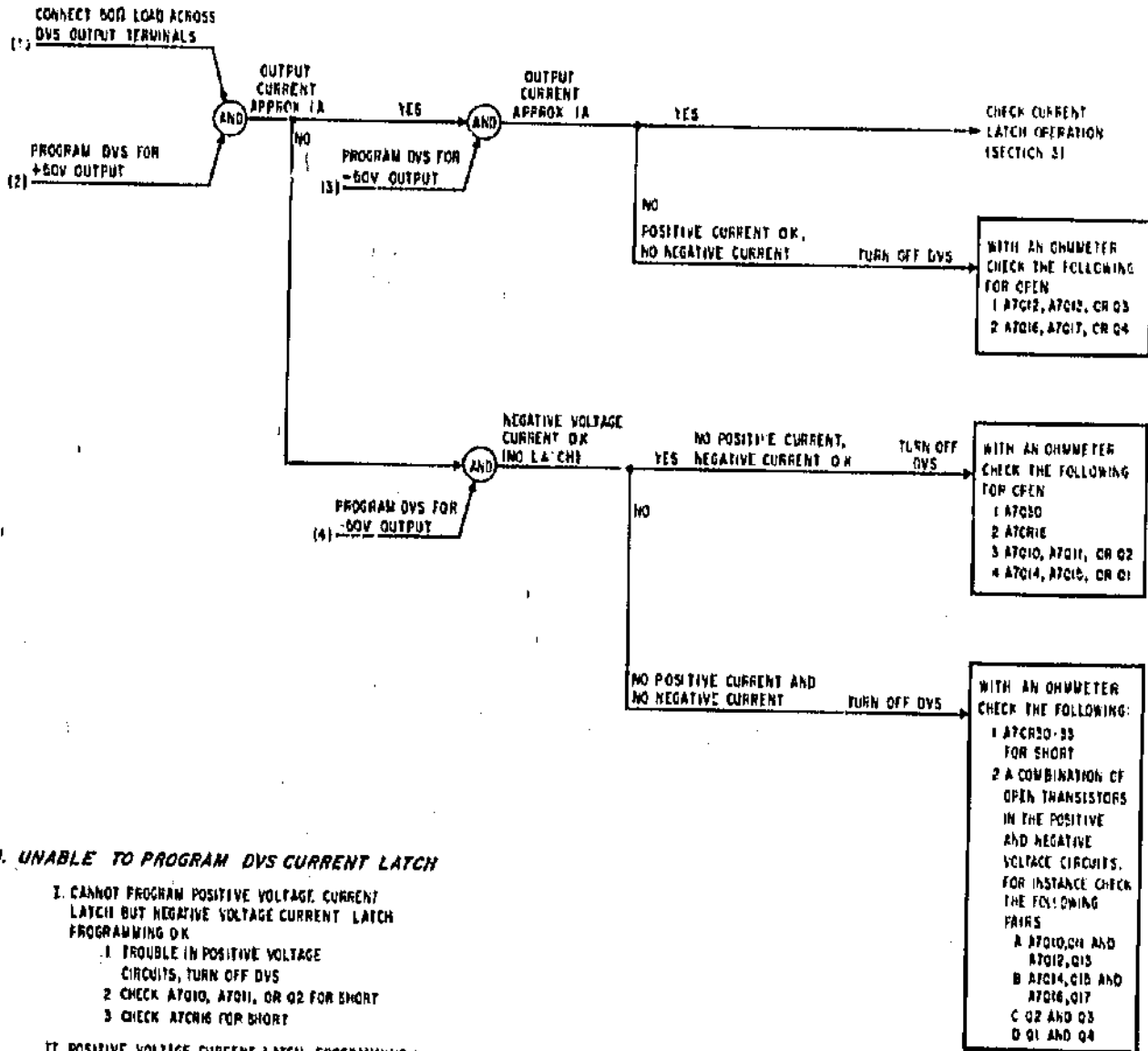
14. Remove input power. Check A7Q7 and Q10 through Q17 for defect.

15. Check power output transistors Q1 through Q4 for defect.

Table 5-13. Gross Current Limiters Troubleshooting

STEP	ACTION	RESPONSE	CONCLUSION
1	With the load removed from the DVS, the output programmed for 0V, and the gross current limiters disconnected from the base of A7Q6, monitor the voltage at the anode of A7CR28.	$-7 \pm 1Vdc$	If the monitored voltage is positive, the negative gross current limiter is locked in the limiting state. Check A7Q18-20
2	Monitor the voltage at the cathode of A7CR29.	$-3 \pm 1Vdc$	If the monitored voltage is excessively negative, the positive gross current limiter is locked in the limiting state. Check A7Q21-23.
3	Again monitor the voltage at the anode A7CR28, but this time connect a 50 Ω , 50 watt load and increase output to a positive level sufficient to draw + 1. 1A.	Monitored voltage switches to $+ 12 \pm 1Vdc$	If the voltage does not switch, the negative gross current limiter is not limiting. Check A7Q18-20.

A. UNABLE TO GET DVS OUT OF CURRENT LATCH



B. UNABLE TO PROGRAM DVS CURRENT LATCH

I. CANNOT PROGRAM POSITIVE VOLTAGE CURRENT LATCH BUT NEGATIVE VOLTAGE CURRENT LATCH PROGRAMMING OK

1. TROUBLE IN POSITIVE VOLTAGE CIRCUITS, TURN OFF DVS
2. CHECK A7C10, A7C11, OR Q2 FOR SHORT
3. CHECK A7C16 FOR SHORT

II POSITIVE VOLTAGE CURRENT LATCH PROGRAMMING OK BUT CANNOT PROGRAM NEGATIVE VOLTAGE CURRENT LATCH

1. TROUBLE IN NEGATIVE VOLTAGE CIRCUIT, TURN OFF DVS
2. CHECK A7C12, A7C13, OR Q3 FOR SHORT
3. CHECK A7C21 OR A7C34 FOR SHORT

Figure 5-10. Localize Current Latch Trouble

Table 5-13. Gross Current Limiters Troubleshooting (Continued)

STEP	ACTION	RESPONSE	CONCLUSION
4	Repeat Step 3, expect monitor the voltage at the cathode of CR29 and increase negative output voltage to draw -1, 1A.	Monitored voltage switches to -12 ± 1Vdc	If the voltage does not switch, the positive gross current limiter is not limiting. Check A7Q21-23

Table 5-14. Feedback Differential Amplifier Troubleshooting, Unit Locked Down (Full Negative)

STEP	ACTION	RESPONSE	CONCLUSION
1	Short A7Q5 emitter to collector	a. Output voltage remains low b. Output voltage increases	a. A7Q5 shorted. b. Remove short and proceed to Step 2.
2	Short A7Q4 emitter to collector	a. Output voltage remains low b. Output voltage increases	a. A7Q5 opened, b. Remove short and proceed to Step 3.
3	Short A7Q3 base to emitter	a. Output voltage remains low b. Output voltage increases	a. A7Q4 opened, A7Q3 shorted. b. Remove short and proceed to Step 4.
4	Short A7Q1B emitter to collector	a. Output voltage remains low b. Output voltage increases	a. A7Q2 defective b. Remove short. Check A7Q1A for short and Q1B for open.

Table 5-15. Feedback Differential Amplifier Troubleshooting, Unit Locked Up (Full Positive)

STEP	ACTION	RESPONSE	CONCLUSION
1	Short A7Q31 base to emitter.	a. Output voltage remains high. b. Output voltage decreases.	a. A7Q31 probably good. Go to Step 2. b. A7Q31 open.
2	Short A7Q5 emitter to base.	a. Output voltage remains high. b. Output voltage decreases.	a. A7Q6 opened, A7Q5 shorted. b. Remove Q5 short and proceed to Step 3.
3	Short A7Q2B emitter to collector and A7Q24 emitter to base.	a. Output voltage remains high. b. Output voltage decreases.	a. A7Q4 shorted, A7Q3 opened, or A7Q2A shorted. b. Remove Q2 shorts and proceed to Step 4.
4	Short A7Q1A emitter to collector, A7Q1B emitter to base.	a. Output voltage remains high. b. Output voltage decreases.	a. A7J2B opened or A7Q1B shorted. b. Remove shorts. Check A7Q1 for defects.

5-69 ADJUSTMENT AND CALIBRATION

5-70 Adjustment and calibration may be required after performance testing, troubleshooting or repair and replacement. Perform only those adjustments that affect the operation of the faulty circuit and no others. All the controls referred to in these adjustments are shown on the component location diagrams in Section VII.

5-71 OUTPUT VOLTAGE ADJUSTMENT

5-72 Before proceeding to the following adjustment procedures, make the following preparations:

1. Strap the following terminals on the rear terminal strip of the DVS:

- a. LO to LO S to GND
 - b. HI to HI S
2. Connect the Pocket Programmer to the data input connector and set its switches as follows:
- a. Set the INPUT LEVEL REF switch to DATA COM.
 - b. Set the MP/DCPS switch to DCPS.
 - c. Set the SOURCE SELECT switch to EXT.
 - d. Set the RANGE switch to X1.
 - e. Set the data and sign bit switches for an output of -0.5mV. (Refer to the appropriate Option Appendix for the correct data and sign bit coding).

- f. Set the LIMIT switches for a 1000mA limit (all three switches down).
3. Set the switch on the A2 board to the STORAGE DISABLE position.
4. Connect a digital voltmeter across the HI S and LO S output terminals.
5. Turn on DVS and momentarily depress GATE switch on Pocket Programmer to deactivate the current latch circuit.
6. With the DVS programmed for an output of -0.5mV, test the voltage processing circuits by individually turning on each bit and observing the relative change in output voltage associated with each bit value. If any voltage bits are not functioning, calibration can not be accomplished (refer to troubleshooting procedures, paragraph 5-37). If all voltage bits are functioning, proceed as follows:

-0.5 MILLIVOLT CALIBRATION

a. Turn DVS off. Remove bottom cover in order to gain access to potentiometer A7R9. Note that if the DVS is installed in a system, both the A3 and A7 boards must be placed in extender boards to perform this calibration.

b. Set all of the potentiometers on the A3 board (A3R18, A3R36, A3R52 through A3R59, and A3R100) to midrange.

c. Set the data and sign bit switches on the Programmer for an output of -0.5mV.

d. Turn on DVS and momentarily depress GATE switch on the programmer. Allow a 30-minute DVS warm-up period.

CAUTION

High voltages are present on the amplifier board A7.

e. Set the RANGE switch on the Programmer to the X10 position and measure the output voltage.

f. Set the RANGE switch to the X1 position and adjust A7R9 until a reading 1/10 the reading in step (e) is obtained.

g. Repeat steps (e) and (f) until no further adjustments are needed.

h. Set the RANGE switch to the X10 position and adjust A3R100 for a reading of -5mV \pm 1mV.

i. Repeat steps (e) through (h) until no further adjustments are needed.

POSITIVE 16.384 VOLT REFERENCE ADJUST

j. On the Programmer, set the RANGE switch to X1 and the OUTPUT SIGN switch for negative

polarity.

k. Connect a digital voltmeter across capacitor A3C30.

l. Adjust A3R36 for a reading of 16.396 \pm .003V.

INDIVIDUAL BIT CALIBRATION

m. The individual bits are adjusted in two groups (8192, 4096, 2048, 1024, and 512, 256, 128, 64) according to the table below. The adjustment of all bits in the first group should be completed before proceeding to the second group. If any potentiometer in a group is adjusted to its end stop, continue adjusting the remaining potentiometers in the group and then back off 10% of the potentiometer that reached its end stop. Reprogram the bit associated with the potentiometer that was adjusted to its end stop and then adjust A3R36 for the correct output voltage level. If A3R36 must be adjusted, the entire bit calibration procedure must be repeated.

Voltage Bit	Meter Reading	Potentiometer
8192	-8192.5mV \pm 100 μ V	A3R52
4096	-4096.5mV \pm 100 μ V	A3R53
2048	-2038.5mV \pm 100 μ V	A3R54
1024	-1024.5mV \pm 100 μ V	A3R55
512	-512.5mV \pm 30 μ V	A3R56
256	-256.5mV \pm 30 μ V	A3R57
128	-128.5mV \pm 30 μ V	A3R58
64	-64.5mV \pm 30 μ V	A3R59

n. Check each of the remaining bits (32mV, 16mV, 8mV, 4mV, 2mV, 1mV, and 0.5mV) to insure that they are within \pm 200 μ V. If not, check the associated switching transistors and ladder network on the A3 board (see Figure 7-2, sheet 1).

POSITIVE ZERO VOLTAGE AND X10 FEEDBACK RESISTOR ADJUSTMENT CALIBRATION

o. Set the data and sign bits on the Programmer for an output of 0 volts.

p. Adjust A3R18 for 0V \pm 100 μ V.

q. Turn on the 4096 bit and observe the voltage reading.

r. Set the Programmer RANGE switch to X10 and adjust A7R85 for 10 times and the reading in Step (q) \pm 1mV.

y. Repeat Steps (p) through (r) until no further adjustments are necessary.

t. Turn off DVS and replace bottom cover or remove extender boards and replace boards as applicable.

5-73 METER ZERO

5-74 To zero-set either the voltmeter or ammeter, proceed as follows:

a. Turn the instrument off. Wait one minute for power supply capacitors to discharge completely.

b. Insert sharp object (pen point or awl) into the small indentation near the top of the round black plastic disc located directly below the meter face.

c. Rotate the disc until meter reads exactly zero.

5-75 VOLTMETER ADJUSTMENT

5-76 To adjust the calibration of the DVS voltmeter, proceed as follows:

a. On the Pocket Programmer, set the data bits, OUTPUT SIGN, and RANGE switches for a voltage output of +10V.

b. Turn on DVS and press GATE switch on Programmer.

c. Set the DVS front panel VOLTAGE control to the 10V position and adjust A4R14 until meter reads +10V.

d. Set the data bit, OUTPUT SIGN, and RANGE switches for an output voltage of -10V. The voltmeter should read -10V.

e. If it does not, halve the error and adjust A4R14 accordingly.

5-77 AMMETER ADJUSTMENT

5-78 To adjust the calibration of the DVS Ammeter proceed as follows:

a. Connect a 10 ohm, 10 watt, 1% resistor across the HI and LO output terminals.

b. On the Programmer set the data bit, OUTPUT SIGN, and RANGE switches for an output voltage of +10V.

c. Turn on DVS and press GATE switch on Programmer.

d. Set the DVS front panel CURRENT switch

to 1.2A and adjust A4R24 until ammeter reads +1A.

e. Set the data bit, OUTPUT SIGN, and RANGE switches for an output voltage of -10V. The meter should read -1A.

f. If it does not, halve the error and adjust A4R24 accordingly.

5-79 CURRENT LATCH ADJUSTMENT

5-80 To calibrate the accuracy of the current latch circuit, proceed as follows:

a. Remove the A6 control board, and using the extender board, place A6 in the extended position. Short the C_T terminals (rear barrier strip).

b. Connect a voltmeter across A6A6Q3 (Figure 7-2, Sheet 2). Connect meter positive to collector and common to emitter of A6A6Q3. When current latch occurs, the voltmeter will read approximately 0.7 volts.

c. Attach a 50 ohm, 50 watt, 1% load resistor across the HI and LO output terminals.

d. Set the switches on the Pocket Programmer for an output voltage of -1.00V and a current latch of 20mA.

e. Adjust potentiometers A6R19, R20, R21, and R108 fully clockwise.

f. Turn on DVS and press GATE switch on Pocket Programmer. Allow a 30-minute DVS warm-up period.

g. Adjust A6R19 ccw until the voltmeter indicates approximately 0.7V.

h. Program the voltage to -02.50V and the current latch to 50mA.

i. Adjust A6R21 ccw until the voltmeter indicates approximately 0.7V.

j. Program the voltage to -03.50V and the current latch to 70mA.

k. Adjust A6R20 until the voltmeter indicates approximately 0.7V.

l. Program the voltage to +01.00V and the current latch to 20mA.

m. Adjust A6R108 until voltmeter indicates approximately 0.7V.

SECTION VI REPLACEABLE PARTS

6-1 INTRODUCTION

6-2 This section contains information for ordering replacement parts. Table 6-4 lists parts in alpha-numeric order by reference designators and provides the following information:

- a. Reference Designators. Refer to Table 6-1.
- b. Description. Refer to Table 6-2 for abbreviations.
- c. Total Quantity (TQ). Given only the first time the part number is listed except in instruments containing many sub-modular assemblies, in which case the TQ appears the first time the part number is listed in each assembly.
- d. Manufacturer's Part Number or Type.
- e. Manufacturer's Federal Supply Code Number. Refer to Table 6-3 for manufacturer's name and address.
- f. Hewlett-Packard Part Number.
- g. Recommended Spare Parts Quantity (RS) for complete maintenance of one instrument during one year of isolated service.
- h. Parts not identified by a reference designator are listed at the end of Table 6-4 under Mechanical and/or Miscellaneous. The former consists of parts belonging to and grouped by individual assemblies; the latter consists of all parts not immediately associated with an assembly.

6-3 ORDERING INFORMATION

6-4 To order a replacement part, address order or inquiry to your local Hewlett-Packard sales office (see lists at rear of this manual for addresses). Specify the following information for each part: Model, complete serial number, and any Option or special modification (O) numbers of the instrument; Hewlett-Packard part number; circuit reference designator; and description. To order a part not listed in Table 6-4, give a complete description of the part, its function, and its location.

Table 6-1. Reference Designators

A	= assembly	E	= miscellaneous electronic part
B	= blower (fan)	F	= fuse
C	= capacitor	J	= Jack, jumper
CB	= circuit breaker	K	= relay
CR	= diode	L	= inductor
DS	= device, signaling (lamp)	M	= meter

Table 6-1. Reference Designators (Continued)

P	= plug	V	= vacuum tube, neon bulb, photocell, etc.
Q	= transistor	VR	= zener diode
R	= resistor	X	= socket
S	= switch	Z	= integrated circuit or network
T	= transformer		
TB	= terminal block		
TS	= thermal switch		

Table 6-2. Description Abbreviations

A	= ampere	mfr	= manufacturer
ac	= alternating current	mod.	= modular or modified
assy.	= assembly	mtg	= mounting
bd	= board	n	= nano = 10^{-9}
bkt	= bracket	NC	= normally closed
°C	= degree Centigrade	NO	= normally open
cd	= card	NP	= nickel-plated
coef	= coefficient	Ω	= ohm
comp	= composition	obd	= order by description
CRT	= cathode-ray tube	OD	= outside diameter
CT	= center-tapped	p	= pico = 10^{-12}
dc	= direct current	P.C.	= printed circuit
DPDT	= double pole, double throw	pot.	= potentiometer
DPST	= double pole, single throw	p-p	= peak-to-peak
elect	= electrolytic	ppm	= parts per million
encap	= encapsulated	pvr	= peak reverse voltage
F	= farad	rect	= rectifier
°F	= degree Fahrenheit	rms	= root mean square
fxd	= fixed	Si	= silicon
Ge	= germanium	SPDT	= single pole, double throw
H	= Henry	SFST	= single pole, single throw
Hz	= Hertz	SS	= small signal
IC	= integrated circuit	T	= slow-blow
ID	= inside diameter	tan.	= tantalum
incnd	= incandescent	Ti	= titanium
k	= kilo = 10^3	V	= volt
m	= milli = 10^{-3}	var	= variable
M	= mega = 10^6	ww	= wirewound
μ	= micro = 10^{-6}	W	= Watt
met.	= metal		

Table 5-3. Code List of Manufacturers

CODE NO.	MANUFACTURER	ADDRESS	CODE NO.	MANUFACTURER	ADDRESS
00629	EBZ Sales Co., Inc.	Jamaica, N. Y.	07138	Westinghouse Electric Corp.	
00656	Aerovox Corp.	New Bedford, Mass.		Electronic Tube Div.	Elmira, N. Y.
00853	Sangamo Electric Co.		07263	Fairchild Camera and Instrument Corp.	Semiconductor Div., Mountain View, Calif.
	S, Carolina Div.	Pickens, S. C.			Los Angeles, Calif.
01121	Allen Bradley Co.	Milwaukee, Wis.	07387	Birtcher Corp., The	
01255	Litton Industries, Inc.	Beverly Hills, Calif.	07397	Sylvania Electric Prod. Inc.	
01281	TRW Semiconductors, Inc.	Lawndale, Calif.		Sylvania Electronic Systems	
01295	Texas Instruments, Inc.		07716	Western Div.	Mountain View, Calif.
	Semiconductor-Components Div.			IRC Div. of TRW Inc.	Burlington Plant
		Dallas, Texas			Burlington, Iowa
01686	RGL Electronics, Inc.	Manchester, N. H.	07910	Continental Device Corp.	Hawthorne, Calif.
01930	Amerock Corp.	Rockford, Ill.	07933	Raytheon Co. Components Div.	
02107	Sparta Mfg. Co.	Dover, Ohio		Semiconductor Operation	
02114	Ferroxcube Corp.	Saugerties, N. Y.			Mountain View, Calif.
02606	Fenwal Laboratories	Morton Grove, Ill.	08484	Breeze Corporations, Inc.	Union, N. J.
02660	Amphenol Corp.	Broadview, Ill.	08530	Reliance Mica Corp.	Brooklyn, N. Y.
02735	Radio Corp. of America, Solid State and Receiving Tube Div.	Somerville, N. J.	08717	Sloan Company, The	Sun Valley, Calif.
03508	G. E. Semiconductor Products Dept.	Syracuse, N. Y.	08730	Vemaline Products Co. Inc.	Wyckoff, N. J.
03797	Eldema Corp.	Compton, Calif.	08806	General Elect. Co. Miniature Lamp Dept.	Cleveland, Ohio
03077	Transitron Electronic Corp.	Wakefield, Mass.	08863	Nylomatic Corp.	Norrisville, Pa.
03089	Pyrofilm Resistor Co. Inc.	Cedar Knolls, N. J.	08919	RCH Supply Co.	Vernon, Calif.
04009	Arrow, Hart and Hegeman Electric Co.	Hartford, Conn.	09021	Airco Speer Electronic Components	Bradford, Pa.
04072	ADJ Electronics, Inc.	Harbor City, Calif.	09102	*Hewlett-Packard Co. New Jersey Div.	Rockaway, N. J.
04213	Caddell & Burns Mfg. Co. Inc.	Mineola, N. Y.	09213	General Elect. Co. Semiconductor Prod. Dept.	Buffalo, N. Y.
04404	*Hewlett-Packard Co. Palo Alto Div.	Palo Alto, Calif.	09214	General Elect. Co. Semiconductor Prod. Dept.	Auburn, N. Y.
04713	Motorola Semiconductor Prod. Inc.	Phoenix, Arizona	09353	C & K Components Inc.	Newton, Mass.
05277	Westinghouse Electric Corp. Semiconductor Dept.	Youngwood, Pa.	09922	Bundy Corp.	Norwalk, Conn.
05347	Ultronix, Inc.	Grand Junction, Colo.	11115	Wagner Electric Corp.	
05820	Wakefield Engr. Inc.	Wakefield, Mass.		Tung-Sol Div.	Bloomfield, N. J.
06001	General Elect. Co. Electronic Capacitor & Battery Dept.	Irmo, S. C.	11236	CTS of Berne, Inc.	Berne, Ind.
06004	Bussak Div. Stewart-Warnor Corp.	Bridgeport, Conn.	11237	Chicago Telephone of Cal. Inc.	So. Pasadena, Calif.
06486	IRC Div. of TRW Inc. Semiconductor Plant	Lynn, Mass.	11802	IRC Div. of TRW Inc. Boone Plant	Boone, N. C.
06540	Amatom Electronic Hardware Co. Inc.	New Rochelle, N. Y.	11711	General Instrument Corp Rectifier Div.	Newark, N. J.
06555	Beeda Electrical Instrument Co.	Penneckok, N. H.	12136	Philadelphia Handle Co. Inc.	Camden, N. J.
06666	General Devices Co. Inc.	Indianapolis, Ind.	12615	U. S. Terminals, Inc.	Cincinnati, Ohio
06751	Semcor Div. Components, Inc.	Phoenix, Arizona	12617	Hamlin Inc.	Lake Mills, Wisconsin
06776	Robinson Nugent, Inc.	New Albany, Ind.	12697	Clarostat Mfg. Co. Inc.	Dover, N. H.
06812	Torrington Mfg. Co., West Div.	Van Nuys, Calif.	13103	Thermalloy Co.	Dallas, Texas
07137	Translator Electronics Corp.	Minneapolis, Minn.	14493	*Hewlett-Packard Co. Loveland Div.	Loveland, Colo.
			14655	Cornell-Dubilier Electronics Div.	Newark, N. J.
				Federal Pacific Electric Co.	
			14936	General Instrument Corp. Semiconductor Prod. Group	Hicksville, N. Y.
			15801	Fenwal Elect.	Framingham, Mass.
			16299	Corning Glass Works, Electronic Components Div.	Raleigh, N. C.

*Use Code 20480 assigned to Hewlett-Packard Co., Palo Alto, California

Table 6-3. Code List of Manufacturers (Continued)

CODE NO.	MANUFACTURER	ADDRESS
16758	Delco Radio Div. of General Motors Corp.	Kokomo, Ind.
17545	Atlantic Semiconductors, Inc.	Asbury Park, N. J.
17803	Fairchild Camera and Instrument Corp Semiconductor Div. Transducer Plant	Mountain View, Calif.
17870	Daven Div, Thomas A. Edison Industries McGraw-Edison Co.	Orange, N. J.
18324	Signetics Corp.	Sunnyvale, Calif.
19315	Bendix Corp. The Navigation and Control Div.	Teterboro, N. J.
19701	Electro/Midland Corp.	Mineral Wells, Texas
21520	Pansteel Metallurgical Corp.	No. Chicago, Ill.
22229	Union Carbide Corp. Electronics Div.	Mountain View, Calif.
22753	UID Electronics Corp.	Hollywood, Fla.
23036	Pamotor, Inc.	Pampa, Texas
24446	General Electric Co.	Schenectady, N. Y.
24455	General Electric Co. Lamp Div. of Con- sumer Prod. Group	Nela Park, Cleveland, Ohio
24655	General Radio Co.	West Concord, Mass.
24681	LTV ElectroSystems Inc Memcor/Com- ponents Operations	Huntington, Ind.
26982	Dynacool Mfg. Co. Inc.	Saugerties, N. Y.
27014	National Semiconductor Corp.	Santa Clara, Calif.
28480	Hewlett-Packard Co.	Palo Alto, Calif.
28520	Heyman Mfg. Co.	Kenilworth, N. J.
28875	IMC Magnetics Corp. New Hampshire Div.	Rochester, N. H.
31514	SAE Advance Packaging, Inc.	Santa Ana, Calif.
31827	Budwig Mfg. Co.	Ramona, Calif.
33173	G. E. Co. Tube Dept.	Owensboro, Ky.
35434	Lectrohm, Inc.	Chicago, Ill.
37942	P. R. Mallory & Co. Inc.	Indianapolis, Ind.
42190	Muter Co.	Chicago, Ill.
43334	New Departure-Hyatt Bearings Div. General Motors Corp.	Sandusky, Ohio
44655	Ohmite Manufacturing Co.	Skokie, Ill.
46384	Penn Engr. and Mfg. Corp.	Doylestown, Pa.
47904	Polaroid Corp.	Cambridge, Mass.
49956	Raytheon Co.	Lexington, Mass.
55026	Simpson Electric Co. Div. of American Gage and Machine Co.	Chicago, Ill.
56289	Sprague Electric Co.	North Adams, Mass.
58474	Superior Electric Co.	Bristol, Conn.
58849	Syntron Div. of FMC Corp.	Homer City, Pa.
59730	Thomas and Betts Co.	Philadelphia, Pa.
61637	Union Carbide Corp.	New York, N. Y.
63743	Ward Leonard Electric Co.	Mt. Vernon, N. Y.

CODE NO.	MANUFACTURER	ADDRESS
70563	Amperite Co. Inc.	Union City, N. J.
70901	Beemer Engrg. Co.	Fort Washington, Pa.
70903	Belden Corp.	Chicago, Ill.
71218	Bud Radio, Inc.	Willoughby, Ohio
71279	Cambridge Thermionic Corp.	Cambridge, Mass.
71400	Bussmann Mfg. Div. of McGraw & Edison Co.	St. Louis, Mo.
71450	CTS Corp.	Elkhart, Ind.
71468	I. T. T. Cannon Electric Inc.	Los Angeles, Calif.
71590	Globe-Union Inc.	Milwaukee, Wis.
71700	General Cable Corp. Cornish Wire Co. Div.	Williamstown, Mass.
71707	Coto Coil Co. Inc.	Providence, R. I.
71744	Chicago Miniature Lamp Works	Chicago, Ill.
71785	Cinch Mfg. Co. and Howard E. Jones Div.	Chicago, Ill.
71984	Dow Corning Corp.	Midland, Mich.
72136	Electro Motive Mfg. Co. Inc.	Willimantic, Conn.
72619	Dialight Corp.	Brooklyn, N. Y.
72699	General Instrument Corp.	Newark, N. J.
72765	Drake Mfg. Co.	Harwood Heights, Ill.
72962	Elastic Stop Nut Div. of Amerace Ensa Corp.	Union, N. J.
72982	Eric Technological Products Inc.	Eric, Pa.
73096	Hart Mfg. Co.	Hartford, Conn.
73138	Beckman Instruments Inc. Hellipot Div.	Fullerton, Calif.
73168	Fenwal, Inc.	Ashland, Mass.
73293	Hughes Aircraft Co. Electron Dynamics Div.	Torrance, Calif.
74445	Amperex Electronic Corp.	Hicksville, N. Y.
73506	Bradley Semiconductor Corp.	New Haven, Conn.
73559	Carling Electric, Inc.	Hartford, Conn.
73734	Federal Screw Products, Inc.	Chicago, Ill.
74193	Heinemann Electric Co.	Trenton, N. J.
74545	Hubbell Harvey Inc.	Bridgeport, Conn.
74668	Amphenol Corp. Amphenol RF Div.	Danbury, Conn.
74970	E. F. Johnson Co.	Waseca, Minn.
75042	IRC Div. of TRW, Inc.	Philadelphia, Pa.
75183	*Howard B. Jones Div. of Cinch Mfg. Corp.	New York, N. Y.
75376	Kurz and Kasch, Inc.	Dayton, Ohio
75382	Kilka Electric Corp.	Mt. Vernon, N. Y.
75915	Littlefuse, Inc.	Des Plaines, Ill.
76381	Minnesota Mining and Mfg. Co.	St. Paul, Minn.
76385	Minor Rubber Co. Inc.	Bloomfield, N. J.
76487	James Millen Mfg. Co. Inc.	Malden, Mass.
76493	J. W. Miller Co.	Compton, Calif.

*Use Code 71785 assigned to Cinch Mfg. Co., Chicago, Ill.

Table 6-3. Code List of Manufacturers (Continued)

CODE NO.	MANUFACTURER	ADDRESS	CODE NO.	MANUFACTURER	ADDRESS
76530	Cinch	City of Industry, Calif.	83508	Grant Pulley and Hardware Co.	West Nyack, N. Y.
76854	Oak Mfg. Co. Div. of Oak	Electro/Netics Corp. Crystal Lake, Ill.	83594	Burroughs Corp. Electronic	Plainfield, N. J.
77058	Bendix Corp., Electrodynamics Div.	No. Hollywood, Calif.	83835	U. S. Radium Corp.	Morristown, N. J.
77122	Palnut Co.	Mountainside, N. J.	83077	Yardeny Laboratories, Inc.	New York, N. Y.
77147	Patton-MacGuyer Co.	Providence, R. I.	84171	Arco Electronics, Inc.	Great Neck, N. Y.
77221	Phaostron Instrument and Electronic Co.	South Pasadena, Calif.	84411	TRW Capacitor Div.	Ogallala, Neb.
77252	Philadelphia Steel and Wire Corp.	Philadelphia, Pa.	86684	RCA Corp. Electronic Components	Harrison, N. J.
77342	American Machine and Foundry Co.	Potter and Brumfield Div. Princeton, Ind.	86838	Rummel Fibre Co.	Newark, N. J.
77630	TRW Electronic Components Div.	Camden, N. J.	87034	Marco & Oak Industries a Div. of Oak	Electro/netics Corp. Anaheim, Calif.
77764	Resistance Products Co.	Harrisburg, Pa.	87216	Philco Corp. Lansdale Div.	Lansdale, Pa.
78189	Illinois Tool Works Inc. Shakeproof Div.	Elgin, Ill.	87585	Stockwell Rubber Co. Inc.	Philadelphia, Pa.
78452	Everlock Chicago, Inc.	Chicago, Ill.	87929	Tower-Olschan Corp.	Bridgeport, Conn.
78488	Stackpole Carbon Co.	St. Marys, Pa.	88140	Cutler-Hammer Inc. Power Distribution	and Control Div. Lincoln Plant
78526	Stanwyck Winding Div.	San Fernando			Lincoln, Ill.
78553	Electric Mfg. Co. Inc.	Newburgh, N. Y.	88245	Litton Precision Products Inc, USECO	Div. Litton Industries Van Nuys, Calif.
78584	Tinnerman Products, Inc.	Cleveland, Ohio	90634	Gulton Industries Inc.	Metuchen, N. J.
79136	Stewart Stamping Corp.	Yonkers, N. Y.	90763	United-Car Inc.	Chicago, Ill.
79136	Walden Kohinoor, Inc.	L. I. C., N. Y.	91345	Miller Dial and Nameplate Co.	El Monte, Calif.
79307	Whitehead Metals Inc.	New York, N. Y.	91418	Radio Materials Co.	Chicago, Ill.
79727	Continental-Wirt Electronics Corp.	Philadelphia, Pa.	91506	Augat, Inc.	Attleboro, Mass.
79963	Zierick Mfg. Co.	Mt. Kisco, N. Y.	91637	Dale Electronics, Inc.	Columbus, Neb.
80031	Mepco Div. of Sessions Clock Co.	Morristown, N. J.	91662	Elco Corp.	Willow Grove, Pa.
80294	Bourns, Inc.	Riverside, Calif.	91929	Honeywell Inc. Div. Micro Switch	Freeport, Ill.
81042	Howard Industries Div. of Mal Ind. Inc.	Racine, Wisc.	92825	Whitso, Inc.	Schiller Pk., Ill.
81073	Grayhill, Inc.	La Grange, Ill.	93332	Sylvania Electric Prod. Inc. Semi-	conductor Prod. Div. Woburn, Mass.
81483	International Rectifier Corp.	El Segundo, Calif.	93410	Essex Wire Corp. Stemco	Controls Div. Mansfield, Ohio
81751	Columbus Electronics Corp.	Yonkers, N. Y.	94144	Raytheon Co. Components Div.	Ind. Components Oper. Quincy, Mass.
82099	Goodyear Sundries & Mechanical Co. Inc.	New York, N. Y.	94154	Wagner Electric Corp.	Tung-Sol Div. Livingston, N. J.
82142	Airco Spear Electronic Components	Du Bois, Pa.	94222	Southco Inc.	Lester, Pa.
82219	Sylvania Electric Products Inc.	Electronic Tube Div. Receiving	95253	Leecraft Mfg. Co. Inc.	L. I. C., N. Y.
82389	Tube Operations	Emporium, Pa.	95354	Methode Mfg. Co.	Rolling Meadows, Ill.
82647	Switchcraft, Inc.	Chicago, Ill.	95712	Bendix Corp. Microwave	Devices Div. Franklin, Ind.
82866	Metals and Controls Inc. Control	Products Group Attleboro, Mass.	95987	Weckesser Co. Inc.	Chicago, Ill.
82877	Research Products Corp.	Madison, Wis.	96791	Amphenol Corp. Amphenol	Controls Div. Janesville, Wis.
82877	Retron Inc.	Woodstock, N. Y.	97464	Industrial Retaining Ring Co.	Irvington, N. J.
82893	Vector Electronic Co.	Glendale, Calif.	97702	IMC Magnetics Corp. Eastern Div.	Westbury, N. Y.
83058	Carr Fastener Co.	Cambridge, Mass.	98291	Scalestro Corp.	Mamaroneck, N. Y.
83186	Victory Engineering Corp.	Springfield, N. J.	98410	ETC Inc.	Cleveland, Ohio
83298	Bendix Corp. Electric Power Div.	Eatontown N. J.	98978	International Electronic Research Corp.	Burbank, Calif.
83330	Herman H. Smith, Inc.	Brooklyn, N. Y.	99934	Ranbrandt, Inc.	Boston, Mass.
83385	Central Screw Co.	Chicago, Ill.			
83501	Gavitt Wire and Cable Div. of	Amerace Esna Corp. Brookfield, Mass.			

Table 6-4, Replaceable Parts

REF. DESIG.	DESCRIPTION	TQ	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A1	Input Board		Refer to proper Option Appendix			
A1A1	Isolator circuit		Refer to proper Option Appendix			
CR1,2	Diode, Si 200mA 75V	2		28480	1901-0050	2
Q1,2	SS NPN Si	2		28480	1854-0071	2
R1,2,3			Refer to proper Option Appendix			
R4	fxd, comp 750 Ω \pm 5%, 1/2W	1	EB-7515	01121	0686-7515	1
R5	fxd, comp 82 Ω \pm 5%, 1/4W	1	CB-8205	01121	0683-8205	1
R6	fxd, comp 750 Ω \pm 5%, 1/4W	1	CB-7515	01121	0683-7515	1
Z1	Photo-isolator	1		28480	1990-0407	1
A1A2 through A1A17	Same as A1A1	16				
A1C1-3	fxd, ceramic .47 μ F 25Vdc	3		28480	0160-0174	1
C4	fxd, ceramic .1 μ F 50Vdc	2		28480	0150-0121	1
C5	fxd, mica 390pF 300Vdc	1	RDM15F39153C	72136	0140-0200	1
C6	fxd, mylar .01 μ F 200Vdc	1	292P19352-PTS	56289	0160-0207	1
C7	fxd, ceramic .1 μ F 50Vdc			28480	0150-0121	
CR1-4	Diode, Si 200mA 75V	4		28480	1901-0050	4
Q1			Refer to Instrument Modification Sheet			
Q2-Q5	SS NPN Si	4		28480	1854-0071	4
Q6			Refer to proper Option Appendix			
Q7			Refer to Instrument Modification Sheet			
R1,2,3			Refer to proper Option Appendix			
R4			Refer to Instrument Modification Sheet			
R5	fxd, comp 1K Ω \pm 5%, 1/4W	3	CB-1025	01121	0683-1025	1
R6	fxd, ww 100 Ω \pm 5%, 3W	2	242E	56289	0813-0050	1
R7	fxd, met film 11K Ω \pm 2%, 1/8W	1	MF4C TD	30983	0757-0949	1
R8	fxd, met film 7.5K Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0757-0440	1
R9	fxd, comp 1K Ω \pm 5%, 1/4W		CB-1025	01121	0683-1025	
R10	fxd, ww 100 Ω \pm 5%, 3W		242E	56289	0813-0050	
R11	fxd, comp 3K Ω \pm 5%, 1/4W	1	CB-3025	01121	0683-3025	1
R12	fxd, comp 910 Ω \pm 5%, 1/2W	1	EB-9115	01121	0686-9115	1
R13	fxd, comp 750 Ω \pm 5%, 1/2W	1	EB-7515	01121	0686-7515	1
R14	fxd, comp 750 Ω \pm 5%, 1/4W	2	CB-7515	01121	0683-7515	1
R15			Refer to proper Option Appendix			
R16	fxd, comp 82 Ω \pm 5%, 1/4W	2	CB-8205	01121	0683-8205	1
R17,18,19			Refer to proper Option Appendix			
R20	fxd, comp 1K Ω \pm 5%, 1/4W		CB-1025	01121	0683-1025	
R21	fxd, comp 750 Ω \pm 5%, 1/4W		CB-7515	01121	0683-7515	
R22	fxd, comp 82 Ω \pm 5%, 1/4W		CB-8205	01121	0683-8205	
R23	fxd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
VR1	Diode, zener 4.22V 400mW	2		28480	1902-3070	2
VR2,3	Diode, zener 4.99V	2	SZ11213-54	04713	1902-0533	2
VR4	Diode, zener 4.22V 400mW			28480	1902-3070	
VR5			Refer to proper Option Appendix			
Z1,2	Photo-Isolator	2		28480	1990-0407	2
Z3,4	Monostable Multivibrator, IC	2	SN13617	01295	1820-0261	2
A2	Logic Plug-In Board		Refer to proper Option Appendix			
C1	fxd, ceramic .47 μ F 25Vdc	6		28480	0160-0174	2
C2	fxd, Mica 150pF 300Vdc	1	RDM15F151J3C	72136	0140-0196	1
C4-8	fxd, ceramic .47 μ F 25Vdc			28480	0160-0174	
C9	fxd, tant. 4.7 μ F 6Vdc	1	150D475X5006A2-DYS	56289	0180-1954	1

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	TQ	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A2DS1	Lamp, 6Vdc incandescent	1	2305RA	11115	2140-0324	1
Q1-3	SS NPN SI	3		28480	1854-0071	3
R1	fxd, comp 1K Ω \pm 5%, 1/4W	4	CB-1025	01121	0683-1025	1
R2	fxd, comp 4.7K Ω \pm 5%, 1/4W	1	CB-4725	01121	0683-4725	1
R3	fxd, comp 1K Ω \pm 5%, 1/4W		CB-1025	01121	0683-1025	
R4	fxd, comp 200 Ω \pm 5%, 1/4W	1	CB-2015	01121	0683-2015	1
R5	fxd, film 30.1K Ω \pm 1%, 1/8W	1		28480	0757-0453	1
R6	fxd, comp 5.1K Ω \pm 5%, 1/4W	1	CB-5125	01121	0683-5125	1
R7	fxd, comp 510 Ω \pm 5%, 1/4W	1	CB-5115	01121	0683-5115	1
R8	fxd, comp 2K Ω \pm 5%, 1/4W	1	CB-2025	01121	0683-2025	1
R9, 10	fxd, comp 1K Ω \pm 5%, 1/4W		CB-1025	01121	0683-1025	
S1	Switch, slide DPDT	1		28480	3101-0932	1
Z1-4			Refer to proper Option Appendix			
Z5	4-2 Input NAND Gate, IC	1		28480	1820-0054	1
Z6	Monostable Multivibrator, IC	1	SN13617	01295	1820-0261	1
Z7, 8	Hybrid Resistive Network, IC	2		28480	1810-0041	2
Z9-12			Refer to proper Option Appendix			
A3	D to A Converter Plug-In Board	1		28480	5060-6192	
A3A1	NOT USED	-		--	--	-
A3A2C1	fxd, ceramic .001 μ F 500Vdc	1		28480	0160-3398	1
Q2	fxd, ceramic .005 μ F 100V	1		28480	0160-2639	1
CR1-3	Diode, Si 200mA 75V	3		28480	1901-0050	3
Q1	SS NPN SI	1		28480	1854-0087	1
Q2	SS PNP SI	1		28480	1853-0078	1
Q3	SS NPN SI	1		28480	1854-0317	1
R1	fxd, comp 3.3K Ω \pm 5%, 1/2W	1	EB-3325	01121	0686-3325	1
R2	fxd, comp 12K Ω \pm 5%, 1/2W	1	EB-1235	01121	0686-1235	1
R3	fxd, comp 2.2K Ω \pm 5%, 1/2W	1	EB-2225	01121	0686-2225	1
R4, 5	fxd, comp 10K Ω \pm 5%, 1/2W	2	EB-1035	01121	0686-1035	1
A3A3 through A3A15	Same as A3A2	13				
A3A16C1	fxd, ceramic .001 μ F 500Vdc	1		28480	0160-3398	1
Q2	fxd, ceramic .005 μ F 100V	1		28480	0160-2639	1
CR1-3	Diode, Si 200mA 75V	3		28480	1901-0050	3
Q1	SS NPN SI	1		28480	1854-0087	1
Q2	SS PNP SI	1		28480	1853-0078	1
Q3	SS NPN SI	1		28480	1854-0317	1
A3A16R1	fxd, comp 3.3K Ω \pm 5%, 1/2W	1	EB-3325	01121	0686-3325	1
R2	fxd, comp 10K Ω \pm 5%, 1/2W	3	EB-1035	01121	0686-1035	1
R3	fxd, comp 2.2K Ω \pm 5%, 1/2W	1	EB-2225	01121	0686-2225	1
R4, 5	fxd, comp 10K Ω \pm 5%, 1/2W	2	EB-1035	01121	0686-1035	1
R6	fxd, comp 33K Ω \pm 5%, 1/2W	1	EB-3335	01121	0686-3335	1
A3AR-Z1	Ref. Amp. 6.8V \pm 5% TC \pm .0005%	1		28480	5080-7139	1
AR-R1	fxd, ww - Part of 5080-7139	1				
AR-R2	fxd, film - Part of 5080-7139	1				
AR-R3	fxd, film - Part of 5080-7139	1				
AR-R4	fxd, film - Part of 5080-7139	1				

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	TQ	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A305	fxd, mica 330pF 500Vdc	1	RCM15331J	00853	0140-0168	1
C11	fxd, ceramic .001 μ F 500Vdc	1		26480	0160-3398	1
C12	fxd, mylar .01 μ F 200V	1	192P10392	56289	0160-0161	1
C13, 30	fxd, elect, 22 μ F 35V	2	150D226X0035R2	56289	0180-0160	1
C40, 41	fxd, elect, 1 μ F 35Vdc	2	150D105X9035A2	56289	0180-0291	1
CR10-14	Diode, Si 200mA 75V	5		28480	1901-0050	5
L1	Ferrite Bead	1		28480	9170-0047	1
Q10	SS PNP Si	3		28480	1853-0099	3
Q11	Dual NPN Si	1		28480	1854-0221	1
Q12	SS NPN Si	2		28480	1854-0071	2
Q13	SS NPN Si	1		28480	1854-0087	1
Q14	SS NPN Si	1		28480	5080-7132	1
Q15, 30	SS PNP Si			28480	1853-0099	
Q31	SS NPN Si	2		28480	1854-0244	2
Q32	SS NPN Si			28480	1854-0071	
Q40	SS NPN Si			28480	1854-0244	
R10	fxd, comp 43K Ω \pm 5%, 1/2W	1	EB-4335	01121	0686-4335	1
R11	fxd, comp 3K Ω \pm 5%, 1/2W	1	EB-3025	01121	0686-3025	1
R12	fxd, met. film 1K Ω \pm 1%, 1/4W	1	Type CCA T-0	07716	0757-0338	1
R13	fxd, comp 2.4K Ω \pm 5%, 1/2W	1	EB-2425	01121	0606-2425	1
R14	fxd, met. film 200K Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0757-0472	1
R15	fxd, met. film 160K Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0698-5092	1
R16	fxd, ww 297 Ω \pm 1%, 1/4W 20ppm	1	Type R303B	01686	0811-1929	1
R17	fxd, ww 243 Ω \pm 1%, 1/4W 20ppm	1	Type R303B	01686	0811-2075	1
R18	var, ww 500 Ω (Type 100)	1	Model 100	11502	2100-0898	1
R19	fxd, ww 10K Ω \pm 0.1%, TC \pm 2ppm	1	Type 7007	01686	0811-2577	1
R20A	fxd, ww 16K Ω \pm 0.1% (Matched to R20B)	1	Type 7007	01686	0811-2757	1
R20B	fxd, ww 15.82K Ω \pm 0.1%	1	Type 7007	01686	0811-2757	1
R21	fxd, comp 1.8K Ω \pm 5%, 1/2W	1	EB-1825	01121	0686-1825	1
R22	fxd, met. film 7.5K Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0757-0440	1
R23	fxd, met. film 12K Ω \pm 1%, 1/8W	2	Type CEA T-0	07716	0698-5088	1
R24	fxd, comp 2.2K Ω \pm 5%, 1/2W	2	EB-2225	01121	0686-2225	1
R25	fxd, met. film 12K Ω \pm 1%, 1/8W		Type CEA T-0	07716	0689-5088	
R26	fxd, comp 2K Ω \pm 5%, 1/2W	1	EB-2025	01121	0686-2025	1
R27	fxd, met. film 600 Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0757-1100	1
R30	fxd, met. film 2K Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0757-0283	1
R31	fxd, comp 51 Ω \pm 5%, 1/2W	1	EB-5105	01121	0686-5105	1
R34A	fxd, ww 2350 Ω \pm 0.1% (Match to R34B)	1	Type 7007	01686	0811-1167	1
R34B	fxd, ww 1940 Ω \pm 0.1%	1	Type 7007	01686	0811-1167	1
R36	var, ww 100 Ω \pm 5%	9	Model 100	11502	2100-1450	2
R40	fxd, comp 1.2K Ω \pm 5%, 1/2W	1	EB-1225	01121	0686-1225	1
R50	fxd, met. film 196 Ω \pm 1%, 1/8W	1	Type CEA T-0	07716	0698-3440	1
R51	fxd, comp 18 Ω \pm 5%, 1/2W	1	EB-1805	01121	0686-1805	1
R52-59	var, ww 100 Ω \pm 5%		Model 100	11502	2100-1450	
R60	fxd, ww 19.96K Ω \pm 1%, TC \pm 2ppm	1	Type 7007	01686	0811-2574	1
R61-67	fxd, ww 19.96K Ω \pm 1%, TC \pm 5ppm	7	Type 7007	01686	0811-2575	2
R68-76	fxd, ww 10K Ω \pm 1%, TC \pm 5ppm	9	Type E30	01686	0811-1994	2
R77, 78	fxd, met. film 10K Ω \pm 1%, 1/8W	2	Type CEA T-0	07716	0757-0442	1
R79	JUMPER	-		--	--	--
R80-86	fxd, ww 20K Ω \pm 1% TC \pm 5ppm	7	Type 7007	01686	0811-2609	2
R87-89, 91	fxd, met. film 20K Ω \pm 1%, 1/8W	4	Type CEA T-0	07716	0757-0449	1
R92	fxd, ww 150K Ω \pm 1% TC \pm 5ppm	1	Type 7007	01686	0811-2763	1

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	TQ	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A3R93	fxd, ww 100K Ω \pm 1%, TC \pm 5ppm	1	Type 7010	01686	0811-1997	1
R94	fxd, ww 406.2 Ω \pm 1%, TC \pm 5ppm	1	Type 7007	01686	0811-2762	1
R95	fxd, met. film 562K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0482	1
R96	fxd, met. film 139 Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-4799	1
R97	fxd, met. film 11K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0443	1
R98	fxd, met. film 1M Ω \pm 1%, 1/4W	1	Type CEB T-O	07716	0757-0344	1
R99	fxd, met. film 390K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-5093	1
R100	var. ww 15K Ω \pm 5%	1	Model 100	11502	2100-0896	1
R102	NOT ASSIGNED	-	-	-	-	-
R103	fxd, comp 5.6K Ω \pm 5%, 1/2W	1	EB-5625	01121	0686-5625	1
VR30	Diode, zener 4.22V 400mW	1		28480	1902-3070	1
VR31	Diode, zener 12.4V 400mW	1		28480	1902-3185	1
VR40	Diode, zener 5.62V 400mW	1		28480	1902-3104	1
A4	Power Supply Board	1		28480	06130-60025	
C4, 5	fxd, elect. 1.450 μ F 45Vdc	2		28480	0180-1893	1
C8, 9	fxd, elect. 400 μ F 100Vdc	2		28480	0180-1887	1
C10	fxd, elect. 100 μ F 25Vdc	2	30D107G025DD2	56289	0180-0094	1
C11-22	fxd, ceramic .05 μ F 400V	12	33C 17A CDH	56289	0150-0052	2
C23	fxd, elect. 100 μ F 25Vdc		30D107G025DD2	56289	0180-0094	
CR1-4	Rect. Si 1A 400prv	18		28480	1901-0328	8
CR5, 6, 7	Rect. Si 250mW 200prv	4		28480	1901-0033	4
CR8-21	Rect. Si 1A 400prv			28480	1901-0326	
CR22	Rect. Si 250mW 200prv			28480	1901-0033	
K1	Relay, 6Vdc	1	643-6V	09023	0490-0513	1
Q1	SS PNP Si	1		28480	1853-0099	1
R1-R3	fxd, comp 560 Ω \pm 5%, 1/2W	3	EB-5615	01121	0686-5615	1
R4, 5	fxd, comp 3.6K Ω \pm 5%, 1/2W	3	EB-3625	01121	0686-3625	1
R6, 7	fxd, met. oxide 5.1K Ω \pm 5%, 2W	2	Type C42S	16299	0698-3644	1
R8, 9	fxd, comp 20K Ω \pm 5%, 1W	2	GB-2035	01121	0689-2035	1
R10	fxd, comp 3K Ω \pm 5%, 1/2W	1	EB-3025	01121	0686-3025	1
R11	fxd, comp 3.6K Ω \pm 5%, 1/2W		EB-3625	01121	0686-3625	
R12	fxd, comp 9.1K Ω \pm 5%, 1/2W	1	EB-9125	01121	0686-9125	1
R13	fxd, comp 33K Ω \pm 5%, 1/2W	1	EB-3335	01121	0686-3335	1
R14	var. ww 5K Ω \pm 5%	1	Type CT-100-4	06486	2100-0741	1
R15	fxd, film 9.09K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0288	1
R16	fxd, film 5.2K Ω \pm 1%, 1/4W	1	Type CEB T-O	07716	0698-5148	1
R17	fxd, film 10.0K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0442	1
R18	fxd, film 68.1K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0461	1
R19	fxd, film 2K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0283	1
R20	fxd, film 392 Ω \pm 1%, 1/2W	1	Type CEC T-O	07716	0757-0811	1
R21	fxd, film 121 Ω \pm 1%, 1/4W	1	Type CEB T-O	07716	0757-0316	1
R22	fxd, film 42.2 Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0757-0069	1
R23	Thermistor 64 Ω \pm 10%	1	LB16J1	02606	0837-0023	1
R24	var. ww 10 Ω \pm 5%	1	Type CT-100-4	06486	2100-1767	1
R25	fxd, film 42.2 Ω \pm 1%, 1/8W		Type CEA T-O	07716	0757-0316	
R26	fxd, comp 200 Ω \pm 5%, 1/2W	1	EB-2015	01121	0686-2015	1
R27	fxd, comp 2K Ω \pm 5%, 1/2W	1	EB-2025	01121	0686-2025	1
T2	Bias Transformer	1		28480	5080-1773	1
A5	Interconnect Board	1		28480	06130-60026	
C1	fxd, mylar, .033 μ F 200Vdc	1	192P33392	56289	0160-0163	1
C2	fxd, tant. 4.7 μ F 35Vdc	1	150D475X9035B2-DYS	56289	0180-0100	1
C3	fxd, ceramic 0.1 μ F 50Vdc	1	5C50B1-CML	56289	0150-0121	1

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	TQ	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A5CR1-0	Rect. SI 1A 200prv	0		28480	1901-0327	6
J1-6	P.C. Board Edge Connectors	6	252-22-30-340	16530	1251-1867	2
L1	Inductor 1 μ H	1		28480	9100-2198	1
R3-5	fxd, ww 1.25 Ω \pm 1%, 4W	3	NS-2-18	91637	0811-2556	1
R8	fxd, comp 10 Ω \pm 5%, 1/2W	1	EB-1000	01121	0686-1000	1
R9	JUMPER					
R10	fxd, film 4K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-5808	1
R11	fxd, film 1K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0260	1
R12	fxd, ww 10K Ω \pm 0.1%, 1/4W	1	Type E30	01686	0811-1994	1
A6	Control Board		Refer to proper Option Appendix			
A6A1	Input Isolator Circuit					
CR1,2	Diode, Si 200mA 75V	2		28480	1901-0050	2
Q1,2	SS NPN SI	2		28480	1854-0071	2
R1,2,3			Refer to proper Option Appendix			
R4	fxd, comp 750 Ω \pm 5%, 1/2W	1	EB-7515	01121	0686-7515	1
R5	fxd, comp 82 Ω \pm 5%, 1/4W	1	CB-8205	01121	0683-8205	1
R6	fxd, comp 750 Ω \pm 5%, 1/4W	1	CB-7515	01121	0683-7515	1
Z1	Photo-isolator	1		28480	1990-0407	1
A6A2 through A6A4	Same as A6A1					
A6A5	Latch Status Isolator and Output Amplifier					
CR1,2	Diode, Si 200mA 75V	2		28480	1901-0050	2
Q1-4	SS NPN SI	4		28480	1854-0071	4
R1	fxd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
R2	fxd, comp 1.3K Ω \pm 5%, 1/2W	1	EB-1325	01121	0686-1325	1
R3	fxd, comp 750 Ω \pm 5%, 1/2W	1	EB-7515	01121	0683-7515	1
R4	fxd, comp 82 Ω \pm 5%, 1/4W	1	CB-8205	01121	0683-8205	1
R5	fxd, comp 12K Ω \pm 5%, 1/4W	1	CB-1235	01121	0683-1235	1
R6	fxd, comp 100 Ω \pm 5%, 1/4W	1	CB-1015	01121	0683-1015	1
R7	fxd, comp 5.6K Ω \pm 5%, 1/2W	1	EB-5625	01121	0686-5625	1
R8						
VR1			Refer to proper Option Appendix			
Z1	Photo-Isolator	1		28480	1900-0407	1
A6A6	Overload Status Isolator and Output Amplifier					
CR1,2	Diode, Si 200ma 75V	2		28480	1901-0050	2
Q1-3	SS NPN SI	3		28480	1854-0071	3
Q4			Refer to Instrument Modification Sheet			
R1	fxd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
R2	fxd, comp 1.3K Ω \pm 5%, 1/2W	1	EB-1325	01121	0686-1325	1
R3	fxd, comp 750 Ω \pm 5%, 1/2W	1	EB-7515	01121	0683-7515	1
R4	fxd, comp 82 Ω \pm 5%, 1/4W	1	CB-8205	01121	0683-8205	1
R5	fxd, comp 12K Ω \pm 5%, 1/4W	1	CB-1235	01121	0683-1235	1
R6	fxd, comp 100 Ω \pm 5%, 1/4W	1	CB-1015	01121	0683-1015	1
R7						
R8			Refer to Instrument Modification Sheet			
VR1			Refer to proper Option Appendix			
Z1			Refer to proper Option Appendix			
A6C1	fxd, mlcc 240pF 300Vdc	4	RDM15F241J3C	00853	0140-0199	1

Table G-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	TQ	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A6C2	fxd, ceramic .47 μ F 25Vdc	2	5C11B7	56289	0160-0174	1
C3	fxd, mica 30pF 300Vdc	1	RDM15E300J3C	00853	0160-2199	1
C4	fxd, mylar .001 μ F 200Vdc	3	192P10292	56289	0160-0153	1
C5, 6, 7	fxd, mica 240pF 300Vdc		RDM15F241J3C	00853	0140-0199	
C8	fxd, mylar 2200pF 200Vdc	1	192P22292	56289	0160-0154	1
C9, 10	fxd, mylar .001 μ F 200Vdc		192P10292	56289	0160-0153	
C11	fxd, mylar .033 μ F 200Vdc	1	192P33392	56289	0160-0163	1
C12	fxd, mica 150pF 300Vdc	1	RDM15F151J3C	00853	0140-0196	1
C13, 14	fxd, mica 390pF 300Vdc	2	RDM15F391J3C	00853	0140-0200	1
C15	fxd, ceramic, 1 μ F 50Vdc	1	5C50B1-CML	56289	0150-0121	1
C16	fxd, tant, 4.7 μ F 35Vdc	1	150D475X9035B2-DYS	56289	0180-0100	1
C17	fxd, ceramic .47 μ F 25Vdc		5C11BC	56289	0160-C174	
CR1, 2	Diode, Si 200mA 75V	17		28480	1901-0050	8
CR5-13	Diode, Si 200mA 75V			28480	1901-0050	
CR14, 15			Refer to proper Option Appendix			
CR16-18	Diode, Si 200mA 75V			28480	1901-0050	
CR19	Stabistor, Si 10prv 400mW	1		28480	1901-0460	1
CR20	Diode, Si 200mA 75V			28480	1901-0050	
A6Q1, 2, 3	SS NPN Si	17		28480	1854-0071	8
Q4	SS NPN Si	6	2N3417	03508	1854-0087	5
Q5, 6	SS NPN Si			28480	1854-0071	
Q8-13	SS PNP Si	9		28480	1853-0099	5
Q14, 15	SS NPN Si			28480	1854-0071	
Q16-18	SS NPN Si		2N3417	03508	1854-0087	
Q19, 20	SS PNP Si			28480	1853-0099	
Q21, 22	SS NPN Si		2N3417	03508	1854-0087	
Q23	SS PNP Si			28480	1853-0099	
Q24-33	SS NPN Si			28480	1854-0071	
Q34	Power NPN Si	1	2N1711	17803	1854-0003	1
R1-3	fxd, comp 3.9K Ω \pm 5%, 1/4W	3	CB-3925	01121	0683-3925	1
R4-6	fxd, comp 39K Ω \pm 5%, 1/4W	3	CB-3935	01121	0683-3935	1
R7	fxd, ww 220 Ω \pm 5%, 2W	1	Type BWH	07716	0811-1763	1
R8-10	fxd, comp 5.1K Ω \pm 5%, 1/4W	9	CB-5125	01121	0683-5125	1
R11-13	fxd, comp 9.1K Ω \pm 5%, 1/4W	3	CB-9125	01121	0683-9125	1
R14, 15	fxd, comp 20K Ω \pm 5%, 1/4W	12	CB-2035	01121	0683-2035	2
R16-18	fxd, film 19.6K Ω \pm 1%, 1/8W	3	Type CEA T-O	07716	0698-3157	1
R19	var, cermet 1K Ω \pm 10%	1	62-224-1	73138	2100-2633	1
R20-21	var, cermet 200 Ω \pm 10%	2	62-222-1	73138	2100-2413	1
R22-24	fxd, film 3.57K Ω \pm 1%, 1/8W	3	Type CEA T-O	07716	0698-3496	1
R25, 26	fxd, comp 200 Ω \pm 5%, 1/4W	2	CB-2015	01121	0683-2015	1
R27	fxd, film 6K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-3476	1
R28	fxd, film 2.37K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-3150	1
R29	fxd, film 4K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-5808	1
R30	fxd, film 121 Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0757-0069	1
R31, 32	fxd, film 432K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0757-0480	1
R33, 34	fxd, film 1K Ω \pm 1%, 1/8W	4	Type CEA T-O	07716	0757-0280	1
R35, 36	fxd, film 10K Ω \pm 1%, 1/8W	3	Type CEA T-O	07716	0757-0442	1
R37	fxd, film 121 Ω \pm 1%, 1/8W		Type CEA T-O	07716	0757-0069	
R38	fxd, film 750 Ω \pm 5% 1/4W	2	CB-7515	01121	0683-7515	1
R39	fxd, film 1K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0757-0280	
R40	fxd, comp 2.4K Ω \pm 5%, 1/4W	1	CB-2425	01121	0683-2425	1
R41	fxd, comp 5.1K Ω \pm 5%, 1/4W		CB-5125	01121	0683-5125	
R42	fxd, film 8.2K Ω \pm 2%, 1/8W	2	Type CEA T-O	07716	0757-0946	1

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	TQ	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A6R43	fxd, film 1K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0757-0280	
R44	fxd, film 102 Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0406	1
R45	fxd, film 6.2K Ω \pm 2%, 1/8W		Type CEA T-O	07716	0757-0946	
R46	fxd, film 11K Ω \pm 1% 1/8W	1	Type CEA T-O	07716	0757-0443	1
R47	fxd, film 1.3K Ω \pm 1%, 1/4W	1	Type CEB T-O	07716	0757-0735	1
R48	fxd, film 1.21K Ω \pm 1%, 1/4W	1	Type CEB T-O	07716	0757-0734	1
R49	fxd, comp 5.1K Ω \pm 5%, 1/4W		CB-5125	01121	0683-5125	
R50-52	fxd, comp 10K Ω \pm 5%, 1/4W	9	CB-1035	01121	0683-1035	1
R53, 54	fxd, comp 20K Ω \pm 5%, 1/4W		CB-2035	01121	0683-2035	
R55, 56	fxd, comp 10K Ω \pm 5%, 1/4W		CB-1035	01121	0683-1035	
R57, 58	fxd, comp 2K Ω \pm 5%, 1/4W	3	CB-2025	01121	0683-2025	1
R59	fxd, comp 5.1K Ω \pm 5%, 1/4W		CB-5125	01121	0683-5125	
R60	fxd, comp 10K Ω \pm 5%, 1/4W		CB-1035	01121	0683-1035	
R61-63	fxd, comp 20K Ω \pm 5%, 1/4W		CB-2035	01121	0683-2035	
R64, 65	fxd, comp 5.1K Ω \pm 5%, 1/4W		CB-5125	01121	0683-5125	
R66	fxd, comp 100 Ω \pm 5%, 1/4W	1	CB-1015	01121	0683-1015	1
R67	fxd, comp 1K Ω \pm 5%, 1/4W	2	CB-1025	01121	0683-1025	1
R73	fxd, comp 4.7K Ω \pm 5%, 1/4W	2	CB-4725	01121	0683-4725	1
R74	fxd, comp 20K Ω \pm 5%, 1/4W		CB-2035	01121	0683-2035	
R75	fxd, comp 6.2K Ω \pm 5%, 1/4W	3	CB-6225	01121	0683-6225	1
R76	fxd, comp 100K Ω \pm 5%, 1/4W	2	CB-1045	01121	0683-1045	1
R77	fxd, comp 5.6K Ω \pm 5%, 1/4W	1	CB-5625	01121	0683-5625	
R78	fxd, comp 4.7K Ω \pm 5%, 1/4W		CB-4725	01121	0683-4725	
R79	fxd, comp 2K Ω \pm 5%, 1/4W		CB-2025	01121	0683-2025	
R80	fxd, comp 20K Ω \pm 5%, 1/4W		CB-2035	01121	0683-2035	
R81	fxd, comp 2.7K Ω \pm 5%, 1/4W	1	CB-2725	01121	0683-2725	1
R82	fxd, comp 1K Ω \pm 5%, 1/4W		CB-1025	01121	0683-1025	
R83	fxd, comp 200K Ω \pm 5%, 1/4W	1	CB-2045	01121	0683-2045	1
R84	fxd, comp 5.1K Ω \pm 5%, 1/4W		CB-5125	01121	0683-5125	
R85	fxd, comp 33K Ω \pm 5%, 1/4W	1	CB-3335	01121	0683-3335	1
R86	fxd, comp 82K Ω \pm 5%, 1/4W	1	CB-8235	01121	0683-8235	1
R87	fxd, comp 3.6K Ω \pm 5%, 1/4W	1	CB-3625	01121	0683-3625	1
R88	fxd, comp 9.1K Ω \pm 5%, 1/4W	1	CB-9125	01121	0683-9125	1
R89, 90	fxd, comp 6.2K Ω \pm 5%, 1/4W		CB-6225	01121	0683-6225	
R91	fxd, comp 100 Ω \pm 5%, 1/4W		CB-1045	01121	0683-1045	
R92	fxd, comp 12K Ω \pm 5%, 1/4W	1	CB-1235	01121	0683-1235	1
R93, 94, 95	fxd, comp 20K Ω \pm 5%, 1/4W		CB-2035	01121	0683-2035	
R96	fxd, comp 1.3K Ω \pm 5%, 1/2W		EB-1325	01121	0686-1325	
R97	fxd, comp 51K Ω \pm 5%, 1/4W	1	CB-5135	01121	0683-5135	1
R98	fxd, comp 750 Ω \pm 5%, 1/4W		CB-7515	01121	0683-7515	
R99	fxd, comp 82 Ω \pm 5%, 1/4W		CB-8205	01121	0683-8205	
R100, 101	fxd, comp 10K Ω \pm 5%, 1/4W		CB-1035	01121	0683-1035	
R102	fxd, ww 390 Ω \pm 5%, 3W	1	242E	56289	0811-1799	1
R103	fxd, comp 10K Ω \pm 5%, 1/4W		CB-1035	01121	0683-1035	
R105	fxd, comp 10Meg \pm 5%, 1/4W	1	CB-1065	01121	0683-1065	1
R106	fxd, film 10K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0757-0442	
R107	fxd, comp 5.6Meg \pm 5%, 1/4W	1	CB-5655	01121	0683-5655	1
R108	var, cermet 20K Ω \pm 10%	1	62-228-1	73138	2100-2514	1
R109	fxd, ww 75 Ω \pm 5%, 5W	1	243E	56289	0812-0097	1
VR1	Diode, zener 4.99V 400mW	1		28480	1902-3092	1
VR2	Diode, zener 12.4V 400mW	1		28480	1902-3185	1
VR4-6	Diode, zener 4.22V 400mW	3		28480	1902-3070	3
Z1	Hybrid Resistive Network IC	1		28480	1810-0041	1
Z2	Quad 4-Bit Bistable Latch IC	1	SN7475	01295	1820-0876	1

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	TQ	MFR. PART NO.	MFR. CODE	HP PART NO.	RC
A623	Operational Amplifier IC	1	SL8641	27014	1820-0223	1
Z4	Dual Operational Amp IC	1		28480	1820-0002	1
A7	Amplifier Plug-In Board	1		28480	06130-60024	
C1	fxd, mica 330pF 500Vdc	2	RCM15E331J	04062	0140-0168	1
C2,3	fxd, mylar .22µF 80Vdc	2	192P2249R8	56289	0160-2453	1
C4	fxd, elect. 1µF 35Vdc	1	150D105X9035A2	56289	0180-0291	1
C5,6	fxd, mylar .0022µF 200V	2	192P22292	55289	0160-0154	1
C7,8	fxd, mylar .1µF 200Vdc	2	192P10492	56289	0160-0168	1
C9	fxd, mica 330pF 500Vdc		RCM15E331J	04062	0140-0168	
C10,11	fxd, mica 82pF 300Vdc	2	RDM15E820J3C	04062	0140-0193	1
C12	fxd, ceramic .001µF 500Vdc	5	40C88A1CDH	56289	0160-3398	1
C14	fxd, mylar .01µF 200Vdc	3	192P10392	56289	0160-0161	1
C15	fxd, ceramic .001µF 500Vdc		40C88A1CDH	56289	0160-3398	
C17	fxd, mylar .01µF 200Vdc		192P10392	56289	0160-0161	
C18	fxd, tant. .47µF 35Vdc	1	150D474X9035A2-DYS	56289	0180-0376	1
C19	fxd, ceramic .001µF 500Vdc		40C88A1CDH	56289	0160-3398	
C20	fxd, ceramic 100pF 1KVdc	1	DD-101	71590	0160-2061	1
C21,22	fxd, ceramic .001µF 500Vdc		40C88A1CDH	56289	0160-3398	
C23	fxd, mylar .01µF 200Vdc		192P10392	56289	0160-0161	
C24,25	fxd, ceramic .47µF 25Vdc	2	5C11B7	56289	0160-0174	1
C26	fxd, ceramic 0.001µF 1KVdc	1	C067B102E102ZS26	56289	0150-0050	1
CR1-15	Diode, Si 15V 400mW	24		28480	1901-0461	12
CR16,17	Stabistor, Si 10prv 400mW	5		28480	1901-0460	5
CR18-20	Diode, Si 15V 400mW			28480	1901-0461	
CR21	Stabistor, Si 10prv 400mW			28480	1901-0460	
CR22,23	Diode, Si 200V 250mW	2		28480	1901-3033	2
CR24-27	Diode, Si 15V 400mW			28480	1901-0461	
CR28,29	Diode, Si 200mA 75V	8		28480	1901-0050	5
CR30,31	Diode, Si 15V 400mW			28480	1901-0461	
CR32,33	Stabistor, Si 10prv 400mW			28480	1901-0460	
CR34	Diode, Si 15V 400mW			28480	1901-0461	
CR35-40	Diode, Si 200mA 75V			28480	1901-0050	
K1	Reed Relay and Coil Assembly	1		28480	5080-7127	1
	Reed Relay (Part of A7K1)	1	DRS-2	12617	0490-0727	1
	Coil (Part of A7K1)	1	SF-12P	71707	0490-0728	1
K2	Reed Relay	1		28480	0490-0399	1
Q1	Diff. Amp, NPN	1		28480	1854-0221	1
Q2	Diff. Amp, NPN	1		28480	1854-0229	1
Q3,4	SS NPN Si	4	2N3417	03508	1854-0087	4
Q5	SS PNP Si	1		28480	1853-0010	1
Q6	SS PNP Si	5		28480	1853-0037	5
Q7	Power NPN Si	7		28480	1854-0095	5
Q8	SS NPN Si	5		28480	1854-0071	5
Q9	SS PNP Si	5		28480	1853-0099	5
Q10,11	Power NPN Si			28480	1854-0095	
Q12,13	SS PNP Si			28480	1853-0037	
Q14,16	Power NPN Si			28480	1854-0095	
Q16,17	SS PNP Si			28480	1853-0037	
Q18,19	SS NPN Si			28480	1854-0071	
Q20-22	SS PNP Si			28480	1853-0099	
Q23	SS NPN Si			28480	1854-0071	
Q24,25	SS NPN Si		2N3417	03508	1854-0087	
Q26	SS PNP Si	1		28480	1853-0041	1
Q27	SS NPN Si			28480	1854-0071	

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	TQ	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A7Q28	SS NPN SI	1		28480	1854-0244	1
Q29	SS PNP SI			28480	1853-0099	
Q30, 31	Power NPN SI			28480	1854-0095	
R1	fxd, film 1M Ω \pm 1%, 1/4W	1	Type CEB T-O	07716	0757-0344	1
R2	fxd, film 45K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-5091	1
R3	fxd, film 619 Ω \pm 1%, 1/4W	1	Type CEB T-O	07716	0757-0728	1
R4, 5	fxd, film 200K Ω \pm 1%, 1/8W	2	Type CEP T-O	07716	0757-0472	1
R6	fxd, comp 1K Ω \pm 5%, 1/2W	6	EB-1025	01121	0686-1025	2
R7	fxd, film 4.75K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0757-0437	1
R8	fxd, film 118K Ω \pm 1%, 1/8W	1	Type CEA T-O	07716	0698-3265	1
R9	var. ww 100 Ω \pm 5%	1	Type 100	11502	2100-1450	1
R10, 11	fxd, film 21.5 Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0698-3430	1
R12, 13	fxd, film 43K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0698-5090	1
R14, 15	fxd, film 12K Ω \pm 1%, 1/8W	3	Type CEA T-O	07716	0698-5068	1
R16	fxd, comp 1K Ω \pm 5%, 1/2W		EB-1025	01121	0686-1025	
R17, 18	fxd, film 510 Ω \pm 1%, 1/4W	2	Type CEB T-O	07716	0698-5145	1
R19	fxd, comp 100 Ω \pm 5%, 1/2W	3	EB-1015	01121	0686-1015	1
R20	fxd, film 12K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0698-5088	
R21	fxd, comp 1.3K Ω \pm 5%, 1/2 W	3	EB-1325	01121	0686-1325	1
R22, 23	fxd, comp 51 Ω \pm 5%, 1/2W	2	EB-5105	01121	0686-5105	1
R24	fxd, comp 5.6K Ω \pm 5%, 1/2W	1	EB-5625	01121	0686-5625	1
R25	fxd, comp 560 Ω \pm 5%, 1/2W	3	EB-5615	01121	0686-5615	1
R26	fxd, comp 510 Ω \pm 5%, 1/2W	1	EB-5115	01121	0686-5115	1
R27	fxd, comp 3K Ω \pm 5%, 1/2W	1	EB-3025	01121	0686-3025	1
R28	fxd, comp 5.1K Ω \pm 5%, 1/2W	4	EB-5125	01121	0686-5125	1
R29	fxd, comp 1.5K Ω \pm 5%, 1/2W	3	EB-1525	01121	0686-1525	1
R30	fxd, comp 2.2K Ω \pm 5%, 1/2W	1	EB-2225	01121	0686-2225	1
R31	fxd, comp 2K Ω \pm 5%, 1/2W	4	EB-2025	01121	0686-2025	1
R32	fxd, comp 8.2K Ω \pm 5%, 1/2W	2	EB-8225	01121	0686-8225	1
R33	fxd, comp 2K Ω \pm 5%, 1/2W		EB-2025	01121	0686-2025	
R34	fxd, comp 8.2K Ω \pm 5%, 1/2W		EB-8225	01121	0686-8225	
R35	fxd, comp 120K Ω \pm 5%, 1/2W	2	EB-1245	01121	0686-1245	1
R36	fxd, comp 910 Ω \pm 5%, 1/2W	1	EB-9115	01121	0686-9115	1
R37	fxd, comp 120K Ω \pm 5%, 1/2W		EB-1245	01121	0686-1245	
R38	fxd, met. oxide 18K Ω \pm 5%, 2W	1	Type C42S	16299	0764-0006	1
R39	fxd, comp 200 Ω \pm 5%, 1/2W	6	EB-2015	01121	0686-2015	1
R40	fxd, comp 12K Ω \pm 5%, 1/2W	1	EB-1235	01121	0686-1235	1
R41	fxd, comp 18 Ω \pm 5%, 1/2W	2	EB-1805	01121	0686-1805	1
R42	fxd, comp 1K Ω \pm 5%, 1/2W		EB-1025	01121	0686-1025	
R43	fxd, comp 200 Ω \pm 5%, 1/2W		EB-2015	01121	0686-2015	
R44	fxd, comp 18 Ω \pm 5%, 1/2W		EB-1805	01121	0686-1805	
R45	fxd, comp 82K Ω \pm 5%, 1/2W	2	EB-8235	01121	0686-8235	1
R46	fxd, comp 62K Ω \pm 5%, 1/2W	2	EB-6235	01121	0686-6235	1
R47	fxd, comp 200 Ω \pm 5%, 1/2W		EB-2015	01121	0686-2015	
R48	fxd, met. oxide 15K Ω \pm 5%, 2W	1	Type C42S	16299	0698-3647	1
R49	fxd, comp 62K Ω \pm 5%, 1/2W		EB-6235	01121	0686-6235	
R50	fxd, comp 82K Ω \pm 5%, 1/2W		EB-8235	01121	0686-8235	
R51, 53	fxd, comp 200 Ω \pm 5%, 1/2W		EB-2015	01121	0686-2015	
R54	fxd, comp 5.1K Ω \pm 5%, 1/2W		EB-5125	01121	0686-5125	
R55	fxd, comp 100 Ω \pm 5%, 1/2W		EB-1015	01121	0686-1015	
R56	fxd, film 1.50K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0757-0427	1
R57	fxd, comp 15K Ω \pm 5%, 1/2W	2	EB-1535	01121	0686-1535	1
R58	fxd, comp 2K Ω \pm 5%, 1/2W		EB-2025	01121	0686-2025	
R59	fxd, comp 1.5K Ω \pm 5%, 1/2W	2	EB-1525	01121	0686-1525	1

Table 6-4, Replaceable Parts

REF. DESIG.	DESCRIPTION	TQ	MFR. PART NO.	MFR. CODE	HP PART NO.	RB
A7R60	fxd, film 1.50K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0757-0427	
R61	fxd, comp 15K Ω \pm 5%, 1/2W		EB-1535	01121	0686-1535	
R62	fxd, comp 1K Ω \pm 5%, 1/2W		EB-1025	01121	0686-1025	
R64	fxd, comp 200 Ω \pm 5%, 1/2W		EB-2015	01121	0686-2015	
R65	fxd, comp 5.1K Ω \pm 5%, 1/2W		EB-5125	01121	0686-5125	
R66	fxd, comp 100 Ω \pm 5%, 1/2W		EB-1015	01121	0686-1015	
R67	fxd, comp 1.5K Ω \pm 5%, 1/2W		EB-1525	01121	0686-1525	
R68	fxd, comp 27K Ω \pm 5%, 1/2W	1	EB-2735	01121	0686-2735	1
R69	fxd, comp 39K Ω \pm 5%, 1/2W	1	EB-3935	01121	0686-3935	1
R70	fxd, comp 150 Ω \pm 5%, 1/2W	1	EB-1515	01121	0686-1515	1
R71	fxd, comp 4.3K Ω \pm 5%, 1/2W	3	EB-4325	01121	0686-4325	1
R72	fxd, comp 0K Ω \pm 5%, 1/2W	2	EB-1035	01121	0686-1035	1
R73	fxd, comp 4.3K Ω \pm 5%, 1/2W		EB-4325	01121	0686-4325	
R74	fxd, comp 750 Ω \pm 5%, 1/2W	2	EB-7515	01121	0686-7515	1
R75	fxd, comp 7.5K Ω \pm 5%, 1/2W	2	EB-7525	01121	0686-7525	1
R76	fxd, comp 560 Ω \pm 5%, 1/2W		EB-5615	01121	0686-5615	
R77	fxd, film 6.2K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0698-5087	1
R78	fxd, film 4.53K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0698-4443	1
R79	fxd, comp 4.3K Ω \pm 5%, 1/2W		EB-4325	01121	0686-4325	
R80	fxd, comp 750 Ω \pm 5%, 1/2W		EB-7515	01121	0686-7515	
R81	fxd, comp 7.5K Ω \pm 5%, 1/2W		EB-7525	01121	0686-7525	
R82	fxd, comp 560 Ω \pm 5%, 1/2W		EB-5615	01121	0686-5615	
R83	fxd, film 6.2K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0698-5087	
R84	fxd, film 4.53K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0698-4443	
R85	var, ww 200 Ω \pm 10%	1	Type 500	11502	2130-1771	1
R86	fxd, ww 89.90K Ω \pm .1%, 5ppm	1	Type 7009	01686	0811-2578	1
R87	fxd, ww 10.0K Ω \pm .1%, 5ppm	1	Type E30	01686	0811-1954	1
R88	fxd, comp 9.1K Ω \pm 5%, 1/2W	1	EB-9125	01121	0686-9125	1
R89	fxd, comp 1.6K Ω \pm 5%, 1/2W	1	EB-1625	01121	0686-1625	1
R90	fxd, comp 5.1K Ω \pm 5%, 1/2W		EB-5125	01121	0686-5125	
R92	fxd, comp 10K Ω \pm 5%, 1/2W		EB-1035	01121	0686-1035	
R93	fxd, comp 3.9K Ω \pm 5%, 1/2W	1	EB-3925	01121	0686-3925	1
R94	fxd, comp 13K Ω \pm 5%, 1/2W	1	EB-1335	01121	0686-1335	1
R108, 109	fxd, comp 1K Ω \pm 5%, 1/2W		EB-1025	01121	0686-1025	
R110	fxd, film 7.5K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0757-0440	1
R111	fxd, film 1.65K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0698-4428	1
R112	fxd, comp 2K Ω \pm 5%, 1/2W		EB-2025	01121	0686-2025	
R113	fxd, film 249K Ω \pm 1%, 1/8W	2	Type CF T-O	07716	0757-0270	1
R114, 115	fxd, comp 1.3K Ω \pm 5%, 1/2W		EB-1325	01121	0686-1325	
R116	fxd, film 1.69K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0698-4428	
R117	fxd, film 249K Ω \pm 1%, 1/8W		Type CEA T-O	07716	0757-0270	
R118, 119	fxd, film 110K Ω \pm 1%, 1/8W	2	Type CEA T-O	07716	0757-0466	1
R120	fxd, film 7.5K Ω \pm 1% 1/8W		Type CEA T-O	07716	0757-0440	
R121	fxd, met. oxide 180 Ω \pm 5%, 1/2W	1	RG-42	07716	0698-3626	1
T1	Toroidal Transformer 1:1:1	1		28480	9100-2185	1
VR1,2	Diode, zener 6.8V 400mW	4		28480	1902-0048	4
VR3	Diode, zener 56.2V \pm 5%, 1W	1		28480	1902-0597	1
VR4	Diode, zener 61.9V \pm 5%, 1W	2		28480	1902-0660	2
VR5,6	Diode, zener 9.4V 500mW	2	1N2163A	04713	1902-0763	2
VR7	Diode, zener 7.5V 400mW	1		28480	1902-0064	1
VR8	Diode, zener 5.62V 400mW	1		28480	1902-3104	1
VR9	Diode, zener 61.9V \pm 5%, 1W			28480	1902-0660	
VR10,11	Diode, zener 6.8V 400mW			28480	1902-0048	

Table G-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	IIP PART NO.	RS
	CHASSIS ELECTRICAL PARTS					
C1,2	fxd, elect, 5,600 μ F 25Vdc	2	32D40018	56288	0180-1921	1
C3	fxd, elect, 4,000 μ F 15Vdc	1	602D4026015AA2A	56288	0180-2385	1
C6,7	fxd, elect, 3,000 μ F 80Vdc	2	36D302308AC2	56288	0180-2193	1
C8	fxd, mylar 0.01 μ F 300Vdc	1	192P10392	56288	0160-0161	1
DS1	Lamp, glow 115V	1	NE-2H	03508	2140-0015	1
F1	Fuse, 2A 250V,T	1	MDX-2A	71400	2110-0303	5
J1	Jack, Input	1		28480	1251-0087	1
M1	Voltmeter, Dual, 0- \pm 60V, 0- \pm 10V	1		28480	1120-1143	1
M2	Ammeter, Dual 0- \pm 1.2A, 0- \pm 0.3A	1		28480	1120-1145	1
P1	Plug, Input	1		28480	1251-0086	1
Q1,2	Power NPN Si	2	2N3714	04713	1954-0338	2
Q3,4	Power PNP Si	2	2N3790	04713	1953-0095	2
S1	Switch, AC Line	1		28480	3101-1055	1
S2	Switch, Range, Current	1		28480	3100-1916	1
S3	Switch, Range, Voltage	1		28480	3100-1919	1
T3	Power Transformer	1		28480	06130-80091	1
Z1	+5V Regulator, IC	1	SL10236	27014	1920-0430	1
	MECHANICAL					
	A1 Input Board					
	Card Extractor Handle	1		28480	5081-4001	
	Roll Pin	1	52012062-250	72962	1480-0059	1
	A2 Logic Board					
	Card Extractor Handle	1		28480	5081-4903	
	Roll Pin	1	52012062-250	72962	1480-0059	1
	IC Socket, 16-pin (Z1-4 or Z9-12)	4	516-AG5D-3R	91506	1200-0767	1
	IC Socket, 14-pin (Z5,Z6)	2	314-AG5D-3R	91506	1200-0768	1
	A3 D/A Board					
	Card Extractor Handle	1		28480	5081-4905	
	Roll Pin	1	52012062-250	72962	1480-0059	1
	Heat Dissipator, Q31	1	NF-207	05820	1205-0033	1
	A5 Control Board					
	Card Extractor Handle	1		28480	5081-4906	
	Roll Pin	1	52012062-250	72962	1480-0059	1
	Heat Dissipator (Q34)	1	NF-207	05820	1205-0033	1
	A7 Amplifier Board					
	Card Extractor Handle	1		28480	06130-80001	
	Roll Pin	1	52012062-250	72962	1480-0059	1
	Heat Dissipator (Q6,7, 11, 13, 15, 17, 26, 28)	8	NF-207	05820	1205-0033	1
	Front Panel Assembly					
	Front Panel (loaded)	1		28480	06130-60011	
	Front Panel (lettering)	1		28480	06130-60010	
	Meter Bezel	2		28480	4040-0297	1
	Meter Spring	8		28480	1460-0256	2
	Base, Indicator DS1	1		28480	5040-0305	1
	Lens, Indicator DS1	1		28480	5040-0234	1
	Knob, Black, Pointer	2		28480	0370-1099	1

Table 6-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
	MECHANICAL					
	Front Door Assembly	1		28480	06130-60009	
	Door, Blank (Lettering Only)	1		28480	06130-00012	
	Spring, Door	1		28480	06130-00011	1
	Lens, Door	1		28480	5040-0234	1
	Latch, Door	1	27-10-301-10	94222	1390-0037	1
	Rear Panel Assembly	1		28480	5060-7902	
	Rear Panel	1		28480	5000-9400	
	Barrier Strip, 10-Terminal	1		75382	0360-1156	1
	Jumper, Barrier Strip	3		28480	0360-1143	1
	Heat Sink, Rear	2		28480	5020-8068	
	Cover, Heat Sink	2		28480	5000-9442	
	Spacer, Heat Sink Cover, Hex, 8-32 x 5/8 long	4		28480	0380-0719	
	AC Line Cord	1		28480	8120-0050	1
	Strain Relief Bushing, Line Cord	1		28480	0400-0013	1
	Shoulder Washer, Gray, Q1-Q4, Mounting Screws	8		28480	2190-0491	6
	Bushing, Transistor Pins, Q1-Q4	8		28480	0340-0166	6
	Bushing, Transistor Screws, Q1-Q4	8		28480	0340-0168	6
	Insulator, Mica, Q1-Q4	4		28480	0340-0174	4
	Hinge, Plastic	2		28480	5040-1449	
	Bracket, Hinge	2		28480	5000-6208	
	Fuse Holder	1	342.014	75915	1400-0084	1
	Hex. Nut, Fuse Holder	1		28480	2950-0038	1
	Lockwasher, Fuse Holder	1		28480	2190-0037	1
	Neoprene Washer, Fuse Holder	1		28480	1400-0090	1
	Rear Chassis	1		28480	5000-6206	
	Spacer, Rear Chassis, Hex 8-32 x 7/8 long	4		28480	0380-0392	
	Cover, Bottom	1		28480	5000-9005	
	Cover, Top	1		28480	5000-9806	
	Side Frame	2		28480	5060-0731	
	Side Cover, Front	2		28480	5000-8703	
	Side Cover, Rear	2		28480	5000-8701	
	Side Trim, Fluted, Adhesive Back	2		28480	5000-0051	
	Handle Assembly, Side	2		28480	5060-0222	1
	Retainer, Side Handle, Sheet Metal	2		28480	5060-0766	1
	Chassis, Power Supply, U- Shape, Aluminum Sheet Metal	1		28480	5000-6205	
	Chassis, Plug-In Card, Aluminum Sheet Metal	1		28480	5000-6204	
	Guide Rail, Plug-In Card, Plastic, Right	5		28480	5040-1419	
	Guide Rail, Plug-In Card, Plastic, Left	5		28480	5040-1420	

Table G-4. Replaceable Parts

REF. DESIG.	DESCRIPTION	TQ	MFR. PART NO.	MFR. CODE	IIP PART NO.	RS
	MECHANICAL					
	Shoulder Washer, Plug-In Card Chassis	8		28480	2190-0492	
	Spacer, P.C. Guide 3/8" O.D., #10 C.L.	12	9319-A-194	06540	0380-0471	
	Clamp Tube, C1, C2	2		28480	5000-6276	
	MISCELLANEOUS					
	Clamp, 1/4" Dia.	3	T4-4	79307	1400-0330	1
	Clamp, 2" Dia., C3	1	4586-2B	56289	0180-0078	1
	Clamp, 1-3/8" Dia., C6, C7	2	4586-97A	56289	0160-2149	1
	Foot Assembly	5		28480	5060-0767	1
	Stand, Tilt	1		28480	1490-0030	1
	Fastener	4	C17859632-24D	89032	0590-0053	1
	Fastener	9	C8022632-24B	89032	0590-0710	2
	Rack Mounting Kit (Includes Rack Ears, Trim, and Screws)	1		28480	5060-8740	
	Packing Carton	1		28480	9211-1180	
	Floater Pad, Packing Carton	2		28480	9220-1400	
	Extender Assembly, Plug-In Board	1		28480	5060-7948	
	Printed Circuit Board	1		28480	5020-8040	
	Printed Circuit Board Connector	1	251-20-3C-390	71785	1251-0495	
	Epoxy Plate	1		28480	5020-5728	

SECTION VII CIRCUIT DIAGRAMS

7-1 INTRODUCTION

7-2 This section contains the circuit diagrams necessary for the operation and maintenance of Model 6130C Digital Voltage Source.

7-3 OVERALL BLOCK DIAGRAM

7-4 This diagram, Figure 7-1, shows the relationship between the instrument assemblies and ties the schematic diagrams together. A timing diagram is provided in Figure 7-1 to aid in the understanding of the operation of the instrument.

7-5 COMPONENT LOCATION ILLUSTRATIONS

7-6 The component location diagrams show the physical location of parts mounted on each assembly. They are included on the schematic diagrams where they apply or on the rear of the previous schematic. Thus, the schematic diagram is unfolded to the right and component location dia-

gram is unfolded to the left.

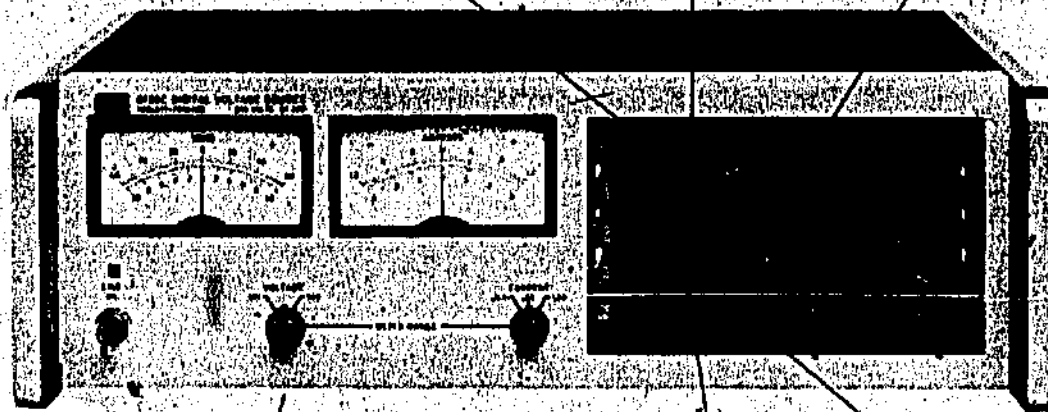
7-7 SCHEMATIC DIAGRAMS

7-8 The circuits are functionally separated and included on a series of schematic diagrams, Figure 7-2, Sheets 1 through 4. Voltage Processing Circuits are contained on Sheet 1. The Current Latch Circuits are contained on Sheet 2. The signals from Sheets 1 and 2 are connected to the Power Amplifier, Sheet 3.

7-9 The Power Distribution Schematic Diagram, Figure 7-2, Sheet 4, illustrates the input ac, dc power supplies, and the distribution of dc voltages throughout the unit.

7-10 Test points (circled numbers) appear throughout the schematics. These points coincide with the test points on the component location diagrams and are referred to throughout the text.

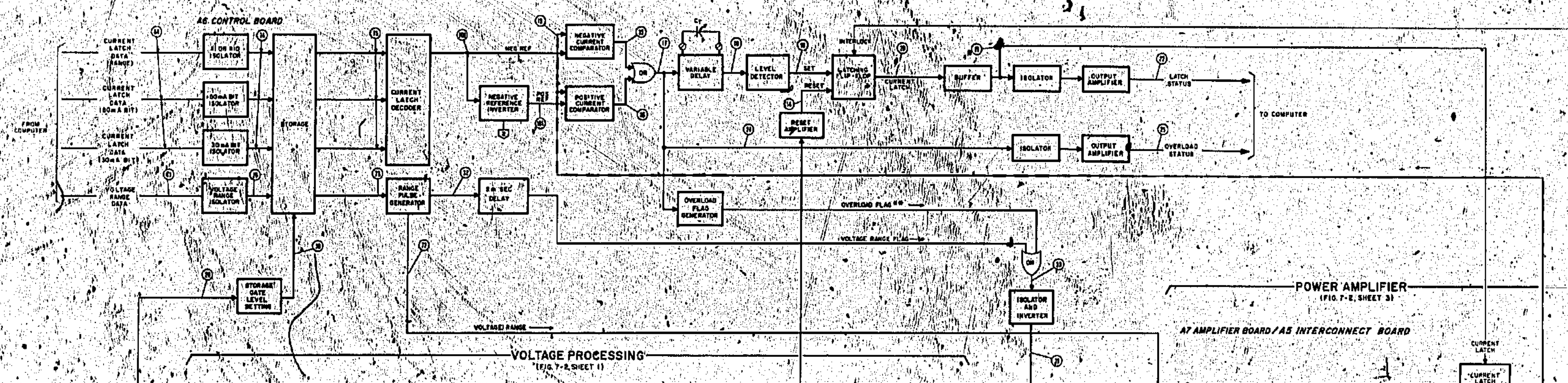
A3 D/A CONVERTER BOARD A2 LOGIC BOARD A1 INPUT BOARD



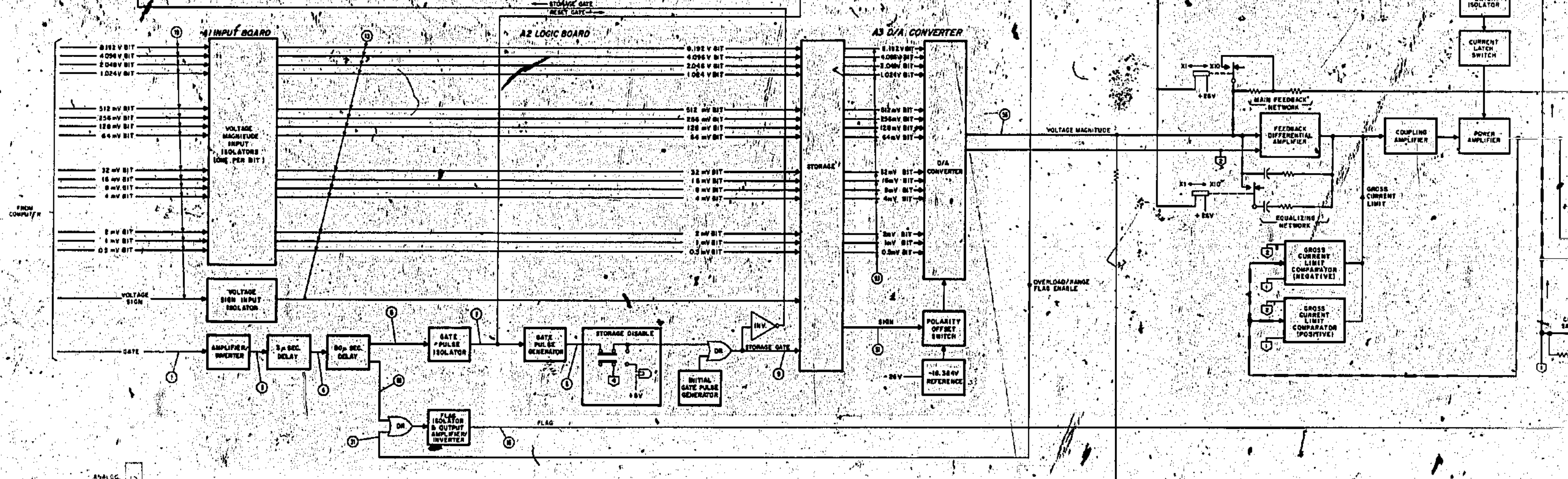
A4 POWER SUPPLY BOARD (INSIDE UNIT) A6 CONTROL BOARD A7 AMPLIFIER BOARD

Subassembly Location

CURRENT LATCH AND VOLTAGE RANGE PROCESSING
(FIG. 7-2, SHEET 2)



VOLTAGE PROCESSING
(FIG. 7-2, SHEET 1)



POWER AMPLIFIER
(FIG. 7-2, SHEET 3)

A7 AMPLIFIER BOARD / A5 INTERCONNECT BOARD

CURRENT SAMPLING

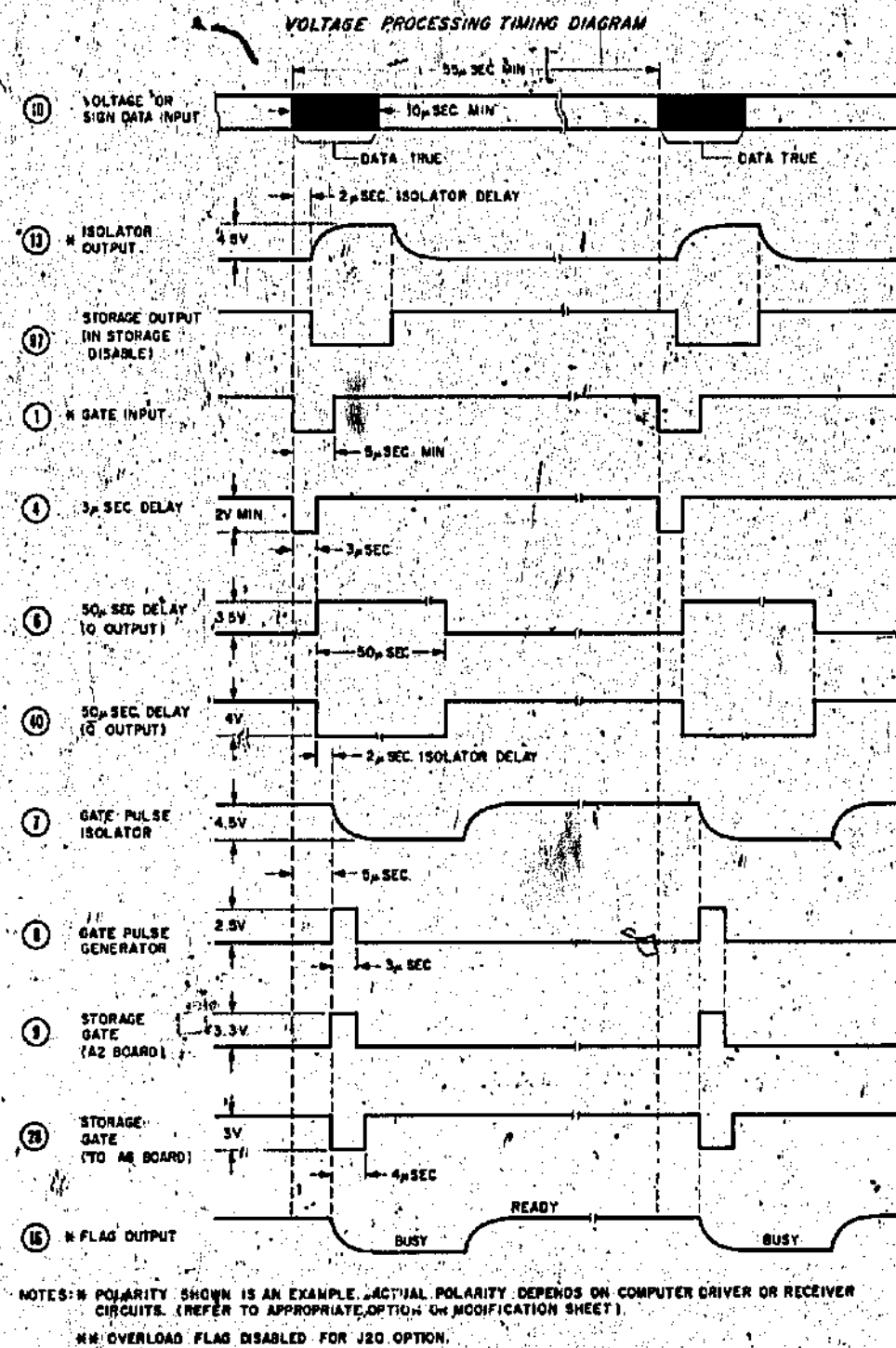
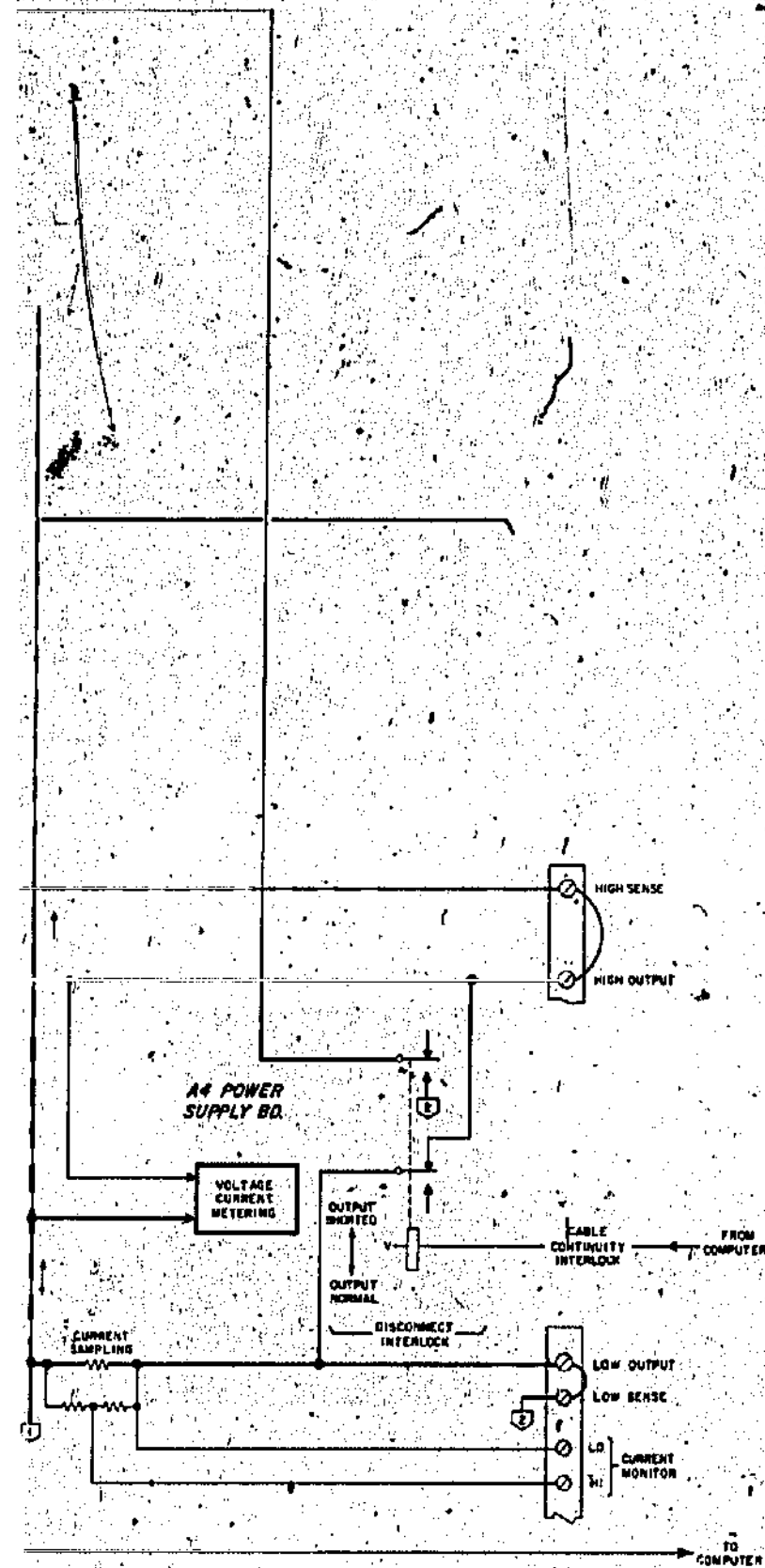
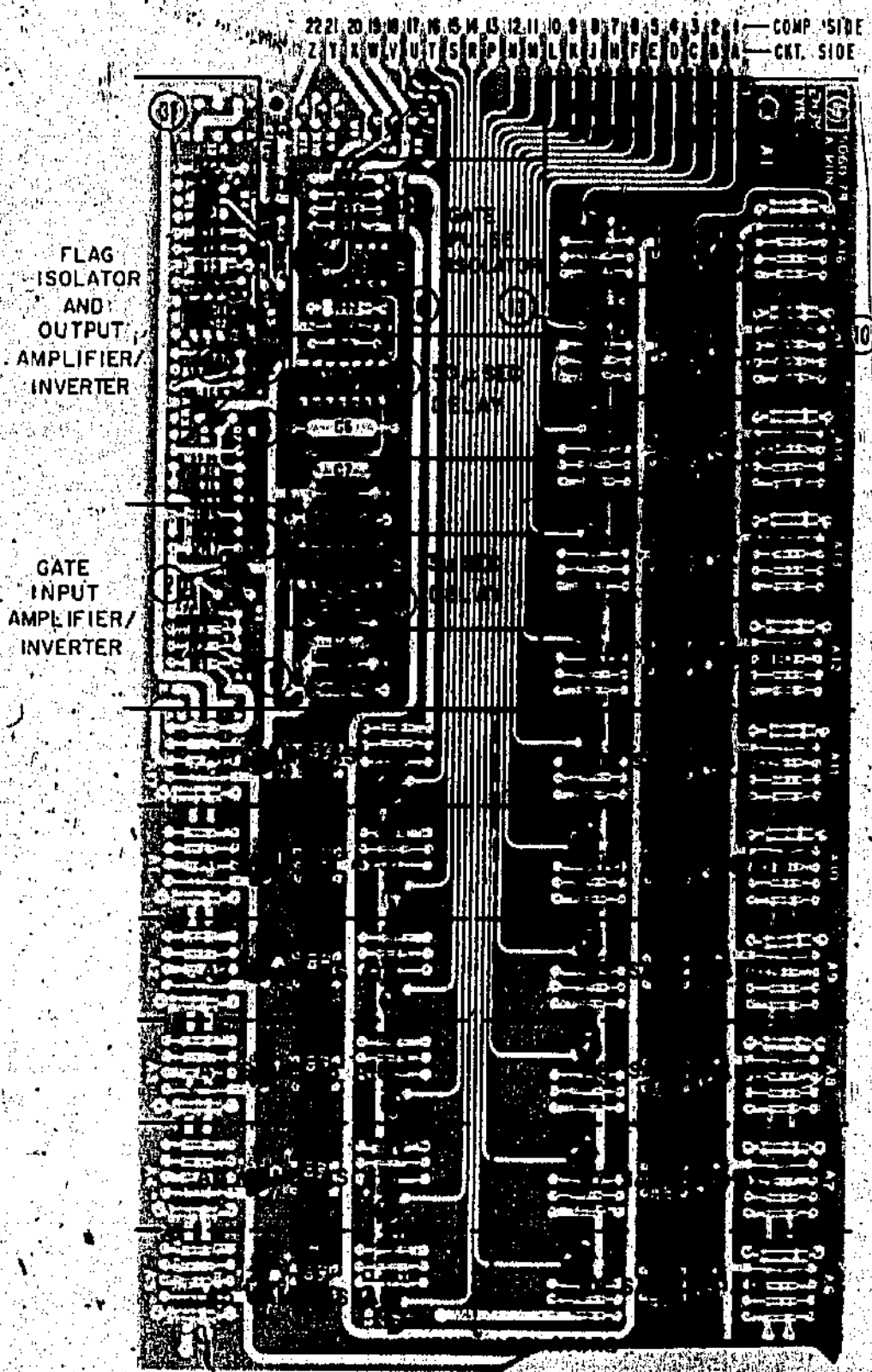
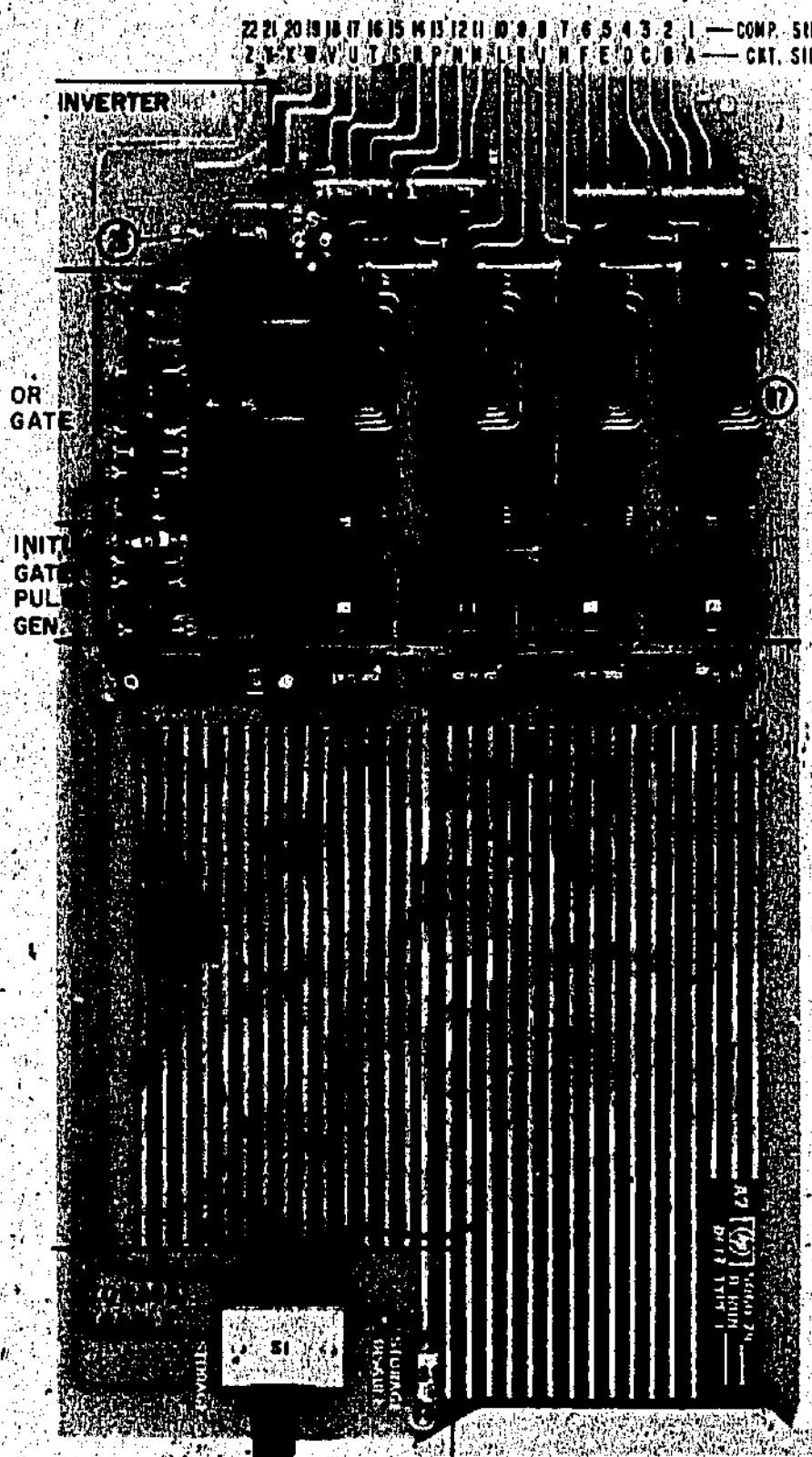


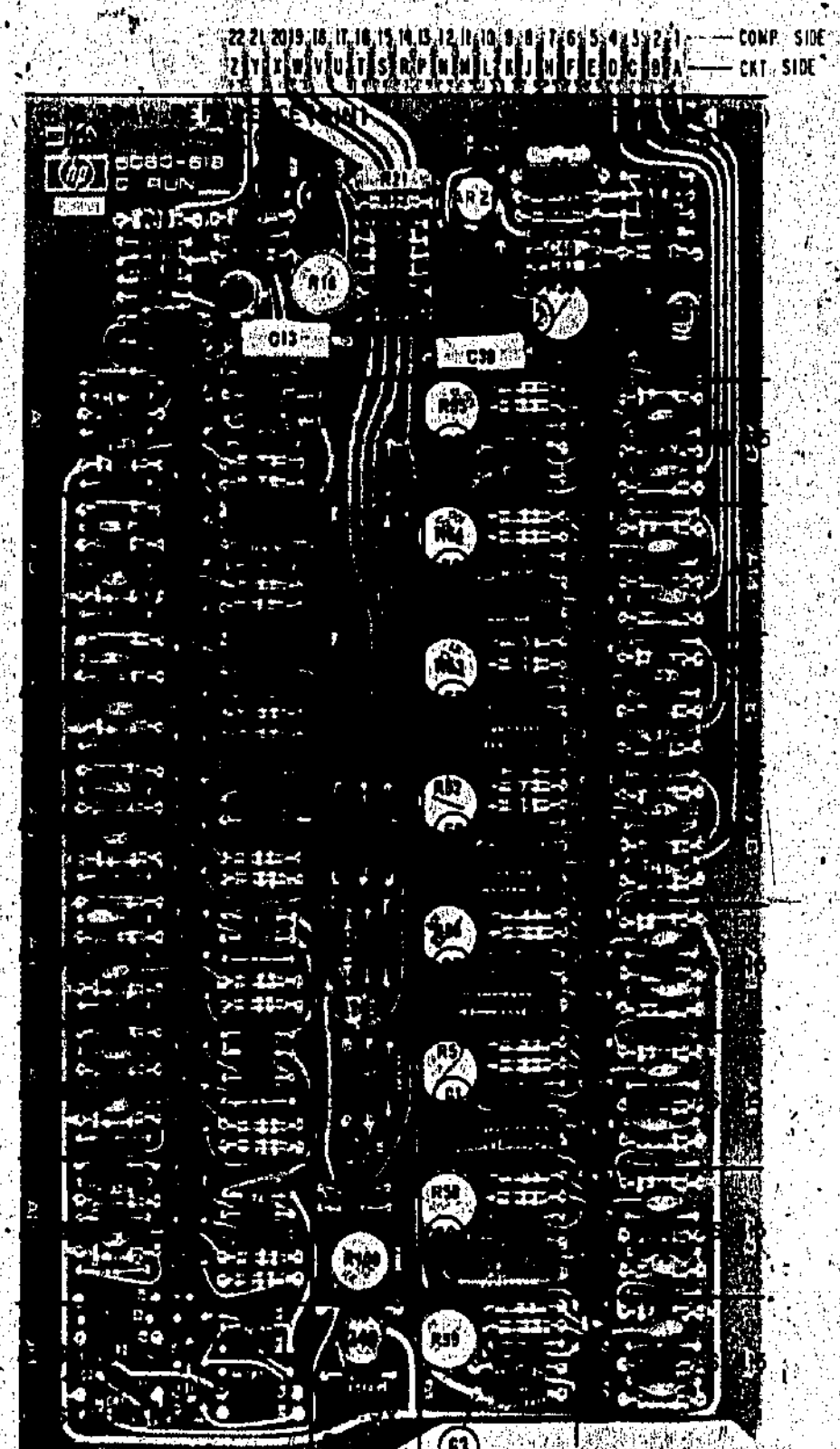
Figure 7-1. Overall Block and Timing Diagram



A1 Input Board, Component Location


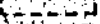





A2 Logic Board, Component Location



A3 D/A Board, Component Location

NOTES

1. ALL RESISTORS ARE IN OHMS, 1/2W, 5% UNLESS OTHERWISE INDICATED.
2. ALL 1/4W AND 1/8W RESISTORS ARE 1% UNLESS OTHERWISE INDICATED.
3. ALL CAPACITORS ARE IN MICROFARADS, UNLESS OTHERWISE INDICATED.
4.  DENOTES FRONT PANEL MARKING.
5.  DENOTES REAR PANEL MARKING.
6.  DENOTES CHASSIS MOUNTED COMPONENT.
7.  DENOTES VOLTAGE FEEDBACK.
8.  DENOTES CURRENT FEEDBACK.
9. PIN LOCATIONS FOR TRANSISTORS ARE AS FOLLOWS:

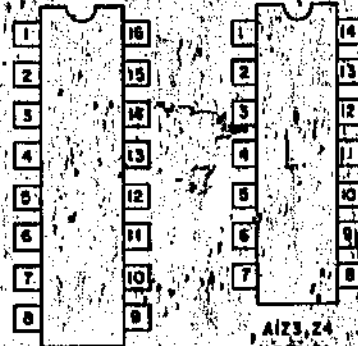


TO-3
(BOTTOM VIEW)



TO-6
(BOTTOM VIEW)

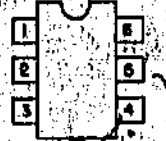
10. PIN LOCATIONS FOR INTEGRATED CIRCUITS ARE AS FOLLOWS:



A221-24 (Z9-Z10)
A822
(TOP VIEW)



A1Z3, Z4
A2Z5, Z6
(TOP VIEW)



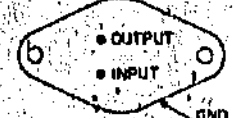
A1A1Z1-A1A1Z2
A1Z1, Z2
A6A1Z1, A6A6Z1
A6Z5
(TOP VIEW)



A6Z3, Z4
(BOTTOM VIEW)



A2Z7, Z8
A6Z1
(BOTTOM VIEW)



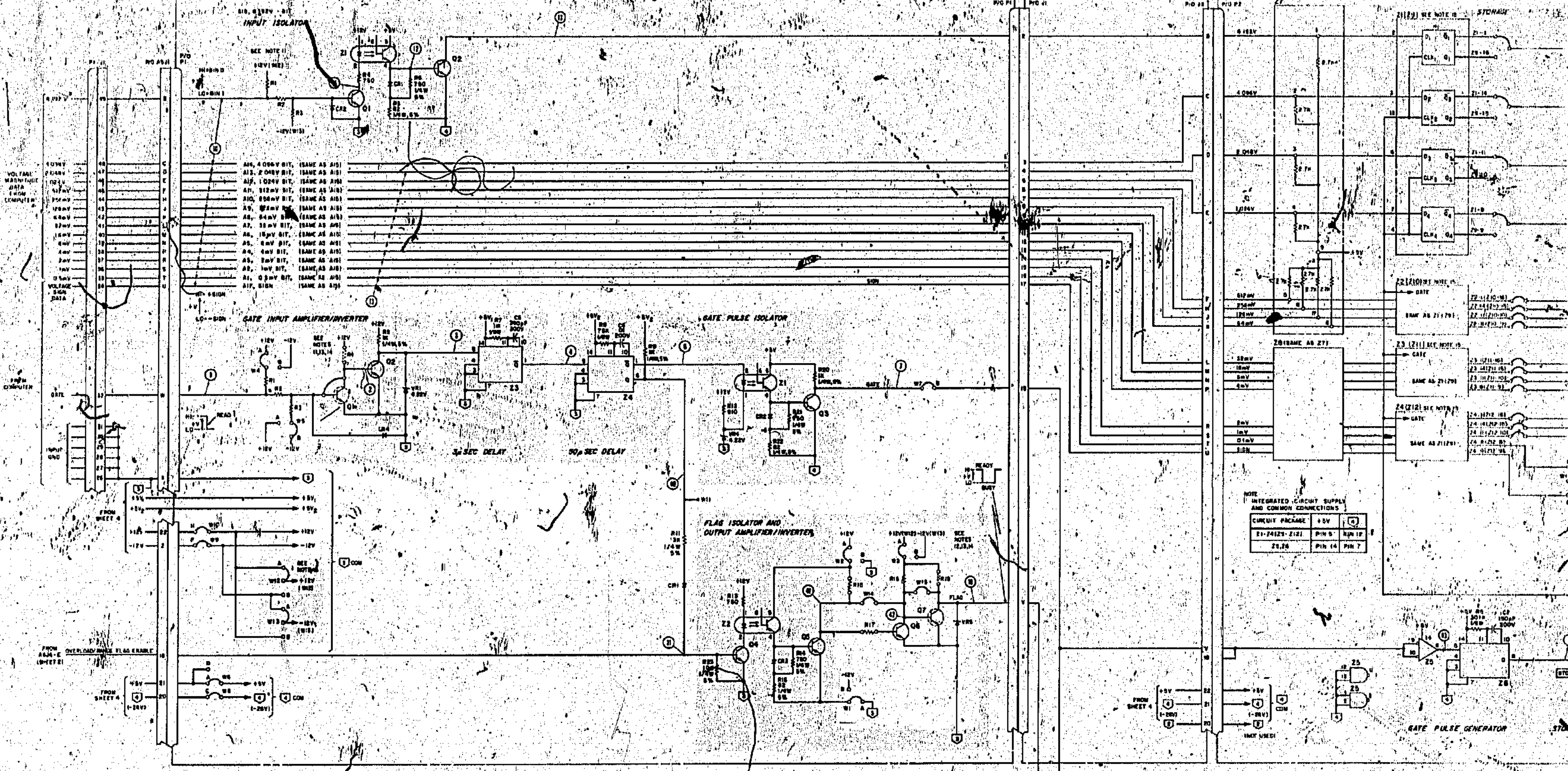
OUTPUT
INPUT
GND (CASE)
(BOTTOM VIEW)

11. THE RESISTANCE VALUES OF BIAS RESISTORS R1-R3 DEPEND ON THE STANDARD OPTION OF THE INSTRUMENT OR WHETHER THE INSTRUMENT IS A SPECIAL MODIFICATION. REFER TO THE APPROPRIATE OPTION APPENDIX OF THE INSTRUMENT MODIFICATION SHEET FOR THIS INFORMATION.
12. THE FOLLOWING COMPONENTS MAY OR MAY NOT BE INCLUDED, DEPENDING ON WHICH STANDARD OPTION APPLIES OR WHETHER THE INSTRUMENT IS A SPECIAL MODIFICATION: A1G6, A1R5, A1R7, A1R8, A1R5, A6CR14, A6CR18, A6A5R8, A6A6R8, A6A5V1, AND A6A6V1. REFER TO THE APPROPRIATE OPTION APPENDIX OR THE INSTRUMENT MODIFICATION SHEET FOR INFORMATION ON THESE COMPONENTS.
13. THESE JUMPERS ON THE A1 AND A6 BOARDS ARE POSITIONED AS SHOWN EXCEPT IN SPECIALLY-MODIFIED INSTRUMENTS. REFER TO THE INSTRUMENT MODIFICATION SHEET SUPPLIED WITH THE INSTRUMENT.
14. THE FOLLOWING COMPONENTS, DRAWN WITH DASHED LINES, ARE NOT INCLUDED EXCEPT IN SPECIALLY-MODIFIED INSTRUMENTS: A1Q1, A1Q7, A1R4, AND A1R3. REFER TO THE INSTRUMENT MODIFICATION SHEET SUPPLIED WITH THE MANUAL.
15. THE OUTPUT POLARITY OF THE FOUR STORAGE IC PACKAGES ON THE A2 BOARD DEPENDS ON WHETHER THEY ARE LOCATED IN THE Z1 THROUGH Z4 OR THE Z9 THROUGH Z12 SOCKETS. THE JUMPERS DRAWN AT THE OUTPUTS REPRESENT THIS CHOICE OF SOCKETS. THE APPROPRIATE OPTION APPENDIX IDENTIFIES WHICH ARE THE PROPER SOCKETS.
16. THE POSITION OF THIS JUMPER ON THE A2 BOARD DEPENDS ON THE STANDARD OPTION OF THE INSTRUMENT OR WHETHER THE INSTRUMENT IS A SPECIAL MODIFICATION. IN OPTION J20 OR OPTION O62 INSTRUMENTS, W1 IS CONNECTED TO B. IN OPTION O64 INSTRUMENTS, W1 IS CONNECTED TO A. FOR SPECIALLY-MODIFIED INSTRUMENTS, REFER TO THE INSTRUMENT MODIFICATION SHEET FOR THIS INFORMATION.
17. FOR SPECIALLY-MODIFIED INSTRUMENTS, THE CIRCUIT CONFIGURATION OF OUTPUT AMPLIFIER STAGES A6A5Q5, A6A5Q4, A6A6Q3, AND A6A6Q4 MAY DIFFER FROM SCHEMATIC. NOTE THAT A6A6Q4 AND A6A6Q7 ARE NOT INCLUDED IN ANY OF THE STANDARD OPTIONS. REFER TO THE INSTRUMENT MODIFICATION SHEET SUPPLIED WITH THE INSTRUMENT.

P/D A1 INPUT BOARD

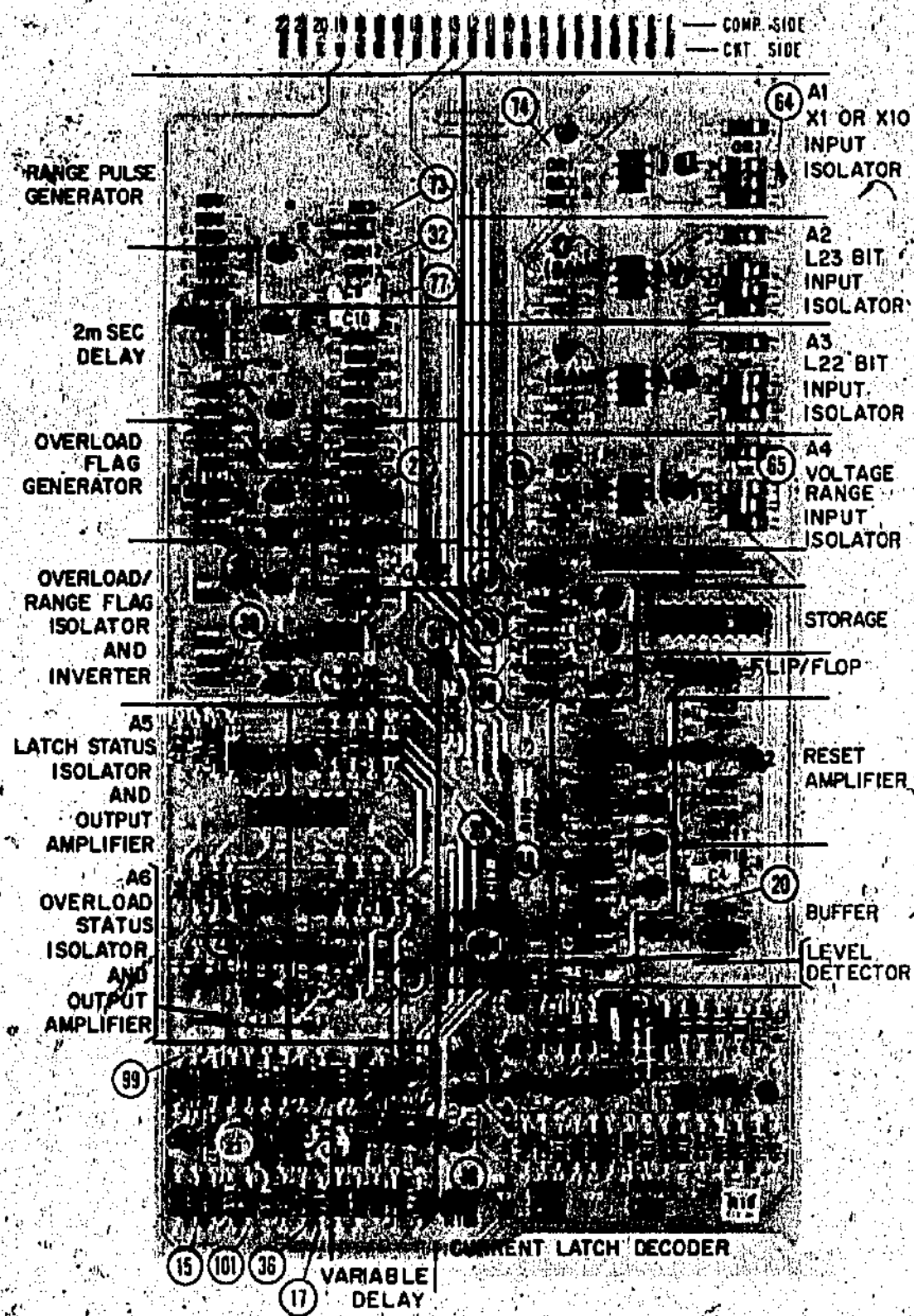
P/D A5 INTERCONNECT BOARD

P/D A2 LOGIC BOARD



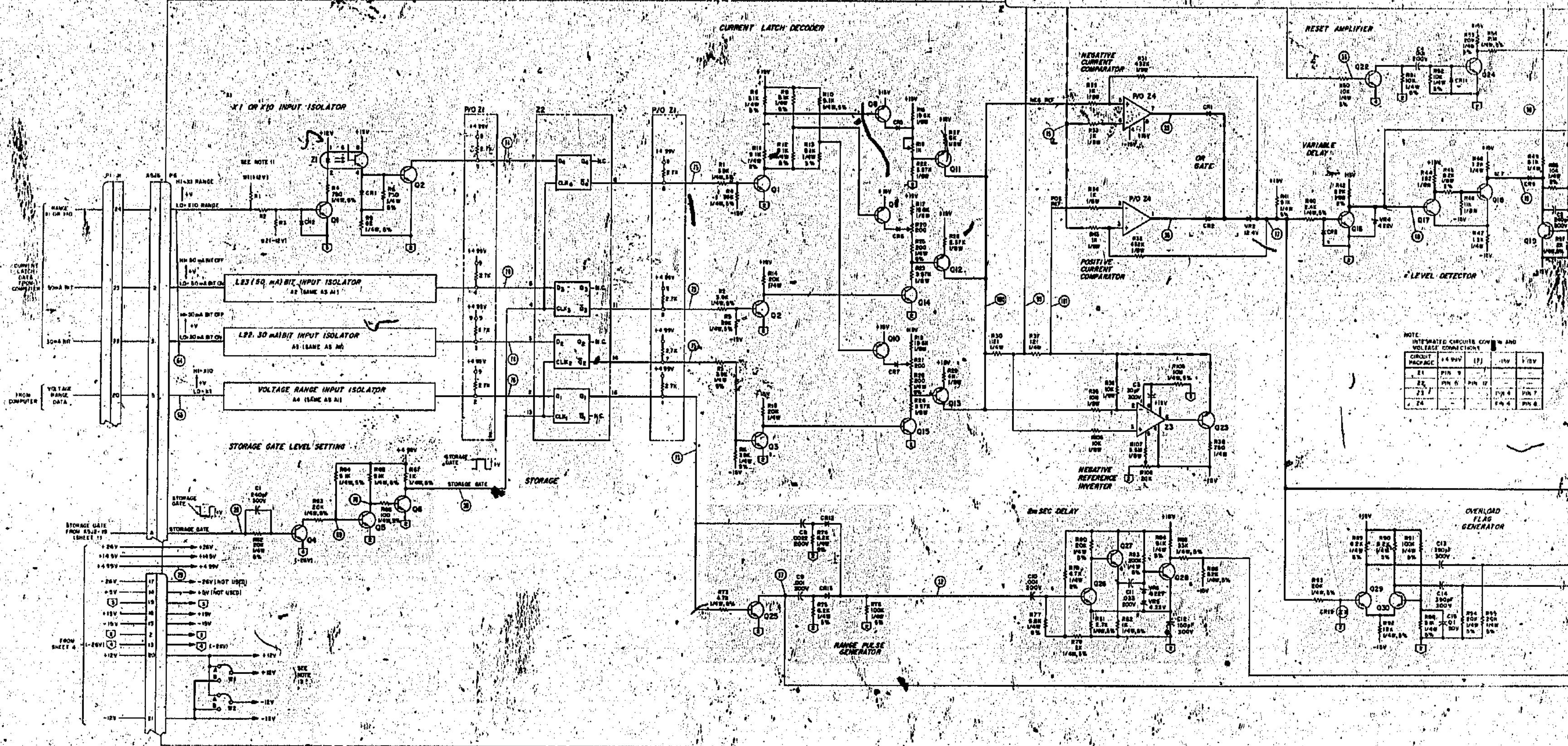
NOTE: INTEGRATED CIRCUIT SUPPLY AND COMMON CONNECTIONS

CIRCUIT PACKAGE	+5V	-12V
74-2412V-2121	PIN 5	PIN 19
74-2412V-2121	PIN 14	PIN 7



A6 Control Board, Component Location

P/O AS CONTROL BOARD



NOTE: INTEGRATED CIRCUIT COMPS AND VOLTAGE CONNECTIONS

CIRCUIT PACKAGE	+4.5V	-1V	-15V
21	PIN 9	PIN 17	---
22	PIN 5	---	---
23	---	---	---
24	---	---	---

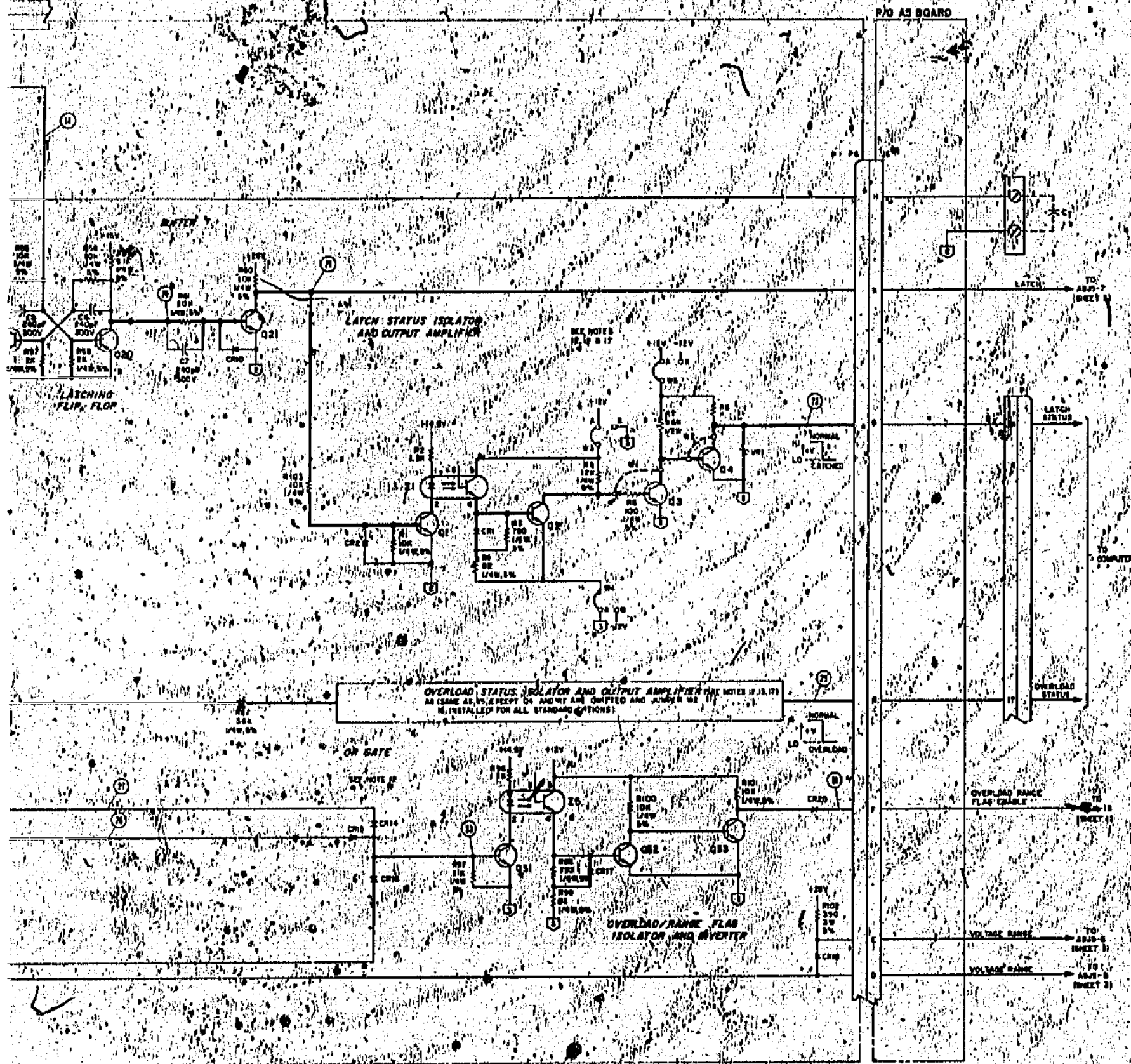
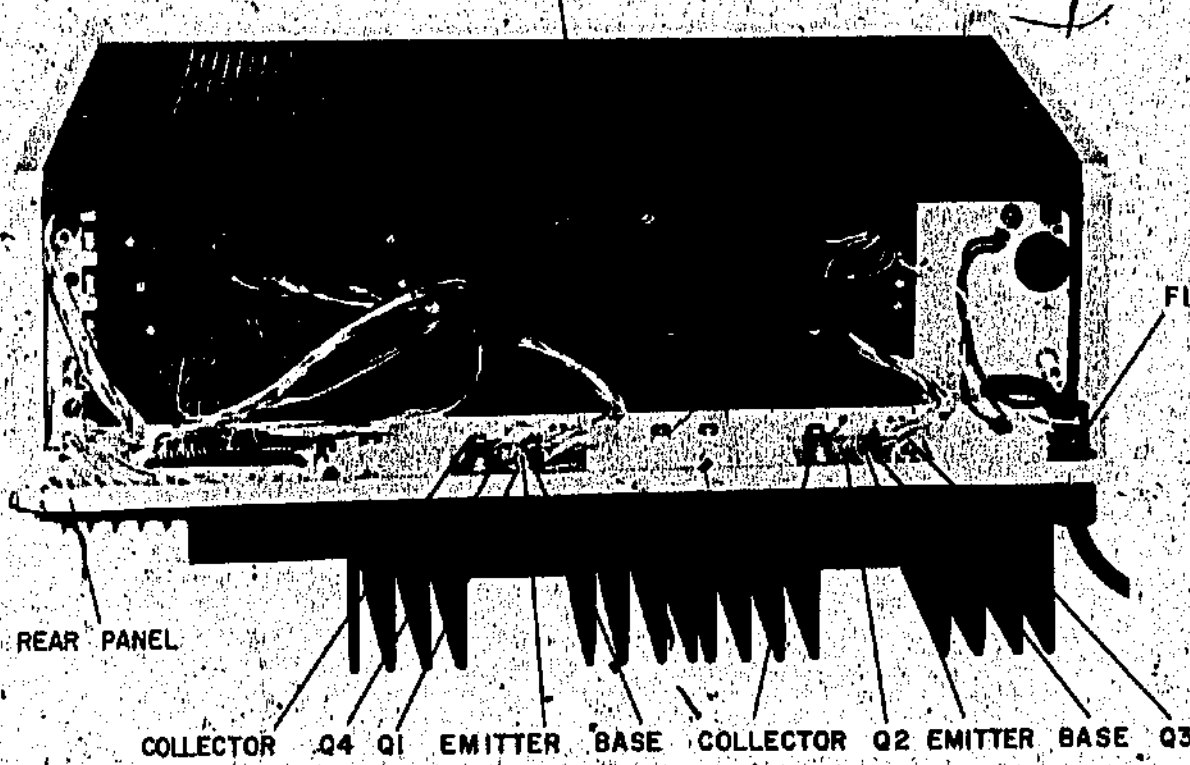


Figure 7-2 (Sheet 2) Current Latch and Voltage Range Processing Schematic Diagram

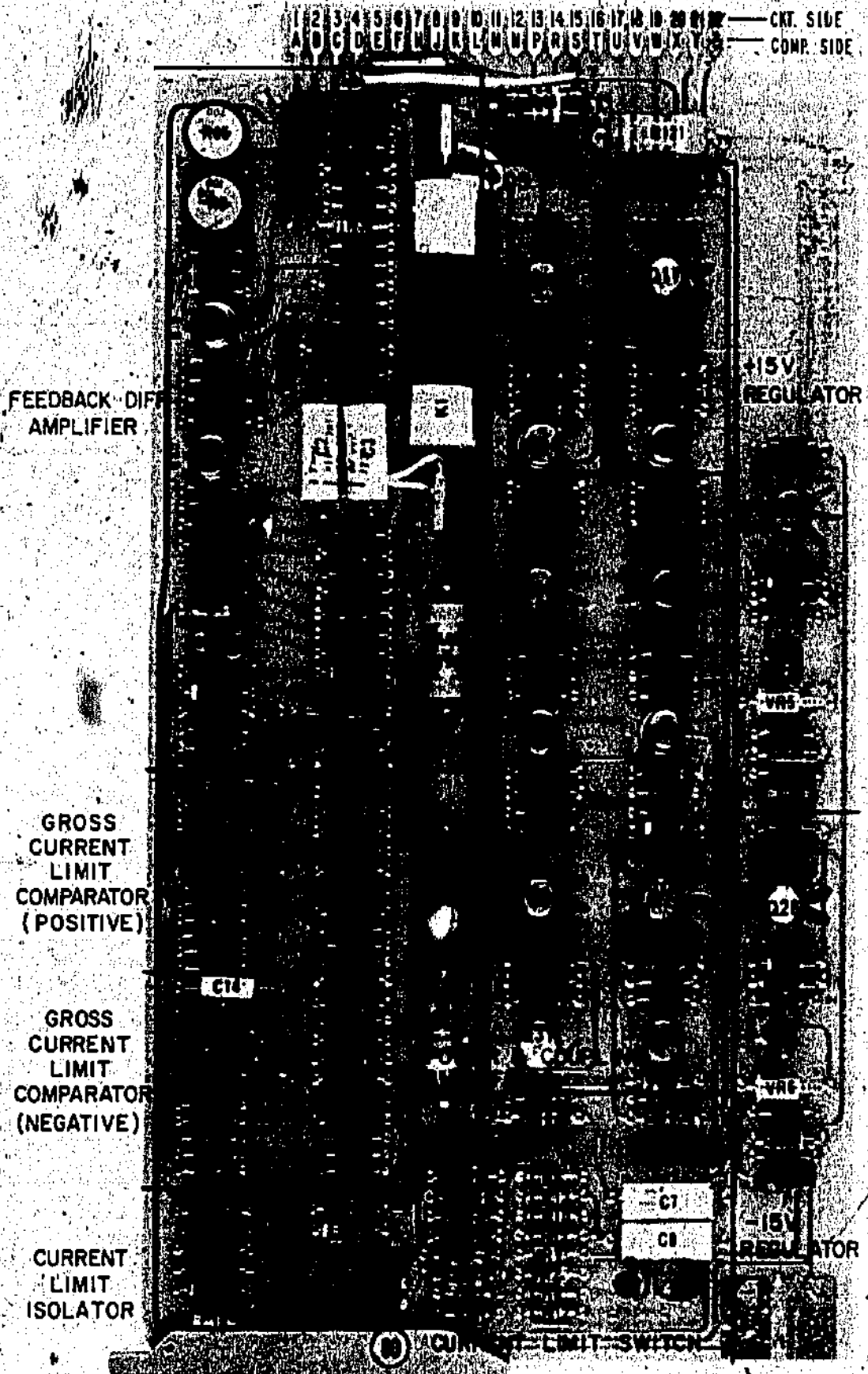
A5 INTERCONNECT BOARD



Rear View, Component Location



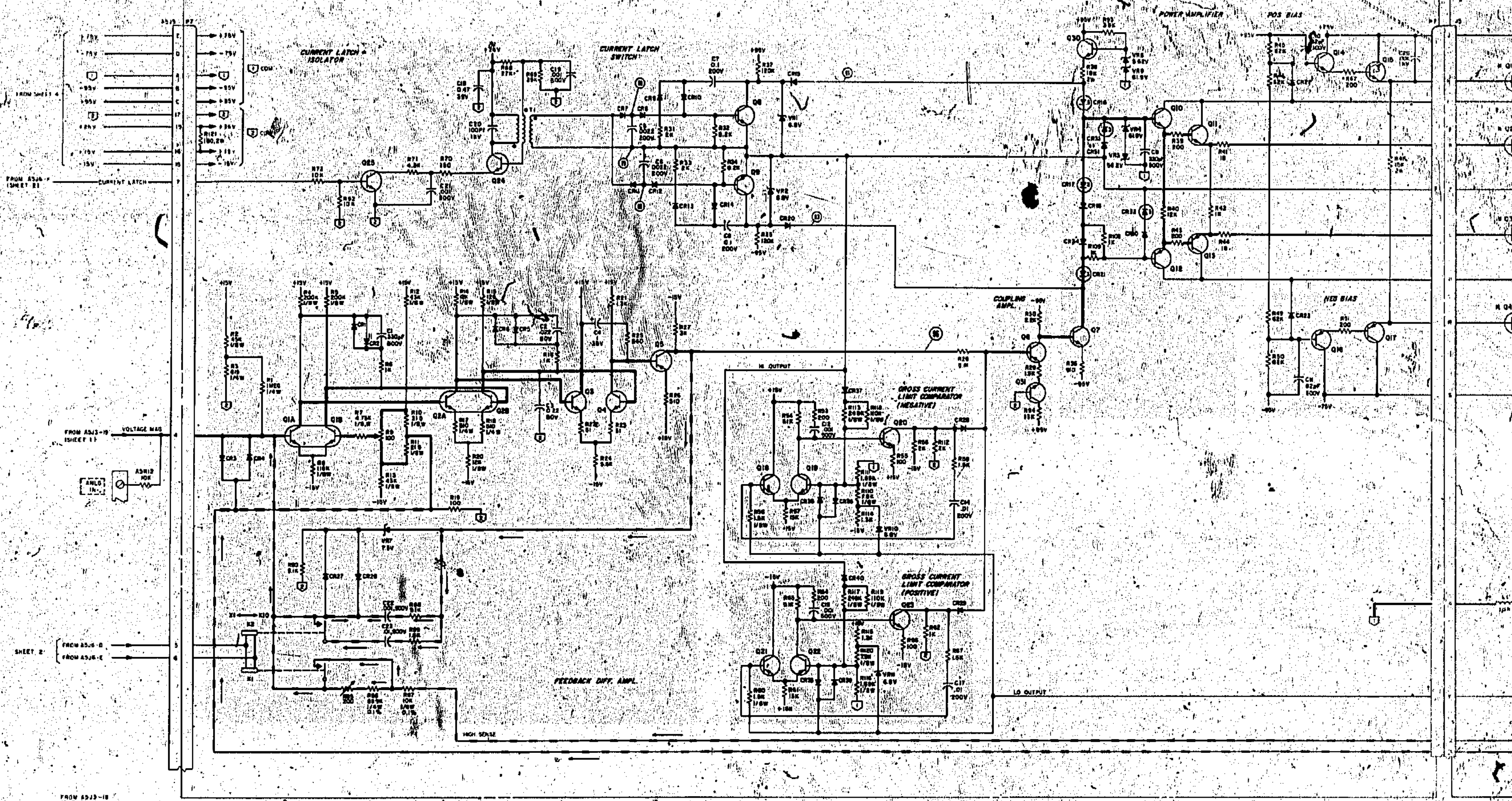
A5 Interconnect Board, Component Location



A7 Amplifier Board, Component Location

AT AMPLIFIER BOARD

A5 INTERCONNECT BOARD



CT BOARD

CT BOARD

A4 POWER SUPPLY BOARD

METER CRT.

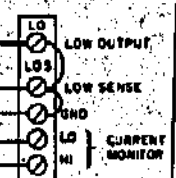
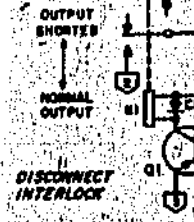
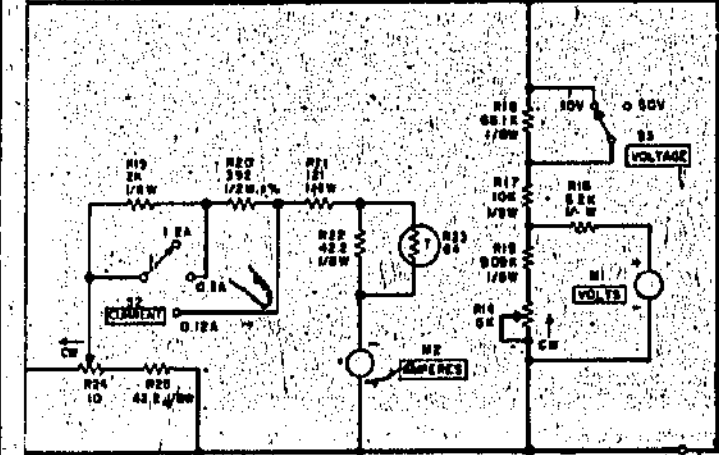
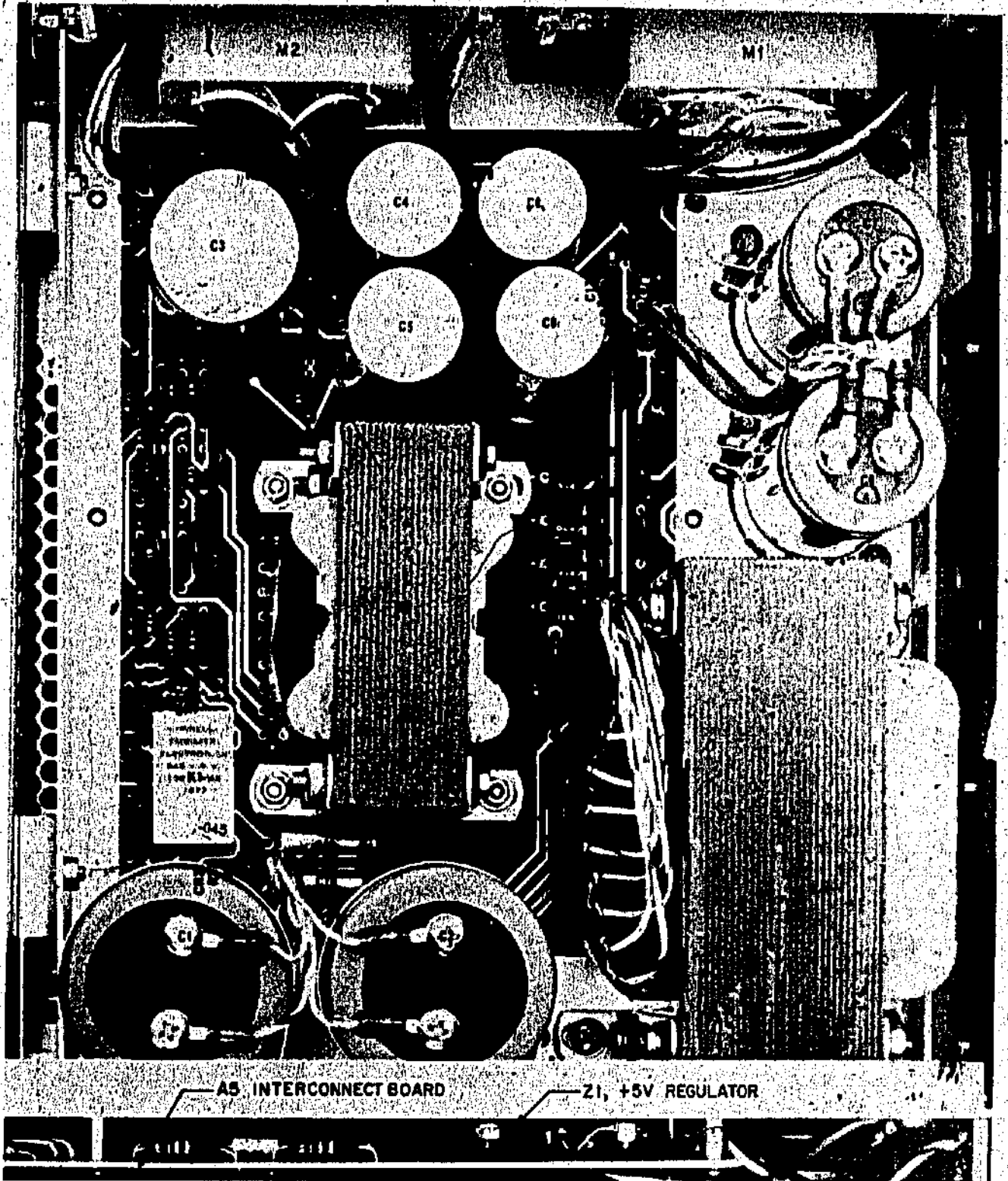


Figure 7-2 (Sheet 3). Power Amplifier, Schematic Diagram



A4 Power Supply Board, Component Location

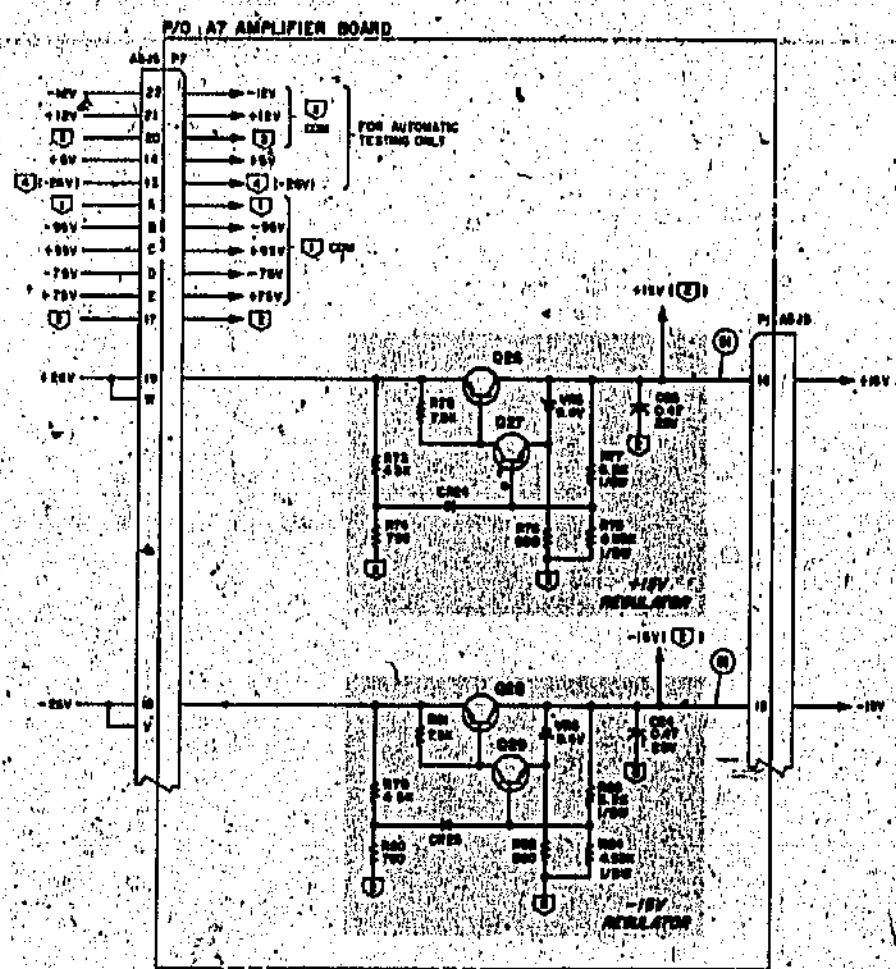
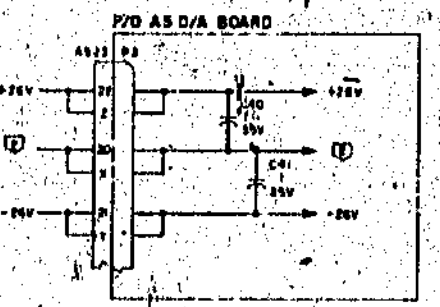
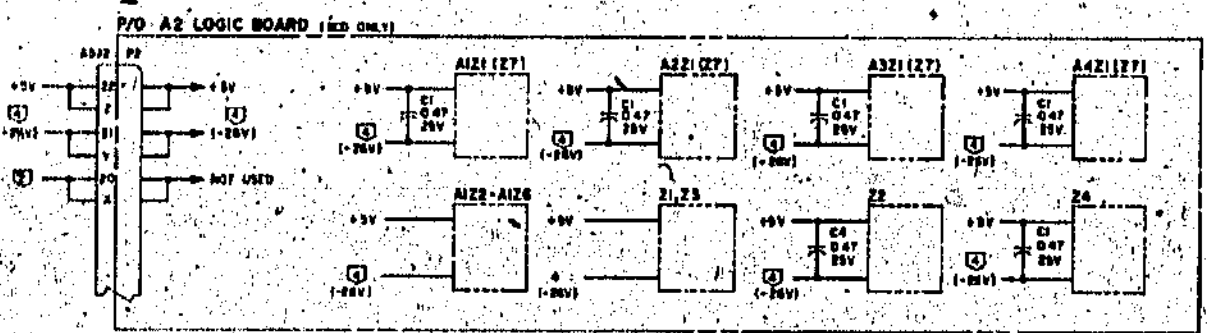
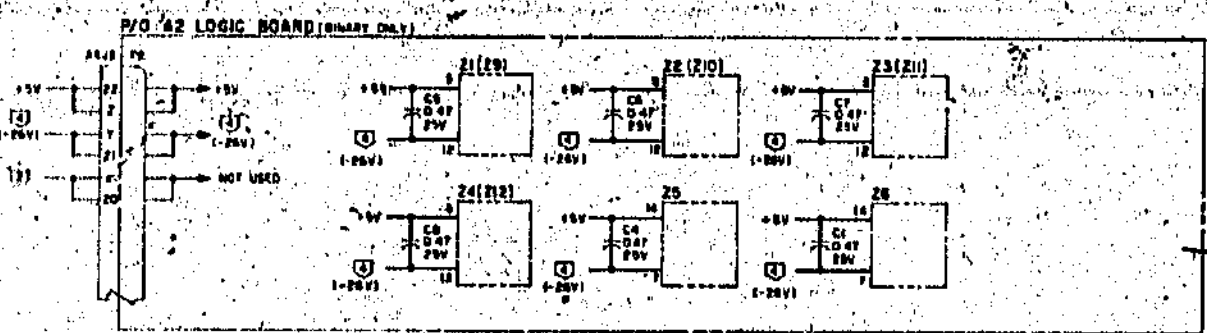
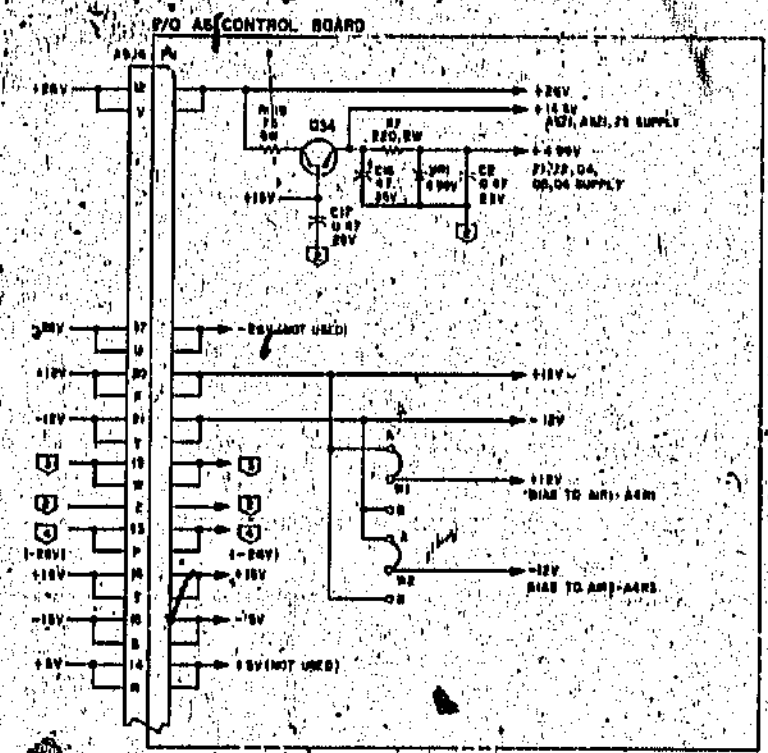
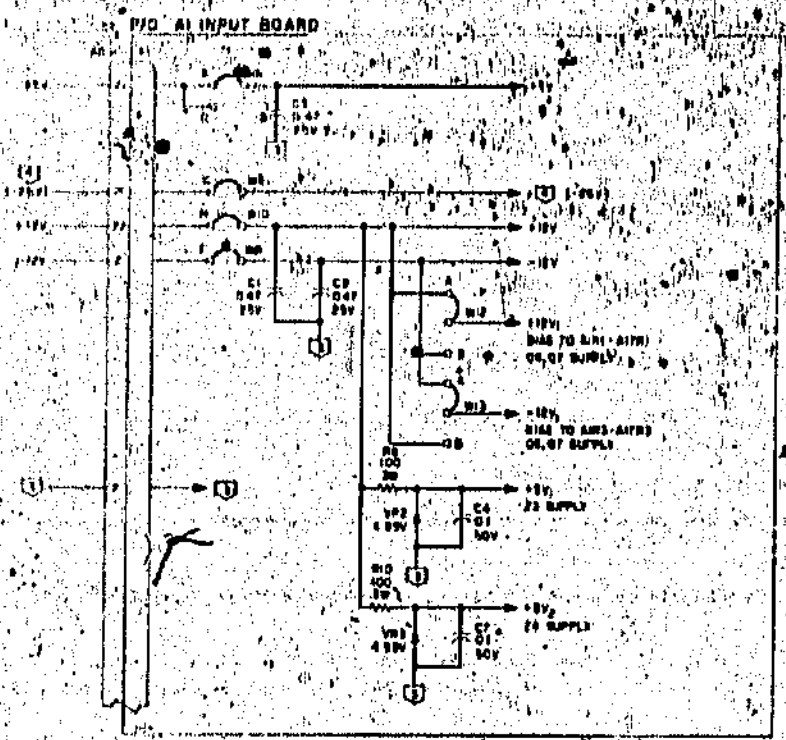


Figure 7-2 (Sheet 4). Power Distribution Schematic Diagram

APPENDIX A

OPTION J20-Binary Interface For The HP 12661A DVS Program Card

A-1 INTRODUCTION

A-2 This Appendix describes the input and output data parameters for interfacing with a digital Binary source employing the HP 12661A DVS Program Card. Only interfacing requirements are discussed in this Appendix. Information of a more general nature is given in Section III of this manual. Hence, for a complete conception of the operating and interfacing requirements, both this Appendix and Section III must be consulted.

A-3 The data parameters described in the following paragraphs include the following:

- (1) Binary voltage magnitude data.
- (2) Input/Output signal polarity.
- (3) Logic coding - significance of high and low input/output signal states.
- (4) Logic levels - voltage limits for high and low digital signal states.

A-4 The digital input/output stages on three of the DVS plug-in boards (A1, A2, and A6) have been especially designed to obtain the desired data parameters under worst case conditions. A list of these special parts is included at the rear of this Appendix.

A-5 DATA CONNECTOR

A-6 Input/output data is connected to the digital programming source by means of the rear connector (Figure A-1). The parameters associated with each of the signals of Figure A-1 are discussed in the following paragraphs.

A-7 INPUT/OUTPUT SIGNAL POLARITY

A-8 All input/output signals are of positive polarity; i.e. are above 0 volts. Therefore, the input/output stages on A1 (input board) and A6 (control board) use NPN transistors as shown in the schematic (Figure 7-2) provided in the manual.

A-9 RECEIVER CIRCUITS AND LOGIC LEVELS

A-10 Figure A-2 shows an input circuit that applies to all of the digital inputs listed on the drawing. The three resistors of the input voltage divider are selected so that a high input level will turn-on the succeeding driver stage and a low input level will cut the stage off. As shown on

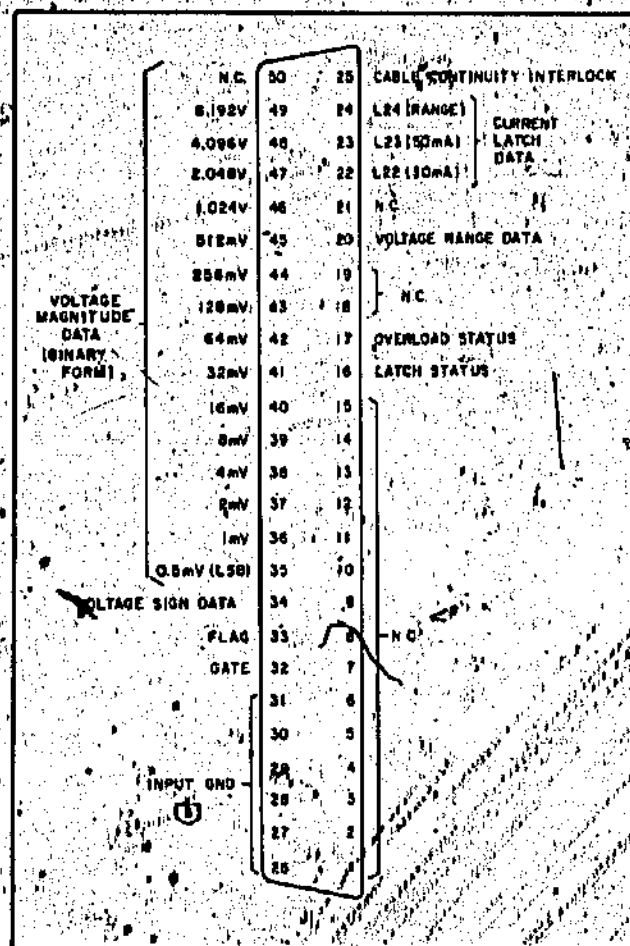


Figure A-2. Input/Output Data Connector

Figure A-2, the logic levels for all of the listed inputs are high = +5.5 to +12V, and low = -1 to +2.8V.

A-11 The maximum current that can be drawn from the input circuit when the input terminals are short circuited is 2mA (designated ISC-MAX on Figure A-2). The maximum voltage that can appear across the input terminals under open circuit conditions (designated EOG-MAX) is 9V.

A-12 VOLTAGE MAGNITUDE INPUT DATA

A-13 Logic Type. The input data to this unit is received in a binary code. Positive numbers are received from the computer in straight binary form while negative numbers are received in 2's complement form, which will be discussed later.

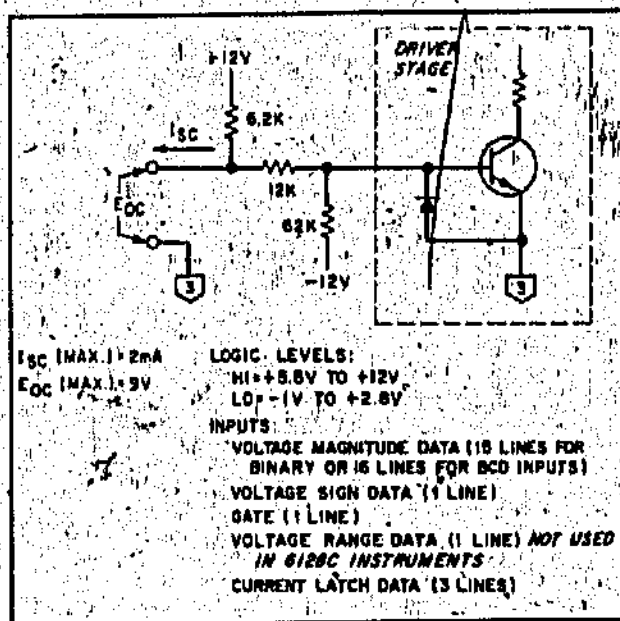
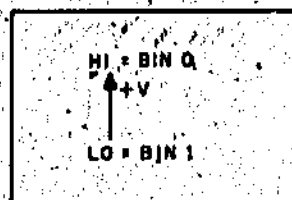


Figure A-2. Receiver Circuit

A-14. Logic Coding.



A-15 Logic Inversion. The A2 storage inverters for the voltage magnitude bits are included for the logic coding (HI = BIN 0) associated with this option as shown in Figure 7-2, Sheet 1. (The storage IC's are installed in the Z1-Z4 positions.)

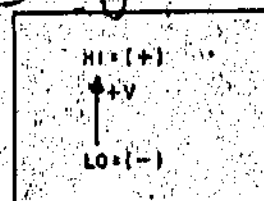
A-16 The voltage magnitude input data is made up of 15 binary bits designated according to their positive analog equivalent value in millivolts (8192, 4096, 2048, . . . 0.5). This input data is used in conjunction with the voltage sign and voltage range data to control the output voltage of the DVS. The voltage magnitude data is programmed into the unit in straight binary form when the voltage sign data is positive, and in 2's complement form when the voltage sign data is negative. 2's complement form consists of complementing the equivalent positive binary number (all ones become zeros, all zeros become ones) and adding a binary 1 to the least significant bit. The voltage sign data determines the polarity of the output voltage while the voltage range program multiplies the voltage program data by X1 or X10. Hence, the output of the DVS may be programmed between -16.384 and +16.385 volts (X1 or X10). Notice that for 6130C instruments, numbers beyond 5.0 in the X10 range are not valid because the maximum rated output

voltage for this unit is 50V. As explained in Section III, the output voltage of the 6130C is limited to approximately 55 volts maximum.

A-17 VOLTAGE SIGN

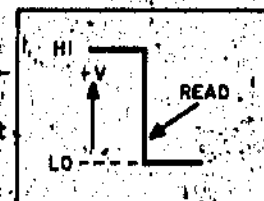
A-18 The voltage sign bit determines the polarity of the output. Jumper connection A2W1-B (Figure 7-2, sheet 1) is included for the coding shown below.

A-19



A-20 GATE

A-21 Coding. As shown, a high to low transition of the gate input permits storage of the voltage magnitude, voltage sign, current latch, and voltage range input data in the DVS storage registers. Notice that the STORAGE switch on the A2 P.C. board (see Figure 3-2) must be in the STORE position to utilize this storage capability.



A-22 VOLTAGE RANGE

A-23 Coding. HI = X10 (High voltage range).
 LO = X1 (Low voltage range).

A-24 The following chart shows the coding required for voltage range.

INPUT CODE	VOLTAGE RANGE
Voltage Range Bit	
LO HI	X1 X10

A-25 CURRENT LATCH

A-26 Coding. The current latch data forms a 3-bit binary code. The input codes for each current latch value are shown in the chart on page 3-5. Notice that the three current latch bits provide a maximum of eight possible combinations.

A-27 Ct Terminals. As described in Section III,

the current latch delay period is determined by the condition of the C_T terminals of the rear of the unit. Notice that if the C_T terminals are shorted, the DVS will not current latch even if the output current exceeds the programmed current latch value.

A-28 CABLE CONTINUITY INTERLOCK

A-29 Before output voltage can be obtained from the DVS, a connection must be made between input common (3) and the cable continuity interlock pin 25 of the input/output connector. If this connection is not made the output terminals of the DVS will be shorted by an internal relay. This protects the load device against excessive voltages in case the input cable is disconnected.

A-30 Cable Continuity Interlock Receiver Circuit. Figure A-3 shows the cable continuity interlock circuit. The three input voltage divider resistors are selected so that a common input will cause A4Q1 to saturate and an open (no input connection) will cause A4Q1 to cutoff. The maximum current (I_{SC-MAX}) that could be drawn from the input circuit when the input terminals are short circuited is 6mA. The maximum voltage (E_{OC-MAX}) that appears across the input terminals under open circuit conditions is 8V.

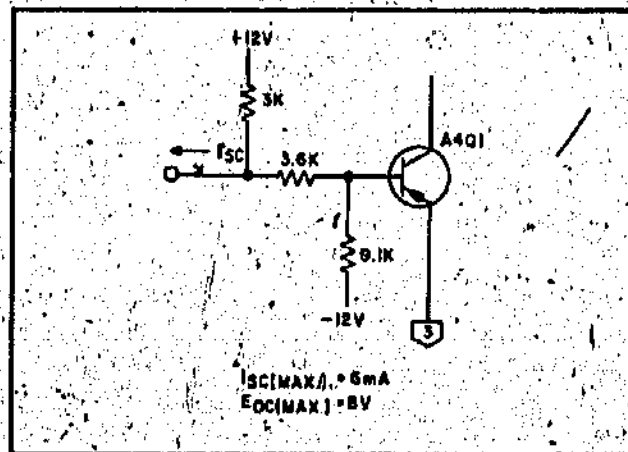


Figure A-3. Cable Continuity Interlock Receiver Circuit

A-31 INPUT GROUND

A-32 Input data common must be connected to common in the DVS 6130C (pins 26 through 31) shown on Figure A-1. These pins are internally shorted together within the connector jack.

A-33 OUTPUT DRIVER CIRCUITS

A-34 Figure A-4 shows the output driver circuit that is used for each digital output signal; namely,

flag; overload status, and latch status. "Open collector" type drivers are used. Each transistor can withstand up to 20V across it in the cutoff condition and can conduct up to 20mA of current when saturated. The output is "high" (more positive) when the driver is cutoff or "low" (less positive) when the driver is conducting. Output impedances under these conditions are shown on the drawing.

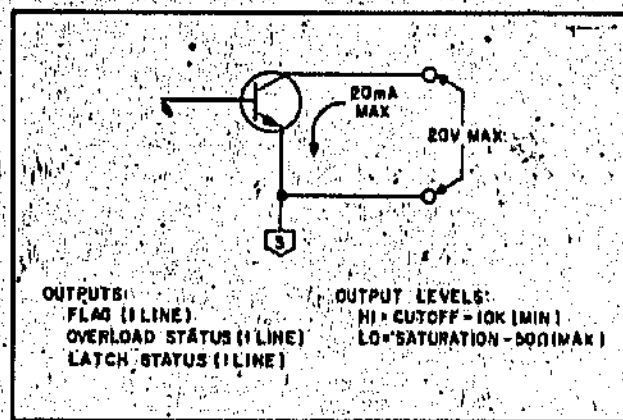
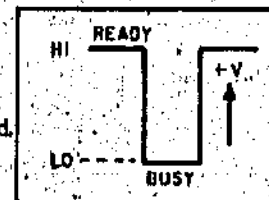


Figure A-4. Driver Circuit

A-35 FLAG OUTPUT

A-36 Flag output signals are issued under two separate conditions. As described in Section III, the flag output switches from ready to busy during: (1) processing of the voltage magnitude data bits, and (2) changing of the voltage range. The time that the flag remains in the busy state is different for each condition (see Figures 3-4, 3-5, and 3-7). For this Option, AGCR14 and AGCR15 are deleted. This means that when an overload condition exists, the Flag, as mentioned in Paragraph 3-30 and shown on Figure 3-7, is not generated. Note, however, that the Flag signal is still generated when a range change occurs.

A-37 Flag Polarity. For this option, transistor A1Q6 and resistor A1R15 are not supplied, jumpers W14 and W15 are installed, and, therefore, the flag polarity is as follows:

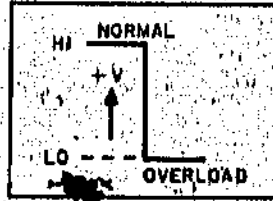


A-38 OVERLOAD STATUS

A-39 The overload status line switches to the overload state whenever the output current exceeds the programmed current latch value (see Figure 3-7). The signal remains in the overload state until the output current is decreased (unit goes into current latch or overload is removed).

A-40 Overload Status Polarity. For this option,

transistor A6A6Q4 and resistor A6A6R7 are not supplied and jumper A6A6W2 is installed. Therefore, transistor A6A6Q3 serves as the output driver and the output signal polarity is as follows:

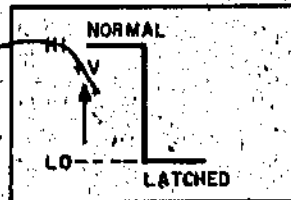


A-41 LATCH STATUS

A-42 The latch status line switches to the latched state if the unit goes from the overload to the latch state (Figure 3-7). In the latch condition, the output current is limited to less than 10mA. The latch status signal will revert from the overload-latch state to the normal state approximately 10µsec after the next gate input is received, providing that the overload condition no longer exists. Therefore, to program the DVS out of the current latch condition and back to normal operation, the overload must be removed or the current latch setting increased; and then a new gate signal must be issued.

A-43 The latch status signal does not switch to the latched state if the C₁ terminals on the rear of the DVS are shorted (refer to Paragraph 3-33).

A-44 Latch Status Polarity. For this Option, transistor A6A5Q4 serves as the output driver. The signal polarity is as follows:



A-45 POCKET-PROGRAMMER 14533B USAGE

A-46 To program the DVS using the IIP Pocket Programmer 14533B, refer to the following chart for appropriate switch positions for this particular option. Note that these switch positions may not apply to the "A" version of the Pocket Programmer 14533A.

SWITCH	POSITION
Voltage Magnitude (0.5-8192) Binary 1 Binary 0	down up
Output Sign Positive Output Negative Output	up down
Current Latch (L22, L23, L24) 20mA 50mA 70mA 100mA 200mA 500mA 700mA 1000mA	L22 L23 L24 up up up down up up up down up down down up up up down down up down up down down down down down
MP/DCPS	down
Input Level Reference	down

A-47 OPTION J20 PARTS LIST

A-48 The following is a tabular listing of the special parts associated with this Option.

Option 120 Replaceable Parts

REF. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A1	Input Board	1		28480	5060-7986	1
A1A1R1	fxd, comp 6.2K Ω \pm 5%, 1/4W	1	CB-6225	01121	0683-6225	1
A1A1R2	fxd, comp 12K Ω \pm 5%, 1/4W	1	CB-1235	01121	0683-1235	1
A1A1R3	fxd, comp 62K Ω \pm 5%, 1/4W	1	CB-6235	01121	0683-6235	1
A1A2 through A1A17	Same as A1A1	16				
A1Q1, Q6, Q7	Omit Q1, Q6, Q7					
A1R1	fxd, comp 1K Ω \pm 5%, 1/4W	1	CB-1025	01121	0683-1025	1
A1R2	fxd, comp 2K Ω \pm 5%, 1/4W	1	CB-2025	01121	0683-2025	1
A1R3	fxd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
A1R4, 15, 17, 18, and 19	Omit R4, 15, 17, 18, and 19					
A1VR5	Omit VR5					
A2	Logic Board	1		28480	5060-7989	1
A2Z1-Z4	Quad, D-Type Latch, IC	4	SN7475	01295	1420-0301	4
A2Z9-Z12	Omit Z9-Z12 (SN7475's installed in Z1-Z4 locations)					
A6	Control Board	1		28480	5060-7993	1
A6A1R1	fxd, comp 6.2K Ω \pm 5%, 1/4W	1	CB-6225	01121	0683-6225	1
A6A1R2	fxd, comp 12K Ω \pm 5%, 1/4W	1	CB-1235	01121	0683-1235	1
A6A1R3	fxd, comp 62K Ω \pm 5%, 1/4W	1	CB-6235	01121	0683-6235	1
A6A2 through A6A4	Same as A6A1	3				
A6A5R8	Omit A6A5R8					
A6A5VR1	Omit A6A5VR1					
A6A6Q4	Omit A6A6Q4					
A6A6R7, R8	Omit A6A6R7; R8					
A6A6VR1	Omit A6A6VR1					
A6CR14, 15	Omit CR14, CR15					

APPENDIX B OPTION 062-Binary Interface For Open Collector Circuits

B-1 INTRODUCTION

B-2 This Appendix describes the input and output data parameters for interfacing with a digital Binary source employing "open collector" driver transistors. Only interfacing requirements are discussed in this Appendix. Information of a more general nature is given in Section III of this manual. Hence, for a complete conception of the operating and interfacing requirements, both this Appendix and Section III must be consulted.

B-3 The data parameters described in the following paragraphs include the following:

- (1) Binary voltage magnitude data.
- (2) Input/Output signal polarity.
- (3) Logic coding - significance of high and

low input/output signal states.

(4) Logic levels - voltage limits for high and low digital signal states.

B-4 The digital input/output stages on three of the DVS plug-in boards (A1, A2, and A6) have been especially designed to obtain the desired data parameters under worse case conditions. A list of these special parts is included at the rear of this Appendix.

B-5 DATA CONNECTOR

B-6 Input/Output data is connected to the digital programming source by means of the rear connector (Figure B-1). The parameters associated with each of the signals of Figure B-1 are discussed in the following paragraphs.

B-7 INPUT/OUTPUT SIGNAL POLARITY

B-8 All input/output signals are of positive polarity; i. e. are above 0 volts. Therefore, the input/output stages on A1 (input board) and A6 (control board) use NPN transistors as shown in the schematic (Figure 7-2) provided in the manual.

B-9 RECEIVER CIRCUITS AND LOGIC LEVELS

B-10 Figure B-2 shows an input circuit that applies to all of the digital inputs listed on the

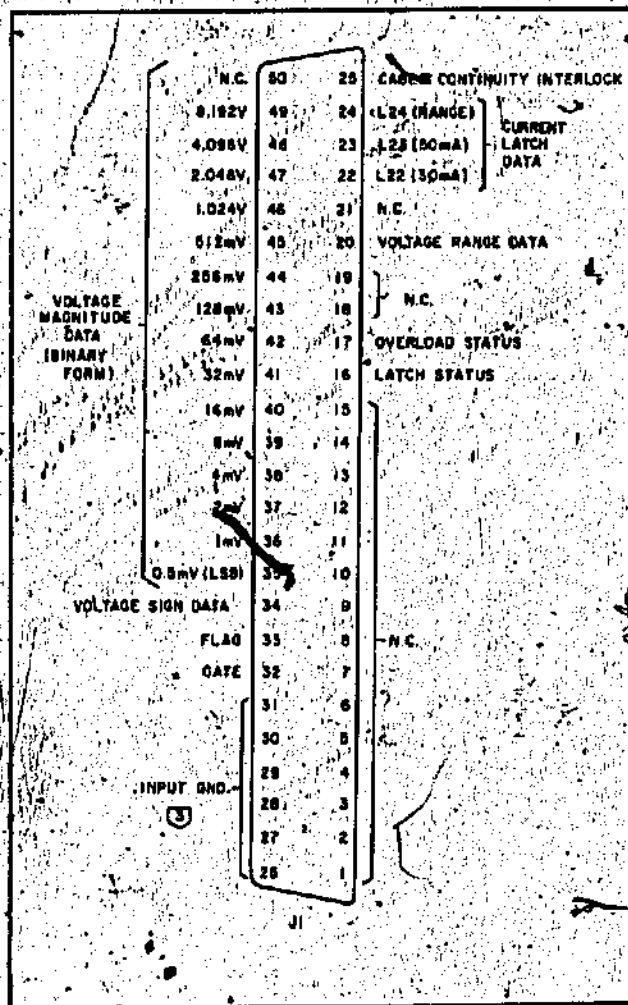


Figure B-1. Input/Output Data Connector

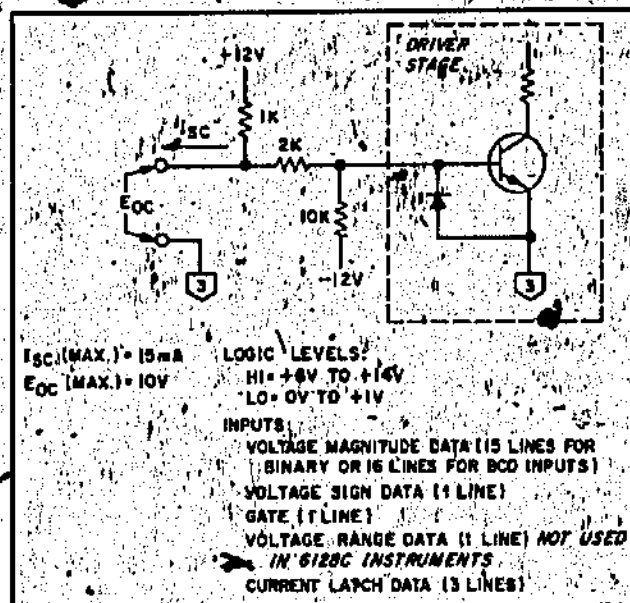


Figure B-2. Receiver Circuit

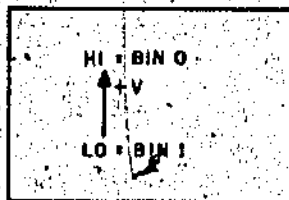
drawing. The three resistors of the input voltage divider are selected so that a high input level will turn-on the succeeding driver stage and a low input level will cut the stage off. As shown on Figure B-2, the logic levels for all of the listed inputs are high = +6V to +14V and low = 0V to +1V.

B-11 The maximum current that can be drawn from the input circuit when the input terminals are short-circuited is 15mA (designated I_{SC-MAX} on Figure B-2). The maximum voltage that can appear across the input terminals under open circuit conditions (designated E_{OC-MAX}) is 10V.

B-12 VOLTAGE MAGNITUDE INPUT DATA

B-13 Logic Type. The input data to this unit is received in a binary code. Positive numbers are received from the computer in straight binary form while negative numbers are received in 2's complement form, which will be discussed later.

B-14 Logic Coding.



B-15 Logic Inversion. The A2 storage inverters for the voltage magnitude bits are included for the logic coding (HI = BIN 0) associated with this option as shown in Figure 7-2, Sheet 1 (the storage IC's are installed in the Z1-Z4 positions).

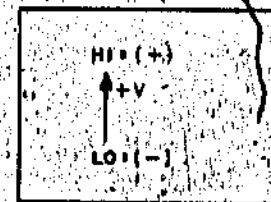
B-16 The voltage magnitude input data is made up of 15 binary bits designated according to their position analog equivalent value in millivolts (8192, 4096, 2048, . . . 0.5). This input data is used in conjunction with the voltage sign and voltage range data to control the output voltage of the DVS. The voltage magnitude data is programmed into the unit in straight binary form when the voltage sign is positive, and in 2's complement form when the voltage sign is negative. 2's complement form consists of complement form consists of complementing the equivalent positive binary number (all ones become zeros, all zeros become ones) and adding a binary 1 to the least significant bit. The voltage sign data determines the polarity of the output voltage while the voltage range program select multiplies the voltage program data by X1 or X10. Hence, the output of the DVS may be programmed between -16,384 and +16,385 volts (X1 or X10). Notice that for 6130C instruments, numbers beyond 5.0 in the X10 range are not valid because the maximum rated output voltage for this unit is 50V. As explained in Section III, the output voltage of the 6130C is limited to approximately

55 volts maximum.

B-17 VOLTAGE SIGN

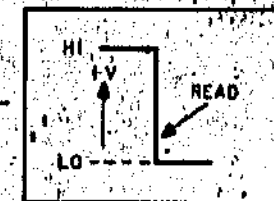
B-18 The voltage sign data bit determines the polarity of the output. Jumper connection A2W1-B (Figure 7-2, sheet 1) is included for the coding shown below.

B-19 Logic Coding.



B-20 GATE

B-21 Coding. As shown, a high to low transition of the gate input permits storage of the voltage magnitude voltage sign, current latch, and voltage range input data in the DVS storage registers. Notice that the STORAGE switch on the A2 P.C. Board (see Figure 3-2) must be in the STORE position to utilize this storage capability.



B-22 VOLTAGE RANGE

B-23 Coding. HI = X10 (High voltage range)
LO = X1 (Low voltage range)

B-24 The following chart shows the coding required for voltage range.

INPUT CODE	VOLTAGE RANGE
Voltage Range Bit	
LO	X1
HI	X10

B-25 CURRENT LATCH

B-26 Coding. The current latch data forms a 3-bit binary code. The input codes for each current latch value are shown in the chart on page 3-5. Notice that the three current latch bits provide a maximum of eight possible combinations.

B-27 C_T Terminals. As described in Section III, the current latch delay period is determined by the condition of the C_T terminals at the rear of the unit. Notice that if the C_T terminals are shorted,

the DVS will not current latch even if the output current exceeds the programmed current latch value.

B-28 CABLE CONTINUITY INTERLOCK

B-29 Before output voltage can be obtained from the DVS, a connection must be made between input common (3) and the cable continuity interlock pin 25 of the input/output connector. If this connection is not made the output terminals of the DVS will be shorted by an internal relay. This protects the load device against excessive voltages in case the input cable is disconnected.

B-30 Cable Continuity Interlock Receiver Circuit. Figure B-3 shows the cable continuity interlock circuit. The three input voltage divider resistors are selected so that a (3) common input will cause A4Q1 to saturate and an open (no input connection) will cause A4Q1 to cut off. The maximum current (ISC-MAX) that could be drawn from the input circuit when the input terminals are short circuited is 6mA. The maximum voltage (ECC-MAX) that appears across the input terminals under open circuit conditions is 6V.

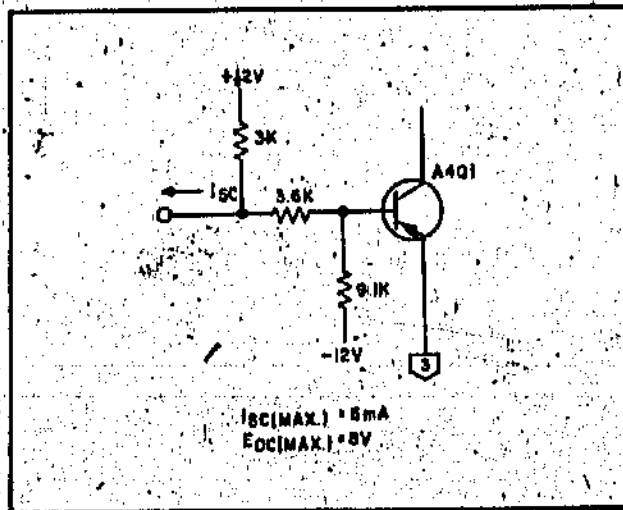


Figure B-3. Cable Continuity Interlock Receiver Circuit

B-31 INPUT GROUND

B-32 Input data common must be connected to (3) common of the DVS (pins 26 through 31 shown on Figure B-1). These pins are internally shorted together within the connector/jack.

B-33 OUTPUT DRIVER CIRCUITS

B-34 Figure B-4 shows the output driver circuit that is used for each digital output signal, namely, flag, overload status, and latch status. "Open collector" type drivers are used. Each transistor can withstand up to 20V across it in the cutoff condition and can conduct up to 20mA of current when saturated. The output is "high" (more positive) when the driver is cut off or "low" (less positive) when the driver is conducting. Output impedances under these conditions are shown on the drawing.

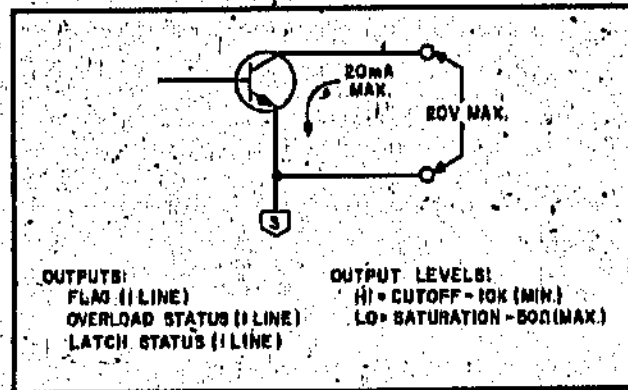
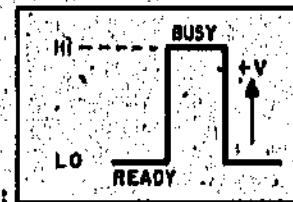


Figure B-4. Driver Circuit

B-35 FLAG OUTPUT

B-36 Flag output signals are issued under three separate conditions. As described in Section III, the flag output switches from ready to busy during: (1) processing of the voltage magnitude data bits, (2) changing of the voltage range, and (3) current overload periods. The time that the flag remains in the busy state is different for each of the three conditions. (see Figures 3-4, 3-5, and 3-7).

B-37 Flag Polarity. For this option, transistor A1Q6 and resistors A1R15 and A1R17 are included, jumper W14 is not installed, and, therefore, the flag polarity is as follows:



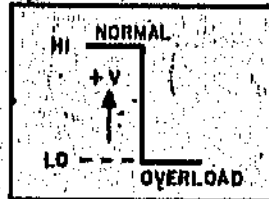
B-38 OVERLOAD STATUS

B-39 The overloaded status line switches to the

overload state whenever the output current exceeds the programmed current latch value (see Figure 3-7). The signal remains in the overload state until the output current is decreased (unit goes into current latch or overload is removed).

B-40 Overload Status Polarity

For this Option, transistor AGA5Q4 and resistor AGA5R7 are not supplied and jumper AGA5W2 is installed. Therefore, transistor AGA6Q3 serves as the output driver and the output signal is as follows:



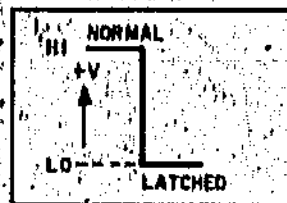
B-41 LATCH STATUS

B-42 The latch status line switches to the latched state if the unit goes from the overload to the latch state (Figure 3-7). In the latch condition, the output current is limited to less than 10mA. The latch status signal will revert from the overload latch state to the normal state approximately 10µsec after the next gate input is received, providing that the overload condition no longer exists. Therefore, to program the DVS out of the current latch condition and back to normal operation, the overload must be removed or the current latch setting increased, and then a new gate signal must be issued.

B-43 The latch status signal does not switch to the latch state if the C_T terminals on the rear of the DVS are shorted (refer to Paragraph 3-33).

B-44 Latch Status Polarity

For this Option, transistor AGA5Q4 serves as the output driver. The signal polarity is as follows:



B-45 POCKET PROGRAMMER 14533B USAGE

B-46 To program the DVS using the HP Pocket Programmer 14533B, refer to the following chart for appropriate switch positions for this particular option. Note that these switch positions may not apply to the "A" version of the Pocket Programmer 14533B.

SWITCH	POSITION
Voltage Magnitude (0, 5-0102) Binary 1 Binary 0	down up
Output Sign Positive Output/ Negative Output	up down
Current Latch (I.22, I.23, I.24)	I.22 I.23 I.24
20mA	up up up
50mA	down up up
70mA	up down up
100mA	down down up
200mA	up up down
500mA	down up down
700mA	up down down
1000mA	down down down
MP/DCPS	down
Input Level Reference	down

B-47 OPTION 062 PARTS LIST

B-48 The following is a tabular listing of the special parts associated with this Option.

Option 062 Replaceable Parts

IMP. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	IMP. PART NO.	RS
A1	Input Board	1		28480	5060-7987	
A1A1R1	(xd, comp 1K Ω \pm 5%, 1/4W	1	CB-1025	01121	0683-1025	1
A1A1R2	(xd, comp 2K Ω \pm 5%, 1/4W	1	CB-2025	01121	0683-2025	1
A1A1R3	(xd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
A1A2 through A1A17	Same as A1A1	16				
A1Q1	Omit Q1					
A1Q6	SS NPN SI.	1		28480	1854-0071	1
A1Q7	Omit Q7					
A1R1	(xd, comp 1K Ω \pm 5%, 1/4W	1	CB-1025	01121	0683-1025	1
A1R2	(xd, comp 2K Ω \pm 5%, 1/4W	1	CB-2025	01121	0683-2025	1
A1R3	(xd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
A1R4	Omit R4					
A1R15	(xd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
A1R17	(xd, comp 2.7 Ω \pm 5%, 1/4W	1	CB-0275	01121	0683-0275	1
A1R18, R19	Omit R18 and R19					
A1VR5	Omit VR5					
A2 Z1-Z4 Z9-Z12	Logic Board Quad, D-Type Latch, IC Omit Z9-Z12 (SN7475 installed in Z1-Z4 locations)	4	SN7475	28480 01295	5060-7989 1820-0301	4
A6 A6A1R1 A6A1R2 A6A1R3	Control Board (xd, comp 1K Ω \pm 5%, 1/4W (xd, comp 2K Ω \pm 5%, 1/4W (xd, comp 10K Ω \pm 5%, 1/4W	1 1 1 1	CB-1025 CB-2025 CB-1035	28480 01121 01121 01121	5060-7994 0683-1025 0683-2025 0683-1035	1 1 1 1
A6A2 through A6A4 A6A5R8 A6A5VR1 A6A6Q4 A6A6R7, R8 A6A6VR1 A6CR14, 15	Same as A6A1 Omit A6A5R8 Omit A6A5VR1 Omit A6A6Q4 Omit A6A6R7, R8 Omit A6A6VR1 Diode, SI, 200mA 75V	3 1 1 1 2		28480	1901-0050	

APPENDIX C OPTION 064-Binary Interface For Microcircuit Logic Levels

C-1 INTRODUCTION

C-2 This Appendix describes the input and output data parameters for interfacing with a digital Binary source employing microcircuits of the TTL or DTL family. Only interfacing requirements are discussed in this Appendix. Information of a more general nature is given in Section III of this manual. Hence, for a complete conception of the operating and interfacing requirements, both this Appendix and Section III must be consulted.

C-3 The data parameters described in the following paragraphs include the following:

- (1) Binary voltage magnitude data.
- (2) Input/output signal polarity.
- (3) Logic coding - significance of high and low input/output signal states.
- (4) Logic levels - voltage limits for high and low digital signal states.

C-4 The digital input/output stages on three of the DVS plug-in boards (A1, A2 and A6) have been especially designed to obtain the desired data parameters under worst case conditions. A list of these parts is included at the rear of this Appendix.

C-5 DATA CONNECTOR

C-6 Input/output data is connected to the digital programming source by means of the rear connector (Figure C-1). The parameters associated with each of the signals of Figure C-1 are discussed in the following paragraphs.

C-7 INPUT/OUTPUT SIGNAL POLARITY

C-8 All input/output signal are of positive polarity; i.e. are above 0 volts. Therefore, the input/output stages on A1 (input board) and A6 (control board) use NPN transistors as shown in the schematic (Figure 7-2) provided in the manual.

C-9 RECEIVER CIRCUITS AND LOGIC LEVELS

C-10 Figure C-2 shows an input circuit that applies to all of the digital inputs listed on the drawing. The three resistors of the input voltage divider are selected so that a high input level will turn-on the succeeding driver stage and a low in-

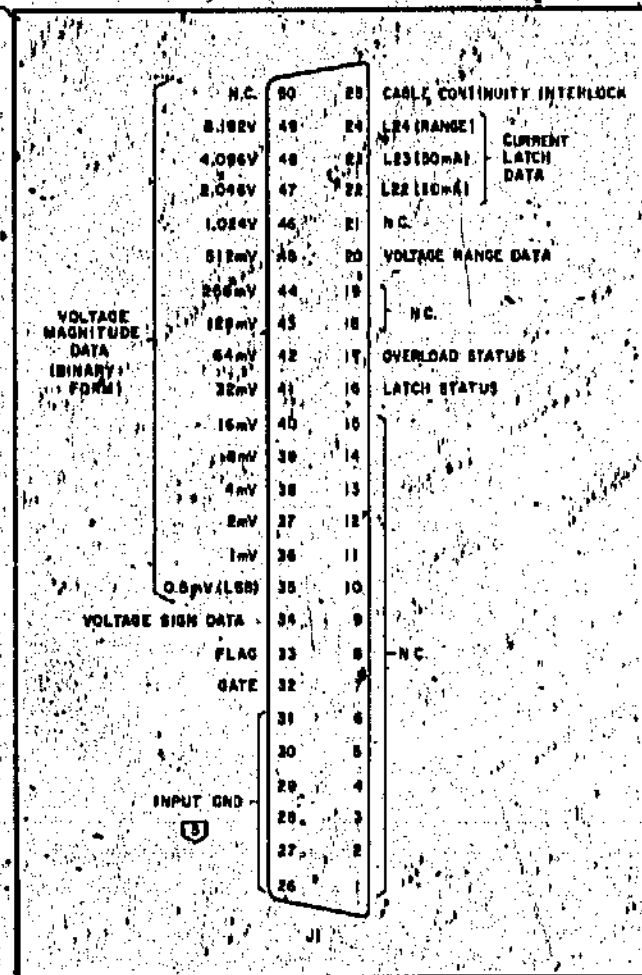


Figure C-1 Input/Output Data Connector

put level will cut the stage off. As shown on Figure C-2, the logic levels for all of the listed inputs are high = +1.9V to +15.5V and low = -4.4V to +1.3V.

C-11 The maximum current that can be drawn from the input circuit when the input terminals are short circuited is 1mA (designated I_{SC-MAX} on Figure C-2). The maximum voltage can appear across the input terminals under open circuit conditions (designated E_{OC-MAX}) is 3.8V.

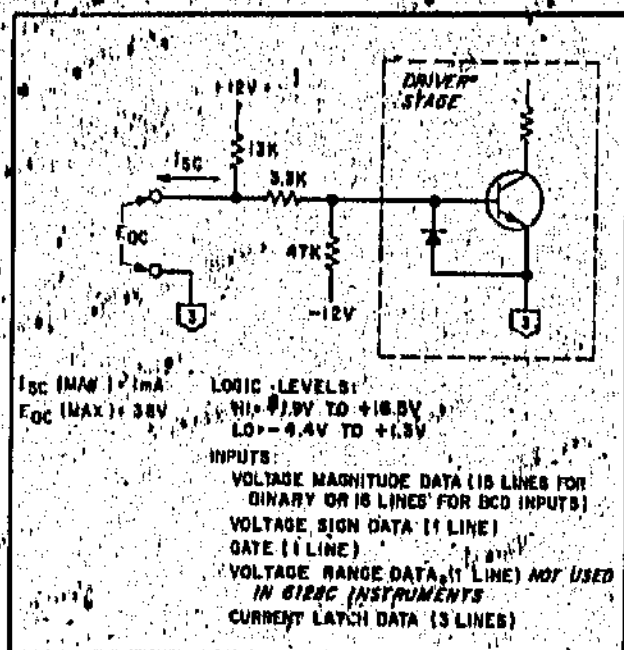
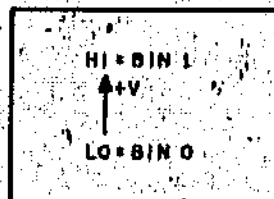


Figure C-2. Receiver Circuit

C-12 VOLTAGE MAGNITUDE INPUT DATA

C-13 Logic Type. The input data to the unit is received in a binary code. Positive numbers are received from the computer in straight binary form while negative numbers are received in 2's complement form, which will be discussed later.

C-14 Logic Coding.



C-15 Logic Inversion. The A2 storage inverters for the voltage magnitude bits are excluded for the logic coding (HI = BIN 1) associated with this option as shown in Figure 7-2, Sheet 1 (the storage IC's are installed in the Z9-Z12 positions).

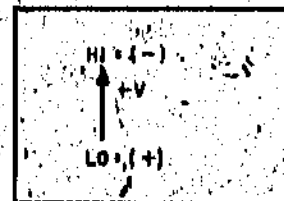
C-16 The voltage magnitude input data is made up of 15 binary bits designated according to their positive analog equivalent value in millivolts (8192, 4096, 2048, ... 0.5). This input data is used in conjunction with the voltage sign and voltage range data to control the output voltage of the DVS. The voltage magnitude data is programmed into the unit in straight binary form when the voltage sign program is positive, and in negative 2's complement form when the voltage sign program is negative. Negative 2's complement form consists of complementing the equivalent positive binary number (all ones become zeros, all zeros become ones)

and adding a binary 1 to the least significant bit. The voltage sign data determines the polarity of the output voltage while the voltage range program select multiplies the voltage program data by X1 or X10. Hence, the output of the DVS may be programmed between -16,384 and +16,386 volts (X1 or X10). Notice that for 6130C instruments, numbers beyond 5.0 in the X10 range are not valid because the maximum rated output voltage for this unit is 50V. As explained in Section III, the output voltage of the 6130C is limited to approximately 55 volts maximum.

C-17 VOLTAGE SIGN

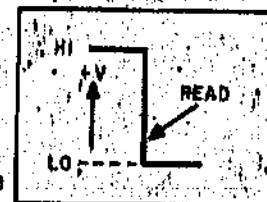
C-18 The voltage sign data bit determines the polarity of the output. Jumper connection A2W1-A (Figure 7-2, Sheet 1) is included for the coding shown below.

C-19 Logic Coding.



C-20 GATE

C-21 Coding. As shown, a high to low transition of the gate input permits storage of the voltage magnitude, voltage sign, current latch, and voltage range input data in the DVS storage registers. Notice that the STORAGE switch on the A2 P.C. Board (see Figure 3-2) must be in the STORE position to utilize this storage capability.



C-22 VOLTAGE RANGE

C-23 Coding. HI = X10 (High voltage range).
LO = X1 (Low voltage range).

C-24 The following chart shows the coding required for voltage range.

INPUT CODE		VOLTAGE RANGE
Voltage Range Bit		
LO		X1
HI		X10

C-25 CURRENT LATCH

C-26 Coding. The current latch data forms a bit binary code. The input codes for each current latch value are shown in the chart on page 3-1. Notice that the three current latch bits provide a maximum of eight possible combinations.

C-27 Cr Terminals. As described in Section III, the current latch delay period is determined by the condition of the Cr terminals at the rear of the unit. Notice that if the Cr terminals are shorted, the DVS will not current latch even if the output current exceeds the programmed current latch value.

C-28 CABLE CONTINUITY INTERLOCK

C-29 Before output voltage can be obtained from the DVS, a connection must be made between input common (3) and the cable continuity interlock pin 25 of the input/output connector. If this connection is not made, the output terminals of the DVS will be shorted by an internal relay. This protects the load device against excessive voltages in case the input cable is disconnected.

C-30 Cable Continuity Interlock Receiver Circuit. Figure C-3 shows the cable continuity interlock

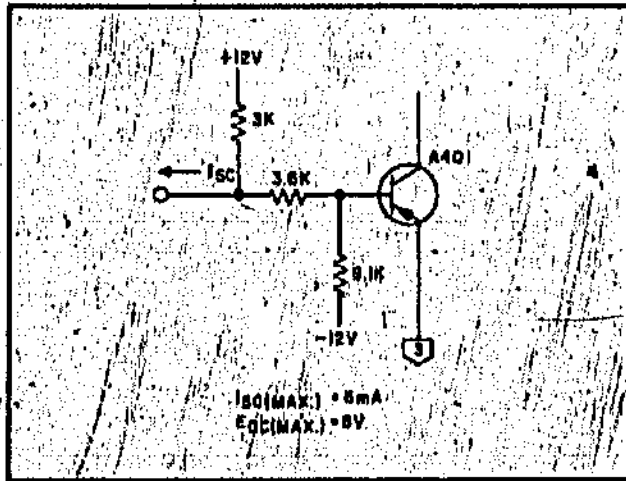


Figure C-3. Cable Continuity Interlock Receiver Circuit

receiver circuit. The three input voltage divider resistors are selected so that a 3 common input will cause A401 to saturate and an open (no input connection) will cause A401 to cut off. The maximum current (I_{SC-MAX}) that could be drawn from the input circuit when the input terminals are short circuited is 6mA. The maximum voltage (E_{OC-MAX}) that appears across the input terminals under open circuit conditions is 8V.

C-31 INPUT GROUND

C-32 Input data must be connected to 3 common of the DVS (pins 26 through 31) shown on Figure C-1. These pins are internally shorted together within the connector jack.

C-33 OUTPUT DRIVER CIRCUITS

C-34 Figure C-4 shows the output driver circuit that is used for each output signal; namely, flag, overload status, and latch status. Transistors A105, A6A5A4, and A6A5C1 serve as the output driver transistors. A zener diode in each output circuit prevents the output voltage from exceeding +4.4V (max) when the output driver is out of high output condition.

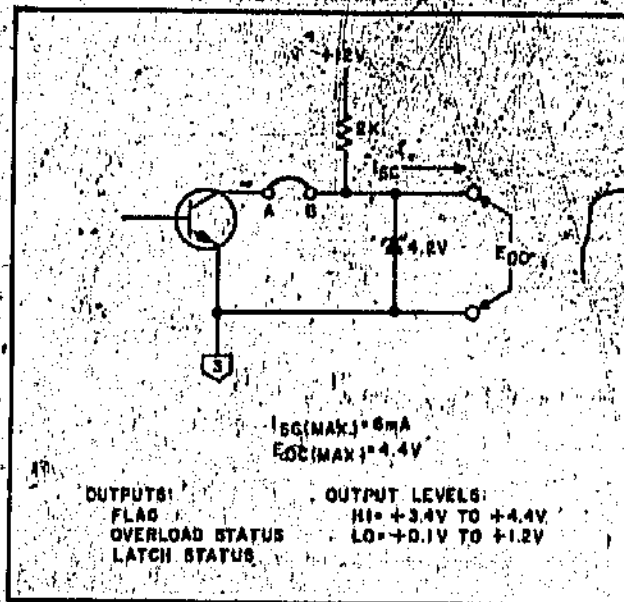


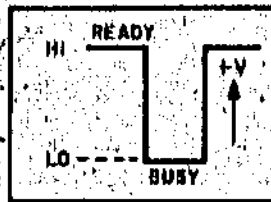
Figure C-4. Driver Circuit

C-35 With the output terminals shorted, the maximum current (I_{SC-MAX}) that can be drawn from the driver circuit is 6mA. With the output terminals open, the maximum voltage (as determined by the zener diode) is +4.4V.

C-36 FLAG OUTPUT

C-37 Flag output signals are issued under three separate conditions. As described in Section III, the flag output switches from ready to busy during: (1) processing of the voltage magnitude data bits, (2) changing of the voltage range, and (3) current overload periods. The time that the flag remains in the busy state is different for each of the three conditions (see Figures 3-4, 3-5, and 3-7).

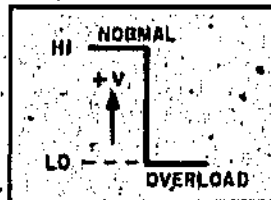
C-38 Clay Polarity. For this option, transistor A1Q5 and resistor A1R15 are not supplied. Jumpers W14 and W15 are installed, and resistor R10 (the load for A1Q5) and zener diode A1VR5 are included. The flag polarity, therefore is as follows:



C-39 OVERLOAD STATUS

C-40 The overload status line switches to the overload state whenever the output current exceeds the programmed current latch value (see Figure 3-7). The signal remains in the overload state until the output current is decreased (unit goes into current latch or overload is removed).

C-41 Overload Status Polarity. For this option, transistor A6A6Q4 and resistor A6A6R7 is not supplied and jumper A6A6Q3 serves as the output transistor with resistor A6A6R8 (load for A6A6Q3) and zener diode A6A6VR1 included. The output signal polarity is as follows:



C-42 LATCH STATUS

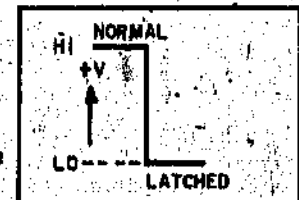
C-43 The latch status line switches to the latch state if the unit goes from the overload to the latch state (Figure 3-7). In the latch condition, the output current is limited to less than 10mA. The latch status signal will revert from the overload latch state to the normal state approximately 10 μ sec after the next gate input is received, providing that the next gate input is received, providing that the overload condition no longer exists. Therefore, to program the DVS out of the current latch condition and back to normal operation, the overload must be removed or the current latch setting increased; and then a new gate signal must be issued.

C-44 The latch status signal does not switch to the latched state if the CT terminals on the rear of the DVS are shorted (refer to Paragraph 3-33).

SWITCH	POSITION
Voltage Magnitude (0, 5-0192) Binary 1 Binary 0	up down
Output Voltage Positive Output Negative Output	down up
Current Latch (L22, L23, L24) 20mA 50mA 70mA 100mA 200mA 500mA 700mA 1000mA	L22 up down up down up down up down up down down down down
Mp/DCPS	down
Input Level Reference	down

C-45 Latch Status Polarity.

For this Option, Transistor A6A5Q4 serves as the output driver with resistor A6A5R8 installed for its load. Zener diode A6A5VR1 is included. The output signal polarity is as follows:



C-46 POCKET PROGRAMMER 14533B USAGE

C-47 To program the DVS using the HP Pocket Programmer 14533B, refer to the preceding chart for appropriate switch positions for this particular option. Note that these switch positions may not apply to the "A" version of the Pocket Programmer 14533A.

C-48 OPTION 064 PARTS LIST

C-49 The following is a tabular listing of the special parts associated with this Option.

Option 064 Replaceable Parts

REF. DESIG.	DESCRIPTION	TO	MFR. PART NO.	MFR. CODE	IIP PART NO.	RS
A1	Input Board	1		28480	5060-7988	
A1AIR1	fxd, comp 13K Ω \pm 5%, 1/4W	1	CB-1335	01121	0683-1335	1
A1AIR2	fxd, comp 3.3K Ω \pm 5%, 1/4W	1	CB-3325	01121	0683-3325	1
A1AIR3	fxd, comp 47K Ω \pm 5%, 1/4W	1	CB-4735	01121	0683-4735	1
A1A2 through A1A17	Same as A1A1	16				
A1Q1, Q6, Q7	Omit Q1, Q6, Q7					
A1R1	fxd, comp 13K Ω \pm 5%, 1/4W	1	CB-1335	01121	0683-1335	1
A1R2	fxd, comp 3.3K Ω \pm 5%, 1/4W	1	CB-3325	01121	0683-3325	1
A1R3	fxd, comp 47K Ω \pm 5%, 1/4W	1	CB-4735	01121	0683-4735	1
A1R4, R15, R17	Omit R4, R15, R17					
A1R18	fxd, comp 2K Ω \pm 5%, 1/4W	1	CB-2025	01121	0683-2025	1
A1R19	Omit R19					
A1VR5	Diode, zener 4.22V \pm 5%	1		28480	1902-3070	1
A2	Logic Board	1		28480	5060-7990	
A2Z1-24	Omit Z1-24 (8N7475's installed in Z9-Z12 locations)					
A2Z9-Z12	Quad, D-Type Latch, IC	4	8N7475	01295	1820-0301	4
A6	Control Board	1		28480	5060-7995	
A6AIR1	fxd, comp 13K Ω \pm 5%, 1/4W	1	CB-1335	01121	0683-1335	1
A6AIR2	fxd, comp 3.3K Ω \pm 5%, 1/4W	1	CB-3325	01121	0683-3325	1
A6AIR3	fxd, comp 47K Ω \pm 5%, 1/4W	1	CB-4735	01121	0683-4735	1
A6A2 through A6A4	Same as A6A1	3				
A6A5R8	fxd, comp 2K Ω \pm 5% 1/2W	1	EB-2025	01121	0686-2025	1
A6A5VR1	Diode, zener 4.22V \pm 5%	1		28480	1902-3070	1
A6AQ4	Omit A6AQ4					
A6AR7	Omit A6AR7					
A6AR8	fxd, comp 2K Ω \pm 5%, 1/2W	1	EB-2025	01121	0686-2025	1
A6AVR1	Diode, zener 4.22V \pm 5%	1		28480	1902-3070	1
A6CR14, CR15	Diode, Si. 200mA 75V	2		28480	1901-0050	2

SECTION VII CIRCUIT DIAGRAMS

7-1 INTRODUCTION

7-2 This section contains the circuit diagrams necessary for the operation and maintenance of Model 6130C Digital Voltage Source.

7-3 OVERALL BLOCK DIAGRAM

7-4 This diagram, Figure 7-1, shows the relationship between the instrument assemblies and ties the schematic diagrams together. A timing diagram is provided in Figure 7-1 to aid in the understanding of the operation of the instrument.

7-5 COMPONENT LOCATION ILLUSTRATIONS

7-6 The component location diagrams show the physical location of parts mounted on each assembly. They are included on the schematic diagrams where they apply or on the rear of the previous schematic. Thus, the schematic diagram is unfolded to the right and component location dia-

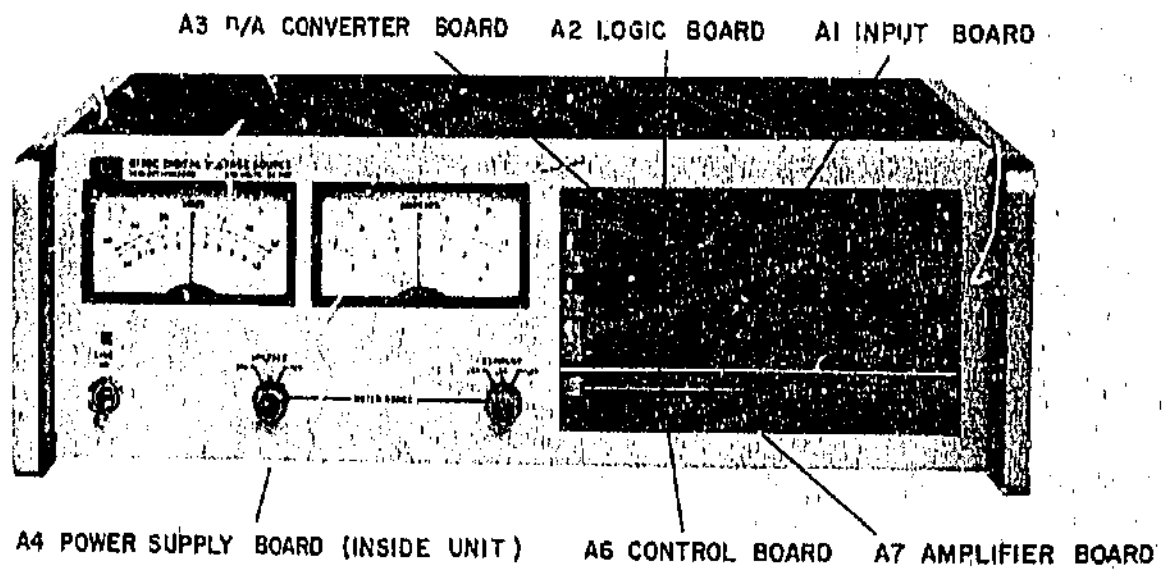
gram is unfolded to the left.

7-7 SCHEMATIC DIAGRAMS

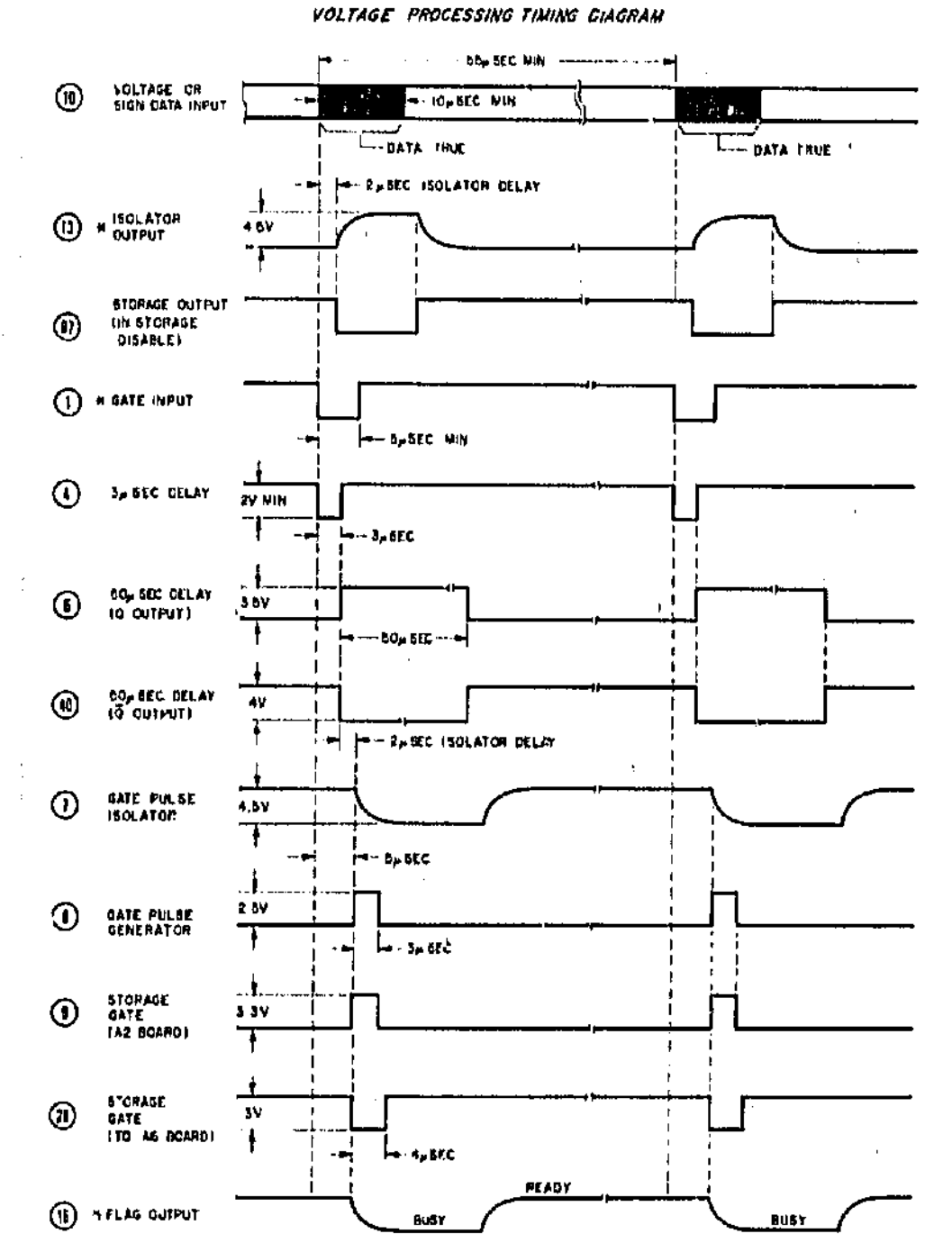
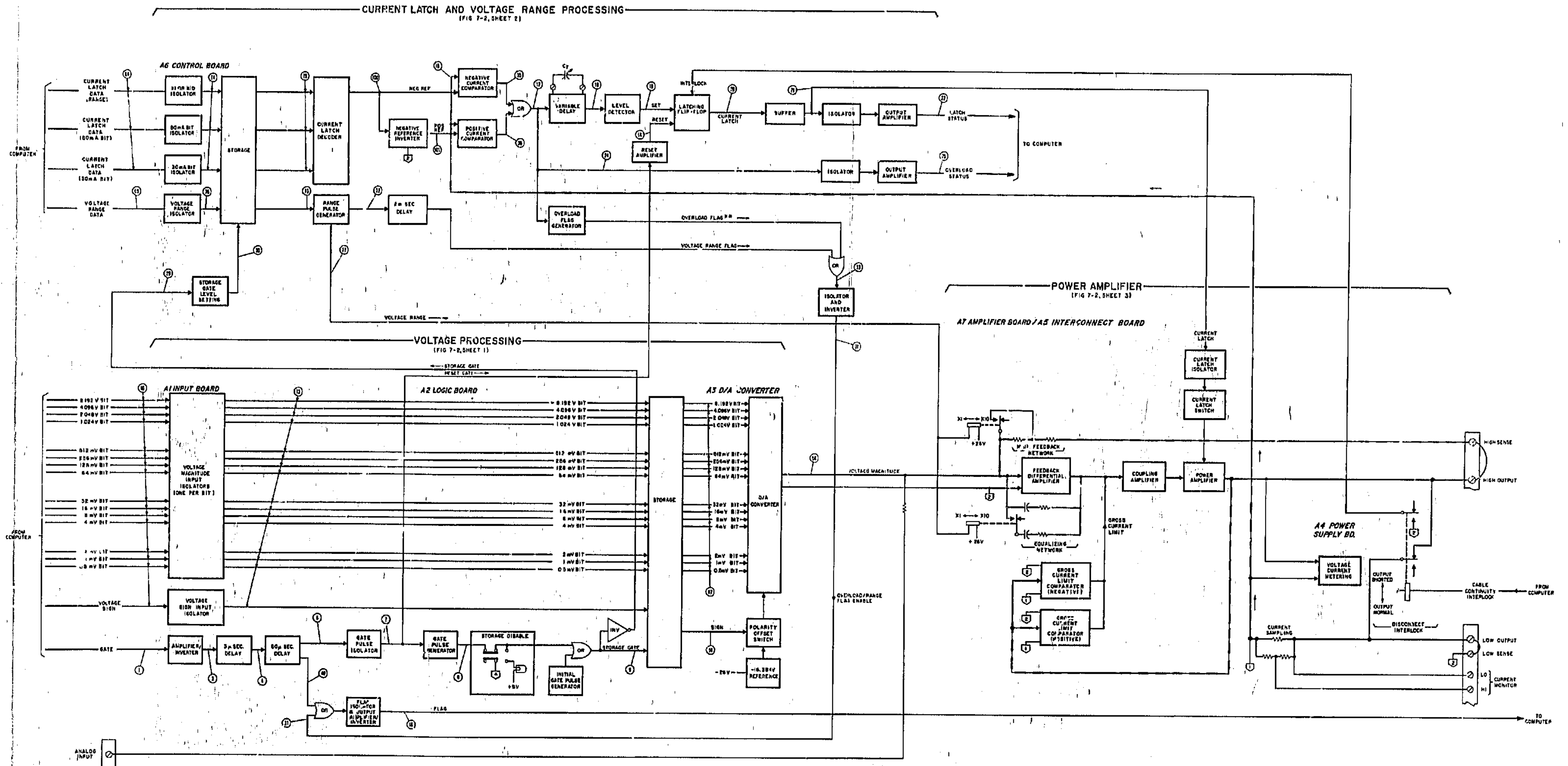
7-8 The circuits are functionally separated and included on a series of schematic diagrams, Figure 7-2, Sheets 1 through 4. Voltage Processing Circuits are contained on Sheet 1. The Current Latch Circuits are contained on Sheet 2. The signals from Sheets 1 and 2 are connected to the Power Amplifier, Sheet 3.

7-9 The Power Distribution Schematic Diagram, Figure 7-2, Sheet 4, illustrates the input ac, dc power supplies, and the distribution of dc voltages throughout the unit.

7-10 Test points (encircled numbers) appear through the schematics. These points coincide with the test points on the component locations diagrams and are referred to throughout the text.

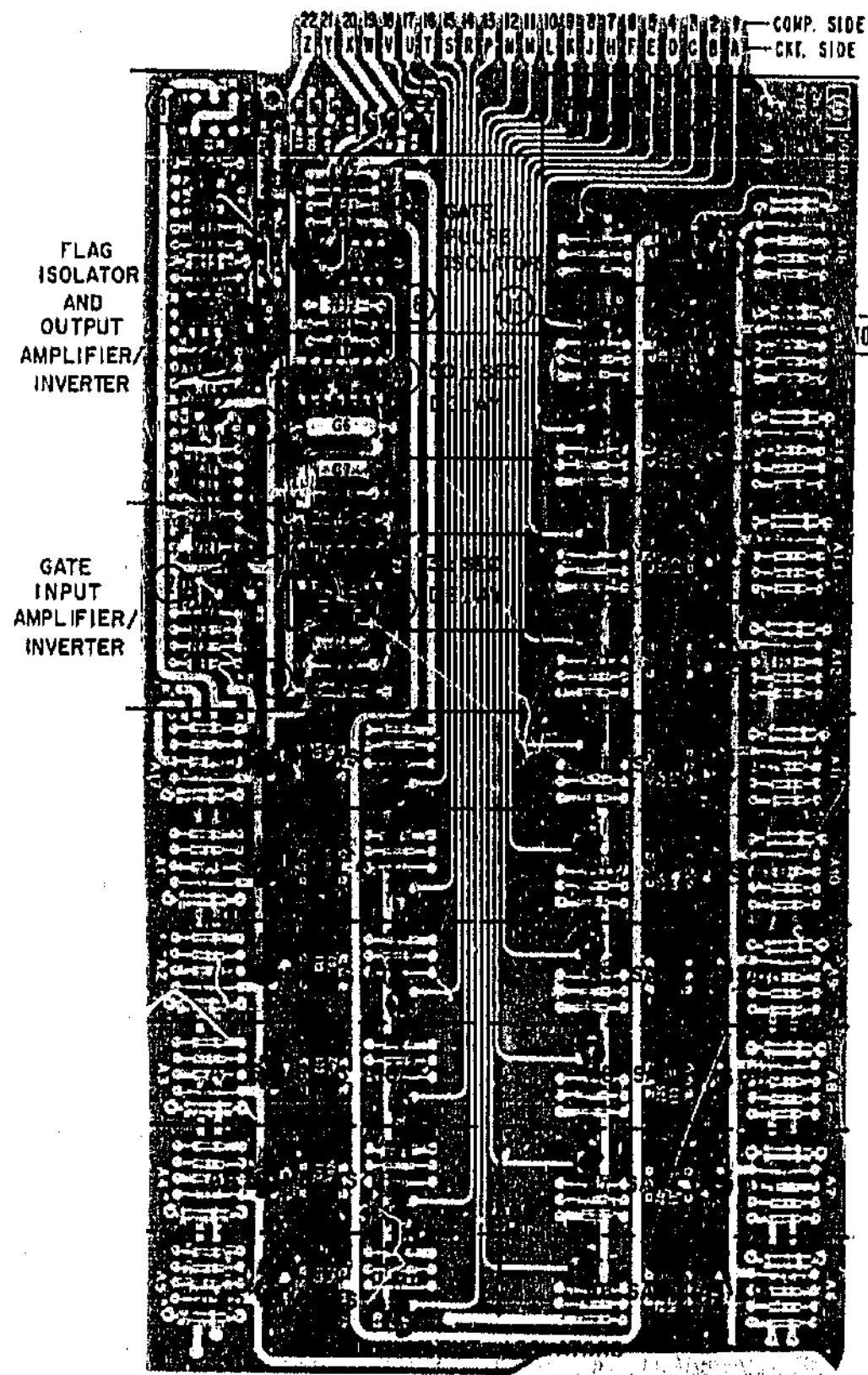


Subassembly Location

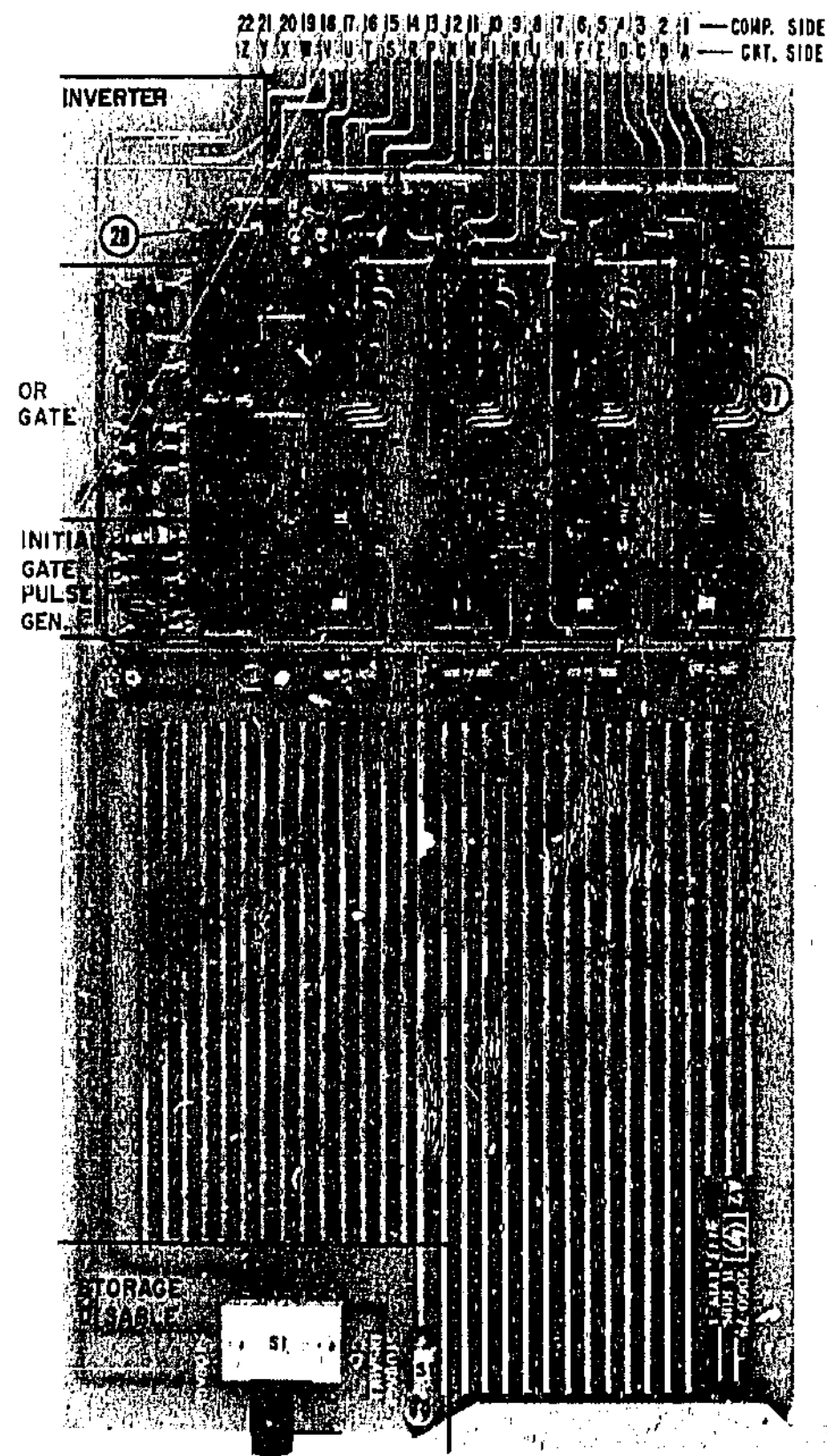


NOTE: 1. POLARITY SHOWN IS AN EXAMPLE. ACTUAL POLARITY DEPENDS ON COMPUTER DRIVER OR RECEIVER CIRCUITS. REFER TO APPROPRIATE OPTION OR MODIFICATION SHEET.
2. OVERLOAD FLAG DISABLED FOR J20 OPTION.

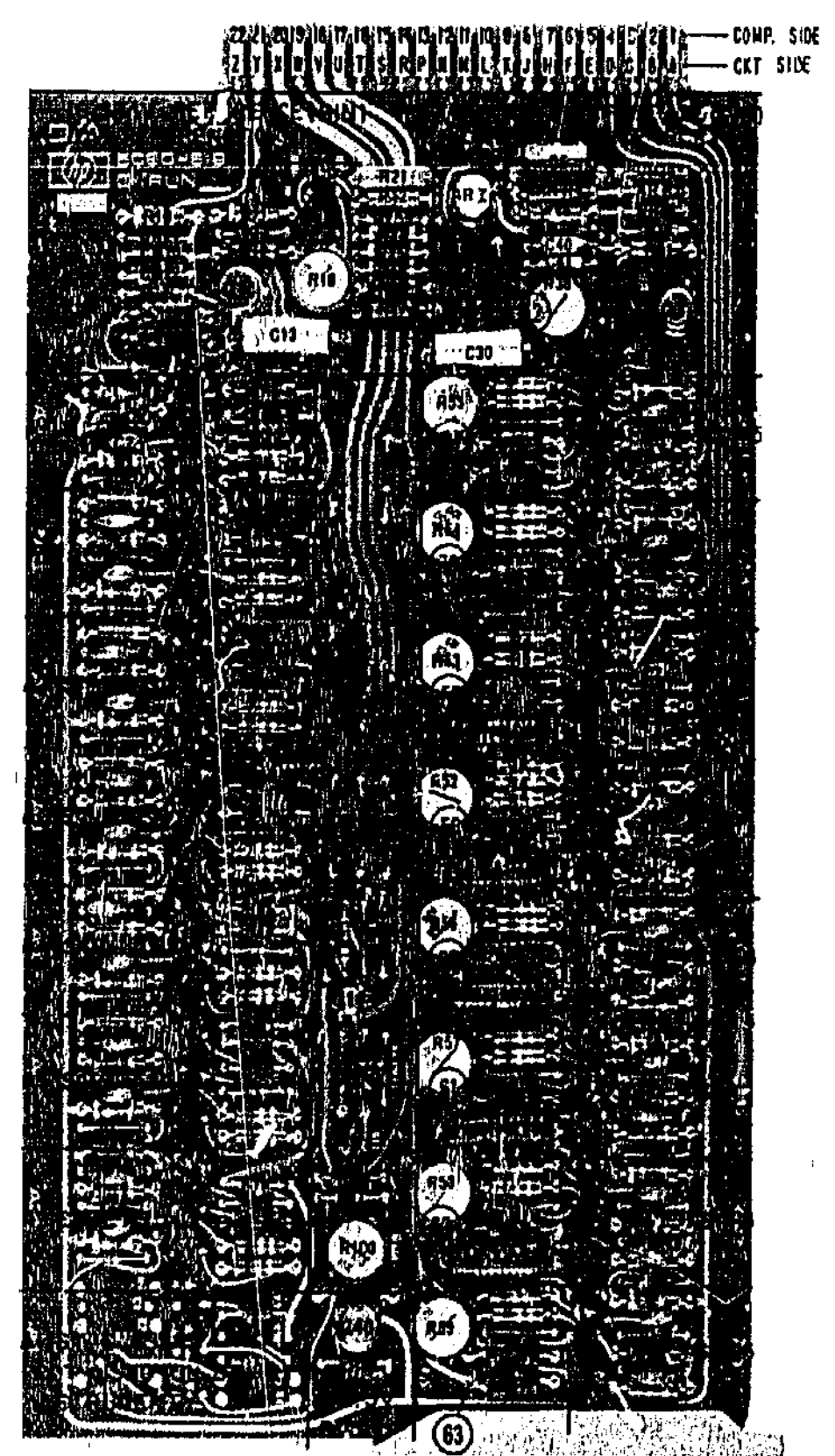
Figure 7-1. Overall Block and Timing Diagram



A1 Input Board, Component Location



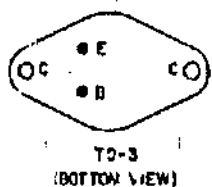
A2 Logic Board, Component Location



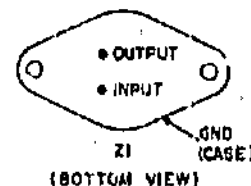
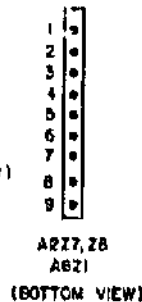
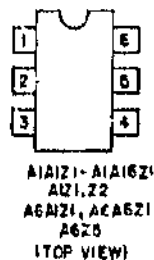
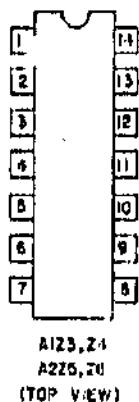
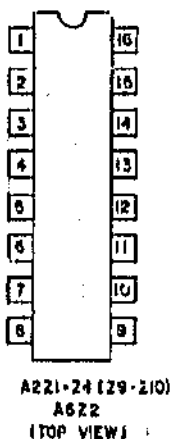
A3 D/A Board, Component Location

NOTES

1. ALL RESISTORS ARE IN OHMS, 1/2W, 5%, UNLESS OTHERWISE INDICATED
2. ALL 1/4W AND 1/8W RESISTORS ARE 1%, UNLESS OTHERWISE INDICATED.
3. ALL CAPACITORS ARE IN MICROFARADS, UNLESS OTHERWISE INDICATED.
4. [] DENOTES FRONT PANEL MARKING
5. [] DENOTES REAR PANEL MARKING
6. M DENOTES CHASSIS-MOUNTED COMPONENT
7. ——— DENOTES VOLTAGE FEEDBACK
8. ——— DENOTES CURRENT FEEDBACK
9. PIN LOCATIONS FOR TRANSISTORS ARE AS FOLLOWS



10. PIN LOCATIONS FOR INTEGRATED CIRCUITS ARE AS FOLLOWS



11. THE RESISTANCE VALUES OF BIAS RESISTORS R1-D DEPEND ON THE STANDARD OPTION OF THE INSTRUMENT OR WHETHER THE INSTRUMENT IS A SPECIAL MODIFICATION. REFER TO THE APPROPRIATE OPTION APPENDIX OF THE INSTRUMENT MODIFICATION SHEET FOR THIS INFORMATION.
12. THE FOLLOWING COMPONENTS MAY OR MAY NOT BE INCLUDED, DEPENDING ON WHICH STANDARD OPTION APPLIES OR WHETHER THE INSTRUMENT IS A SPECIAL MODIFICATION: A106, A1915, A1R17, A1R18, A1VR5, A6CR14, A6CR15, A6ABR8, A6AER8, A6ABVR1, AND A6AVR1 REFER TO THE APPROPRIATE OPTION APPENDIX OR THE INSTRUMENT MODIFICATION SHEET FOR INFORMATION ON THESE COMPONENTS.
13. THESE JUMPERS ON THE A1 AND A6 BOARDS ARE POSITIONED AS SHOWN EXCEPT IN SPECIALLY-MODIFIED INSTRUMENTS REFER TO THE INSTRUMENT MODIFICATION SHEET SUPPLIED WITH THE INSTRUMENT.
14. THE FOLLOWING COMPONENTS, DRAWN WITH DASHED LINES, ARE NOT INCLUDED EXCEPT IN SPECIALLY-MODIFIED INSTRUMENTS: A1Q1, A1Q7, A1R4, AND A1R10. REFER TO THE INSTRUMENT MODIFICATION SHEET SUPPLIED WITH THE MANUAL.
15. THE OUTPUT POLARITY OF THE FOUR STORAGE IC PACKAGES ON THE A2 BOARD DEPENDS ON WHETHER THEY ARE LOCATED IN THE Z1 THROUGH Z4 OR THE ZD THROUGH Z12 SOCKETS. THE JUMPERS DRAWN AT THE OUTPUTS REPRESENT THIS CHOICE OF SOCKETS. THE APPROPRIATE OPTION APPENDIX IDENTIFIES WHICH ARE THE PROPER SOCKETS.
16. THE POSITION OF THIS JUMPER ON THE A2 BOARD DEPENDS ON THE STANDARD OPTION OF THE INSTRUMENT OR WHETHER THE INSTRUMENT IS A SPECIAL MODIFICATION. IN OPTION J20 OR OPTION 062 INSTRUMENTS, W1 IS CONNECTED TO B. IN OPTION 064 INSTRUMENTS, W1 IS CONNECTED TO A. FOR SPECIALLY-MODIFIED INSTRUMENTS, REFER TO THE INSTRUMENT MODIFICATION SHEET FOR THIS INFORMATION.
17. FOR SPECIALLY-MODIFIED INSTRUMENTS, THE CIRCUIT CONFIGURATION OF OUTPUT AMPLIFIER STAGES A6A5Q3, A6A5Q4, A6A6Q3, AND A6A6Q4 MAY DIFFER FROM SCHEMATIC. NOTE THAT A6A6Q4 AND A6A6R7 ARE NOT INCLUDED IN ANY OF THE STANDARD OPTIONS. REFER TO THE INSTRUMENT MODIFICATION SHEET SUPPLIED WITH THE INSTRUMENT.

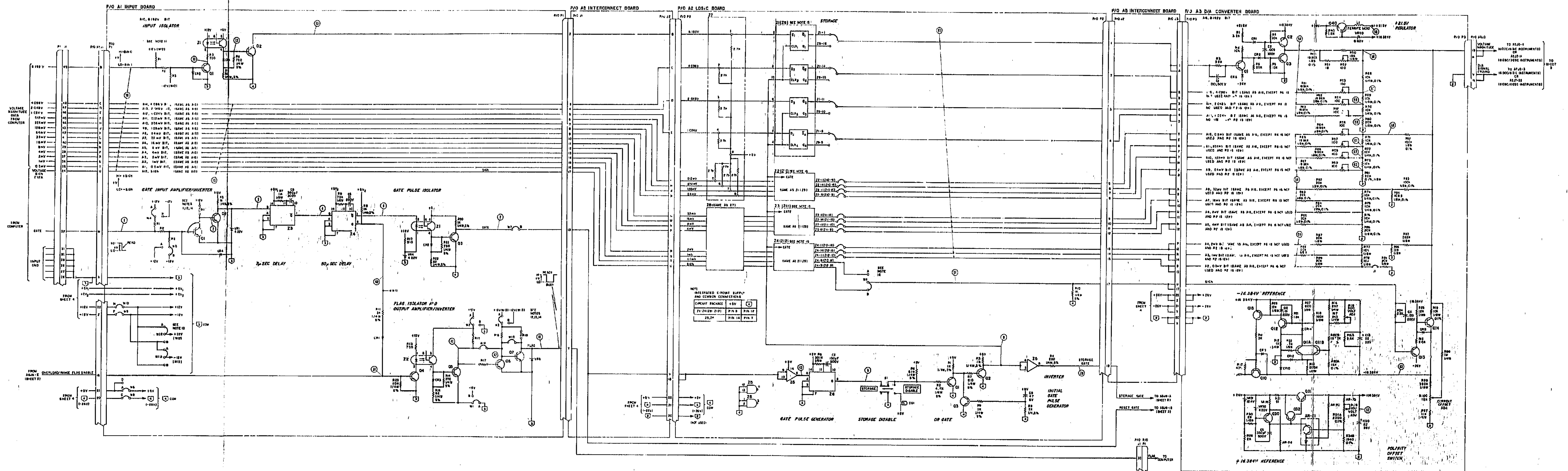
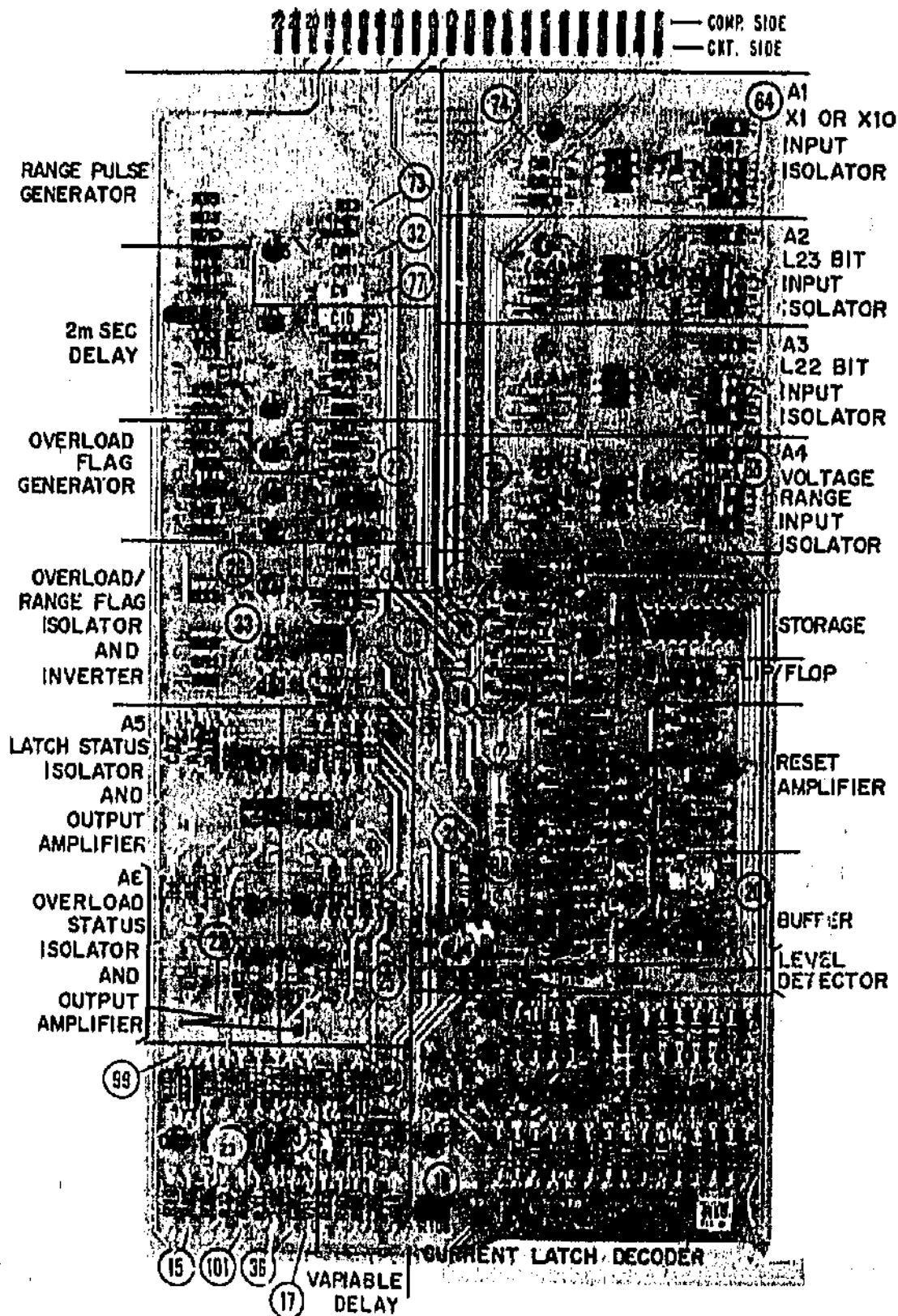


Figure 7-2 (Sheet 1). Voltage Processing, Schematic Diagram



A6 Control Board, Component Location

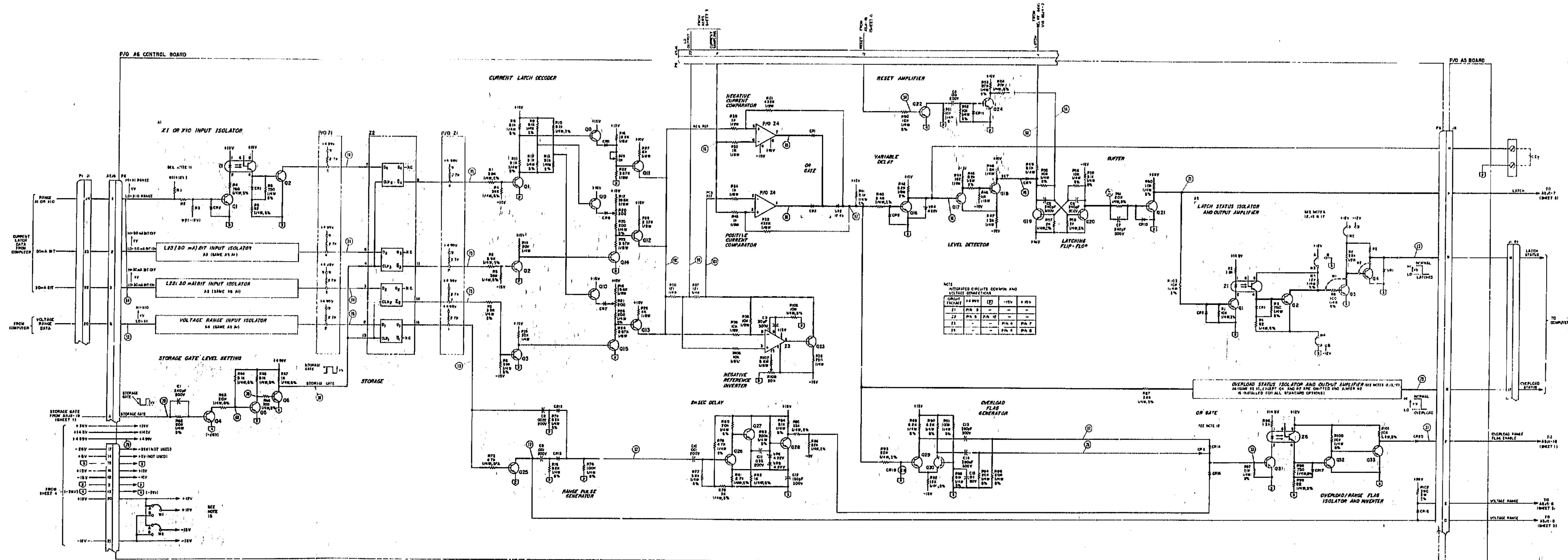
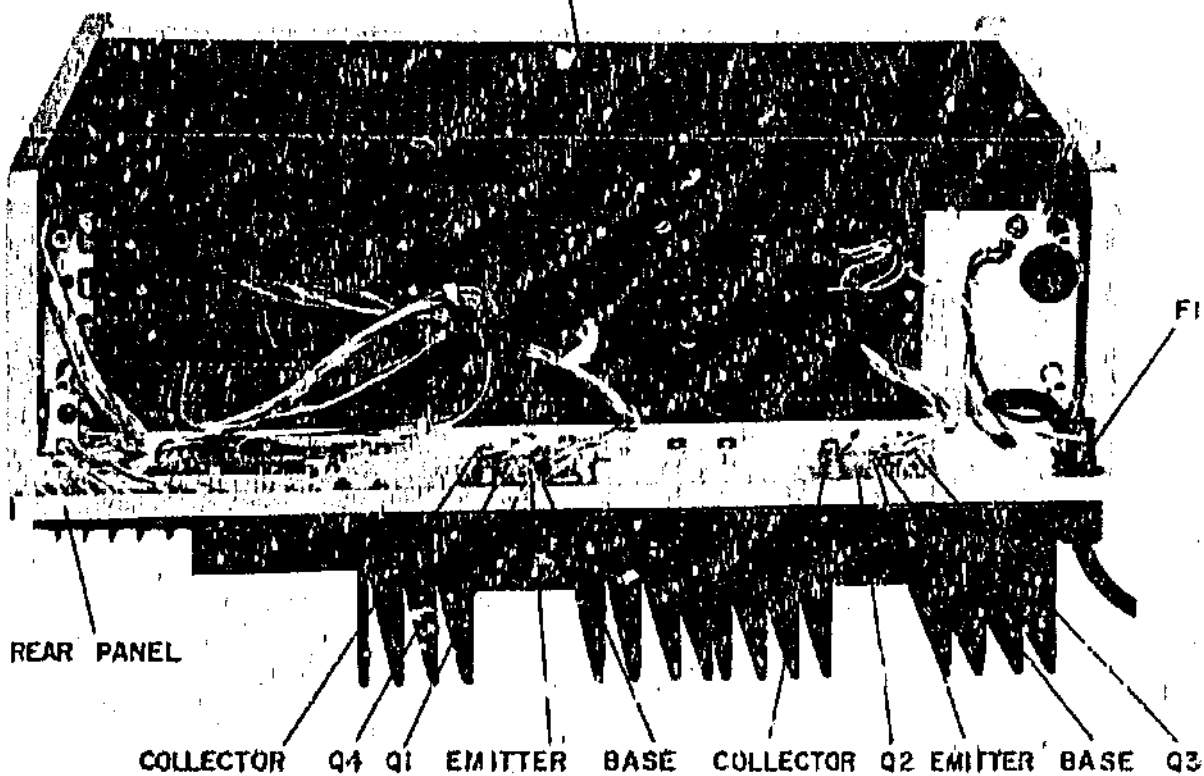


Figure 7-2 (Sheet 2). Current Latch and Voltage Range Processing, Schematic Diagram

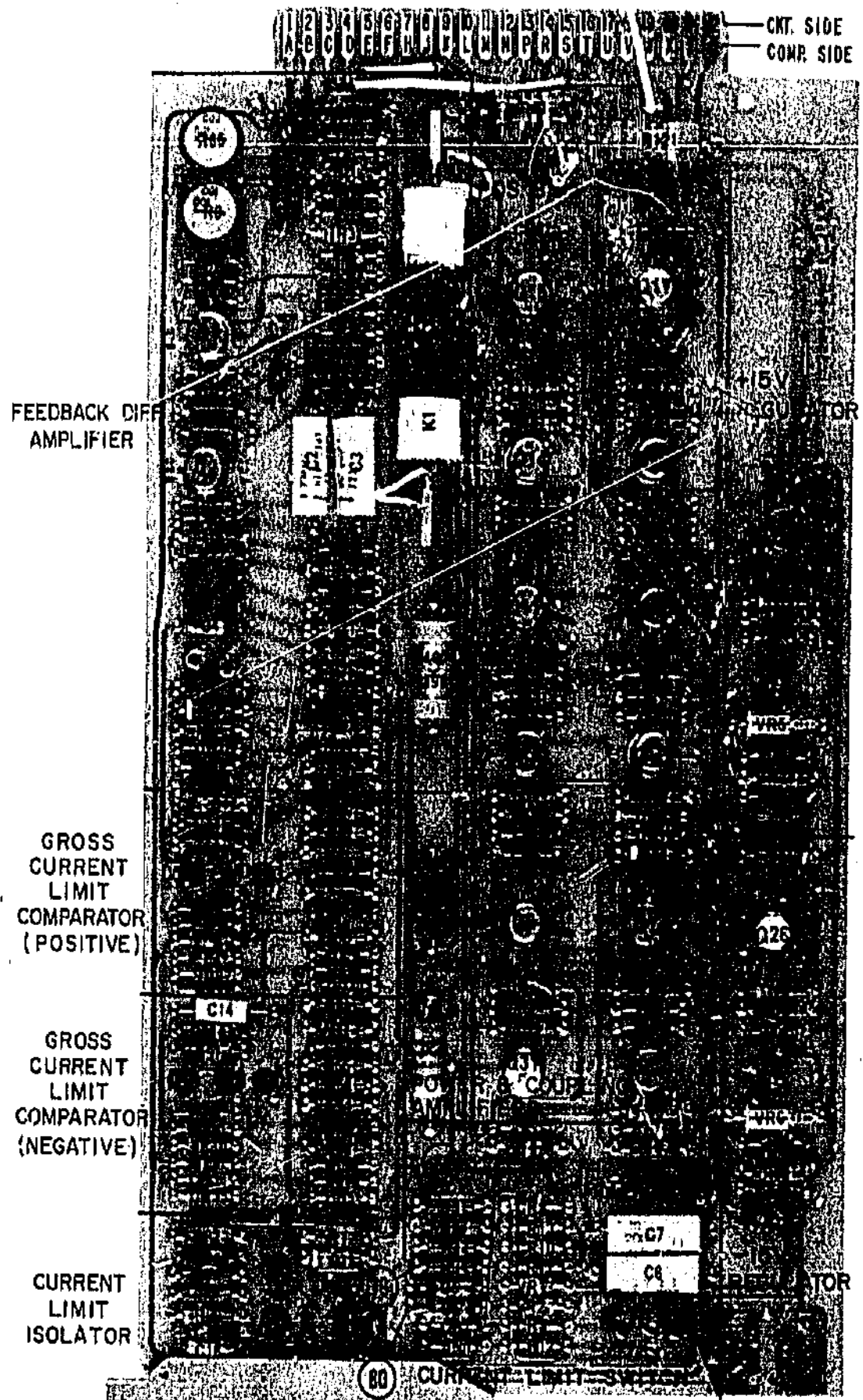
A5 INTERCONNECT BOARD



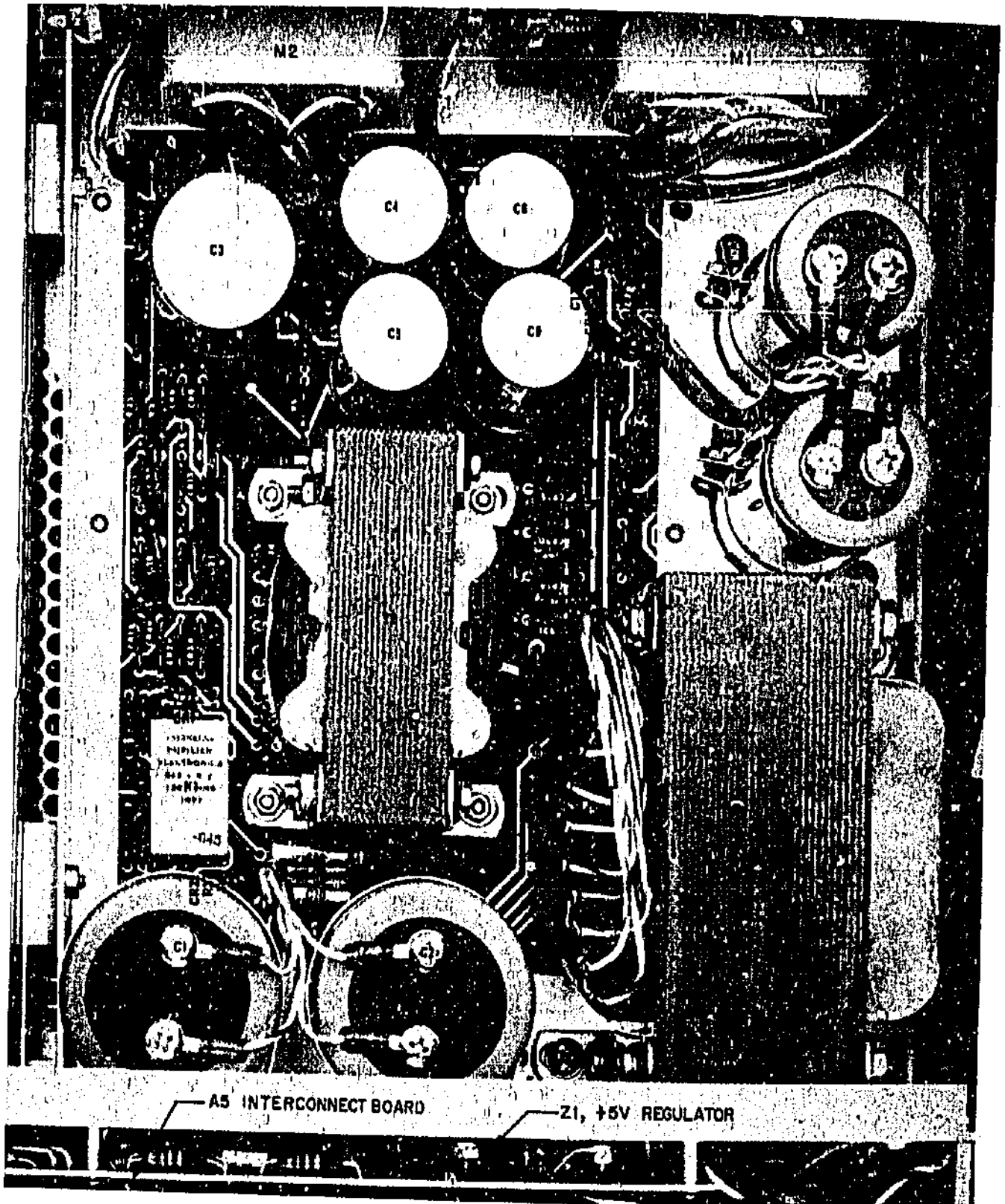
Rear View, Component Location



A5 Interconnect Board, Component Location



A7 Amplifier Board, Component Location



A4 Power Supply Board, Component Location

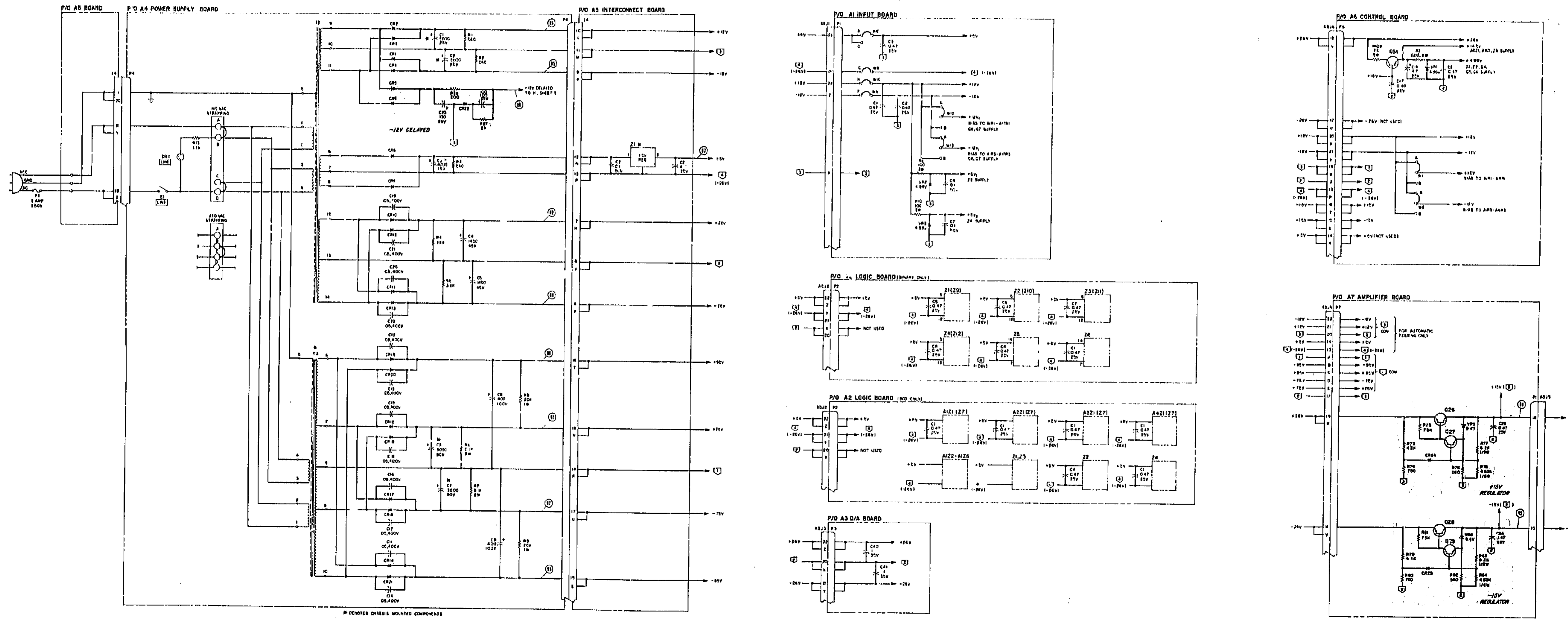


Figure 7-2 (Sheet 4), Power Distribution Schematic Diagram

APPENDIX A

OPTION J20-Binary Interface For The HP 12661A DVS Program Card

A-1 INTRODUCTION

A-2 This Appendix describes the input and output data parameters for interfacing with a digital Binary source employing the HP 12661A DVS Program Card. Only interfacing requirements are discussed in this Appendix. Information of a more general nature is given in Section III of this manual. Hence, for a complete conception of the operating and interfacing requirements, both this Appendix and Section III must be consulted.

A-3 The data parameters described in the following paragraphs include the following:

- (1) Binary voltage magnitude data.
- (2) Input/Output signal polarity.
- (3) Logic coding - significance of high and low input/output signal states.
- (4) Logic levels - voltage limits for high and low digital signal states.

A-4 The digital input/output stages on three of the DVS plug-in boards (A1, A2, and A6) have been especially designed to obtain the desired data parameters under worst case conditions. A list of these special parts is included at the rear of this Appendix.

A-5 DATA CONNECTOR

A-6 Input/output data is connected to the digital programming source by means of the rear connector (Figure A-1). The parameters associated with each of the signals of Figure A-1 are discussed in the following paragraphs.

A-7 INPUT/OUTPUT SIGNAL POLARITY

A-8 All input/output signals are of positive polarity; i.e., are above 0 volts. Therefore, the input/output stages on A1 (input board) and A6 (control board) use NPN transistors as shown in the schematic (Figure 7-2) provided in the manual.

A-9 RECEIVER CIRCUITS AND LOGIC LEVELS

A-10 Figure A-2 shows an input circuit that applies to all of the digital inputs listed on the drawing. The three resistors of the input voltage divider are selected so that a high input level will turn-on the succeeding driver stage and a low input level will cut the stage off. As shown on

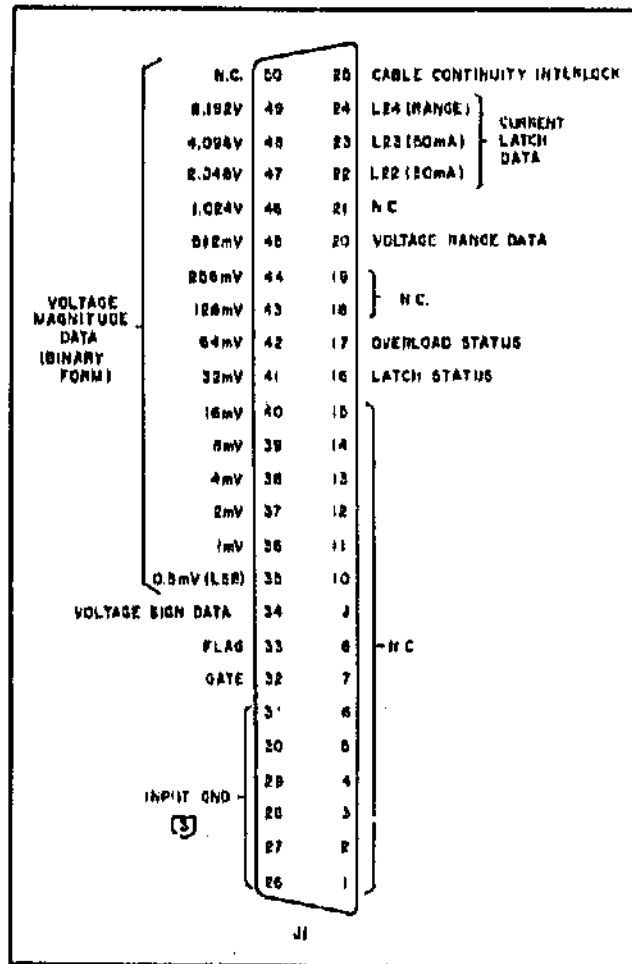


Figure A-1. Input/Output Data Connector

Figure A-2, the logic levels for all of the listed inputs are high = +5.5 to +12V and low = -1 to +2.8V.

A-11 The maximum current that can be drawn from the input circuit when the input terminals are short circuited is 2mA (designated I_{SC-MAX} on Figure A-2). The maximum voltage that can appear across the input terminals under open circuit conditions (designated E_{OC-MAX}) is 9V.

A-12 VOLTAGE MAGNITUDE INPUT DATA

A-13 Logic Type. The input data to this unit is received in a binary code. Positive numbers are received from the computer in straight binary form while negative numbers are received in 2's complement form, which will be discussed later.

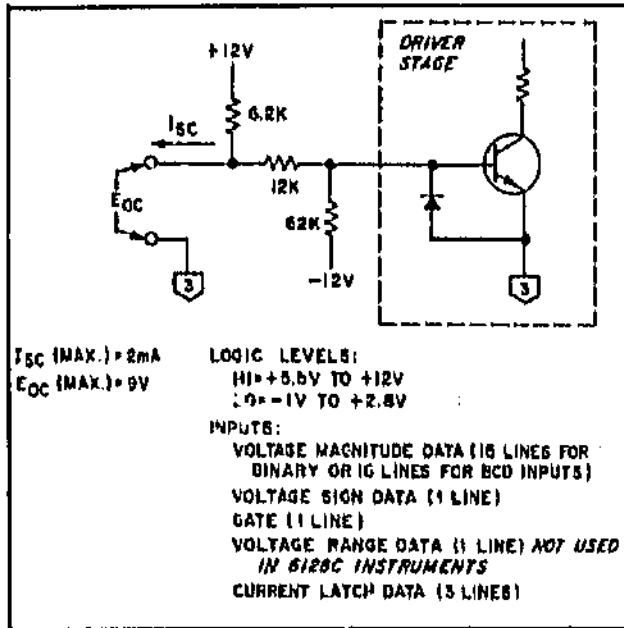
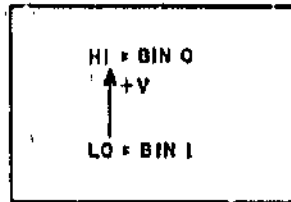


Figure A-2, Receiver Circuit

A-14 Logic Coding.



A-15 Logic Inversion. The A2 storage inverters for the voltage magnitude bits are included for the logic coding (HI = BIN 0) associated with this option; as shown in Figure 7-2, Sheet 1. (The storage IC's are installed in the Z1-24 positions.)

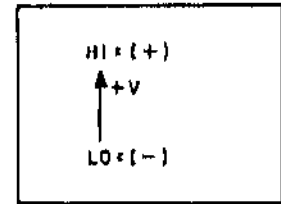
A-16 The voltage magnitude input data is made up of 16 binary bits designated according to their positive analog equivalent value in millivolts (8192, 4096, 2048, . . . 0.5). This input data is used in conjunction with the voltage sign and voltage range data to control the output voltage of the DVS. The voltage magnitude data is programmed into the unit in straight binary form when the voltage sign data is positive, and in 2's complement form when the voltage sign data is negative. 2's complement form consists of complementing the equivalent positive binary number (all ones become zeros, all zeros become ones) and adding a binary 1 to the least significant bit. The voltage sign data determines the polarity of the output voltage while the voltage range program multiplies the voltage program data by X1 or X10. Hence, the output of the DVS may be programmed between -16.384 and +16.385 volts (X1 or X10). Notice that for 6130C instruments, numbers beyond 5.0 in the X10 range are not valid because the maximum rated output

voltage for this unit is 50V. As explained in Section III, the output voltage of the 6130C is limited to approximately 55 volts maximum.

A-17 VOLTAGE SIGN

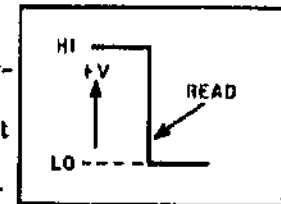
A-18 The voltage sign bit determines the polarity of the output. Jumper connection A2W1-B (Figure 7-2, sheet 1) is included for the coding shown below.

A-19



A-20 GATE

A-21 Coding. As shown, a high to low transition of the gate input permits storage of the voltage magnitude, voltage sign, current latch, and voltage range input data in the DVS storage registers. Notice that the STORAGE switch on the A2 P. C. board (see Figure 3-2) must be in the STORE position to utilize this storage capability.



A-22 VOLTAGE RANGE

A-23 Coding. HI = X10 (High voltage range).
LO = X1 (Low voltage range).

A-24 The following chart shows the coding required for voltage range.

INPUT CODE	VOLTAGE RANGE
Voltage Range Bit	
LO	X1
HI	X10

A-25 CURRENT LATCH

A-26 Coding. The current latch data forms a 3-bit binary code. The input codes for each current latch value are shown in the chart on page 3-5. Notice that the three current latch bits provide a maximum of eight possible combinations.

A-27 CT Terminals. As described in Section III,

the current latch delay period is determined by the condition of the C_T terminals at the rear of the unit. Notice that if the C_T terminals are shorted, the DVS will not current latch even if the output current exceeds the programmed current latch value.

A-28 CABLE CONTINUITY INTERLOCK

A-29 Before output voltage can be obtained from the DVS, a connection must be made between input common (3) and the cable continuity interlock pin 25 of the Input/output connector. If this connection is not made the output terminals of the DVS will be shorted by an internal relay. This protects the load device against excessive voltages in case the input cable is disconnected.

A-30 Cable Continuity Interlock Receiver Circuit. Figure A-3 shows the cable continuity interlock circuit. The three input voltage divider resistors are selected so that a (3) common input will cause A4Q1 to saturate and an open (no input connection) will cause A4Q1 to cutoff. The maximum current (I_{SC-MAX}) that could be drawn from the input circuit when the input terminals are short circuited is 6mA. The maximum voltage (E_{OC-MAX}) that appears across the input terminals under open circuit conditions is 8V.

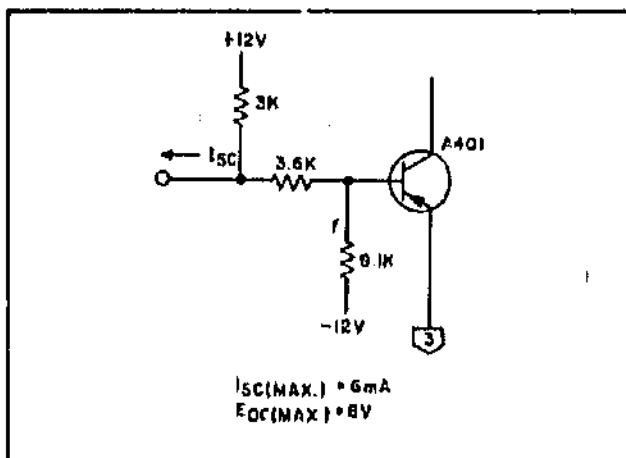


Figure A-3. Cable Continuity Interlock Receiver Circuit

A-31 INPUT GROUND

A-32 Input data common must be connected to common in the DVS 6130C (pins 26 through 31) shown on Figure A-1. These pins are internally shorted together within the connector jack.

A-33 OUTPUT DRIVER CIRCUITS

A-34 Figure A-4 shows the output driver circuit that is used for each digital output signal; namely,

flag, overload status, and latch status. "Open collector" type drivers are used. Each transistor can withstand up to 20V across it in the cutoff condition and can conduct up to 20mA of current when saturated. The output is "high" (more positive) when the driver is cutoff or "low" (less positive) when the driver is conducting. Output impedances under these conditions are shown on the drawing.

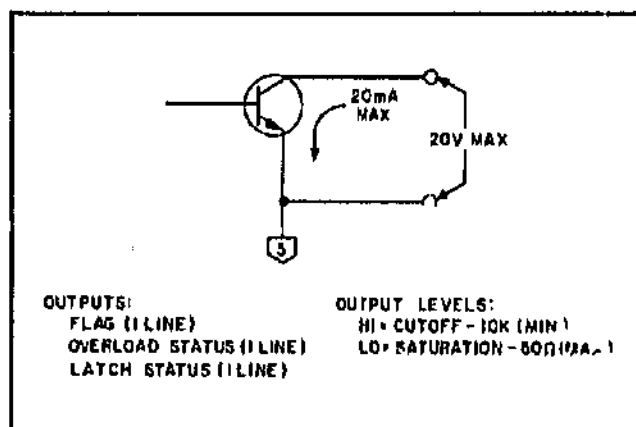
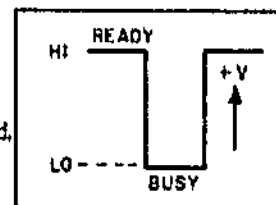


Figure A-4. Driver Circuit

A-35 FLAG OUTPUT

A-36 Flag output signals are issued under two separate conditions. As described in Section III, the flag output switches from ready to busy during (1) processing of the voltage magnitude data bits, and (2) changing of the voltage range. The time that the flag remains in the busy state is different for each condition (see Figures 3-4, 3-5, and 3-7). For this Option, A6CR14 and A6CR15 are deleted. This means that when an overload condition exists, the Flag, as mentioned in Paragraph 3-30 and shown on Figure 3-7, is not generated. Note, however, that the Flag signal is still generated when a range change occurs.

A-37 Flag Polarity. For this option, transistor A1Q6 and resistor A1R15 are not supplied, jumpers W14 and W15 are installed, and, therefore, the flag polarity is as follows:

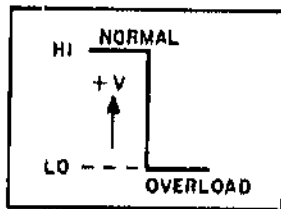


A-38 OVERLOAD STATUS

A-39 The overload status line switches to the overload state whenever the output current exceeds the programmed current latch value (see Figure 3-7). The signal remains in the overload state until the output current is decreased (unit goes into current latch or overload is removed).

A-40 Overload Status Polarity. For this option,

transistor A6A5Q4 and resistor A6A6R7 are not supplied and jumper A6A6W2 is installed. Therefore, transistor A6A6Q3 serves as the output driver and the output signal polarity is as follows:

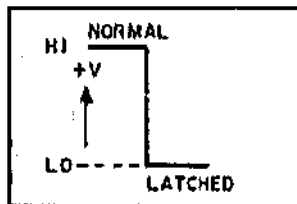


A-41 LATCH STATUS

A-42 The latch status line switches to the latched state if the unit goes from the overload to the latch state (Figure 3-7). In the latch condition, the output current is limited to less than 10mA. The latch status signal will revert from the overload latch state to the normal state approximately 10μsec after the next gate input is received, providing that the overload condition no longer exists. Therefore, to program the DVS out of the current latch condition and back to normal operation, the overload must be removed or the current latch setting increased; and then a new gate signal must be issued.

A-43 The latch status signal does not switch to the latched state if the C_T terminals on the rear of the DVS are shorted (refer to Paragraph 3-33).

A-44 Latch Status Polarity. For this Option, transistor A6A5Q4 serves as the output driver. The signal polarity is as follows:



A-45 POCKET-PROGRAMMER 14533B USAGE

A-46 To program the DVS using the HP Pocket Programmer 14533B, refer to the following chart for appropriate switch positions for this particular option. Note that these switch positions may not apply to the "A" version of the Pocket Programmer 14533A.

SWITCH	POSITION		
Voltage Magnitude (0.5-8192) Binary 1 Binary 0	down up		
Output Sign Positive Output Negative Output	up down		
Current Latch (L22, L23, L24)	L22	L23	L24
20mA	up	up	up
50mA	down	up	up
70mA	up	down	up
100mA	down	down	up
200mA	up	up	down
500mA	down	up	down
700mA	up	down	down
1000mA	down	down	down
MP/DCPS	down		
Input Level Reference	down		

A-47 OPTION J20 PARTS LIST

A-48 The following is a tabular listing of the special parts associated with this Option.

Option 120 Replaceable Parts

REF. DESIG.	DESCRIPTION	TQ	MFR. PART NO.	MTR. CODE	HP PART NO.	RS
A1	Input Board	1		28480	5060-7986	1
A1A1R1	fxd, comp 6.2K Ω \pm 5%, 1/4W	1	CB-6225	01121	0683-6225	1
A1A1R2	fxd, comp 12K Ω \pm 5%, 1/4W	1	CB-1235	01121	0683-1235	1
A1A1R3	fxd, comp 62K Ω \pm 5%, 1/4W	1	CB-6235	01121	0683-6235	1
A1A2 through A1A17	Same as A1A1	16				
A1Q1, Q6, Q7	Omit Q1, Q6, Q7					
A1R1	fxd, comp 1K Ω \pm 5%, 1/4W	1	CB-1025	01121	0683-1025	1
A1R2	fxd, comp 2K Ω \pm 5%, 1/4W	1	CB-2025	01121	0683-2025	1
A1R3	fxd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
A1R4, 15, 17, 18, and 19 A1VR5	Omit R4, 15, 17, 18, and 19 Omit VR5					
A2	Logic Board	1		28480	5060-7989	
A2Z1-24	Quad, D-Type Latch, IC	4	SN7475	01295	1820-0301	4
A2Z9-212	Omit Z9-Z12 (SN7475's installed in Z1-Z4 locations)					
A6	Control Board	1		28480	5060-7993	
A6A1R1	fxd, comp 6.2K Ω \pm 5%, 1/4W	1	CB-6225	01121	0683-6225	1
A6A1R2	fxd, comp 12K Ω \pm 5%, 1/4W	1	CB-1235	01121	0683-1235	1
A6A1R3	fxd, comp 62K Ω \pm 5%, 1/4W	1	CB-6235	01121	0683-6235	1
A6A2 through A6A4	Same as A6A1	3				
A6A5R8	Omit A6A5R8					
A6A5VR1	Omit A6A5VR1					
A6A6Q4	Omit A6A6Q4					
A6A6R7, R8	Omit A6A6R7, R8					
A6A6VR1	Omit A6A6VR1					
A6CR14, 15	Omit CR14, CR15					

APPENDIX B OPTION 062-Binary Interface For Open Collector Circuits

B-1 INTRODUCTION

B-2 This Appendix describes the input and output data parameters for interfacing with a digital Binary source employing "open collector" driver transistors. Only interfacing requirements are discussed in this Appendix. Information of a more general nature is given in Section III of this manual. Hence, for a complete conception of the operating and interfacing requirements, both this Appendix and Section III must be consulted.

B-3 The data parameters described in the following paragraphs include the following:

- (1) Binary voltage magnitude data.
- (2) Input/Output signal polarity.
- (3) Logic coding - significance of high and

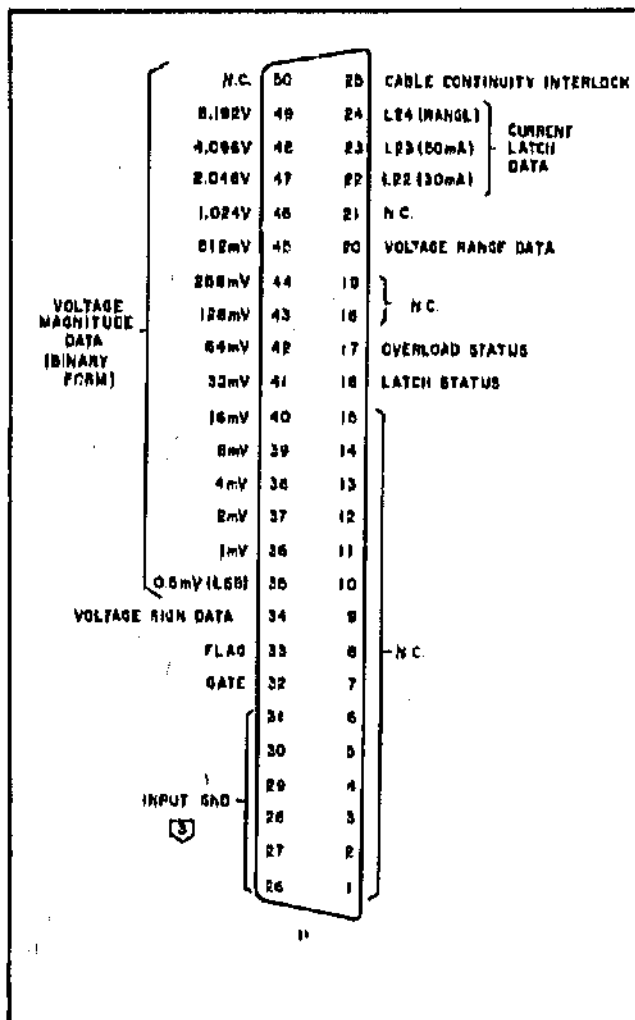


Figure B-1. Input/Output Data Connector

low input/output signal states.

(4) Logic levels - voltage limits for high and low digital signal states.

B-4 The digital input/output stages on three of the DVS plug-in boards (A1, A2, and A6) have been especially designed to obtain the desired data parameters under worse case conditions. A list of these special parts is included at the rear of this Appendix.

B-5 DATA CONNECTOR

B-6 Input/Output data is connected to the digital programming source by means of the rear connector (Figure B-1). The parameters associated with each of the signals of Figure B-1 are discussed in the following paragraphs.

B-7 INPUT/OUTPUT SIGNAL POLARITY

B-8 All input/output signals are of positive polarity; i.e. are above 0 volts. Therefore, the input/output stages on A1 (Input board) and A6 (control board) use NPN transistors as shown in the schematic (Figure 7-2) provided in the manual.

B-9 RECEIVER CIRCUITS AND LOGIC LEVELS

B-10 Figure B-2 shows an input circuit that applies to all of the digital inputs listed on the

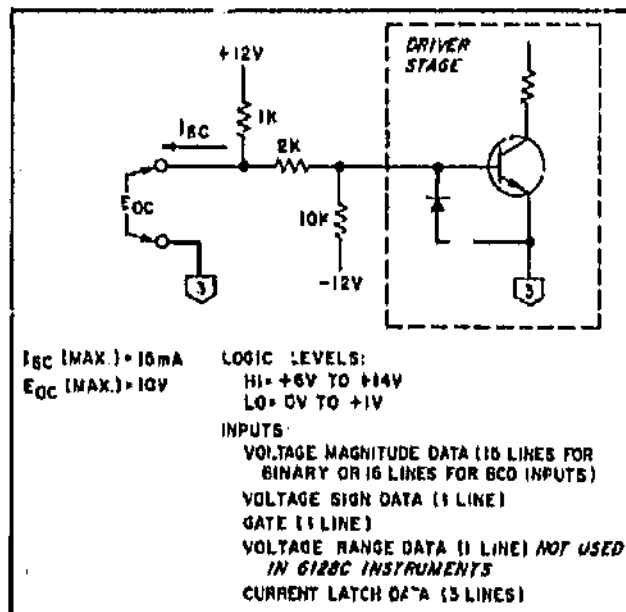


Figure B-2. Receiver Circuit

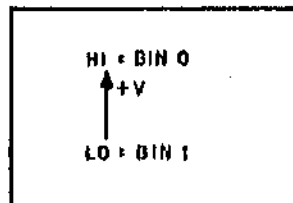
drawing. The three resistors of the input voltage divider are selected so that a high input level will turn-on the succeeding driver stage and a low input level will cut the stage off. As shown on Figure B-2, the logic levels for all of the listed inputs are high = +6V to +14V and low = 0V to +1V.

B-11 The maximum current that can be drawn from the input circuit when the input terminals are short circuited is 15mA (designated I_{SC}-MAX on Figure B-2). The maximum voltage that can appear across the input terminals under open circuit conditions (designated E_{OC}-MAX) is 10V.

B-12 VOLTAGE MAGNITUDE INPUT DATA

B-13 Logic Type. The input data to this unit is received in a binary code. Positive numbers are received from the computer in straight binary form while negative numbers are received in 2's complement form, which will be discussed later.

B-14 Logic Coding.



B-15 Logic Inversion. The A2 storage inverters for the voltage magnitude bits are included for the logic coding (HI = BIN 0) associated with this option as shown in Figure 7-2, Sheet 1 (the storage IC's are installed in the Z1-Z4 positions).

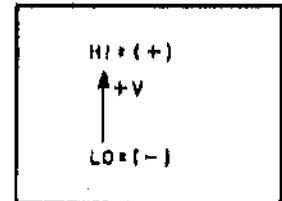
B-16 The voltage magnitude input data is made up of 15 binary bits designated according to their position analog equivalent value in millivolts (8192, 4096, 2048, ... 0.5). This input data is used in conjunction with the voltage sign and voltage range data to control the output voltage of the DVS. The voltage magnitude data is programmed into the unit in straight binary form when the voltage sign is positive, and in 2's complement form when the voltage sign is negative. 2's complement form consists of complement form consists of complementing the equivalent positive binary number (all ones become zeros, all zeros become ones) and adding a binary 1 to the least significant bit. The voltage sign data determines the polarity of the output voltage while the voltage range program select multiplies the voltage program data by X1 or X10; hence, the output of the DVS may be programmed between -16,384 and +16,385 volts (X1 or X10). Notice that for 6130C instruments, numbers beyond 5.9 in the X10 range are not valid because the maximum rated output voltage for this unit is 50V. As explained in Section III, the output voltage of the 6130C is limited to approximately

55 volts maximum.

B-17 VOLTAGE SIGN

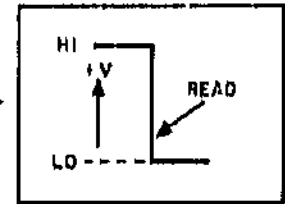
B-18 The voltage sign data bit determines the polarity of the output. Jumper connection A2W1-P (Figure 7-2, sheet 1) is included for the coding shown below.

B-19 Logic Coding.



B-20 GATE

B-21 Coding. As shown, a high to low transition of the gate input permits storage of the voltage magnitude voltage sign, current latch, and voltage range input data in the DVS storage registers. Notice that the STORAGE switch on the A2 P.C. Board (see Figure 3-2) must be in the STORE position to utilize this storage capability.



B-22 VOLTAGE RANGE

B-23 Coding. HI = X10 (High voltage range)
LO = X1 (Low voltage range)

B-24 The following chart shows the coding required for voltage range.

INPUT CODE	VOLTAGE RANGE
LO	X1
HI	X10

B-25 CURRENT LATCH

B-26 Coding. The current latch data forms a 3-bit binary code. The input codes for each current latch value are shown in the chart on page 3-5. Notice that the three current latch bits provide a maximum of eight possible combinations.

B-27 C_T Terminals. As described in Section III, the current latch delay period is determined by the condition of the C_T terminals at the rear of the unit. Notice that if the C_T terminals are shorted,

the DVS will not current latch even if the output current exceeds the programmed current latch value.

B-28 CABLE CONTINUITY INTERLOCK

B-29 Before output voltage can be obtained from the DVS, a connection must be made between input common (3) and the cable continuity interlock pin 25 of the input/output connector. If this connection is not made the output terminals of the DVS will be shorted by an internal relay. This protects the load device against excessive voltages in case the input cable is disconnected.

B-30 Cable Continuity Interlock Receiver Circuit. Figure B-3 shows the cable continuity interlock circuit. The three input voltage divider resistors are selected so that a (3) common input will cause A1Q1 to saturate and an open (no input connection) will cause A1Q1 to cut off. The maximum current (I_{SC-MAX}) that could be drawn from the input circuit when the input terminals are short circuited is 6mA. The maximum voltage (E_{OC-MAX}) that appears across the input terminals under open circuit conditions is 9V.

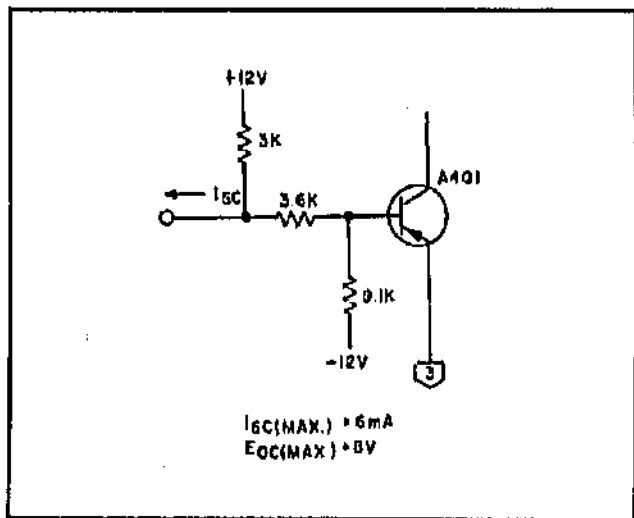


Figure B-3. Cable Continuity Interlock Receiver Circuit

B-31 INPUT GROUND

B-32 Input data common must be connected to (3) common of the DVS (pins 26 through 31 shown on Figure B-1). These pins are internally shorted together within the connector jack.

B-33 OUTPUT DRIVER CIRCUITS

B-34 Figure B-4 shows the output driver circuit that is used for each digital output signal; namely, flag, overload status, and latch status. "Open collector" type drivers are used. Each transistor can withstand up to 20V across it in the cutoff condition and can conduct up to 20mA of current when saturated. The output is "high" (more positive) when the driver is cut off or "low" (less positive) when the driver is conducting. Output impedances under these conditions are shown on the drawing.

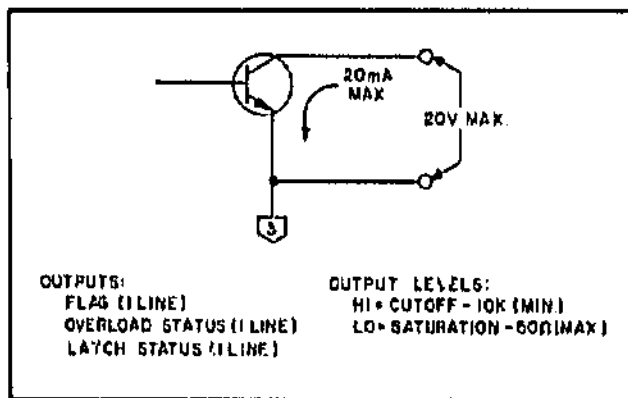
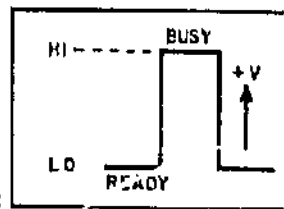


Figure B-4. Driver Circuit

B-35 FLAG OUTPUT

B-36 Flag output signals are issued under three separate conditions. As described in Section III, the flag output switches from ready to busy during: (1) processing of the voltage magnitude data bits, (2) changing of the voltage range, and (3) current overload periods. The time that the flag remains in the busy state is different for each of the three conditions (see Figures 3-4, 3-5, and 3-7).

B-37 Flag Polarity. For this option, transistor A1Q6 and resistors A1R15 and A1R17 are included, jumper W14 is not installed, and, therefore, the flag polarity is as follows:



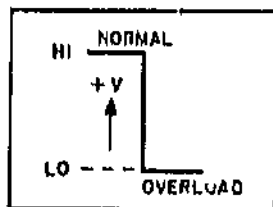
B-38 OVERLOAD STATUS

B-39 The overload status line switches to the

overload state whenever the output current exceeds the programmed current latch value (see Figure 3-7). The signal remains in the overload state until the output current is decreased (unit goes into current latch or overload is removed).

B-40 Overload Status Polarity.

For this Option, transistor A6A6Q4 and resistor A6A6R7 are not supplied and jumper A6A6W2 is installed. Therefore, transistor A6A6Q3 serves as the output driver and the output signal is as follows:



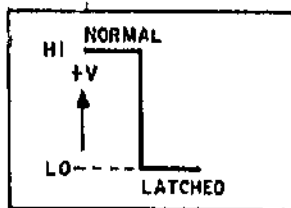
B-41 LATCH STATUS

B-42 The latch status line switches to the latched state if the unit goes from the overload to the latch state (Figure 3-7). In the latch condition, the output current is limited to less than 10mA. The latch status signal will revert from the overload latch state to the normal state approximately 10µsec after the next gate input is received, providing that the overload condition no longer exists. Therefore, to program the DVS out of the current latch condition and back to normal operation, the overload must be removed or the current latch setting increased; and then a new gate signal must be issued.

B-43 The latch status signal does not switch to the latch state if the C_T terminals on the rear of the DVS are shorted (refer to Paragraph 3-33).

B-44 Latch Status Polarity.

For this Option, transistor A6A5Q4 serves as the output driver. The signal polarity is as follows:



B-45 POCKET PROGRAMMER 14533B USAGE

B-46 To program the DVS using the HP Pocket Programmer 14533B, refer to the following chart for appropriate switch positions for this particular option. Note that these switch positions may not apply to the "A" version of the Pocket Programmer 14533B.

SWITCH	POSITION		
Voltage Magnitude (0, 5-8192) Binary 1 Binary 0	down up		
Output Sign Positive Output Negative Output	up down		
Current Latch (L22, L23, L24)	L22	L23	L24
20mA	up	up	up
50mA	down	up	up
70mA	up	down	up
100mA	down	down	up
200mA	up	up	down
500mA	down	up	down
700mA	up	down	down
1000mA	down	down	down
MP/DCPS	down		
Input Level Reference	down		

B-47 OPTION 062 PARTS LIST

B-48 The following is a tabular listing of the special parts associated with this Option.

Option 062 Replaceable Parts

REF. DESIG.	DESCRIPTION	TQ	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A1	Input Board	1		28480	5060-7987	
A1A1R1	fxd, comp 1K Ω \pm 5%, 1/4W	1	CB-1025	01121	0683-1025	1
A1A1R2	fxd, comp 2K Ω \pm 5%, 1/4W	1	CB-2025	01121	0683-2025	1
A1A1R3	fxd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
A1A2 through A1A17	Same as A1A1	16				
A1Q1	Omit Q1					
A1Q6	SS NPN SI,	1		28480	1854-0071	1
A1Q7	Omit Q7					
A1R1	fxd, comp 1K Ω \pm 5%, 1/4W	1	CB-1025	01121	0683-1025	1
A1R2	fxd, comp 2K Ω \pm 5%, 1/4W	1	CB-2025	01121	0683-2025	1
A1R3	fxd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
A1R4	Omit R4					
A1R15	fxd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
A1R17	fxd, comp 2.7K Ω \pm 5%, 1/4W	1	CB-0275	01121	0683-0275	1
A1R18, R19	Omit R18 and R19					
A1VR5	Omit VR5					
A2 Z1-Z4 Z9-Z12	Logic Board Quad, D-Type Latch, IC Omit Z9-Z12 (SN7475 installed in Z1-Z4 locations)	4	SN7475	28480 01295	5060-7989 1020-0201	4
A6	Control Board	1		28480	5060-7994	
A6A1R1	fxd, comp 1K Ω \pm 5%, 1/4W	1	CB-1025	01121	0683-1025	1
A6A1R2	fxd, comp 2K Ω \pm 5%, 1/4W	1	CB-2025	01121	0683-2025	1
A6A1R3	fxd, comp 10K Ω \pm 5%, 1/4W	1	CB-1035	01121	0683-1035	1
A6A2 through A6A4	Same as A6A1	3				
A6A5R8	Omit A6A5R8					
A6A5VR1	Omit A6A5VR1					
A6A6Q4	Omit A6A6Q4					
A6A6R7, R8	Omit A6A6R7, R8					
A6A6VR1	Omit A6A6VR1					
AGCR14, 15	Diode, SI, 200mA 75V	2		28480	1901-0050	

APPENDIX C

OPTION 064-Binary Interface For Microcircuit Logic Levels

C-1 INTRODUCTION

C-2 This Appendix describes the input and output data parameters for interfacing with a digital binary source employing microcircuits of the TTL or DTL family. Only interfacing requirements are discussed in this Appendix. Information of a more general nature is given in Section III of this manual. Hence, for a complete conception of the operating and interfacing requirements, both this Appendix and Section III must be consulted.

C-3 The data parameters described in the following paragraphs include the following:

- (1) Binary voltage magnitude data,
- (2) Input/output signal polarity,
- (3) Logic coding - significance of high and low input/output signal states.
- (4) Logic levels - voltage limits for high and low digital signal states.

C-4 The digital input/output stages on three of the DVS plug-in boards (A1, A2 and A6) have been especially designed to obtain the desired data parameters under worst case conditions. A list of these parts is included at the rear of this Appendix.

C-5 DATA CONNECTOR

C-6 Input/output data is connected to the digital programming source by means of the rear connector (Figure C-1). The parameters associated with each of the signals of Figure C-1 are discussed in the following paragraphs.

C-7 INPUT/OUTPUT SIGNAL POLARITY

C-8 All input/output signal are of positive polarity; i.e. are above 0 volts. Therefore, the input/output stages on A1 (input board) and A6 (control board) use NPN transistors as shown in the schematic (Figure 7-2) provided in the manual.

C-9 RECEIVER CIRCUITS AND LOGIC LEVELS

C-10 Figure C-2 shows an input circuit that applies to all of the digital inputs listed on the drawing. The three resistors of the input voltage divider are selected so that a high input level will turn-on the succeeding driver stage and a low in-

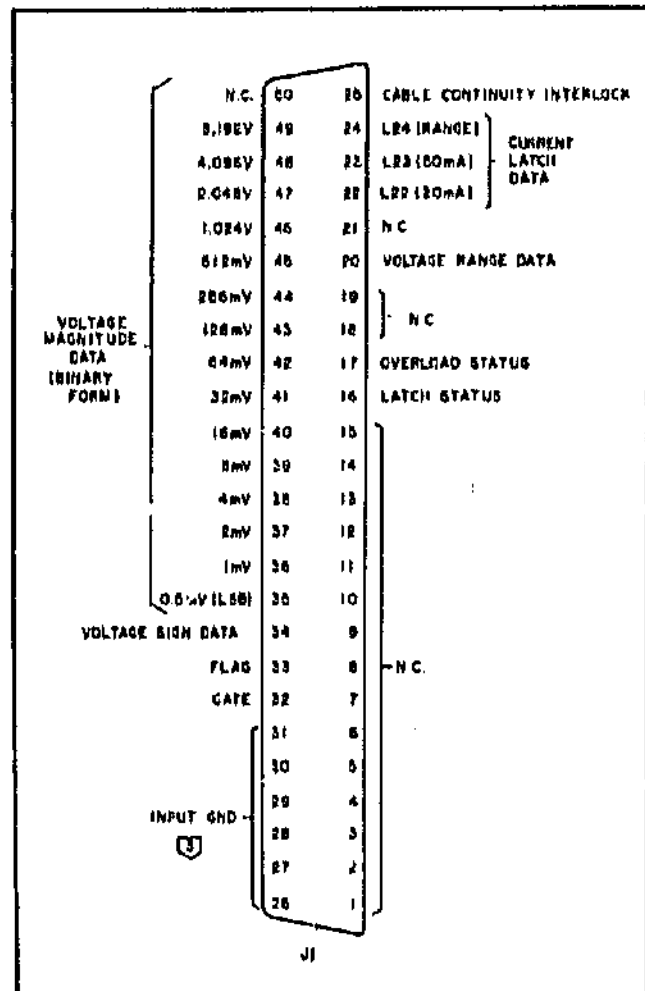


Figure C-1. Input/Output Data Connector

put level will cut the stage off. As shown on Figure C-2, the logic levels for all of the listed inputs are high = +1.9V to +16.5V and low = -4.4V to +1.3V.

C-11 The maximum current that can be drawn from the input circuit when the input terminals are short circuited is 1mA (designated I_{SC-MAX} on Figure C-2). The maximum voltage can appear across the input terminals under open circuit conditions (designated E_{OC-MAX}) is 3.6V.

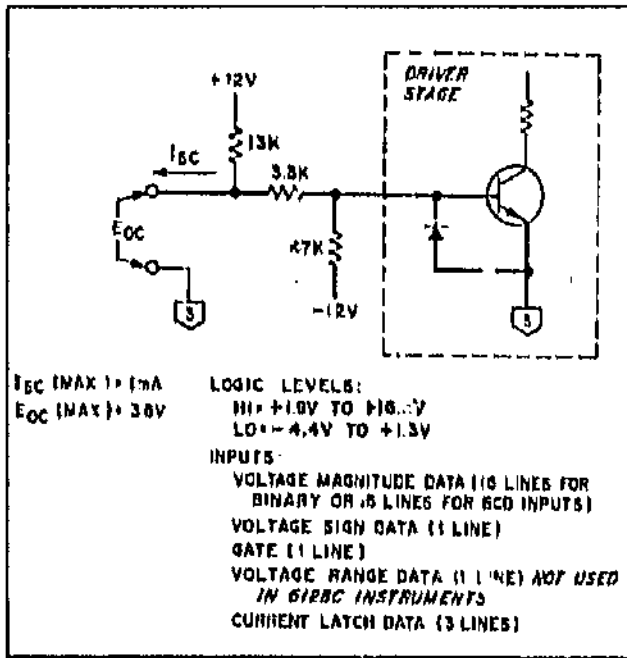
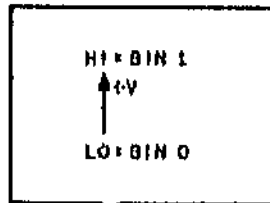


Figure C-2, Receiver Circuit

C-12 VOLTAGE MAGNITUDE INPUT DATA

C-13 Logic Type. The input data to the unit is received in a binary code. Positive numbers are received from the computer in straight binary form while negative numbers are received in 2's complement form, which will be discussed later.

C-14 Logic Coding.



C-15 Logic Inversion. The A2 storage inverters for the voltage magnitude bits are excluded for the logic coding (HI = BIN 1) associated with this option as shown in Figure 7-2, Sheet 1 (the storage IC's are installed in the 29-312 positions).

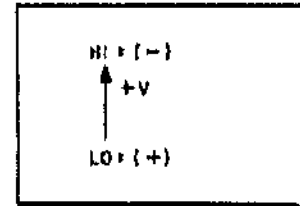
C-16 The voltage magnitude input data is made up of 16 binary bits designated according to their positive analog equivalent value in millivolts (8192, 4096, 2048, ..., 0.5). This input data is used in conjunction with the voltage sign and voltage range data to control the output voltage of the DVS. The voltage magnitude data is programmed into the unit in straight binary form when the voltage sign program is positive, and in negative 2's complement form when the voltage sign program is negative. Negative 2's complement form consists of complementing the equivalent positive binary number (all ones become zeros, all zeros become ones)

and adding a binary 1 to the least significant bit. The voltage sign data determines the polarity of the output voltage while the voltage range program select multiplies the voltage program data by X1 or X10. Hence, the output of the DVS may be programmed between -16,384 and +16,385 volts (X1 or X10). Notice that for 6130C instruments, numbers beyond 5.0 in the X10 range are not valid because the maximum rated output voltage for this unit is 50V. As explained in Section III, the output voltage of the 6130C is limited to approximately 55 volts maximum.

C-17 VOLTAGE SIGN

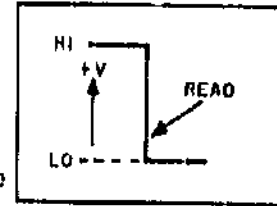
C-18 The voltage sign data bit determines the polarity of the output. Jumper connection A2W1-A (Figure 7-2, Sheet 1) is included for the coding shown below.

C-19 Logic Coding.



C-20 GATE

C-21 Coding. As shown, a high to low transition of the gate input permits storage of the voltage magnitude, voltage sign, current latch, and voltage range input data in the DVS storage registers. Notice that the STORAGE switch on the A2 P.C. Board (see Figure 3-2) must be in the STORE position to utilize this storage capability.



C-22 VOLTAGE RANGE

C-23 Coding. HI = X10 (High voltage range),
 LO = X1 (Low voltage range).

C-24 The following chart shows the coding required for voltage range.

INPUT CODE		VOLTAGE RANGE
Voltage Range Bit		
LO		X1
HI		X10

C-26 CURRENT LATCH

C-26 Coding. The current latch data forms a 3-bit binary code. The input codes for each current latch value are shown in the chart on page 3-5. Notice that the three current latch bits provide a maximum of eight possible combinations.

C-27 C_T Terminals. As described in Section III, the current latch delay period is determined by the condition of the C_T terminals at the rear of the unit. Notice that if the C_T terminals are shorted, the DVS will not current latch even if the output current exceeds the programmed current latch value.

C-28 CABLE CONTINUITY INTERLOCK

C-29 Before output voltage can be obtained from the DVS, a connection must be made between input common (3) and the cable continuity interlock pin 25 of the input/output connector. If this connection is not made, the output terminals of the DVS will be shorted by an internal relay. This protects the load device against excessive voltages in case the input cable is disconnected.

C-30 Cable Continuity Interlock Receiver Circuit. Figure C-3 shows the cable continuity interlock

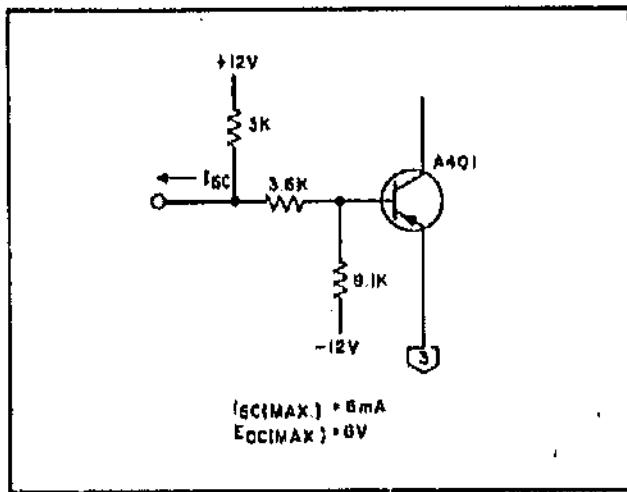


Figure C-3, Cable Continuity Interlock Receiver Circuit

receiver circuit. The three input voltage divider resistors are selected so that a (3) common input will cause A401 to saturate and an open (no input connection) will cause A401 to cut off. The maximum current (I_{SC-MAX}) that could be drawn from the input circuit when the input terminals are short circuited is 6mA. The maximum voltage (E_{OC-MAX}) that appears across the input terminals under open circuit conditions is 8V.

C-31 INPUT GROUND

C-32 Input data must be connected to (3) common of the DVS (pins 26 through 31) shown on Figure C-1. These pins are internally shorted together within the connector jack.

C-33 OUTPUT DRIVER CIRCUITS

C-34 Figure C-4 shows the output driver circuit that is used for each output signal; namely, flag, overload status, and latch status. Transistors A1Q5, A6A5A4, and A5A6Q3 serve as the output driver transistors. A zener diode in each output circuit prevents the output voltage from exceeding +4.4V (max) when the output driver is cut off (high output condition).

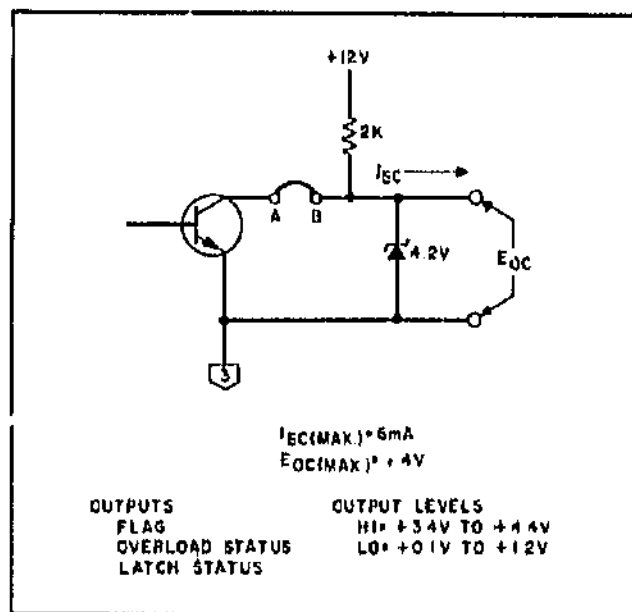


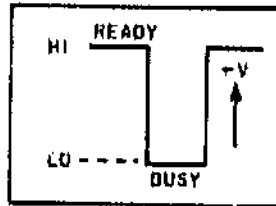
Figure C-4, Driver Circuit

C-35 With the output terminals shorted, the maximum current (I_{SC-MAX}) that can be drawn from the driver circuit is 6mA. With the output terminals open, the maximum voltage (as determined by the zener diode) is +4.4V.

C-36 FLAG OUTPUT

C-37 Flag output signals are issued under three separate conditions. As described in Section III, the flag output switches from ready to busy during: (1) processing of the voltage magnitude data bits, (2) changing of the voltage range, and (3) current overload periods. The time that the flag remains in the busy state is different for each of the three conditions (see Figures 3-4, 3-5, and 3-7).

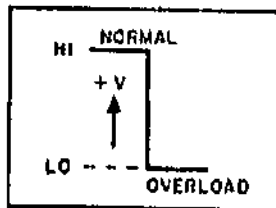
C-38 Flag Polarity. For this option, transistor A1Q6 and resistor A1R15 are not supplied, jumpers W14 and W15 are installed, and resistor R18 (the load for A1Q5) and zener diode A1VR5 are included. The flag polarity, therefore is as follows:



C-39 OVRLOAD STATUS

C-40 The overload status line switches to the overload state whenever the output current exceeds the programmed current latch value (see Figure 3-7). The signal remains in the overload state until the output current is decreased (unit goes into current latch or overload is removed).

C-41 Overload Status Polarity. For this option, transistor A6A6Q4 and resistor A6A6R7 is not supplied and jumper A6A6Q3 serves as the output transistor with resistor A6A6R8 (load for A6A6Q3) and zener diode A6A6VR1 included. The output signal polarity is as follows:



C-42 LATCH STATUS

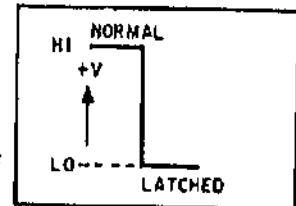
C-43 The latch status line switches to the latch state if the unit goes from the overload to the latch state (Figure 3-7). In the latch condition, the output current is limited to less than 10mA. The latch status signal will revert from the overload latch state to the normal state approximately 10μsec after the next gate input is received, providing that the next gate input is received, providing that the overload condition no longer exists. Therefore, to program the DVS out of the current latch condition and back to normal operation, the overload must be removed or the current latch setting increased; and then a new gate signal must be issued.

C-44 The latch status signal does not switch to the latched state if the CT terminals on the rear of the DVS are shorted (refer to Paragraph 3-33).

SWITCH	POSITION
Voltage Magnitude (0.5-8192) Binary 1 Binary 0	up down
Output Voltage Positive Output Negative Output	down up
Current Latch (L22, L23, L24)	L22 L23 L24
20mA	up up up
50mA	down up up
70mA	up down up
100mA	down down up
200mA	up up down
500mA	down up down
700mA	up down down
1000mA	down down down
Mp/DUPS	down
Input Level Reference	down

C-45 Latch Status Polarity.

For this Option, Transistor A6A5Q4 serves as the output driver with resistor A6A5R8 (installed for its load). Zener diode A6A5VR1 is included. The output signal polarity is as follows:



C-46 POCKET PROGRAMMER 14533B USAGE

C-47 To program the DVS using the IIP Pocket Programmer 14533B, refer to the preceding chart for appropriate switch positions for this particular option. Note that these switch positions may not apply to the "A" version of the Pocket Programmer 14533A.

C-48 OPTION 064 PARTS LIST

C-49 The following is a tabular listing of the special parts associated with this Option.

Option 064 Replaceable Parts

REF. DESIG.	DESCRIPTION	QTY	MFR. PART NO.	MFR. CODE	HP PART NO.	RS
A1	Input Board	1		28480	5060-7988	
A1A1R1	fxd, comp 13K Ω \pm 5%, 1/4W	1	CB-1335	01121	0683-1335	1
A1A1R2	fxd, comp 3.3K Ω \pm 5%, 1/4W	1	CB-3325	01121	0683-3325	1
A1A1R3	fxd, comp 47K Ω \pm 5%, 1/4W	1	CB-4735	01121	0683-4735	1
A1A2 through A1A17	Same as A1A1	16				
A1Q1, Q6, Q7	Omit Q1, Q6, Q7					
A1R1	fxd, comp 13K Ω \pm 5%, 1/4W	1	CB-1335	01121	0683-1335	1
A1R2	fxd, comp 3.3K Ω \pm 5%, 1/4W	1	CB-3325	01121	0683-3325	1
A1R3	fxd, comp 47K Ω \pm 5%, 1/4W	1	CB-4735	01121	0683-4735	1
A1R4, R15, R17	Omit R4, R15, R17					
A1R18	fxd, comp 2K Ω \pm 5%, 1/4W	1	CB-2025	01121	0683-2025	1
A1R19	Omit R19					
A1VR5	Diode, zener 4.22V \pm 5%	1		28480	1902-3070	1
A2	Logic Board	1		28480	5060-7990	
A2Z1-24	Omit Z1-24 (SN7475's installed in Z9-Z12 locat ons)					
A2Z9-212	Quad. D-Type latch, IC	4	SN7475	01295	1820-0301	4
A6	Control Board	1		28480	5060-7995	
A6A1R1	fxd, comp 13K Ω \pm 5%, 1/4W	1	CB-1335	01121	0683-1335	1
A6A1R2	fxd, comp 3.3K Ω \pm 5%, 1/4W	1	CB-3325	01121	0683-3325	1
A6A1R3	fxd, comp 47K Ω \pm 5%, 1/4W	1	CB-4735	01121	0683-4735	1
A6A2 through A6A4	Same as A6A1	3				
A6A5R8	fxd, comp 2K Ω \pm 5% 1/2W	1	EB-2025	01121	0686-2025	1
A6A5VR1	Diode, zener 4.22V \pm 5%	1		28480	1902-3070	1
A6A6Q4	Omit A6A6Q4					
A6A6R7	Omit A6A6R7					
A6A6R8	fxd, comp 2K Ω \pm 5%, 1/2W	1	EB-2025	01121	0686-2025	1
A6A6VR1	Diode, zener 4.22V \pm 5%	1		28480	1902-3070	1
A6CR14, CR15	Diode, Si, 200mA 75V	2		28480	1901-0050	2