

Errata

Title & Document Type: 5355A Automatic Frequency Converter and 5356A/B/C Frequency Converter Heads Operating and Service Manual

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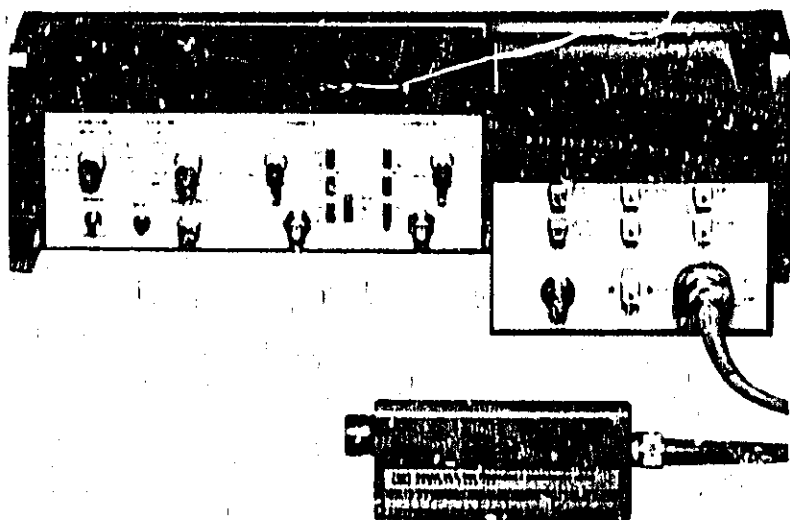
Agilent Technologies

OPERATING AND SERVICE MANUAL

5355A AUTOMATIC FREQUENCY CONVERTER

AND

5356A/B/C FREQUENCY CONVERTER HEADS



General Information
Installation
Operating and Programming
Performance Tests
Adjustments
Replaceable Parts
Manual Changes
Service



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OPERATING AND SERVICE MANUAL

5355A Automatic Frequency Converter and 5356A/B/C Frequency Converter Heads

SERIAL PREFIX: 2016A

This manual applies to 5355A Serial Prefix 2016A, and 5356A/B/C Serial Prefix 1952A unless accompanied by a Manual Change Sheet indicating otherwise.

OLDER INSTRUMENTS

For serial prefixes below 2016A, refer to Section VII for manual backdating.

First Edition — December 1980

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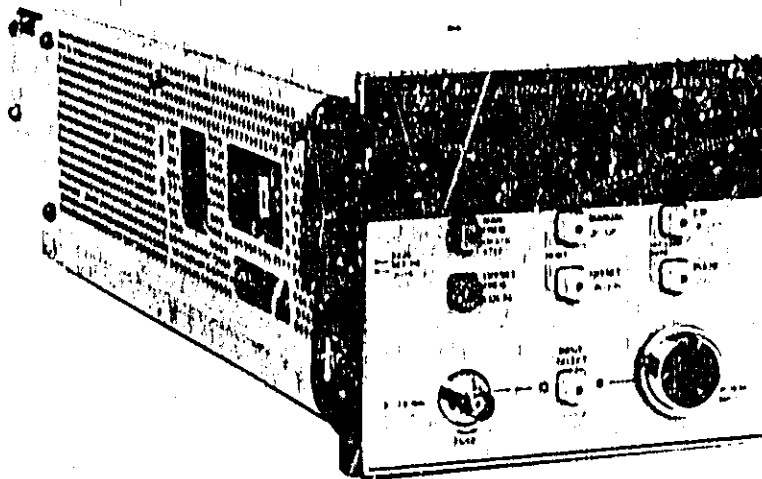
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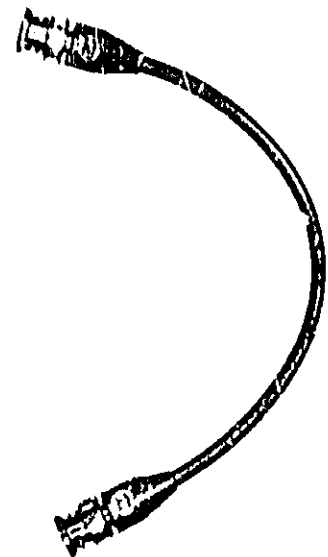
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EQUIPMENT SUPPLIED

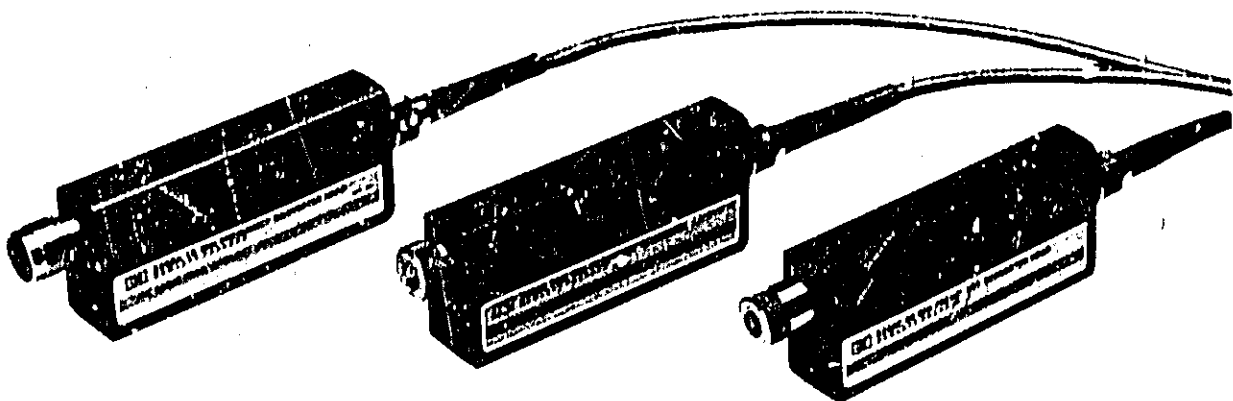


**5355A
AUTOMATIC FREQUENCY CONVERTER**



**REAR PANEL CABLE
10502A**

**ACCESSORIES
(FREQUENCY CONVERTER HEADS)**



**5356A
(1.5 to 18 GHz)**

**5356B
(1.5 to 26.5 GHz)**

**5356C
(1.5 to 40 GHz)**

Figure 1-1. HP 5355A Automatic Frequency Converter and Accessories

SECTION I GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This manual provides information pertaining to the installation, operation, testing, adjustment, and maintenance of the HP Model 5355A Automatic Frequency Converter and accessories.

1-3. Figure 1-1 shows the HP 5355A and accessories. The 5355A is a plug-in unit for the HP 5345A Electronic Counter. The 5356A, 5356B, or 5356C Frequency Converter Head extends the frequency range of the 5355A.

1-4. SPECIFICATIONS

1-5. Instrument specifications are listed in Table 1-1. These specifications are the performance standards or limits against which the instrument may be tested. Specifications are based on operation with the HP 5345A Electronic Counter.

1-6. INSTRUMENTS COVERED BY MANUAL

1-7. This instrument has a two-part serial number. The first four digits and the letter comprise the serial number prefix. The last five digits form the sequential suffix that is unique to each instrument. The contents of this manual apply directly to instruments having the same serial number prefix(es) as listed under SERIAL PREFIX on the title page.

1-8. An instrument manufactured after the printing of this manual may have a serial prefix that is not listed on the title page. This unlisted serial prefix indicates that the instrument is different from those documented in this manual. The manual for this instrument is supplied with a yellow Manual Changes supplement that contains change information that documents the differences.

1-9. OPERATING MANUAL

1-10. Packaged with this manual is an Operating Information Supplement. This is simply a copy of the first three sections of this manual. This supplement should be kept with the instrument for use by the operator. Additional copies of the Operating Information Supplement or the Operating and Service Manual can be ordered through your nearest Hewlett-Packard Sales and Service Office (a list of these offices is provided at the end of this manual). The part numbers are listed on the title page of this manual.

1-11. MICROFICHE

1-12. Also listed on the title page of this manual following the Operating and Service Manual and Operating Information Supplement part numbers are Microfiche part numbers for these publications. These numbers can be used to order 4- X 6-inch microfilm transparencies of these publications. The Microfiche package includes the latest Manual Changes supplement and all pertinent Service Notes.

Model 5353A
General Information

Table 1-1. Model 5353A Specifications

INPUT SPECIFICATIONS (PULSE AND CW MODE)				
	5356A	5356B*	5356C*	5355A†
Frequency Range	1.5—18 GHz	1.5—26.5 GHz (Option 001: 18—26.5 GHz)	1.5—40 GHz (Option 001: 26.5—40 GHz)	0.4—1.6 GHz
Sensitivity 0.4—1.6 GHz 1.5—12.4 GHz 12.4—18 GHz 18—26.5 GHz 26.5—34 GHz 34—40 GHz	— —20 dBm —15 dBm — — —	— —20 dBm —15 dBm —15 dBm — —	— —25 dBm —20 dBm —20 dBm —15 dBm —10 dBm	—15 dBm — — — — —
NOTE: For pulse widths <200 ns reduce sensitivity by 5 dB				
Maximum Input 0.4—1.6 GHz 1.5—12.4 GHz 12.4—18 GHz 18—26.5 GHz 26.5—40 GHz	— +5 dBm -5 dBm — —	— +5 dBm +5 dBm +5 dBm —	— +5 dBm +15 dBm +15 dBm +15 dBm	+5 dBm — — — —
Dynamic Range 0.4—1.6 GHz 1.5—12.4 GHz 12.4—18 GHz 18—26.5 GHz 26.5—34 GHz 34—40 GHz	— 25 dB 20 dB — — —	— 25 dB 20 dB 20 dB — —	— 30 dB 35 dB 35 dB 30 dB 25 dB	20 dB — — — — —
Damage Level	+25 dBm peak	+25 dBm peak	+25 dBm peak	+24 dBm peak (fuse in BNC connector)
Impedance	50Ω NOMINAL	50Ω NOMINAL	50Ω NOMINAL	50Ω NOMINAL
SWR 0.4—1.6 GHz 1.5—10 GHz 10—18 GHz 18—26.5 GHz 26.5—34 GHz 34—40 GHz	— <2:1 TYPICAL <3:1 TYPICAL — — —	— <2:1 TYPICAL <3:1 TYPICAL <3:1 TYPICAL — —	— <2:1 TYPICAL <3:1 TYPICAL <3:1 TYPICAL <3:1 TYPICAL <5:1 TYPICAL	<2.5:1 TYPICAL — — — — —
Connector	N Male	SMA male with collar (Option 001: 18—26.5 GHz waveguide (WR 42))	APC-3.5 male with collar (Option 001: 26.5—40 GHz waveguide (WR 28))	BNC

*Specifications in italics apply to both the standard 5356 Head and Option 001 of the same model.

† 0.4—1.6 GHz Input

OPERATING MODE SPECIFICATIONS (CW MODE)

	5356A/B/C INPUT AUTO MODE	5356A/B/C MAN MODE	5355A 0.4—1.6 GHz INPUT
FM Tolerance	5356A/B: 15 MHz p-p (60 MHz in special FM mode) 5356C: 60 MHz p-p Rate: dc—10 MHz	80 MHz p-p Rate: dc—10 MHz	Instantaneous frequency must not exceed 0.4—1.6 GHz range.
AM Tolerance	Any modulation index provided the minimum signal level is greater than the counter sensitivity.		
Multiple Signal Discrimination (TYPICAL)	Automatically measures largest signal provided signal is 8 dB greater than any signal within 500 MHz and 20 dB greater than any signal over 1.5—26.5 GHz range. (5356C only: 15 dB (option 001: 20 dB) greater than any signal over 26.5—40 GHz range)		
Acquisition Time (TYPICAL)	5356A/B: 400 ms (1.1s in special FM mode) 5356C: 1.4s (option 001: 1.1s)	15 ms	<1 ms (FREQ ≥ 800 MHz) 5345A GATE TIME + 45 ms (FREQ < 800 MHz)

Specifications describe the instrument's warranted performance. Supplemental characteristics are intended to provide information useful in applying the instrument by giving TYPICAL or NOMINAL, but nonwarranted performance parameters. Definition of terms is provided at the end of the specification section.

Table 1-1. Model 5355A Specifications (Continued)

OPERATING MODE SPECIFICATIONS (CW MODE) (Continued)			
	5356A/B/C INPUT AUTO MODE	5356A/B/C MAN MODE	5355A 0.4—1.6 GHz INPUT
Measurement Time	Gate Time $\leq$ 100 ms: Acquisition time + 4 X 5345A GATE TIME + 5345A Sample Rate + 125 ms. Gate Time > 100 ms: Acquisition time + 5345A GATE TIME + 5345A Sample Rate + 35 ms		Acquisition time + 5345A GATE TIME + 5345A SAMPLE RATE + 35 ms
LSD Displayed	$\frac{1 \text{ Hz}}{5345A \text{ GATE TIME}}$		
Resolution	$\pm 2 \times \text{LSD} \pm 1 \times 10^{-10} \text{ rms} \times \text{FREQ}$		$\pm 5 \times \text{LSD}$
Accuracy†	Resolution $\pm$ (time base error X FREQ)		Resolution $\pm$ (time base error X FREQ)
PULSE MODE			
	5356A/B/C INPUT AUTO MODE	5356A/B/C INPUT MAN MODE	5355A* 0.4—1.6 GHz INPUT
FM Tolerance (TYPICAL)	50 MHz p-p chirp	80 MHz p-p chirp	Instantaneous frequency must not exceed 0.4—1.6 GHz range
Acquisition Time (TYPICAL)	5356A/B/C MAN MODE: 0 5356A/B AUTO MODE: 100 $\mu\text{s}/(\text{EXT. GATE WIDTH} \times \text{PRF}) + 650 \text{ ms}$ for EXT GATE $\leq 100 \mu\text{s}$. (2/PRF) + 650 ms for EXT GATE > 100 μs . 5356C AUTO MODE: 100 $\mu\text{s}/(\text{EXT GATE WIDTH} \times \text{PRF}) + 1.55\text{s}$ (Option 001: 1.25s) + 8 (Option 001: 7)/PRF for EXT GATE $\leq 100 \mu\text{s}$. 10 (Option 001: 9)/PRF + 1.55s (Option 001: 1.25s) for EXT GATE > 100 μs .		0 (FREQ $\geq 800 \text{ MHz}$) $\frac{5345A \text{ GATE TIME}}{\text{EXT GATE WIDTH} \times \text{PRF}}$ + 45 ms (FREQ < 800 MHz)
Calibration Time	$\frac{5345A \text{ GATE TIME}}{\text{EXT GATE WIDTH} \times \text{PRF}} + 75 \text{ ms}$ Performed during 10 consecutive measurements when PULSE Mode is selected, after any front panel change, or when the EXTERNAL GATE width changes by more than 12%. Only calibrates if External Gate is $\leq 100 \mu\text{s}$.		
Measurement Time (TYPICAL)	Acquisition Time + Calibration Time + 5345A SAMPLE RATE + 5345A GATE TIME or 100 μs (whichever is greater) $\frac{\text{EXT GATE WIDTH} \times \text{PRF}}{+ 100 \text{ ms}}$	Acquisition Time + Calibration Time + 5345A SAMPLE RATE + 60 ms + (1 μs + 5345A GATE TIME) $\frac{\text{EXT GATE WIDTH} \times \text{PRF}}$	
Pulse Width: Min: Max:	100 ns 20 ms	60 ns 20 ms	100 ns 1 s
Pulse Repetition Frequency Min: Max:	NOTE: Minimum off time is 400 ns (i.e., 2 MHz PRF with 100 ns pulses) 50 Hz 2 MHz		
Minimum ON/OFF RATIO	25 dB (TYPICAL)		
Maximum Video Feedthrough	15 mV p-p (TYPICAL) for rf burst rise and fall times $\geq 10 \text{ ns}$		
LSD Displayed	1 Hz/5345A GATE TIME		
Resolution	$\pm 2 \times \text{LSD} \pm \text{rms jitter}^{**}$		$\pm 10 \times \text{LSD} \pm 5 \times \text{rms jitter}^{**}$
Accuracy†	Resolution $\pm \frac{.04}{\text{EXT GATE WIDTH}}$ $\pm 3 \text{ KHz} \pm (\text{Time base error} \times \text{FREQ})$		($\pm 16 \times \text{LSD}$) $\pm$ (5 X rms jitter**) $\pm$ (.08/EXT GATE WIDTH) $\pm 24 \text{ KHz}$ $\pm (\text{Time base error} \times \text{FREQ})$

Specifications apply only to external gating of 5345/5355. ** See jitter specification on following page.

† After one minute warm-up

Model 5355A
General Information

Table 1-1. Model 5355A Specifications (Continued)

5356A OPTION 001 HIGH PASS FILTER SPECIFICATIONS Insertion Loss: <1 dB from 1.5—18 GHz Insertion Loss below 100 MHz: <35 dB	DEFINITIONS LSD Displayed: Unit value of least significant digit. Resolution: Maximum deviation (or rms deviation) between successive measurements under constant environmental and constant input conditions.
GENERAL IF OUT: Down converted signal in range of 80—375 MHz available at 5355 rear panel IF OUT connector. 0 dBm (NOMINAL level) GATE OUT: 0 to -1 volt detected IF signal used to drive 5345A EXTERNAL GATE CONTROL INPUT. Width of GATE OUT is approximately 30 ns less than rf burst width. PULSE OUT: Detected IF signal: TTL levels; TTL low indicates signal present; +1 to 0V TYPICAL into 50Ω. Operating Temperature: 0° to 55°C Weight: 5355A: 3.75 kg (8 lb., 4 oz.) net 5356A/B/C: 0.54 kg (1 lb., 3 oz.) net 5356A/B/C Dimensions: 27.4 mm, 138 mm, 56.6 mm (1.08", 5.43", 2.23") Cable length: 1.60 metres (66")	Accuracy: Deviation from the true value as fixed by universally accepted standards for frequency and time. Minimum ON/OFF Ratio: For a pulsed rf input, the required minimum difference, in dB, between the pulse ON signal level and pulse OFF signal level which will enable the 5355 to distinguish a pulse input. Maximum Video Feedthrough: For a pulse rf input, the maximum peak-to-peak voltage caused by the superposition of video components above 75 MHz, which the 5355/56 can tolerate in the burst. rms jitter = $\frac{1}{\sqrt{(5345A \text{ GATE TIME})^2 + (EXT \text{ GATE WIDTH})^2}} \times X$ $X = 100 \text{ Hz rms}$ For EXT GATE signals generated by the 5355A, the EXT GATE WIDTH equals the input PULSE WIDTH minus 30 ns (TYPICAL) for the 5356A/B/C input and equals input PULSE width minus 40 ns (TYPICAL) for the 5355 0.4—1.6 GHz input.

1-13. SAFETY CONSIDERATIONS

1-14. This product is used as part of a Safety Class I instrument (provided with a protective earth terminal). Safety information pertinent to the operation and servicing of this instrument is included in appropriate sections of this manual.

1-15. EQUIPMENT SUPPLIED

1-16. The only equipment supplied with the 5355A plug-in unit is the BNC Cable (HP Part No. 05355-60101) shown in Figure 1-1.

1-17. ACCESSORIES

1-18. Accessories available for use with the 5355A are as follows (connector and filter options listed in Table 1-2):

- 5356A Frequency Converter Head (1.5—18 GHz)
- 5356B Frequency Converter Head (1.5—26.5 GHz)
- 5356C Frequency Converter Head (1.5—40 GHz)
- Extender Board Service Kit, HP Part No. 05355-60100 (See paragraph 1-19)
- APC 7 to N(f) Adapter, HP 11524A

Table 1-2. 5356 Frequency Converter Head Options

Connector Options	5356A (1.5—18 GHz)	5356B (1.5—26.5 GHz)	5356C (1.5-40 GHz)
TYPE N MALE	Standard or H10 for 24 GHz	N/A	N/A
SMA MALE W/COLLAR	Option H01	Standard	
APC 3.5 MALE W/COLLAR	N/A	Option H01	Standard
WAVEGUIDE	N/A	Option 001 (WR-42)	Option 001 (WR-28)
FILTER OPTION			
High Pass Filter	Option 001	N/A	N/A

1-19. DESCRIPTION

1-20. The 5355A plug-in unit, when used with a 5345A Electronic Counter provides measurements of CW or burst frequencies from 400 MHz to 1.6 GHz. Since the 5345A has a range of 0 to 500 MHz, the 5345A/5355A combination offers frequency measurement capability from 0—1.6 GHz. Frequencies up to 40 GHz may be measured by use of the accessories described in the following paragraph.

1-21. For higher frequency measurements, the 5356A, 5356B, or 5356C Frequency Converter Head is used. The heads use the single sampler, harmonic heterodyne technique to downconvert the input signal frequency. The 5356A allows measurements from 1.5 to 18 GHz, the 5356B allows measurements from 1.5 to 26.5 GHz, and the 5356C allows measurements from 1.5 to 40 GHz. The head connects to the signal source and the attached 5½ foot cable connects to the multi-pin connector on the front panel of the 5355A.

1-22. Signals in the 0.4 to 1.6 GHz range are sent through a prescaler (divider) in the 5355A to the IF circuits. Signals in the 1.5 to 40 GHz range are sent through the down-converter head to the IF circuits. The 5355A automatically acquires the input CW or pulsed rf signal and under control of its microprocessors algorithm, routes the down-converted signal to the 5345A mainframe to be counted and displayed.

1-23. SERVICE EQUIPMENT AVAILABLE

1-24. A kit of extender boards is available to allow servicing printed circuit assemblies while extended from the instrument. The extender boards allow the assemblies to be extended from their plug-in connectors for monitoring with appropriate test equipment. The HP part number of the kit is 05355-60100. Refer to paragraph 8-103 for detailed information.

1-25. RECOMMENDED TEST EQUIPMENT

1-26. The test equipment listed in Table 1-3 is recommended for use during performance tests, adjustments, and troubleshooting. Substitute test equipment may be used if it meets the required characteristics listed in the table.

Model 5355A
General Information

Table 1-3. Recommended Test Equipment

Instrument	Required Characteristics	Recommended Model
Oscilloscope	dc to 275 MHz	HP 1725A
Oscilloscope	dc to 1 GHz	HP 180A/1810A
Oscilloscope	dc to 200 MHz	HP 183C/1830A/1840A
Oscilloscope Probe Kit		HP 10020A
Signal Generator	.1 to 4.3 GHz .4 to 2.0 GHz 2 to 18 GHz 13 to 26.5 GHz 26.5 to 40 GHz	HP 8620C/8621B HP 8620C/86222B HP 8620C/86290B HP 8690B/8696A HP 8690A/8697A
Digital Multimeter	20V range	HP 3465A
AC Voltmeter	10 to 375 MHz	HP 3406A
Power Splitter	dc to 18 GHz	HP 11667A
Signature Analyzer		HP 5004A
Power Meter	10 MHz to 18 GHz	HP 436A
Power Sensor	10 MHz to 18 GHz -30 dBm to +20 dBm	HP 8481A
Spectrum Analyzer	10 MHz to 500 MHz	HP 8565A
Resistive Divider Probe Set	50 Ω , 20:1 Attenuation	HP 10020A
Sweep Analyzer	100 MHz to 1 GHz	HP 8755A/182T
Detector	100 MHz to 1 GHz	HP 11664A
Crystal Detector	18 to 26.5 GHz 26.5 to 40 GHz	HP K422A HP R422A
Power Meter	18 to 26.5 GHz	HP 432A
Thermistor Mount	18 to 26.5 GHz 26.5 to 40 GHz	HP K486A HP R486A
Directional Coupler	18 to 26.5 GHz 26.5 to 40 GHz	HP K752A HP R752A, R752C
Step Attenuator	10 dB step, dc to 26.5 GHz, APC-3.5	HP 8495D (With Option 004)
Attenuator	3 dB, 100 MHz to 1 GHz	HP 8491A
Variable Attenuator	18 to 26.5 GHz 26.5 to 40 GHz	HP K382A HP R382A
Adapter	Waveguide (WR-42) to SMA	OSM P/N 2000-6256-00 Model #20183A)
Adapter	Waveguide to OSM, 26.5 to 40 GHz	Maury Microwave, U223A
Adapter	Waveguide (WR-42) to APC-3.5	Narda 4608B
Waveguide, Straight Section	26.5 to 40 GHz	Maury Microwave, U101A4
Waveguide, Bend	26.5 to 40 GHz	Maury Microwave, U135A
Logic Probe	TTL Compatibility	HP 545A
Logic Pulser	TTL Compatibility	HP 546A
Current Tracer	1 mA to 1A range	HP 547A
AP Clips	Clip for 14/16 pin IC's	HP P/N 705-004B

Table 1-3. Recommended Test Equipment (Continued)

Instrument	Required Characteristics	Recommended Model
Pulse Modulator	2 to 18 GHz	HP 11720A
Pulse Generator	General purpose	HP 8012A
Extender Board Kit	5355A Compatibility	05355-60100
Power Supply	1 to 15V	HP 6284A
Modulator	Sweep Analyzer Compatibility	HP 11665B
Signal Generator	Pulse Modulation Capability 50 to 400 MHz	HP 8640B
Pulse Generator	1 to 20 μ s Pulse Width 1 to 20 μ s Pulse Repetition Rate 0 to 5V Output	HP 8013A
Frequency Counter	To 225 MHz CW	HP 5382A
Frequency Counter	To 120.1 MHz CW	HP 5340A
HP-IB Bus Analyzer	HP-IB Compatibility	HP 59401A
Active Probe	500 MHz	HP 1120A
Probe Power Supply	1120A Compatibility	HP 1122A
Mixer	.2 to 2 GHz (WJM11)	HP P/N 0960-0455

SECTION II INSTALLATION

2-1. INTRODUCTION

2-2. This section provides instructions for unpacking, inspection, preparation for use, storage, and shipment of the 5355A plug-in.

2-3. UNPACKING AND INSPECTION

2-4. If the shipping carton is damaged, inspect the 5355A for visible damage (scratches, dents, etc.). If the 5355A is damaged, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately (offices are listed at the back of this manual). Keep the shipping carton and packing material for the carrier's inspection. The HP Sales and Service Office will arrange for repair or replacement of your instrument without waiting for the claim against the carrier to be settled.

2-5. PREPARATION FOR USE

2-6. Power Requirements

2-7. The 5355A does not require external ac power. All necessary power is supplied by the 5345A when the 5355A is plugged in.

2-8. Operating Environment

2-9. The operating temperature range is 0°C to 55°C. If these limits are exceeded at the installation site, auxiliary cooling or heating should be used to keep environment within limits.

2-10. Installation

2-11. To install the 5355A, proceed as follows:

- a. On the 5345A, set POWER switch to STANDBY.
- b. Pull the locking handle on the left side of the 5355A up to the horizontal position.
- c. Slide the 5355A into the 5345A. Use caution to prevent damage to interface connectors at rear of unit.
- d. Push locking handle down and toward the instrument until it is parallel with the front panel.
- e. For operating information, address switch settings, and connections to rear panel BNC connectors, refer to Section III.

2-12. Compatibility with 5345A

2-13. The 5345A must be in EXT GATE mode when the 5355A is in PULSE mode and must be in INT GATE mode when the 5355A is in CW mode. If the GATE CONTROL switch on the rear panel of the 5345A is left in INT position, then the proper gating mode is selected automatically in 5345A's that have Serial Prefix 1808A or higher. Older 5345A's with serial prefix 1744A and below require manual selection of EXT GATE mode (for PULSE) and INT GATE mode (for CW). However, a minor modification can be added (see paragraph 8-13) which updates these units.

2-14. HP-IB Interconnections

2-15. **HEWLETT-PACKARD INTERFACE BUS.** Interconnection data concerning the rear panel HP-IB connector is provided in Figure 2-1. This connector is compatible with the HP 10833A/B/C/D HP-IB cables. The HP-IB system allows interconnection of up to 15 (including the controller) HP-IB compatible Instruments. The HP-IB cables have identical "piggy-back" connectors on both ends so that several cables can be connected to a single source without special adapters or switch boxes. System components and devices may be connected in virtually any configuration desired. There must, of course, be a path from the calculator (or other controller) to every device operating on the bus. As a practical matter, avoid stacking more than three or four cables on any one connector. If the stack gets too large, the force on the stack produces great leverage which can damage the connector mounting. Be sure each connector is firmly (finger tight) screwed in place to keep it from working loose during use.

2-16. **CABLE LENGTH RESTRICTIONS.** To achieve design performance with the HP-IB, proper voltage levels and timing relationship must be maintained. If the system cable is too long, the lines cannot be driven properly and the system will fail to perform properly. Therefore, when interconnecting an HP-IB system, it is important to observe the following rules:

- a. The total cable length for the system must be less than or equal to 20 metres (65 feet).
- b. The total cable length for the system must be equal to or less than 2 metres (6.6 feet) times the total number of devices connected to the bus.
- c. The total number of Instruments connected to the bus must not exceed 15.

2-17. 5355A Listen Address

2-18. The 5355A contains a rear panel HP-IB instrument address selection switch. There are five switches designated (A₅, A₄, A₃, A₂, A₁) which are used to select the address. Instructions for setting and changing the listen address are provided in Section III of this manual along with programming codes

2-19. HP-IB Descriptions

2-20. A description of the HP-IB is provided in Section III of this manual. A study of this information is necessary if the user is not familiar with the HP-IB concept. Additional information concerning the design criteria and operation of the bus is available in IEEE Standard 488-1975, titled "IEEE Standard Digital Interface for Programmable Instrumentation".

2-21. Operational Check

2-22. To determine if the Instrument is operating properly, refer to the performance check in Section IV. Contact the nearest HP Sales and Service Office (see manual back cover) for information relative to warranty claims

2-23. PACKAGING FOR RESHIPMENT

2-24. Original Packaging

2-25. The same containers and materials used in factory packing can be obtained through the Hewlett-Packard Sales and Service Offices listed at the rear of this manual.

2-26. If the instrument is being returned to Hewlett-Packard for service, attach a tag indicating the type of service required, return address, model number, and full serial number. Mark the container FRAGILE to assure careful handling.

2-27. In any correspondence refer to the instrument by model number and full serial number.

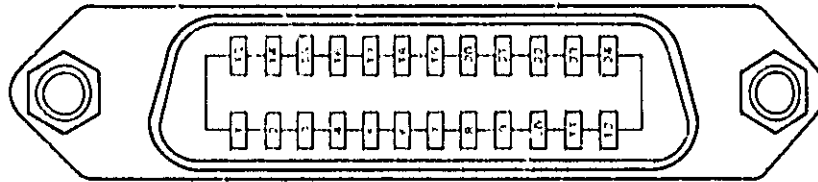
2-28. Other Packaging Methods

2-29. If it becomes necessary to reship an instrument, good commercial packing should be used. Contract packaging companies in many cities can provide dependable custom packaging on short notice. The following general instructions should be followed when repackaging with commercially available materials.

- a. If shipping to a Hewlett-Packard Office or Center, attach a tag indicating the type of service required, return address, model number, and full serial number.
- b. Wrap the instrument in heavy paper or plastic.
- c. Use a strong shipping container. A double-wall carton made of 350-pound test material is adequate.
- d. Use enough shock-absorbing material (3- to 4-inch layer) around all sides of the instrument to provide a firm cushion and prevent movement inside the container. Protect the control panel with cardboard.
- e. Seal the shipping container securely.
- f. Mark the shipping container FRAGILE to assure careful handling.

2-30. STORAGE

2-31. If the instrument is to be stored for an extended period of time, it should be enclosed in a clean, sealed container.

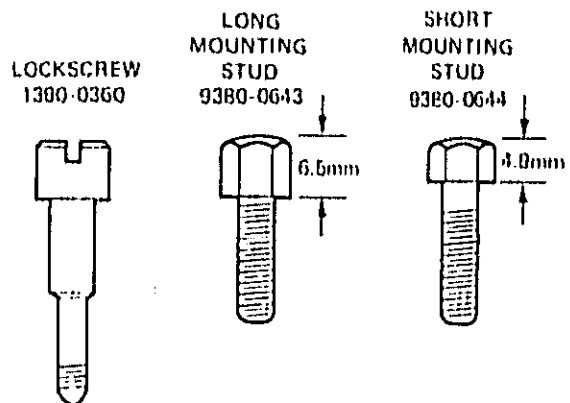


PIN	LINE
1	DIO1
2	DIO2
3	DIO3
4	DIO4
13	DIO5
14	DIO6
15	DIO7
16	DIO8
5	EOI
17	REN
6	DAV
7	NRTD
8	NDAC
9	IFC
10	SRQ
11	ATN
12	SHIELD-CHASSIS GROUND
18	P/O TWISTED PAIR WITH PIN 6
19	P/O TWISTED PAIR WITH PIN 7
20	P/O TWISTED PAIR WITH PIN 8
21	P/O TWISTED PAIR WITH PIN 9
22	P/O TWISTED PAIR WITH PIN 10
23	P/O TWISTED PAIR WITH PIN 11
24	ISOLATED DIGITAL GROUND

THESE PINS
ARE
INTERNALLY
GROUNDED

CAUTION

The 5355A contains metric threaded HP-IB cable mounting studs as opposed to English threads. Metric threaded HP 10631A, B, C, or D HP-IB cable lockscrews must be used to secure the cable to the instrument. Identification of the two types of mounting studs and lockscrews is made by their color. English threaded fasteners are colored silver and metric threaded fasteners are colored black. DO NOT mate silver and black fasteners to each other or the threads of either or both will be destroyed. Metric threaded HP-IB cable hardware illustrations and part numbers follow.



Logic Levels

The Hewlett-Packard Interface Bus logic levels are TTL compatible, i.e., the true (1) state is 0.0V dc to 0.4V dc and the false (0) state is +2.5V dc to +4.0V dc.

Programming

Refer to Section III, Operation

Mating Connector

HP 1251-0293; Amphenol 57-30240.

Mating Cables Available

- HP 10833A, 1 metre (3.28 ft.)
- HP 10833B, 2 metres (6.56 ft.)
- HP 10833C, 4 metres (13.12 ft.)
- HP 10833D, 0.5 metre (1.64 ft.)

Cabling Restrictions for Standard System

1. A Hewlett-Packard Interface Bus System may contain no more than 1.0 metres (6 ft.) of connecting cable per instrument.
2. The maximum accumulative length of connecting cable for any Hewlett-Packard Interface Bus System is 20.0 metres (65.6 ft.).

Figure 2-1. Hewlett-Packard Interface Bus Connection

OPERATION

SECTION III OPERATION AND PROGRAMMING

3-1. INTRODUCTION

3-2. This section contains descriptions of operating characteristics and modes, operating procedures, descriptions of front and rear panel controls and indicators, keyboard test procedures, and Hewlett-Packard Interface Bus (HP-IB) programming information.

3-3. The 5355A is a plug-in for the 5345A Electronic Counter. Operating and programming characteristics of the 5345A must be understood before attempting to operate and program the 5355A. For complete information on the 5345A, refer to the 5345A Operating and Service Manual. When appropriate, the 5355A programming explanations that follow contain notes on the interrelated 5345A programming instructions.

3-4. The 5355A is programmed via the HP-IB. The HP-IB is a carefully defined instrumentation interface which simplifies the integration of instruments, calculators, and computers into systems. The HP-IB is Hewlett-Packard's implementation of IEEE Standard 488-1975, "Standard Digital Interface for Programmable Instrumentation".

3-5. OPERATING CHARACTERISTICS

3-6. The following paragraphs describe the operating ranges and modes, AM and FM tolerance and automatic amplitude discrimination.

3-7. Operating Ranges

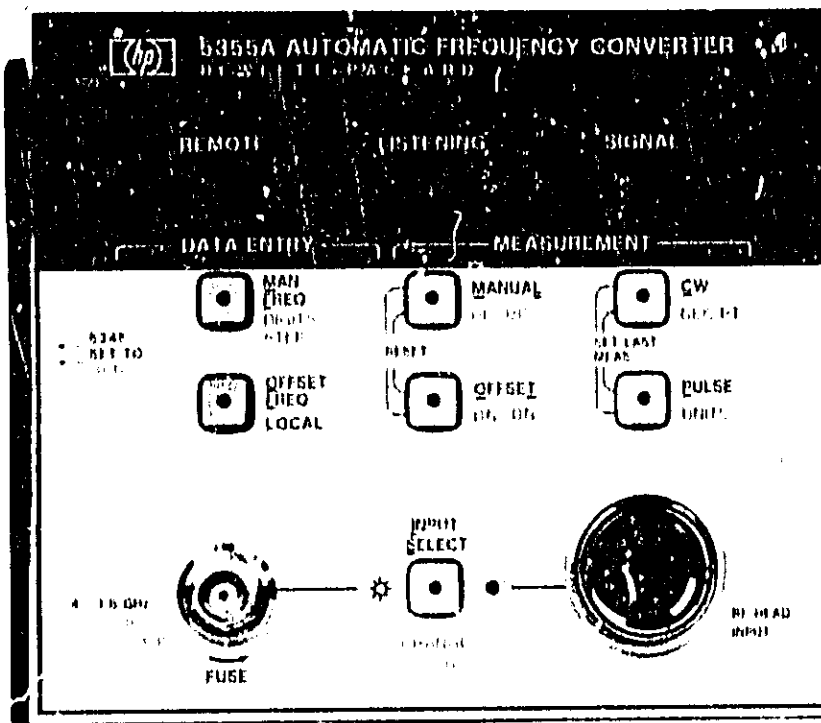
3-8. The two operating ranges are 0.4 to 1.6 GHz, and 1.5 to 40 GHz. Frequencies in the lower range are measured by use of a prescaler technique while frequencies in the higher range are measured by use of a harmonic heterodyne down-conversion technique. A separate front panel input connector is provided for each range (see Figure 3-1). Selection of the two ranges is

provided by the  key on the front panel. When the  key indicator is lit,

the 0.4—1.6 GHz input (BNC) is routed to the prescaler. When the  key indicator is not

lit, the RF HEAD INPUT (multi-pin connector) is sent to the IF circuits. The multi-pin connector input requires the use of the 5356A/B/C Frequency Converter Head. The 5356A covers the range of 1.5 to 18 GHz, the 5356B covers 1.5 to 26.5 GHz, and the 5356C covers 1.5 to 40 GHz. See

Table 1-2. When the  LED is illuminated, the 0.4 to 1.6 GHz input (BNC) is connected, otherwise the RF HEAD INPUT is connected.



INDICATORS

REMOTE. Indicator illuminates when 5355A is under remote operation and all front panel controls are inoperative except the LOCAL key (unless Local Lockout command has been sent).

LISTENING. Indicator illuminates when 5355A is addressed and monitoring the interface bus.

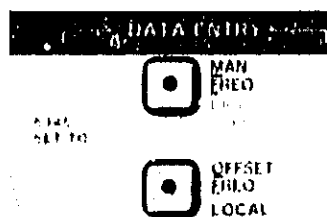
SIGNAL. Indicator illuminates when input signal is of sufficient level to be counted.

KEY INDICATORS. Indicator within a key illuminates when the key is pressed to initiate the key function. Pressing the key again releases the function and the indicator extinguishes (except for the CW and PULSE keys).

CONTROLS

All front panel controls are pushbutton keys with center indicators that indicate the operating function of the plug-in. The keys are grouped under two general functional headings, DATA ENTRY and MEASUREMENT, as described below.

DATA ENTRY Keys



The two color-coded DATA ENTRY keys on the left side of the front panel are used to enter data for a manual center frequency or an offset frequency. When one of these keys is enabled (key indicator illuminated) the functions of the MEASUREMENTS keys to the right are defined by the label whose color corresponds to that of the enabled DATA ENTRY key.

Figure 3-1. Front Panel Controls, Connectors and Indicators

MEASUREMENT KEYS



When key is pressed and illuminated, enters the manual center frequency shown on the counters

display (controlled by  or ).

When  pressed again and extinguished,

and  pressed, counter displays mea-

surement. The DIGIT STEPS (blue-label) function is in effect when OFFSET FREQ key (blue) is illuminated. Each time the DIGIT STEPS key is pressed, the display is expanded by two digits until 10 decimal places are displayed (depending upon resolution).



When pressed and illuminated, this key enters the offset frequency (controlled by the UP or DN key) on the counters display and activates all key functions labeled in blue. The OFFSET FREQ key function is in LOCAL control unless the REMOTE

Indicator is illuminated. When  key is

pressed again and extinguished, and 

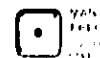
pressed, counter displays the measurement. Successive presses will result in alternate display of measured and offset frequencies. The offset frequency is positive unless the minus (-) sign is

displayed (controlled by the  key).



When key is pressed and illuminated, a manual frequency measurement is displayed, provided a manual center frequency, within 50 MHz of the

input signal has been entered via the



function (DATA ENTRY). When either DATA ENTRY key is in effect (illuminated) the UP function will cause the display to count up while the UP key is held in. If both the MANUAL and OFFSET keys are pressed simultaneously, the display will reset.



When key is pressed and illuminated, a resultant frequency (sum or difference of input signal and offset frequency) is displayed, provided an offset

frequency has been entered via the  key.

When either DATA ENTRY key is in effect (illuminated) the DN function will cause the display to count down while the DN key is held in.

NOTE

If both



keys are pressed

simultaneously, the display will reset.

Figure 3-1. Front Panel Controls, Connectors and Indicators (Continued)



When key is pressed and illuminated, a CW signal input frequency is automatically acquired, measured and displayed. The CW measurement mode is initiated whenever power is applied to the plug-in.



When the DEC PT key function is active (illuminated) the DEC PT (blue-label) function is active. With at least 3 digits displayed, the DEC PT key shifts the decimal point on the display to the right one place for each of the first two presses of the DEC PT key, then two places to the left on the third press. This sequence repeats for successive presses of the key.



When key is pressed and illuminated, a pulsed RF signal input frequency is automatically acquired, measured and displayed.

NOTE

To operate in PULSE mode, the GATE OUT connector on the rear panel of the 5355A must be connected to the GATE CONTROL INPUT connector on the rear panel of the 5345A.



When the UNITS key function is active (illuminated) the UNITS (blue-label) function is active. The UNITS key shifts the displayed resolution annunciator from GHz to MHz, kHz, Hz, mHz, and μ Hz, respectively, with each successive press of the UNITS key.

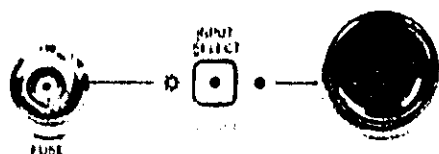
NOTE



If both the SET LAST MEAS and PULS keys are pressed



simultaneously (SET LAST MEAS) the last measurement will be displayed on the 5345A if the 5355A is in the OFFSET FREQ or MAN FREQ DATA ENTRY mode. (See Table 3-5.)



When key is pressed and illuminated, the 0.4 to 1.6 GHz is connected. Otherwise, the RF HEAD INPUT is connected. If the 5356A/B/C Frequency Converter Head is not connected to the 5355A, the 0.4 to 1.6 GHz input is automatically selected when power is applied.



When the CHANGE SIGN key function is active (illuminated) the CHANGE SIGN key function is active. Each time the key is pressed, the minus (-) sign changes (on or off) in the display.

Figure 3-1. Front Panel Controls, Connectors and Indicators (Continued)

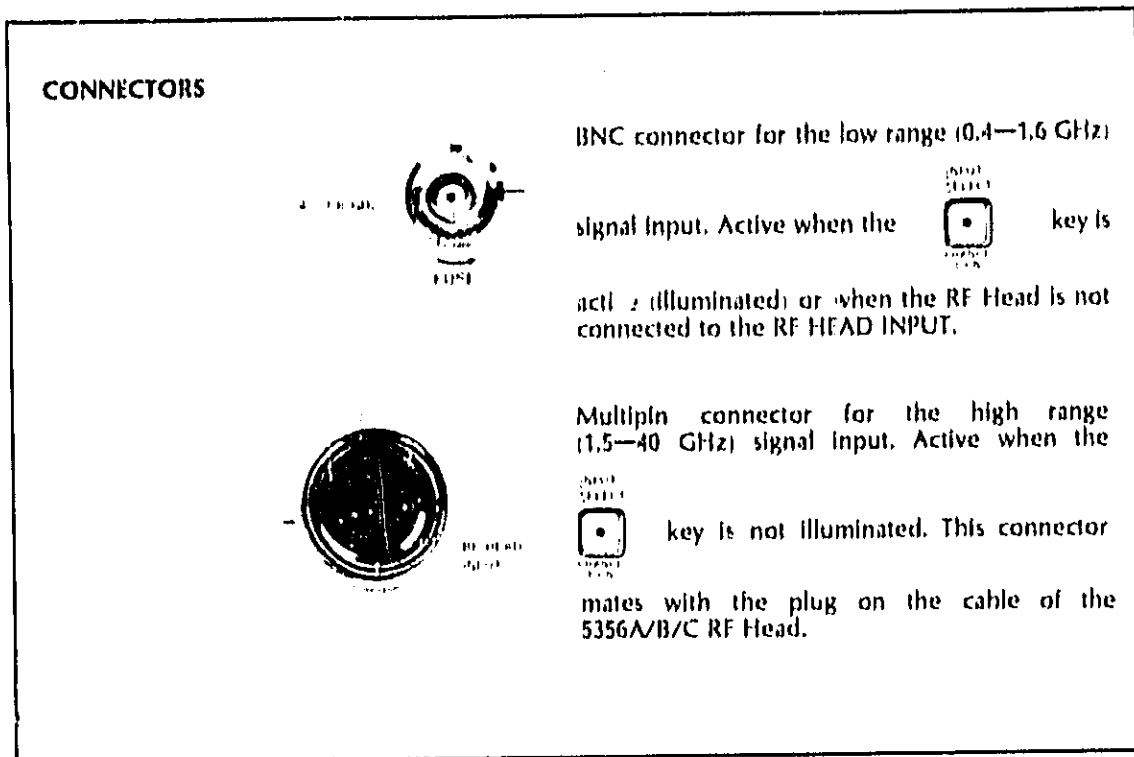


Figure 3-1. Front Panel Controls, Connectors and Indicators (Continued)

3-9. Operating Modes

3-10. Operating modes are selected by the front panel pushbutton keys. The following modes may be selected:

- CW
- Pulsed RF
- Manual
- Offset

3-11. CW Mode

3-12. The automatic mode of operation for CW signals is initiated by applying power to the instrument. Input CW signals are acquired, measured and displayed automatically. The illuminated indicator in the CW key shows the operator that this mode of operation is in effect. If other key indicators are illuminated, the 5355A is operating in the mode indicated.

3-13. Pulsed RF Mode

3-14. The Pulsed RF mode (for reception of pulsed RF signals) is initiated by pressing  on the front panel. To operate in this mode, the GATE OUT connector on the rear panel of the 5355A must be connected to the GATE CONTROL INPUT connector on the rear panel of the 5345A. Input pulsed RF signals are acquired, measured, and displayed automatically. The illuminated indicator in the PULSE key shows the operator that this mode of operation is in effect. Measurement of a pulsed RF signal is described in Table 3-2.

3-15. Manual Mode

3-16. The manual mode of operation is initiated by pressing the  key. To operate in this mode, the input signal frequency must be known within 50 MHz and this manual frequency must be entered into the display prior to the measurement. Use of the manual mode is described in the following paragraph and an example is shown in Table 3-3.

3-17. Pressing the  key results in a display of the low frequency listed below (or a previously entered manual frequency). The  key indicator lights and the gold-labeled key functions are in effect. Press and hold the  key to cause the display to count up to the high frequency listed below in .1 GHz (100 MHz) steps. Press and hold the  key to cause the display to count down to the low frequency in .1 GHz steps. These keys are used to set the display to a frequency within .1 GHz of the input signal. Press and release the  key to depart the DATA ENTRY function and press  to enter the MEASUREMENT function. The following table lists the high and low frequency displayed for each mode of the 5356 Frequency Converter Heads:

Head Installed	Display High Frequency (GHz)	Displayed Low Frequency (GHz)
5356A/B	40	1.5
5356B, Option 001	27.7	17
5356C	60	1.5
5356C, Option 001	60	17

3-18. OFFSET Mode

3-19. The OFFSET mode is used to add or subtract a constant to/from a measurement. For example, a radio frequency can be measured by measuring the local oscillator frequency and then adding the IF as a positive offset. Use of the OFFSET mode is described in the following paragraph and an example is shown in Table 3-4.

3-20. The OFFSET mode of operation is initiated by pressing the  key, which results in a display of -1 GHz (or a previously entered offset frequency). The  key indicator lights and the blue-labeled key functions are in effect.   keys cause the display to count up or down between 1. and 9. GHz to select the offset frequency. The display can be expanded and the resolution of the offset frequency increased by using the  key and  key functions. In addition,  key can be used for limited

shifting of the decimal point. The  key adds two digits to the display each time it is pressed for a total of 10 decimal places.  key changes the display annunciators from GHz to MHz, kHz, Hz, mHz, and μ Hz.

3-21. When the offset frequency has been selected as described in the preceding paragraph, press and release the  key to depart the DATA ENTRY mode and press  key to enter the OFFSET mode.

3-22. Remote Programming Mode

3-23. The 5355A is remotely controlled via internal interface circuits and a rear panel connector to the Hewlett-Packard Interface Bus (HP-IB). The 5355A operates in the Listen Only mode. Remote programming is described in detail in paragraph 3-50.

3-24. The REMOTE indicator on the front panel, when illuminated, indicates the 5355A is under remote operation and all front panel controls are inoperative, except  pushbutton (unless the Local Lockout command has been sent).

3-25. The LISTENING indicator on the front panel, when illuminated, indicates the 5355A is addressed and monitoring the interface bus.

3-26. AM Tolerance

3-27. The 5355A/5345A will measure carrier frequencies containing amplitude modulation to any modulation index provided the minimum voltage of the signal is greater than the sensitivity specification of the 5355A.

3-28. FM Tolerance

3-29. The 5355A/5345A will measure carrier frequencies which are modulated in frequency such as a microwave radio carrier. The FM tolerance is the worst case FM deviation which can be present without affecting the counter's ability to acquire the signal. If the deviations about the carrier are symmetrical, then the counter averages out the deviations to measure the actual carrier frequency. The FM tolerance is determined by the mode of operation. See Table 1-1. The auto mode provides FM tolerance of 15 MHz peak-to-peak. A special FM mode is selected by

pressing  and  simultaneously (in CW auto mode). The special FM mode provides a tolerance of 60 MHz peak-to-peak but results in slower acquisition time (1.1 second compared to 400 milliseconds for CW position).

NOTE

Most measurements should be made without using the special FM mode. The special FM mode should be used only when the input signal has significant amounts of FM (>15 MHz p-p).

3-30. Automatic Amplitude Discrimination (CW Mode)

3-31. The automatic amplitude discrimination feature allows the 5355A to acquire and display the highest level signal within its sensitivity range. The highest level signal must be 8 dB greater in amplitude than any other signal present within 500 MHz and 20 dB greater than any signal over the full range. This feature is useful for discriminating against spurious signals and harmonics.

3-32. OPERATING PROCEDURES

3-33. Operating procedures for the 5355A are given in the following paragraphs. Refer to *Figures 3-1 and 3-2* for descriptions of front and rear panel controls, connectors and indicators, and to *Tables 3-2 through 3-5* for specific examples. Power-up codes are described in paragraph 3-54, Frequency Converter Head codes in paragraph 3-56, and frequency range coverage in *Table 6-21*. Refer to the 5345A manual for operating procedures for the 5345A.

3-34. Preliminary Procedures

3-35. To operate the 5355A and 5345A combined, perform the following preliminary procedures:

- a. Set the 5345A POWER switch to STANDBY.
- b. Set the 5345A FUNCTION switch to PLUG-IN.
- c. Install the 5355A into the 5345A as described in Section II, and attach GATE cable as described in paragraph 3-14.
- d. Set the 5345A SAMPLE RATE fully ccw.
- e. Set 5345A DISPLAY POSITION switch to AUTO, GATE TIME switch to 100 μ s, and channel select switch to COM A or SEP.
- f. Set 5345A rear panel GATE CONTROL INPUT switch to INTERNAL.

3-36. CW Signal Operation

3-37. Perform the preliminary procedures in paragraph 3-35 and proceed:

CAUTION

Do not connect signals with power levels greater than +24 dBm to the BNC input connector.



- a. For source signals in the .4 to 1.6 GHz range, connect the signal from the source to the BNC connector on the front panel of the 5355A.

CAUTION

Do not connect signals with power levels greater than 300 milliwatts (+25 dBm), peak to the 5356A/B/C Frequency Converter Head. Higher power levels may damage internal circuits.

- b. For signals in the 1.5—40 GHz range, refer to *Table 1-2* for the 5356 model to use. Connect the Frequency Converter Head to the source and connect the attached cable to the 5355A.



- c. Set the 5345A POWER switch to ON.

- d. If the signal is of sufficient amplitude to light the 5355A SIGNAL Indicator, the signal will be automatically measured and displayed on the 5345A.
- e.  indicator light should be on.

3-38. Pulsed RF Signal Operation

3-39. Use the same procedures as in CW Signal Operation (paragraph 3-37) except as follows (see Table 3-2):

NOTE

In the following step, use of a cable of different length may cause measurement errors.

- a. Connect the GATE OUT connector on the rear panel of the 5355A to the GATE CONTROL INPUT connector on the rear panel of the 5345A, using the 10502A cable provided.
- b. Place the 5345A GATE CONTROL switch to INT. (In this switch position a control signal from the 5355A automatically sets the 5345A to EXT GATE mode when PULSE mode on the 5355A is selected and to INT GATE mode when CW mode on the 5355A is selected. However, older 5345A's with Serial Prefix 1744A and below do not have this capability. For these 5345A's when in PULSE mode, set the 5345A GATE CONTROL switch to EXT and when in CW mode, set the switch to INT. A minor modification (see paragraph 8-13) can be made which updates the older 5345A's for automatic selection of EXT/INT GATE.)
- c. Press  key on the front panel of the 5355A.

NOTE

In the 5355A's PULSE mode, a calibration factor is automatically computed during the first 10 measurements (a  is displayed in the 5345A's most significant digit to indicate that the calibration factor is being computed). All subsequent frequency measurements are multiplied by the calibration factor in order to reduce the effects of error. The calibration factor remains unchanged unless the external gate width changes by more than 12% in which case another calibration factor is computed. The accuracy specification applies to readings after the first 10 (see Table 1-1).

3-40. Manual Signal Operation

- a. Press  key and use the  or  to enter a manual center frequency that is within 50 MHz of the input signal frequency.
- b. Press  key again to release the DATA ENTRY mode and press  key to enter the MEASUREMENT mode.

3-42. Offset Measurements

3-43. To make offset measurements proceed as follows (see Table 3-4):

- a. Make a CW measurement or a pulsed RF measurement as listed in the applicable procedures in the above paragraphs.

NOTE

In the following step, the offset frequency will be preceded by a minus (-) sign for a negative offset.

To change to a positive offset, press the  key.

- b. Press the  key to display the offset frequency.
- c. Press the  or the  key to change the value of the offset frequency displayed.
- d. Use the  key to expand the display, the  key to move the decimal point and  key to change the units annunciators as described in Table 3-1.
- e. Press the  key to extinguish the key indicator and enter the MEASUREMENT mode. The input signal should be displayed.
- f. Press  key to illuminate the key indicator and display the resultant frequency (sum or difference of input signal frequency and offset frequency. Will be the difference if offset displayed was preceded by a minus (-) sign).

3-44 Set Last Measurement Function

3-45. The SET LAST MEAS function (labeled on the front panel) is used in the offset mode or the manual mode to automatically store the last measurement as a negative offset or as a manual

center frequency. This function is accomplished by pressing  keys simultaneously.

while in the offset or manual data entry mode. Refer to Table 3-5 for an example of the SET LAST MEAS function.

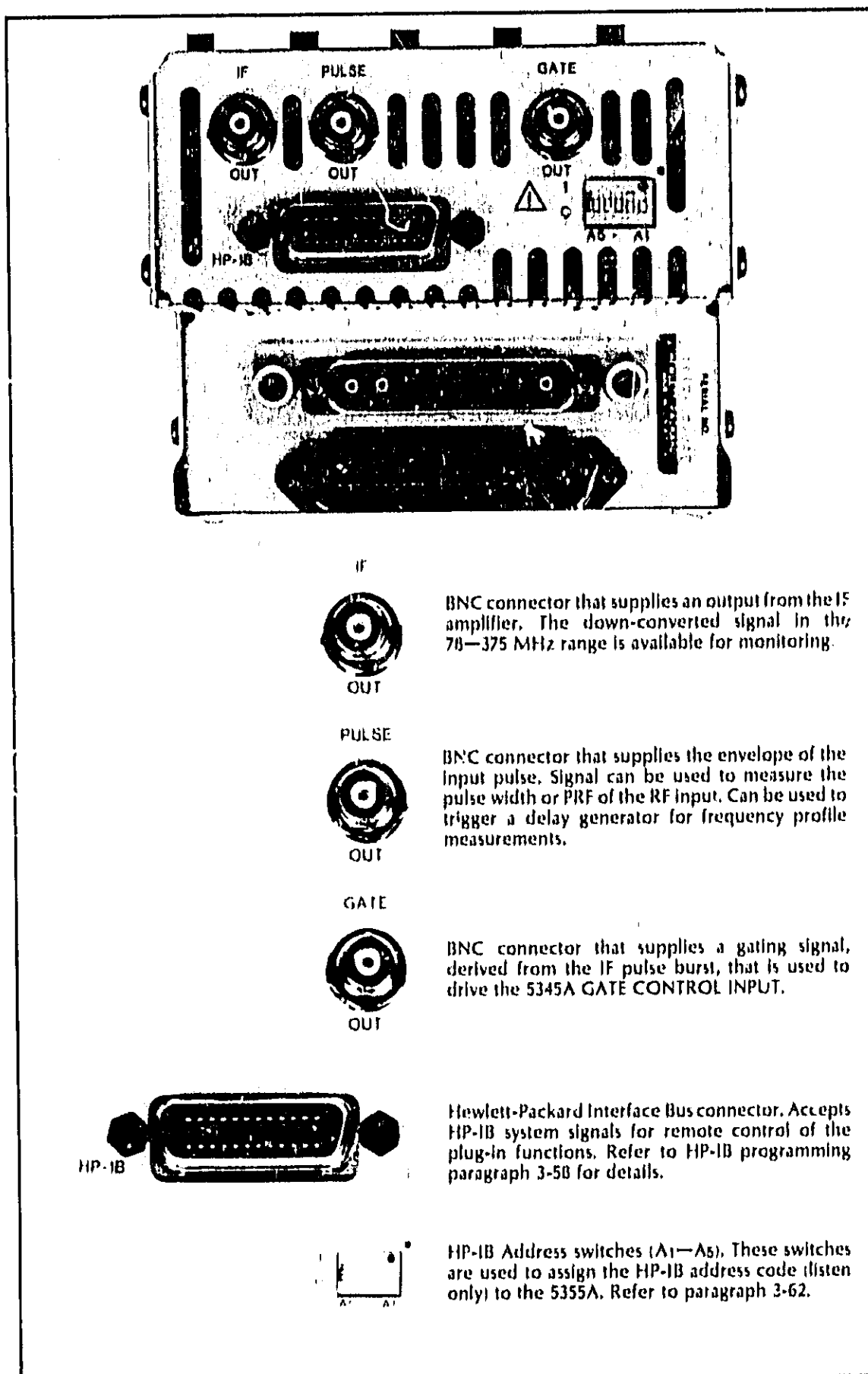


Figure 3-2. Rear Panel Control and Connectors

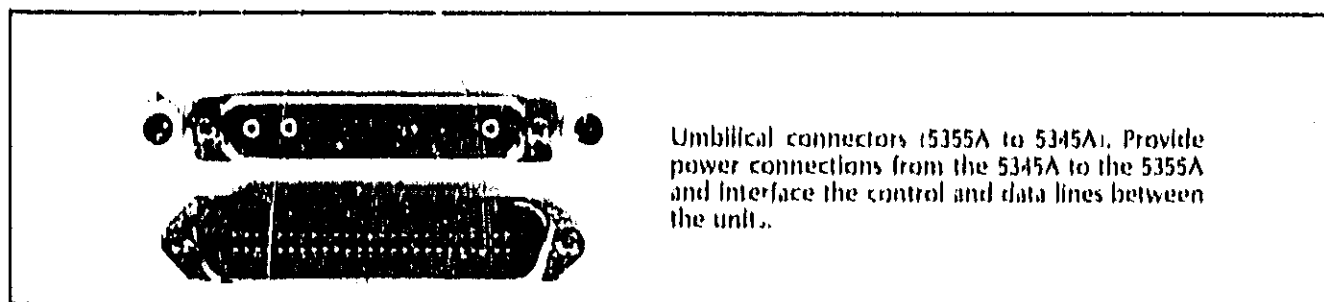


Figure 3-2. Rear Panel Control and Connectors (Continued)

3-46. KEYBOARD CHECK

3-47. Check for proper operation of the keyboard and display by performing the procedures listed in Table 3-1.

Table 3-1. Keyboard Check

NOTE		
Perform the preliminary procedures in paragraph 3-34 and connect a 5356A/B/C Frequency Converter Head to the 5355A prior to proceeding. If a 5356B, Option 001 or 5356C is used refer to paragraph 3-17 for differences in frequencies displayed in steps 4 and 7 through 12.		
STEP	PROCEDURE	RESULTS
1	Set 5345A POWER switch to ON	All 5355A key LEDs illuminate momentarily.
2	Press  PULSE UNITS	 key illuminates. 5345A displays head code momentarily. See paragraph 3-56.) 5345A displays all zeros.
		 key LED illuminates.
		 key LED extinguishes. 5345A displays all zeros, except the most significant digit shows  when pulse signal is present (for calibration routine.) See note in paragraph 3-39 for details.
3	Return to CW mode by pressing  CW DISC PT	5345A displays all zeros.
4	Press  MANUAL UP	Key LED illuminates. 5345A displays 1.5 GHz for one second, then all zeros.
5	Turn manual mode off by pressing  MANUAL DOWN	Key LED extinguishes.
6	Press  OFFSET DOWN	Key LED illuminates. 5345A displays -1.0000000000 GHz.
	Turn off offset mode by pressing  OFFSET ON	Key LED extinguishes. 5345A displays all zeros.

Table 3-1. Keyboard Check (Continued)

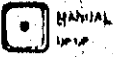
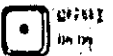
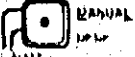
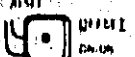
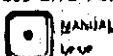
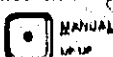
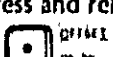
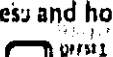
STEP	PROCEDURE	RESULTS
7	Press 	Key LED illuminates. 5345A displays 1.5 GHz, CW key LED extinguished. NOTE Leave MAN FREQ mode in effect (key LED on) for steps 8 through 12.
8	Press and release 	5345A displays increments by 0.1, i.e., display increases to 1.6.
9	Press and hold 	5345A displays rapidly increments up to 40 and rolls over to 1.5.
10	Press and release 	5345A decrements by 0.1 each time the key is pressed. If display is 1.5 before pressing key, display will roll back to 40.
11	Press and hold 	5345A display rapidly decrements back to 1.5 before rolling over to 40.
12	Simultaneously press  and 	5345A display resets to 1.5.
13	Press  to turn off manual mode	Key LED extinguishes. 5345A displays all zeros.
14	Press 	Key LED illuminates. 5345A displays -1. GHz, CW key LED extinguishes. NOTE Leave OFFSET FREQ mode in effect (key LED on) for steps 15 through 25.
15	Press and release 	5345A displays increments by 1 each time key is pressed.
16	Press and hold 	5345A rapidly increments up to 9, then rolls over to 1.
17	Press and release 	5345A display decrements by 1 each time key is pressed.
18	Press and hold 	5345A display rapidly decrements.

Table 3-1. Keyboard Check (Continued)

STEP	PROCEDURE	RESULTS
19	Press and release 	5345A displays two additional zeros. These two digits may be incremented by the  key and decremented by the  key.
20	Simultaneously press and release  and 	5345A display resets to -1. GHz.
21	Press and release 	5345A minus sign (-) display goes blank. Press this key again to display minus sign.
22	Press 	5345A displays -1.00 GHz.
23	Press and release 	5345A display decimal point shifts one place to the right each time the key is pressed for the first two presses, then shifts two places to the left for the third press. This sequence repeats.
24	Press and release 	For each press of the key, the 5345A displays a different unit of measurement, in the following order: GHz, MHz, kHz, Hz, mHz, and μ Hz. Displays -1. μ Hz.
25	Turn off the OFFSET FREQ mode by pressing 	5345A displays all zeros.
26	Press 	Key LED illuminates.

Table 3-2. Pulsed RF Measurements

NOTE

Connect the GATE OUT connector on the rear panel of the 5355A to the GATE CONTROL INPUT connector on the rear panel of the 5345A, using 10502A cable provided.

STEP	PROCEDURE	RESULTS
1	Perform the preliminary procedures in paragraph 3-34. Set the 5345A POWER switch to ON.	The 5355A key LED: illuminate momentarily.  key illuminates. 5345A displays head code momentarily. (See paragraph 3-56.) 5345A displays all zeros.
2	Apply pulsed RF signal to RF HEAD INPUT and press 	SIGNAL LED and  LED illuminate. 5345A displays signal frequency.

Table 3-3. Manual Measurements

NOTE

The manual measurement mode decreases acquisition time (see Table 1-1) and can be used if the input frequency is known within 50 MHz.

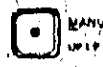
STEP	PROCEDURE	RESULTS
1	Perform the preliminary procedures in paragraph 3-34. Set the 5345A POWER switch to ON.	The 5355A key LEDs illuminate momentarily.  key illuminates. 5345A displays head code momentarily. (See paragraph 3-56.) 5345A displays all zeros.
2	Press 	Key LED illuminates. 5345A displays the low frequency listed in paragraph 3-17.
3	Press and Hold  until displayed number is within 50 MHz of the known input signal frequency.	5345A displays selector number.
4	Press and release  Press 	Key LED extinguishes. Key LED illuminates. 5345A displays input signal frequency. CW key LED illuminates. SIGNAL LED illuminates.

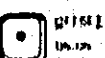
Table 3-4. Offset Measurements

NOTE

The offset measurement mode allows a constant to be added to or subtracted from a measurement, as shown below.

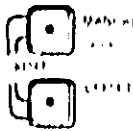
STEP	PROCEDURE	RESULT
1	Perform the preliminary procedures in paragraph 3-34. Set the 5345A POWER switch to ON.	The 5355A key LED's illuminate momentarily.  key illuminates. 5345A displays head code momentarily. (See paragraph 3-56.) 5345A displays all zeros.
2	Press 	Key LED illuminates. 5345A displays -1. GHz.
NOTE Steps 3 through 9 show how to expand the number of digits in the display, position the decimal point and select displayed resolution for precise offset frequencies. If these procedures are understood, proceed to step 10.		
3	Press 	5345A display changes from -1. to -1.00 GHz.
4	Repeat step 3 four more times	5345A display adds two zeros each time key is pressed (for a total of 10 zeros).
5	Press 	Key LED illuminates. Decimal point moves one place to right.
6	Repeat step 5	Same as step 5.
7	Repeat step 5	Decimal point moves two places to left.
8	Press 	5345A display change from GHz to MHz.
9	Repeat step 8 five more times.	5345A display changes from MHz to kHz, Hz, mHz, μ Hz, and back to GHz, in that order.
10	Using procedures described in steps 3 through 9, select desired offset frequency.	5345A displays offset frequency.
11	Apply signal to be measured to RF HEAD INPUT, then press 	Key LED extinguishes. 5345A displays input signal.
12	Press 	Key LED illuminates. 5345A displays resultant frequency.

Table 3-5. Set Last Measurement Functions

NOTE		
For automatic offset mode or manual mode operation perform the preliminary procedures in paragraph 3-34, and connect the signal to be measured to the 5355A. Perform steps 1 through 3 for manual mode. Perform steps 4 through 6 for offset mode of operation.		
STEP	PROCEDURE	RESULTS
FOR MANUAL MODE:		
1	To set the last measurement as a manual center frequency press  frequency press	Key LED illuminates. 5345A displays any previously entered manual center frequency or the low frequency (listed in paragraph 3-17).
	Simultaneously press  	Sets the manual center frequency determined by the last measurement.
2	Press  to exit the d.b.t. entry mode.	Key LED extinguishes. 5345A displays input frequency.
3	Press  to enter the manual mode.	Key LED illuminates. 5345A displays input frequency in manual mode.
FOR OFFSET MODE:		
4	To automatically store the last measurement as a negative offset, press 	Key LED illuminates. 5345A displays any previously entered offset or -1. GHz.
	Simultaneously press:  	5345A displays the last measurement as a negative offset.
5	Press  to exit the offset mode.	Key LED extinguishes. 5345A displays input frequency.
6	Press  to enter offset mode.	5345A displays the drift of the input frequency.

3-48. RESET FUNCTION

3-49. The RESET function, as shown,



requires that the MANUAL and OFFSET keys

be pressed simultaneously. This action resets the display during either DATA ENTRY mode of operation. The display resets to 1.5 GHz (or low frequency listed in paragraph 3-17) when in the manual mode and resets to -1 GHz when in the offset mode. The RESET function allows for error correction in the DATA ENTRY mode.

3-50. SPECIAL MODES

3-51. The two special modes are (1) the FM tolerance mode which increases FM tolerance from 15 MHz p-p to 60 MHz p-p in the automatic mode of operation, and (2) the continuous calibration mode during pulse operation which causes the measurements to be continuously calibrated instead of just the first 10 measurements, as in normal calibration. Procedures for entering the special modes are described below.

3-52. FM TOLERANCE. To enter the special FM tolerance mode during the CW mode of

operation, simultaneously press



keys. The  key will continue flashing during this mode.

3-53. CONTINUOUS CALIBRATION. To calibrate continuously during the pulse mode of

operation, simultaneously press

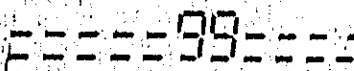
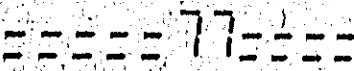


keys. A flashing  will be displayed in the most

significant digit position during calibration.

3-54. POWER-UP CODES

3-55. When power is applied to the 5355A, certain error codes are displayed on the 5345A to indicate error conditions. Diagnostic indications used for troubleshooting are listed in paragraph 8-197. Operating error indications are listed below:

DISPLAY	ERROR CONDITION
 (CW Automatic only)	5345A rear panel GATE CONTROL INPUT switch in wrong position. Should be in INTERNAL position.
	Harmonic number (n)=0 due to a low input frequency or due to the CHECK/COM A/SEP switch on 5345A front panel in CHECK position. Should be in COM A or SEP.
	Indicates the CHECK/COM A/SEP switch on 5345A front panel in CHECK position. Should be in COM A or SEP.

3-56. CONVERTER CODES

3-57. When power is applied to the 5355A certain codes are displayed to indicate which Frequency Converter Head is installed, as follows:

DISPLAY	HEAD INSTALLED
=====0=====	5356A (1.5—18 GHz)
=====1=====	5356B (1.5—26.5 GHz)
=====2=====	5356B Option 001 (18-26.5 GHz)
=====4=====	5356C (1.5—40 GHz)
=====5=====	5356C Option 001 (26.5-40 GHz)

3-58. PROGRAMMING

3-59. Bus Characteristics

3-60. The capability of a device connected to the HP-IB is specified by the interface functions that it has. Table 3-6 lists the interface functions included in the 5355A. The "Interface Function Subset Identifier" refers to the particular capability of the interface function as listed in Appendix C of IEEE Standard 488-1975.

Table 3-6. HP-IB Interface Capability

INTERFACE FUNCTION SUBSET IDENTIFIER	INTERFACE FUNCTION DESCRIPTION
SH0	No source handshake capability.
AH1	Complete acceptor handshake capability.
T0, TE0	No talker (no basic talker, no serial poll, no talk only mode, does not unaddress to talk if addressed to listen).
L2, LE0	Listener (basic listener, no listen only mode, does not unaddress to listen if addressed to talk).
SR0	No service request capability.
RL1	No complete remote/local capability (with local lockout).
PP0	No parallel poll capability.
DC1	Device clear capability (presets to power-up control states).
DT1	Device trigger capability.
C0	No controller capability.
E1	1 Unit Bus Load.
NOTE: Interface functions provide the means for a device to receive, process and send messages over the bus.	

3-61. Bus messages are of 12 types. Table 3-7 lists each bus message, a brief description of the message, and the response of the 5355A/5345A to the message. The last column shows typical examples of how to send/receive each message using the 9825A computing controller. For complete details on sending bus messages using the 9825A refer to the "9825A Extended I/O Programming Manual" (Part Number 09825-90025).

Table 3-7. 5355A Bus Message Usage

Message	Description	5355A Use	Sample 9825 State-ments (5355A Set to Address 02)
Data	Transfers device-dependent information from one device to one or more devices on the bus.	5355A sends measurement data via its talk output. 5355A is controlled by program codes. See Table 3-9 for code set.	red 702, A wrt 702, "PRHD1T"
Trigger	Causes a group of selected devices to simultaneously initiate a set of device-dependent actions.	Starts a new measurement.	trg 7 or trg 702
Clear	Causes an instrument to be set to a predefined state (a certain range, function, etc.).	Preset code PR presets 5355A to power-up condition and triggers one measurement.	wrt 702 "PR"
Remote	Permits selected devices to be set to remote operation, allowing parameters and device characteristics to be controlled by Bus Messages.	5355A goes to remote if REN is true and addressed to listen. In absence of program data, remote operation is according to the state of the front panel settings just prior to going to remote.	ram 702
Local	Causes selected devices to return to local (front panel) operation.	5355A goes to local front panel control. In absence of front panel data, local operation is according to the state of the remote data just prior to going to local.	lcl 702
Local Lockout	Disables local (front panel) controls of selected devices.	Disables front panel control. 5355A remains in remote.	llo 7
Clear Lockout and Local	Returns all devices to local (front panel) control and simultaneously clears the Local Lockout Message.	Local lockout cleared and returns to local front panel control.	lcl 7
Require Service	Indicates a device's need for interaction with the controller.	None	—
Status Byte	Presents status information of a particular device; one bit indicates whether or not the device currently requires service, the other 7 bits (optional) are used to indicate the type of service required.	None (refer to Table 3-10 for status display).	—
Status Bit	A single bit of device-dependent status information which may be logically combined with status bit information from other devices by the controller.	None	—
Pass Control	Passes bus controller responsibilities from the current controller to a device which can assume the Bus supervisory role.	None	—
Abort	Unconditionally terminates Bus communications and returns control to the system controller.	5355A unlistens.	cli 7

3-62. Address Selection

3-63. The 5355A must be assigned a bus address. *Table 3-8* gives the allowable address switch settings. The setting of switches A₁ through A₆ defines the addresses. The listen address (*Table 3-8*) is used to program the functions of the 5355A.

3-64. Before learning the programming details of the 5355A, some knowledge of 5345A programming is required, as described below.

3-65. Programming the 5355A/5345A

3-66. The 5355A is programmed for remote control of all its operating modes by the codes shown in *Table 3-9*. The 5355A operates remotely only in the listen function and does not output to the HF-IB.

3-67. Measurement data from the 5355A is sent to the 5345A for processing and display. This information is sent to the HF-IB via the talk output of the 5345A which must be programmed by the codes shown in the 5345A Operating and Service Manual, except as described in paragraph 3-68 below.

NOTE

5345A program codes E9 and J1 are invalid when the 5355A is plugged in, as detailed in the following paragraph.

3-68. INVALID 5345A PROGRAM CODES. The 5345A program codes E9 (Sample Rate Hold) and J1 (Sample Trigger Command) are invalid when the 5355A is plugged into the 5345A. These functions are performed by programming the 5355A plug-in using the Hold code, i.e., HD0 selects the 5345A Sample Rate and HD1 is used in place of the normal 5345A code E9 for Sample Rate Hold. (Refer to *Table 3-9*).

NOTE

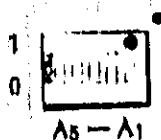
When the 5345A is operating in remote control, the rear panel GATE CONTROL INPUT switch function must be programmed according to the operating mode of the 5355A. The 5345A must be programmed for External Gate (E₂) when the 5355A is in the pulse mode of operation. The 5345A must be programmed for Internal Gate (E₃) when the 5355A is in the CW mode of operation.

3-69. Status Display

3-70. The status of the 5355A operation is shown on the display of the 5345A when program code R (Read Status) is sent to the 5355A. The display contains a digit in each position that indicates the mode of operation (first 8 digits) the head code (9th digit) and the error code or diagnostic mode (10th and 11th digits) as illustrated in *Table 3-10*. The head code indicates which Frequency Converter Head is installed. The error codes are described in paragraph 3-54. Diagnostic modes are described in *Table 3-11*.

Table 3-8. Address Selection

ADDRESS SWITCHES



NOTE

Select the listen address from the table below and set the address switches to the corresponding positions.

ASCII CODE CHARACTER	ADDRESS SWITCHES					5-BIT DECIMAL CODE	OCTAL CODE
LISTEN	A5	A4	A3	A2	A1		
SP	0	0	0	0	0	00	040
!	0	0	0	0	1	01	041
"	0	0	0	1	0	02	042
#	0	0	0	1	1	03	043
\$	0	0	1	0	0	04	044
%	0	0	1	0	1	05	045
&	0	0	1	1	0	06	046
'	0	0	1	1	1	07	047
(	0	1	0	0	0	08	050
)	0	1	0	0	1	09	051
*	0	1	0	1	0	10	052
+	0	1	0	1	1	11	053
,	0	1	1	0	0	12	054
-	0	1	1	0	1	13	055
.	0	1	1	1	0	14	056
/	0	1	1	1	1	15	057
0	1	0	0	0	0	16	060
1	1	0	0	0	1	17	061
2	1	0	0	1	0	18	062
3	1	0	0	1	1	19	063
4	1	0	1	0	0	20	064
5	1	0	1	0	1	21	065
6	1	0	1	1	0	22	066
7	1	0	1	1	1	23	067
8	1	1	0	0	0	24	070
9	1	1	0	0	1	25	071
:	1	1	0	1	0	26	072
;	1	1	0	1	1	27	073
<	1	1	1	0	0	28	074
=	1	1	1	0	1	29	075
>	1	1	1	1	0	30	076

Table 3-9. 5355A Program Code Set

NOTE 1

Underlined letters are code letters. Asterisk (*) indicates conditions of 5355A at power up.

FUNCTION	CODE
<u>HOLD</u>	*HD0 (Selects 5345A Sample Rate) HD1 (Sample Rate Hold — Replaces 5345A "E9" T (with HD1 — Same as "J1")
<u>TRIGGER</u> (see Note 3 below)	
<u>INPUT SELECT</u>	IS1 IS2
<u>MANUAL MODE</u>	ML0 ML1
<u>CW/PULSE</u>	CP1 } Note: If 5345A is in REMOTE you must program CP2 } ext/int gate (CP1-int, CP2-ext).
<u>OFFSET MODE</u>	OT0 OT1
<u>OFFSET FREQUENCY ENTRY</u>	OF [FLOATING POINT] CR LF
<u>MANUAL FREQUENCY ENTRY</u>	MF [FLOATING POINT] CR LF
<u>SPECIAL FUNCTION</u> Pulse mode (normal calibration) CW mode (normal FM tolerance) Pulse mode (continuous calibration) CW mode (High FM tolerance)	*SF0 SF1
<u>DIAGNOSTIC DISPLAY</u>	*DD00 DD07 DD01 DD08 DD02 DD09 DD03 DD10 DD04 DD11 DD05 DD12 DD06 etc.
	See Table 3-11
<u>PRESET CONTROLS</u> (Immediate Execute)	*PR (Presets to 5355A power-up condition and triggers one measurement) with the exception that manual and offset frequencies are not initialized. (See Table 3-10)
<u>READ STATUS</u>	

NOTE 2

Program Code R will act as a non-T trigger (see NOTE below for description of non-T triggers) if measurement cycle is not complete or if instrument is out of Hold (in HD0). This condition is indicated when the display starts with a minus (-) sign.

GROUP COMMANDS:

LOCAL LOCKOUT
GO TO LOCAL
DEVICE CLEAR
SELECTED DEVICE CLEAR } See NOTE 3
GROUP EXECUTE TRIGGER } See NOTE 4

NOTE 3

Any HP-IB program code sequence will also trigger the 5355A, however, a non-T trigger will restart a measurement sequence to cause restarts of the 10 measurement calibration. The T trigger will calibrate the first 10 measurements then stop calibration (normal measurement sequence). Some non-T trigger are: N, CP2, DEVICE CLEAR, etc.

NOTE 4

When the 5355A is in Remote and programmed to HOLD (HD1), the Group Execute Trigger acts the same as a T trigger, otherwise it acts the same as Device Clear.

Table 3-10. 5345A Display of 5355A Status

NOTE										
The READ Status (R) code results in the following display of 5355A status on the 5345A display. This status is also available at the 5345A talk output.										
MODES OF OPERATION (Digits listed in either row may be displayed to indicate mode)									HEAD CODE	ERROR CODE OR DIAGNOSTIC MODE
Display	-1	1	1	1	1	1	1	1	0	00 GHz
Indication	CW	PRS	MAN	OFF	SIG	SPEC FUNC	CAL	LLO	5356A	NO ERR
Display	-2	2	0	0	0	0	0	0	1	01 GHz
Indication	PS	HD	NO MAN	NO OFF	NO SIG	NO SPEC FUNC	NO CAL	NO LLO	5356B	See Table 3-11 for 01 through 19
									2 5356B OPT. 001	77 N=0. 5345A "CHECK" switch position error possible.
									4 5356C	99 5345A GATE CONTROL Switch Position Error
									5 5356C Opt. 001	88 5345A "CHECK" switch position error certain, No synthesizer power up test.
									7 No Head	

MODE	DISPLAY
CW	= Continuous Wave 1
PS	= Pulse 2
PRS	= Prescaler 1
HD	= Head 2
MAN	= Manual 1
OFF	= Offset 1
SIG	= Signal 1
SPEC FUNC	= Special Function 1
CAL	= Calibrate 1
LLO	= Local Lockout 1
5356	= Head Code 0-7
NO ERR	= No Error 00

NOTE
The decimal point (.), and GHz annunciator shown above are standard on each status display. The first eight digits show operating modes, the ninth digit shows the type of Frequency Converter Head installed, the tenth and eleventh digits show the error code or diagnostic mode (see Table 3-11). The display contains a minus sign (-) before the first digit to indicate a non-T trigger (see Table 3-9).

Table 3-11. Diagnostic Modes and Special Functions

NOTE				
IN LOCAL operation the diagnostic modes listed below are obtained in numerical sequence by pressing the gold MAN FREQ and blue OFFSET FREQ keys simultaneously. Observe the display for the mode number listed below to determine the diagnostic mode of the 5355A each time the keys are pressed. If diagnostic mode (1-10) is started in one column, the sequence will stay in that column. Press reset on 5345A and set desired operational mode on 5355A to restart sequence. In REMOTE operation, the diagnostic modes are programmed by use of the codes shown in Table 3-9.				
MODE 1 second display each time gold and blue key is pressed	0.4—1.6 GHz INPUT		RF HEAD INPUT	
	Column 1 CW	Column 2 PULSE	Column 3 CW	Column 4 PULSE
DIAGNOSTIC MODES				
====01====	Displays 885.2 MHz self-check frequency (synthesizer set to 1 GHz).		Displays synthesizer frequency to 100 kHz resolution.	
====02====	NA	Displays ratio of measured pulse width to reference pulse width.	Displays calculated N number. Ignore annunciator and round to nearest integer. (-) sign means add IF.	
====03====	NA	• Displays reference pulse width †	Displays (A-B) counts from synthesizer during N determination.	Displays calibration factor. Ignore annunciator.
====04====	NA	• Displays measured pulse width.	Displays (A-B) counts from IF during N determination.	Displays ratio of measured pulse width to reference pulse width.
====05====	Displays prescaler frequency; i.e., input frequency divided by 8.		Displays IF frequency.	• Displays measured pulse width. • Displays reference pulse width. †
====06====	NA	Displays calibration factor. Ignore annunciator.	NA	
====07====		NA	NA	Displays IF during N determination.
====08====		NA	NA	Displays IFa during N determination.
====09====		NA	Manual mode frequency measurements with synthesizer set to frequency entered in offset mode.	
====10====		NA	Displays IF frequency produced by synthesizer set to frequency entered in offset mode.	
SPECIAL FUNCTIONS				
====11====	The integer M in the equation $f_{displayed} = M \cdot f_{measured} \pm B$ may be entered. Go to OFFSET mode; M is the integer located in the second through fifth digits; 0001 to 9999.			
====12====	Measurements made are multiplied by M entered in mode 11. An offset may also be entered.			
====13====	Bypasses 5345A SAMPLE RATE (Manual and Auto)		Bypasses 5345A SAMPLE RATE (Manual and Auto)	
====14====	Disables calibration All Modes (Manual and Auto)		Disables calibration All Modes (Manual and Auto)	
====15====	Both 13 and 14 above		Both 13 and 14 above	
====16-19====	Unassigned (Will reset sequence)			
====1c====	VCO search at low gain. Used to adjust A5R10			
====1e====	VCO search at high gain. Used to adjust A5R7			
NOTES:				
† Reference pulse width is measured during calibration only.				
• Pulse width measurements are displayed by annunciators equivalent to time, as follows:				
	Display	Time		
	kHz	ns		
	MHz	μs		
	GHz	ms		

3-71. SAMPLE PROGRAM

3-72. A sample program for the 5355A is shown below. The 5355A is set to address 08 and the 5345A is set to address 18. The 9825A controller is used with the following equipment installed:

- a. 98210A String-Advanced Programming ROM.
- b. 98213A or 98214A or 98216A General-Extended I/O ROM.
- c. 98034A Interface Card.

```
0: dim A$(25)
1: wrt 718,"12F2E;I1";wait 100
2: wrt 708,"PRCP2HD1";wait 100
3: wrt 703,"R";red 718,A$;prt A$
4: wrt 708,"HD0"
5: red 718,A$;prt A$
6: end
*982
```

```
-2.2001000000E+9
2.997629094E+9
```

3-73. This printout shows a program for reading 5355A status ("R") to be displayed on the 5345A and sent to the 9825A for display and listing. The status is listed at the end of the program. Then a pulse measurement is made and printed out below the status printout.

PERFORMANCE CHECK

SECTION IV PERFORMANCE TESTS

4-1. INTRODUCTION

4-2. The procedures in this section test the electrical performance of the 5355A and the associated 5356A, B, or C using the specifications listed in *Table 1-1* as a standard. To test the equipment to the complete performance specifications, all of the tests in this section should be performed. To merely verify that the 5355/5356 is basically operating properly, only the tests listed in paragraph 4-8 need to be performed (operational verification).

4-3. EQUIPMENT REQUIRED

4-4. Equipment required for performance testing is listed in *Table 1-3*. Any equipment that satisfies the critical specification given in the table may be substituted for the recommended model.

4-5. TEST RECORD

4-6. Results of the operational verification or performance tests may be recorded in *Tables 4-3* or *4-4*, respectively, at the end of this section.

4-7. OPERATIONAL VERIFICATION

4-8. To verify proper operation of the equipment, perform the tests listed below. These tests can be performed to provide a high degree of confidence that the equipment is operating properly without conducting the complete performance test. The operational verification should be used for incoming QA, routine maintenance, and after instrument repair.

Paragraph	Test
4-11.	5355A Input Sensitivity Test, CW Mode
4-12.	5355A Input Sensitivity Test, Pulsed RF Mode
4-18.	5355A/5356 Input Sensitivity Tests, CW Mode
4-19.	Test 1. 1.5-12.4 GHz
4-20.	Test 2. 12.4-18 GHz
4-21.	Test 3. 18-26.5 GHz
4-22.	Test 4. 26.5-40 GHz
4-23.	5355A/5356 Input Sensitivity Test, Pulsed RF Mode
4-24.	Test 1. 1.5-12.4 GHz
4-25.	Test 2. 12.4-18 GHz
4-26.	Test 3. 18-26.5 GHz
4-27.	Test 4. 26.5-40 GHz
4-49.	HP-IB Verification

4-9. PERFORMANCE TESTS

4-10. The performance tests consist of all the tests given in this section as listed below. These tests verify the specifications in Table 1-1. All tests can be performed without access to the interior of the instrument.

Paragraph	Test
4-11.	5355A (.4-1.6 GHz) Input Sensitivity Test, CW Mode
4-12.	5355A (.4-1.6 GHz) Input Sensitivity Test, Pulsed RF Mode
4-15.	5355A (.4-1.6 GHz) Input Tests: Pulse Width, Pulse Repetition Frequency and Input Sensitivity (with <200 ns Pulse Width)
4-16.	Test 1. 2 MHz PRF with 100 ns Pulse Width, Input Sensitivity: -10 dBm for Pulse Widths <200 ns
4-17.	Test 2. 100 Hz PRF with 10 ms Pulse Width (minimum off time of 400 ns)
4-18.	5355A/5356 Input Sensitivity Tests, CW Mode
4-19.	Test 1. 1.5-12.4 GHz
4-20.	Test 2. 12.4-18 GHz
4-21.	Test 3. 18-26.5 GHz
4-22.	Test 4. 26.5-40 GHz
4-23.	5355A/5356 Input Sensitivity Tests, Pulsed RF Mode
4-24.	Test 1. 1.5-12.4 GHz
4-25.	Test 2. 12.4-18 GHz
4-26.	Test 3. 18-26.5 GHz
4-27.	Test 4. 26.5-40 GHz
4-28.	5355A/5356 Input Tests: Pulse Width, Pulse Repetition Frequency, and Input Sensitivity with <200 ns Pulse Width
4-29.	Test 1, Auto Mode: 2 MHz PRF with 100 ns Pulse Width, Input Sensitivity
4-30.	Test 2, Manual Mode: 2 MHz PRF with 60 ns Pulse Width, Input Sensitivity
4-31.	Test 3, Manual Mode: 50 Hz PRF with 20 ms Pulse Width (with minimum off time of 400 ns)
4-32.	Test 4, Auto Mode: 50 Hz PRF with 20 ms Pulse Width (with minimum off time of 400 ns)
4-33.	5355A (.4-1.6 GHz) Maximum Input Test
4-34.	5355A/5356 Maximum Input Tests
4-35.	Test 1. 1.5-18 GHz
4-36.	Test 2. 18-26.5 GHz
4-37.	5355A/5356 FM Tolerance Test
4-38.	5355A (.4-1.6 GHz) Accuracy Test, CW Mode
4-39.	5355A (.4-1.6 GHz) Accuracy Test, Pulsed RF Mode
4-40.	5355A/5356 Accuracy Test, CW Mode
4-41.	5355A/5356 Accuracy Test, Pulsed RF Mode
4-42.	Rear Panel Output Tests: Gate Out, Pulse Out, IF Out
4-43.	Gate Out Test
4-44.	Pulse Out Test
4-45.	IF Out Test
4-49.	HP-IB Verification

4-11. 5355A (.4-1.6 GHz) Input Sensitivity Test, CW Mode

Specification: Sensitivity = -15 dBm for frequencies from .4 to 1.6 GHz.

Description: The 5355A is set to the lower frequency (prescaler) range and a signal at the rated sensitivity is applied to the BNC input. The frequency is slowly swept up to 1.6 GHz at a constant level while the 5345A display is checked for the proper count.

Test Setup: Figure 4-1

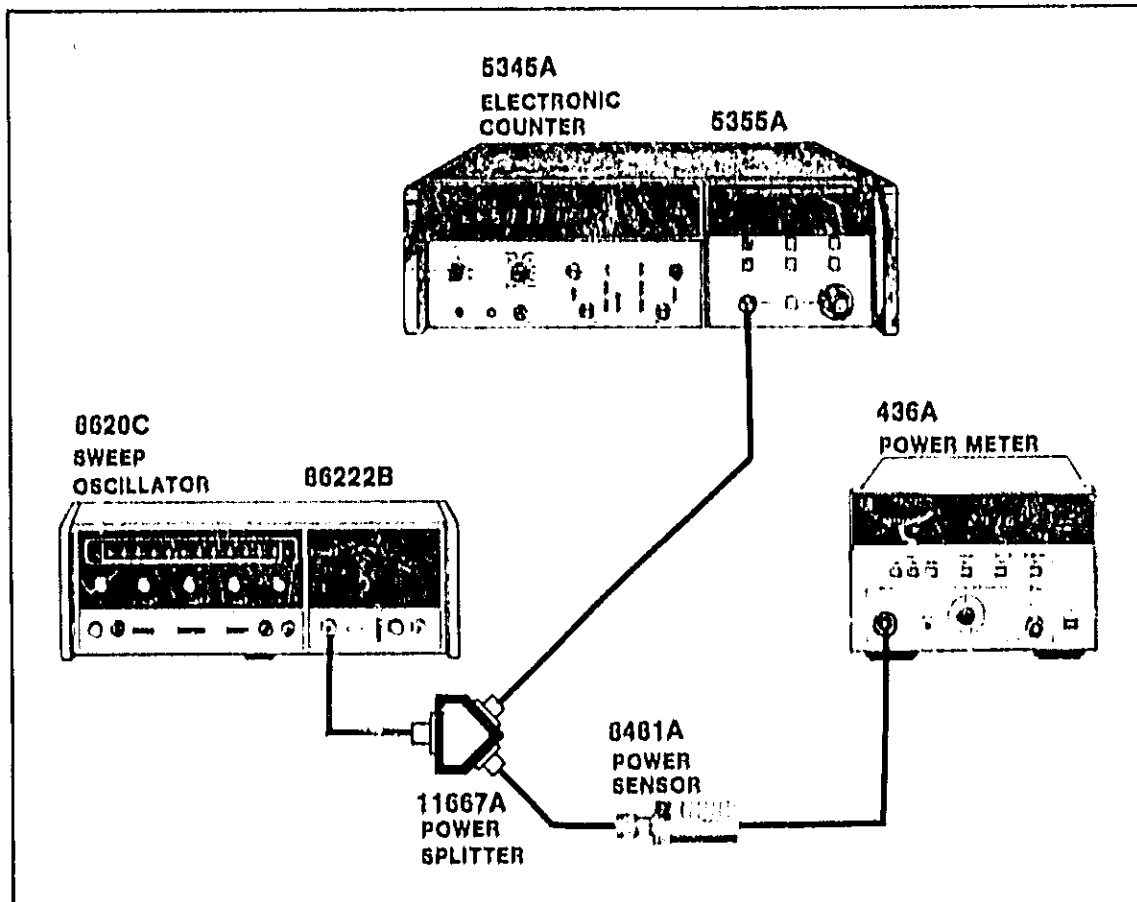


Figure 4-1. 5355A (1.4-1.6 GHz) Input Sensitivity Test, CW Mode Setup

- Turn on 5345A power. Push INPUT SELECT key on 5355A to select the prescaler input.
- Set 436A power meter for auto range (RANGE HOLD button out) and dBm mode.
- Set the 86222B for INT leveling and adjust the output power level for a 436A reading of -15 dBm.
- Vary the 8620C frequency over the range of 400 MHz to 1.6 GHz and verify that the 5355A counts properly. Use the 436A to verify input power.
- Record results on operational verification record (Table 4-3) or on performance test record (Table 4-4), as applicable.

Model 5355A
Performance Tests

4-12. 5355A (.4-1.6 GHz) Input Sensitivity Test, Pulsed RF Mode

Specification: Sensitivity = -15 dBm for frequencies from .4 to 1.6 GHz.

Description: The 5355A is set to the lower frequency (prescaler) range and the pulse mode. A pulsed RF signal at the rated sensitivity is then applied to the BNC Input. The frequency is slowly swept up to 1.6 GHz at a constant level while the 5345A display is checked for the proper count.

Test Setup: Figure 4-2.

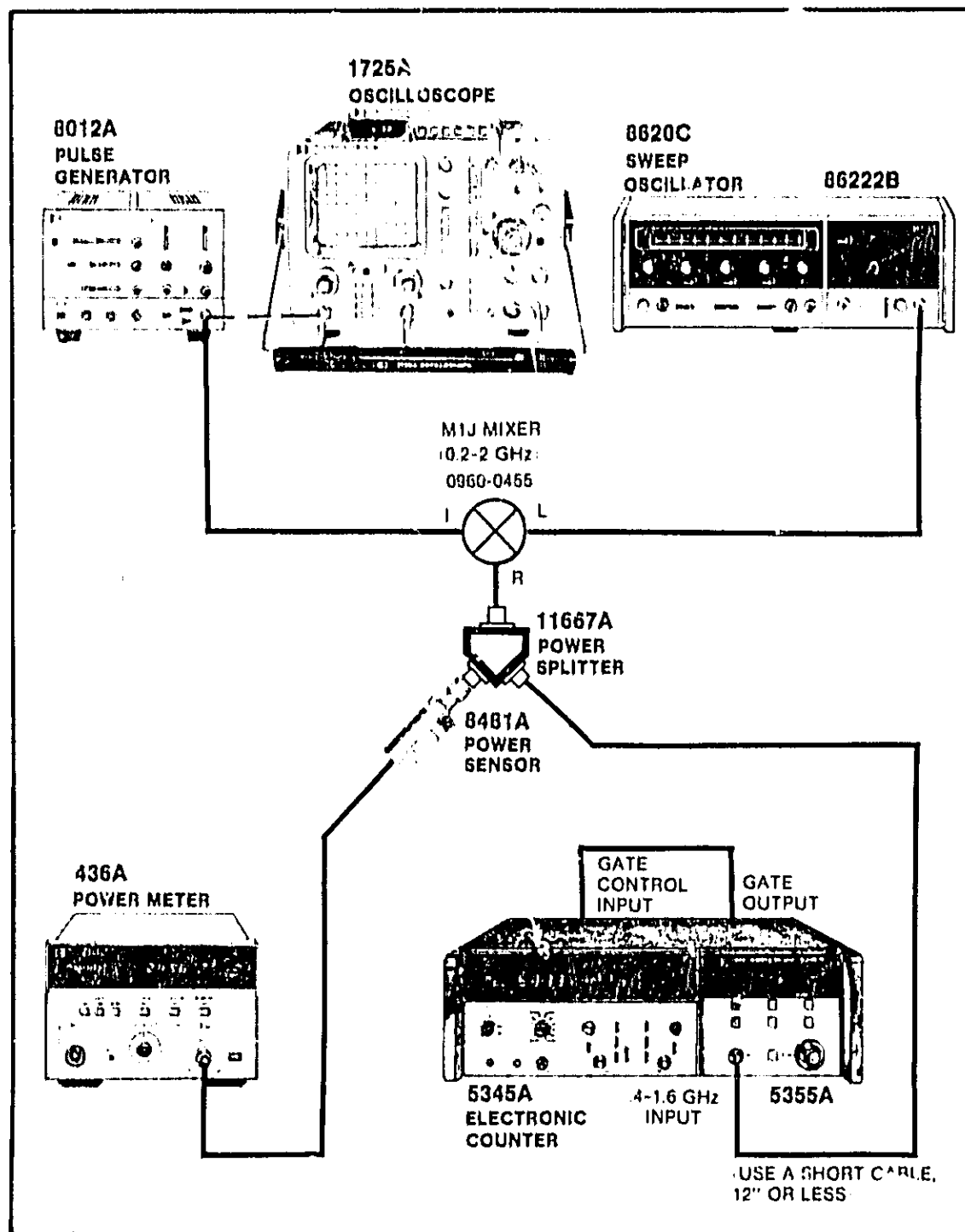
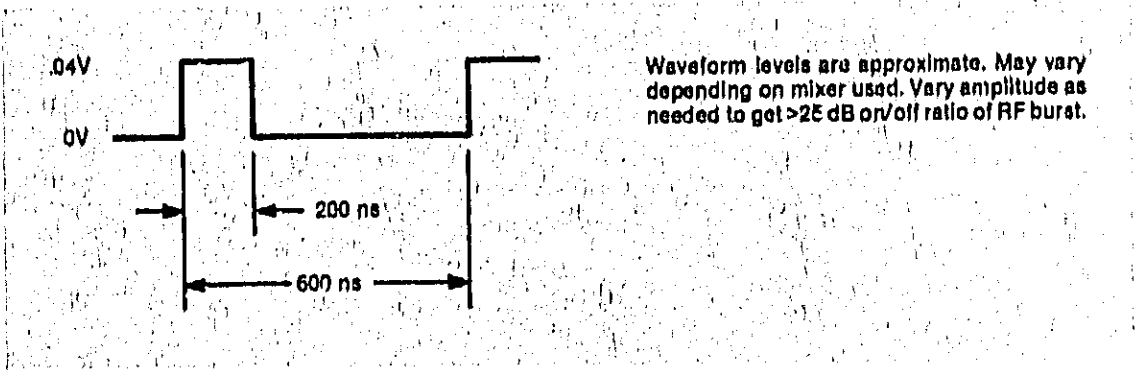


Figure 4-2. 5355A (.4-1.6 GHz) Input Sensitivity Test, Pulsed RF Mode Setup

a. 8012A Settings

PULSE PERIOD	20 ns-1 μs
DELAY	35 ns-1 μs
PULSE WIDTH SWITCH	10 ns-1 μs
PULSE WIDTH VERNIER	200 ns
TRANSITION TIME	5 ns--0.5 μs
LEADING AND TRAILING EDGES	ccw
AMPLITUDE SWITCH	0.2 to 0.5V or 0.5 to 1V
AMPLITUDE VERNIER	Vary amplitude for best RF burst
OFFSET SWITCH	OFF
PULSE POLARITY	+

- b. The pulse signal can be observed on an oscilloscope using a 50-ohm termination for final adjustment. The waveform should conform to the figure below.



- c. Turn on 5345A power. Push INPUT SELECT key on 5355A to select prescaler input and push PULSE to select pulsed RF mode.
- d. Set 436A power meter for auto range (RANGE HOLD button out) and dBm mode.
- e. Set the 86222B for INT leveling and adjust the output power level for a 436A reading of -19.8 dBm, which is equivalent to -15 dBm CW. Equation is:

$$\text{Power Meter Reading} = \text{Counter Input Power} + 10 \log \frac{\text{Pulse Width}}{\text{PRI}},$$

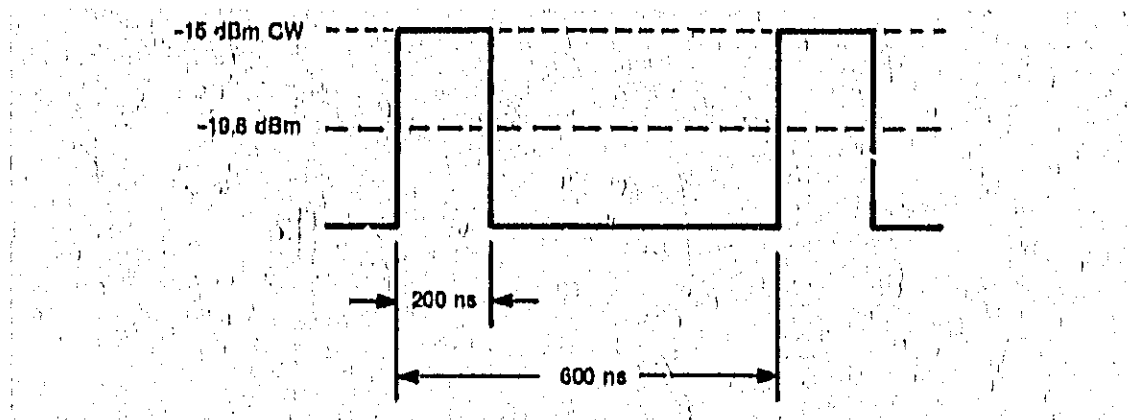
$$\text{e.g., } -19.8 \text{ dBm} = -15 \text{ dBm} + 10 \log 0.33 = (-15 \text{ dBm}) + (-4.8 \text{ dBm})$$

See paragraph 4-13 for explanation.

- f. Vary the 8620C frequency over the range of 400 MHz to 1.6 GHz and verify that the 5355A counts properly. Use the 436A to verify input power.
- g. Record results on operational verification record (Table 4-3) or on performance test record (Table 4-4), as applicable.

4-13. PULSED RF AMPLITUDE SETTINGS EXAMPLE

4-14. The following waveform shows the relationship between peak pulse power and the power meter reading.



For pulsed RF having the same peak level as the CW level, a power meter will average the pulse level and display a lower reading. To arrive at the required peak pulse power, this must be taken into account when setting up the source power level. The relationship is shown below:

$$\text{Power Meter Reading} = \text{Required Input Power} + 10 \log \frac{\text{Pulse Width}}{\text{Pulse Rep Interval}}$$

In the example above, it works out thus:

$$\begin{aligned} \text{Power Meter Reading} &= -15 \text{ dBm} + 10 \log \frac{200}{600} \\ &= (-15 \text{ dBm}) + (-4.8 \text{ dB}) \\ &= -19.8 \text{ dBm} \end{aligned}$$

-19.8 dBm is what the power meter will read if the above signal conditions are used.

4-15. 5355A (.4-1.6 GHz) Input Tests: Pulse Width, Pulse Repetition Frequency, and Input Sensitivity with <200 ns Pulse Width

Specifications:

Pulse Width

Minimum 100 ns*

Maximum 10 ms*

Pulse Repetition Frequency

Minimum 100 Hz*

Maximum 2 MHz*

*(Minimum off time is 400 ns)

Input Sensitivity:

-10 dBm for pulse widths <200 ns

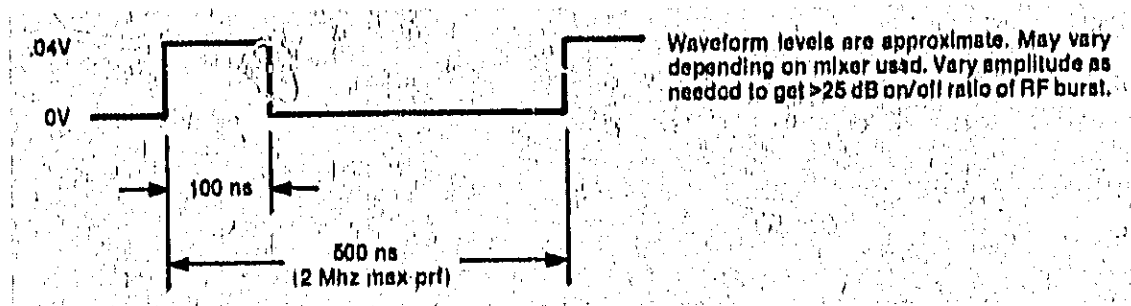
Description: The 5355A is set to the lower frequency (prescaler) range and pulse mode. A pulsed RF signal is then applied to the BNC input. The modulating waveform is varied in two steps to provide the limits specified above:

- 2 MHz PRF with 100 ns pulse width, input sensitivity with <200 ns pulse width.
- 100 Hz PRF with 10 ms pulse width (minimum off time of 400 ns).

Setup: Use equipment setup shown in Figure 4-2 and 8012A settings as described in paragraph 4-12a. The 8012A output can be observed on an oscilloscope for final adjustment.

4-16. TEST 1. 2 MHz PRF WITH 100 ns PULSE WIDTH, INPUT SENSITIVITY: -10 dBm FOR PULSE WIDTHS <200 ns

- a. The waveform should conform to the figure below.



- b. Turn on 5345A power. Push INPUT SELECT key on 5355A to select prescaler input.
c. Set 436A power meter for auto range (RANGE HOLD button out) and dBm mode.
d. Set the 8620C to 1 GHz and set the 86222B for INT leveling.
e. Adjust the output power level for a 436A reading of -17 dBm.

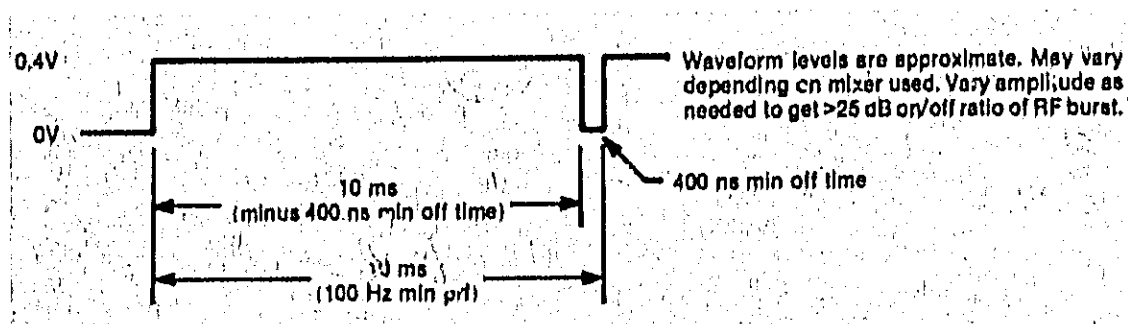
$$-10 \text{ dBm} + 10 \log \frac{100 \text{ ns}}{500 \text{ ns}}$$

See paragraph 4-13 for explanation.

- f. Push 5355A PULSE key to select pulsed RF mode and ensure the 5355A counts properly. Record results on operational verification record (Table 4-3) or on performance test record (Table 4-4) and then continue with Test 2.

4-17. TEST 2. 100 Hz PRF WITH 10 ms PULSE WIDTH (MINIMUM OFF TIME OF 400 ns)

- a. **Setup:** Use the same setup (Figure 4-2) but change the waveform to conform to the figure below. This can be done by setting the 8012A to positive polarity and adjusting the negative-going pulse for 400 ns. Then set the 8012A PULSE PERIOD to 10 ms - 1 s. Connect the pulse generator to the 5345A and perform a T.I. + to - measurement while varying the PULSE PERIOD VERNIER for a 10 ms display.



- b. Set 5345A to a 1 μ s gate time and connect setup as before. Power meter should read -10 dBm.
c. The 5355A should correctly count the 1 GHz signal. Record results on operational verification record (Table 4-3) or on performance test record (Table 4-4), as applicable.

4-10. 5355A/5356 Input Sensitivity Tests, CW Mode

Specifications: See Table 4-1.

Description: The 5355A is set to the higher frequency (converter head) range and a signal at the rated sensitivity (Table 4-1) is applied to the converter head (5356A, 5356B, or 5356C). The frequency is slowly swept through the appropriate range at a constant level while the 5345A display is checked for the proper count. A separate test is provided for each of the four ranges of frequencies.

4-19. TEST 1. 1.5—12.4 GHz. See Table 4-1 specifications for head under test.

Setup: Figure 4-3.

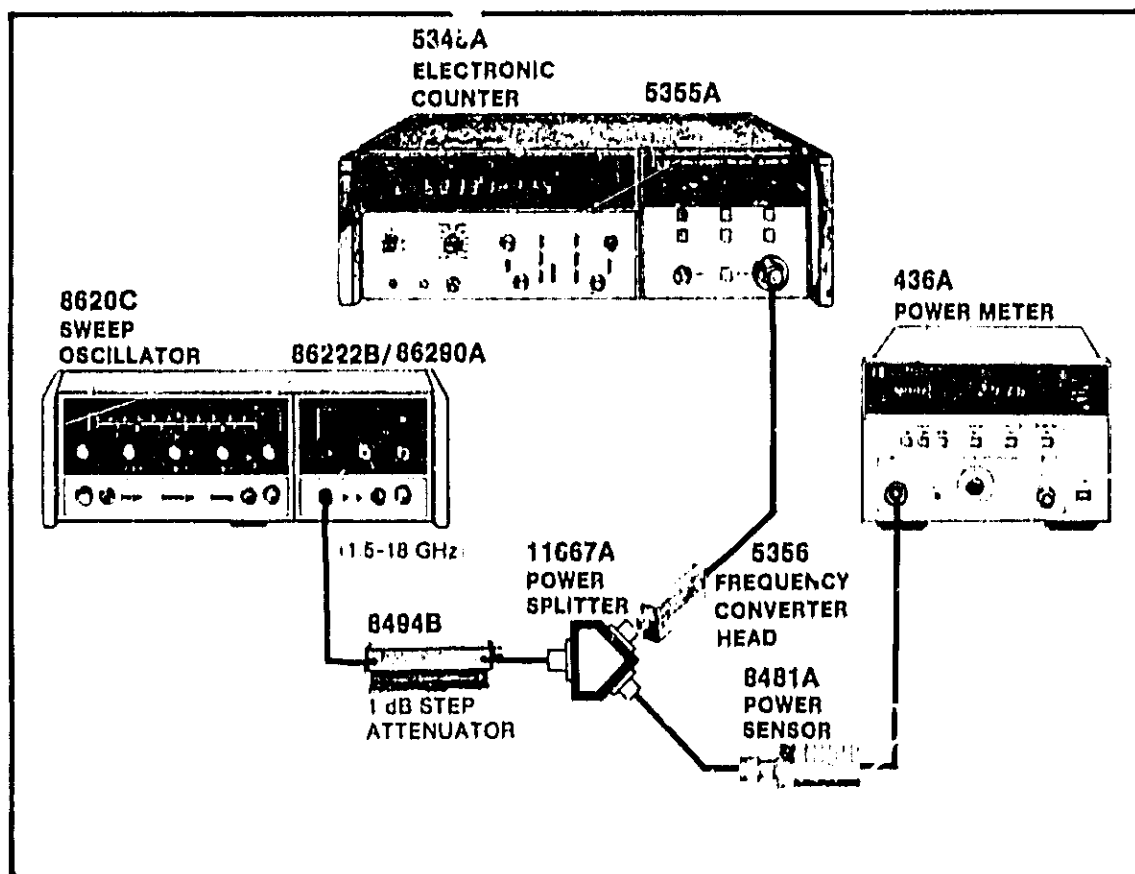


Figure 4-3. 5355A/5356 Input Sensitivity Test, CW Mode 1.5—18 GHz Setup

- Turn on 5345A power.
- Set 436A power meter for auto range (RANGE HOLD button out) and dBm mode.
- Set the 86222B/86290A for INT leveling and adjust the output power level for a 436A reading per Table 4-1.
- Vary the 8620C frequency over the range of 1.5 to 12.4 GHz and verify that the 5355A counts properly. Use the 436A to verify input power.
- Record results on operational verification record (Table 4-3) or on performance test record (Table 4-4), as applicable.

Table 4-1. Specifications for HP Models 5356A/B/C Frequency Converter Heads

	5356A	5356B	5356B Option 001	5356C	5356C Option 001
Sensitivity:					
1.5—12.4 GHz	-20 dBm	-20 dBm	—	-25 dBm	—
12.4—18 GHz	-15 dBm	-15 dBm	—	-20 dBm	—
18—26.5 GHz	—	-15 dBm	-15 dBm	-20 dBm	—
26.5—34 GHz	—	—	—	-15 dBm	-15 dBm
34—40GHz	—	—	—	-10 dBm	-10 dBm
NOTE: For pulse widths <200 ns reduce sensitivity by 5dB.					

- 4-20. TEST 2, 12.4—18 GHz. See Table 4-1 specifications for head under test.
- a. **Setup:** Use same setup (Figure 4-3) but adjust the power level of the 86290A for a 436A reading per Table 4-1.
 - b. Vary the 8620C frequency over the range of 12.4 to 18 GHz and verify that the 5355A counts properly. Use the 436A to verify input power.
 - c. Record results on operational verification record (Table 4-3) or on performance test record (Table 4-4), as applicable.

4-21. TEST 3, 18—26.5 GHz. See Table 4-1 specifications for head under test.

Setup: Figure 4-4.

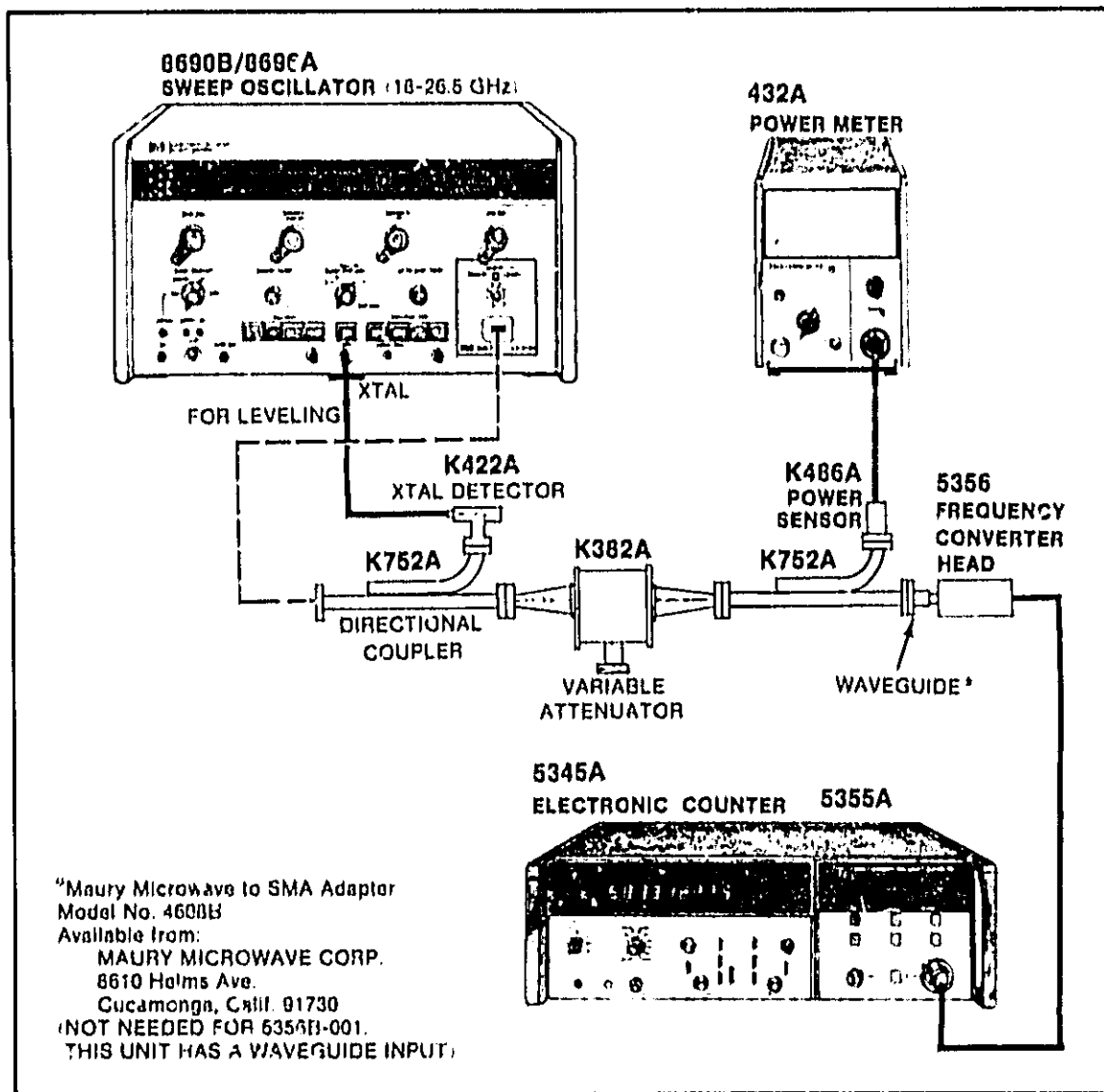


Figure 4-4. 5355A/5356 Input Sensitivity Test, CW Mode, 18—26.5 GHz Setup

- Set the 8690B/8696A for a CW signal and adjust power level using 8696A and K382A variable attenuator for a 432A reading per Table 4-1.
- Vary the 8690B frequency over the range of 18 to 26.5 GHz and verify that the 5355A counts properly. Use the 432A to verify input power.
- Record results on operational verification record (Table 4-3) or on performance test record (Table 4-4).

4-22. TEST 4, 26.5—40 GHz. See Table 4-1 specifications for head under test.

Setup: Figure 4-5.

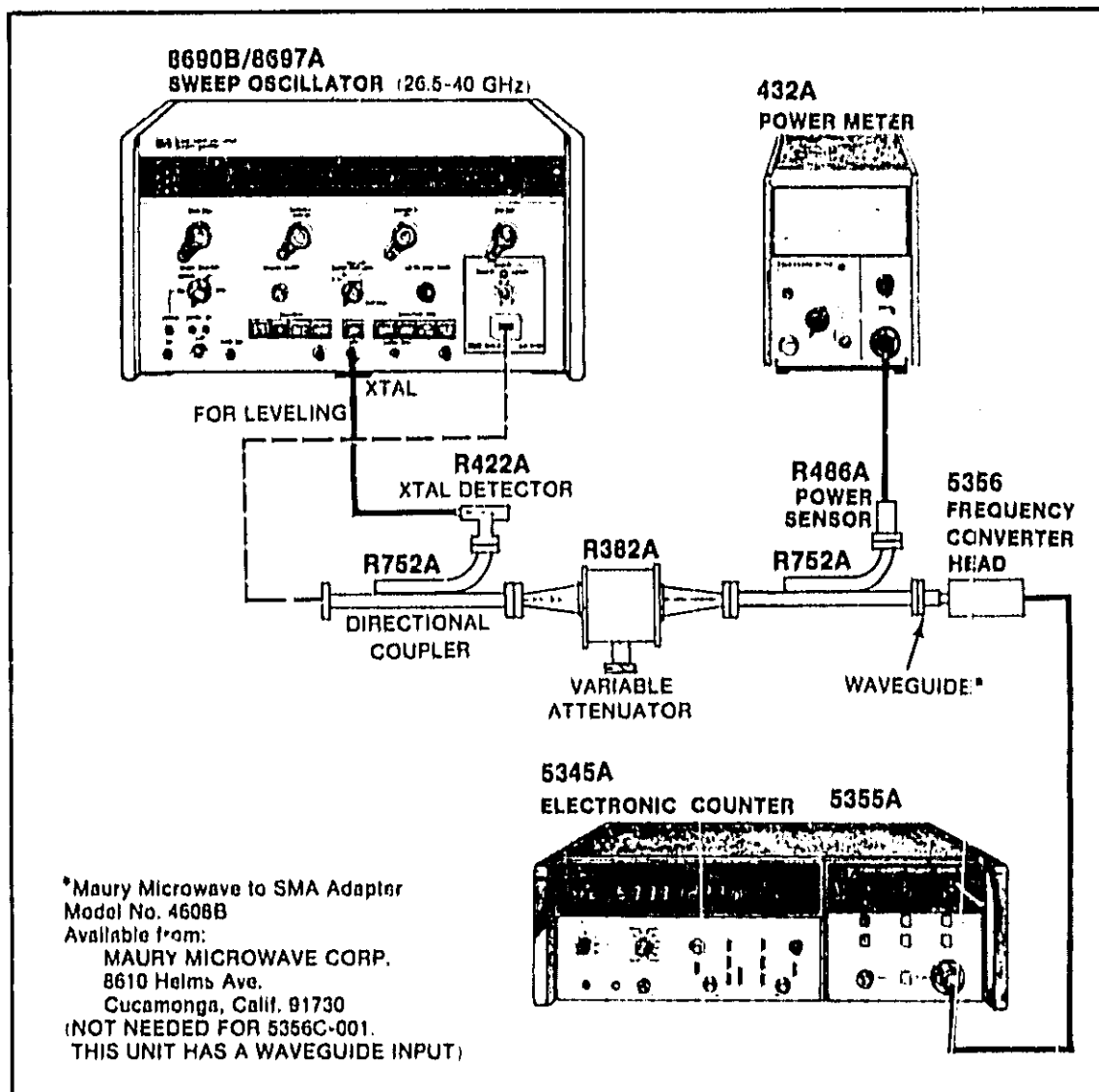


Figure 4-5. 5355A/5356 Input Sensitivity Test, CW Mode, 26.5—40 GHz Setup

- Set the 8690B/8697A for a CW signal and adjust the power level using the 8697A and R382 variable attenuator for a 432A reading per Table 4-1.
- Vary the 8690B frequency over the range of 26.5 to 40 GHz, and verify that the 5355A counts properly. Use the 432A to verify input power.
- Record results on operational verification record (Table 4-3) or on performance test record (Table 4-4), as applicable.

4-23. 5355A/5356 Input Sensitivity Test, Pulsed RF Mode

Specification: See Table 4-1.

Description: The 5355A is set to the higher frequency (converter head) range and the pulse mode. A pulsed RF signal at the rated sensitivity is then applied to the converter head. The frequency is slowly swept through the appropriate range at a constant level while the 5345A display is checked for the proper count.

4-24. TEST 1, 1.5–12.4 GHz. See Table 4-1 specifications for head under test.

Setup: Figure 4-6.

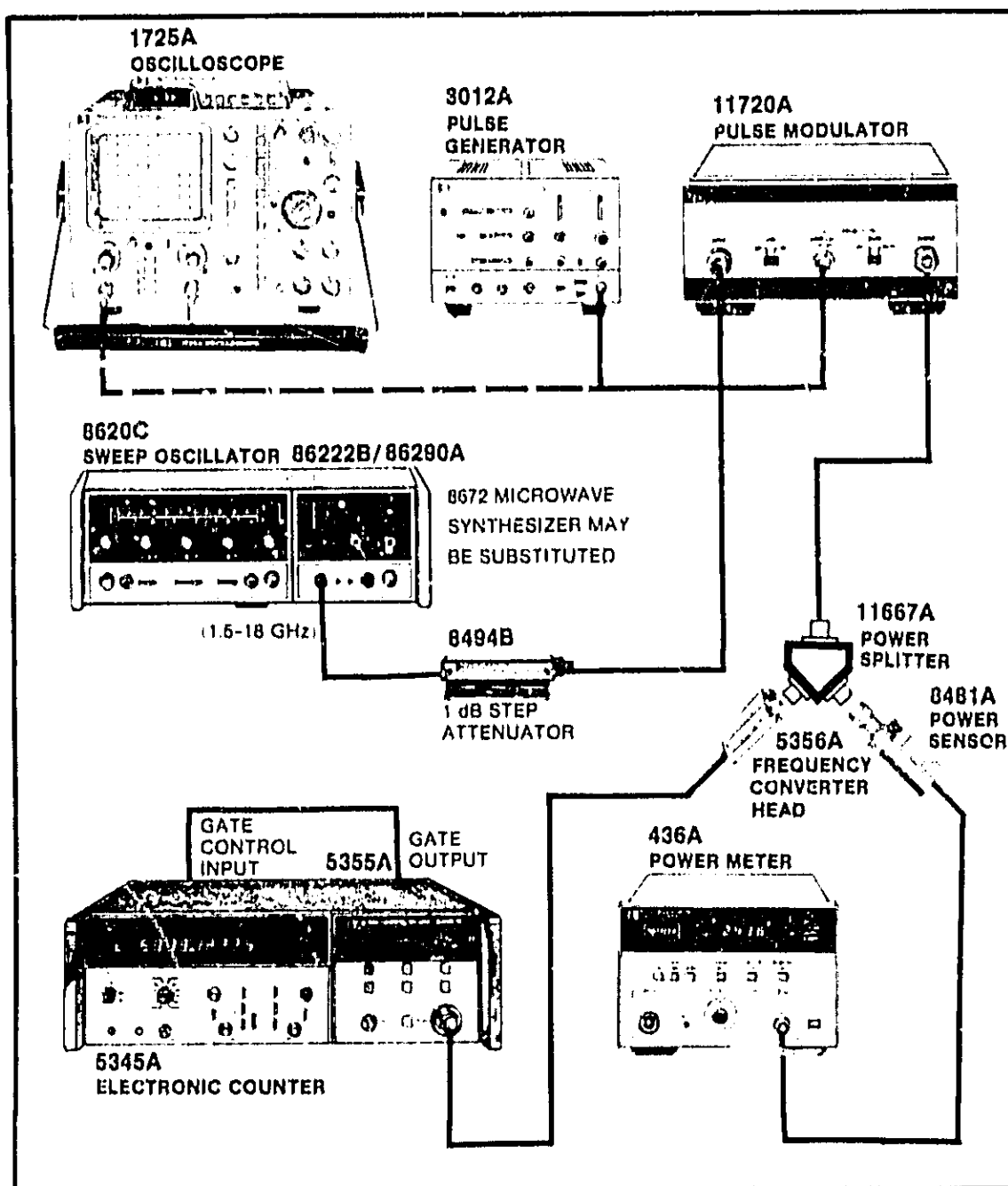
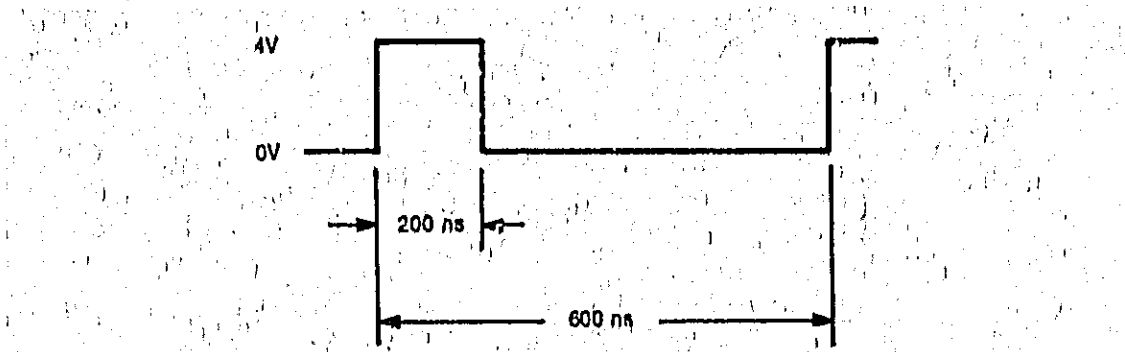


Figure 4-6. 5355A/5356 Input Sensitivity Test, Pulse Mode, 1.5–18 GHz Setup

8012A Setup:

PULSE PERIOD	20 ns-1 μ s	LEADING AND TRAILING EDGE	CLW
DELAY	35 ns-1 μ s	AMPLITUDE SWITCH	2.0-5.0V
PULSE WIDTH SWITCH	10 ns-1 μ s	AMPLITUDE VERNIER	4.0V
PULSE WIDTH VERNIER	20 ns	OFFSET	OFF
TRANSITION TIME	5 ns-0.5 μ s	PULSE POLARITY	+

- Observe the pulse signal on the oscilloscope (as shown by dotted line in Figure 4-6) using a 50-ohm termination for final adjustment. The waveform should conform to the figure below.



- Turn on 5345A and push PULSE key on 5355A to select pulsed RF mode.
- Set 436A power meter for auto range (RANGE HOLD button out) and dBm mode.
- Set the 86222B/86290A for INT leveling and the output power level for a 436A reading per Table 4-1.

$$\text{Plus } 10 \log \frac{200 \text{ ns}}{600 \text{ ns}} \text{ to account for duty cycle.}$$

$$10 \log \frac{200 \text{ ns}}{600 \text{ ns}} = -4.77 \text{ dB.}$$

See paragraph 4-13 for explanation.

- Vary the 8620C frequency over the range of 1.5 to 12.4 GHz and verify that the 5355A counts properly. Use the 436A to verify input power.
- Record results on operational verification record (Table 4-3) or on performance test record (Table 4-4), as applicable.

4-25. TEST 2. 12.4—18 GHz. See Table 4-1 specifications for head under test.

Setup: Use setup in Figure 4-6 but adjust the power level of the 86290A for a 436A reading per Table 4-1.

$$\text{Plus } 10 \log \frac{200 \text{ ns}}{600 \text{ ns}} \text{ to account for duty cycle.}$$

$$10 \log \frac{200 \text{ ns}}{600 \text{ ns}} = -4.77 \text{ dB.}$$

See paragraph 4-13 for explanation.

- Vary the 8620C frequency over the range of 12.4 to 18 GHz and verify that the 5355A counts properly. Use the 436A to verify input power.
- Record results on operational verification record (Table 4-3) or on performance test record (Table 4-4), as applicable.

Model 5355A
Performance Tests

4-26. TEST 3. 10—26.5 GHz. See Table 4-1 specifications for head under test.

Setup: Figure 4-7.

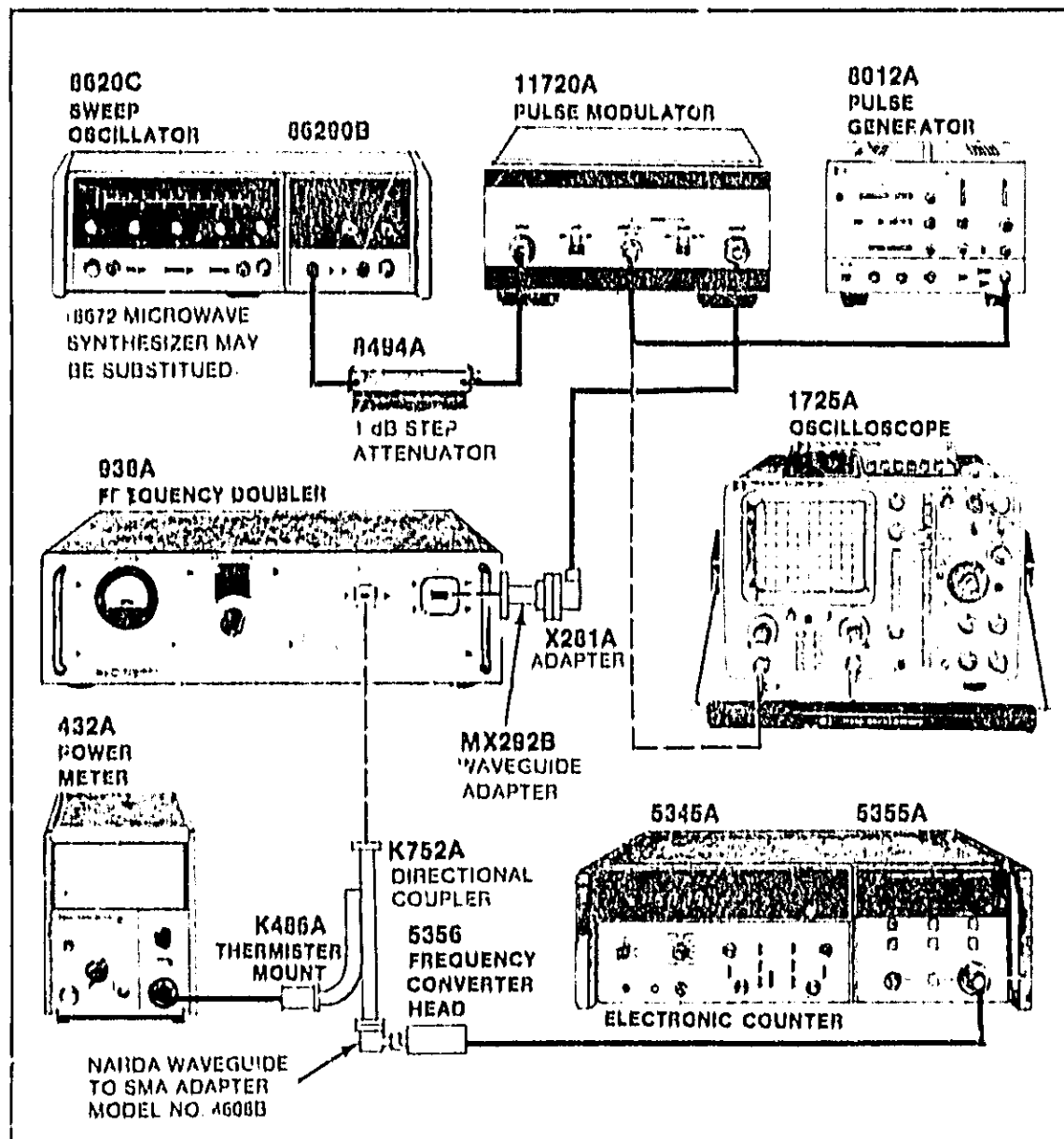


Figure 4-7. 5355A/5356 Input Sensitivity Test, Pulse Mode, 10—26.5 GHz Setup

- Using the 1725 oscilloscope as an adjustment aid, set up the 8012 pulse output as shown in paragraph 4-24a.
- Using the level controls on the 86290A and the 938A doubler, and the 1 dB step attenuator, adjust for a 432A reading per Table 4-1, -4.77 dB. (-4.77 dB is to account for pulse duty cycle.) See paragraph 4-13 for explanation.
- Vary the 8620C frequency over the range of 9 to 13.25 GHz, (938 doubler will output 18 to 26.5 GHz) and verify that the 5355A counts properly. Use the 432A to verify input power.
- Record results on operational verification record (Table 4-3) or on performance test record (Table 4-4).

4-27. TEST 4. 26.5—40 GHz. See Table 4-1 specifications for head under test.

Setup: Figure 4-8.

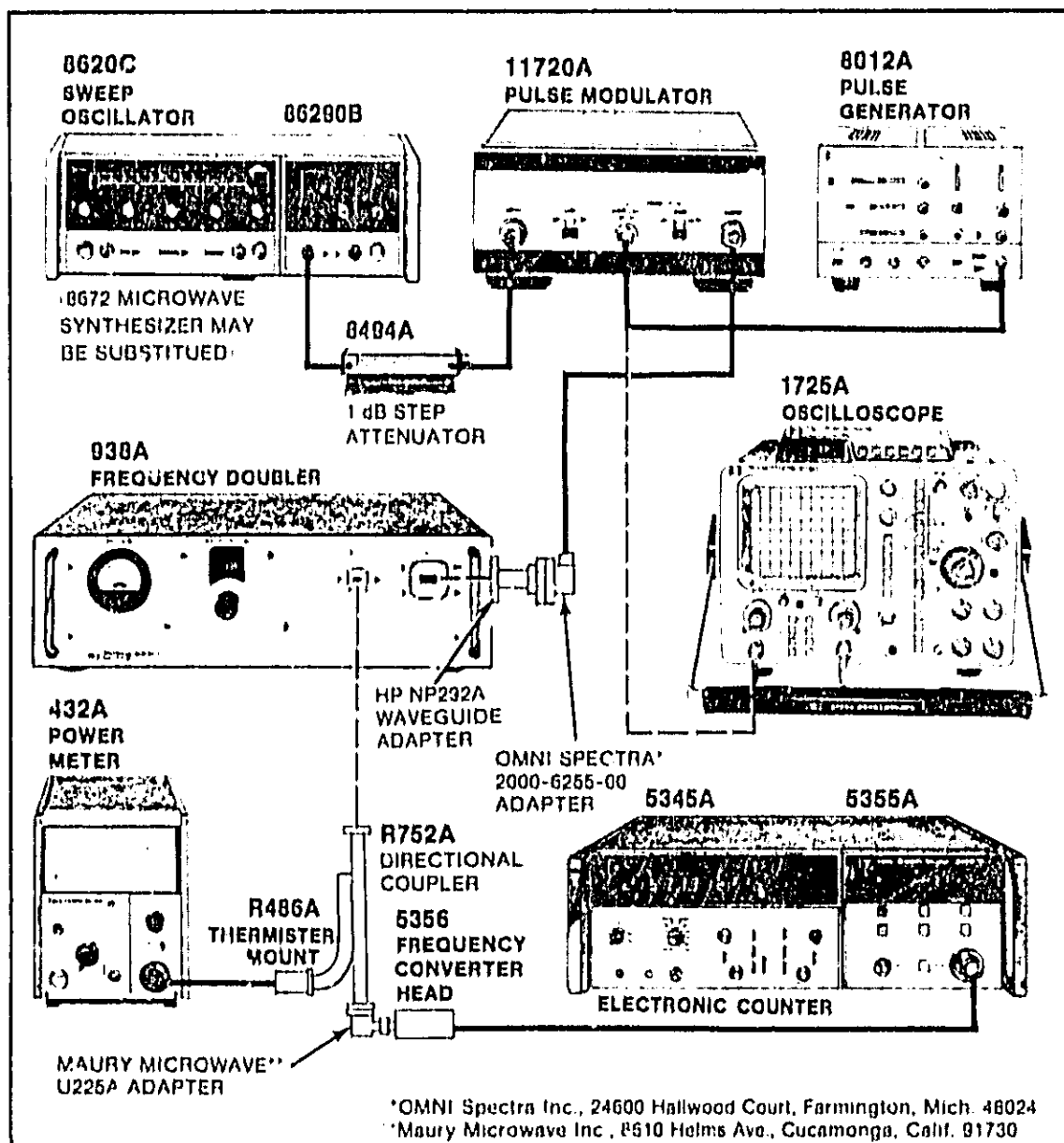


Figure 4-8. 5355A/5356 Input Sensitivity Test. Pulse Mode, 26.5—40 GHz

- Using the 1725 oscilloscope as an adjustment aid, set up the 8012 pulse output as shown in paragraph 4-24a.
- Using the level controls on the 86290, the 940A Doubler, and the 1 dB step attenuator, adjust for a 432A reading per Table 4-1, -4.77 dB (4.77 dB is to account for pulse duty cycle). See paragraph 4-13 for explanation.
- Vary the 8620C frequency over the range of 13.25 to 18 GHz, (940A doubler will output 26.5 to 36 GHz) and verify that the 5355A counts properly. Use the 432A to verify input power. Note specification change at 34 GHz.
- Record results on operational verification record (Table 4-3) or on performance test record (Table 4-4), as applicable.

4-28. 5355A/5356 Input Tests: Pulse Width, Pulse Repetition Frequency, and Input Sensitivity with <200 ns Pulse Width

Specifications:

	AUTO MODE	MANUAL MODE
Pulse Width		
Minimum	100 ns*	60 ns*
Maximum	20 ms*	20 ms*
Pulse Repetition Frequency		
Minimum	50 Hz*	50 Hz*
Maximum	2 MHz*	2 MHz*

(*Minimum off time is 400 ns)

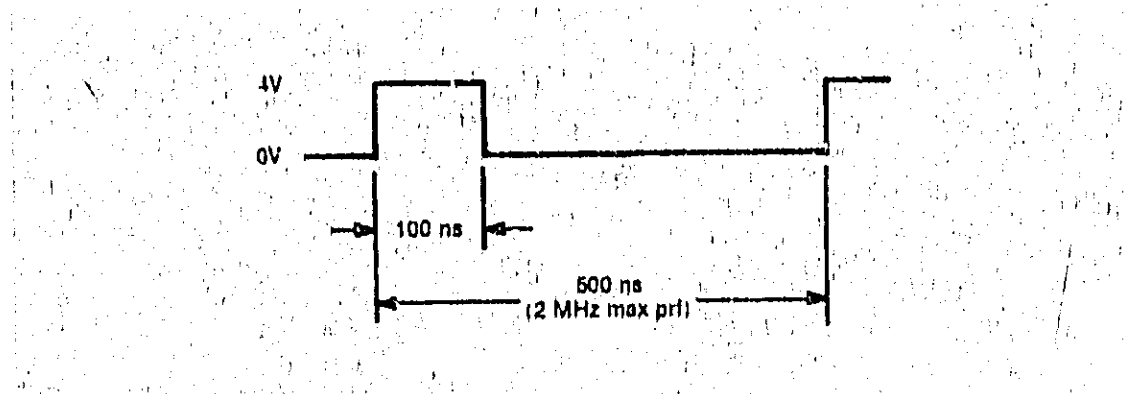
Sensitivity: 5 dB below normal specification for pulse widths <200 ns.

Description: The 5355A is set to the high frequency (converter head) range and pulse mode. A pulsed RF signal is then applied to the converter head input. The modulating waveform is varied in three steps to provide the limits specified above while the 5355A is changed from AUTO to MANUAL mode.

Setup: Use same equipment setup and 8012A setup as described in paragraph 4-24. The 8012A output can be observed on an oscilloscope for final adjustment.

4-29. TEST 1, AUTO MODE: 2 MHz PRF WITH 100 ns PULSE WIDTH, INPUT SENSITIVITY
(See Table 4-1 specifications for head under test. For pulse widths <200 ns, subtract 5 dB from CW specification.)

- The 8012A output should conform to the figure below.



- Turn on 5345A power.
- Set 436A power meter for auto range (RANGE HOLD button out) and dBm mode.
- Set the 8620C to 10 GHz and adjust the output power level for a 436A reading per specifications,

$$\text{plus } 10 \log \frac{100 \text{ ns}}{500 \text{ ns}} ,$$

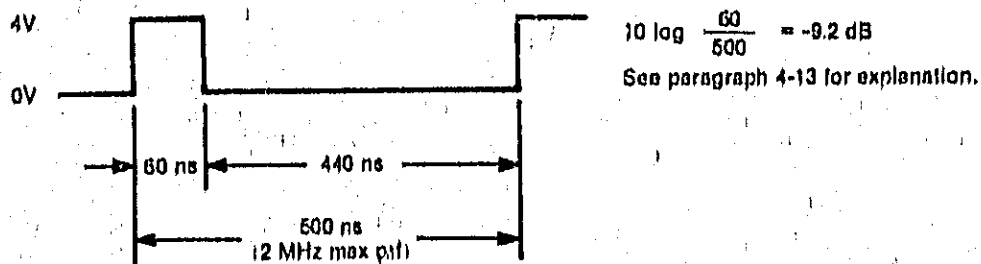
$$10 \log \frac{100 \text{ ns}}{500 \text{ ns}} = -7 \text{ dB.}$$

See paragraph 4-13 for explanation.

- Push the 5355A pulse key to select pulsed RF mode and ensure the 5355A counts properly. Record results on performance test record (Table 4-4) and then continue with Test 2.

4-30. TEST 2, MANUAL MODE: 2 MHz PRF WITH 60 ns PULSE WIDTH, INPUT SENSITIVITY: See Table 4-1 specifications for head under test. (For pulse widths <200 ns, subtract 5 dB from CW specification)

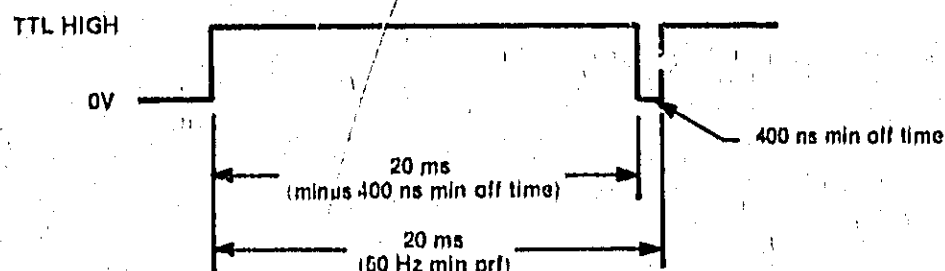
- a. Use the same setup as in paragraph 4-24 but change the waveform to conform to the figure below.



- b. Power meter should read specification value -9.2 dB.
- c. Push the 5355A MAN FREQ key and use the UP/DN keys to give a 5345A display of 10.0 GHz.
- d. Push the MAN FREQ key again to exit the data entry mode. Recheck source frequency at 10 GHz.
- e. Push the MANUAL key to enter the manual mode and ensure the 5355A counts properly. Record results on performance test record (*Table 4-4*) and then continue with Test 3.

4-31. TEST 3, MANUAL MODE: 50 Hz PRF WITH 20 μ s PULSE WIDTH (WITH MINIMUM OFF TIME OF 400 ns)

- a. Use the same setup as paragraph 4-30, but change the waveform to conform to the figure below. This can be done by setting the 8012A to - polarity, OFFSET switch to ON, OFFSET control to maximum CW, and using AMPLITUDE control to set bottom of waveform to 0V. Vary the PULSE WIDTH VERNIER for a negative-going pulse of 400 ns. Then change the PULSE PERIOD switch to the 10m -1 position. Connect the pulse generator to the 5345A and perform a frequency measurement while varying the PULSE PERIOD VERNIER for a 50 Hz display.



- b. Set 5345A FUNCTION switch to PLUG-IN and connect setup as before.
- c. The 5355A should correctly count the 10 GHz signal. Record results on performance test record (Table 4-4) and continue with test 4.

4-32. TEST 4, AUTO MODE: 50 Hz PRF WITH 20 ms PULSE WIDTH (WITH MINIMUM OFF TIME OF 400 ns).

- Use the same setup as in Test 3 but push the 5355A MANUAL key (light out) to enter the automatic mode. The 5355A should correctly count the 10 GHz signal.
- Record results on performance test record (Table 4-4).

4-33. 5355A (.4—1.6 GHz) Maximum Input Test

Specification: +5 dBm

Description: The 5355A is set to the 0.4—1.6 GHz range and a signal at the maximum rated level is applied to the BNC Input. The frequency is slowly swept up to 1.6 GHz at a constant level while the 5355A display is checked for the proper count.

Setup: Figure 4-9.

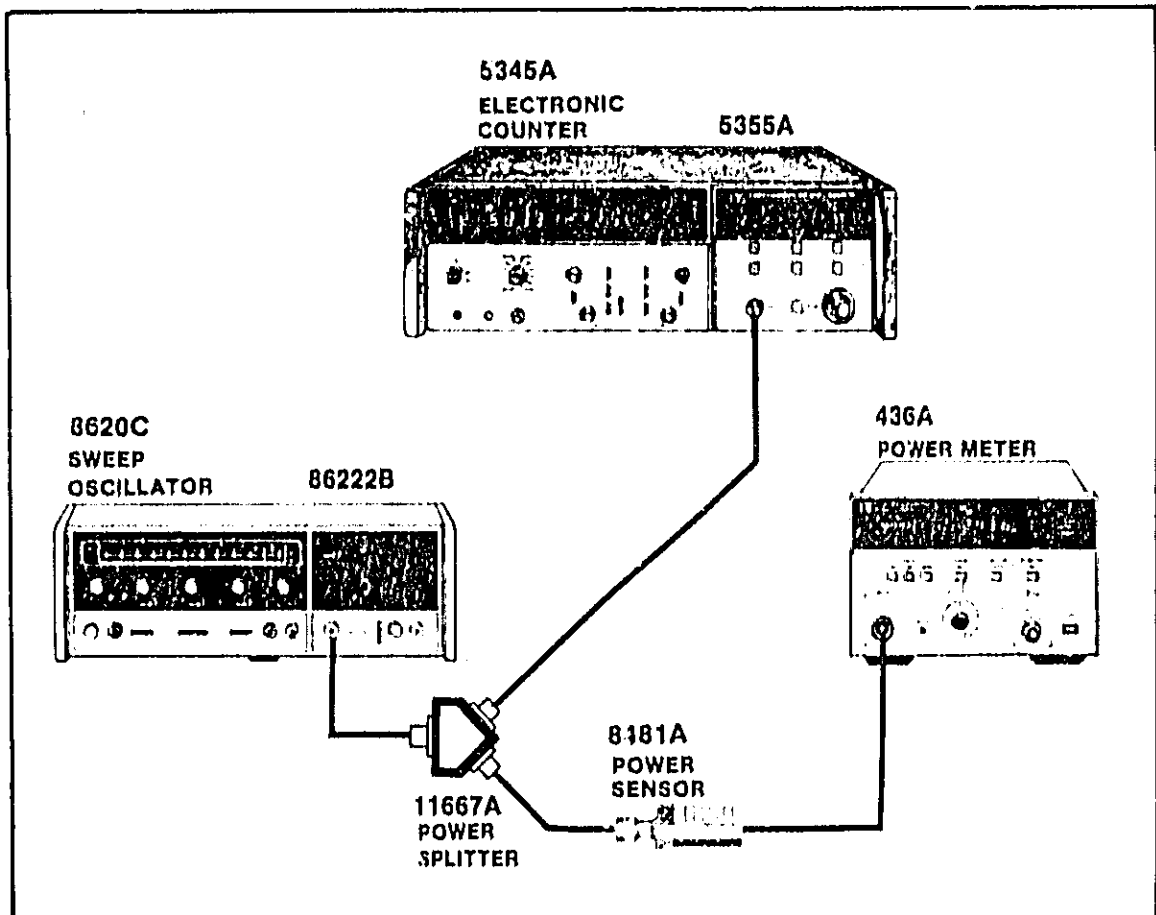


Figure 4-9. 5355A (.4—1.6 GHz) Maximum Input Test

- Turn on 5345A power. Push INPUT SELECT key on 5355A to select the prescaler input.
- Set 436A power meter for auto range (RANGE HOLD button out) and dBm mode.
- Set 86222B for INT leveling and adjust the output level for a 436A reading of +5 dBm.
- Set the 8620C to 400 MHz at +5 dBm as measured by the 436A Power Meter. Monitor the power meter while slowly sweeping the frequency up to 1.6 GHz. Verify that the 5355A counts correctly across the band at the rated power level. Enter the results on the performance test record (Table 4-4).

4-34. 5355A/5356 Maximum Input Tests

Specification: See Table 4-2.

Description: The 5355A is set to the higher frequency (converter head) range and a signal at the maximum rated level is applied to the converter head. The frequency is slowly swept through the appropriate range at a constant level while the 5345A display is checked for the proper count.

4-35. TEST 1. 1.5—18 GHz. See Table 4-2 specifications for head under test.

Setup: Figure 4-10.

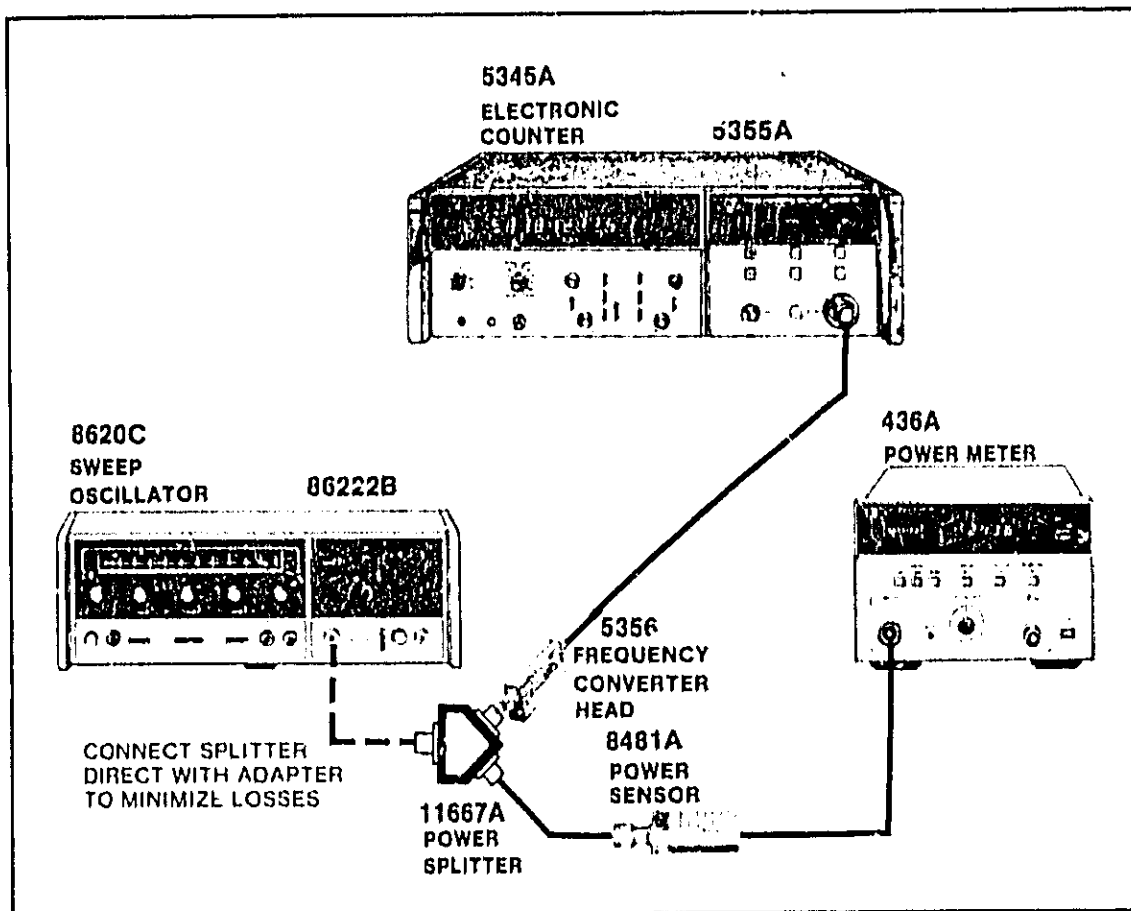


Figure 4-10. 5355A/5356 Maximum Input Test, 1.5—18 GHz Setup

- Turn on 5345A power.
- Set 436A power meter for auto range (RANGE HOLD button out) and dBm mode.
- Set 86222B/86250A for INT leveling and adjust the output power level for a 436A reading per Table 4-2 for head under test.
- Vary the 8620C frequency over the range of 1.5 to 18 GHz and verify that the 5355A counts properly. Use the 436A to verify input power. Enter the results on the performance test record (Table 4-4).

Table 4-2. Maximum Input Specifications, HP Model 5356A, B, and C Frequency Converter Heads

Frequency	5356A	5356B	5356B Option 001	5356C	5356C Option 001
1.5—12.4 GHz	+5 dBm	+5 dBm	—	+ 5 dBm	—
12.4—18 GHz	+5 dBm	+5 dBm	—	+15 dBm	—
18—26.5 GHz	—	+5 dBm	+5 dBm	+15 dBm	—
26.5—40 GHz	—	—	—	+15 dBm	+15 dBm

4-36. TEST 2: 18—26.5 GHz. See Table 4-2 specifications for head under test.

Setup: Figure 4-11.

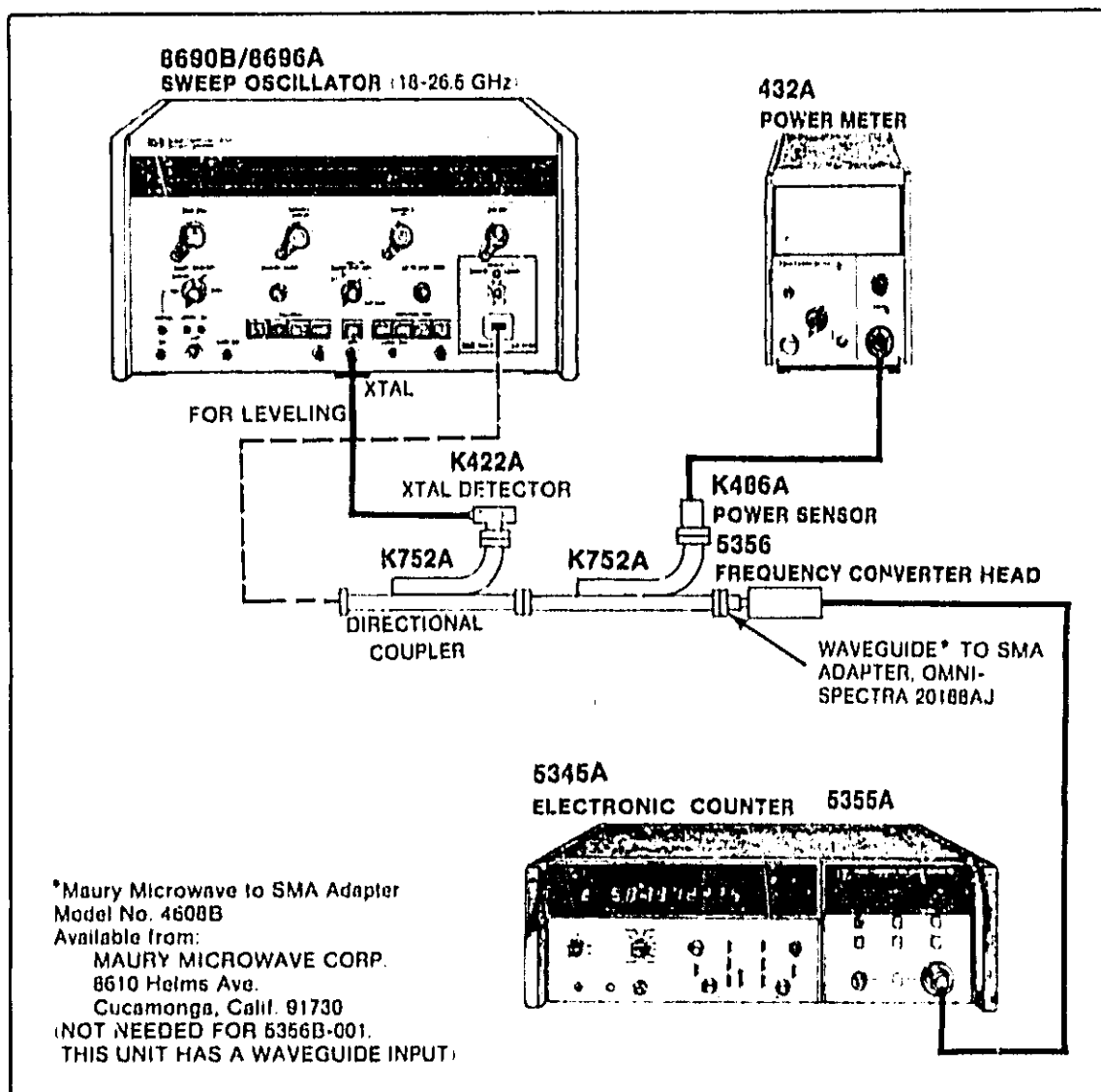


Figure 4-11. 5355A/5356 Maximum Input Test, 18—26.5 GHz Setup

- Set the 8690B/8696A for a CW signal and adjust power level for a 432A reading per Table 4-2.
- Vary the 8690B frequency over the range of 18 to 26.5 GHz and verify that the 5355A counts properly. Use the 432A to verify input power. Enter the results on the performance test record (Table 4-4).

4-37. 5355A/5356 FM Tolerance Test

Specification:

Auto Mode: 15 MHz p-p
60 MHz p-p in special FM mode

Manual Mode: 80 MHz p-p

Description: The FM tolerance specification indicates the worst case FM deviation that can be present on a carrier that the counter can acquire and count. If the deviations are symmetrical about the carrier, then the counter averages out the deviations and displays only the carrier frequency. In this test, a test oscillator is used to FM the 86290A and the output is examined on a spectrum analyzer to measure the peak-to-peak deviation. The amplitude of the modulating waveform is adjusted for deviations of 15 MHz p-p and 60 MHz p-p in the auto mode and for 80 MHz p-p in the manual mode.

Setup: Figure 4-12

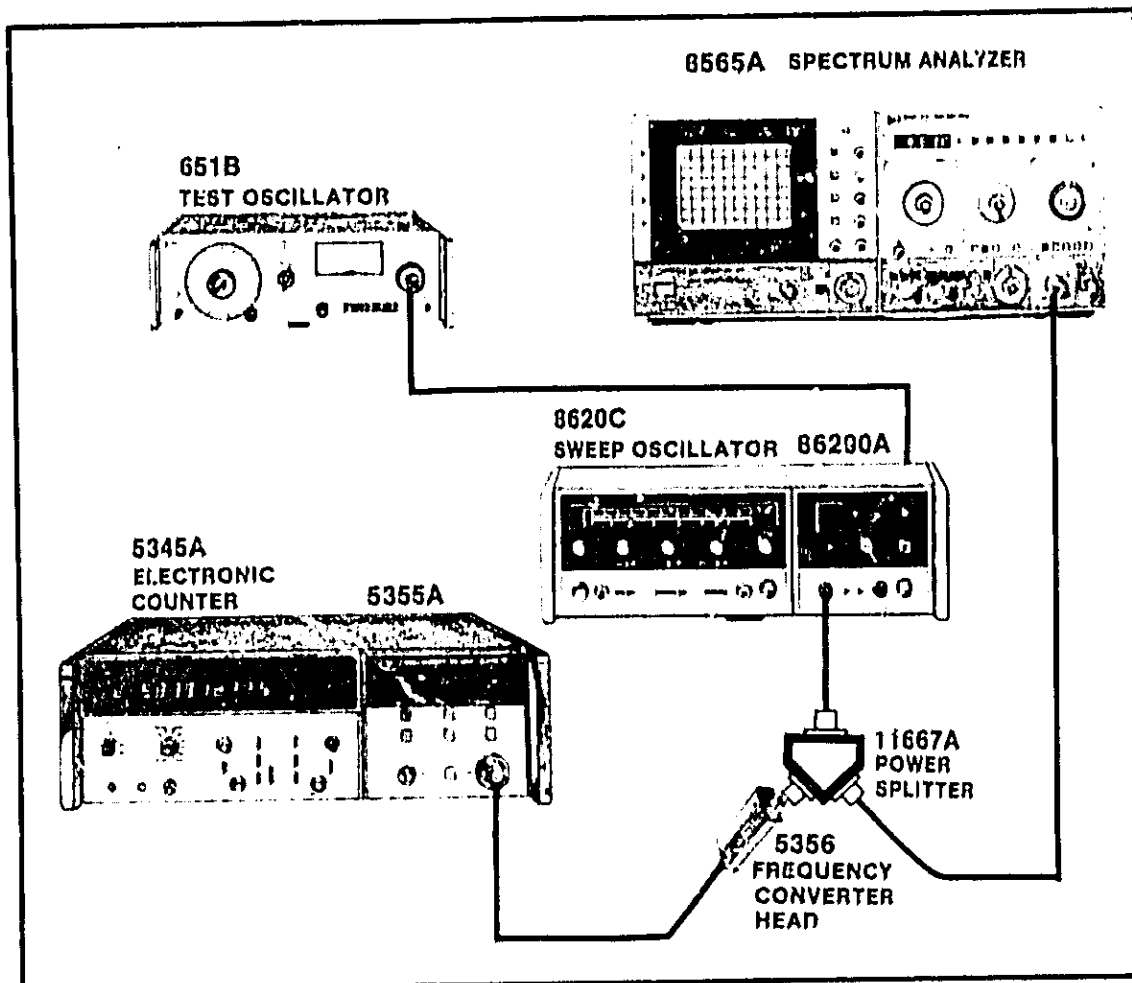
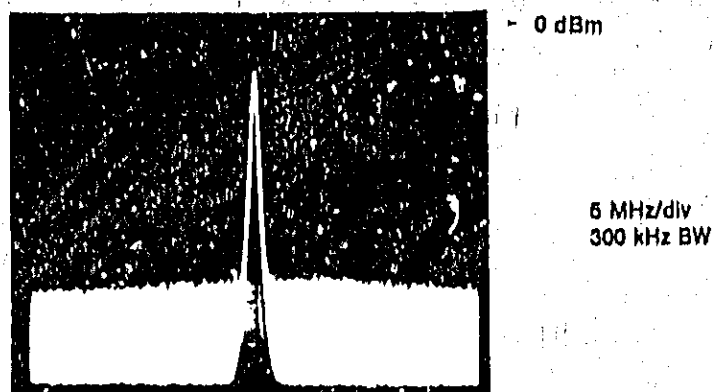


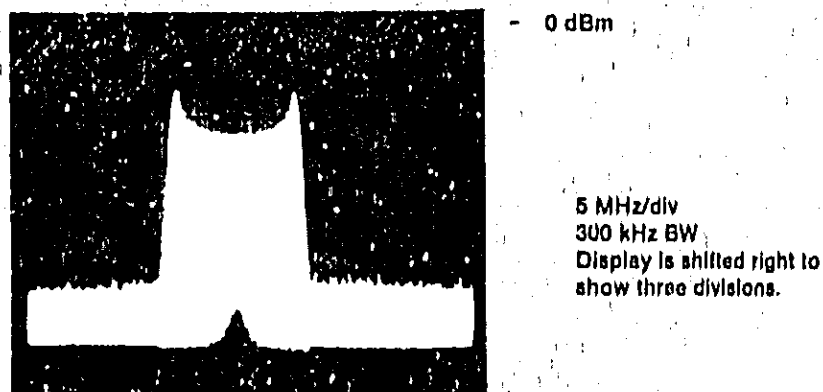
Figure 4-12. 5355A/5356 FM Tolerance Setup

Model 5355A
Performance Tests

- a. Set 651A OUTPUT ATTENUATOR switch full CCW.
- b. Set B6290A to 10 GHz at -10 dBm as displayed on spectrum analyzer, shown below.

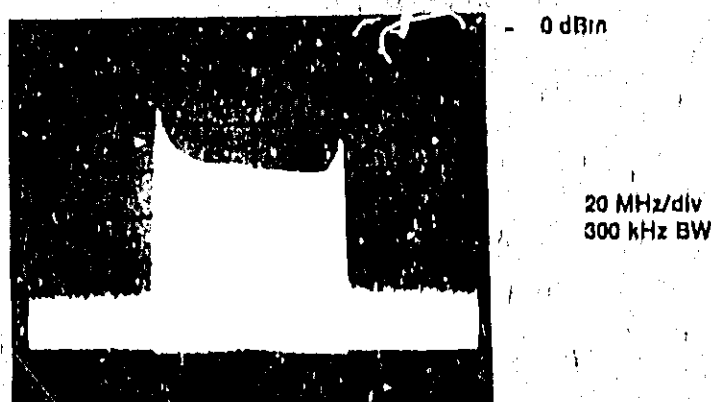


- c. Set the 651A to 100 kHz and increase the output level until the spectrum analyzer shows a 15 MHz p-p FM deviation.



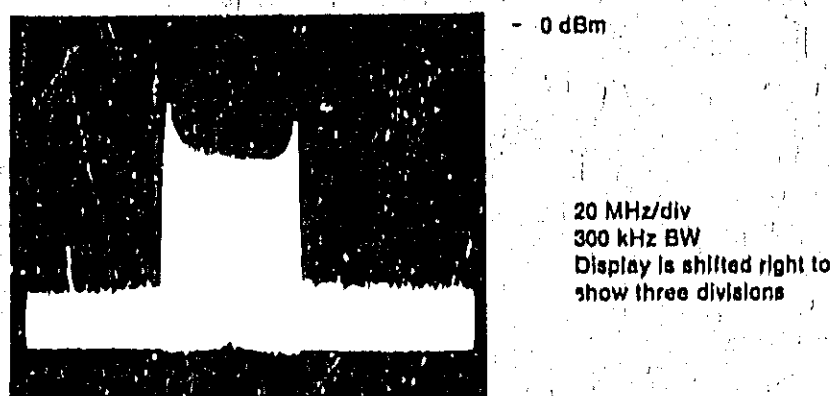
- d. Verify that the 5355A will acquire and count the signal. Record results on performance test record (Table 4-4).
- e. If deviations are symmetrical about the center frequency, the 5355A will average out the deviations and display the 10 GHz center frequency.
- f. Push the 5355A MANUAL key to enter the manual mode.

- g. Increase the 651A output level until the spectrum analyzer shows an 80 MHz p-p FM deviation.



10 GHz with 80 MHz p-p FM Deviation

- h. The 5355A should acquire and count the signal. Record the results on performance test record (Table 4-4).
- i. If deviations are symmetrical about the center frequency, the 5355A will average out the deviations and display the 10 GHz center frequency.
- j. Remove FM from signal by reducing 651A output level.
- k. Push the 5355A MANUAL key to return to the auto mode (MANUAL light out).
- l. Simultaneously push the 5355A CW and PULSE keys to enter the special FM mode. The CW light will blink slowly to indicate that the FM mode has been entered.
- m. Increase the 651A output level until the spectrum analyzer shows a 60 MHz p-p FM deviation.



10 GHz with 60 MHz p-p FM Deviation

- n. Verify that the 5355A will acquire and count the signal. Record the results on performance test record (Table 4-4).

4-38. 5355A (.4—1.6 GHz) Accuracy Test, CW Mode

Specification: $\pm 10 \times \text{LSD} \pm \text{time base error} \times \text{input frequency}$.

Description: The 5355A is set to the lower frequency (prescaler) range and a signal from a frequency synthesizer is applied to the BNC input. The internal oscillators of the synthesizer and 5345A are locked together to eliminate the time base portion of the specification. The 5345A display is then checked for the proper count.

Setup: Figure 4-13.

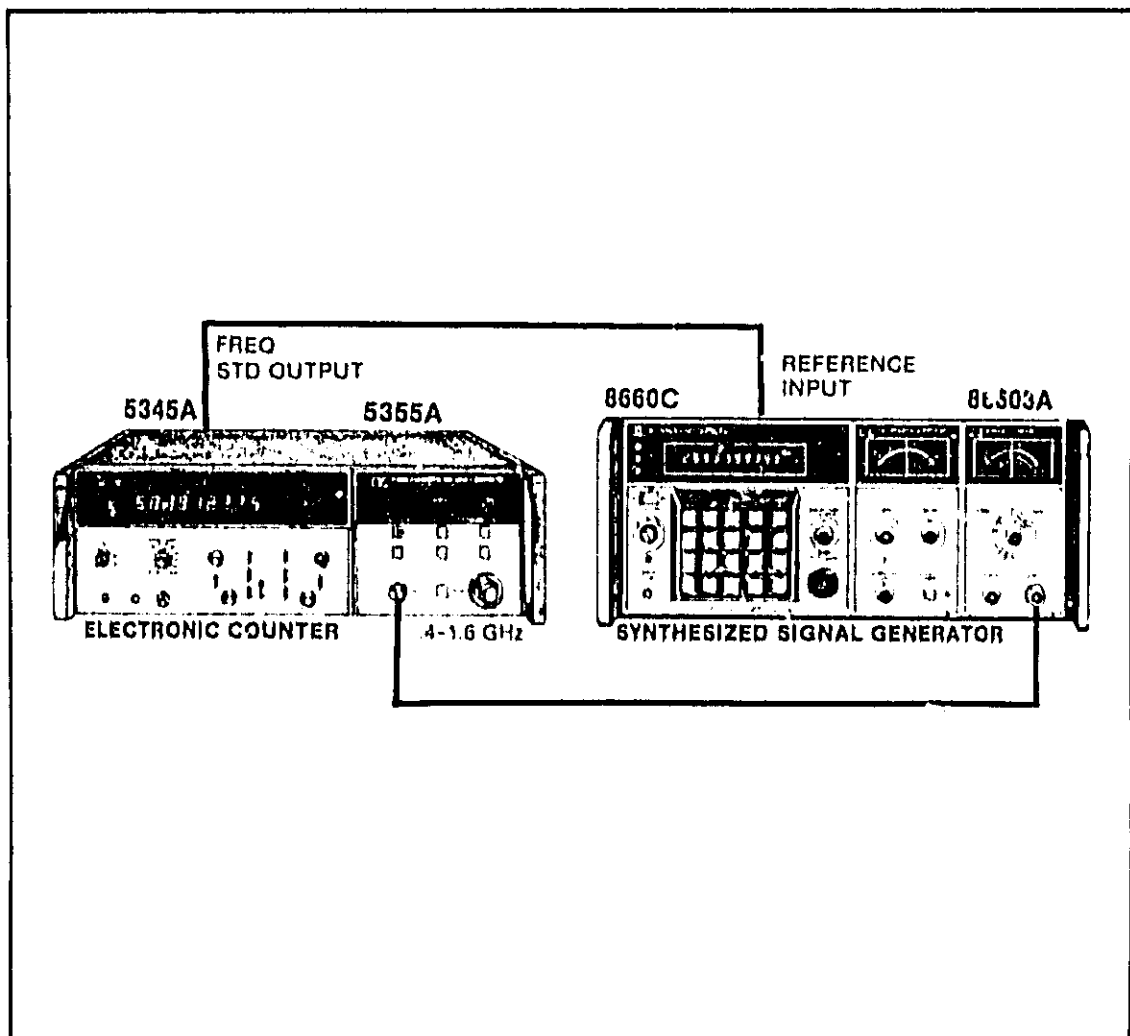


Figure 4-13. 5355A (.4—1.6 GHz) Accuracy Test, CW Mode Setup

- Set 5345A GATE TIME switch to 1 s.
- Turn on 5345A power. Push 5355A INPUT SELECT key to select the prescaler input.
- Connect the internal oscillators as shown above.
- Set the 8660C for 400 MHz at -10 dBm.
- The 5345A display should read 400.000000 MHz ± 10 Hz. Record results on performance test record (Table 4-4).

4-39. 5355A (.4—1.6 GHz) Accuracy Test, Pulsed RF Mode

Specification: $\pm 16 \times \text{LSB} \pm 5 \times \text{rms jitter}^* \pm \frac{.08}{\text{EXT GATE WIDTH}}$

$\pm 24 \text{ kHz} \pm \text{time base error} \times \text{Input frequency.}$

$$^*\text{rms jitter} = \frac{1}{\sqrt{(5345\text{A GATE TIME})(\text{EXT GATE WIDTH})}} + 100 \text{ Hz rms.}$$

Description: The 5355A is set to the lower frequency (prescaler) range and the pulse mode. A pulsed RF signal from a frequency synthesizer is applied to the BNC input. The internal oscillators of the synthesizer and 5345A are locked together to eliminate the time base portion of the specification. The 5345A display is then checked for the proper count.

Setup: Figure 4-14.

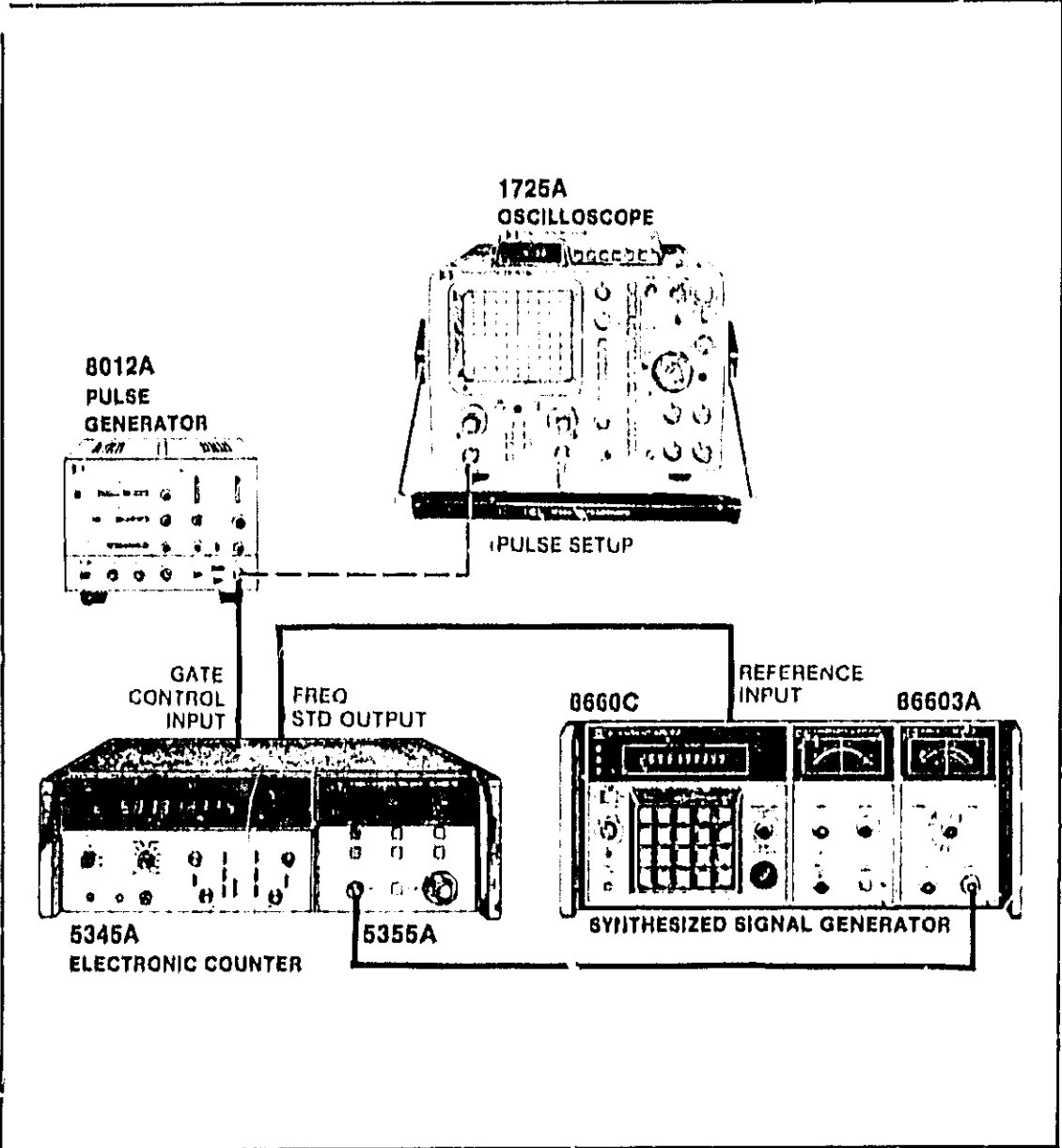


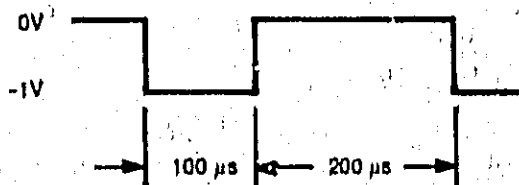
Figure 4-14. 5355A (.4—1.6 GHz) Accuracy Test, Pulsed RF Mode Setup

Model 5355A Performance Tests

8012A Setup:

PULSE PERIOD	0.1 ms-10 ms
DELAY	25 ns-1 μ s
PULSE WIDTH SWITCH	1 μ s-0.1 ms
TRANSITION TIME	5 ns-0.5 μ s
LEADING AND TRAILING EDGES	ccw
AMPLITUDE SWITCH	0.5-1V
AMPLITUDE VERNIER	1V
OFFSET	OFF
PULSE POLARITY	-

The signal can be observed on an oscilloscope using a 50-ohm termination for final adjustment. The waveform should conform to the figure below.



5345A Settings:

GATE CONTROL SWITCH	EXT GATE
GATE TIME	100 ms

- Turn on 5345A power. Push 5355A INPUT SELECT key to select the prescaler input.
- Connect the internal oscillators as shown in Figure 4-14.
- Set the 8660C for 500 MHz at 0 dBm.
- The 5345A display should read 500.000 MHz $\pm$ 27 kHz. (This is the accuracy at the 1 σ (sigma) point of the rms jitter. Individual readings may be worse than this by several times the jitter number, which is 2.18 kHz.) Record results on performance test record (Table 4-4).

NOTE

When finished, return GATE CONTROL switch to the INTERNAL position.

4-40. 5355A/5356 Accuracy Test, CW Mode

Specification: $\pm 2 \times \text{LSD} \pm 1 \times 10^{-10} \text{ rms} \times \text{Input frequency} \pm \text{time base error} \times \text{Input frequency}$.

Description: The frequency is set to the higher frequency (converter head) range and a signal from a frequency synthesizer is applied to the converter head. The internal oscillators of the synthesizer and 5345A are locked together to eliminate the time base portion of the specification. The 5345A display is then checked for the proper count.

Setup: Figure 4-15.

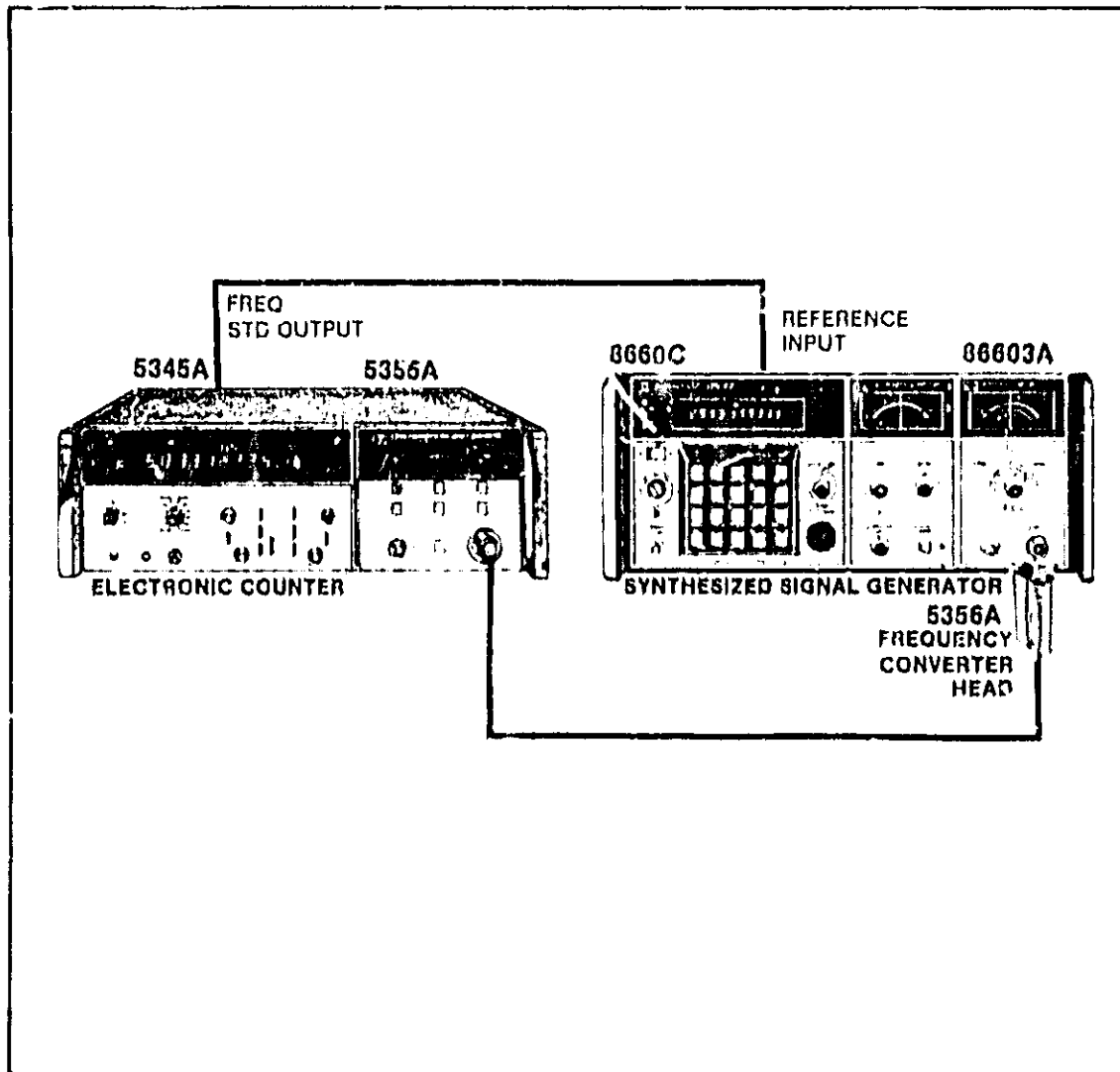


Figure 4-15. 5355A/5356 Accuracy Test, CW Mode Setup

- Set 5345A GATE TIME switch to 1 s.
- Turn on 5345A power.
- Connect the internal oscillators as shown in Figure 4-15. Set the 8660C for external reference.
- Set the 8660C for 2.0 GHz at 0 dBm.
- The 5345A display should read 2.000000000 GHz ± 2 Hz. Record results on performance test record (Table 4-4).

4-41. 5355A/5356 Accuracy Test, Pulsed RF Mode

Specification: $\pm 2 \times \text{LSD} \pm \text{rms jitter}^* \pm \frac{.04}{\text{EXT GATE WIDTH}}$

$\pm 3 \text{ kHz} \pm \text{time base error} \times \text{input frequency}$

$$^*\text{rms jitter} = \frac{1}{\sqrt{(5345\text{A GATE TIME}) (\text{EXT GATE WIDTH})}} + 100 \text{ Hz rms.}$$

Description: The 5355A is set to the higher frequency (converter head) range and then to the manual mode at a specified frequency. A signal from a frequency synthesizer is applied to the converter head. The internal oscillators of the synthesizer and 5345A are locked together to eliminate the time base portion of the specification. The 5345A is then checked for the proper count.

Setup: Figure 4-16.

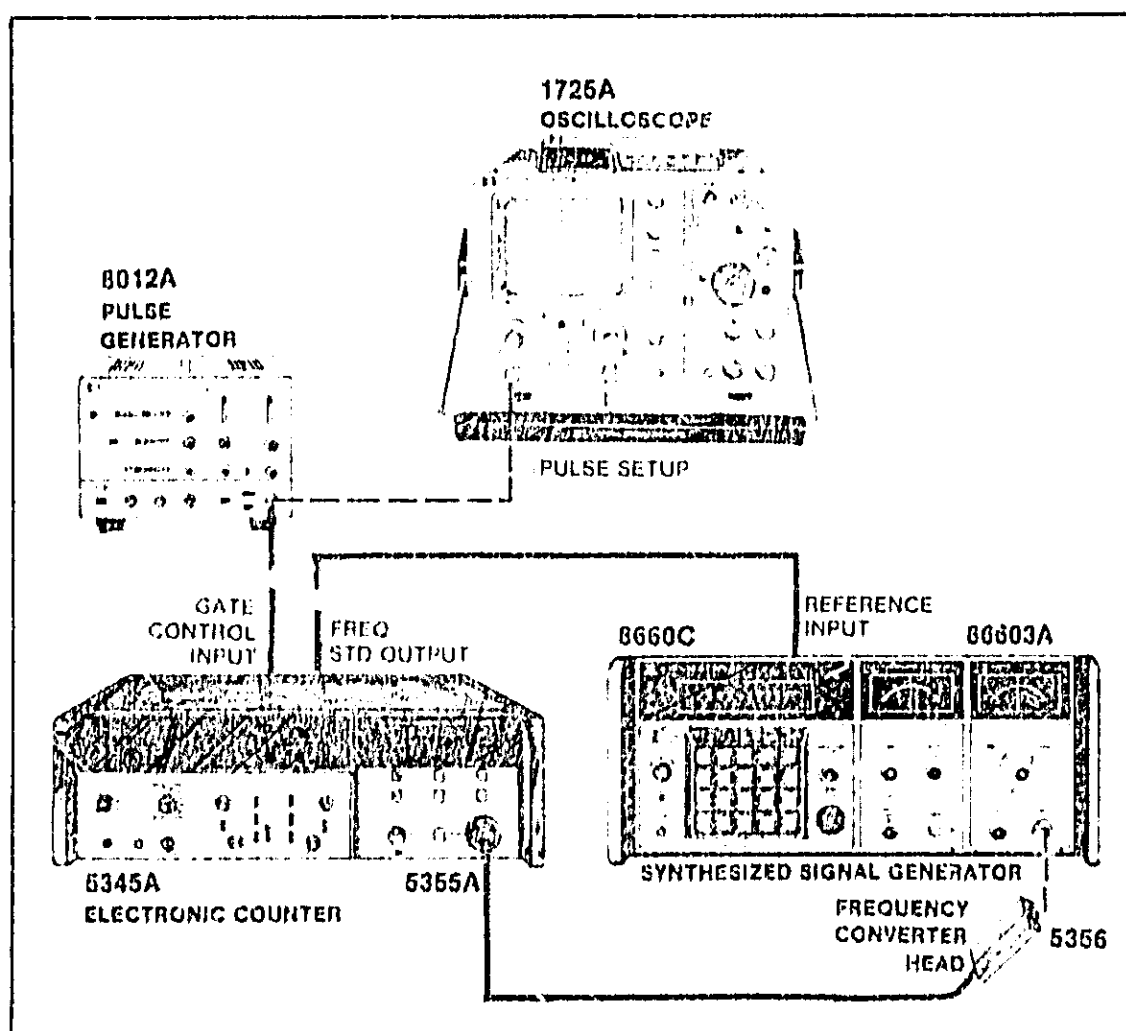
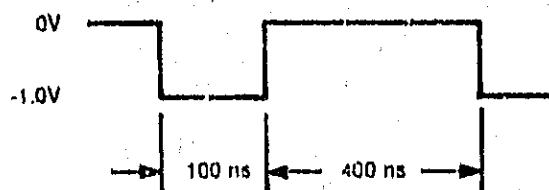


Figure 4-16. 5355A/5356 Accuracy Test, Pulsed RF Mode Setup

8012A Setup:

PULSE PERIOD	20 ns–1 μ s
DELAY	35 ns–1 μ s
PULSE WIDTH SWITCH	1 μ s–0.1 ms
TRANSITION TIME	5 ns–0.5 μ s
LEADING AND TRAILING EDGES	CCW
AMPLITUDE SWITCH	1.0–2.0V
OFFSET	OFF
PULSE POLARITY	–

The signal can be observed on an oscilloscope using a 50-ohm termination for final adjustment. The waveform should conform to the figure below.



5345A Settings:

GATE CONTROL SWITCH	EXT GATE
GATE TIME	1 ms

- Turn on 5345A power.
- Push MAN FREQ key and set manual frequency to 2.4 GHz. Push MAN FREQ key to exit data entry mode and MANUAL key to enter the manual measurement mode.
- Push 5355A PULSE key.
- Set the 8660C for 2.330 GHz at 0 dBm. Also, set for external reference.
- The 5345A display should read 2.330000 GHz $\pm$ 505 kHz. (This is the accuracy at the 1 σ (sigma) point of the rms jitter. Individual readings may be worse than this by several times the jitter number, which is 100 kHz.) Record results on performance test record (Table 4-4).

NOTE

The above procedure checks the accuracy at the worse case point. If the accuracy specification cannot be met, the cause may lie in the 5345A circuits and not in the 5355A. To determine if the error is in the 5345A circuits, perform the procedure described in paragraph 4-47, 5345A Accuracy Test, Pulsed RF mode.

4-42. Rear Panel Output Tests: Gate Out, Pulse Out, IF Out

Specifications:

GATE OUT: 0 to -1V pulse output. Width of GATE OUT signal is approximately 30 ns less than RF burst width.

PULSE OUT: Detected IF signal: TTL levels; 0 to 1V typical into 50-ohms.

IF OUT: Down converted signal in range of 70—375 MHz at 0 dBm nominal level.

Description: Apply pulsed RF and CW signals and monitor the output jacks for proper signal conditions.

4-43. GATE OUT TEST

Setup: Figure 4-17.

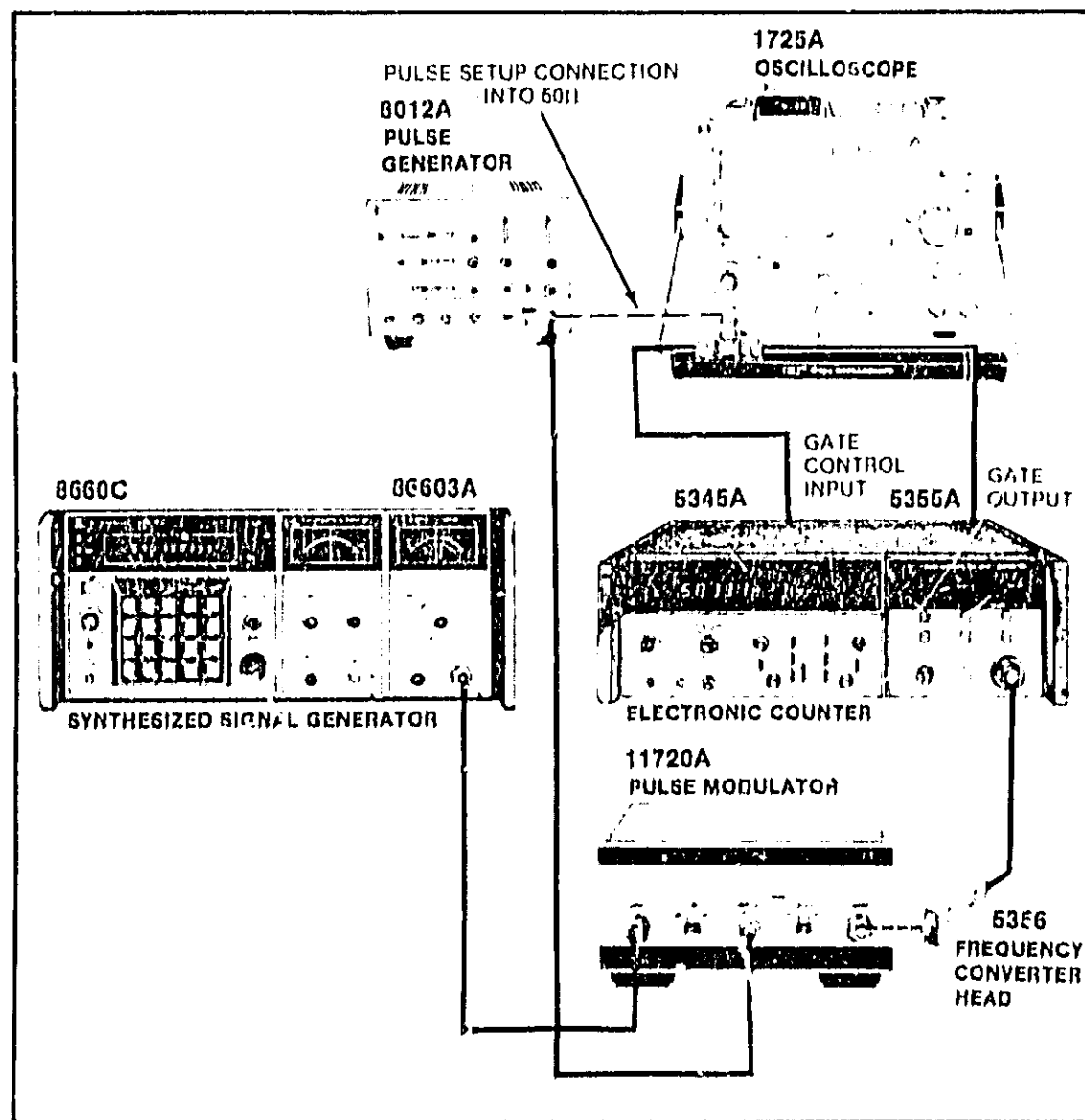
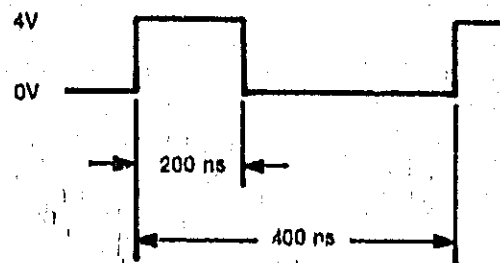


Figure 4-17. Gate Out Test Setup

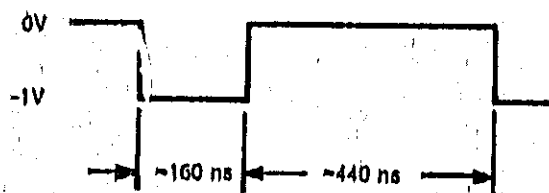
8012A Setup:

PULSE PERIOD	20 ns-1 μ s
PULSE DELAY	35 ns-1 μ s
PULSE WIDTH	10 ns-1 μ s
TRANSITION TIME	5 ns-0.5 μ s
LEADING AND TRAILING EDGES	ccw
AMPLITUDE SWITCH	2.0-5.0V
OFFSET	OFF
PULSE POLARITY	+

The signal can be observed on an oscilloscope using a 50-ohm termination for final adjustment. The waveform should conform to the figure below.



- Set 8660C to 2.0 GHz at 0 dBm.
- Turn on 5345A power.
- Push PULSE key on 5355A and monitor waveform on oscilloscope. The waveform should appear as follows. Record on performance test record (Table 4-4). (Ignore 5345A display. Circuit connections are optimized to monitor the GATE OUT pulse.)



4-44. PULSE OUT TEST

- Use same basic test setup as Figure 4-17 with exception of connections shown in Figure 4-17a.

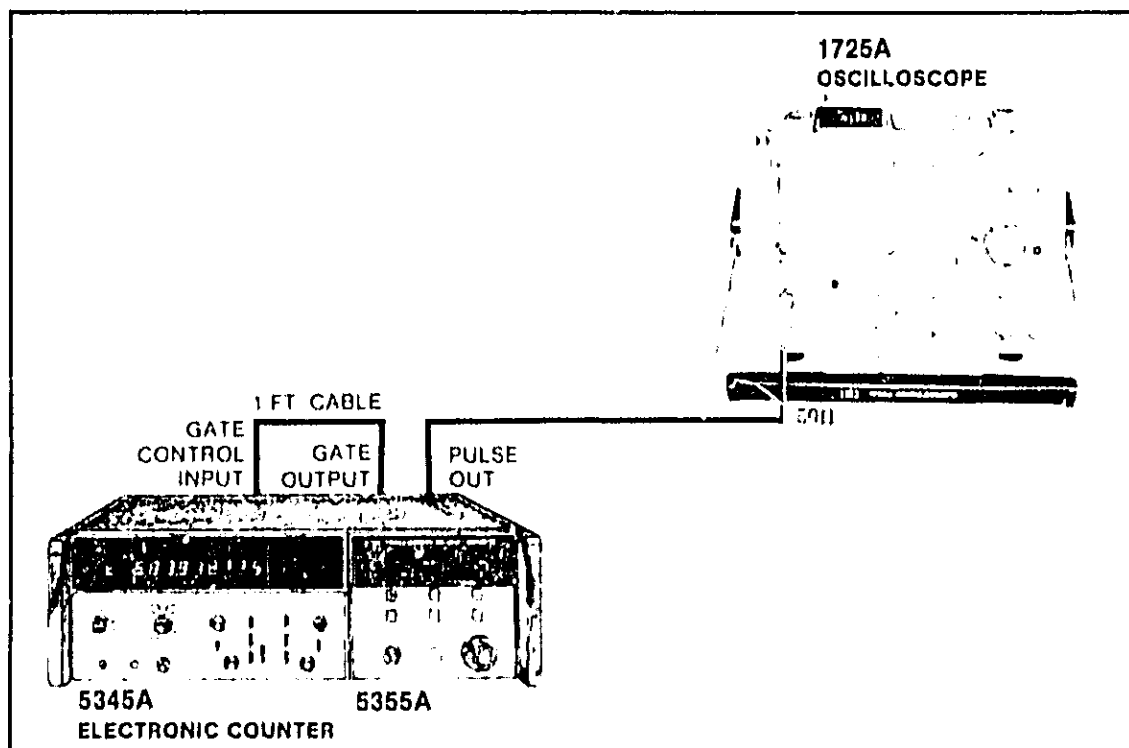
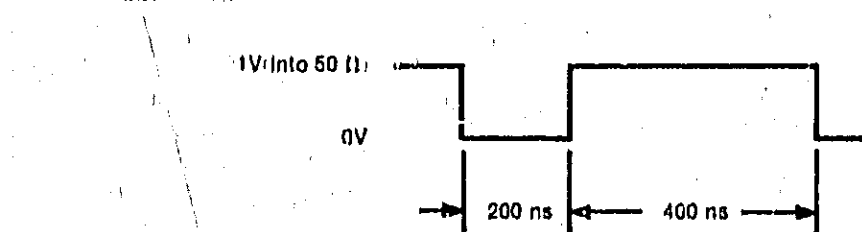


Figure 4-17a. Pulse Out Test Setup

- The waveform should appear as shown below. Record results on performance test record (Table 4-4).



4-45. IF OUT TEST

4-46. Use same basic setup as in Figure 4-17 but make the following changes:

- Connect 436A Power Meter with B4B1A Power Sensor to 5355A IF OUT jack.
- Set 11720A LINE switch to OFF.
- Push CW key on 5355A.
- Power meter should read approximately 0 dBm or greater. Record results on performance test record (Table 4-4).
- Remove power meter and connect a BNC cable from the IF OUT jack to the 5345A CHANNEL A jack.
- Set 5345A FUNCTION switch to FREQ A. IF frequency should be between 70 to 375 MHz. Record results on performance test record (Table 4-4).

NOTE

The following test (5345A Accuracy Test, Pulsed RF Mode), needs to be performed only in the event that the 5355A/5356 Accuracy Test, Pulsed RF Mode (paragraph 4-41) fails to meet specifications. If the counter fails the accuracy test in paragraph 4-48, refer to subparagraph m.

4-47. 5345A Accuracy Test, Pulsed RF Mode

4-48. Use the following procedure to determine if the 5345A gate bias error is within the required tolerances.

- a. Set up the test equipment as shown below (Figure 4-18) and allow a few minutes for warmup.

Setup: Figure 4-18.

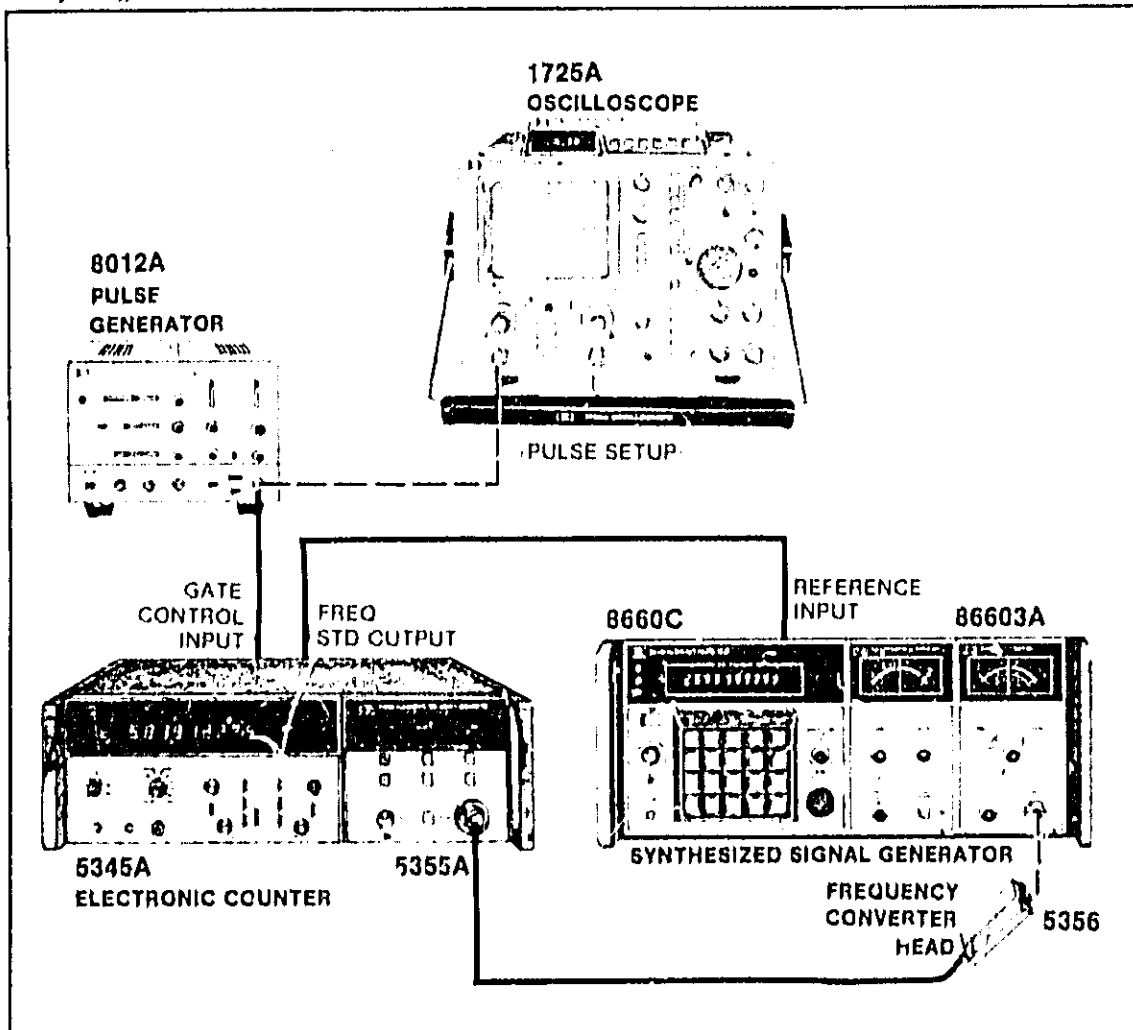


Figure 4-18. 5345A Accuracy Test, Pulsed RF Mode Setup

NOTE

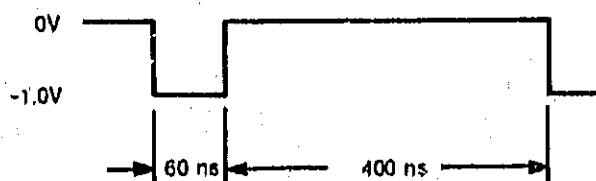
The setup shown above is not valid for the following converter heads: 5356B Option 001 or 5356C Option 001. If these are the only converter heads available, use the alternate test setup in Figure 4-19. Since this setup requires connecting cables within the 5355A, it should be performed only by qualified service personnel. Continue test at step h.

Model 5355A
Performance Tests

b. 8012A Setup:

PULSE PERIOD	20 ns-1 μ s
PULSE DELAY	35 ns-1 μ s
PULSE WIDTH	10 ns-1 μ s
TRANSITION TIME	5 ns-0.5 μ s
LEADING AND TRAILING EDGES	CCW
AMPLITUDE SWITCH	1.0-2.0V
OFFSET	OFF
PULSE POLARITY	-

- c. The signal can be observed on an oscilloscope using a 50-ohm termination for final adjustment. The waveform should conform to the figure below.



- d. Set 5345A GATE TIME switch to 100 ms and turn on power to instrument.
- e. Set 8660C to exactly 220 MHz at 0 dBm.
- f. On 5355A, simultaneously push the MAN FREQ and OFFSET FREQ keys until the numbers on the 5345A display advance to $\text{-----} \text{---} \text{---}$. The counter should now display the input frequency.
- g. Set the 5345A rear panel GATE CONTROL switch to EXT GATE. The displayed frequency will change from the original reading.
- h. Subtract the present reading from the input frequency and multiply the difference by 1.5. Record this value for later use.
- i. Change 8660C frequency to 325 MHz.
- j. Subtract the present reading from the input frequency and record this value.
- k. If both readings were off in the same direction, i.e., both readings higher or lower than the input frequencies, calculate the difference between the two recorded values (see Example 1 in step n). The difference should be <660 kHz. If not, see step m.
- l. If the readings were off in opposite directions, i.e., one higher than the input frequency and the other lower, add the first recorded value to the second recorded value. (See Example 2 in step n.) The summation should be <660 kHz. If not, see step m.
- m. If the counter fails this test, return it, the 5355A and the 5356 to the nearest Hewlett-Packard Sales and Service office for modification.

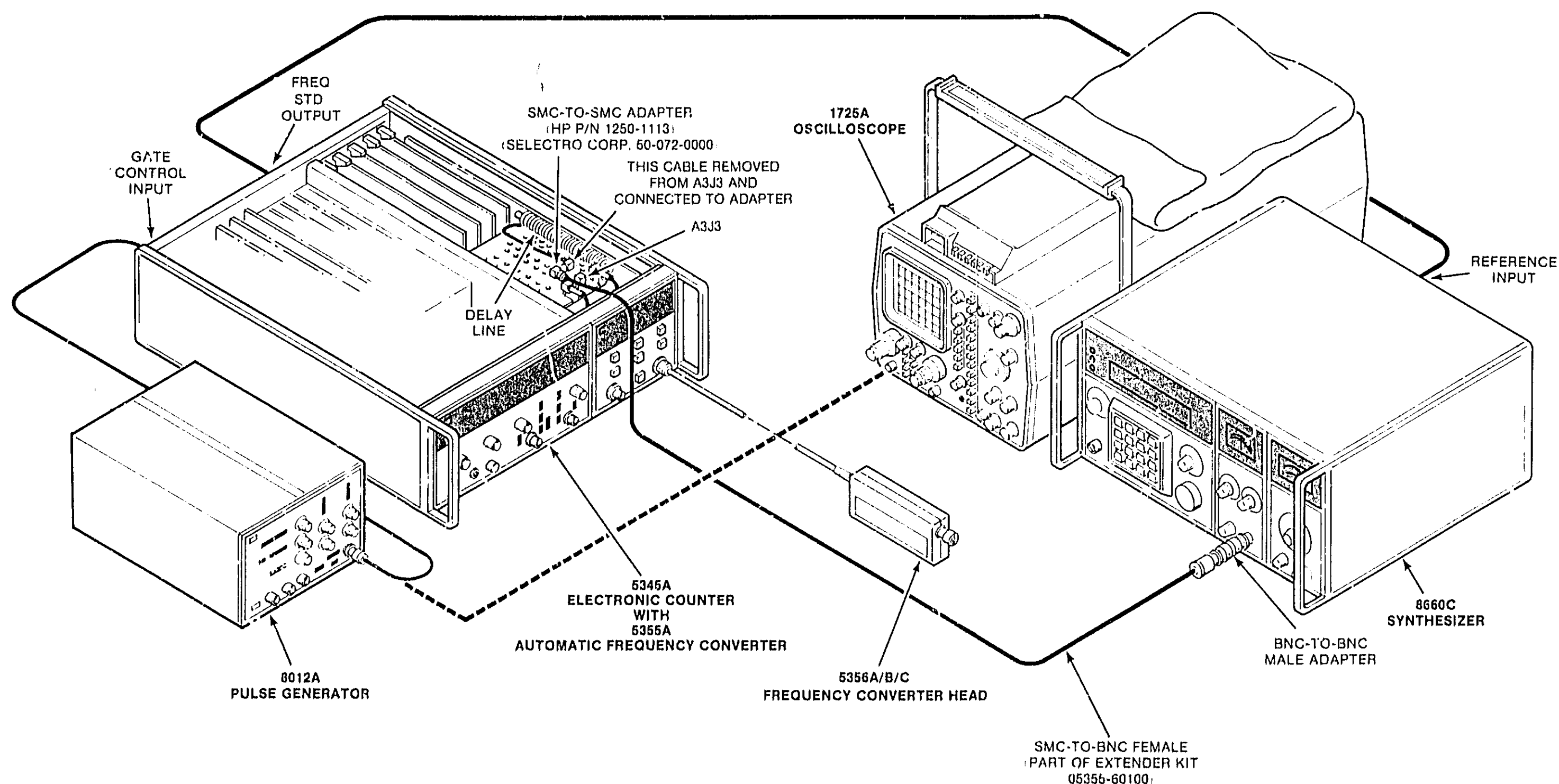


Figure 4-19. 5345A Accuracy Test, Pulsed RF Mode Alternate Setup

4-49. HP-IB VERIFICATION PROGRAM

4-50. The 9825A program listed in Table 4-6 exercises the 5355A through various operating modes, described below, via its HP-IB Interface. If the 5355A successfully completes all phases of the verification program, then there is a high probability that the HP-IB Interface (A8 assembly) is working properly. If the 5355A does not respond as described, refer to HP-IB troubleshooting in Section VIII.

4-51. To perform the verification, set up the equipment as shown below and set the 5355A rear panel address switches to Address 00. The 5345A is not part of the HP-IB programs that follow. Therefore, the 5345A must not be connected to the Bus. If readings are desired on the bus, the 5345A must be connected and separately programmed. Refer to 5345A Operating and Service Manual for information.

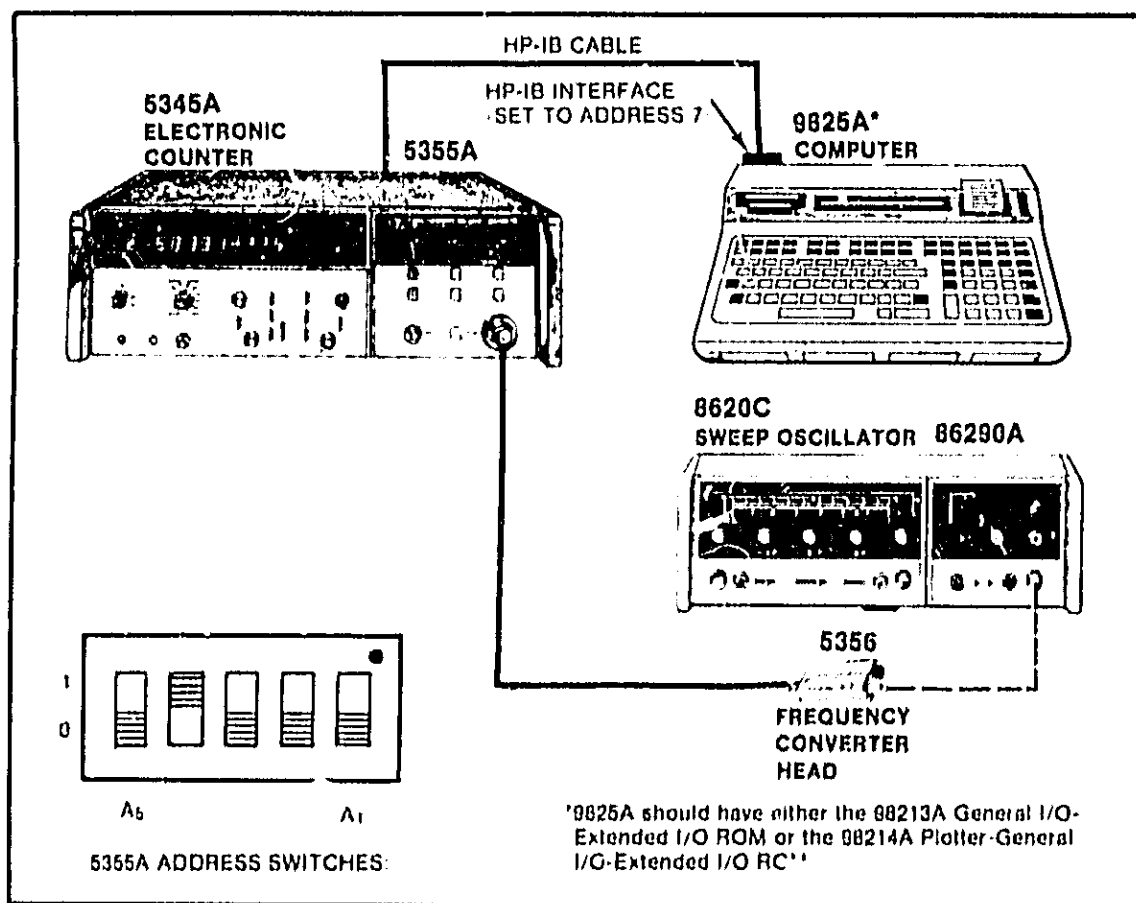


Figure 4-20. HP-IB Verification Test Setup

4-52. The program listed in Table 4-6 may be keyed into the 9825A using the program codes from Table 4-5, or may be loaded from a HP-IB Verification Cassette, HP P/N 59300-10001, which also contains HP-IB verification programs for the 59300 series of instruments. To run the program on the cassette, insert the cassette into the 9825A, load file 0, and press RUN. Enter "5355" when the instrument mode number is requested and select code "700" when select code is requested. The 9825A will then load the 5355A verification program into memory.

4-53. The program goes through 11 check points as described in Table 4-7. The information in Table 4-7 tells what occurs during each test and what should be observed by the operator if the test has been successfully completed. At the conclusion of each test, the program stops and displays the current check point. To advance to the next test, simply press CONTINUE. If it is desired to repeat a test, set the variable L to 1 via the keyboard (1 → L EXECUTE). To go on to the next test after looping, set L back to 0 when the program halts (0 → L EXECUTE). Record on operational verification record (Table 4-3) or the performance test record (Table 4-4) as applicable.

4-54. Table 4-8 is a sample printout from the 9825A.

Table 4-3. Operational Verification Record

5355A S/N _____		Test Performed By _____
5356A S/N _____		
5356B S/N _____		
5356C S/N _____		Date _____
PARAGRAPH NUMBER	TEST	RESULTS PASS/FAIL
4-11.	5355A Input Sensitivity, CW Mode	_____
4-12.	5355A Input Sensitivity, Pulsed RF Mode	_____
4-18.	5355A/5356 Input Sensitivity, CW	_____
4-19.	Test 1. 1.5-12.4 GHz	_____
4-20.	Test 2. 12.4-18 GHz	_____
4-21.	Test 3. 18-26.5 GHz	_____
4-22.	Test 4. 26.5-40 GHz	_____
4-23.	5355A/5356 Input Sensitivity, Pulsed RF	_____
4-24.	Test 1. 1.5-12.4 GHz	_____
4-25.	Test 2. 12.4-18 GHz	_____
4-26.	Test 3. 18-26.5 GHz	_____
4-27.	Test 4. 26.5-40 GHz	_____
4-49.	HP-IB Verification	_____

Table 4-4. Performance Test Record

5355A S/N _____		Test Performed By _____
5356A S/N _____		
5356B S/N _____		
5356C S/N _____		Date _____
Paragraph Number	Test	Actual Results
4-11.	5355A Input Sensitivity, CW	_____
4-12.	5355A Input Sensitivity, Pulsed RF	_____
4-15.	5355A Input Tests, PW, PRF	_____
4-16.	Test 1. 2 MHz PRF, 100 ns	_____
4-17.	Test 2. 100 Hz PRF, 10 ms	_____
4-18.	5355A/5356 Input Sensitivity, CW	_____
4-19.	Test 1. 1.5—12.4 GHz	_____
4-20.	Test 2. 12.4—18 GHz	_____
4-21.	Test 3. 18—26.5 GHz	_____
4-22.	Test 4. 26.5—40 GHz	_____
4-23.	5355A/5356 Input Sensitivity, Pulsed RF	_____
4-24.	Test 1. 1.5—12.4 GHz	_____
4-25.	Test 2. 12.4—18 GHz	_____
4-26.	Test 3. 18—26.5 GHz	_____
4-27.	Test 4. 26.5—37.2 GHz	_____
4-28.	5355A/5356 Input Test, PW, PRF	_____
4-29.	Test 1. Auto Mode, 2 MHz PRF, 100 ns	_____
4-30.	Test 2. Manual Mode, 2 MHz PRF, 60 ns	_____
4-31.	Test 3. Manual Mode, 50 Hz PRF, 20 ms	_____
4-32.	Test 4. Auto Mode, 50 Hz PRF, 20 ms	_____
4-33.	5355A Maximum Input	_____
4-34.	5355A/5356 Maximum Input	_____
4-35.	Test 1. 1.5—18 GHz	_____
4-36.	Test 2. 18—26.5 GHz	_____
4-37.	5355A/5356 FA ¹ Tolerance	_____
4-38.	Accuracy, CW	_____
4-39.	5355A Accuracy, Pulsed RF	_____
4-40.	5355A/5356 Accuracy, CW	_____
4-41.	5355A/5356 Accuracy, Pulsed RF	_____
4-42.	Rear Panel Outputs	_____
4-43.	GATE OUT	_____
4-44.	PULSE OUT	_____
4-45.	IF OUT	_____
4-49.	HP-IB Verification	_____

Table 4-5. 5355A HP-IB Codes

1. FREQUENCY RANGE SELECT		
0.5-1.6 GHz Input	IS1	
*5356A/B/C RF head Input	IS2	
2. MANUAL MODE SELECT		
*MANUAL OFF (AUTO mode)	ML0	
MANUAL ON	ML1	
3. CW/PULSE MODE SELECT		
*CW mode	CP1	
PULSE mode	CP2	
4. OFFSET MODE SELECT		
*OFFSET off	OT0	
OFFSET on	OT1	
5. OFFSET FREQUENCY ENTRY Carriage return line feed		
OF (Floating point number) CR LF		
(e.g., OF 60.521 E+06 CR LF sets the offset to 60.521 MHz.)		
6. MANUAL FREQUENCY ENTRY		
MF (Floating point number) CR LF		
(e.g., MF 16.4 E+09 CR LF sets the manual frequency to 16.4 GHz.)		
7. SPECIAL FUNCTION MODE		
*SPECIAL FUNCTION OFF	SF1	
SPECIAL FUNCTION ON	SF1	
The definition of special function depends upon whether the 5355A is in PULSE or CW when the SPECIAL FUNCTION is enabled. If in CW mode, then SF1 provides 60 MHz FM tolerance. This would be programmed CP1 SF1. If in PULSE mode, SF1 goes into continuous calibration mode. This is programmed as CP2 SF1.		
8. DIAGNOSTIC DISPLAY	DD	
*NORMAL	DD00	
DIAGNOSTIC MODE 1	DD01	
DIAGNOSTIC MODE 2	DD02	
.....		
.....		
DIAGNOSTIC MODE 12	DD12	
9. *PRESET FUNCTION	PR	
10. READ STATUS	R (See Note 1)	
R causes the 5355A to write a status word into the 5345A display indicating the state of all programmable functions in addition to error codes and diagnostic modes enabled. This status word may also be output from the 5345A to a controller for troubleshooting purposes. Table 3-10 describes the bits in the word.		
11. HOLD AND TRIGGER		
*5345A SAMPLE RATE	FD0	
HOLD	HD1	
TRIGGER (use with HD1, (see Note 1))	T	
The 5345A E9 (HOLD) and J1 (TRIGGER) commands may not be used (are invalid) with the 5355A.		
NOTE		
The 5355A responds to two types of triggers, the T trigger and "Non-T" trigger. The first occurs with program code "T". Non-T triggers occur after a program code set (i.e., N, CP2, R, etc.), a Device Clear or Selected Device Clear command have been sent. Both types of trigger will start a measurement sequence. When in the PRF mode the measurement sequence starts with a calibration cycle consisting of 10 measurements.		

Immediately sets all programmable functions to starred () values.

**PERFORMANCE
CHECK
CON'T**

Table 4-6. Model 9025A Program

```

0: dim C61401;dsp "MODEL 5355A PLUG-IN";wait 2000
1: "code"ent "select code? (2XX)";CONTINUE";5
2: if S=771;dsp "error:calculator address";wait 1000;goto "code"
3: if S>730;dsp "out of address range+high";wait 1000;goto "code"
4: if S<700;dsp "out of address range+low";wait 1000;goto "code"
5: dev "ctr";S;prt "5355A HB-IR TEST";spc 2
6: prt "-----";"CHECK POINT 1";spc 2
7: rem "ctr";beep
8: prt "REMOTE ON","LISTENING ON";spc 2
9: dsp "CHECK POINT 1 COMPLETE";wait 2000
10: dsp "press CONTINUE";stp
11: if L=1;goto 7
12: prt "-----";"CHECK POINT 2";spc 2
13: wrt "ctr","IS2";beep
14: prt "RF HEAD INPUT","ACTIVE";spc 2;wait 5000
15: wrt "ctr","IS1";beep
16: prt "RF HEAD INPUT","INACTIVE"
17: prt "PRESCALE INPUT","ACTIVE";spc 2
18: dsp "CHECK POINT 2 COMPLETE";wait 2000
19: dsp "press CONTINUE";stp
20: if L=1;goto 12
21: prt "-----";"CHECK POINT 3";spc 2
22: wrt "ctr","IS2ML1";beep
23: prt "MANUAL MODE","ACTIVE";spc 2;wait 5000
24: wrt "ctr","ML0IS1";beep
25: prt "MANUAL MODE","INACTIVE"
26: prt "AUTO MODE","ACTIVE";spc 2
27: dsp "CHECK POINT 3 COMPLETE";wait 2000
28: dsp "press CONTINUE";stp
29: if L=1;goto 21
30: prt "-----";"CHECK POINT 4";spc 2
31: wrt "ctr","CP2";beep
32: prt "PULSE MODE","ACTIVE";spc 2;wait 5000
33: wrt "ctr","CP1";beep
34: prt "PULSE MODE","INACTIVE"
35: prt "CW MODE ACTIVE";spc 2
36: dsp "CHECK POINT 4 COMPLETE";wait 2000
37: dsp "press CONTINUE";stp
38: if L=1;goto 30
39: prt "-----";"CHECK POINT 5";spc 2
40: wrt "ctr","QT1";beep
41: prt "OFFSET MODE","ACTIVE";spc 2;wait 5000
42: wrt "ctr","QT0";beep
43: prt "OFFSET MODE","INACTIVE";spc 2
44: dsp "CHECK POINT 5 COMPLETE";wait 2000
45: dsp "press CONTINUE";stp
46: if L=1;goto 39
47: prt "-----";"CHECK POINT 6","ENTER FREQUENCY"
48: prt "OFFSET IN Hz";spc 2
49: ent X;fmt 1,"PROT10F",f.6,wrt "ctr.1",X
50: fxd 6;prt "RECALL OFFSET";spc 1;prt "DOES OFFSET=";X;spc 2

```

Table 4-6. Model 9825A Program (Continued)

```

51: dsp "CHECK POINT 5 COMPLETE";wait 2000
52: dsp "press CONTINUE";stp
53: if L=1;goto 47
54: prt "-----", "CHECK POINT 7", "ENTER MANUAL"
55: prt "CENTER FREQUENCY";spc 2
56: ent Y
57: if Y<1.5;dsp "OUT OF RANGELOW";beep;wait 1000;goto 56
58: if Y>99;dsp "OUT OF RANGEHIGH";beep;wait 1000;goto 56
59: Y*1e9-Y;fmt 2, "PRMLAMP", f.6;wrt "ctr.2", Y
60: fxd 6;prt "RECALL MANUAL", "FREQUENCY";spc 2
61: prt "DOES MANUAL", "CENTER"
62: prt "FREQUENCY=";Y;spc 2
63: dsp "CHECK POINT 7 COMPLETE";wait 2000
64: dsp "press CONTINUE";stp
65: if L=1;goto 54
66: prt "-----", "CHECK POINT 8";spc 2
67: prt "SPECIAL FUNCTION", "MODE";spc 2
68: wrt "ctr", "CPISF1"
69: prt "SPECIAL FUNCTION", "ONE ACTIVE";spc 2;wait 2000
70: wrt "ctr", "PR";prt "SPECIAL FUNCTION", "OFF";spc 2
71: dsp "CHECK POINT 8 COMPLETE";wait 2000
72: dsp "press CONTINUE";stp
73: if L=1;goto 66
74: prt "-----", "CHECK POINT 9";spc 2
75: prt "DIAGNOSTIC MODE", "CHECK";spc 2
76: wrt "ctr", "DD01";wait 5000
77: prt "DIAGNOSTIC CHECK", "COMPLETE";spc 2
78: wrt "ctr", "PR"
79: dsp "CHECK POINT 9 COMPLETE";wait 3000
80: dsp "press CONTINUE";stp
81: if L=1;goto 74
82: prt "-----", "CHECK POINT 10";spc 2
83: prt "READ STATUS", "CHECK";spc 2
84: for I=1 to 25
85: wrt "ctr", "R";wait 500
86: next I
87: wrt "ctr", "PR"
88: prt "STATUS CHECK", "COMPLETE";spc 2
89: dsp "CHECK POINT 10", "COMPLETE";wait 2000
90: dsp "press CONTINUE";stp
91: if L=1;goto 82
92: prt "-----", "CHECK POINT 11";spc 2
93: prt "HOLD & TRIGGER", "CHECK";spc 2
94: wrt "ctr", "HD0";prt "VARY SAMPLE", "RATE";spc 2
95: dsp "press CONTINUE";stp
96: wrt "ctr", "HD1";prt "SAMPLE RATE", "HOLD";spc 2
97: dsp "press CONTINUE";stp
98: for I=1 to 5
99: wrt "ctr", "I";prt "TRIGGER", "MEASUREMENT";spc
100: next I
101: dsp "CHECK POINT 11 COMPLETE";wait 3000
102: prt "END OF TEST";spc 2;stp
*20536

```

Table 4-7. 5355A HP-IB Verification Program Description

At power up: No input signal applied
No frequency converter head connected
CW lamp is on
INPUT SELECT lamp is on (prescale input is active)

NOTE

It is helpful to read each check point description **BEFORE** executing the given check point. This will allow the operator to be in a position to observe the 5355A knowing what action to expect.

CHECK POINT 1: REMOTE

After entering device code and pressing CONTINUE on 9825A, observe that the REMOTE and LISTENING lamps are on. The CW and INPUT SELECT lamps will still be on. The calculator will print a message of the test. Press CONTINUE.

CHECK POINT 2: FREQUENCY RANGE SELECT

After pressing CONTINUE, observe that the INPUT SELECT lamp goes off, indicating that the RF HEAD INPUT is active (approximately 5 seconds). Then observe that the INPUT SELECT lamp will again be on, indicating that the prescale input is again active. The calculator will print a message to this effect. Press CONTINUE.

CHECK POINT 3: MANUAL MODE SELECT

After pressing CONTINUE, observe that the MANUAL MEASUREMENT lamp is on (approximately 5 seconds). Note that the INPUT SELECT lamp will be off, as manual measurements are only relevant in the RF head input position. The MANUAL MEASUREMENT lamp will go out, and the 5355A will again be in the AUTOMATIC measurement mode. Also note that the INPUT SELECT lamp is again on, indicating a message of these events. Press CONTINUE.

CHECK POINT 4: CW/PULSE MODE SELECT

After pressing CONTINUE, observe that the PULSE MODE lamp is on and the CW lamp has gone off (approximately 5 seconds). The CW lamp will again be on, and the PULSE lamp will be off. The INPUT SELECT lamp will also be on. The calculator will print a message to this effect. Press CONTINUE.

CHECK POINT 5: OFFSET MODE SELECT

After pressing CONTINUE, observe the OFFSET lamp on (approximately 5 seconds). Then, the OFFSET lamp will go out, INPUT SELECT and CW lamps will stay on. Calculator will print a message of the test. Press CONTINUE.

CHECK POINT 6: OFFSET FREQUENCY ENTRY

After pressing CONTINUE, the calculator will print: "ENTER FREQUENCY OFFSET IN HZ." Enter the offset desired, in Hz. The use of exponents is approved, such as 1e9 for 1 GHz. Input range for this mode is 1e-6 to 999e9 Hz. Press CONTINUE after the entry. The 5355A should have its REMOTE, LISTENING, CW and OFFSET MEASUREMENT lamps on.

The calculator will then print "RECALL OFFSET", and will also print the offset value entered. To check that the offset entered truly was received by the 5355A, press the BLUE key to put the display of the 5345A. Note that the REMOTE lamp on the 5355A was extinguished when placed into LOCAL mode. Press CONTINUE.

Table 4-7. 5355A HP-IB Verification Program Description (Continued)

CHECK POINT 7: MANUAL FREQUENCY ENTRY

After pressing CONTINUE, the calculator will print "ENTER MANUAL CENTER FREQUENCY". The entry should be a number between 1.5 and 99.0. The calculator will format this into a Gigahertz entry frequency. Press CONTINUE.

The calculator will then print "RECALL MANUAL FREQUENCY", and will also print the frequency entered. To check that the manual frequency entered was received by the 5355A, press the BLUE and then the YELLOW key on the 5355A. The entered manual center frequency should appear on the display of the 5345A.

NOTE 1.

The program commands the 5355A to RF HEAD INPUT mode, as manual mode center frequencies are only relevant in this mode. The INPUT SELECT lamp will be out.

NOTE 2.

The range of manual center frequencies is 1.5 to 99.0 GHz. Exceeding this range will cause the calculator to display an error message. Simply re-enter the proper frequency. Press CONTINUE.

CHECK POINT 8: SPECIAL FUNCTION MODE

NOTE

To test this function, apply a CW input to the RF head input via one of the frequency converter heads: 5356A, 5356B, or 5356C. An input is necessary to cause the 5355A to go into the special function mode.

After pressing CONTINUE on the calculator, observe the CW key lamp blink slowly. This indicates that the CW special function of 60 MHz FM tolerance is active. This will occur for approximately 10 seconds. The program will then turn off the special function. Press CONTINUE.

CHECK POINT 9: DIAGNOSTIC DISPLAY

The diagnostic modes capability of the 5355A can be utilized via HP-IB. To check this function, only the first diagnostic will be programmed. This diagnostic allows the operator to view the 5355A synthesizer frequency on the display of the 5345A. Other diagnostic codes may be inserted into the HP-IB verification program if so desired.

Apply a CW input signal to the 5356 head. After pressing CONTINUE, observe on the 5345A display of 5355A synthesizer frequency between 805.2 and 1052.8 MHz. The displayed frequency is dependent upon the input frequency applied.

The display will remain for approximately 5 seconds, after which it will be reset by the calculator. Press CONTINUE.

CHECK POINT 10: READ STATUS CHECK

The status of the 5355A can be read via HP-IB. Normally, it is read to the calculator via the 5345A for a system check of the 5355A. However, this program provides a software loop whereby the status is checked and displayed 25 times so that it is visible on the 5345A display. An input is not necessary. Actual interpretation of the status word is available in Table 3-10. After pressing CONTINUE, observe the status word displayed on the 5345A. This will continue for approximately 10 seconds. At the end of the program loop, the input frequency will again be displayed, if one is applied. Press CONTINUE.

CHECK POINT 11: HOLD AND TRIGGER

Apply a CW input via the 5356 head. After pressing CONTINUE, the calculator will print "VARY SAMPLE RATE". Manually adjust the SAMPLE RATE knob on the 5345A to see that it actually has an effect. The program is stopped at this point to allow time to make this check. When satisfied, press CONTINUE.

After pressing CONTINUE, the calculator will print "SAMPLE RATE HOLD". Manually adjust the SAMPLE RATE knob on the 5345A and observe that it has NO effect. The program is stopped at this point to allow time to make this check. When satisfied, press CONTINUE.

After pressing CONTINUE, the calculator will command 5 triggered measurements, and print a message to this effect. After this is complete, the 5355A will be in hold.

This completes the 5355A HP-IB verification test.

Table 4-8. Sample Printout

5355A RB-10 TEST	

CHECK POINT 1	CHECK POINT 4
REMOTE ON	PULSE MODE
LISTENING ON	ACTIVE

CHECK POINT 2	PULSE MODE
	INACTIVE
	CW MODE ACTIVE
RF HEAD INPUT	
ACTIVE	-----
	CHECK POINT 5
RF HEAD INPUT	
INACTIVE	OFFSET MODE
PRESCALE INPUT	ACTIVE
ACTIVE	

CHECK POINT 3	OFFSET MODE
	INACTIVE
MANUAL MODE	-----
ACTIVE	CHECK POINT 6
	ENTER FREQUENCY
	OFFSET IN Hz
MANUAL MODE	
INACTIVE	RECALL OFFSET
AUTO MODE	
ACTIVE	DOES OFFSET:
	1.0000000000e 00
-----	-----

Table 4-8. Sample Printout (Continued)

CHECK POINT 7	CHECK POINT 10
ENTER MANUAL CENTER FREQUENCY	READ STATUS CHECK
RECALL MANUAL FREQUENCY	STATUS CHECK COMPLETE
DOES MANUAL CENTER FREQUENCY=	-----
2.000000000e 09	CHECK POINT 11
-----	HOLD & TRIGGER CHECK
CHECK POINT 8	VARY SAMPLE RATE
SPECIAL FUNCTION MODE	SAMPLE RATE HOLD
SPECIAL FUNCTION ONE ACTIVE	TRIGGER MEASUREMENT
SPECIAL FUNCTION OFF	TRIGGER MEASUREMENT
-----	TRIGGER MEASUREMENT
CHECK POINT 9	TRIGGER MEASUREMENT
DIAGNOSTIC MODE CHECK	TRIGGER MEASUREMENT
DIAGNOSTIC CHECK COMPLETE	TRIGGER MEASUREMENT
-----	END OF TEST

ADJUSTMENTS

SECTION V ADJUSTMENTS

5-1. INTRODUCTION

5-2. This section describes the adjustments required to maintain operating characteristics within specifications. Adjustments should be made when required, such as after an operational verification or performance test failure, or when components are replaced that may affect an adjustment. For complete realignment, follow the sequence listed below:

Assembly	Adjustment	Paragraph
A5 DC Amplifier/Compensator	Loop Gain	5-12
	Filter Tuning Voltage	5-13
	Pseudorandom Modulator	5-14
A2 IF Amplifier	Amplifier DC Current Balance	5-17
	Gain versus Frequency	5-18
	AGC Diode Bias	5-19
A3 Filter/Detector	Amplifier Balance	5-22
A11 Signal Switch	Bias 1	5-27
	Bias 2	5-28
A6 Prescaler	Binary Bias and Hysteresis	5-32
	Arming Circuit	5-33
	AGC Bias, AGC Level and LV AGC	5-34
	PRS Gate	5-35

5-3. EQUIPMENT REQUIRED

5-4. The test equipment required for the adjustment procedures is listed in *Table 1-3, Recommended Test Equipment*. Substitute Instruments may be used if they meet the critical specifications.

5-5. ADJUSTMENT LOCATIONS

5-6. Adjustment locations are identified in the component locators in Section VIII, Schematic Diagrams and in the top view of the 5355A, *Figure 8-24*.

5-7. SAFETY CONSIDERATIONS

5-8. This section contains warnings and cautions that must be followed for your protection and to avoid damage to the equipment.

WARNING

MAINTENANCE DESCRIBED HEREIN IS PERFORMED WITH POWER SUPPLIED TO THE INSTRUMENT, AND PROTECTIVE COVERS REMOVED. SUCH MAINTENANCE SHOULD BE PERFORMED ONLY BY SERVICE-TRAINED PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED (FOR EXAMPLE, FIRE AND ELECTRICAL SHOCK). WHERE MAINTENANCE CAN BE PERFORMED WITHOUT POWER APPLIED, THE POWER SHOULD BE REMOVED.

BEFORE ANY REPAIR IS COMPLETED, ENSURE THAT ALL SAFETY FEATURES ARE INTACT AND FUNCTIONING, AND THAT ALL NECESSARY PARTS ARE CONNECTED TO THEIR PROTECTIVE GROUNDING MEANS.

5-9. ADJUSTMENT PROCEDURES

NOTE

If complete realignment is to be performed, follow the sequence of adjustments as listed here. This is to ensure that each circuit assembly provides the proper signals for those following. The sequence of adjustments is A5 first, followed by A2, A3, A11, and A6.

Circuit assemblies may be individually realigned, but the technician is cautioned to check the assembly that provides signals if the assembly under adjustment will not respond properly.

After performing adjustments, conduct the applicable performance tests in Section IV.

CAUTION

The power switch on the 5345A counter must be in **STANDBY** position during removal or installation of PC assemblies.

5-10. A5 DC Amplifier/Compensator Assembly

5-11. The following adjustments are provided for the A5 assembly:

- a. Loop gain
- b. Filter tuning voltage
- c. Pseudorandom modulator

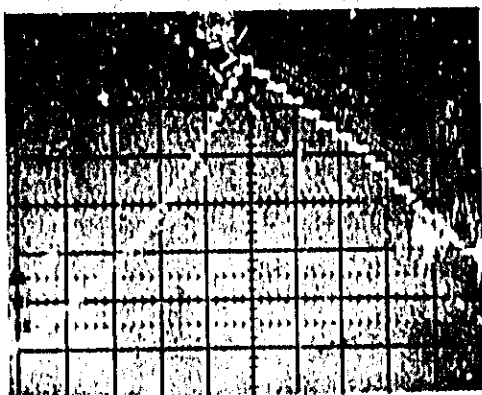
5-12. LOOP GAIN. Perform these adjustments:

- a. Set up the test equipment as shown in *Figure 5-1*. Connect a converter head to the 5355A but do not apply an input signal. Turn on the 5345A. The 5355A should power up in the automatic and CW modes.

NOTE

Do not use a 5356B Option 001 head when performing this adjustment. If this is the only head available, disconnect the head from the plug-in and jumper A8, pin 24 to ground. This can also be accomplished by grounding the RFC1 pin on the front panel multipin connector (see A13 theory of operation for plug pin wiring).

- b. Adjust the oscilloscope (connected to A5TP5) to display a staircase ramp as shown in the photo below. Use NORM sweep, + slope for scope triggering. Set sweep time to 10 ms/div. and amplitude to 0.1V/div. Set 1120A active probe to DC coupling and - OFFSET. Adjust OFFSET control and scope vertical position to center the display as shown below.



Horiz: .01 s/div., sweep "main"
EXT TRIGGER, ac coupled, 1 meg probe
LF reject ON
AUTO/NORM in NORM
Vert: .1V/div., with 1120A active probe in use.

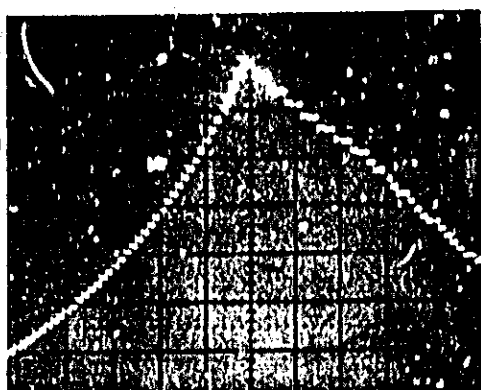
NOTE

If A5R2 and A5R7 are too far off normal adjustment, the waveform will not be as shown. Adjust these pots as necessary to show waveform.

NOTE

The scope triggering adjustments for this procedure are very sensitive. Proceed slowly to get the best results. As the vertical deflection factor is increased, the display may move off the screen. Use the 1120A OFFSET control to restore the display. If not successful, go back to the starting point, as triggering was probably lost.

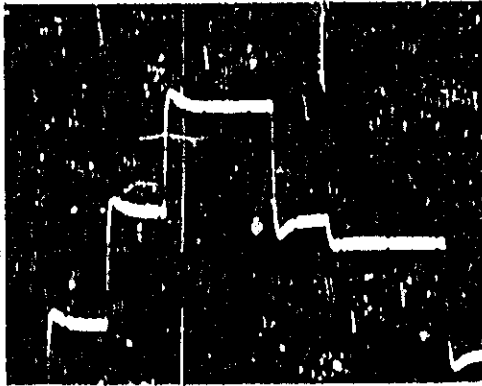
- c. Set up the oscilloscope to expand the step b view. Set SWEEP MODE to MAIN INTEN and DELAYED TIME/DIV to 1 ms. Using DELAY vernier, position intensified portion of display at peak of waveform, as shown below. Adjust INTENSITY for best contrast.



Horiz: .01 s/div., sweep mode "main intensity"
Delay Time/div., 1 ms/div.
Delay Time Vernier - Position bright portion on peak.
Vert: .1V/div., with 1120A active probe in use.

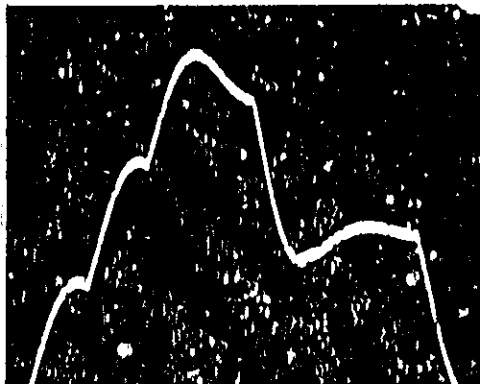
Model 5355A
Adjustments

- d. Set scope SWEEP MODE to DELAYED to expand intensified part of display. Adjust vertical deflection factor, vertical position on scope and OFFSET on 1120A for centered display. Adjust to show peak of overall waveform as shown below.



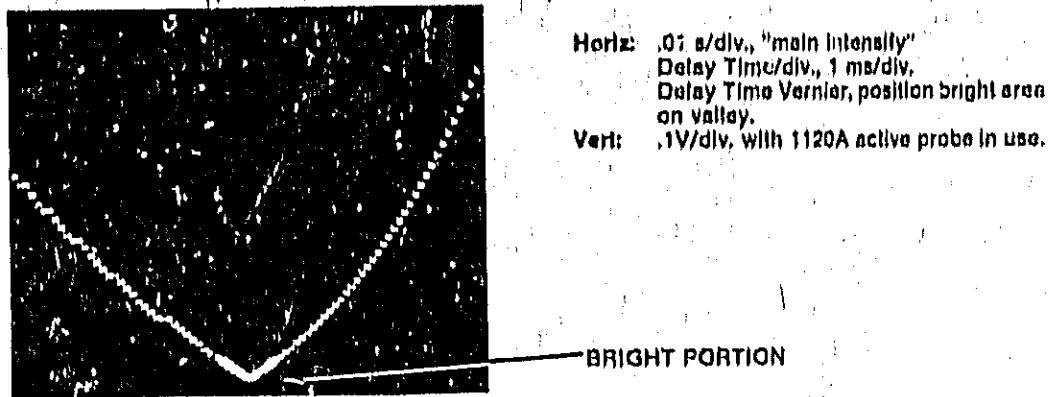
Horiz: Sweep mode "Delayed"
.01 s/div., main
1 ms/div., delayed
Vert: .01V/div., 1120A active probe in use.

- e. Set A5R7 (GAIN H) to midrange.
f. Set the VCO to sweep in the low gain mode by simultaneously pressing the 5355A MAN FREQ and OFFSET FREQ keys until the numbers on the 5345A display advance to 0000 0000.
g. Adjust A5R2 (GAIN L) for display shown below, or as close as possible.

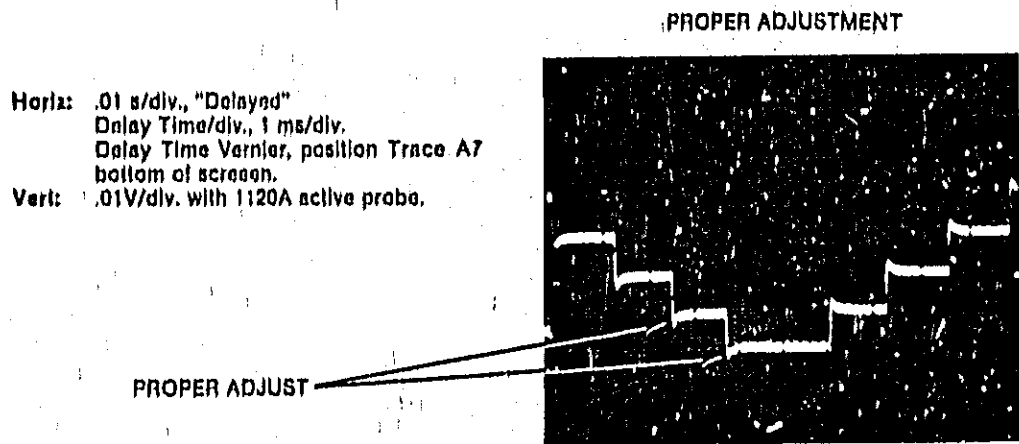


Horiz: Sweep mode "Delayed"
.01 s/div., main
1 ms/div., delayed
Vert: .01V/div., 1120A active probe in use.

h. Set up the scope to view bottom of overall waveform as shown below.



i. To ensure that the high gain circuits can be switched in properly, simultaneously press the 5355A MAN FREQ and OFFSET FREQ keys one time. The 5345A display will advance to If the circuit has advanced to the high gain mode, the display should change from the waveform shown in the previous step to one similar to that shown below. Adjust A5R7 to match the display below.



The following photo shows improper adjustment.

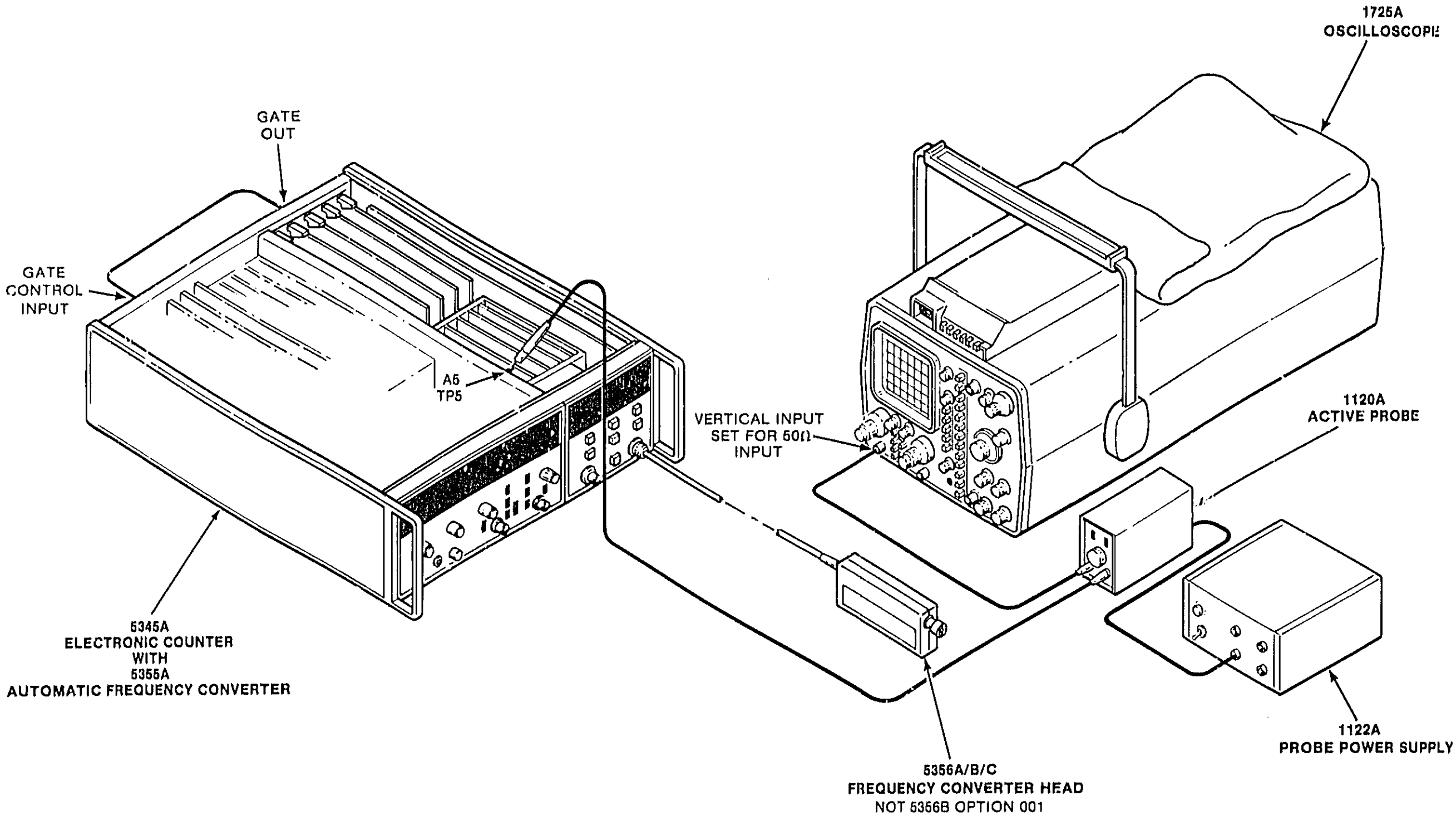
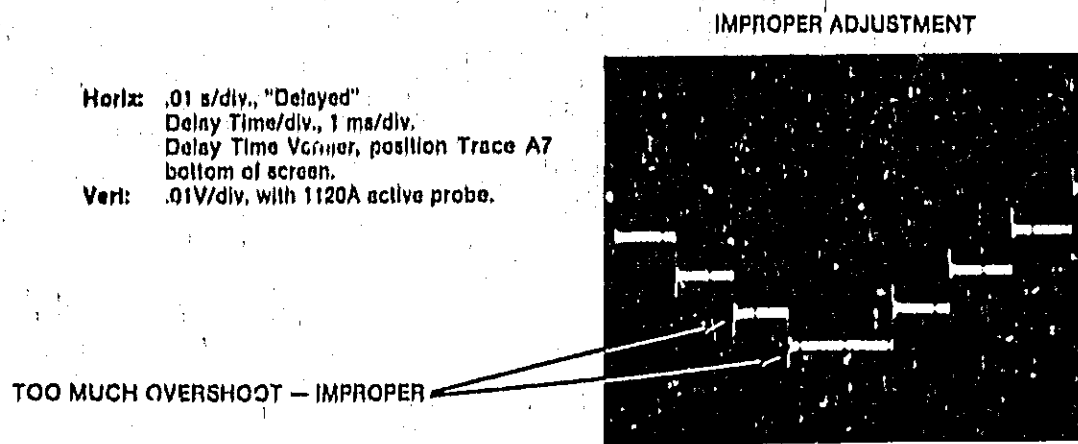


Figure 5-1. A5 Gain Adjustment Setup

- 5-13. FILTER TUNING VOLTAGE. Perform the filter tuning voltage adjustments as follows:
- a. Connect the test equipment as shown in *Figure 5-2*. The maximum voltage to be measured is 15 volts. Adjust the multimeter accordingly.
 - b. Turn the 5345A on and after power-up reset, press the 5355A MANUAL MEASUREMENT key. The 5345A should display 1.5 GHz for about 1 second and then display all zeros.

NOTE

At 1.5 GHz, the VCO frequency is 885.2 MrHz. The frequency counter connected to A14J8 will verify this.

CAUTION

The power level at A14J8 is about +13 dBm. Use a 10 dB attenuator in series with the 50 Ω input to the HP Model 5340A shown in *Figure 5-2*.

- c. On A5 board, turn R15 (FILT-AMP) fully counterclockwise and R14 (FILT-LEVEL) fully clockwise.
- d. Press the 5355A MAN FREQ DATA ENTRY key to set the manual frequency to 1.9 GHz. Press the MAN FREQ key again to return to the manual measurement mode. The VCO should move to 1056.0 MHz. The dc voltage at TP4 should be greater than +12V.

NOTE

The VCO will not change to the new frequency while in the DATA ENTRY mode and must be returned to the manual measurement mode by pressing the MAN FREQ key a second time. The VCO will then move to the desired frequency.

- e. Press the MAN FREQ DATA ENTRY key and set the manual frequency to 1.5 GHz. Press key a second time to return to manual measurement mode.
- f. Adjust R15 (FILT-LEVEL) to get +5 (± 0.2)V at TP4.
- g. Press the MAN FREQ DATA ENTRY key and set the manual frequency to 1.9 GHz. Press key a second time to return to manual measurement mode.
- h. Adjust R15 (FILT-AMP) to get +12 (± 0.5)V at TP4.
- i. Repeat steps e through h until the correct voltages are obtained.

NOTE

Table 5-1 contains the representative values for the other manual frequencies.

Table 5-1. Representative Values for 5355A Manual Frequencies

Manual Frequency	VCO Frequency	VCO Control Voltage* (A5TP5)	Filter Tuning Values (A5TP4)
1.5 GHz	885.2 MHz	2.0V	5.0(± 0.2)V
1.6 GHz	922.0 MHz	2.8V	5.6V*
1.7 GHz	972.0 MHz	3.6V	6.9V*
1.8 GHz	1022.0 MHz	7.9V	9.3V*
1.9 GHz	1056.0 MHz	11.8V	12.0(± 0.5)V

* These voltages are approximate.

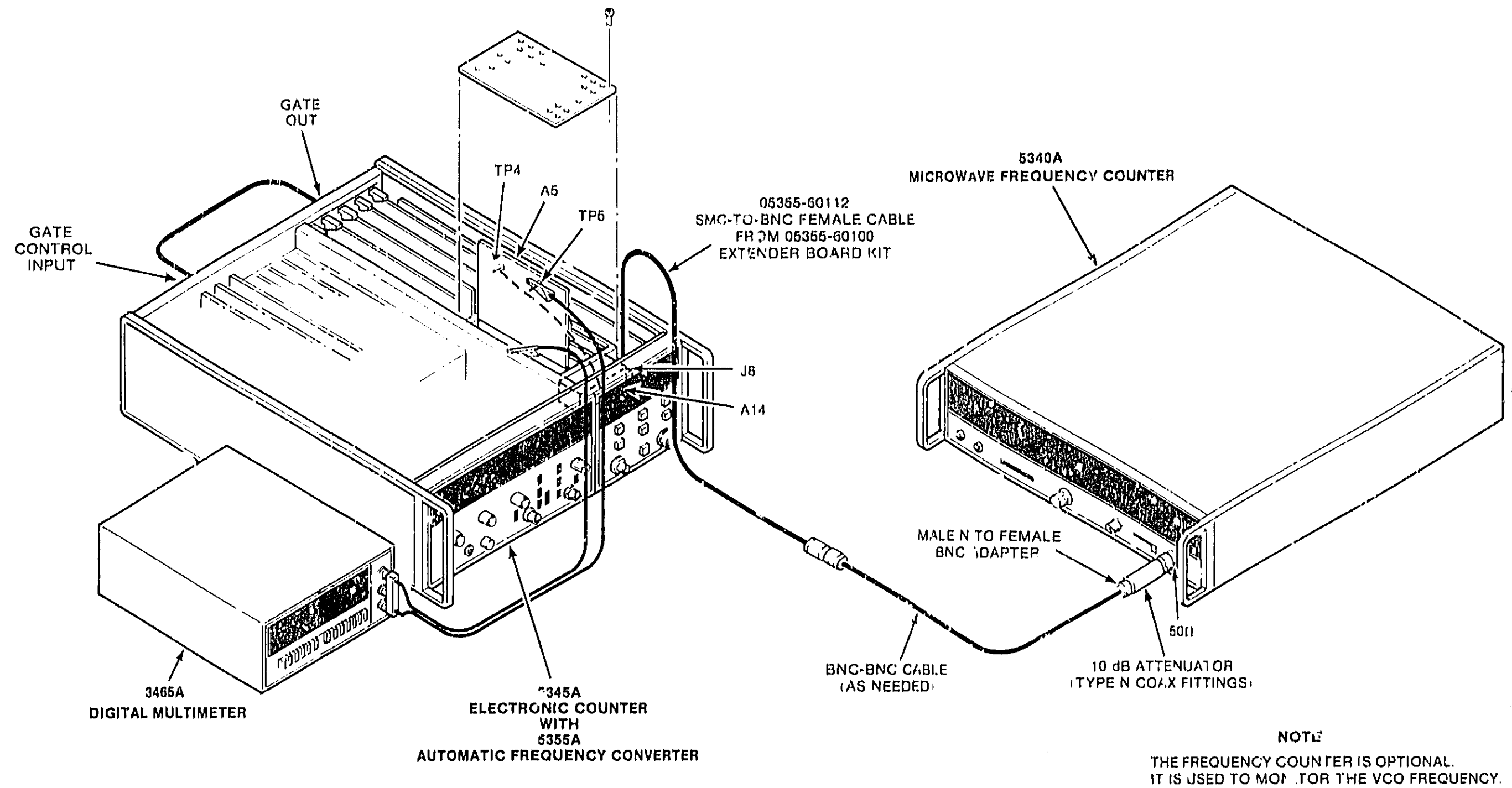


Figure 5-2. A5 Filter Tuning Adjustment Setup

5-14. PSEUDORANDOM MODULATOR. Perform the pseudorandom modulator adjustments as follows:

- a. Connect the test equipment as shown in Figure 5-3.

NOTE

Use a short (less than 6 inches) clip lead to ground A10TP4. Minimum inductance is needed at this point. This allows a continuous PRS (pseudorandom sequence).

- b. Connect the output of A14JB to the spectrum analyzer. Set up the spectrum analyzer as follows:

INPUT ATTENUATOR 40 dB
REF LEVEL 20 dBm
AMPLITUDE SCALE 10 dB/div
FREQUENCY SPAN 1 MHz/div
RESOLUTION B/W 300 kHz
VIDEO FILTER OFF
SWEEP TRIGGER FREERUN
SWEEP TIME AUTO
Set the TUNING FREQUENCY to 1.056 GHz.

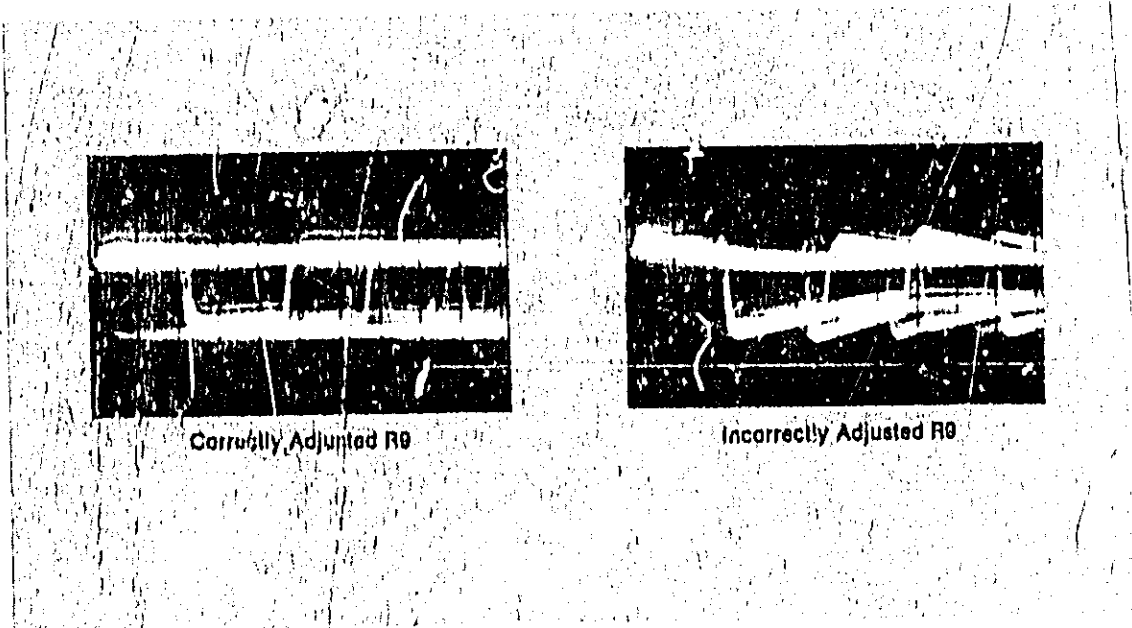
- c. Turn 5345A POWER switch to ON. (If counter is already on, it must be turned off and on again before proper routine can be entered.)
- d. Center the signal on the display of the spectrum analyzer. The display should appear similar to the photo below, assuming A5R9 (TILT) and A5RB (AMPL) are set reasonably close to their final positions (approximately midrange).



Signal from A14JB (1 MHz/div.)

- e. With oscilloscope connected to A5TP5, adjust the oscilloscope trigger properly for the cleanest presentation. The displayed signal will not trigger properly because of the pseudorandom action. Oscilloscope settings: 0.02V/div., ac coupled, 5 μ s/div.

1. Adjust A5R9 (TILT) to remove any tilt in the wave-shape as shown in the photo below.



2. Adjust A5R8 (AMPL) for a 4 MHz wide display on the spectrum analyzer as shown in the photo below.

NOTE

Oscilloscope display will change once A5R8 is adjusted. Repeat adjustments until both are correct.

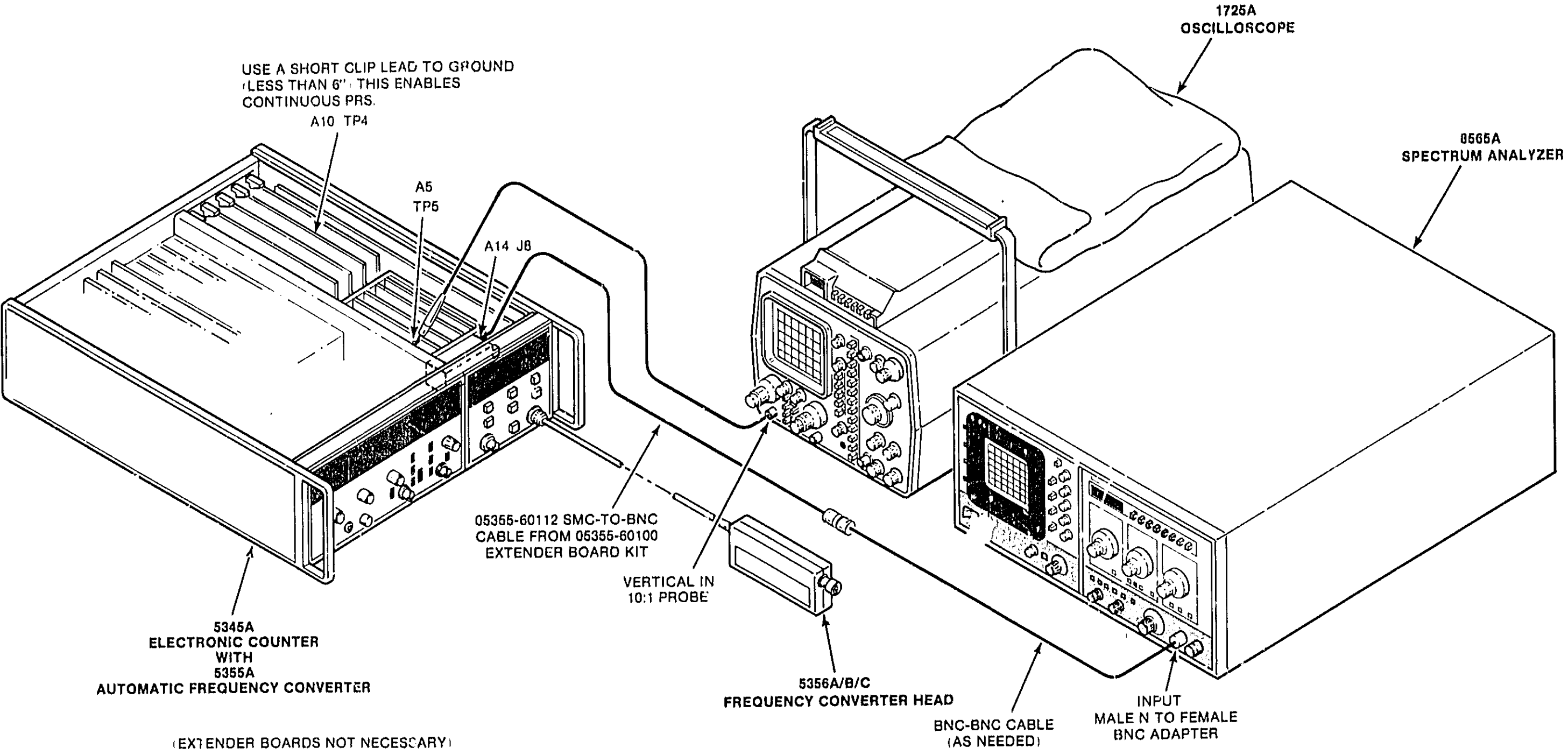
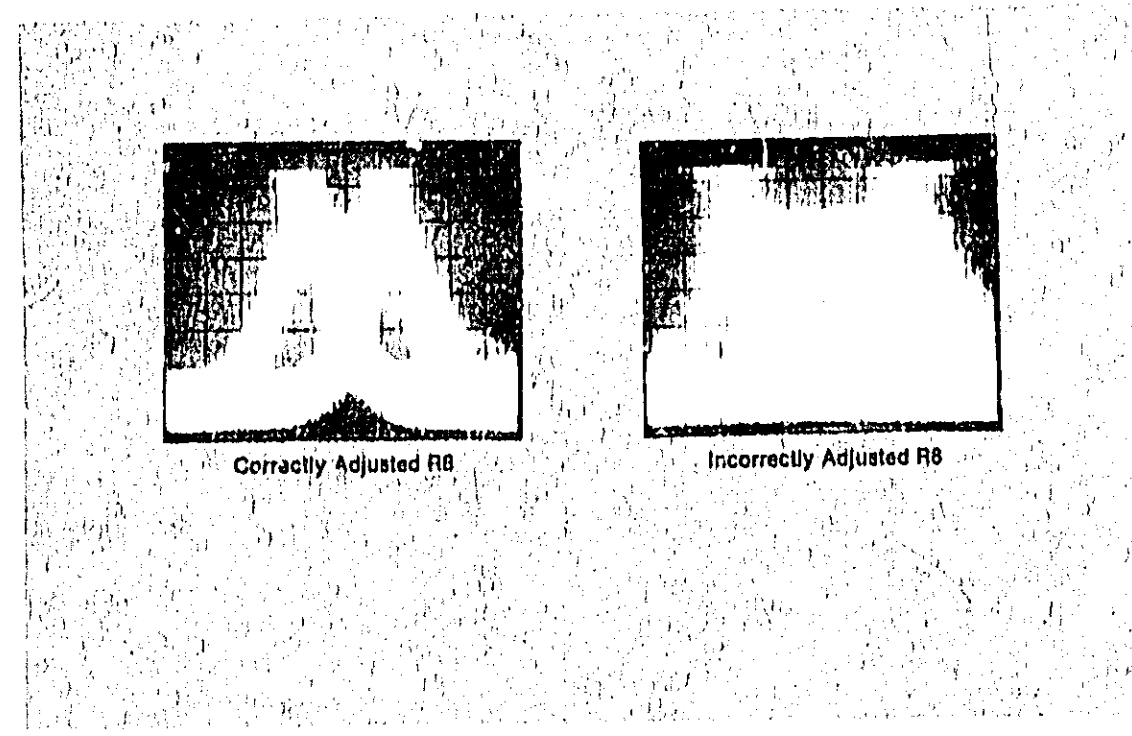


Figure 5-3. A5 Pseudorandom Modulator Adjustment Setup

5-15. A2 IF Amplifier Assembly

5-16. Adjustment of the A2 assembly is performed in three major steps, each requiring a unique test equipment configuration. These configurations are shown at the beginning of each step. Perform the steps in the following order:

- a. Amplifier dc current balance
- b. Gain versus frequency
- c. AGC diode bias.

5-17. AMPLIFIER DC CURRENT BALANCE. Adjust the amplifier dc current balance as follows:

CAUTION

The power switch on the 5345A counter must be in the STBY position during removal or installation of PC assemblies.

CAUTION

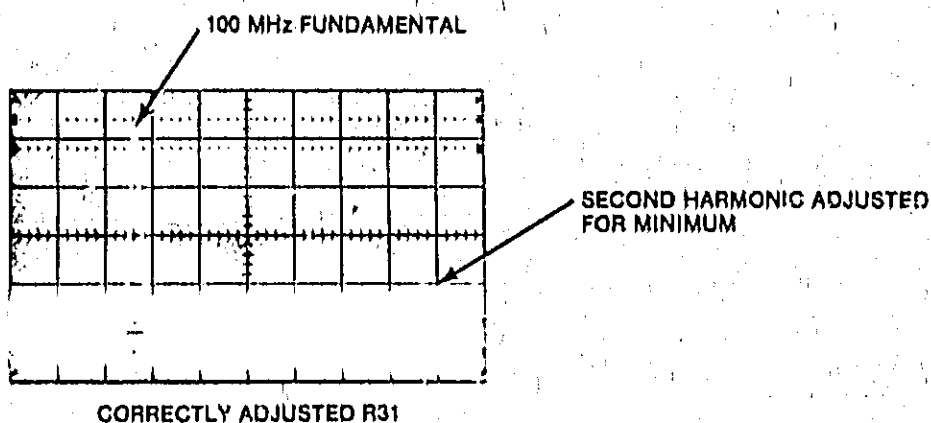
Remove both the A2 and A3 assemblies together being careful not to damage the rigid coax interconnector located at the upper rear corners of the two assemblies.

- a. Remove the interconnector and reinstall the assemblies with A2 on an extender board.
- b. Connect the test equipment as shown in Figure 5-4.
- c. Set the 8640B to 0 dBm at 100 MHz with no modulation.
- d. Using a 20:1 divider probe (HP 10020A), connect the spectrum analyzer to display both the 100 MHz fundamental and the 200 MHz second harmonic.

NOTE

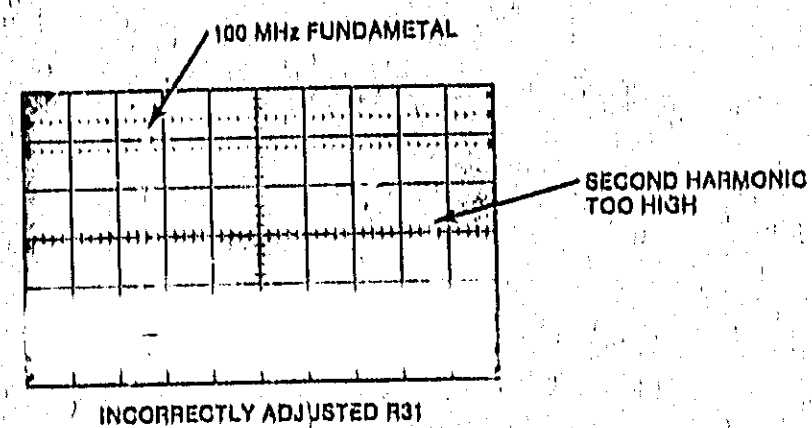
At this point, set the AGC adjustment control (A2R24) fully counterclockwise and make sure the 5355A is in the CW mode.

- e. While observing the 200 MHz second harmonic on the spectrum analyzer, adjust variable resistor A2R31 (AMP) for a minimum 200 MHz signal as shown below:



NOTE

The photo below illustrates an example of a misadjusted A2R31 (AMP) control.



- f. Move the test probe from TPA to TPB. Adjust the 8640B from 0 dB to -10 dB.
- g. Adjust variable resistor A2R23 (AMP 2) for a minimum 200 MHz signal as observed on the spectrum analyzer.
- h. Move the test probe from TPB to IF output jack J2. Adjust the 8640B from -10 dB to -20 dB.
- i. Adjust variable resistor A2R18 (AMP 3) for a minimum 200 MHz signal as observed on the spectrum analyzer.

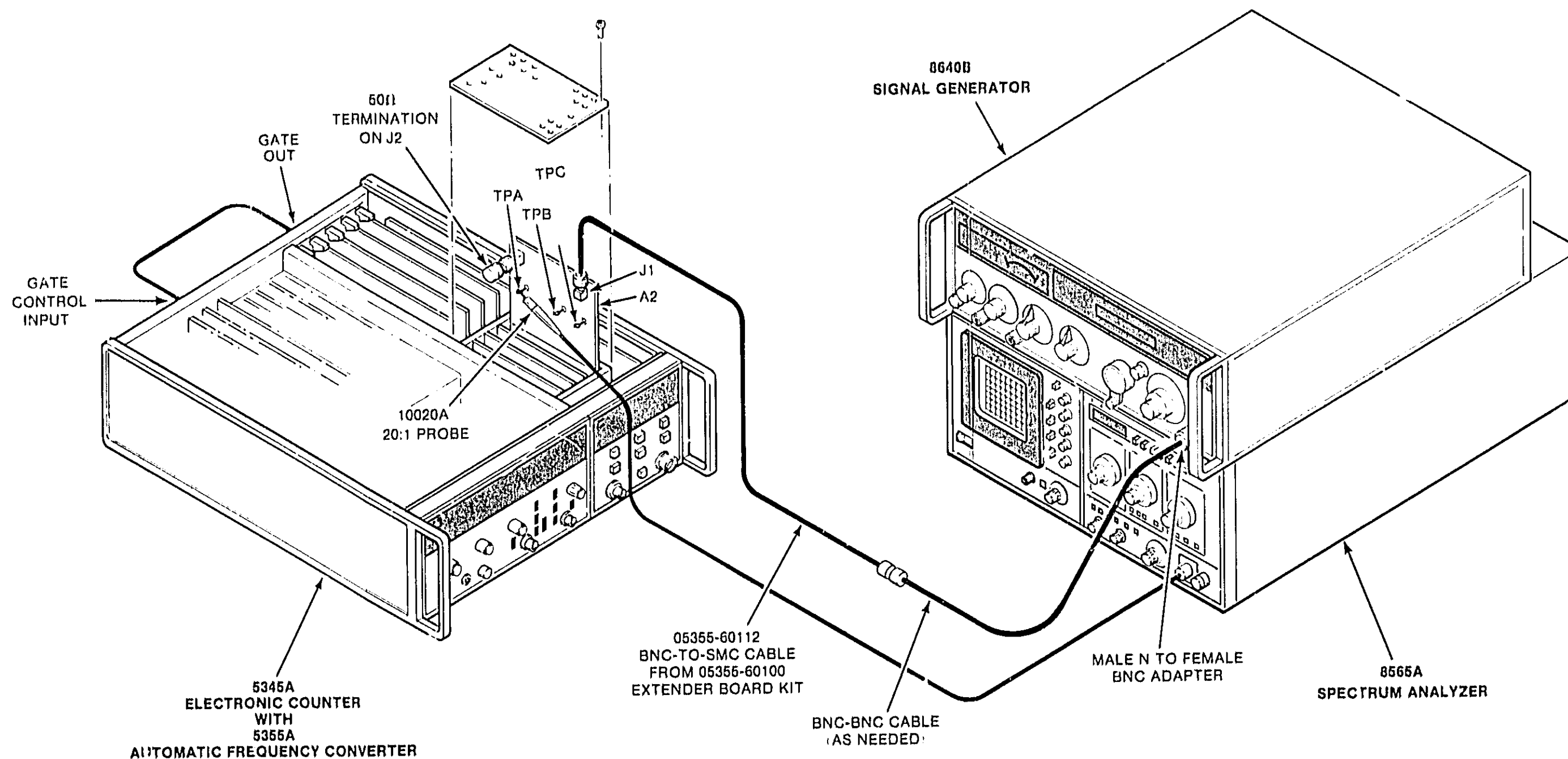


Figure 5-4. Amplifier DC Current Balance Adjustment Setup

5-10. GAIN VERSUS FREQUENCY. Perform the gain versus frequency adjustment as follows:

- a. Perform step a in paragraph 5-17.
- b. Connect the test equipment as shown in *Figure 5-5*.

NOTE

The power supply connected to A5TP4 should be adjusted to $12V \pm 300 \text{ mV}$. (This applies a constant voltage to the IF tuning filter.) The current should be monitored and should not exceed 40 mA. On the rear panel of the 8620 Sweeper, set the DISPLAY BLANKING to ON and the RF BLANKING to OFF.

- c. Set the oscilloscope for external horizontal input. Adjust the oscilloscope external vernier for a full screen display, while adjusting the sweeper output from 100 MHz to 1 GHz.
- d. Set the sweeper's sweep time to the .1 to 1 second position and the vernier to full clockwise.
- e. Perform the following numbered steps to calibrate the setup:

1. Disconnect the BNC-to-SMC test cable between the power splitter and A2J1. Connect the 436A power meter to the splitter output. Disconnect the 11665B modulator drive cable.
2. Set the sweeper to 500 MHz in the CW mode. With the step attenuator set to 0 dB, adjust the sweeper output to 0 dBm.
3. Reconnect the BNC-to-SMC test cable and the 11665B modulator. Disconnect the two test cables from the A2 assembly and join them together with an SMC barrel. Set the sweeper to SWEEP mode and ensure the attenuator is set to 0 dB.
4. Adjust the 8755A Sweep Analyzer Channel A as follows:

OFFSET dB 00
dB/div 10
DISPLAY A/R

SET THE OFFSET dB switch to ON and adjust the VERNIER to center the trace on the screen. This is the zero dB reference line. Do not move the VERNIER after this adjustment.

5. Set the marker switch on the 8620 Sweeper to INTEN. A bright spot or marker should appear on the sweep analyzer display. Adjust 102C oscilloscope Intensity for best viewing.
6. Disconnect the test cable from the output of the power splitter and connect it to Channel A of the 5345A. Set the 5345A FUNCTION switch to FREQ A and the GATE TIME switch to 10 μs . Disconnect the 11665B modulator drive cable. Set the 8620 Sweeper to CW, adjust the step attenuator setting for the 5345A counter response and using the sweeper CW control, adjust the marker frequency to 525 MHz. This is above the 5345A maximum frequency specification. However, the 5345A will generally count this frequency. If not, use another counter (5340A, 5342A).
7. Disconnect the test cable from the counter and reconnect it to the power splitter. Reconnect the modulator drive cable.
8. Reconnect the test cables to A2 input (J1) and output (J2). On the 5355A, press the MANUAL (MEASUREMENT) switch (not the manual data entry).

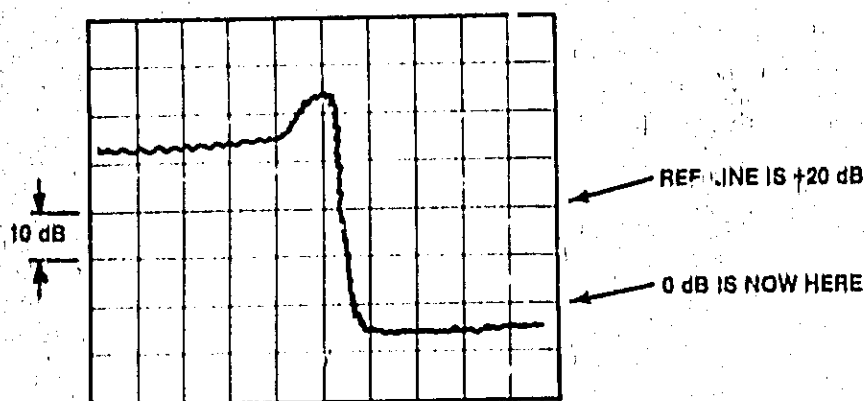
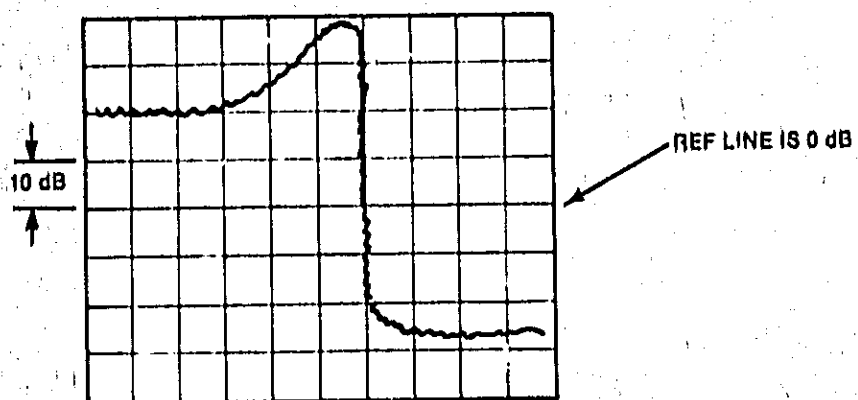
9. Adjust the power supply output to $+12V \pm 300 \text{ mV}$ (at A5TP4). Set the step attenuator to 40 dB.
10. Adjust the 8755A analyzer OFFSET dB thumbwheel switch to +20. The reference line now is 20 dB above its previous value, which was zero dB. See example below.

NOTE

Do not move the OFFSET CAL knob, as this will destroy the reference calibration.

NOTE

These illustrations are for example only, to show movement of reference line.



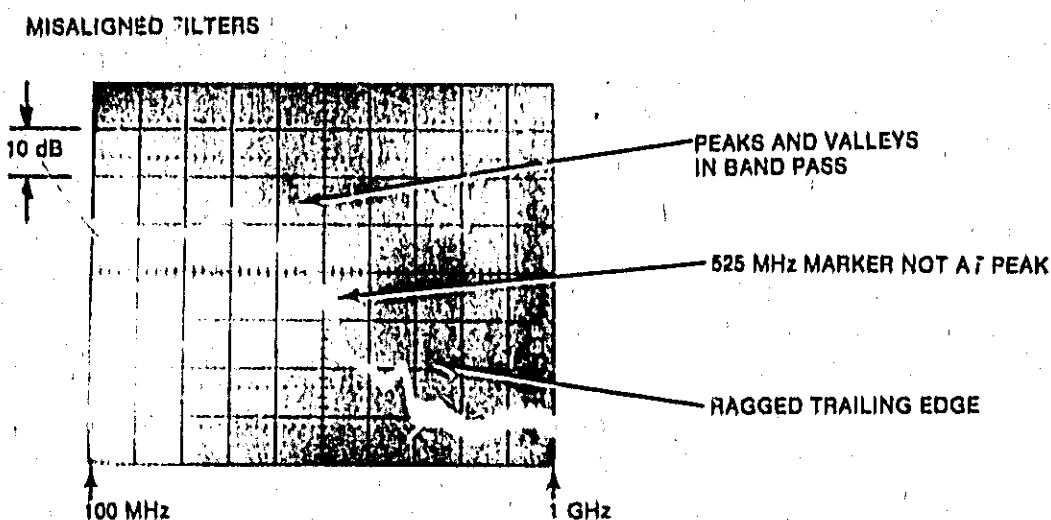
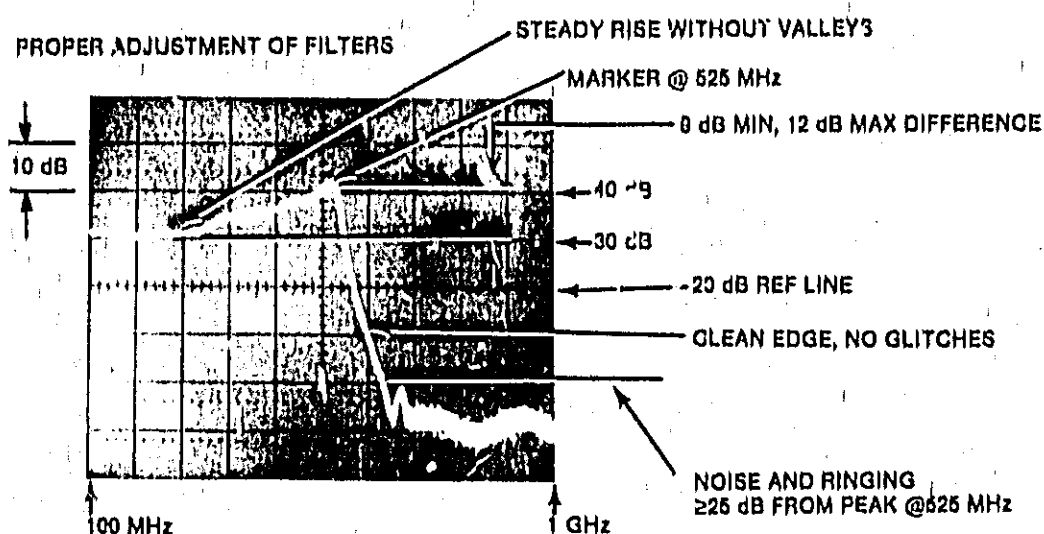
- f. Adjust F1(R35), F2(R36), F3(R40), and C10 for a sharp cutoff as shown in the photos below. Adjustments should be rechecked as they are interactive.

NOTE

If necessary, adjust the turn spacing or number of turns on A2L1, L2 and L3 to get the response needed. Start with L1. (Number of turns may be easily adjusted by soldering turns together.)

Gain Check:

The 8755A Sweep Analyzer should indicate a signal $\geq +29$ dB at 50 MHz and $\geq +41$ dB at 525 MHz (marker). The peaking should be between 9 and 12 dB. These levels are referenced to the reference set in step e4 and as offset in step e10.



- g. Using the procedure outlined in steps e6 and e7, set the marker from 525 MHz to 490 MHz.

- h. Set the 8755A Sweep Analyzer to 5 dB/div. Lower the output of the variable power supply until the 490 MHz marker drops 1 dB.

Test Limit:

The supply voltage should be between +5 and +11 volts.

- i. Using the procedure outlined in steps e6 and e7, set the marker from 490 MHz to 450 MHz.

- j. Adjust the output of the variable power supply until the marker drops 3 dB.

Test Limit:

The supply voltage should be between +4.5 and +8 volts.

NOTE

If these limits cannot be obtained, recheck the overall gain and if necessary readjust F1, F2, F3 and C1B, per step f

- k. Press the PULSE (MEASUREMENT) switch on the 5355A. Using the procedure outlined in steps e6 and e7, set the marker from 450 MHz to 375 MHz.

- l. Adjust variable resistor R43(PRF) to peak the sweep analyzer display at 375 MHz. Set 8755A for 5 dB/div for better resolution.

After the signal is peaked, readjust R43 to drop the 375 MHz marker 1 dB.

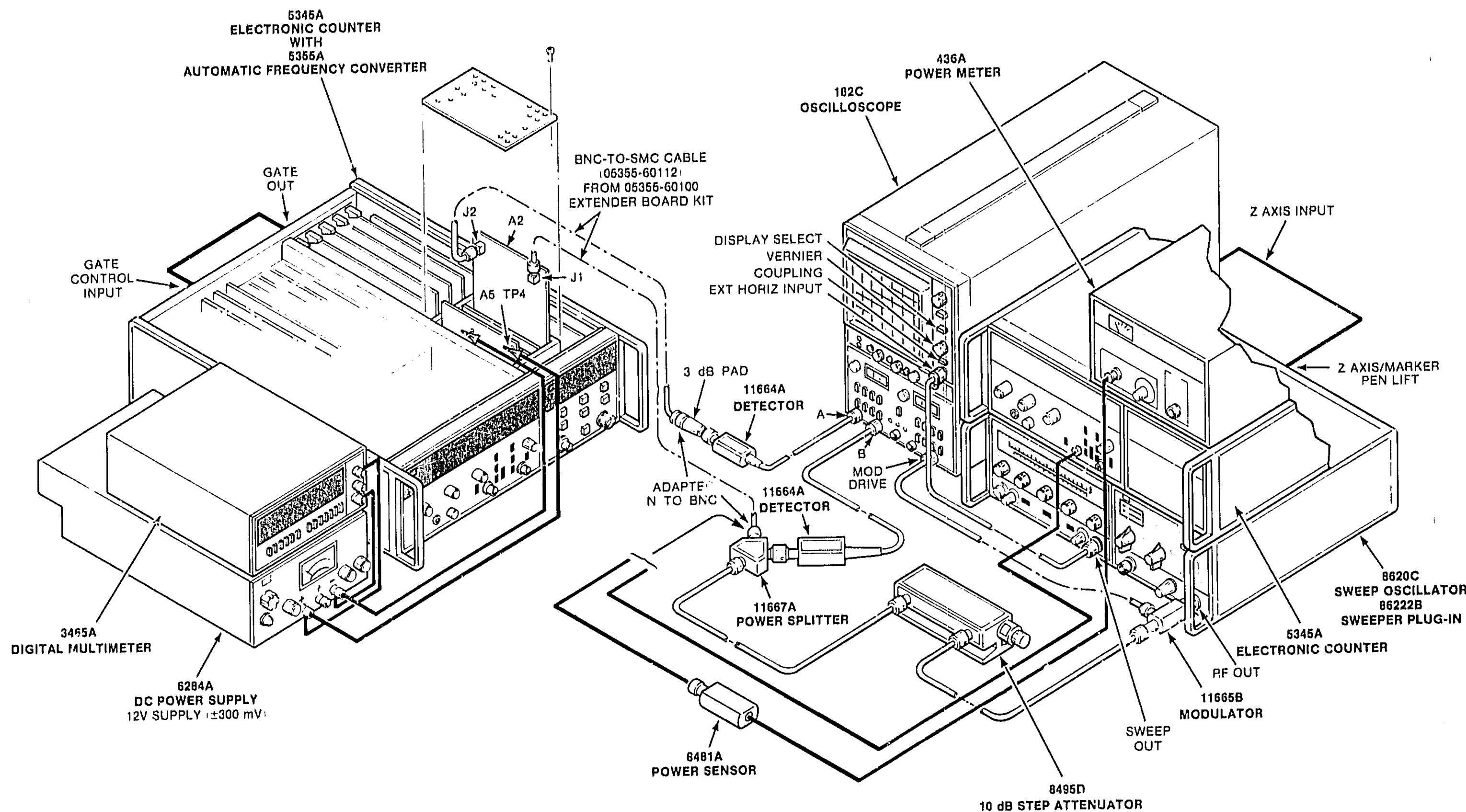
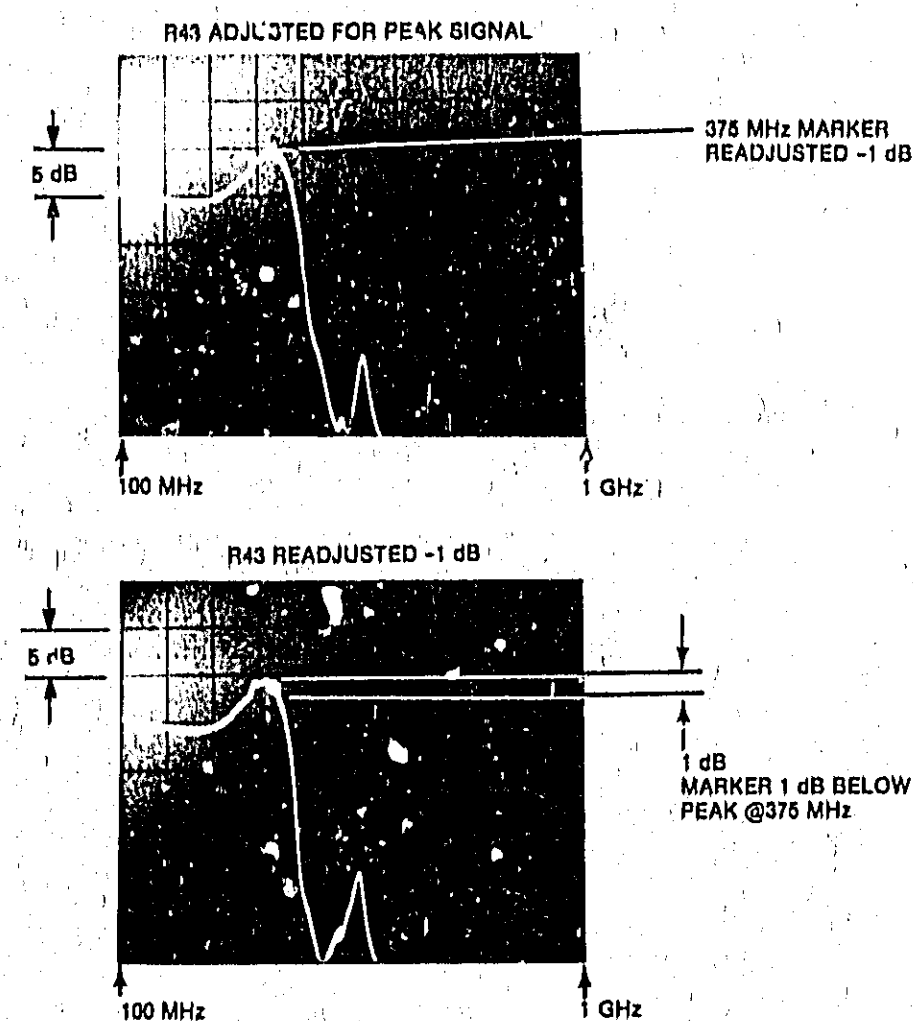


Figure 5-5. Gain Versus Frequency Adjustment Setup

5-19. AGC DIODE BIAS. Perform the AGC Diode Bias adjustment as follows:

- a. Connect the test equipment as shown in *Figure 5-6*.
- b. On 5355A, press the PULSE and MANUAL MEASUREMENT switches.
- c. Disconnect the input at A2J1.
- d. Connect the oscilloscope probe to A2TPD. Adjust variable resistor R11 (BIAS) to $+0.7V \pm 50 \text{ mV}$ as indicated on the oscilloscope.

NOTE

AGC circuit gain is extremely high and the oscilloscope display may appear erratic, as though a circuit problem exists. When an input signal is applied, this erratic action will become smooth, depending on the input signal level. Keep hands, tools and test leads away from board for best results. Check levels after adjustment hand and tool is removed to see that level is correct.

- e. Move the oscilloscope probe from TPD to TPE. Adjust variable resistor R24 (AGC) just to the point where the dc level starts to drop (approximately $+12V$).
- f. Set the 8640A to 200 MHz at 0 dBm with no modulation. Set the output level to -50 dB and connect it to A2J1.
- g. While observing the dc level on the oscilloscope, quickly change the output level to -30 dB . The dc level should rapidly decrease.
- h. While observing the dc level on the oscilloscope, quickly change the output level back to -50 dB . The dc level should slowly increase. If this action does not occur, troubleshoot the AGC circuit per *Table 8-13*.

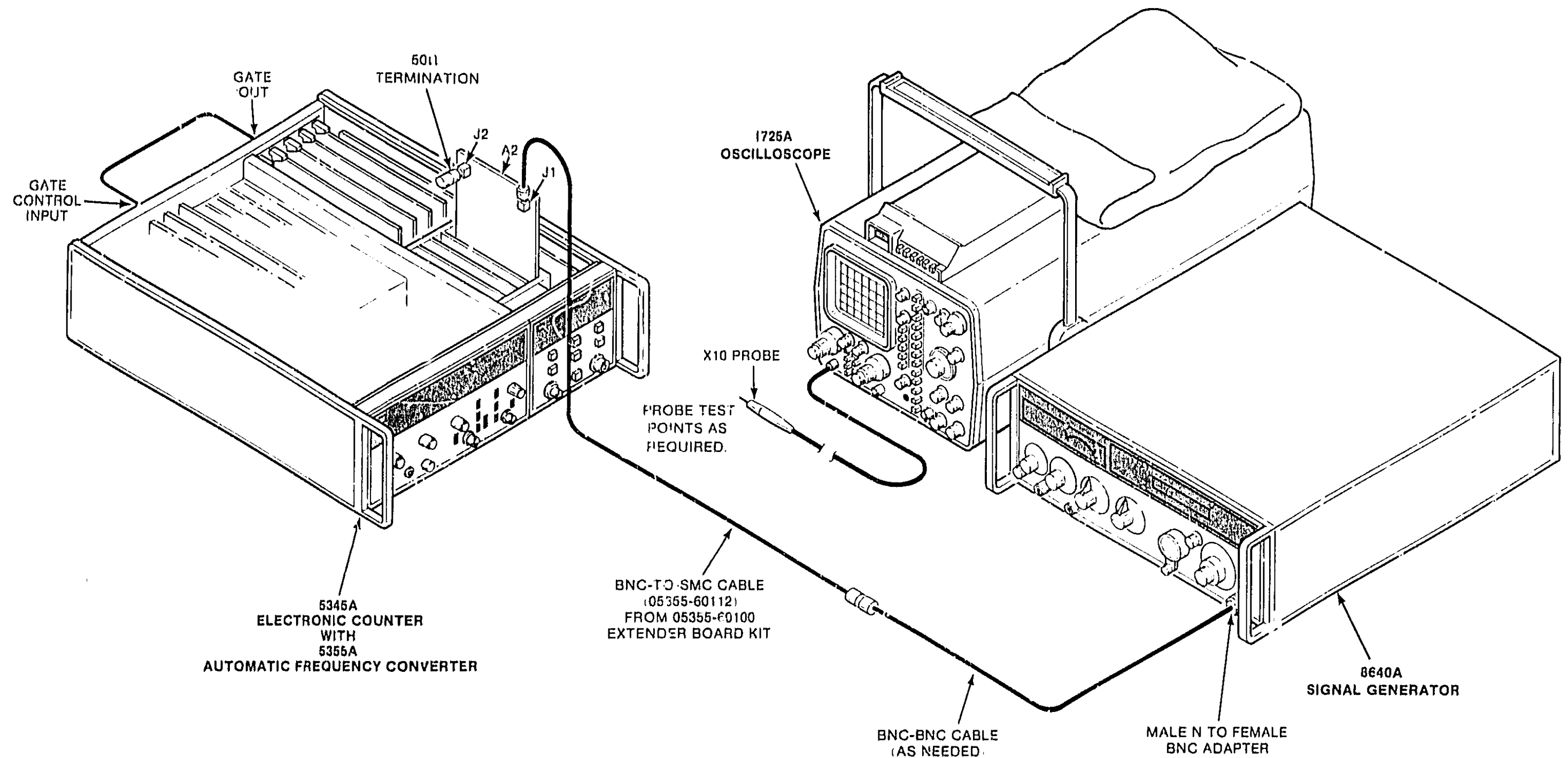


Figure 5-6. AGC Diode Bias Adjustment Setup

5-20. A3 Filter/Detector Assembly

5-21. The following adjustments tune the amplifier and various filters on the A3 assembly.

CAUTION

The power switch on the 5345A counter must be in the STBY position during removal or installation of PC assemblies.

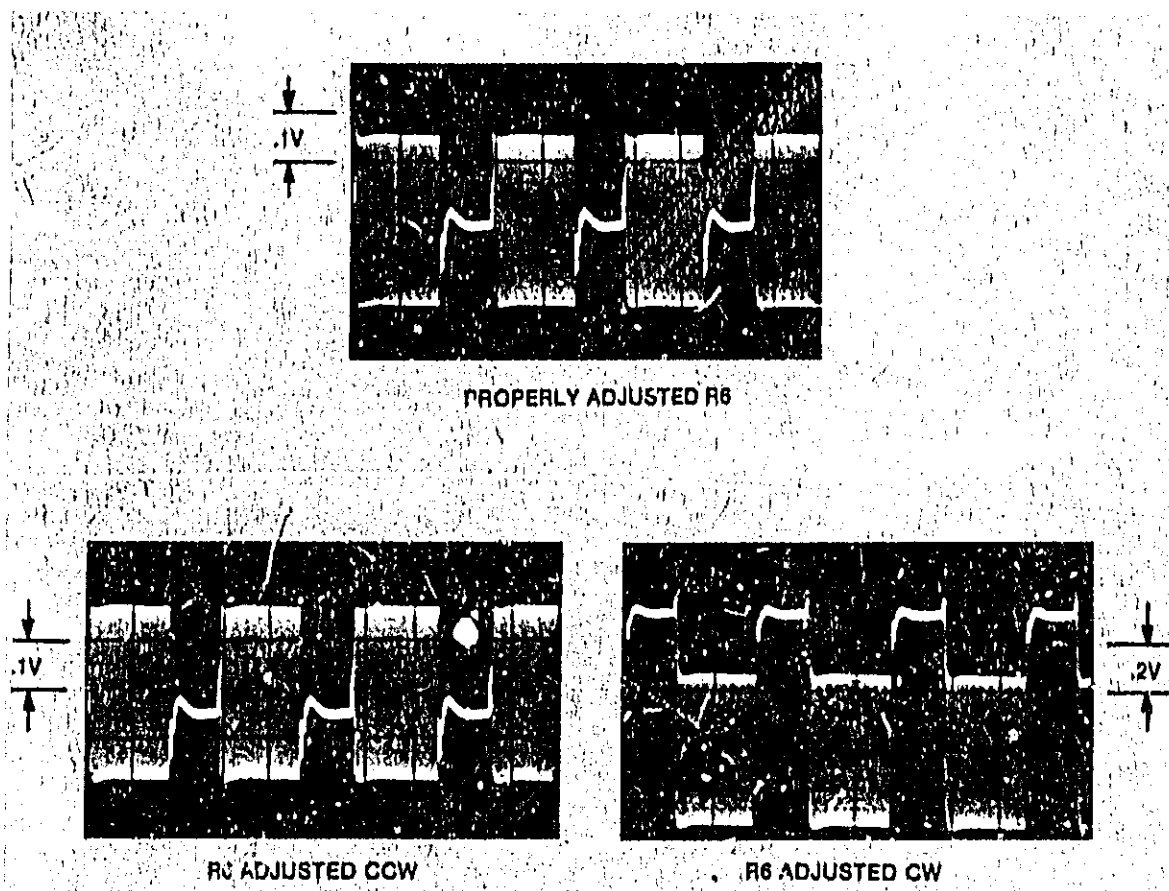
5-22. AMPLIFIER BALANCE ADJUSTMENTS. Perform adjustments as follows:

- a. Remove both the A2 and A3 assemblies together being careful not to damage the rigid coax interconnector located at the upper rear corners of the two assemblies. Remove the interconnector and reinstall the assemblies with A3 on an extender board.

NOTE

Connect 5356 converter head but do not apply an RF signal to it. This puts the 5355A in "RF HEAD INPUT" necessary for the following adjustments

- b. Set up the test equipment as shown in Figure 5-7.
- c. Set the 8640A Signal Generator for PULSE MODULATION and an output of 160 MHz at 0 dBm.
- d. Connect the oscilloscope to A3TPD (ac coupled) using a X10 probe.
- e. Adjust A3R6 (BIAS 1) until the RF pulse is symmetrical about its center line as shown in the top photo below.



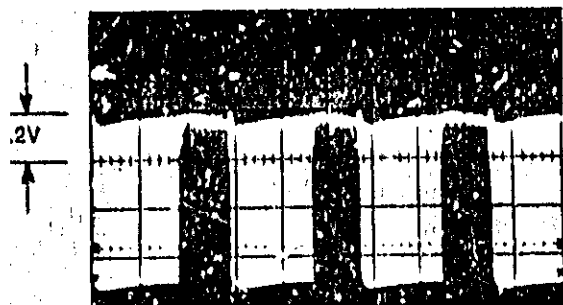
- I. Connect the oscilloscope to A3J3, ac coupled.
- B. Adjust A3R2B (BIAS 2) until the RF pulse is symmetrical about its center line as shown in the top photo below.

NOTE

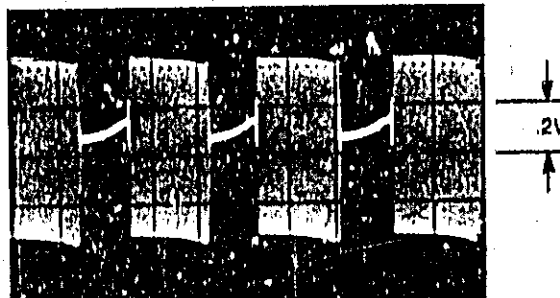
Test Limit: Amplitude symmetrical about center line $\pm 0.4V$.



PROPERLY ADJUSTED R2G



R2G ADJUSTED CCW



R2B ADJUSTED CW

5-23. PRELIMINARY FILTER ADJUSTMENTS. Perform adjustments as follows:

NOTE

Using the test setup in Figure 5-7, perform the following steps in the sequence listed. Extend only the A3 board for the preliminary adjustments. If A2 and A3 are extended together, interaction may result.

- a. Set the B640A for CW output of 7B MHz at 0 dBm.
- b. Connect the oscilloscope to A3TPJ (use 1M input).

NOTE

In the following adjustments the voltage range is at TTL levels. Mid-range settings are approximately 2 volts. Do not be concerned if oscillations occur.

Model 5355A Adjustments

- c. Adjust A3R23 (78) until a high-to-low transition occurs. Set A3R23 at the middle of the transition range.
- d. Set the 8640A to 157.5 MHz at -8 dBm.
- e. Connect the oscilloscope to A3TPH.
- f. Adjust A3R10 (157.5) until a low-to-high transition occurs. Set A3R10 at the middle of the transition range.
- g. Set the 8640A to 375 MHz at 0 dBm.
- h. Connect the oscilloscope to A3TPJ.
- i. Adjust A3R20 (375) until a high-to-low transition occurs. Set A3R20 at the middle of the transition range.
- j. Set the 8640A to 330 MHz at -8 dBm.
- k. Connect the oscilloscope to A3TPK.
- l. Adjust A3R31 (330) until a low-to-high transition occurs. Set A3R31 at the middle of the transition range.

5-24. FINAL TUNING OF FILTERS. To check the final tuning of the filter circuits, perform the following fine-tune procedures, in the sequence listed:

NOTE

Prior to making these adjustments, be sure that the A2 board adjustments have been made to ensure proper drive level.

CAUTION

The power switch on the 5345A must be in the STANDBY position during removal or installation of PC assemblies.

- a. Using the test setup in Figure 5-7, place the A2 and A3 boards (together) on extender boards and apply the input to A2J1. Connect A2J3 to the delay line (normal output connection). Prescaler Input A2J2 is not used.
- b. Set 8640A for CW output of 200 MHz at -20 dBm. Observe that the 5355A SIGNAL light comes on and 5345A displays 200 MHz.
- c. Set 8640A to 80 MHz and decrease frequency slowly until SIGNAL light goes off. Frequency should be between 77.5 and 79.5 MHz.
- d. If frequency in step c was too low, adjust A3R23 clockwise; if too high adjust counterclockwise.
- e. Repeat steps b and c until frequency is between 77.5 and 79.5 MHz.
- f. Remove A2 and A3 boards from extenders and reinstall in normal position in 5355A.
- g. Set 8640A to 155 MHz at -38 dBm and increase frequency slowly until 5355A SIGNAL light comes on. Frequency should be between 156.5 and 158.5 MHz.
- h. If frequency in step g was too low, adjust A3R10 clockwise; if too high, adjust counterclockwise.
- i. To recheck, set 8640A to below 78 MHz, then repeat steps g and h until frequency is between 156.5 and 158.5 MHz.
- j. Set 8640A to 370 MHz at -20 dBm and increase frequency slowly until SIGNAL light on 5355A goes off. Frequency should be between 374 and 376 MHz.

- k. If frequency in step l was too low, adjust A3R20 clockwise, if too high, adjust counterclockwise.
- l. To recheck, set 8640A to below 320 MHz, then repeat steps k and l until frequency is between 374 and 376 MHz. (This check is very sensitive and the procedure will require repetition to meet the ± 1 MHz tolerance.)
- m. Set 8640A to 333 MHz at -40 dBm and decrease frequency slowly until SIGNAL light on 5355A comes on. Frequency should be between 329 and 331 MHz.
- n. If frequency in step m was too high, adjust A3R31 clockwise, if too low, adjust counterclockwise.
- o. To recheck, set 8640A to above 375 MHz then repeat steps m and n until frequency is between 329 and 331 MHz.
- p. Approximate settings for A3 variable resistors R31, R20 and R10 at the end of the adjustments should be as shown below:

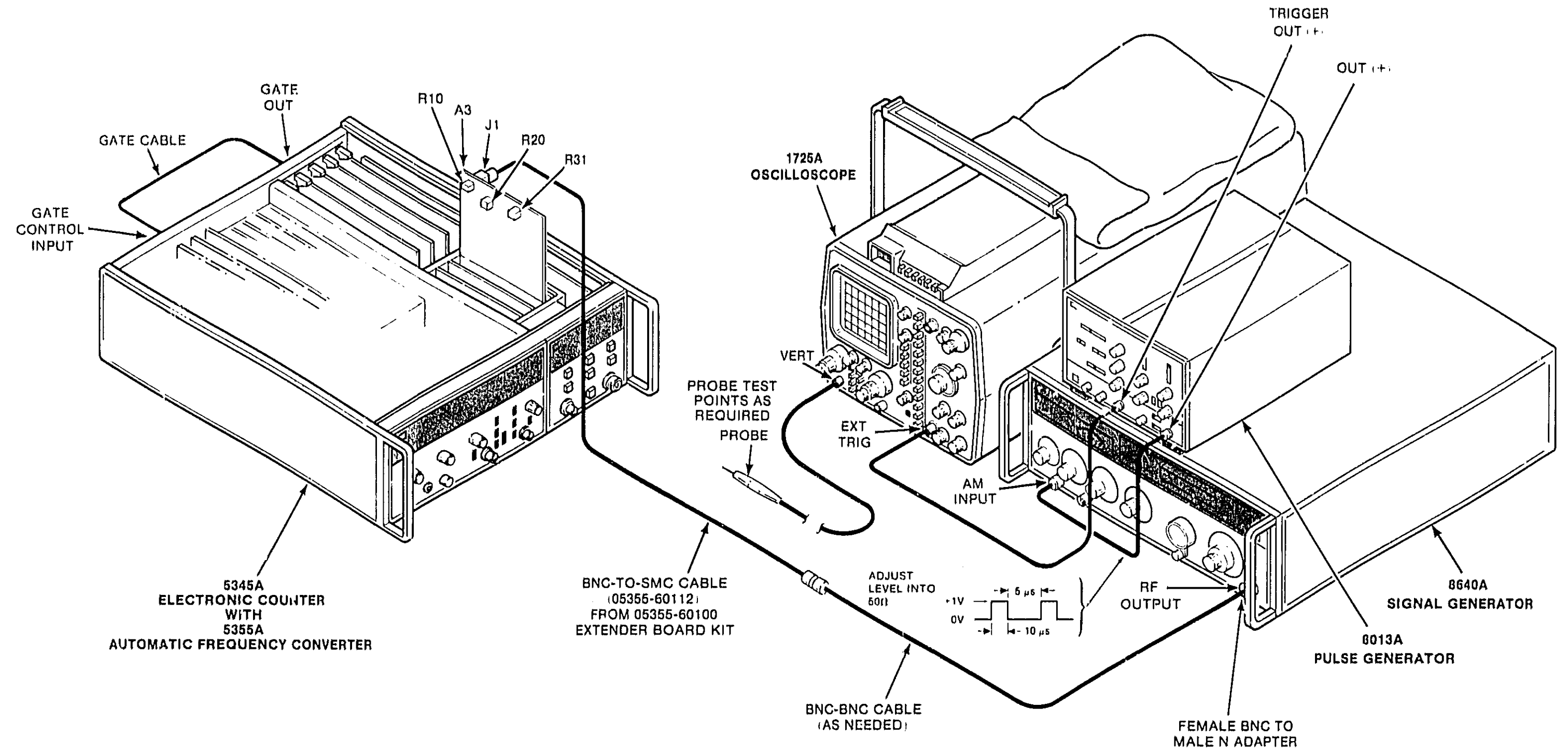
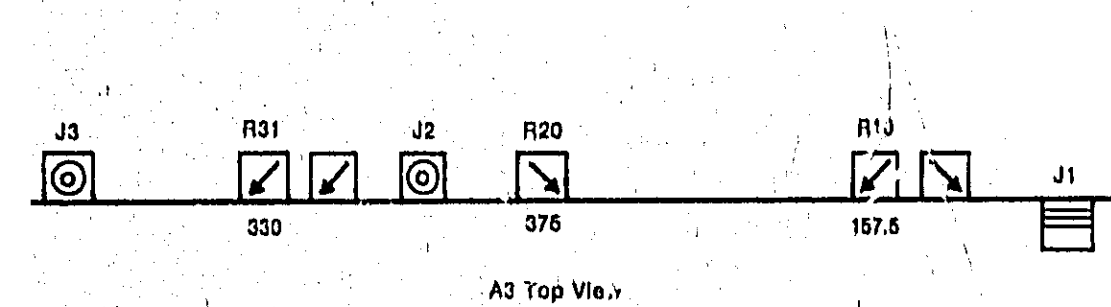


Figure 5-7. A3 Adjustments Test Equipment Setup

5-25. A11 Signal Switch Assembly

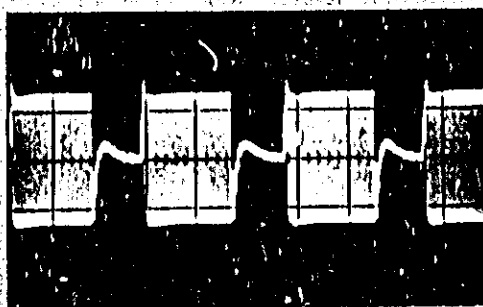
5-26. The only two adjustments on the A11 assembly (BIAS 1 and BIAS 2) determine the input dc bias on the two input differential amplifiers.

CAUTION

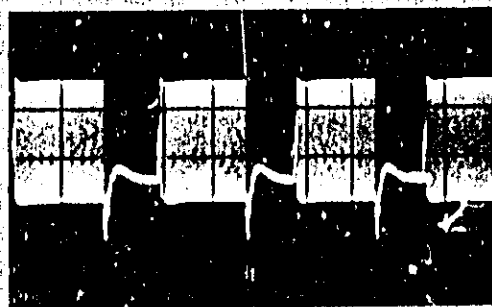
The power switch on the 5345A counter must be in the **STBY** position during removal or installation of PC assemblies.

5-27. BIAS 1. Perform the BIAS 1 adjustment as follows:

- Remove the A11 assembly and place on an extender board.
- Assemble the test equipment as shown in *Figure 5-8*.
- Adjust the output of the 0640A Signal Generator to 150 MHz at 0 dBm and connect it to A11J1.
- Connect the oscilloscope to A11TP5 and adjust R46 (BIAS 1) to give a signal symmetrical around its center line as shown in the top photo below.



CORRECTLY ADJUSTED R46



R46 ADJUSTED FULLY CCW
(INCORRECT)



R46 ADJUSTED FULLY CW
(INCORRECT)

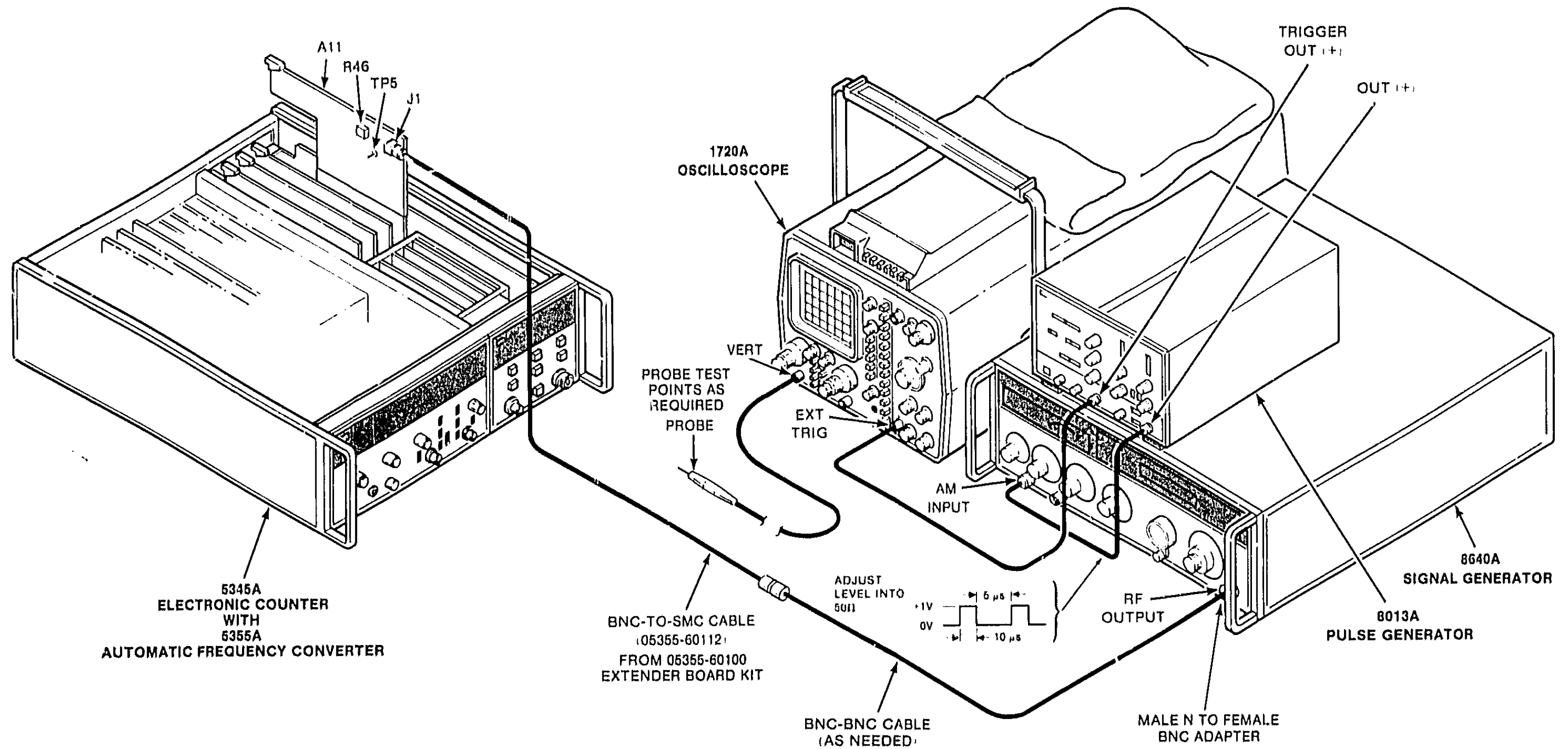


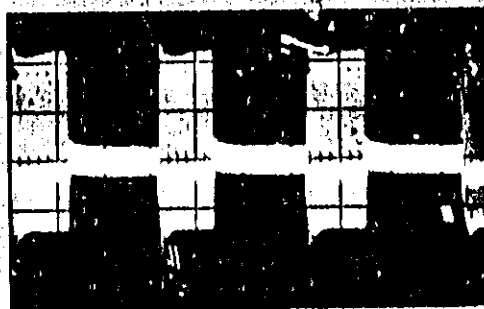
Figure 5-8. A11 Bias 1 Adjustment Setup

5-20. BIAS 2. Perform the BIAS 2 adjustment as follows:

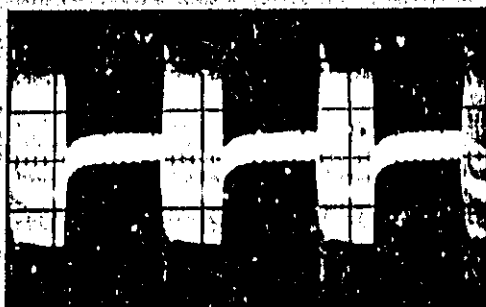
- a. Disconnect the input at A11J1.
- b. Assemble the test equipment as shown in Figure 5-9.
- c. Connect the 8640 Signal Generator output to A4J1. (The signal going to A4J1 is divided by 4 and output to XA11 (T5).)
- d. Set the 8640A Signal Generator to CW mode with an output of 1000 MHz at +5 dBm. After the signal generator has been properly adjusted, switch to PULSE output mode.
- e. Set the 5355A to RF HEAD INPUT mode and CW.
- f. Connect the oscilloscope to A11TP6 and adjust R37 (BIAS 2) to give a signal symmetrical about its center line as shown in the top photo below.

NOTE

As can be seen in the photos below, this adjustment has a small effect on the signal. The scope probe type and position, 8640A pulse modulator on-off ratio, and over-all circuit performance will affect the display and adjustment obtained.



CORRECTLY ADJUSTED R37



**R37 ADJUSTED FULLY CCW
(INCORRECT)**



**R37 ADJUSTED FULLY CW
(INCORRECT)**

Model 5355A Adjustments

5-29. A6 Prescaler Assembly

5-30. There are four adjustment areas on the A6 Prescaler assembly:

- a. Bias and hysteresis of 1.6 GHz binary (R38, R44)
- b. Arming circuit (R25)
- c. AGC and LV AGC (R42, R5, R8)
- d. PRS Gate (R6)

NOTE

Allow 5-minute warm-up before performing adjustments.

5-31. INITIAL SETUP: Proceed as follows (Figure 5-10):

- a. Remove 5355A from 5345A and connect the 5355A extender board (05355-60023) to the 5355A. Note the correct end as labeled on the board. Insert 5355A and extender into compartment, and connect extender card to the 5345A's connectors. The A6 prescaler is now visible through the 5355A's side frame. Extender board 05355-60023 is used to keep RF path length for the A6 board to a minimum. Keep GATE cable as short as possible.

NOTE

It is NOT recommended that the A6 board extender 05355-60020 be used during adjustment procedures. The longer signal paths with this extender may result in different performance levels.

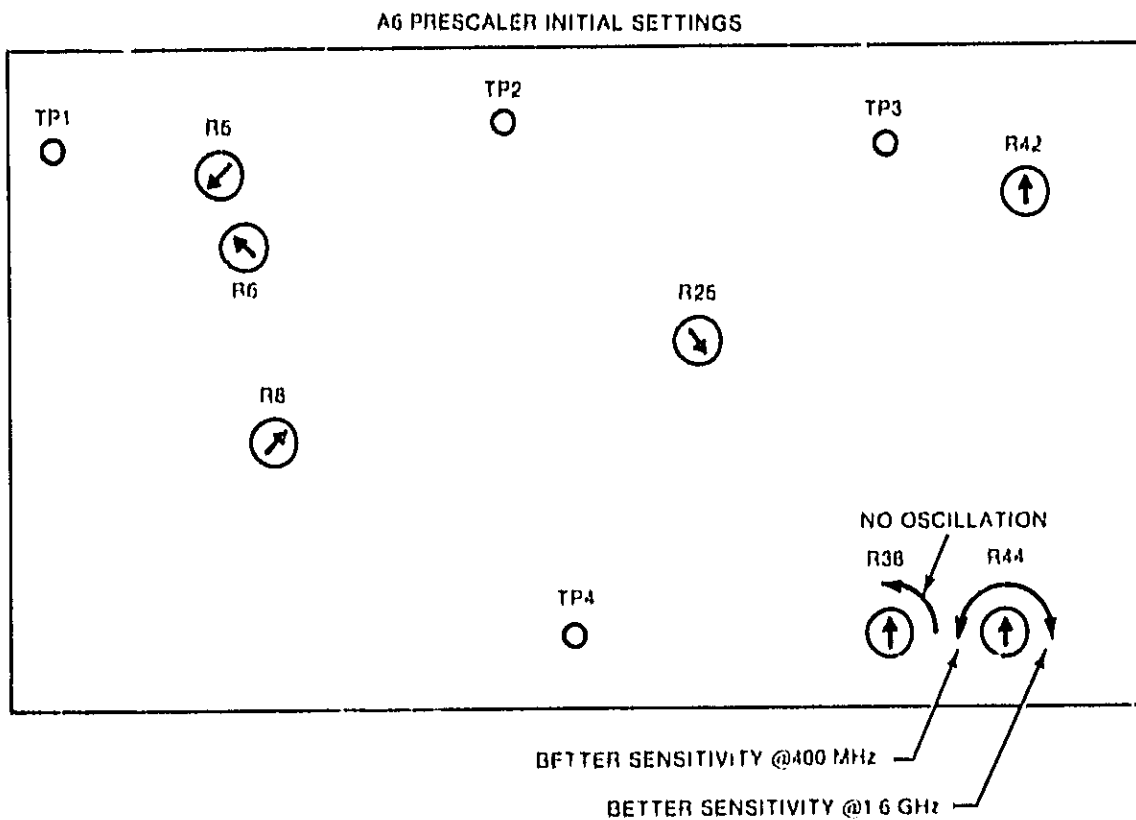
CAUTION

The A6 assembly operates at very high frequencies (up to 1.6 GHz). It is critical that the following steps be carried out EXACTLY as stated, in sequence! Don't use different frequencies or levels for adjustments. Several circuits are both frequency and amplitude sensitive. Proper adjustment and subsequent operation depend on proper adjustment procedures. If a given adjustment won't give the results indicated, stop and find out why. Refer to troubleshooting information in Section VIII if needed.

- b. Connect the test equipment as shown in Figure 5-10. Set step attenuators to 0 dB. Set 8620C level to 0 dBm as observed on 436 power meter. Then use step attenuators to set 5355A input levels.
- c. Set 8620C Sweep Oscillator to CW, 1.6 GHz, and RF switch to OFF.

d. Preset AG adjustments as follows (shown below):

R5 (AGC LEVEL) full cw
 R6 (PR5 GATE) midrange
 R8 (LV AGC) full cw
 R25 (ARMING) full cw
 R38 (BINARY BIAS) midrange
 R42 (AGC BIAS) midrange
 R44 (HYSTERESIS) midrange



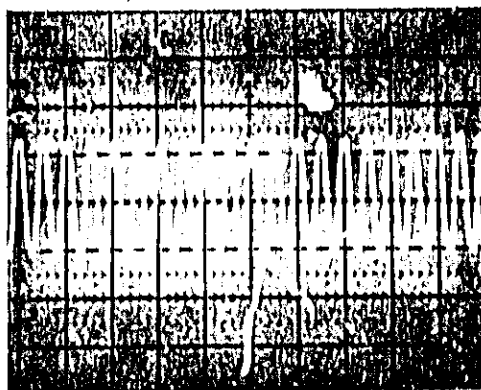
e. Check AGC voltage at TP2. It should be $>+12$ VDC. This means that the AGC circuit is "wide open" and will not attenuate the RF input signal. For the R5 preset position described above, the AGC level should be $>+12$ V. If not, troubleshoot AG per Table 8-11.

5-32. BINARY BIAS (R38) AND HYSTERESIS (R44). Adjust the bias and hysteresis using the setup in Figure 5-10, as follows:

- Turn on power to 5355A and set for prescaler input, CW mode. No RF input should be applied.
- Adjust R38 (BINARY BIAS) for maximum frequency of oscillation as observed on oscilloscope connected to IF out on 5355A. Ignore 5345A counter display throughout this adjustment.
- Slowly turn R38 (BINARY BIAS) cw until the oscillation just stops.
- Apply an RF input at 1.6 GHz and adjust power level using step attenuators. Determine the minimum RF signal level that can be applied while maintaining a clean crisp display on the scope. Be sure to check scope triggering adjustments. See photos 1 and 2 for a proper and improper interpretation of a scope display. Make a note of the input power level (merely read the attenuator settings). Level should be <-20 dBm, i.e., -20 dBm to approximately -26 dBm, depending on individual circuit gain.

Model 5355A
Adjustments

PHOTO 1
PROPER DISPLAY



RF INPUT -22 dBm
@1000 MHz

GROUND

Horiz: 10 ns/div.
Vert: 0.5V/div., 1:1 BNC cable in use.

PHOTO 2
IMPROPER DISPLAY



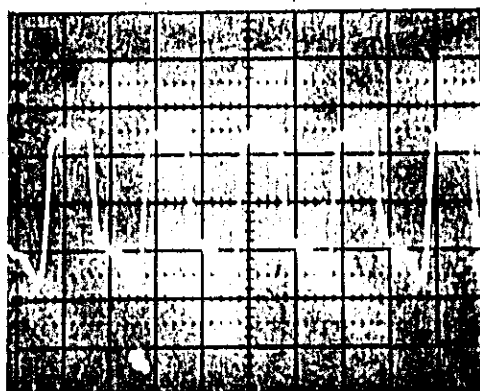
RF INPUT -24 DBm
@1000 MHz

GROUND

Horiz: 10 ns/div.
Vert: 0.5V/div., 1:1 BNC cable in use.

- e. Adjust RF source to 400 MHz and again determine minimum power level for clean crisp display. See photo 3 and 4 for proper and improper interpretations of scope display. A6 prescaler is designed to divide by 8. Connect another counter temporarily to IF OUT and determine that the IF output frequency is approximately 50 MHz. If it is higher (100 MHz or other multiple of 50 MHz), adjust input power level up to where proper division takes place. See photo 5 for an example of improper division. Make a note of the input power level at this frequency.

PHOTO 3
PROPER DISPLAY

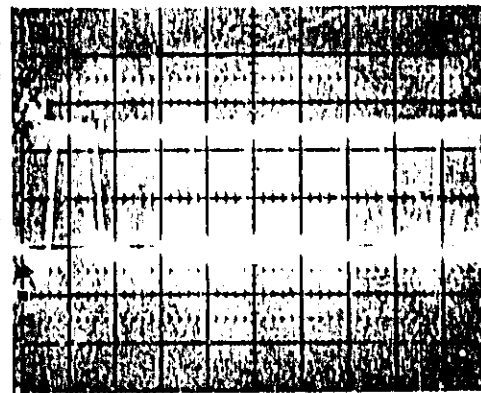


RF INPUT -33 dBm
@400 MHz

GROUND

Horiz: 10 ns/div.
Vert: .5V/div.

PHOTO 4
IMPROPER DISPLAY

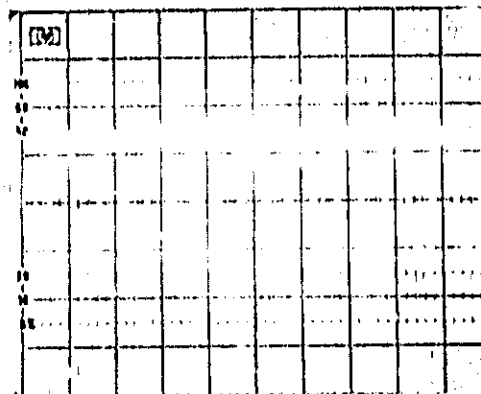


RF INPUT -34 dBm
@400 MHz

GROUND

Horiz: 10 ns/div.
Vert: .5V/div.

PHOTO 5
EXAMPLE OF IMPROPER
DIVISION. SIGNAL SHOWN
IS 100 MHz. SHOULD BE
60 MHz AS IN PHOTO 3.



RF INPUT -33 dBm
@400 MHz

GROUND

Horiz: 10 ns/div.
Vert: .5V/div.

- f. Adjust R44 (hysteresis) and R38 (binary bias) for best sensitivity at 400 and 1600 MHz, as follows:
 1. Adjust RF source to 1600 MHz.
 2. Set RF input level 1 dB lower than that obtained in step d. Scope picture should be fuzzy. If it is not, step d was not done properly.
 3. Adjust R44 clockwise from its midrange preset position to clean up the scope presentation.
 4. Adjust RF source to 400 MHz.
 5. Find minimum power level for clean crisp display. Note this level by reading step attenuator setting. It should be higher in power level than that found in step e above (If step e level was -34 dBm, level now should be in the range of -32 to -28 dBm, for example).
 6. Repeat steps f 1 through f.5 until power levels are 2 dB, or as close as possible to 2 dB apart at 400 and 1600 MHz. The RF input level required for a clear scope presentation at 1600 MHz must be greater than that required at 400 MHz.
 7. At this point, remove the RF input from the 5355A. Self-oscillation will probably occur. If so, turn R38 (binary bias) slightly ccw until it stops.
 8. Recheck the power levels for clear scope presentations at 1600 and 400 MHz. They will have dropped from those in step f.6 above. Readjust R44 and R38 as described in steps f.6 and f.7 to optimize the sensitivity and keep the 2 dB spread; or as close to a 2 dB spread as possible. Sensitivity must be ≤ -20 dBm at the least sensitive input frequency.

- g. Increase the input power level to 0 dBm and check for improper division as in step e. If this occurs, turn R44 (hysteresis) slightly counterclockwise. Beware also of improper division at low power levels. The adjustment of R44 ccw will also help this problem.
- h. As a last check before considering this adjustment complete, remove the RF input from the 5355A and check for oscillation. The A6 board circuit must NOT oscillate. (This is applicable only in CW mode.)
- i. Do not touch these adjustments any further. If these adjustments will not work, do not proceed further. Check that the other adjustments are preset as described in paragraph 5-28.d. (If the AGC pots are not preset, the circuit gain will be affected.) If adjustments still cannot be done, refer to Table 8-17 troubleshooting for procedures to find the fault.

5-33. ARMING CIRCUIT. Perform the arming circuit adjustment (R25) as follows (ignore 5345A display):

- a. Using the setup in Figure 5-10, set the 8620C to 1500 MHz and adjust the input power level for a clean, crisp scope display. Reduce power to where output to scope becomes unstable.
- b. Adjust R25 (ARMING) ccw until divided signal (as seen on oscilloscope) drops out. Yellow light on A6 may be on. If not, it should come on. (Yellow light on = input, yellow light off = no input.)
- c. Slowly adjust R25 (ARMING) cw until divided signal reappears on oscilloscope. (Yellow light should go off.)
- d. Adjust input power above and below best sensitivity point. Divided signal should snap on and off, not fade in and out. Using the step attenuators, a 1 to 3 dB change may be required to go from a clean "on" state to the "off" state.
- e. Set RF source to 400 MHz and check the snap action of R25 arming, observing the oscilloscope and the yellow lamp. As the RF input power level is decreased, the A6 board may go from a ± 8 operation to a ± 4 operation, before snapping off. (This phenomenon was discussed in paragraph 5-32e.) This is permissible. Do not touch R38 or R44 to "fix" this. The range of power levels for this situation will range from that obtained in paragraph 5-32.f.8 ≈ -26 dBm (typical) to ≈ -30 dBm.

5-34. AGC BIAS (R42), AGC LEVEL (R5), and LV AGC (R8) adjustments. Perform these adjustments using the test setup in Figure 5-10, as follows:

- a. Disconnect RF input from 5355A.
- b. Set 5355A to PULSE MEASUREMENT. Oscillation will occur and be observable on the scope. This is normal.
- c. On A6 board, connect DVM to TP3. Adjust R42 AGC BIAS to read $0.7 \pm (0.1)$ V. If voltage is too low, decrease value of R39, and if voltage is too high, increase value of R35. (About 1K Ω up or down.)
- d. Set 8620C output to 800 MHz CW and apply RF input to 5355A.
- e. Monitor IF OUT of 5355A and adjust step attenuators for minimum input signal for clean crisp waveform. Check scope trigger adjustments to be sure scope is not contributing to the fuzzy waveform. At this point, typical RF input levels may be -30 to -40 dBm.
- f. Increase power applied to 5355A by 2 dB. Do this by decreasing attenuation by 2 dB.
- g. Connect DVM to TP2. Adjust R5 AGC LEVEL ccw to the point where the DC voltage just starts to drop. This provides a preliminary adjustment.

- h. Set RF source to 1600 MHz and check for a minimum 2 dB margin as per steps e and f. Adjust R5 AGC LEVEL if necessary. Adjust RF source to 1500 MHz and repeat procedure. Continue repeating this procedure each 100 MHz down to 400 MHz.

NOTE

It is permissible to have a margin >2 dB; it must not be less. In effect, the AGC system is set to the least sensitive point in the range of 400 to 1600 MHz. Typically, the sensitivity is poorest at these extremes, but due to the critical nature of the circuits, there may be dips in between the extremes. This explains the importance of checks every 100 MHz.

- i. Set RF source to 800 MHz.
j. Adjust RF Input level until the voltage at TP2 is +11.5V.
k. Adjust R8 LV AGC ccw until green light turns on.

GATE CABLE
GATE CONTROL CABLE 05355-60101 FURNISHED WITH THE 5355 IS NOT LONG ENOUGH FOR THIS SET-UP. USE A LOCALLY SUPPLIED BNC-BNC CABLE AS A SUBSTITUTE AND KEEP IT UNDER 2 FEET LONG.

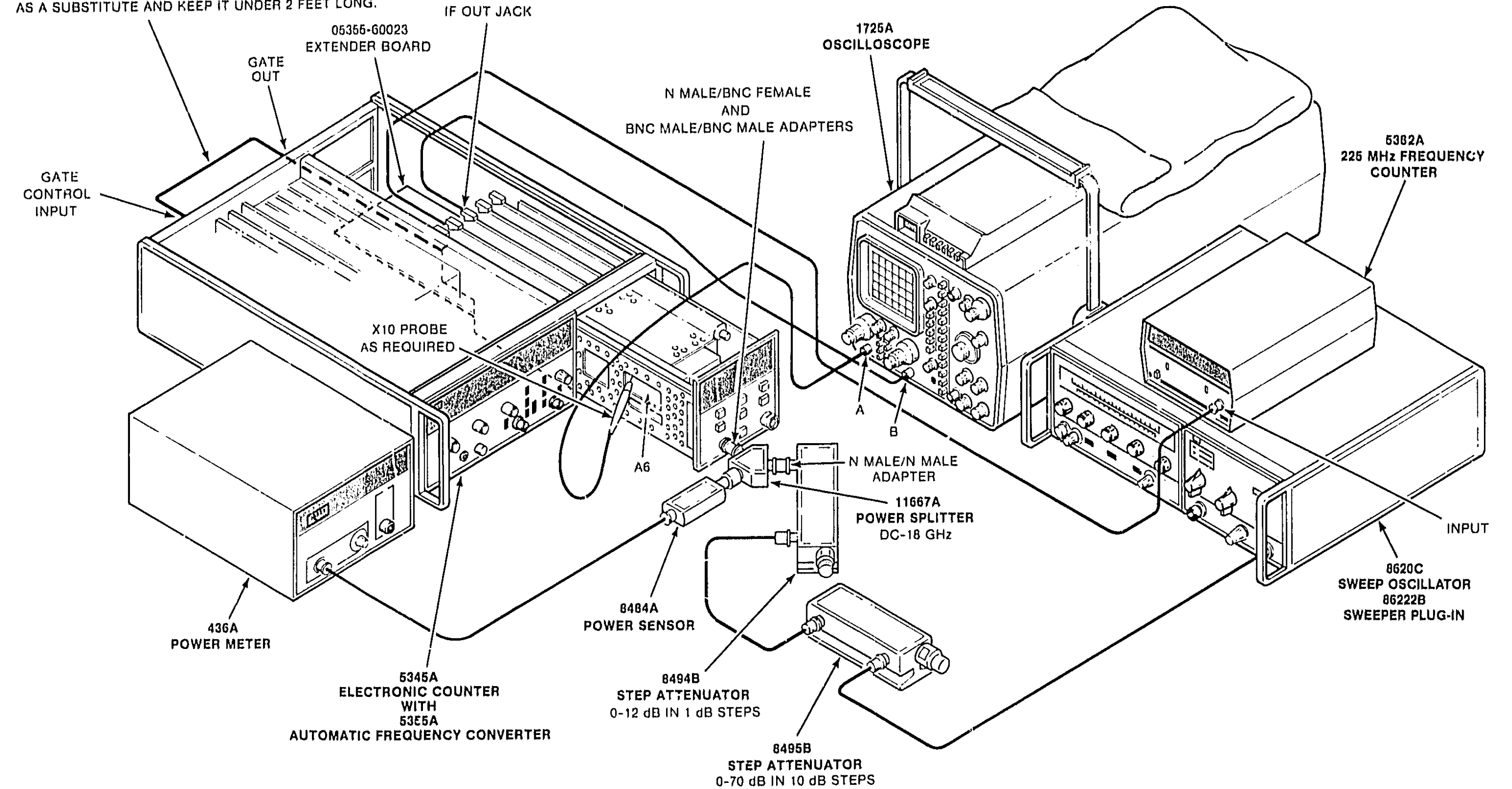
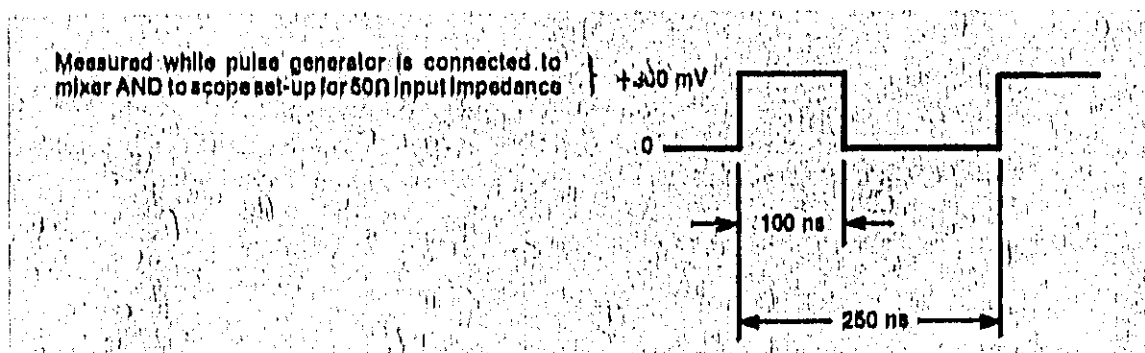


Figure 5-10. A6 Prescaler Initial Test Setup

5-35. PRS GATE (R6) ADJUSTMENT. Adjust the Prescaler (PRS) Gate circuit as follows:

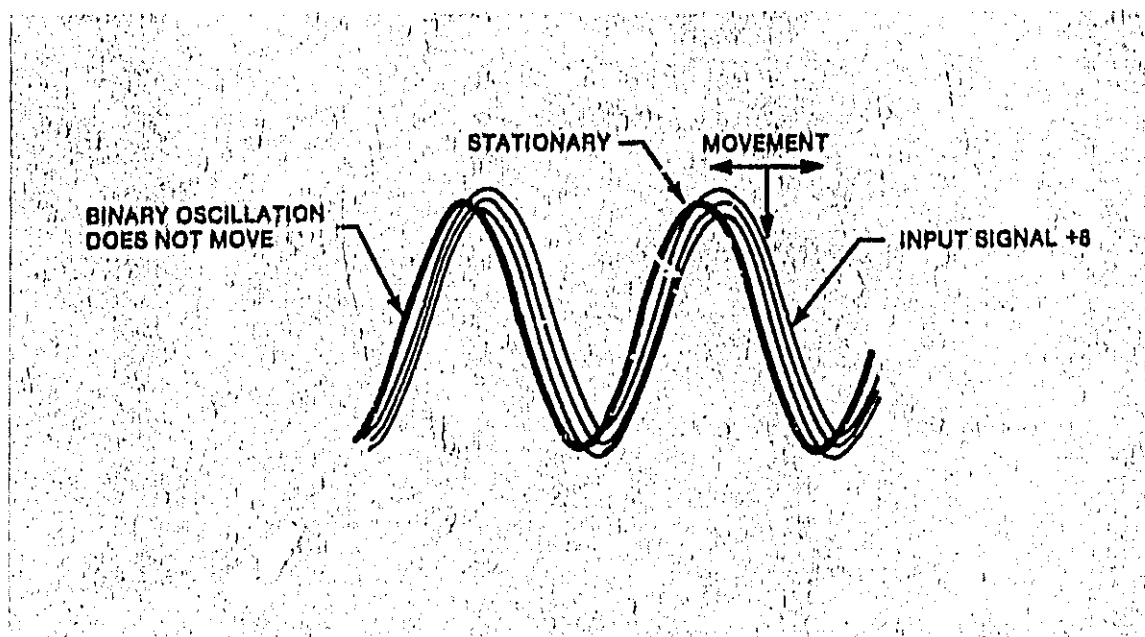
- Connect equipment setup as shown in Figure 5-11.
- Adjust pulse generator for output as shown below:



NOTE

A separate oscilloscope is required for viewing the signal at TP1. This is due to sync timing problems with using one scope for both.

- Set 8620C at 1500 MHz. Set 5355A in PULSE mode. Set step attenuator to 20 dB.
- The following description of the RF Input signal level adjustments is provided because a scope photo will not show the detail or the relative motion that occurs. It is critical that these steps be followed to obtain the proper adjustment of R6.
 - Set up oscilloscope to view the IF output. Typical settings: Vert .2V/div., horiz 10 ns/div. Set up oscilloscope connected to TP1 to view a TTL signal; Vert .2V/div. with X10 probe, horiz 50 ns/div.
 - Start RF level adjustment using vernier on 86222 set at minimum. You will note that when the power level is increased, two waveforms will be visible, and one will move with respect to the other.



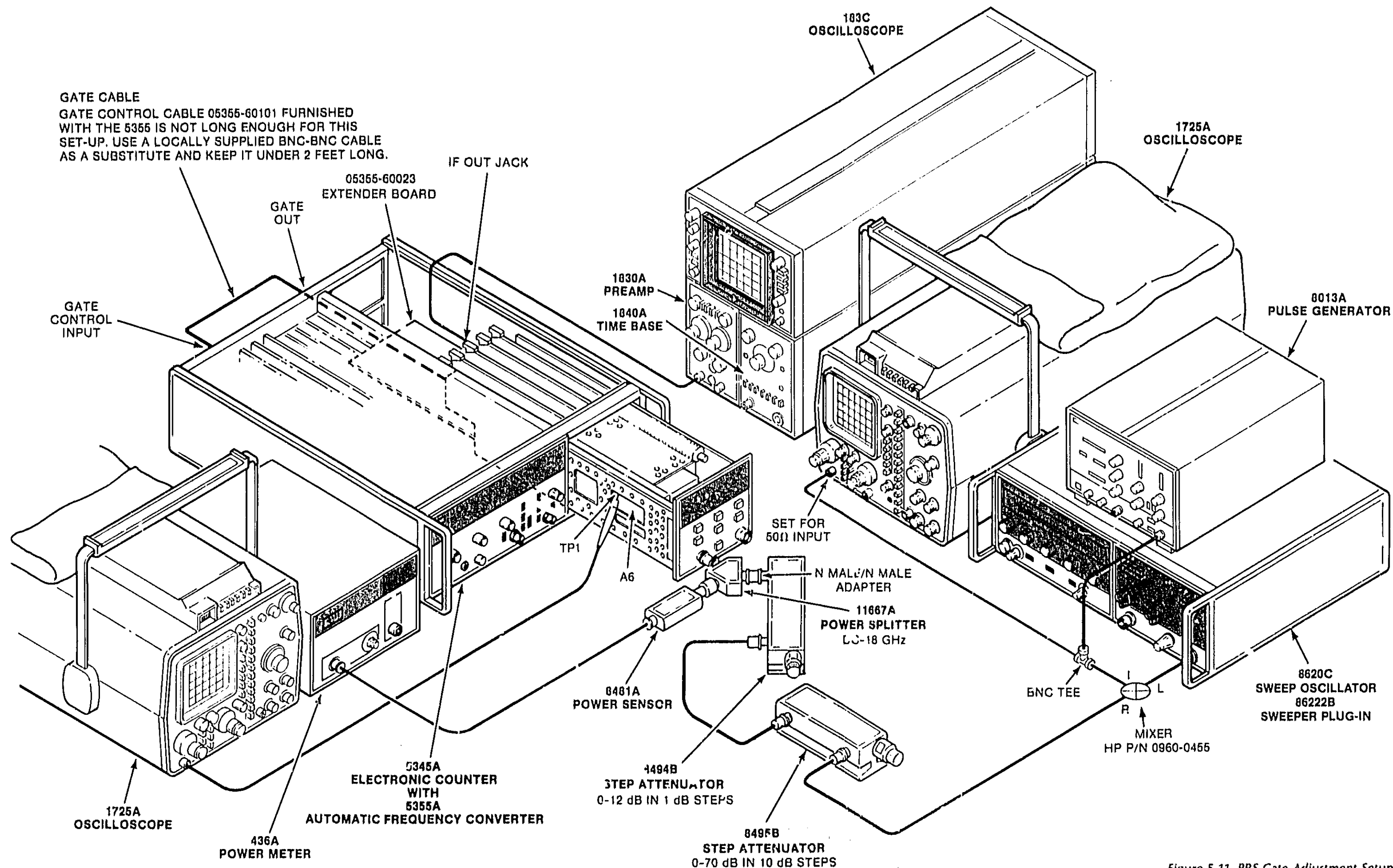
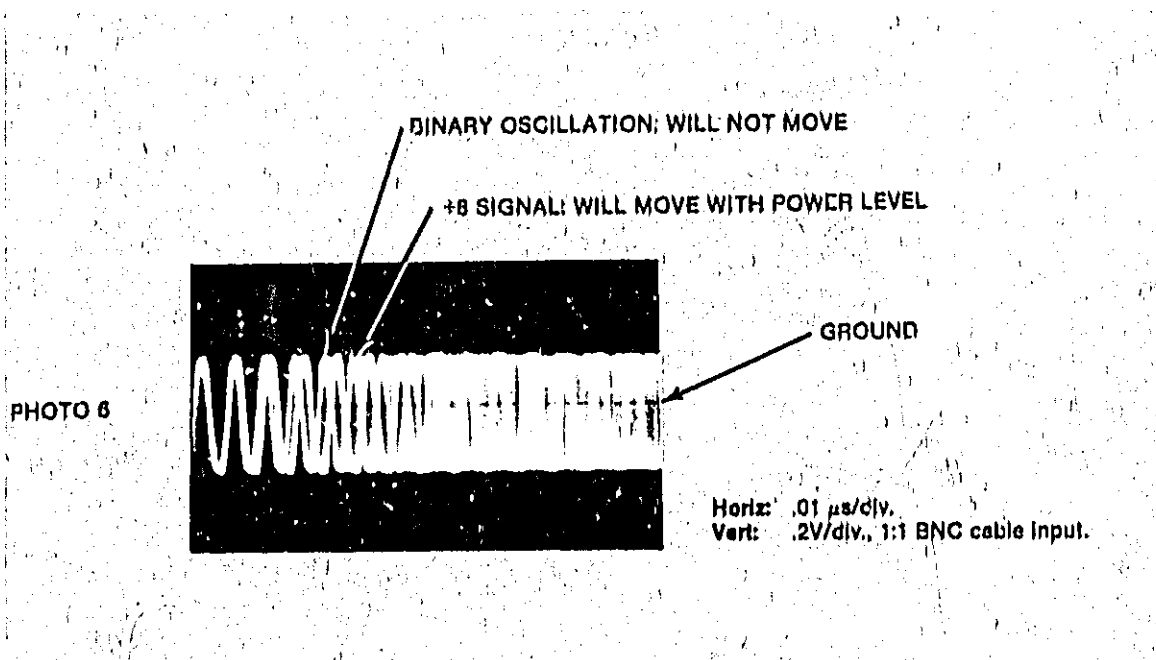


Figure 5-11. PRS Gate Adjustment Setup

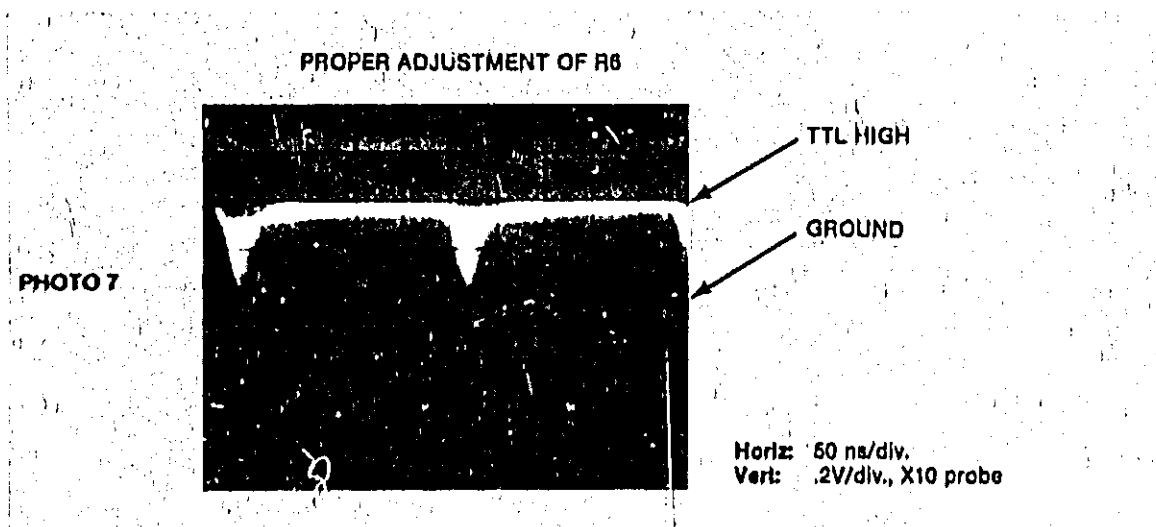
3. As the power level is increased further, a point will be reached where no further movement of the $\pm B$ signal will occur. This is the point to which the RF input level is to be adjusted. Experiment with this level adjustment and the scope action that occurs. Set the RF level at the point where the movement just stops as the level is increased from minimum.

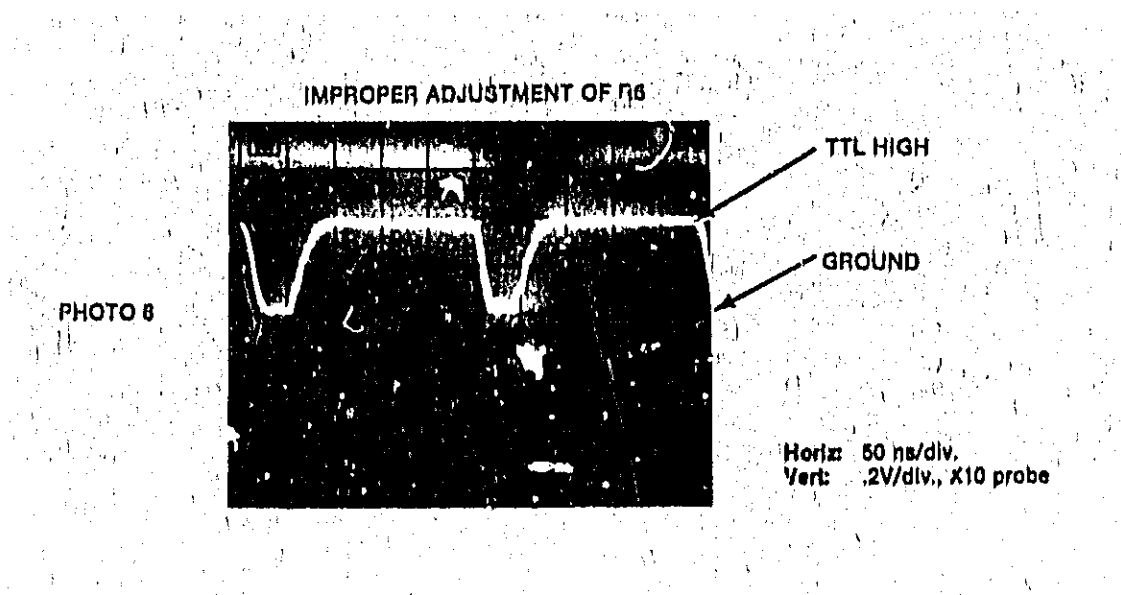
NOTE

Other "garbage" will probably be visible on the scope display, as a hazy background signal, and it may give the impression that the circuit is faulty. The presentation of the two signals of interest is clear enough to be seen. See photo 6. The absolute RF input level is not important for this adjustment.



- e. Turn R6 (PR5 gate adjust) so the level at TP1 is TTL high (or full ccw). Slowly turn R6 clockwise until signal observed at TP1 just starts to go low. See photo 7. Don't turn R6 too far cw, or pulse specifications will be degraded. See photo 8 for example of misadjusted R6. Adjustment is sensitive, so take your time.





5-36. To check the validity of all A6 adjustments, perform full performance tests for the .4-1.6 GHz input described in Section IV.

PARTS LIST

SECTION VI REPLACEABLE PARTS

6-1. INTRODUCTION

6-2. This section contains information for ordering replacement parts. Table 6-1 lists reference designations and abbreviations used in the parts list and throughout the manual. Table 6-2 lists 5355A parts in alphanumerical order of their reference designators and indicates the description and HP Part Number of each part, together with any applicable notes. This same type of information for the 5356A, B and C is contained in Tables 6-3, 6-4, and 6-5, respectively. A description of the parts list and ordering information is included in this section.

6-3. INPUT CONNECTOR J1 AND FUSE F1

6-4. Input connector J1 is a special connector designed to house fuse F1 as shown in Figure 6-1.

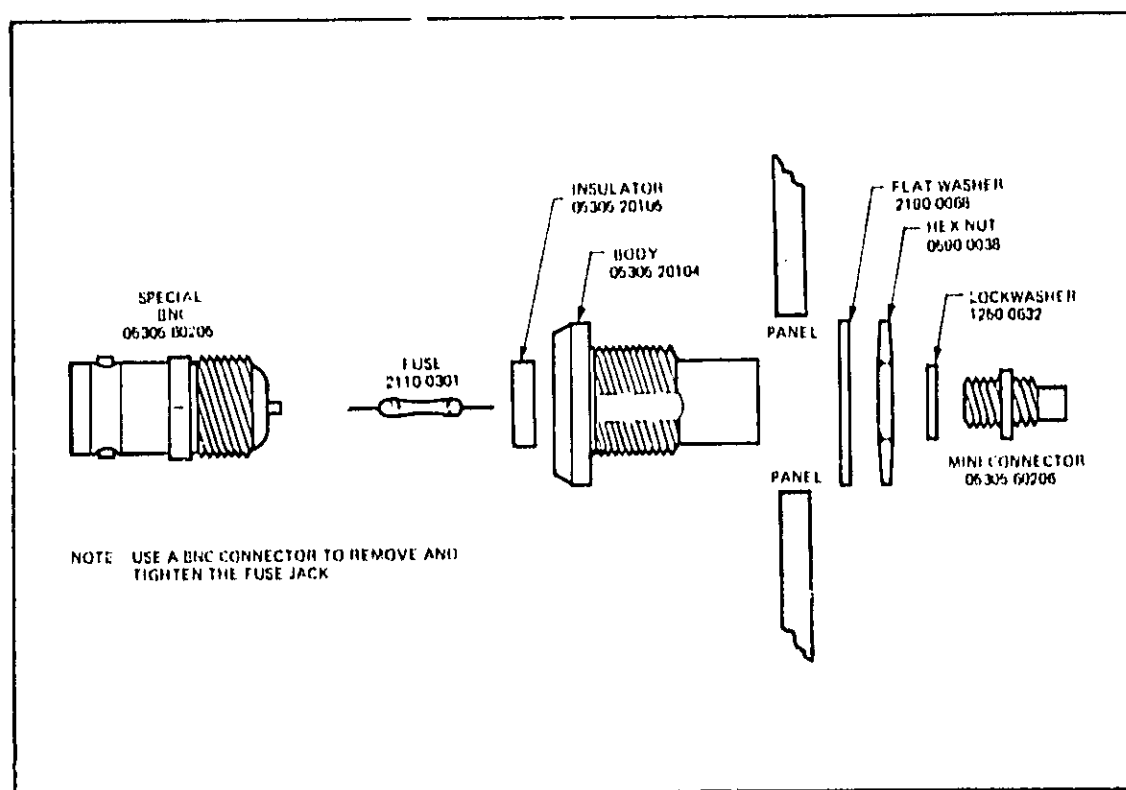


Figure 6-1. Details of Input Connector J1 and Fuse Mounting

6-5. MANUFACTURERS CODE LIST

6-6. Table 6-6 contains the names and addresses that correspond to the manufacturers code numbers.

Model 535A Replaceable Parts

Table 6-1 Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	assembly	DL	delay line	K	relay	T	transformer
AT	attenuator, isolator, termination	DS	annunciator, signaling device, audible or visual lamp, LED	L	coil, inductor	TB	terminal board
B	bar, motor	E	miscellaneous electrical part	M	metre	TC	thermocouple
BT	battery	F	fuse	MP	miscellaneous mechanical part	TP	test point
C	capacitor	FL	filter	P	electrical connector, movable	U	integrated circuit, microcircuit
CP	coupler	H	hardware	Q	transistor, SCR, triode thyristor	V	electron tube
CR	diode, diode thyristor, varactor	HY	circulator	R	resistor	VR	voltage regulator, breakdown diode
DC	directional coupler	J	electrical connector, stationary, porton, jack	RT	thermistor	W	wire, cable, transmission path, wire
				S	switch	X	socket
						Y	crystal unit, piezo electric
						Z	tuned cavity, tuned circuit

ABBREVIATIONS

A	amperes	hD	head	hZ	hertz	SPST	single pole, single throw
AC	alternating current	HDW	hardware	NEG	negative	SSB	single sideband
ACCESS	accessory	HF	high frequency	NI	nickel	SSY	stainless steel
ADJ	adjustment	HG	mercury	NI PL	nickel plate	STL	steel
A/D	analog to digital	HI	high	N/O	normally open	SQ	square
AF	audio frequency	HP	Hewlett-Packard	NOM	nominal	SWR	standing wave ratio
AFC	automatic frequency control	HPL	high pass filter	NORM	normal	SYNC	synchronize
AGC	automatic gain control	HS	hook, used in parts list	NPN	negative-positive-negative	T	timed, slow blow fuse
Al	aluminum	HV	high voltage	NPO	negative-positive-zero, zero temperature coefficient	TA	tantalum
ALC	automatic level control	HZ	hertz	NRFR	not recommended for field replacement	TC	temperature compensating
AM	amplitude modulation	IC	integrated circuit	ns	nanosecond	TD	time delay
AMPL	amplifier	ID	inside diameter	NSR	not separately replaceable	TERM	terminal
AFC	automatic phase control	IF	intermediate frequency	nW	nanowatt	TFT	thin-film transistor
ASBY	assembly	IMPG	impregnated	OB	order by description	TGL	toggle
AUX	auxiliary	IN	inch	OD	outside diameter	THD	thread
AVG	average	INCD	incandescent	OH	ohm	THRU	through
AWG	american wire gauge	INCL	include a	OP AMPL	operational amplifier	Ti	titanium
BAL	balance	INP	input	OPT	option	TOL	tolerance
BCD	binary coded decimal	INT	internal	OSC	oscillator	TRIM	trimmer
BD	board	kg	kilogram	OX	oxide	TSTR	transistor
BE CU	beryllium copper	kHz	kilohertz	P	peak, used in parts list	TTL	transistor-transistor logic
BFO	beat frequency oscillator	kV	kilovolt	PAM	pulse-amplitude modulation	TV	television
BM	bumper head	lb	pound	PC	printed circuit	Twi	television interference
BKDN	breakdown	LC	inductance, capacitance	PCM	pulse-code modulation	TWT	traveling wave tube
BP	bandpass	LED	light-emitting diode	PCL	pulse-count modulation	U	micro, 10 ⁻⁶ , used in parts list
BPF	bandpass filter	LF	low frequency	PCL	pulse-length modulation	UF	microfarad, used in parts list
BRS	brass	LG	long	PCL	pulse-count modulation	UHF	ultrahigh frequency
BWO	backward wave oscillator	LH	left hand	PCL	pulse-count modulation	UNREG	unregulated
CAL	calibrate	LIM	limit	PCL	pulse-count modulation	V	volt
CCW	counterclockwise	LIM	linear taper, used in parts list	PCL	pulse-count modulation	VA	voltampere
CER	ceramic	lin	linear	PCL	pulse-count modulation	Vac	vacuum
CHAN	channel	LK WASH	lockwasher	PCL	pulse-count modulation	VAR	variable
cm	centimeter	LO	low local oscillator	PCL	pulse-count modulation	VCO	voltage controlled oscillator
CMO	coaxial	LOV	local logic, used in parts list	PCL	pulse-count modulation	Vdc	voltage dc
COEF	coefficient	log	logarithm	PCL	pulse-count modulation	VDCW	voltage dc working, used in parts list
COM	common	LFF	low pass filter	PCL	pulse-count modulation	V F	voltage filtered
COMP	composition	LV	low voltage	PCL	pulse-count modulation	VFO	variable frequency oscillator
COMPL	complete	m	metre, distance	PCL	pulse-count modulation	VHF	very high frequency
CONN	connector	mA	milliamperes	PCL	pulse-count modulation	Vpk	voltage peak
CP	cadmium plate	MAX	maximum	PCL	pulse-count modulation	Vp p	voltage peak to peak
CRT	cathode ray tube	ME	megohm	PCL	pulse-count modulation	Vrms	voltage rms
CTL	complementary transistor logic	MEG	megaohm, used in parts list	PCL	pulse-count modulation	VSWR	voltage standing wave ratio
CW	continuous wave	MEI FLM	metal film	PCL	pulse-count modulation	VTO	voltage tuned oscillator
DA	digital to analog	MEI OX	metal oxide	PCL	pulse-count modulation	VTVM	vacuum tube voltmeter
dB	decibel	MF	medium frequency, microfarad, used in parts list	PCL	pulse-count modulation	V V	voltage switched
dBm	decibel referred to 1mW	MFR	manufacturer	PCL	pulse-count modulation	W	watt
dc	direct current	mg	milligram	PCL	pulse-count modulation	W	watt
deg	degree, temperature	MHz	megahertz	PCL	pulse-count modulation	WV	working inverse voltage
°	degree, plane angle	mH	millihenry	PCL	pulse-count modulation	WW	wirewound
°C	degree Celsius, centigrade	mH	millihenry	PCL	pulse-count modulation	WQ	without
°F	degree Fahrenheit	mH	millihenry	PCL	pulse-count modulation	YIG	yttrium-iron garnet
°K	degree Kelvin	mH	millihenry	PCL	pulse-count modulation	Zn	characteristic impedance
DEPC	deposited carbon	mH	millihenry	PCL	pulse-count modulation		
DET	detector	mH	millihenry	PCL	pulse-count modulation		
diam	diameter	mH	millihenry	PCL	pulse-count modulation		
DIA	diameter, used in parts list	mH	millihenry	PCL	pulse-count modulation		
DIFF AMPL	differential amplifier	mH	millihenry	PCL	pulse-count modulation		
div	division	mH	millihenry	PCL	pulse-count modulation		
DPDT	double pole, double throw	mH	millihenry	PCL	pulse-count modulation		
DR	drive	mH	millihenry	PCL	pulse-count modulation		
DRP	double sideband	mH	millihenry	PCL	pulse-count modulation		
DTE	diode transistor logic	mH	millihenry	PCL	pulse-count modulation		
DVM	digital voltmeter	mH	millihenry	PCL	pulse-count modulation		
LCC	linear coupled logic	mH	millihenry	PCL	pulse-count modulation		
EMF	electromotive force	mH	millihenry	PCL	pulse-count modulation		
EDP	electronic data processing	mH	millihenry	PCL	pulse-count modulation		
ELECT	electronic	mH	millihenry	PCL	pulse-count modulation		
ENCAP	encapsulated	mH	millihenry	PCL	pulse-count modulation		
EXT	external	mH	millihenry	PCL	pulse-count modulation		
F	farad	mH	millihenry	PCL	pulse-count modulation		
FET	field effect transistor	mH	millihenry	PCL	pulse-count modulation		
F F	flip flop	mH	millihenry	PCL	pulse-count modulation		
FM	frequency modulation	mH	millihenry	PCL	pulse-count modulation		
FM	frequency modulation	mH	millihenry	PCL	pulse-count modulation		
FREQ	frequency	mH	millihenry	PCL	pulse-count modulation		
FxD	fixed	mH	millihenry	PCL	pulse-count modulation		
G	gram	mH	millihenry	PCL	pulse-count modulation		
GE	germanium	mH	millihenry	PCL	pulse-count modulation		
GHz	gigahertz	mH	millihenry	PCL	pulse-count modulation		
GL	glass	mH	millihenry	PCL	pulse-count modulation		
GND	grounded	mH	millihenry	PCL	pulse-count modulation		
H	henry	mH	millihenry	PCL	pulse-count modulation		
H	hour	mH	millihenry	PCL	pulse-count modulation		
HET	heterodyne	mH	millihenry	PCL	pulse-count modulation		
HEX	hexagonal	mH	millihenry	PCL	pulse-count modulation		

NOTE

All abbreviations in the parts list will be in upper case.

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10 ¹²
G	giga	10 ⁹
M	mega	10 ⁶
k	kilo	10 ³
d	deka	10 ¹
d	deci	10 ⁻¹
c	centi	10 ⁻²
m	milli	10 ⁻³
μ	micro	10 ⁻⁶
n	nano	10 ⁻⁹
p	pico	10 ⁻¹²
f	femto	10 ⁻¹⁵
a	atto	10 ⁻¹⁸

NOTE

All abbreviations in the parts list will be in upper case.

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10 ¹²
G	giga	10 ⁹
M	mega	10 ⁶
k	kilo	10 ³
da	deka	10
d	deci	10 ⁻¹
c	centi	10 ⁻²
m	milli	10 ⁻³
μ	micro	10 ⁻⁶
n	nano	10 ⁻⁹
p	pico	10 ⁻¹²
f	femto	10 ⁻¹⁵
a	atto	10 ⁻¹⁸

6-7. REPLACEABLE PARTS LIST

6-8. Tables 6-2 through 6-5 are lists of replaceable parts and are organized as follows:

- a. Electrical assemblies and their components in alphanumerical order by reference designation.
- b. Chassis-mounted parts in alphanumerical order by reference designation.
- c. Miscellaneous parts.

6-9. The information given for each part consists of the following:

- a. The Hewlett-Packard part number.
- b. Part number check digit (CD).
- c. The total quantity (Qty) in the instrument.
- d. The description of the part.
- e. A typical manufacturer of the part in a five-digit code.
- f. The manufacturer's number of the part.

6-10. The total quantity for each part is given only once — at the first appearance of the part number in the list.

6-11. ORDERING INFORMATION

6-12. To order a part listed in the replaceable parts tables, quote the Hewlett-Packard part number, the check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your order.

6-13. To order a part that is not listed in the replaceable parts tables, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Office.

6-14. DIRECT MAIL ORDER SYSTEM

6-15. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

- a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.
- b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).
- c. Prepaid transportation (there is a small handling charge for each order).
- d. No invoices — to provide these advantages, a check or money order must accompany each order.

6-16. Mail order forms and specific ordering information is available through your HP office. Addresses and phone numbers are located at the back of this manual.

6-17. CABINET PARTS

6-18. Refer to Figure 6-2 for identification of mechanical cabinet parts.

Model 5355A
Replaceable Parts

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C. U.	Qty	Description	Mfr Code	Mfr Part Number
A1	05355-60001	1	1	FRONT PANEL CONTROL ASSEMBLY (SERIES 1840)	20480	05355-60001
A1C1	0160-3874	7	2	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3874
A1C2	0160-3874	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3874
A1C3	0160-0224	7	1	CAPACITOR-FXD .33UF+-10% 10VDC TA	54774	15C3336140104
A1D81	1990-0466	2	3	LED-VISIBLE LUM-INTIMCD 1F20MA-MAX	28480	1990-0466
A1D82	1990-0466	3	7	LED-VISIBLE LUM-INTIMCD 1F20MA-MAX	28480	1990-0466
A1D83	1990-0466	3		LED-VISIBLE LUM-INTIMCD 1F20MA-MAX	28480	1990-0466
A1D84	1990-0466	3		LED-VISIBLE LUM-INTIMCD 1F20MA-MAX	28480	1990-0466
A1D85	1990-0466	3		LED-VISIBLE LUM-INTIMCD 1F20MA-MAX	28480	1990-0466
A1D86	1990-0466	3		LED-VISIBLE LUM-INTIMCD 1F20MA-MAX	28480	1990-0466
A1D87	1990-0466	3		LED-VISIBLE LUM-INTIMCD 1F20MA-MAX	28480	1990-0466
A1D88	1990-0466	3		LED-VISIBLE LUM-INTIMCD 1F20MA-MAX	28480	1990-0466
A1D89	1990-0466	3		LED-VISIBLE LUM-INTIMCD 1F20MA-MAX	28480	1990-0466
A1D90	1990-0466	3		LED-VISIBLE LUM-INTIMCD 1F20MA-MAX	28480	1990-0466
A1J1	1200-0348	3	1	SOCKET-IC 16-CONT DIP DIP-BLDR	28480	1200-0348
A1L2	9100-1788	6	1	CORE-WIDE BANC EXHIBED CHMS 180 MHZ	02114	VR200 20/48
A1R1	1810-0231	9	1	NETWORK, RES 2.2K	01121	20A222
A1R2	1810-0363	8	2	NETWORK, RES 330	01121	20A331
A1R3	1810-0363	8		NETWORK, RES 330	01121	20A331
A1S1	5060-9436	7	7	PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S2	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S3	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S4	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S5	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S6	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S7	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1U1	1820-1197	1	1	IC BPN TTL LS LINE DRVR OCTL	01295	8474L82404
A1U2	1820-1196	8	2	IC PP TTL LS D-TYPE POS-EDGE-TRIG COM	01295	8474L81744
A1U3	1820-1196	8		IC PP TTL LS D-TYPE POS-EDGE-TRIG COM	01295	8474L81744
	1200-0473	8	2	SOCKET-IC 16-CONT DIP DIP-BLDR	28480	1200-0473
	1203-0585	1	1	SOCKET-IC 20-CONT DBL STAP DIP-BLDR	28480	1200-0525
	5041-0252	7	5	KEY CAP, QUARTER	28480	5041-0252
	5041-0450	7	1	KEY CAP, QUARTER, BLUE	28480	5041-0450
	5041-0483	6	1	KEY CAP, QUARTER	28480	5041-0483
	05328-40004	9	3	STANDOFF, LED, SHORT	28480	05328-40004

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	05355-60002	2	1	LIMITER AMPLIFIER ASSEMBLY (SERIES 2018)	28480	05355-60002
A2C1	0160-3879	7	20	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C2	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C3	0160-0192	6	2	CAPACITOR-PXD .33UF +-20% 35VDC TA	56289	15003350015A2
A2C4	0160-4743	6	1	CAPACITOR-PXD 470PF +-10% 100VDC	28480	0160-4743
A2C5	0160-0230	6	2	CAPACITOR-PXD 1UF +-20% 50VDC TA	56289	150010510050A2
A2C6	0160-0571	6	1	CAPACITOR-PXD 470PF +-20% 100VDC CER	28480	0160-0571
A2C7	0160-3879	3	1	CAPACITOR-PXD 33UF +-20% 35VDC CER 0+-30	28480	0160-3879
A2C8	0160-0128	3	1	CAPACITOR-PXD 2.2UF +-20% 50VDC CER	28480	0160-0128
A2C9	0160-0576	5	2	CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	0160-0576
A2C10	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C11	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C12	0160-0418	6	1	CAPACITOR-PXD 1UF +-20% 35VDC TA	28480	0160-0418
A2C13	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C14	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C15	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C16	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C17	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C18	0160-0512	7	1	CAPACITOR-PXD 100VDC CER 2-5PF 100V PC-MTG	28480	0160-0512
A2C19	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C20	0160-0562	1	9	CAPACITOR-PXD .33UF +-20% 10VDC TA	56289	15003350010A1
A2C21	0160-0562	1		CAPACITOR-PXD .33UF +-20% 10VDC TA	56289	15003350010A1
A2C22	0160-0562	1		CAPACITOR-PXD .33UF +-20% 10VDC TA	56289	15003350010A1
A2C23	0160-0562	1		CAPACITOR-PXD .33UF +-20% 10VDC TA	56289	15003350010A1
A2C24	0160-0562	1		CAPACITOR-PXD .33UF +-20% 10VDC TA	56289	15003350010A1
A2C25	0160-0562	1		CAPACITOR-PXD .33UF +-20% 10VDC TA	56289	15003350010A1
A2C26	0160-0562	1		CAPACITOR-PXD .33UF +-20% 10VDC TA	56289	15003350010A1
A2C27	0160-0562	1		CAPACITOR-PXD .33UF +-20% 10VDC TA	56289	15003350010A1
A2C28	0160-0562	1		CAPACITOR-PXD .33UF +-20% 10VDC TA	56289	15003350010A1
A2C29	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C30	0160-3728	5	3	CAPACITOR-PXD .01UF +-20% 50VDC CER	51959	100510312P
A2C31	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C32	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C33	0160-1701	2	1	CAPACITOR-PXD .68UF +-20% 6VDC TA	56289	15000551000A2
A2C34	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C35	0160-1746	5	1	CAPACITOR-PXD 15UF +-10% 20VDC TA	56289	150015619020A2
A2C36	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C37	0160-3728	5		CAPACITOR-PXD .01UF +-20% 50VDC CER	51959	100510312P
A2C38	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C39	0160-3728	5		CAPACITOR-PXD .01UF +-20% 50VDC CER	51959	100510312P
A2C40	0160-0576	5		CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	0160-0576
A2C41	0160-0195	6		CAPACITOR-PXD .33UF +-20% 35VDC TA	56289	15003350015A2
A2C42	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C43	0160-0230	7	2	CAPACITOR-PXD .33UF +-20% 35VDC TA	56289	15003350015A2
A2C44	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C45	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C46	0160-0230	6		CAPACITOR-PXD 1UF +-20% 50VDC TA	56289	150010510050A2
A2C47	0160-0230	6		CAPACITOR-PXD .33UF +-20% 35VDC TA	56289	15003350015A2
A2C48	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C49	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C50	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C51	1901-0639	7	1	DIODE-MICROWAVE SPEC TR8(04)-46 MAX	28480	1901-0639
A2C52	1901-0639	1	3	DIODE-SWITCHING 80V 20MA 300NS DO-7	28480	1901-0639
A2C53	1901-0639	1		DIODE-SWITCHING 80V 20MA 300NS DO-7	28480	1901-0639
A2C54	1901-0639	1		DIODE-SWITCHING 80V 20MA 300NS DO-7	28480	1901-0639
A2C55	1901-1050	1	1	DIODE-RECTIFY 150V 1A 20V 1A	28480	1901-1050
A2C56	0122-0245	5	3	DIODE-VVC 1N5139 6,8PF 10X	01281	155139
A2C57	0122-0245	5		DIODE-VVC 1N5139 6,8PF 10X	01281	155139
A2C58	0122-0245	5		DIODE-VVC 1N5139 6,8PF 10X	01281	155139
A2C59	1902-0057	2	1	DIODE-ZNR 6.49V 5% DO-35 PWR, 4A	28480	1902-0057
A2C60	1901-0639	4	4	DIODE-PIN 110V	28480	1901-0639
A2C61	1901-0639	4		DIODE-PIN 110V	28480	1901-0639
A2C62	1901-0639	4		DIODE-PIN 110V	28480	1901-0639
A2C63	1902-3171	7	1	DIODE-RECT 11V 5% DO-35 PWR, 4A TCR, 0.62A	28480	1902-3171
A2J1	1250-0835	2	1	CONNECTOR-RF BNC M PC 50-OHM	28480	1250-0835
A2J2	1250-0835	1	1	CONNECTOR-RF BNC M PC 50-OHM	28480	1250-0835
A2L1	05355-80006	8	2	COIL-4 TURNS	28480	05355-80006
A2L2	0159-0005	0	1	WIRE 22AWG M PVC 1222 80F	28480	0159-0005
A2L3	05355-80006	8		COIL, 4-TURNS	28480	05355-80006
A2L4	05355-80007	4	1	COIL, 6-TURNS	28480	05355-80007
A2L5	0160-0334	0	2	INDUCTOR-RF-CR-MLO 100UH 10X	28480	0160-0334

See introduction to this section for ordering information.
* Indicates factory selected value.

Model 5355A

Replaceable Parts

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	QTY	Description	Mfr Code	Mfr Part Number
A2L5	9100-0334	0	INDUCTOR RF-CM-HLD 100UH 10%	28480	28-103
A2L6	05355-80009	1	COIL, LOOP	28480	05355-80009
A2L7	9100-2276	4	INDUCTOR RF-CM-HLD 100UH 10% 105DX, 26LG	28480	9100-2276
A2L8	9100-2276	4	INDUCTOR RF-CM-HLD 100UH 10% 105DX, 26LG	28480	9100-2276
A2L9	9100-0144	0	INDUCTOR RF-CM-HLD 4.7UH 10% 105DX, 26LG	28480	9100-0144
A2L10	05355-80009	1	COIL-LOOP	28480	05355-80009
A2L11	9100-2276	7	INDUCTOR RF-CM-HLD 100UH 10% 105DX, 26LG	28480	9100-2276
A2L12	9100-2276	4	INDUCTOR RF-CM-HLD 100UH 10% 105DX, 26LG	28480	9100-2276
A2L13	9100-0144	0	INDUCTOR RF-CM-HLD 4.7UH 10% 105DX, 26LG	28480	9100-0144
A201	1854-0071	7	TRANSISTOR NPN 2N5179 2N5179 2N5179 2N5179 2N5179 2N5179 2N5179	28480	1854-0071
A202	1854-0345	2	TRANSISTOR NPN 2N5179 2N5179 2N5179 2N5179 2N5179 2N5179 2N5179	04713	2N5179
A203	1854-0345	2	TRANSISTOR NPN 2N5179 2N5179 2N5179 2N5179 2N5179 2N5179 2N5179	04713	2N5179
A204	1854-0215	1	TRANSISTOR NPN 2N5179 2N5179 2N5179 2N5179 2N5179 2N5179 2N5179	04713	2N5179
A205	1854-0250	6	TRANSISTOR MOSFET 3A218 4-CHAN D-MODE	01245	3A218
A206	1854-0071	7	TRANSISTOR NPN 2N5179 2N5179 2N5179 2N5179 2N5179 2N5179 2N5179	28480	1854-0071
A207	0698-7236	7	RESISTOR 1K 1% .05W P TCR00-100	24546	C3-1/8-T0-1001-G
A208	0698-7236	4	RESISTOR 2.2K 1% .05W P TCR00-100	24546	C3-1/8-T0-221-G
A209	0698-7236	2	RESISTOR 7.5K 1% .05W P TCR00-100	24546	C3-1/8-T0-7501-G
A210	0757-0280	7	RESISTOR 1.1K 1% .125W P TCR00-100	24546	C3-1/8-T0-1101-G
A211	0698-7236	5	RESISTOR 3.0K 1% .05W P TCR00-100	24546	C3-1/8-T0-301-G
A212	0698-7236	8	RESISTOR 90.9 1% .05W P TCR00-100	24546	C3-1/8-T0-909-G
A213	0698-7236	3	RESISTOR 383 1% .05W P TCR00-100	24546	C3-1/8-T0-383-G
A214	0757-0280	3	RESISTOR 1K 1% .125W P TCR00-100	24546	C4-1/8-T0-1001-G
A215	0698-7236	7	RESISTOR 5.1K 1% .05W P TCR00-100	24546	C3-1/8-T0-511-G
A216	0698-7236	8	RESISTOR 10K 1% .05W P TCR00-100	24546	C3-1/8-T0-1002-G
A217	9100-2413	4	RESISTOR-TYHM 200 10K C BIDE-ADJ 1-TYM	30483	ET502401
A218	0698-7236	0	RESISTOR 51.1 1% .05W P TCR00-100	24546	C3-1/8-T0-511-G
A219	0698-7236	7	RESISTOR 1K 1% .05W P TCR00-100	24546	C3-1/8-T0-1001-G
A220	0757-0397	3	RESISTOR 88.1 1% .125W P TCR00-100	24546	C4-1/8-T0-881-G
A221	0757-0397	0	RESISTOR 51.1 1% .125W P TCR00-100	24546	C4-1/8-T0-511-G
A222	0698-7236	8	RESISTOR 28.7 1% .125W P TCR00-100	30483	P455-1/8-T0-287-G
A223	0698-7236	3	RESISTOR 28.7 1% .125W P TCR00-100	30483	P455-1/8-T0-287-G
A224	2100-2484	4	RESISTOR-TYHM 5K 10K C BIDE-ADJ 1-TYM	30483	ET502502
A225	0757-0280	3	RESISTOR 5.1K 1% .125W P TCR00-100	24546	C4-1/8-T0-511-G
A226	0757-0397	3	RESISTOR 88.1 1% .125W P TCR00-100	24546	C4-1/8-T0-881-G
A227	0698-7236	8	RESISTOR 5.1K 1% .05W P TCR00-100	24546	C3-1/8-T0-511-G
A228	0698-7236	0	RESISTOR 237 1% .05W P TCR00-100	24546	C3-1/8-T0-237-G
A229	2100-2484	4	RESISTOR-TYHM 5K 10K C BIDE-ADJ 1-TYM	30483	ET502502
A230	2100-2514	1	RESISTOR-TYHM 20K 10K C BIDE-ADJ 1-TYM	30483	ET502503
A231	0698-7236	0	RESISTOR 5.1K 1% .05W P TCR00-100	24546	C3-1/8-T0-511-G
A232	0698-7236	8	RESISTOR 1.0K 1% .05W P TCR00-100	28480	0698-7241
A233	0698-7236	0	RESISTOR 28.7 1% .125W P TCR00-100	30483	P455-1/8-T0-287-G
A234	0757-0397	0	RESISTOR 51.1 1% .125W P TCR00-100	24546	C4-1/8-T0-511-G
A235	0757-0397	3	RESISTOR 5.1K 1% .125W P TCR00-100	24546	C4-1/8-T0-511-G
A236	2100-2582	1	RESISTOR-TYHM 10K 10K C BIDE-ADJ 1-TYM	30483	ET502403
A237	0698-7236	7	RESISTOR 1K 1% .05W P TCR00-100	24546	C3-1/8-T0-1001-G
A238	0698-7236	7	RESISTOR 5.1K 1% .05W P TCR00-100	24546	C3-1/8-T0-511-G
A239	0698-7236	8	RESISTOR 5.1K 1% .05W P TCR00-100	24546	C3-1/8-T0-511-G
A240	2100-2582	1	RESISTOR-TYHM 10K 10K C BIDE-ADJ 1-TYM	30483	ET502403
A241	0698-7240	7	RESISTOR 10K 1% .05W P TCR00-100	24546	C3-1/8-T0-1002-G
A242	0698-7243	4	RESISTOR 1.9K 1% .05W P TCR00-100	24546	C3-1/8-T0-1901-G
A243	2100-2484	4	RESISTOR-TYHM 5K 10K C BIDE-ADJ 1-TYM	30483	ET502502
A244	0698-7228	7	RESISTOR 408 1% .05W P TCR00-100	24546	C4-1/8-T0-408-G
A245	0757-0397	3	RESISTOR 5.1K 1% .125W P TCR00-100	24546	C4-1/8-T0-511-G
A246	0698-7260	7	RESISTOR 10K 1% .05W P TCR00-100	24546	C3-1/8-T0-1002-G
A247	0698-7260	7	RESISTOR 10K 1% .05W P TCR00-100	24546	C3-1/8-T0-1002-G
A248	0698-7253	8	RESISTOR 5.1K 1% .05W P TCR00-100	24546	C3-1/8-T0-511-G
A249	0698-7188	4	RESISTOR 10 1% .05W P TCR00-100	24546	C3-1/8-T0-1001-G
A250	0698-7218	4	RESISTOR 100 1% .05W P TCR00-100	24546	C3-1/8-T0-1004-G
A251	0837-0035	4	THERMISTOR DISC 5K-0PM TCR=0.02/C-DEG	28480	0837-0035
A251A	0300-1682	0	TERMINAL-STUD SGL-TUR PRESS-MYS	28480	0300-1682
A251B	0300-1682	0	TERMINAL-STUD SGL-TUR PRESS-MYS	28480	0300-1682
A251C	0300-1682	0	TERMINAL-STUD SGL-TUR PRESS-MYS	28480	0300-1682
A251D	0300-1682	0	TERMINAL-STUD SGL-TUR PRESS-MYS	28480	0300-1682
A251E	0300-1682	0	TERMINAL-STUD SGL-TUR PRESS-MYS	28480	0300-1682
A251F	0300-1682	0	TERMINAL-STUD SGL-TUR PRESS-MYS	28480	0300-1682
A251	1826-0372	2	IC-5 GND LIMITER/AMP	28480	1826-0372
A252	1826-0208	3	IC OP AMP GP 8-DIP-P	27014	L43104
A253	1826-0372	2	IC-5 GND LIMITER/AMP	28480	1826-0372
A254	1826-0493	4	IC OP AMP GP 8-DIP-P	27014	L43074
A255	1826-0372	2	IC-5 GND LIMITER/AMP	28480	1826-0372

*Indicates factory selected value

Model 5355A
Replaceable Parts

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
AZV01	1020-0222	3	1	IC V RELTR TO-92	04713	HC74L12ACP
AZV02	1020-0276	8	1	IC 74059 V RELTR TO-92	04713	HC74059ACP
				AZ MISCELLANEOUS PARTS*		
	0340-0060	4	1	TERMINAL-STUD SPCL-POTHRU PRESS-MTG	98291	011-0004 000 209
	0380-0111	0	1	STANDOFF-RVT-ON ,25-IN-LG 6-32TMD	00000	ORDER BY DESC-1PTICH
	05355-00008	2	2	SPRING, GROUND	28480	05355-00008
	1251-1950	7	8	CONNECTOR-BGL CONT BKT ,018-IN-BBC-BZ	28480	1251-1950

See introduction to this section for ordering information.
*Indicates factory selected value.

Table 6-2 Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	06355-60003	3	1	FILTER DETECTOR ASSEMBLY (SERIES 1852)	28480	06355-60003
A3C1	0160-1875	3	3	CAPACITOR-FXD .01UF +-5% 200VDC CER 0+-30	28480	0160-1875
A3C2	0160-1875	3	3	CAPACITOR-FXD .01UF +-5% 200VDC CER 0+-30	28480	0160-1875
A3C3	0160-1875	7	28	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C4	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C5	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C6	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C7	0160-1875	7	4	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C8	0160-1875	7	1	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C9	0160-1875	7	1	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C10	0160-1875	7	2	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C11	0160-1875	7	3	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C12	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C13	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C14	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C15	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C16	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C17	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C18	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C19	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C20	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C21	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C22	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C23	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C24	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C25	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C26	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C27	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C28	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C29	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C30	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C31	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C32	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C33	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C34	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C35	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C36	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C37	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C38	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C39	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C40	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C41	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C42	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C43	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C44	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C45	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C46	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C47	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C48	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C49	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C50	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C51	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C52	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C53	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C54	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C55	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C56	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C57	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C58	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C59	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C60	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C61	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C62	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C63	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C64	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C65	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C66	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C67	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C68	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C69	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C70	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C71	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C72	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C73	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C74	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C75	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C76	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C77	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C78	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C79	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C80	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C81	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C82	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C83	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C84	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C85	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C86	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C87	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C88	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C89	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C90	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C91	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C92	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C93	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C94	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C95	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C96	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C97	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C98	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C99	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C100	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C101	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C102	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C103	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C104	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C105	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C106	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C107	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C108	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C109	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C110	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C111	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C112	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C113	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C114	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C115	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C116	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C117	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C118	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C119	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C120	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C121	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C122	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C123	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C124	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C125	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C126	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C127	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C128	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C129	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C130	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C131	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C132	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C133	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C134	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C135	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C136	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C137	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C138	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C139	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C140	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C141	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-1875
A3C142	0160-1875	7		CAPACITOR-FXD .01UF +-20% 100VDC CER		

*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3L11	9100-0210	1	2	INDUCTORRY-CM-WLD 100UH 1K ,1000X,20SLG	28480	9100-0210
A3L12	9100-0541	1	2	INDUCTORRY-CM-WLD 250UH 10K ,250X,5LG	28480	9100-0541
A3L13	9100-0541	1	2	INDUCTORRY-CM-WLD 250UH 10K ,250X,5LG	28480	9100-0541
A3L14	9100-2250	1	2	INDUCTORRY-CM-WLD 100UH 10K ,1000X,20SLG	28480	9100-2250
A301	1854-0215	1	3	TRANSISTOR NPN 81 PD=350MH FTY=300MHZ	04713	243404
A302	1854-0215	1	3	TRANSISTOR NPN 81 PD=350MH FTY=300MHZ	04713	243404
A303	1853-0379	1	2	TRANSISTOR PNP 81 TO-18 PD=350MH	28480	1853-0379
A304	1853-0379	1	2	TRANSISTOR PNP 81 TO-18 PD=350MH	28480	1853-0379
A305	1853-0215	1	3	TRANSISTOR MOSFET N-CHAN E-MODE TO-18 81	28480	1853-0215
A306	1854-0019	1	3	TRANSISTOR NPN 81 TO-18 PD=350MH	28480	1854-0019
A307	1853-0215	1	3	TRANSISTOR MOSFET N-CHAN E-MODE TO-18 81	28480	1853-0215
A308	1854-0215	1	3	TRANSISTOR NPN 81 PD=350MH FTY=300MHZ	04713	243404
A3N1	0757-0430	1	3	RESISTOR 5,11K 1% ,125W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N2	0698-1049	1	3	RESISTOR 348 1% ,125W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N3	0757-0199	1	3	RESISTOR 21,5K 1% ,125W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N4				NOT ASSIGNED		
A3N5	0757-0442	1	3	RESISTOR 10K 1% ,125W F TC=0+-100	24546	C4-1/2-TO-1002-F
A3P6	2100-2849	1	2	RESISTOR-TXMR 5K 10% C SIDE-ADJ 1-TXN	30483	E750302
A3P7	0698-7211	1	2	RESISTOR 40,9 1% ,05W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3P8	0698-7211	1	2	RESISTOR 147 1% ,125W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3P9	0757-0430	1	3	RESISTOR 5,11K 1% ,125W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N10	2100-2874	1	2	RESISTOR-TXMR 500 10% C SIDE-ADJ 1-TXN	30483	E750301
A3N11	0698-7201	1	2	RESISTOR 34,8 1% ,05W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N12	0698-7201	1	2	RESISTOR 51,1 1% ,05W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N13	0698-7201	1	2	RESISTOR 10K 1% ,125W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N14	0757-0402	1	3	RESISTOR 110 1% ,125W F TC=0+-100	24546	C4-1/2-TO-1011-F
A3N15	0757-0417	1	3	RESISTOR 562 1% ,125W F TC=0+-100	24546	C4-1/2-TO-3111-F
A3N16	0698-7249	1	2	RESISTOR 3,48K 1% ,05W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N17	0698-7211	1	2	RESISTOR 147 1% ,125W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N18	0698-7240	1	2	RESISTOR 1,47K 1% ,05W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N19	0698-7211	1	2	RESISTOR 147 1% ,125W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N20	2100-2872	1	2	RESISTOR-TXMR 10K 10% C SIDE-ADJ 1-TXN	30483	E750303
A3N21	0757-0402	1	3	RESISTOR 110 1% ,125W F TC=0+-100	24546	C4-1/2-TO-1011-F
A3N22	0698-7211	1	2	RESISTOR 40,9 1% ,05W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N23	2100-1748	1	2	RESISTOR-TXMR 500 10% C TOP-ADJ 1-TXN	30483	E750300
A3N24	0757-0442	1	3	RESISTOR 10K 1% ,125W F TC=0+-100	24546	C4-1/2-TO-1002-F
A3N25	0757-0396	1	3	RESISTOR 51,1 1% ,125W F TC=0+-100	24546	C4-1/2-TO-3111-F
A3N26	0757-0396	1	3	RESISTOR 51,1 1% ,125W F TC=0+-100	24546	C4-1/2-TO-3111-F
A3N27	0698-7201	1	2	RESISTOR 51,1 1% ,05W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N28	2100-2849	1	2	RESISTOR-TXMR 5K 10% C SIDE-ADJ 1-TXN	30483	E750302
A3N29	0757-0402	1	3	RESISTOR 110 1% ,125W F TC=0+-100	24546	C4-1/2-TO-1002-F
A3N30	0757-0430	1	3	RESISTOR 5,11K 1% ,125W F TC=0+-100	24546	C4-1/2-TO-3111-F
A3N31	2100-2874	1	2	RESISTOR-TXMR 500 10% C SIDE-ADJ 1-TXN	30483	E750301
A3N32	0698-7226	1	2	RESISTOR 303 1% ,05W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N33	0757-0402	1	3	RESISTOR 110 1% ,125W F TC=0+-100	24546	C4-1/2-TO-1011-F
A3N34	0698-7201	1	2	RESISTOR 51,1 1% ,05W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N35	0698-7211	1	2	RESISTOR 40,9 1% ,05W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N36	0698-7217	1	2	RESISTOR 102 1% ,05W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N37	0698-7233	1	2	RESISTOR 5,11K 1% ,05W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N38	0698-7230	1	2	RESISTOR 562 1% ,05W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N39	0698-7201	1	2	RESISTOR 34,8 1% ,05W F TC=0+-100	24546	C3-1/8-TO-3111-F
A3N40	0608-7226	1	2	RESISTOR 363 1% 05W F TC 0+-100	24546	C3-1/8-TO-363R-G
A3U1	1826-0372	1	2	IC	28480	1826-0372
A3U2	1826-1492	1	2	IC BPA TTL LB INV MEX 1-INP	01295	874L816EAB
A3U3	1826-1240	1	2	IC LCM TTL LB QUAD	01295	874L82704
A3U4	1826-1200	1	2	IC GATE TTL LB OR QUAD 2-INP	01295	874L8124
A3U5	1826-0340	1	2	IC COMPARATOR MB 14-DIP-C	27014	LM101J
A3U6	1826-0340	1	2	IC COMPARATOR MB 14-DIP-C	27014	LM101J
A3U7	1826-0372	1	2	IC	28480	1826-0372
A3U8	1826-0340	1	2	IC COMPARATOR MB 14-DIP-C	27014	LM101J
				A3 MISCELLANEOUS PARTS		
	0360-1042	0	12	TERMINAL-STUD SCL-FUR PRESS-MTG	28480	0360-1042
	0360-0193	0	1	STANDOFF-RVT-ON ,112-14-G 0-32THC	00000	CROCK BY DESCRIPTION
	1200-0473	0	1	ROCKET-IC 16-CONT DIP 01P-BLDR	28480	1200-0473
	8154-0009	0	1	WIRE 22AWG N PVC 1222 BUC	28480	8154-0009

See introduction to this section for ordering information
*Indicates factory selected value

Model 5355A Replaceable Parts

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4	05355-60004	4	1	PROGRAMMABLE DIVIDER (-M) ASSEMBLY (SERIES 1840)	28420	05355-60004
AAC1	0180-3879	7	15	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC2	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC3	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC4	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC5	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC6	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC7	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC8	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC9	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC10	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC11	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC12	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC13	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC14	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC15	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC16	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC17	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC18	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC19	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC20	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC21	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC22	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC23	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC24	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC25	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC26	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC27	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC28	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC29	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC30	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC31	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC32	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC33	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC34	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC35	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC36	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC37	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC38	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC39	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC40	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC41	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC42	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC43	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC44	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC45	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC46	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC47	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC48	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC49	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC50	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC51	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC52	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC53	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC54	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC55	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC56	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC57	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC58	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC59	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC60	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC61	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC62	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC63	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC64	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC65	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC66	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC67	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC68	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC69	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC70	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC71	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC72	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC73	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC74	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC75	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC76	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC77	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC78	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC79	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC80	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC81	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC82	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC83	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC84	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC85	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC86	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC87	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC88	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC89	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC90	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC91	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC92	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC93	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC94	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC95	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC96	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC97	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC98	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC99	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC100	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC101	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC102	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC103	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC104	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC105	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC106	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC107	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC108	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC109	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC110	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC111	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC112	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC113	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC114	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC115	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC116	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC117	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC118	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC119	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC120	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC121	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC122	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC123	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC124	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC125	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC126	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC127	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC128	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC129	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC130	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC131	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC132	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC133	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC134	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC135	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC136	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC137	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC138	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC139	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC140	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC141	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC142	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC143	0180-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0180-3879
AAC144	0180-3879	7		CAPACITOR-FXD .01UF +-20		

*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
AB	00355-60005	B	1	DC AMPLIFIER/COMPENSATOR ASSEMBLY (SERIES 1840)	28480	00355-60005
ABC1	0180-0198	9	1	CAPACITOR-PXO 5000PF ±10% 200VDC POLYE	28480	0180-0198
ABC2	0180-0223	7	1	CAPACITOR-PXO 200PF ±1% 300VDC MICA	28480	0180-0223
ABC3	0180-0193	4	1	CAPACITOR-PXO 1000PF ±10% 200VDC POLYE	28480	0180-0193
ABC4	0180-0198	5	1	CAPACITOR-PXO 2200PF ±10% 200VDC POLYE	28480	0180-0198
ABC5	0180-0229	7	1	CAPACITOR-PXO 330PF ±10% 10VDC TA	28480	0180-0229
ABC6	0180-0198	4	1	CAPACITOR-PXO 3300PF ±10% 200VDC POLYE	28480	0180-0198
ABC7	0180-1746	5	3	CAPACITOR-PXO 150PF ±10% 20VDC TA	28480	0180-1746
ABC8	0180-1746	5	3	CAPACITOR-PXO 150PF ±10% 20VDC TA	28480	0180-1746
ABC9	0180-0576	5	3	CAPACITOR-PXO .1UF ±20% 50VDC CER	28480	0180-0576
ABC10	0180-0576	5	3	CAPACITOR-PXO .1UF ±20% 50VDC CER	28480	0180-0576
ABC11	0180-0181	6	3	CAPACITOR-PXO 3.3UF ±10% 35VDC TA	00908	0180-0181
ABC12	0180-0181	6	3	CAPACITOR-PXO 3.3UF ±10% 35VDC TA	00908	0180-0181
ABC13	0180-1746	5	3	CAPACITOR-PXO 150PF ±10% 20VDC TA	28480	0180-1746
ABC14	0180-0576	5	3	CAPACITOR-PXO .1UF ±20% 50VDC CER	28480	0180-0576
ABC15	0180-0181	6	3	CAPACITOR-PXO 3.3UF ±10% 35VDC TA	00908	0180-0181
ABCR1	1701-0539	3	1	DIODE-RECTIFY	28480	1701-0539
ABL1	00355-80017	1	1	COIL, 10MH, SHIELD	28480	00355-80017
ABR1	0498-3195	1	1	RESISTOR 4.04K 1% .125W P TC00±100	24546	0498-3195
ABR2	2100-3355	0	4	RESISTOR-TYMH 100K 10% C BIDE-ADJ 1-TMH	28480	2100-3355
ABR3	0797-0277	5	1	RESISTOR 200K 1% .125W P TC00±100	24546	0797-0277
ABR4				NOT ASSIGNED		
ABR5	0797-0283	6	3	RESISTOR 2K 1% .125W P TC00±100	24546	0797-0283
ABR6	0797-0283	6	3	RESISTOR 2K 1% .125W P TC00±100	24546	0797-0283
ABR7	2100-3355	0	4	RESISTOR-TYMH 100K 10% C BIDE-ADJ 1-TMH	28480	2100-3355
ABR8	2100-3355	0	4	RESISTOR-TYMH 50K 10% C BIDE-ADJ 1-TMH	28480	2100-3355
ABR9	2100-3355	0	4	RESISTOR-TYMH 50K 10% C BIDE-ADJ 1-TMH	28480	2100-3355
ABR10	0797-0283	6	3	RESISTOR 2K 1% .125W P TC00±100	24546	0797-0283
ABR11	0498-0083	8	1	RESISTOR 1.98K 1% .125W P TC00±100	24546	0498-0083
ABR12	0797-0123	3	1	RESISTOR 32.8K 1% .125W P TC00±100	24546	0797-0123
ABR13	0498-3195	4	2	RESISTOR 3.03K 1% .125W P TC00±100	24546	0498-3195
ABR14	2100-3355	0	4	RESISTOR-TYMH 100K 10% C BIDE-ADJ 1-TMH	28480	2100-3355
ABR15	2100-3355	0	4	RESISTOR-TYMH 100K 10% C BIDE-ADJ 1-TMH	28480	2100-3355
ABR16	0797-0442	9	2	RESISTOR 10K 1% .125W P TC00±100	24546	0797-0442
ABR17	0797-0280	3	1	RESISTOR 1K 1% .125W P TC00±100	24546	0797-0280
ABR18	0797-0442	9	2	RESISTOR 10K 1% .125W P TC00±100	24546	0797-0442
ABR19	0498-3195	4	2	RESISTOR 3.03K 1% .125W P TC00±100	24546	0498-3195
ABU1	1826-1417	6	1	IC GATE TTL 6N AND QUAD 2-INP	01295	1826-1417
ABU2	1826-1325	5	1	IC SWITCH ANLG QUAD 1-IN-01P-P	01928	1826-1325
ABU3	1826-0630	3	1	IC MISC TTL	04713	1826-0630
ABU4	1826-1443	6	2	IC OP AMP GP 8-DIP-P	27014	1826-1443
ABU5	1826-0274	3	1	IC 78L15A V RGLTR TO-92	04713	1826-0274
ABU6	1826-0276	3	1	IC 78L05A V RGLTR TO-92	04713	1826-0276
ABU7	1826-0493	6	1	IC OP AMP GP 8-DIP-P	27014	1826-0493
ABU8	1826-0282	3	1	IC 78L15A V RGLTR TO-92	04713	1826-0282
				AS MISCELLANEOUS PARTS		
	0300-1682	0	5	TERMINAL-BLUD BCL-TUR PHLBB-MTC	28480	0300-1682
	0300-0111	0	1	STANDOFF-RVT-ON .25-IN-LG 6-32TND	00000	0300-0111

See introduction to this section for ordering information
*Indicates factory selected value

Model 5355A Replaceable Parts

Table C-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6	06385-PC006	6	1	PRESALER ASSEMBLY (SERIES 1840)	28480	06385-60306
A6C1	0180-3879	7	25	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C2	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	50278-10000221-
A6C3	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C4	0180-3879	7	3	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	1500334-603342
A6C5	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C6	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C7	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C8	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C9	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C10	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C11	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C12	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	1500334-603342
A6C13	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	1500334-603342
A6C14	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C15	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C16	0180-3879	7	2	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	1500334-603342
A6C17	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C18	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	1500334-603342
A6C19	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C20	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C21	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C22	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C23	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C24	0180-3879	7	2	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	1500334-603342
A6C25	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C26	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C27	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C28	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	1500334-603342
A6C29	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C30	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C31	0180-3879	7	5	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	1500334-603342
A6C32	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C33	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	1500334-603342
A6C34	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C35	0180-3879	7	5	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C36	0180-3879	7	5	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	1500334-603342
A6C37	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C38	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C39	0180-3879	7	2	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C40	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C41	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C42	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C43	0180-3879	7	5	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	1500334-603342
A6C44	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C45	0180-3879	7	2	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C46	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	1500334-603342
A6C47	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C48	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	1500334-603342
A6C49	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C50	0180-3879	7	5	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	1500334-603342
A6C51	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C52	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C53	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C54	0180-3879	7	3	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C55	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C56	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C57	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C58	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C59	0180-3879	7	5	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C60	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C61	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C62	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C63	0180-3879	7	2	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C64	0180-3879	7	5	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C65	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C66	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C67	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C68	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C69	0180-3879	7	5	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C70	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C71	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C72	0180-3879	7	2	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C73	0180-3879	7	5	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C74	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C75	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C76	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C77	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C78	0180-3879	7	2	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C79	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C80	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C81	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C82	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C83	0180-3879	7	2	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C84	0180-3879	7	5	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C85	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C86	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C87	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C88	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C89	0180-3879	7	5	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C90	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C91	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C92	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C93	0180-3879	7	2	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C94	0180-3879	7	5	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C95	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C96	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C97	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C98	0180-3879	7	2	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C99	0180-3879	7	1	CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879
A6C100	0180-3879	7		CAPACITOR-PXO .01UF +-20% 100VDC CER	28480	0180-3879

*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6C11	1901-0040	1		DIODE-SWITCHING 10V 30MA 278 DC-35	28480	1901-0040
A6C12	1901-0039	4	2	DIODE-PIN 110V	28480	1001-C630
A6C13	1901-0039	4		DIODE-PIN 110V	28480	1001-0039
A6C14	1902-0028	4	1	DIODE-120V 5% DU-35 PDS,AA TC=0,081	28480	1902-0028
A6D1	1990-0483	5	1	LED-VISIBLE LUM-INTRODUCO 1PP30MA-MAX	28480	1090-0483
A6D2	1990-0487	7	1	LED-VISIBLE LUM-INTRODUCO 1PP22MA-MAX	28480	1090-0487
A6J1	1250-0514	1	1	CONNECTOR-HP 8H-8CN * PC 30-00W	28480	1250-0514
A6L1	9100-1033	0	3	INDUCTOR-HP-CH-MLO 60UH 5% 1000X,389LG	28480	9100-1033
A6L2	9100-1033	0		INDUCTOR-HP-CH-MLO 60UH 5% 1000X,389LG	28480	9100-1033
A6L3	9100-1033	0		INDUCTOR-HP-CH-MLO 60UH 5% 1000X,389LG	28480	9100-1033
A6L4	9100-0941	7	1	INDUCTOR-HP-CH-MLO 250UH 10% 250X,5LG	28480	9100-0941
A6L5	9100-0144	0	2	INDUCTOR-HP-CH-MLO 0.7UH 10% 1050X,26LG	28480	9100-0144
A6L9	9100-2265	0	1	INDUCTOR-HP-CH-MLO 10UH 10% 1050X,26LG	28480	9100-2265
A6L10	9100-0144	0		INDUCTOR-HP-CH-MLO 0.7UH 10% 1050X,26LG	28480	9100-0144
A6L11	9100-2274	7	2	INDUCTOR-HP-CH-MLO 60UH 10% 1050X,26LG	28480	9100-2274
A6L12	05355-00000	0	1	COIL, 4-TURNS	28480	05355-00000
A6L13	05355-00000	0	1	COIL, 2-TURNS	28480	05355-00000
A6L15	9100-2274	7		INDUCTOR-HP-CH-MLO 60UH 10% 1050X,26LG	28480	9100-2274
A6Q1	1853-0038	2	1	TRANSISTOR PNP 81 PDS100W FT230MMZ	28480	1853-0038
A6Q2	1854-0215	1	1	TRANSISTOR NPN 81 PDS100W FT230MMZ	04713	243704
A6Q3	1854-0345	2	2	TRANSISTOR NPN 24379 81 TO-72 PDS200W	04713	243774
A6Q4	1854-0345	2		TRANSISTOR NPN 24379 81 TO-72 PDS200W	04713	243774
A6R1	0690-7260	7	2	RESISTOR 10K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-1002-G
A6R2	0690-7260	7	1	RESISTOR 10K 1% 0.5W F TC=0+-100	24546	0690-7260
A6R3	0690-7261	4	1	RESISTOR 10K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-1002-G
A6R4	0690-7261	4	1	RESISTOR 10K 1% 0.5W F TC=0+-100	24546	0690-7261
A6R5	2100-1030	0	1	RESISTOR-TMR 20K 10% C TOP-ADJ 1-TM	73138	82PM20K
A6R6	2100-1030	0	2	RESISTOR-TMR 5K 10% C TOP-ADJ 1-TM	73138	82PM5K
A6R7	0690-7260	0	5	RESISTOR 511 1% 0.5W F TC=0+-100	24546	C3-1/8-10-511M-G
A6R8	2100-1738	4	3	RESISTOR-TMR 10K 10% C TOP-ADJ 1-TM	73138	82PM10K
A6R9	0690-7261	0	1	RESISTOR 5.1K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-5111-G
A6R10	0690-7260	7	1	RESISTOR 2.15K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-2151-G
A6R11	0690-7260	7	2	RESISTOR 1K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-1001-G
A6R12	0690-7260	0		RESISTOR 511 1% 0.5W F TC=0+-100	24546	C3-1/8-10-511M-G
A6R13	0690-7260	0		RESISTOR 511 1% 0.5W F TC=0+-100	24546	C3-1/8-10-511M-G
A6R14	0690-7260	1	1	RESISTOR 14.7K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-1472-G
A6R15	0690-7260	0	1	RESISTOR 237K 1% 0.5W F TC=0+-100	24546	C4-1/8-10-2373-F
A6R16	0690-7260	1	2	RESISTOR 562 1% 0.5W F TC=0+-100	24546	C3-1/8-10-562M-G
A6R17	0690-7261	0	2	RESISTOR 237 1% 0.5W F TC=0+-100	24546	C3-1/8-10-237M-G
A6R18	0690-7260	7		RESISTOR 1K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-1001-G
A6R19	0690-7260	0		RESISTOR 511 1% 0.5W F TC=0+-100	24546	C3-1/8-10-511M-G
A6R20	0690-7260	1		RESISTOR 562 1% 0.5W F TC=0+-100	24546	C3-1/8-10-562M-G
A6R21	0690-7261	0	1	RESISTOR 1.1K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-1101-G
A6R22	0690-7261	0	1	RESISTOR 14K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-140M-G
A6R23	0690-7260	0	1	RESISTOR 2.37K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-2371-G
A6R24	0690-7260	0	1	RESISTOR 1.78K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-1781-G
A6R25	2100-1738	9		RESISTOR-TMR 10K 10% C TOP-ADJ 1-TM	73138	82PM10K
A6R26	0690-7261	2	3	RESISTOR 7.5K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-7501-G
A6R27	0690-7260	0	1	RESISTOR 51.1 1% 0.5W F TC=0+-100	24546	C3-1/8-10-511M-G
A6R28	0690-7260	4	1	RESISTOR 750 1% 0.5W F TC=0+-100	24546	C3-1/8-10-750M-G
A6R29	0757-0484	7	2	RESISTOR 1.1K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-1101-G
A6R30	0757-0484	7		RESISTOR 1.1K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-1101-G
A6R31	0690-7260	4	1	RESISTOR 75 1% 0.5W F TC=0+-100	24546	C3-1/8-10-750M-G
A6R32	0690-7260	0	2	RESISTOR 100 1% 0.5W F TC=0+-100	24546	C3-1/8-10-100M-G
A6R33	0690-7260	0		RESISTOR 100 1% 0.5W F TC=0+-100	24546	C3-1/8-10-100M-G
A6R34	0811-3468	1	2	RESISTOR 240 1% 0.5W PHS TC=5500+-300	28480	0811-3468
A6R35	0811-3468	1		RESISTOR 240 1% 0.5W PHS TC=5500+-300	28480	0811-3468
A6R36	0690-7260	0	1	RESISTOR 103 1% 0.5W F TC=0+-100	24546	C3-1/8-10-103M-G
A6R37	0690-7261	0	1	RESISTOR 40.9 1% 0.5W F TC=0+-100	24546	C3-1/8-10-409M-G
A6R38	2100-1738	9	1	RESISTOR-TMR 1K 10% C TOP-ADJ 1-TM	73138	82PM1K
A6R39	0690-7261	2		RESISTOR 7.5K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-7501-G
A6R40	0690-7260	0		RESISTOR 511 1% 0.5W F TC=0+-100	24546	C3-1/8-10-511M-G
A6R41	0690-7261	2	1	RESISTOR 61.9 1% 0.5W F TC=0+-100	24546	C3-1/8-10-619M-G
A6R42	2100-2210	0		RESISTOR-TMR 5K 10% C TOP-ADJ 1-TM	73138	82PM5K
A6R43	0690-7261	0		RESISTOR 237 1% 0.5W F TC=0+-100	24546	C3-1/8-10-237M-G
A6R44	2100-1738	9		RESISTOR-TMR 10K 10% C TOP-ADJ 1-TM	73138	82PM10K
A6R45	0690-7261	2		RESISTOR 7.5K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-7501-G
A6R46	0690-7260	7		RESISTOR 10K 1% 0.5W F TC=0+-100	24546	C3-1/8-10-1002-G
A6R47	0690-5378	0	1	RESISTOR 100 10% 1K C TC=0+-200	28480	3C10K
A6R48	0690-7184	0	1	RESISTOR 10 1% 0.5W F TC=0+-100	24546	C3-1/8-10-10M-G
A6T1	0839-0008	7	1	THERMISTOR 0.5C 1K-00W TC=0.02/C-DEG	28480	0839-0008

See introduction to this section for ordering information.
*Indicates factory selected value.

Model 5355A Replaceable Parts

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
161P1	1281-0000	0	1	CONNECTOR-BGL CONT PIN 1, 16-11-1000-02 02	2240	1281-0000
161P2	1281-0000	0	1	CONNECTOR-BGL CONT PIN 1, 16-11-1000-02 02	2240	1281-0000
161P3	1281-0000	0	1	CONNECTOR-BGL CONT PIN 1, 16-11-1000-02 02	2240	1281-0000
161P4	1281-0000	0	1	CONNECTOR-BGL CONT PIN 1, 16-11-1000-02 02	2240	1281-0000
161P5	1281-0000	0	1	CONNECTOR-BGL CONT PIN 1, 16-11-1000-02 02	2240	1281-0000
161J1	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J2	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J3	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J4	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J5	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J6	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J7	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J8	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J9	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J10	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J11	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J12	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J13	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J14	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J15	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J16	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J17	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J18	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J19	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J20	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J21	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J22	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J23	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J24	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J25	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J26	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J27	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J28	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J29	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J30	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J31	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J32	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J33	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J34	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J35	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J36	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J37	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J38	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J39	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J40	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J41	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J42	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J43	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J44	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J45	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J46	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J47	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J48	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J49	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J50	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J51	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J52	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J53	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J54	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J55	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J56	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J57	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J58	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J59	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J60	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J61	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J62	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J63	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J64	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J65	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J66	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J67	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J68	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J69	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J70	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J71	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J72	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J73	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J74	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J75	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J76	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J77	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J78	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J79	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J80	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J81	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J82	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J83	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J84	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J85	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J86	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J87	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J88	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J89	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J90	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J91	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J92	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J93	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J94	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J95	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J96	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J97	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J98	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J99	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J100	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J101	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J102	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J103	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J104	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J105	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J106	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J107	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J108	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J109	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J110	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J111	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J112	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J113	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J114	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J115	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J116	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J117	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J118	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J119	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J120	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J121	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J122	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J123	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J124	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J125	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J126	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J127	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J128	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J129	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J130	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J131	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J132	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J133	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J134	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J135	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J136	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J137	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J138	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J139	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J140	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J141	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J142	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J143	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J144	1280-0000	0	1	IC COMPANATOR MB 14-DIP-0	27014	1280-0000
161J145						

*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7	06368-60007	7	1	MICROPROCESSOR ASSEMBLY (SERIES 1628)	28480	06368-60007
A7C1	0180-3879	7	7	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0180-3879
A7C2				NOT ASSIGNED		
A7C3	0180-3879	7	7	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0180-3879
A7C4	0180-3879	7	7	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0180-3879
A7C5	0180-3879	7	7	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0180-3879
A7C6	0180-3879	7	7	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0180-3879
A7C7	0180-3879	7	7	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0180-3879
A7C8	0180-3879	7	7	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0180-3879
A7C9	0180-3879	7	7	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0180-3879
A7C10	0180-3879	7	7	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0180-3879
A7C11	1901-0535	9	8	DIODE-SC-HOTTY	28480	1901-0535
A7C12	1901-0535	9	8	DIODE-SC-HOTTY	28480	1901-0535
A7C13	1901-0535	9	8	DIODE-SC-HOTTY	28480	1901-0535
A7C14	1901-0535	9	8	DIODE-SC-HOTTY	28480	1901-0535
A7L1	9100-1788	4	1	CHROME-NICE BAND ZMARF600 OHMS 180 MHZ	02114	9100-1788
A7R1	0757-0442	9	8	RESISTOR 10K 1% .125W P TC00+-100	28480	0757-0442
A7R2	0757-0442	9	8	RESISTOR 10K 1% .125W P TC00+-100	28480	0757-0442
A7R3	0757-0442	9	8	RESISTOR 10K 1% .125W P TC00+-100	28480	0757-0442
A7R4	0757-0442	9	8	RESISTOR 10K 1% .125W P TC00+-100	28480	0757-0442
A7R5	0757-0442	9	8	RESISTOR 10K 1% .125W P TC00+-100	28480	0757-0442
A7R6	0757-0442	9	8	RESISTOR 10K 1% .125W P TC00+-100	28480	0757-0442
A7R7	0757-0442	9	8	RESISTOR 10K 1% .125W P TC00+-100	28480	0757-0442
A7R8	0757-0442	9	8	RESISTOR 10K 1% .125W P TC00+-100	28480	0757-0442
A7R9	0757-0442	9	8	RESISTOR 10K 1% .125W P TC00+-100	28480	0757-0442
A7R10	0757-0442	9	8	RESISTOR 10K 1% .125W P TC00+-100	28480	0757-0442
A7S1	3101-1856	4	1	SWITCH-RL 8-1A DIP-8LICE-ARRY .1A 30VDC	28480	3101-1856
A7TP1	0300-1882	0	11	TERMINAL-STUD SGL-TUP PRESS-MTC	28480	0300-1882
A7TP2	0300-1882	0	11	TERMINAL-STUD SGL-TUP PRESS-MTC	28480	0300-1882
A7TP3	0300-1882	0	11	TERMINAL-STUD SGL-TUP PRESS-MTC	28480	0300-1882
A7TP4	0300-1882	0	11	TERMINAL-STUD SGL-TUP PRESS-MTC	28480	0300-1882
A7TP5	0300-1882	0	11	TERMINAL-STUD SGL-TUP PRESS-MTC	28480	0300-1882
A7TP6	0300-1882	0	11	TERMINAL-STUD SGL-TUP PRESS-MTC	28480	0300-1882
A7TP7	0300-1882	0	11	TERMINAL-STUD SGL-TUP PRESS-MTC	28480	0300-1882
A7TP8	0300-1882	0	11	TERMINAL-STUD SGL-TUP PRESS-MTC	28480	0300-1882
A7TP9	0300-1882	0	11	TERMINAL-STUD SGL-TUP PRESS-MTC	28480	0300-1882
A7TP10	0300-1882	0	11	TERMINAL-STUD SGL-TUP PRESS-MTC	28480	0300-1882
A7TP11	0300-1882	0	11	TERMINAL-STUD SGL-TUP PRESS-MTC	28480	0300-1882
A7U1	1820-2137	9	1	IC MICPROC 4808 8-BIT	04713	1820-2137
A7U2	1820-1917	1	2	IC BPR TTL LB LINE DRVR OCTL	01295	1820-1917
A7U3	1820-1917	1	2	IC BPR TTL LB LINE DRVR OCTL	01295	1820-1917
A7U4	1820-1199	1	1	IC INV TTL LB HEX 1-INP	01295	1820-1199
A7U5	1820-0894	9	1	PROGRAM ROM 4K 2-B (PART NO 05355-80010 USED FOR US ON EARLY MODELS)	01295	1820-0894
A7U6	1820-0433	0	4	SOCKET-IC 24-CONT	28480	1820-0433
A7U7	1820-1197	9	2	IC GATE TTL LB NAND QUAD 2-INP	01295	1820-1197
A7U8	1820-1197	9	2	IC GATE TTL LB NAND QUAD 2-INP	01295	1820-1197
A7U9	1820-0433	0	4	IC 4808 4808 RAM STAT 280-NS 3-B	01295	1820-0433
A7U10	1820-0433	0	4	IC 4808 4808 RAM STAT 280-NS 3-B	01295	1820-0433
A7U11	1820-0433	0	4	IC 4808 4808 RAM STAT 280-NS 3-B	01295	1820-0433
A7U12	1820-0433	0	4	IC 4808 4808 RAM STAT 280-NS 3-B	01295	1820-0433
A7U13	1820-1207	2	1	IC GATE TTL LB NAND 8-INP	01295	1820-1207
A7U14	1820-1207	2	1	IC GATE TTL LB NAND 8-INP	01295	1820-1207
A7U15	1820-0525	1	4	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0525
A7U16	1820-1201	2	1	IC DECM TTL LB 2-TO-4-LINE OUAL 2-INP	01295	1820-1201
A7U17	1820-1201	2	1	IC GATE TTL LB NAND TPL 3-INP	01295	1820-1201
A7U18	1820-1197	9	2	IC GATE TTL LB NAND QUAD 2-INP	01295	1820-1197
A7XU1	1820-0532	4	1	SOCKET-IC 40-CONT DIP-8LDR	28480	1820-0532
A7XU2	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU3	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU4	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU5	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU6	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU7	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU8	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU9	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU10	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU11	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU12	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU13	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU14	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU15	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU16	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU17	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU18	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU19	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU20	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU21	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU22	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU23	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU24	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU25	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU26	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU27	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU28	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU29	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU30	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU31	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU32	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU33	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU34	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU35	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU36	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU37	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU38	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU39	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU40	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU41	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU42	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU43	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU44	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU45	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU46	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU47	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU48	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU49	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU50	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU51	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU52	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU53	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU54	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU55	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU56	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU57	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU58	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU59	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU60	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU61	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU62	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU63	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU64	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU65	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU66	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU67	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU68	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU69	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU70	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU71	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU72	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU73	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU74	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU75	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU76	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU77	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU78	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU79	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU80	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU81	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU82	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU83	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR	28480	1820-0532
A7XU84	1820-0532	4	1	SOCKET-IC 20-CONT DBL STMP DIP-8LDR		

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
AP	05355-60008	8	1	DECODER-HP-IB ASSEMBLY (SERIES 1840)	28480	05355-60008
ABC1	0160-3879	7	12	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
ABC2	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
ABC3	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
ABC4	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
ABC5	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
ABC6	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
ABC7	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
ABC8	0160-0106	4	1	CAPACITOR-PXD 50UF+-20% 4VDC TA	28480	15000001PC0004
ABC9	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
ABC10	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
ABC11	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
ABC12	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
ABC13	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
ABL1	9100-1788	6	1	CHOKER-WIDE BAND ZWAFER-BED OHM 180 MHZ	02114	91200 30118
ABR1	0757-0901	0	2	RESISTOR 100 1% .125W P TCHO+-100	24546	CW-1/P-10-101MF
ABR2	0698-4009	6	1	RESISTOR 50K 1% .125W P TCHO+-100	24546	CW-1/P-10-5002MF
ABR3	0757-0902	0	1	RESISTOR 10K 1% .125W P TCHO+-100	24546	CW-1/P-10-1002MF
ABR4	0757-0901	0		RESISTOR 100 1% .125W P TCHO+-100	24546	CW-1/P-10-101MF
ABR5	0698-3190	6	3	RESISTOR 2.37K 1% .125W P TCHO+-100	24546	CW-1/P-10-2371MF
ABR6	0698-3190	6		RESISTOR 2.37K 1% .125W P TCHO+-100	24546	CW-1/P-10-2371MF
ABR7	0698-3190	6		RESISTOR 2.37K 1% .125W P TCHO+-100	24546	CW-1/P-10-2371MF
ABTP1	0360-1682	0	3	TERMINAL-8TUD SGL-TUR PRESS-MTG	28480	0360-1682
ABTP2	0360-1682	0		TERMINAL-8TUD SGL-TUR PRESS-MTG	28480	0360-1682
ABTP3	0360-1682	0		TERMINAL-8TUD SGL-TUR PRESS-MTG	28480	0360-1682
ABU1	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	874LB004N
ABU2	1820-1206	1	1	IC GATE TTL LS NON TPL 3-INP	01295	874LB274N
ABU3	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	874LB004N
ABU4	1820-1197	9	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	874LB374N
ABU5	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	874LB374N
ABU6	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	874LB374N
ABU7	1820-1284	5	1	IC GATE TTL LS AND-OR-INV 8-INP	01295	874LB554N
ABU8	1820-0621	2	1	IC BFR TTL NAND QUAD 2-INP	01295	874LB34N
ABU9	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	874LB304N
ABU10	1820-1196	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG CCH	01295	874LB174N
ABU11	1820-1212	7	1	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	874LB1124N
ABU12	1820-1212	7	1	IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	874LB1094N
ABU13	1820-1295	0	1	IC INV TTL HEX 1-INP	01295	874LB004N
ABU14	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	874LB104N
ABU15	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	874LB004N
ABU16	1820-1211	8	2	IC GATE TTL LS 1-INCL-OR QUAD 2-INP	01295	874LB484N
ABU17	1820-1197	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	874LB374N
ABU18	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	874LB384N
ABU19	1820-1200	7	1	IC INV TTL LS HEX	01295	874LB004N
ABU20				NOT ASSIGNED		
ABU21	1820-1117	1	1	IC BFR TTL LS LINE CHN OCTL	01295	874LB274N
ABU22	1820-1216	1	3	IC OCMR TTL LS 3-TO-8-LINE 3-INP	01295	874LB1384N
ABU23	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	874LB004N
ABU24	1820-1216	3		IC OCMR TTL LS 3-TO-8-LINE 3-INP	01295	874LB1384N
ABU25	1820-1216	3		IC OCMR TTL LS 3-TO-8-LINE 3-INP	01295	874LB1384N
ABXU1	1200-0639	8	3	SOCKET-IC 20-CONT DIP DIP-8LDR	28480	1200-0639
ABXU2	1200-0673	8	1	SOCKET-IC 18-CONT DIP DIP-8LDR	28480	1200-0673
ABXU3	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-8LDR	28480	1200-0639
ABXU4	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-8LDR	28480	1200-0639
				AB MISCELLANEOUS PARTS		
	1480-0116	8	1	MIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
	5040-9043	4	1	PIV-P.C. BOARD EXTRACTOR	28480	5040-9043
	5040-1464	3	1	EXTRACTOR, PC BOARD	28480	5040-1464
	5040-6883	4	1	EXTRACTOR, PC BOARD, HMDAN	28480	5040-6883

See introduction to this section for ordering information.
* Indicates factory selected value.

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
AN	09359-60009	9	1	INTERFACE ASSEMBLY (SERIES 1840)	28480	09359-60009
ANC1	0180-1879	7	2	CAPACITOR-PAD .01UF +-20% 100VDC CER	28480	0180-1879
ANC2	0180-1879	7	2	CAPACITOR-PAD .01UF +-20% 100VDC CER	28480	0180-1879
ANC3	0180-0870	9	2	CAPACITOR-PAD 220PF +-20% 100VDC CER	28480	0180-0870
ANC4	0180-0870	9	2	CAPACITOR-PAD 220PF +-20% 100VDC CER	28480	0180-0870
ANC5	0180-1878	9	1	CAPACITOR-PAD 1000PF +-20% 100VDC CER	28480	0180-1878
ANC6	0180-1879	7	2	CAPACITOR-PAD .01UF +-20% 100VDC CER	28480	0180-1879
ANC7	0180-0829	7	1	CAPACITOR-PAD .01UF +-20% 10VDC TA	28480	0180-0829
ANC8	0180-1879	7	2	CAPACITOR-PAD .01UF +-20% 100VDC CER	28480	0180-1879
ANC9	1901-0535	9	1	DIODE-SC-OTVNY	28480	1901-0535
ANC10	1901-0535	9	1	DIODE-SC-OTVNY	28480	1901-0535
ANL1	9100-1788	8	1	CLOCK-PRICE BAND IMAR-600 OHMS 180 MHz	02114	9100-1788
ANR1	0757-0924	2	1	RESISTOR 1/4W 120VDC TC 0-100	28480	0757-0924
AQU1	1020-1202	7	2	IC GATE TTL LS NAND TTL 3-INP	01295	1020-1202
AQU2	1020-1196	0	1	IC GATE TTL LS NAND GUAL 3-INP	01295	1020-1196
AQU3	1020-1196	1	1	IC INV TTL LS HEX 1-INP	01295	1020-1196
AQU4	1020-1204	9	2	IC GATE TTL LS NAND DUAL 4-INP	01295	1020-1204
AQU5	1020-1192	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	1020-1192
AQU6	1020-1202	7	2	IC GATE TTL LS NAND TTL 3-INP	01295	1020-1202
AQU7	1020-1196	0	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	1020-1196
AQU8	1020-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	1020-1204
AQU9	1020-1203	3	1	IC CNT9 TTL LS 814 SYNCHRO POS-EDGE-TRIG	01295	1020-1203
AQU10	1020-1203	8	1	IC GATE TTL LS AND GUAL 2-INP	01295	1020-1203
AQU11	1018-1189	9	2	IC TTL LS 8N-BIT RAM STAT 80-NS 3-B	27014	1018-1189
AQU12	1018-1189	9	2	IC TTL LS 8N-BIT RAM STAT 80-NS 3-B	27014	1018-1189
AQU13	1020-1196	0	1	IC BUFF-DRTR TTL LS R-B PRL-IN PRL-OUT	01295	1020-1196
AQU14	1020-1196	1	1	IC RFR TTL LS INV HEX 1-INP	01295	1020-1196
AQU15	1020-1194	7	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	1020-1194
AQU16	1020-1195	7	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	1020-1195
AQU17	1020-1195	7	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	1020-1195
AQU18	1020-1195	7	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	1020-1195
AQU19	1020-1195	7	2	IC SCHMITT-TRIG TTL LS NAND DUAL 4-INP	01295	1020-1195
AQU20	1020-1204	9	2	IC BUFF-DRTR TTL LS R-B PRL-IN PRL-OUT	01295	1020-1204
AQU21	1200-0473	8	7	SOCKET-IC 16-CONT DIP DIP-BLDR	28480	1200-0473
AQU22	1200-0473	8	7	SOCKET-IC 16-CONT DIP DIP-BLDR	28480	1200-0473
AQU23	1200-0474	9	2	SOCKET-IC 16-CONT DIP DIP-BLDR	28480	1200-0474
AQU24	1200-0473	8	7	SOCKET-IC 16-CONT DIP DIP-BLDR	28480	1200-0473
AQU25	1200-0473	8	7	SOCKET-IC 16-CONT DIP DIP-BLDR	28480	1200-0473
AQU26	1200-0473	8	7	SOCKET-IC 16-CONT DIP DIP-BLDR	28480	1200-0473
AQU27	1200-0473	8	7	SOCKET-IC 16-CONT DIP DIP-BLDR	28480	1200-0473
AQU28	1200-0473	8	7	SOCKET-IC 16-CONT DIP DIP-BLDR	28480	1200-0473
AQU29	1200-0474	9	2	SOCKET-IC 16-CONT DIP DIP-BLDR	28480	1200-0474
AN MISCELLANEOUS PARTS						
	0180-1882	0	2	TERMINAL-BYD SOL-TUN PRESC-MTG	28480	0180-1882
	1480-0116	8	1	PTH-GRV .0482-IN-DIA .28-IN-LG ETL	28480	1480-0116
	5000-9043	3	1	PTH-P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-1484	3	1	EXTRACTOR, PC BOARD	28480	5040-1484
	5040-8247	8	1	EXTRACTOR, PC BOARD, RLD	28480	5040-8247

See introduction to this section for ordering information.
* Indicates factory selected value.

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10	05355-60010	2	1	PSEUDORANDOM SEQUENCE GENERATOR ASSEMBLY (SERIES 1840)	28480	05355-60010
A10C1	0180-3879	7	3	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0180-3879
A10C2	0180-0576	5	3	CAPACITOR-PXD .1UF +-20% 50VDC CER	28480	0180-0576
A10C3	0180-0576	8	3	CAPACITOR-PXD .1UF +-20% 50VDC CER	28480	0180-0576
A10C4	0180-0576	5	3	CAPACITOR-PXD .1UF +-20% 50VDC CER	28480	0180-0576
A10C5	0180-2811	7	3	CAPACITOR-PXD .01UF +-20% 35VDC TA	28480	0180-2811
A10C6	0180-2811	7	3	CAPACITOR-PXD .01UF +-20% 35VDC TA	28480	0180-2811
A10C7	0180-2811	7	3	CAPACITOR-PXD .01UF +-20% 35VDC TA	28480	0180-2811
A10C8	0180-3879	7	3	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0180-3879
A10C9	0180-3879	7	3	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0180-3879
A10L1	9100-1768	6	3	CHOKENRICE BAND ZMAR680 OHMS 180 MHZ	02114	17200 20748
A10L2	9100-1768	6	3	CHOKENRICE BAND ZMAR680 OHMS 180 MHZ	02114	17200 20748
A10L3	9100-1768	6	3	CHOKENRICE BAND ZMAR680 OHMS 180 MHZ	02114	17200 20748
A10R1	0698-7252	7	1	RESISTOR 4.0K 1% .05W P TCR0+-100	28480	C3-1/8-10-48H-G
A10R2	0698-7250	7	1	RESISTOR 10K 1% .05W P TCR0+-100	28480	C3-1/8-10-100H-G
A10R3	0698-7251	0	1	RESISTOR 51.1 K 1% .05W P TCR0+-100	28480	C3-1/8-100-51H-G
A10U1	1820-1882	7	3	IC CNTR TTL LB DECO ASYNCHRO	01295	874682904
A10U2	1820-1802	7	1	IC GATE TTL LB NAND TPL 3-INP	01295	874681004
A10U3	1820-1833	8	2	IC SHF-RSTR TTL LB N-S SERIAL-IN PNL-CUT	01295	874681804
A10U4	1820-1455	8	2	IC SHF-RSTR TTL LB N-S SERIAL-IN PNL-CUT	01295	874681804
A10U5	1820-1112	8	2	IC FF TTL LB D-TYPE POS-EDGE-TRIG	01295	874687404
A10U6	1820-1112	8	2	IC FF TTL LB D-TYPE POS-EDGE-TRIG	01295	874687404
A10U7	1820-1147	9	3	IC GATE TTL LB NAND QUAD 2-INP	01295	874680004
A10U8	1820-1830	3	1	IC CNTR TTL LB B1N ASYNCHRO POS-EDGE-TRIG	01295	874681804
A10U9	1820-1211	8	1	IC GATE TTL LB EXCL-OR QUAD 2-INP	01295	874682604
A10U10	1820-1147	9	3	IC GATE TTL LB NAND QUAD 2-INP	01295	874680004
A10U11	1820-1147	9	3	IC GATE TTL LB NAND QUAD 2-INP	01295	874680004
A10U12	1820-1146	8	1	IC FF TTL LB D-TYPE POS-EDGE-TRIG COM	01295	874681704
A10U13	1820-1149	1	1	IC INV TTL LB HEX 1-INP	01295	874680404
A10U14	1820-1442	7	3	IC CNTR TTL LB DECO ASYNCHRO	01295	874682904
A10U15	1820-1442	7	3	IC CNTR TTL LB DECO ASYNCHRO	01295	874682904
A10U16	1820-0132	2	1	IC COMPARATOR NB 14-DIP-C	07263	UAT600C
				A10 MISCELLANEOUS PARTS		
	0360-1882	0	9	TERMINAL-STUD BCL-TUR PRESS-MTC	28480	0360-1882
	1480-0114	8	1	PIN-GRV .002-IN DIA .25-IN LG STL	28480	1480-0114
	9000-9043	6	1	PIN-P.C. BOARD EXTRACTOR	28480	9000-9043
	9040-1864	3	1	EXTRACTOR, PC BOARD	28480	9040-1864
	9040-8852	3	1	EXTRACTOR, PC BOARD, ORANGE	28480	9040-8852

See introduction to this section for ordering information.
*Indicates factory selected value.

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11	00355-60011	3	1	SIGNAL SWITCH ASSEMBLY (S1 HEB 1028)	28480	00355-60011
A11C1	0160-3879	7	13	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C2	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C3	0160-4554	1	4	CAPACITOR-PXD .01UF +-20% 10VDC TA	28480	0160-4554
A11C4	0160-4554	1		CAPACITOR-PXD .01UF +-20% 10VDC TA	28480	0160-4554
A11C5	0160-4554	7	10	CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	0160-4554
A11C6	0160-4554	1		CAPACITOR-PXD .01UF +-20% 10VDC TA	28480	0160-4554
A11C7	0160-4554	1		CAPACITOR-PXD .01UF +-20% 10VDC TA	28480	0160-4554
A11C8	0160-4554	7		CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	0160-4554
A11C9	0160-4554	7		CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	0160-4554
A11C10	0160-4554	7		CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	0160-4554
A11C11	0160-4554	7		CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	0160-4554
A11C12	0160-4554	7	1	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-4554
A11C13	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C14	0160-4554	7		CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	0160-4554
A11C15	0160-4554	7	1	CAPACITOR-PXD .01UF +-20% 200VDC CER 0+-10	28480	0160-4554
A11C16	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C17	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C18	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C19	0160-4554	7		CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	0160-4554
A11C20	0160-4554	7		CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	0160-4554
A11C21	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C22	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C23	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C24	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C25	0160-4554	7		CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	0160-4554
A11C26	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C27	0160-4554	7		CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	0160-4554
A11C28	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C29	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C30	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C31	1901-1097	0	6	DIODE-PIN	28480	1901-1097
A11C32	1901-1097	0		DIODE-PIN	28480	1901-1097
A11C33	1901-1097	0		DIODE-PIN	28480	1901-1097
A11C34	1901-1097	0		DIODE-PIN	28480	1901-1097
A11C35	1901-1097	0		DIODE-PIN	28480	1901-1097
A11C36	1901-1097	0		DIODE-PIN	28480	1901-1097
A11J1	1250-0036	2	4	CONNECTOR-RF BNC M PC 50-OHM	28480	1250-0036
A11J2	1250-0036	2		CONNECTOR-RF BNC M PC 50-OHM	28480	1250-0036
A11J3	1250-0036	2		CONNECTOR-RF BNC M PC 50-OHM	28480	1250-0036
A11J4	1250-0036	2		CONNECTOR-RF BNC M PC 50-OHM	28480	1250-0036
A11L1	9100-0541	7	2	INDUCTOR-RF CH-MLD 250UH 10% 250K,SLG	28480	9100-0541
A11L2	9100-0541	7		INDUCTOR-RF CH-MLD 250UH 10% 250K,SLG	28480	9100-0541
A11L3	9100-2265	2	2	INDUCTOR-RF CH-MLD 10UH 10% 1050K,2xLG	28480	9100-2265
A11L4	9100-2265	2		INDUCTOR-RF CH-MLD 10UH 10% 1050K,2xLG	28480	9100-2265
A11M1	1894-0215	1	6	TRANSISTOR NPN B1 PD0350MH FTY300MHZ	04713	1894-0215
A11M2	1894-0215	1		TRANSISTOR NPN B1 PD0350MH FTY300MHZ	04713	1894-0215
A11M3	1894-0215	1		TRANSISTOR NPN B1 PD0350MH FTY300MHZ	04713	1894-0215
A11M4	1894-0215	1		TRANSISTOR NPN B1 PD0350MH FTY300MHZ	04713	1894-0215
A11M5	1894-0215	1		TRANSISTOR NPN B1 PD0350MH FTY300MHZ	04713	1894-0215
A11M6	1894-0215	1		TRANSISTOR NPN B1 PD0350MH FTY300MHZ	04713	1894-0215
A11M7	1893-0058	2	3	TRANSISTOR NPN B1 PD0300MH FTY200MHZ	07263	1893-0058
A11M8	1893-0058	2		TRANSISTOR NPN B1 PD0300MH FTY200MHZ	07263	1893-0058
A11M9	1893-0058	2		TRANSISTOR NPN B1 PD0300MH FTY200MHZ	07263	1893-0058
A11M10	1894-0345	2	1	TRANSISTOR NPN B1 PD0350MH FTY300MHZ	04713	1894-0345
A11N1	0698-7205	0	2	RESISTOR 51.1 K 1% 125W F TC00+-100	24546	0698-7205
A11N2	0698-7212	0	2	RESISTOR 100 K 1% 125W F TC00+-100	24546	0698-7212
A11N3	0698-7204	0	2	RESISTOR 46.4 K 1% 125W F TC00+-100	24546	0698-7204
A11N4	0698-7205	0		RESISTOR 51.1 K 1% 125W F TC00+-100	24546	0698-7205
A11N5	0698-7212	0		RESISTOR 100 K 1% 125W F TC00+-100	24546	0698-7212
A11N6	0698-7204	0		RESISTOR 46.4 K 1% 125W F TC00+-100	24546	0698-7204
A11N7	0757-0405	4	3	RESISTOR 162 K 1% 125W F TC00+-100	24546	0757-0405
A11N8	0757-0405	4		RESISTOR 162 K 1% 125W F TC00+-100	24546	0757-0405
A11N9	0757-0405	4		RESISTOR 162 K 1% 125W F TC00+-100	24546	0757-0405
A11N10	0757-0405	4		RESISTOR 162 K 1% 125W F TC00+-100	24546	0757-0405
A11R11	0698-3155	1	5	RESISTOR 4.64K 1% 125W F TC00+-100	24546	0698-3155
A11R12	0757-0405	3	2	RESISTOR 150 K 1% 125W F TC00+-100	24546	0757-0405
A11R13	0757-0405	3		RESISTOR 150 K 1% 125W F TC00+-100	24546	0757-0405
A11R14	0698-3155	1	3	RESISTOR 237 K 1% 125W F TC00+-100	24546	0698-3155
A11R15	0698-3155	1		RESISTOR 4.64K 1% 125W F TC00+-100	24546	0698-3155
A11R16	0757-0405	4	1	RESISTOR 6.81K 1% 125W F TC00+-100	24546	0757-0405
A11R17	0698-3155	4	3	RESISTOR 2.15K 1% 125W F TC00+-100	24546	0698-3155
A11R18	0698-3155	4		RESISTOR 3.48K 1% 125W F TC00+-100	24546	0698-3155
A11R19	0698-3155	4		RESISTOR 2.61K 1% 125W F TC00+-100	24546	0698-3155
A11R20	0698-3155	1		RESISTOR 4.64K 1% 125W F TC00+-100	24546	0698-3155

See introduction to this section for ordering information.
*Indicates factory selected value.

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	U D	Qty	Description	Mfr Code	Mfr Part Number
A11R21	0698-3132	8	1	RESISTOR 201 1% .125W P TC00+-100	24546	Cu=1/8-T0-2010-P
A11R22	0698-3482	9	1	RESISTOR 237 1% .125W P TC00+-100	24546	Cu=1/8-T0-2370-P
A11R23	0757-0743	6	1	RESISTOR 24 1% .125W P TC00+-100	24546	Cu=1/8-T0-2401-P
A11R24	0698-3410	5	1	RESISTOR 21.5 1% .125W P TC00+-100	03888	Pu=55-1/8-T0-2145-P
A11R25	0698-3433	8	1	RESISTOR 28.7 1% .125W P TC00+-100	03888	Pu=150-1/8-T0-2870-P
A11R26	0757-1094	4	1	RESISTOR 1.47K 1% .125W P TC00+-100	24546	Cu=1/8-T0-1471-P
A11R27	0757-1094	9	1	RESISTOR 1.47K 1% .125W P TC00+-100	24546	Cu=1/8-T0-1471-P
A11R28	0698-0068	0	1	RESISTOR 2.61P 1% .125W P TC00+-100	24546	Cu=1/8-T0-2611-P
A11R29	0698-3139	1	1	RESISTOR 4.04K 1% .125W P TC00+-100	24546	Cu=1/8-T0-4041-P
A11R30	0698-3139	8	1	RESISTOR 3.02K 1% .125W P TC00+-100	24546	Cu=1/8-T0-3021-P
A11R31	0698-0088	9	1	RESISTOR 2.15K 1% .125W P TC00+-100	24546	Cu=1/8-T0-2151-P
A11R32	0698-0088	0	1	RESISTOR 2.15K 1% .125W P TC00+-100	24546	Cu=1/8-T0-2151-P
A11R33	0698-0172	2	1	RESISTOR 3.02K 1% .125W P TC00+-100	24546	Cu=1/8-T0-3021-P
A11R34	0757-0416	7	1	RESISTOR 51.1 1% .125W P TC00+-100	24546	Cu=1/8-T0-5110-P
A11R35	0698-0088	0	1	RESISTOR 2.01K 1% .125W P TC00+-100	24546	Cu=1/8-T0-2011-P
A11R36	0757-0447	4	1	RESISTOR 16.2K 1% .125W P TC00+-100	24546	Cu=1/8-T0-1622-P
A11R37	0757-0394	0	2	RESISTOR 51.1 1% .125W P TC00+-100	24546	Cu=1/8-T0-5111-P
A11R38	0698-3133	1	1	RESISTOR 4.04K 1% .125W P TC00+-100	24546	Cu=1/8-T0-4041-P
A11R39	0698-3442	9	1	RESISTOR 237 1% .125W P TC00+-100	24546	Cu=1/8-T0-2370-P
A11R40	0757-0394	0	1	RESISTOR 51.1 1% .125W P TC00+-100	24546	Cu=1/8-T0-5111-P
A11R41	0698-3434	9	2	RESISTOR 34.2 1% .125W P TC00+-100	24546	Cu=1/8-T0-3420-P
A11R42	2100-2489	9	2	RESISTOR-TM4 5K 10% C SIDE-ADJ 1-TM4	30483	ETS 1302
A11R43	0757-0428	7	3	RESISTOR 1.1K 1% .125W P TC00+-100	24546	Cu=1/8-T0-1101-P
A11R44	0757-0316	8	1	RESISTOR 42.2 1% .125W P TC00+-100	24546	Cu=1/8-T0-4220-P
A11R45	0698-3444	3	1	RESISTOR 103 1% .125W P TC00+-100	24546	Cu=1/8-T0-1030-P
A11R46	2100-2489	9	1	RESISTOR-TM4 5K 10% C SIDE-ADJ 1-TM4	30483	ETS1302
A11R47	0757-0438	3	2	RESISTOR 4.11K 1% .125W P TC00+-100	24546	Cu=1/8-T0-4111-P
A11R48	0757-0414	7	1	RESISTOR 1.1K 1% .125W P TC00+-100	24546	Cu=1/8-T0-1101-P
A11R49	0698-3434	3	1	RESISTOR 107 1% .125W P TC00+-100	24546	Cu=1/8-T0-1070-P
A11R50	0757-0438	3	1	RESISTOR 4.11K 1% .125W P TC00+-100	24546	Cu=1/8-T0-4111-P
A11R51	0757-C401	0	2	RESISTOR 100 1% .125W P TC00+-100	24546	Cu=1/8-T0-1010-P
A11R52	0757-C401	0	1	RESISTOR 100 1% .125W P TC00+-100	24546	Cu=1/8-T0-1010-P
A11R53	0757-0428	9	1	RESISTOR 1.1K 1% .125W P TC00+-100	24546	Cu=1/8-T0-1101-P
A11R54	0757-0400	7	2	RESISTOR 90.9 1% .125W P TC00+-100	24546	Cu=1/8-T0-9090-P
A11R55	0698-3434	9	1	RESISTOR 34.2 1% .125W P TC00+-100	24546	Cu=1/8-T0-3420-P
A11R56	0757-0400	9	1	RESISTOR 90.9 1% .125W P TC00+-100	24546	Cu=1/8-T0-9090-P
A11TP1	0360-1682	2	10	TERMINAL-STUD SGL-TUP PREBB-MTC	28480	0360-1682
A11TP2	0360-1682	0	10	TERMINAL-STUD SGL-TUP PREBB-MTC	28480	0360-1682
A11TP3	0360-1682	0	10	TERMINAL-STUD SGL-TUP PREBB-MTC	28480	0360-1682
A11TP4	0360-1682	0	10	TERMINAL-STUD SGL-TUP PREBB-MTC	28480	0360-1682
A11TP5	0360-1682	0	10	TERMINAL-STUD SGL-TUP PREBB-MTC	28480	0360-1682
A11TP6	0360-1682	0	10	TERMINAL-STUD SGL-TUP PREBB-MTC	28480	0360-1682
A11TP7	0360-1682	0	10	TERMINAL-STUD SGL-TUP PREBB-MTC	28480	0360-1682
A11TP8	0360-1682	0	10	TERMINAL-STUD SGL-TUP PREBB-MTC	28480	0360-1682
A11TP9	0360-1682	0	10	TERMINAL-STUD SGL-TUP PREBB-MTC	28480	0360-1682
A11TP10	0360-1682	0	10	TERMINAL-STUD SGL-TUP PREBB-MTC	28480	0360-1682
A11U1	1820-2112	0	2	IC 3 IN MUX ECL	28480	1820-2112
A11U2	1820-2112	0	2	IC 3 IN MUX ECL	28480	1820-2112
A11U3	1820-0982	8	1	IC DIFF AMPL HS 16 DIP C	28480	1820-0982
A11U4	1820-0372	2	2	IC 5 GHZ LIMITER AMP	28480	1820-0372
A11U5	1820-0372	2	2	IC 5 GHZ LIMITER AMP	28480	1820-0372
				ALL MISCELLANEOUS PARTS		
				PIN-GRY .060-IN-DIA .25-IN-LG STL	28480	1480-0116
				PIN-P.C. BOARD EXTRACTOR	28480	5000-9043
				EXTRACTOR CARD	28480	5040-1484
				EXTRACTOR, PC BOARD, YELLOW	28480	5040-9848

See introduction to this section for ordering information.
*Indicates factory selected value.

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A12	05355-60012	A	1	HP-IB INPUT ASSEMBLY (SERIES 1840)	28480	05355-60012
A12CR1	1401-0535	9	1	DECIDE-RECHOTTRY	28480	1401-0535
A12J1	1251-1020	2	1	CONNECTOR-PC EDGE 12-CUNT/PCB 2-PCB	28480	1251-1020
A12P1	1251-3283	1	1	CONNECTOR 24-PIN F HIGHCH1880N	28480	1251-3283
A12R1	1810-0130	3	2	NETWORK-RES 10-BIP MULTIS-VALUE	28480	1810-0130
A12R2	1810-0130	3	3	NETWORK-RES 10-BIP MULTIS-VALUE	28480	1810-0130
A12R3	1810-0280	8	1	NETWORK-RES 10-BIP10,0K OHM K 4	01121	2104103
A12S1	3101-1000	1	1	SWITCH-EL 5-1A DIP-6SLIDE-ABBY 1A 50VDC	28480	3101-1000
A12U1	1820-1199	1	2	IC 14V TTL LS HEX 1-INP	01295	8474L8004
A12U2	1820-1199	1	1	IC 14V TTL LS HEX 1-INP	01295	8474L8004
A12U3	1820-1010	8	1	IC COMPTN TTL LS MAGTD 8-BIT	01295	8474L8004
				AIR MISCELLANEOUS PARTS		
	1200-0487	4	1	ROCKET-IC 16-CUNT DIP DIP-8LCH	28480	1200-0487
	1330-1098	8	2	CLEVIS 0,070-IN x 8LY; 0,45-IN PIN CTR	00000	CODEN BY DESCRIPTION

See introduction to this section for ordering information.
*Indicates factory selected value.

Model 5355A
Replaceable Parts

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A13	06365-60013	6	1	MOTHERBOARD (SERIES 1840)	28480	06365-60013
A13C1	0180-2617	1	2	CAPACITOR-PFD 4,50V-102 35VDC YA	28088	0180-2617
A13C2	0180-2617	1	2	CAPACITOR-PFD 10V-202 35VDC YA	28480	0180-2617
A13C3	0180-2617	1	1	CAPACITOR-PFD 4,50V-102 35VDC YA	28088	0180-2617
A13C4	0180-2617	1	1	CAPACITOR-PFD 10V-202 35VDC YA	28480	0180-2617
A13J1	1200-0548	8	2	BOCKET-IC 16-CHYT DIP 01P-BLDR	28480	1200-0548
A13J2	1200-0548	8	2	BOCKET-IC 16-CHYT DIP 01P-BLDR	28480	1200-0548
A13P1	1281-0099	1	1	CONNECTOR 30-PIN M MICRO RIBBON	28480	1281-0099
A13U1	1826-0215	2	1	IC V REGTR YO-220	04713	1826-0215
A13U2	1826-0215	0	1	IC V REGTR YO-220	04713	1826-0215
A13X2	1281-2035	4	1	CONNECTOR-PC EDGE 15-CHYT/RON 2-RODS	28480	1281-2035
A13X3	1281-1305	4	3	CONNECTOR-PC EDGE 25-CHYT/RON 2-RODS	28480	1281-1305
A13X4	1281-1305	4	4	CONNECTOR-PC EDGE 25-CHYT/RON 2-RODS	28480	1281-1305
A13X5	1281-1305	4	4	CONNECTOR-PC EDGE 25-CHYT/RON 2-RODS	28480	1281-1305
A13X6	1281-1305	3	2	CONNECTOR-PC EDGE 15-CHYT/RON 2-RODS	28480	1281-1305
A13X7	1281-2915	4	4	CONNECTOR-PC EDGE 25-CHYT/RON 2-RODS	28480	1281-2915
A13X8	1281-2915	4	4	CONNECTOR-PC EDGE 25-CHYT/RON 2-RODS	28480	1281-2915
A13X9	1281-2915	4	4	CONNECTOR-PC EDGE 25-CHYT/RON 2-RODS	28480	1281-2915
A13X10	1281-2915	4	4	CONNECTOR-PC EDGE 25-CHYT/RON 2-RODS	28480	1281-2915
A13X11	1281-1305	3	3	CONNECTOR-PC EDGE 15-CHYT/RON 2-RODS	28480	1281-1305
				A13 MISCELLANEOUS PARTS		
	1281-1115	4	4	PCLARIZING KEY-PC EDGE CONN	28480	1281-1115

See introduction to this section for ordering information.
*Indicates factory selected value.

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A14	06355-60014	6	1	VOLTAGE CONTROL OSCILLATOR (VCO) ASSEMBLY (SERIES 1840)	28480	06355-60014
A14C1	0160-3879	7	5	CAPACITOR-PHD .01UF +-20% 100VDC CER	28480	0160-3879
A14C2	0160-3879	7		CAPACITOR-PHD .01UF +-20% 100VDC CER	28480	0160-3879
A14C3	0160-3879	7		CAPACITOR-PHD .01UF +-20% 100VDC CER	28480	0160-3879
A14C4	0160-3879	7		CAPACITOR-PHD .01UF +-20% 100VDC CER	28480	0160-3879
A14C5	0160-3879	7		CAPACITOR-PHD .01UF +-20% 100VDC CER	28480	0160-3879
A14R1	0737-0400	9	1	RESISTOR 90.4 1% .125W P TC=0+-100	28546	C4=1/8-10-TC=0+-100
A14R2	0696-7265	C	1	RESISTOR 51.1 1% .05W P TC=0+-100	28546	C3=1/P-100-51.1+-100
A14R3	0696-7265	7	1	RESISTOR 466 1% .05W P TC=0+-100	28546	C3=1/8-10-466+-100
A14U1	9088-7023	9	1	VCO	28480	9088-7023
A14U2	9088-7026	9	1	AMPLIFIER 1	28480	9088-7026
A14U3	9088-7017	9	1	1.5 OHM AMPLIFIER	28480	9088-7017
				A14 MISCELLANEOUS PARTS		
	1291-1556	7	24	CONNECTOR-ECG CONT 8MT .014-IN-68C-8Z	28480	1291-1556

See introduction to this section for ordering information.
*Indicates factory selected value.

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
CHASSIS PARTS						
C1	0180-4082	6	2	CAPACITOR-POTHRU 1000PF 20% 200V CEN	28480	0180-4082
C2	0180-4082	6		CAPACITOR-POTHRU 1000PF 20% 200V CEN	28480	0180-4082
CP1	1250-1113	0	1	ADAPTER-COAX 57R F-8MC F-8MC (AP/AS)	28480	1250-1113
DL1	05355-40004	4	1	DELAY LINE	28480	05355-40004
F1	2110-0301	1	1	FUSE .125A 125V .281X.093	28480	2110-0301
J1 Part 2 See Figure 6-1	05303-20104	1	1	HOLDER, FUSE	28480	05303-20104
J1	05303-20104	2	1	INSULATOR	28480	05303-20104
J1	05303-40205	7	1	CONNECTOR ASSEMBLY, 8NC	28480	05303-40205
J1	05303-40205	4	1	CONNECTOR ASSEMBLY, 8NC	28480	05303-40205
J2	5020-3357	4	1	BOOBYREX PLATE	28480	5020-3357
J2	5020-3358	5	1	NUT/HEX	28480	5020-3358
J2	5020-3359	6	1	NUT/HEX/FLD	28480	5020-3359
J2	05355-40108	9	1	CABLE ASSEMBLY, RF HEAD	28480	05355-40108
J3	1250-0829	3	3	CONNECTOR-RF 8MC M 80L-HOLE-FR 50-OM	28480	1250-0829
J4	1250-0829	3	3	CONNECTOR-RF 8MC M 80L-HOLE-FR 50-OM	28480	1250-0829
J4	1250-0829	3	3	CONNECTOR-RF 8MC M 80L-HOLE-FR 50-OM	28480	1250-0829
J4	05355-40101	2	1	CONNECTOR ASSEMBLY, REAR PANEL INCLUDES CABLES #8, #9, & #10	28480	05355-40101
MP1 Mechanical Parts	7120-4172	4	2	LABEL, INPON "5355A"	28480	7120-4172
MP2 See Figure 6-2	05355-00001	5	1	PANEL, FRONT	28480	05355-00001
MP3	05355-00002	4	1	SWITCH, PC BOARD	28480	05355-00002
MP4	05355-00003	7	1	WIRE PANEL, RIGHT	28480	05355-00003
MP5	05355-00004	8	1	WIRE PANEL, LEFT	28480	05355-00004
MP6	05355-00005	9	1	PANEL, REAR	28480	05355-00005
MP7	05355-00006	0	1	COVER, TOP	28480	05355-00006
MP8	05355-00007	1	1	COVER, CARRYING	28480	05355-00007
MP9	05355-00010	4	1	COVER, VCO	28480	05355-00010
MP10	05355-00011	7	1	WELDING	28480	05355-00011
MP11	05355-20201	9	1	MOUNTING, MAIN	28480	05355-20201
MP12	05355-20205	3	1	PANEL, FRONT, SUB	28480	05355-20205
MP13	06021-20051	6	1	HANDLE, CRANK LATCH	28480	06021-20051
R1	05355-40105	4	1	CABLE ASSEMBLY, PRE IN	28480	05355-40105
R4	05355-40104	5	1	CABLE ASSEMBLY, VCO TUNE	28480	05355-40104
R5	05355-40109	0	1	CABLE ASSEMBLY, +5.2V	28480	05355-40109
R6	05355-40110	3	1	CABLE ASSEMBLY, +15V	28480	05355-40110
R7	05355-40116	7	1	CABLE ASSEMBLY, VCO OUTPUT	28480	05355-40116
R15	05355-40102	3	1	CABLE ASSEMBLY, GATE OUTPUT	28480	05355-40102
R16	05355-40103	4	1	CABLE ASSEMBLY, PULSE OUTPUT	28480	05355-40103
R17	05355-40107	8	1	CABLE ASSEMBLY, IF OUTPUT	28480	05355-40107
R18	05355-40111	4	1	CABLE ASSEMBLY, PRE OUT	28480	05355-40111
R19	0120-1855	6	1	CABLE ASSEMBLY, 1.4 ANG (A1)	28480	0120-1855
MISCELLANEOUS PARTS						
	0340-0284	6	1	INSULATOR-808A THERMOCOCT	28480	0340-0284
	0361-0508	4	12	RIVET-BLIND	28480	0361-0508
	0578-0034	9	1	SCREEN-MACH 4-NO .25-IN-HLG 40-MU-BLT	00000	ORDER BY DESCRIPTION
	0590-0038	5	1	NUT-HEX-DBL-CHAN 1/2-32-THD .074-IN-TMX	00000	ORDER BY DESCRIPTION
	1200-0547	7	2	LOCK-DUAL INLINE PMS IC FOR 1P PIN	28480	1200-0547
	1400-0034	5	1	CLAMP-CABLE .078-DIA .375-NO STL	28480	1400-0034
	1400-0082	9	2	CLAMP-CABLE .125-DIA .375-NO STL	28480	1400-0082
	1401-0110	6	1	CAP-PROT	28480	1401-0110
	1400-1186	2	1	WIREFORM MUR BLK OXD	28480	1400-1186
	2190-0044	5	1	WASHER-LK INTL T 1/2 IN .305-IN-ID	28480	2190-0044
	2190-0124	4	3	WASHER-LK INTL T NO. 10 .142-IN-ID	28480	2190-0124
	2190-0124	9	1	WASHER-LK INTL T 1 IN 1.005-IN-ID	28480	2190-0124
	2200-0147	4	2	SCREEN-MACH 4-NO .5-IN-HLG 40-MU-POZ	00000	ORDER BY DESCRIPTION
	2360-0182	5	4	SCREEN-MACH 4-NO .512-IN-HLG 82 DEG	00000	ORDER BY DESCRIPTION
	3090-0005	5	1	WASHER-BLDR NO. 6 .142-IN-ID .375-IN-OD	28480	3090-0005
	3090-0159	0	2	WASHER-PL NM NO. 6 .142-IN-ID .312-IN-OD	28480	3090-0159
	8120-2682	2	1	CABLE, REAR PANEL	28480	8120-2682
	05355-00012	6	1	PAD, HEAT SHNK	28480	05355-00012
	05355-00013	4	2	PAD, HEAT SHNK .05	28480	05355-00013
	05355-20207	5	4	SPACER, BOARD	28480	05355-20207
	06021-20052	7	1	SCREEN, LATCH	28480	06021-20052
	10940-40001	5	1	SPACER, CONNECTOR ALIGNMENT	28480	10940-40001

See introduction to this section for ordering information.
*Indicates factory selected value.

Model 5355A
Replaceable Parts

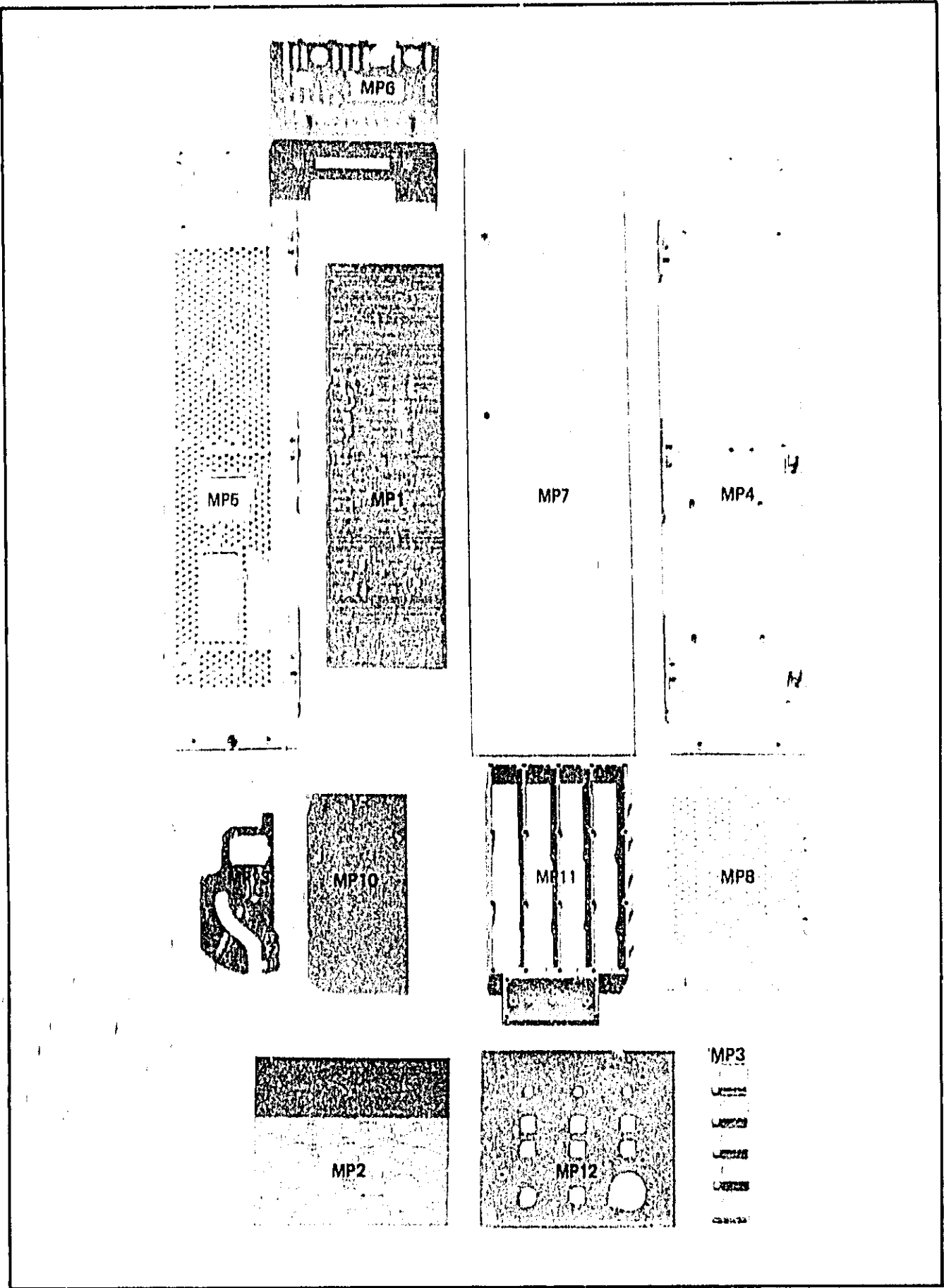


Figure 6-2. 5355A Cabinet Parts

Model 535A
Replaceable Parts

Table 6-3. Model 5356A 18 GHz Frequency Converter Head
Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	05356-60001	2	1	AMPLIFIER (SERIES 1962)	28480	05356-60001
A1C1	0160-3879	7	2	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C2	0160-3879	7		CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A1J1	1250-1642	0		CONNECTOR-RF SMA FEM PC 50-OHM	28480	1250-1642
A1U1	5088-7027	4	1	POWER AMPLIFIER, 1 GHz	20480	5088-7027
A2	05356-60002	3	1	IF AMPLIFIER (SERIES 1840)	28480	05356-60002
A2C1	0160-3833	1	4	CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	160C3833(0) N/SPECIAL EM
A2C2	0160-3833	1		CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	160C3833(0) N/SPECIAL EM
A2C3	0160-3833	1		CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	160C3833(0) N/SPECIAL EM
A2C4	0160-3833	1		CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	160C3833(0) N/SPECIAL EM
A2C5	0160-3879	4	1	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A2J1	1200-0647	8	1	SOCKET-PYR 3-CONT TO-18 DIP-8LDR	28480	1200-0647
A2R1	0757-0401	0	1	RESISTOR 100 1% .125W P TC00+-100	28480	CM-1/8-70-101-F
A2R2	0757-0409	0	1	RESISTOR 20K 1% .125W P TC00+-100	28480	CM-1/8-70-2002-F
A2U1	5088-7017	4	1	AMPLIFIER- 1.3 GHz	28480	5088-7017
				A2 MISCELLANEOUS PARTS		
	05356-20203	2	1	ADAPTER-CONNECTOR	28480	05356-20203
	05356-20204	3	1	SHELL-CONNECTOR	28480	05356-20204
				CHARIE PARTS		
J1	1250-1636	2	1	ADAPTER-COAX STR M-M SMA	28480	1250-1636
U1	5088-7031	2	1	SAMPLER-26 GHz	28480	5088-7031
U2	5088-7029	0	1	(BLUE STRIPE EXCHANGE PART NO. 5088-7531) SAMPLER DRIVER	28480	5088-7029
				MISCELLANEOUS PARTS		
	1250-1347	2	1	ADAPTER-COAX R-ANG M-SMA M-SMA	28480	1250-1347
	0120-2781	2	1	CABLE ASBY-COAX 1.502-IN-LG	28480	0120-2781
	05356-20201	0	1	HOUSING-BOTTOM	28480	05356-20201
	05356-20202	1	1	HOUSING-TOP	28480	05356-20202
	05356-60101	3	1	CABLE ASSEMBLY-INTERCONNECTION	28480	05356-60101
	5088-7032	3	1	HIGH PASS FILTER- 1.2 GHz (CP1 001)	28480	5088-7032

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-4. Model 5356B 26.5 GHz Frequency Converter Head
Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	05356-60001	2	1	AMPLIFIER (SERIES 1802)	28480	05356-60001
A1C1	0160-3879	7	2	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C2	0160-3879	7	2	CAPACITOR-PXD .01UF +-20% 100VDC CER	28480	0160-3879
A1J1	1250-1692	0	1	CONNECTOR-BP SMA FEM PC 50-OMH	28480	1250-1692
A1U1	5088-7027	6	1	POWER AMPLIFIER- 1 GHZ	28480	5088-7027
A2	05356-60002	3	1	IF AMPLIFIER (SERIES 1840)	28480	05356-60002
A2C1	0160-3833	1	4	CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	18X0508103M(D) N/SPECIAL LB
A2C2	0160-3833	1	4	CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	18X0508103M(D) N/SPECIAL LB
A2C3	0160-3833	1	4	CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	18X0508103M(D) N/SPECIAL LB
A2C4	0160-3833	1	4	CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	18X0508103M(D) N/SPECIAL LB
A2C5	0160-3833	1	4	CAPACITOR-PXD .01UF +-20% 50VDC CER	28480	0160-3833
A2J1	1200-0847	8	1	SOCKET-BYTR 3-COMT TO-18 DIP-6LDR	28480	1200-0847
A2R1P	0757-0901	0	1	RESISTOR 100 1% .125W P TCM0+-100	28480	CW-1/P-TCM-101-P
A2R2	0757-0901	0	1	RESISTOR 20K 1% .125W P TCM0+-100	28480	CW-1/P-TCM-2002-P
A2U1	5088-7017	4	1	AMPLIFIER- 1.3 GHZ	28480	5088-7017
				12 MISCELLANEOUS PARTS		
	05356-20203	2	1	ADAPTER-CONNECTOR	28480	05356-20203
	05356-20204	3	1	SHELL-CONNECTOR	28480	05356-20204
				CHASSIS PARTS		
J1	1250-1377	2	1	ADAPTER-COAX RTANG M-SMA M-SMA	28480	1250-1377
	1250-1634	0	1	ADAPTER-COAX BYR M-SMA M-SMA	28480	1250-1634
	05356-20205	4	1	SUPPORT-COLLAR	28480	05356-20205
	05356-20206	5	1	COLLAR-CONNECTOR	28480	05356-20206
U1	5088-7031	2	1	SAMPLER-26 GHZ	28480	5088-7031
U2	5088-7029	2	1	(BLUE STRIPE EXCHANGE PART NO. 5088-7931)	28480	5088-7029
				MISCELLANEOUS PARTS		
	3030-0291	1	3	SCREW-SKT NO CAP #4-40 .025-14-LG SST	00000	ORDER BY DESCRIPTION
	8120-2701	2	1	CABLE ASBY-COAX 1.502-14-LG	28480	8120-2701
	05356-20201	0	1	HOUSING-BOTTOM	28480	05356-20201
	05356-20202	1	1	HOUSING-TOP	28480	05356-20202
	05356-00101	3	1	CABLE ASSEMBLY-INTERCONNECTION	28480	05356-00101
				OPTION 001		
	1250-1677	1	1	WG ADAPTER COAX TO WAVEGUIDE	28480	1250-1677
	05356-20213	4	2	SUPPORT-WAVEGUIDE	28480	05356-20213

See introduction to this section for ordering information
*Indicates factory selected value

Model 5355A
Replaceable Parts

Table 6-5. Model 5356C 40 GHz Frequency Converter Head
Replaceable Parts

Reference Designation	PP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	05355-80001	2	1	AMPLIFIER (SERIES 1800)	28480	05355-80001
A1C1	0100-3079	7	2	CAPACITOR-PAD, 01UF ±20% 100VDC CER	28480	0100-3079
A1C2	0100-3079	7	2	CAPACITOR-PAD, 01UF ±20% 100VDC CER	28480	0100-3079
A1J1	1250-1647	0	1	CONNECTOR-RF SMA FEM PC 50-OM	28480	1250-1647
A1U1	5000-7027	4	1	POWER AMPLIFIER- 1 GHz	28480	5000-7027
A2	05355-80003	4	1	IF AMPLIFIER (SERIES 1840)	28480	05355-80003
A2C1	0100-3033	1	2	CAPACITOR-PAD, 01UF ±20% 50VDC CER	28480	120508103M101 M/SPECIAL EM
A2C2	0100-3033	1	2	CAPACITOR-PAD, 01UF ±20% 50VDC CER	28480	120508103M101 M/SPECIAL EM
A2C3	0100-3033	1	2	CAPACITOR-PAD, 01UF ±20% 50VDC CER	28480	120508103M101 M/SPECIAL EM
A2C4	0100-3033	1	2	CAPACITOR-PAD, 01UF ±20% 50VDC CER	28480	120508103M101 M/SPECIAL EM
A2C5	0100-3033	1	2	CAPACITOR-PAD, 01UF ±20% 50VDC CER	28480	120508103M101 M/SPECIAL EM
A2J1	1200-0647	2	1	ROCKET-KRTP 3-CONT TC=18 DIP=BLDN	28480	1200-0647
A2R1	0757-0403	2	1	RESISTOR 121 1% 1/8W P TC=0±100	28480	C4=1/8WTC=121M-P
A2R2	0757-0404	2	1	RESISTOR 121 1% 1/8W P TC=0±100	28480	C4=1/8WTC=121M-P
A2U1	5000-7047	0	1	AMPLIFIER- 800 MHz	28480	5000-7047
				A2 MISCELLANEOUS PARTS		
				05355-20203	28480	05355-20203
				05355-20204	28480	05355-20204
				A2 MISCELLANEOUS PARTS		
J1	05355-80001	4	1	CONNECTOR ASSEMBLY M-M M-SMA	28480	05355-80001
U1	5000-7033	2	1	SAMPLER- 40 GHz	28480	5000-7033
U2	5000-7030	1	1	SAMPLER DRIVER	28480	5000-7030
				MISCELLANEOUS PARTS		
				1250-1347	28480	1250-1347
				1250-2781	28480	1250-2781
				05355-20201	28480	05355-20201
				05355-20202	28480	05355-20202
				05355-20203	28480	05355-20203
				05355-20204	28480	05355-20204
				OPTION 001 PARTS		
				05355-20210	28480	05355-20210
				05355-20217	28480	05355-20217
				5000-0159	28480	5000-0159

See introduction to this section for ordering information.
*Indicates factory selected value.

Table 6-6. Manufacturers Code List

MFR. NO.	MANUFACTURER NAME AND ADDRESS	ZIP CODE
09000	ANY SATISFACTORY SUPPLIER	
00908	KEMET ELEK DIV. UNION CARBIDE, GREENVILLE, SC	
01121	ALLEN-BRADLEY CO., MILWAUKEE, WI	53204
01281	TRW INC., SEMICONDUCTOR DIV., LAWDALE, CA	90260
01295	TEXAS INSTR. INC., SEMICOND. CMPNT. DIV., DALLAS, TX	75222
01928	RCA CORP., SOLID STATE DIV., SOMERVILLE, NJ	08876
02114	FERROXCUBE CORP., SAUGERTIES, NY	12477
03888	KDI PYROFILM CORP., WHIPPANY, NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS., PHOENIX, AZ	85062
07263	FAIRCHILD SEMICONDUCTOR DIV., MOUNTAIN VIEW, CA	94042
16299	CORNING GL. WK. ELEC. CMPNT. DIV., RALEIGH, NC	27604
16546	U.S. CAPACITOR CORP., BURBANK, CA	91504
20932	EMCON. DIV. ITW, SAN DIEGO, CA	92129
24546	CORNING GLASS WORKS (BRADFORD), BRADFORD, PA	16701
25088	SIEMENS CORP., ISELIN, NJ	08830
26654	VARADYNE INC., SANTA MONICA, CA	90404
27014	NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CA	95051
28480	HEWLETT-PACKARD CO., CORPORATE HQ., PALO ALTO, CA	94304
30983	MEPCO/ELECTRA CORP., SAN DIEGO, CA	92121
50088	MOSTEK CORP., CARROLLTON, TX	75006
51642	CENTRE ENGINEERING INC., STATE COLLEGE, PA	16801
51959	VICLAN INC., SAN DIEGO, CA	92138
52648	PLESSEY SEMICONDUCTORS, SANTA ANA, CA	92705
56289	SPRAGUE ELECTRIC CO., NORTH ADAMS, MA	01247
72136	ELECTRO MOTIVE CORP., SUB. IEC, WILLIMANTIC, CT	06226
72982	ERIE TECHNOLOGICAL PRODUCTS, INC., ERIE, PA	16512
73138	BECKMAN INSTRUMENTS INC., HELIPOINT DIV., FULLERTON, CA	92634
80483	ALADDIN INDUSTRIES, INC., NASHVILLE, TN	37210
95275	VITRAMON, INC., BRIDGEPORT, CT	06601
98291	SEAELECTRO, CORP., MAMARONECK, NY	10544

BACK DATING MANUAL CHANGES

SECTION VII MANUAL CHANGES

7-1. INTRODUCTION

7-2. This section contains information necessary to adapt this manual to apply to older instruments.

7-3. MANUAL CHANGES

7-4. This manual applies directly to Model 5355A Automatic Frequency Converters with prefix 2016A. As engineering changes are made, newer instruments may have serial prefix numbers higher than those listed on the title page of this manual. The manuals for these instruments will be supplied with "MANUAL CHANGES" sheets containing the required information. Replace affected pages or modify existing manual information as directed in the "MANUAL CHANGES" pages. Contact the nearest Hewlett-Packard Sales and Service Office if the change information is missing.

7-5. OLDER INSTRUMENTS

7-6. To adapt this manual to older instruments having a serial prefix lower than 2016A, perform the backdating that applies to your instrument's serial prefix as listed in Table 7-1 below.

Table 7-1. Manual Backdating

If Instrument Has Serial Prefix	Make The Following Changes To Manual
1952A	1
1928A	1,2
1840A	1,2,3

CHANGE 1

Page 6-6, Table 6-2, A2 Replaceable Parts:

Change A2 series number from 2016 to 1928.

Change A2R14 and A2R20 from 0757-0397 (68.1 ohms) to 0757-0400; CD=9; resistor 90.9 1% .125W F TC=0+-100, 24546; C4-1/8-TOO-90R9-F.

Change A2R34 from 0698-7218 (68.1 ohms) to 0698-7211; CD=8; resistor 90.9 1% .05W F TC=0+-100; 24546 C3-1/8-TOO-90R9-6.

Page 8-119, Figure 8-29, A2 Schematic Diagram:

Change series number (top of diagram) from 2016 to 1928.

Change A2R14, R20 and R34 from 68.1 to 90.9 ohms.

CHANGE 2

Page 6-9, Table 6-2, A3 Replaceable Parts:

Change A3Q6 part number from 1854-0019 to 1854-0345, and add manufacturer part number 2N5179.

Change A3 series number from 1952 to 1840.

Page 8-121, Figure 8-30, A3 Schematic Diagram:

Change series number (top of diagram) from 1952 to 1840.

Model 5355A
Manual Changes

CHANGE 3

Page 6-5, Table 6-2, A2 Replaceable Parts:

Change A2 series number from 1928 to 1840.

Change A2C1 and C28 from 0180-0562 (33 μ f) to 0180-0229; Capacitor-fxd 33 μ f $\pm$ 10% 10VDC 1A; 56289; 150D336X9010B2

Page 6-119, Figure 8-29, A2 Schematic Diagram:

Change series number (top of diagram) from 1928 to 1840.

Page 6-19, Table 6-2, A11 Replaceable Parts:

Change A11 series number from 1928 to 1840.

Change A11R3 and R6 from 0698-7204 (46.4 ohms) to 0698-7203; CD=8; resistor 42.2 1% .05W T TC=0 $\pm$ -100; 24546; C3-1/8-TOO-46R4-G.

Change A11U1 and U2 part number from 1820-2112 to 1820-1999; CD=4; IC 3 IN MUX EECL; 24840; 1820-1999.

Page 8-136, Figure 8-38, A11 Schematic Diagrams:

Change series number (top of diagram) from 1928 to 1840.

Change A11R3 and R6 from 46.4 to 42.2 ohms.

NOTE

The 1820-2112 multiplexers are the recommended replacement for A11U1 and U2 in all instruments. Resistor A11R3 and R6 must be changed to 46.4 ohms when the 1820-2112 IC's are used.

SERVICE INFORMATION

SECTION VIII

SERVICE

8-1. INTRODUCTION

8-2. This section contains assembly designations, identification marking descriptions, signal name descriptions, theory of operation, troubleshooting, schematic diagrams, and part locators. The part locators show the location by reference designator.

8-3. SCHEMATIC DIAGRAM SYMBOLS AND REFERENCE DESIGNATORS

8-4. Figure 8-1 shows the symbols used on the schematic diagrams. At the bottom of Figure 8-1, the system for reference designators, assemblies, and subassemblies is shown.

8-5. ASSEMBLY DESIGNATIONS

8-6. Table 8-1 lists the designations, description, and HP Part Number of assemblies used in the 5355A.

8-7. Reference Designations

8-8. Assemblies such as printed circuit boards are assigned numbers in sequence, A1, A2, etc. As shown in Figure 8-1, subassemblies within an assembly are given a subordinate A number. For example, rectifier subassembly A1 has the complete designator of A25A1. For individual components, the complete designator is determined by adding the assembly number and subassembly number, if any. For example, CR1 on the rectifier assembly is designated A25A1CR1.

Table 8-1. Assembly Identification

Assembly	Description	HP Part Number
A1	Front Panel Control	05355-60001
A2	IF Line Amplifier	05355-60002
A3	Filter Detector	05355-60003
A4	Programmable Divider (+M)	05355-60004
A5	DC Amplifier/Loop Compensator	05355-60005
A6	Prescaler	05355-60006
A7	Microprocessor	05355-60007
A8	Decoder/HP-IB	05355-60008
A9	Interface	05355-60009
A10	Pseudorandom Sequence Generator	05355-60010
A11	Signal Switch	05355-60011
A12	HP-IB Input	05355-60012
A13	Motherboard	05355-60013
A14	Voltage Controlled Oscillator	05355-60014

8-9. IDENTIFICATION MARKINGS ON PRINTED CIRCUIT BOARDS

8-10. HP printed circuit boards (see Figure 8-1) have four identification numbers; an assembly part number, a series number, a revision letter, and a production code.

8-11. SIGNAL NAMES

8-12. Table 8-2 is a list of the signal names used in the 5355A. The list is in alphabetical order and includes the mnemonics used on the schematic diagram signals. A description of the function and the source and destination is included for each signal.

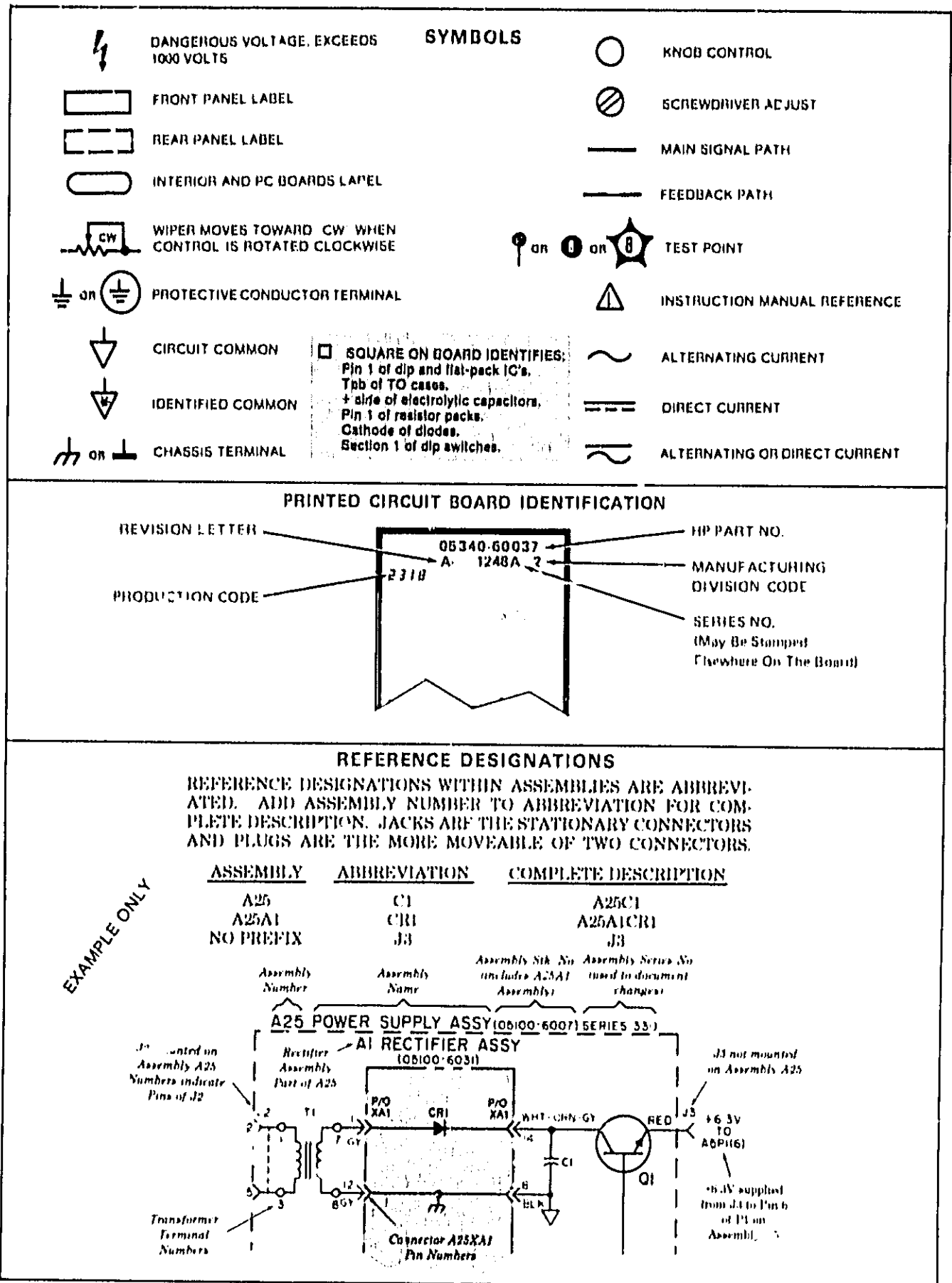


Figure 8-1. Schematic Diagram Notes

Table 8-2. Signal Names

MEMORIC	FROM	TO	FUNCTION
A/B GATE	A10(16)	A11(9, 10)	Channel A/B Gate. Signal from A10 PRSG board to A11 signal switch board that "gates off" the IF or LO/4 signal to the 5345A while the signal is being switched between the A and B channels.
A/B SWITCH	A10(18)	A5(11), A11(11, 11)	Channel A/B Switch. Signal from A10 PRSG board to A5 DC Ampl/Comp board and to A11 Signal Switch board that switches the IF or LO/4 signal between channels A and B and applies the pseudorandom sequence to the LO.
DISP STR/ INIT PROC	A9(4)	P1(15)	Display Storage/Inhibit Processor. Signal from A9 Interface circuit to 5345A. Inactive when HIGH. Dual function when low depending on status of PROC BUSY. When active during PROC BUSY low then 5355 supplies stored display to 5345A. When active during PROC BUSY high then the 5355 inhibits the 5345A from processing (PROC BUSY will be held high).
DP A DP B DP C DP D DP E DP F	A9(18) A9(4) A9(3) A9(9) A9(6) A9(5)	P1(43) P1(7) P1(8) P1(20) P1(17) P1(6)	Decimal Point Code. Bidirectional lines to transmit decimal point data between 5355A and 5345A.
DR A DR B DR C DR D	A9(10) A9(7) A9(9) A9(8)	P1(1) P1(4) P1(2) P1(3)	Denominator register code. Bidirectional lines to transmit data (mantissa) between 5355A and 5345A.
D0	A7(18, 18)	A11(18), A3(4), A4(7), A8(18) A9(20), A10(14)	Data Lines. The data bus lines form a bidirectional bus that is used for all transfers of data between A7 NIPU and other assemblies within the 5355A. See Figure 8-18.
D1	A7(19, 19)	A11(6), A3(4) A4(5), A8(19), A9(19), A10(15)	
D2	A7(20, 20)	A11(9), A3(5), A4(4), A8(20), A9(20), A10(16)	
D3	A7(21, 21)	A11(11), A8(21) A9(21), A10(17), A4(3)	
D4	A7(22, 22)	A11(10), A3(3), A4(3), A8(22), A9(22), A10(18)	
D5	A7(25, 25)	A11(12), A4(4), A8(23), A9(23) A10(19)	
D6	A7(24, 24)	A11(13), A4(5), A8(24), A9(24)	
D7	A7(23, 23)	A11(14), A4(6), A8(25), A9(25)	
GA CNT	A4(8)	A5(4)	Gain Control. Signal from A4 Programmable Divider to A5 DC Amp/Comp Operational Amplifier U4 to control U4's gain.
GATE OUT	A3(13)	REAR PANEL VIA A13E6	Gate Out signal from A3 Filter/Detector circuit to 5345A Gate Control Input (rear panel) connector. Gates the 5345A when the 5355A IF is in the proper passband in PRF mode.

Table 8-2. Signal Names (Continued)

MNEMONIC	FROM	TO	FUNCTION
HB02	A7(6)	A8(5) A13 Test Socket (10)	High Bus Phase Two. Clock signal from A7 Microprocessor clock logic to A8 Decoder/HP-IB circuits. Brought out to motherboard test socket as a service aid.
HCWH1J/ LCWPR5C	A8(16)	A2(4), A6(2)	Low for RF Head Pulse mode and Prescaler CW mode. Turns on AGC on A2 for Pulses. Forces, maximum sensitivity on A6 for pulses.
HDSENS	A6(1)	A8(7)	High Desensitize. High pulse that desensitizes the prescaler input.
HEN	A7(7)	A13 Test Socket (2)	High Enable for service aid. Brought out to motherboard test socket.
HPR/IF	A8(13)	A3(6)	High Prescaler/Intermediate Frequency. High signal from A8 Decoder/HP-IB circuit selects Prescaler input to A3 Decoder/HP-IB via relay A3K1. Low signal selects IF input.
HSQ8Y	A8(9)	A10(1)	High Sequence Busy signal from A8. High indicates that the pseudorandom sequence is busy.
HVMA	A7(7)	A8(5), A13 Test Socket (6)	High Valid Memory Address signal from A7 Microprocessor to A8 Decoder circuits. Brought out to motherboard test socket as a service aid.
IF TUNING	A5(22)	A2(15)	IF Tuning. Signal from A5 DC Amp/Comp to A2 IF Amplifier. This signal is a dc voltage applied to the tuned filter to track the change in VCO frequency.
LA0, LA1, LA2	A7(3), A7(3), A7(4)	A8(1), A8(2), A8(2)	Low Address lines from A7 Microprocessor to A8 Decoder. These three lines are decoded into 8 address lines to control MPU peripherals.
LA13 LA14	A7(15) A7(16)	A13 Test Socket (12) A13 Test Socket (11)	Low Address Bits 13 and 14. Brought out to motherboard test socket as a service aid.
LFDP0	A8(13)	A3(6)	Low Filter Detector Pulse 0. Low signal from A8 Decoder circuit that resets the A3 latches for D0, D2, and D4 data lines.
LFDR5	A18(10)	A3(5)	Low Filter Detector Read Status. Low signal from A8 Decoder circuit that enables the A3 Output Buffers for the D0, D1, D2, and D4 data lines to read the status.
LFPR5	A8(15)	A1(4)	Low Front Panel Read Status. Low signal from A8 enables the A1 Output Buffers, allowing the A7 MPU to read the front panel status.
LFPV1	A8(14)	A1(7)	Low Front Panel Write 1. Pulses low to send bit pattern to control byte 1.
LFPW2	A8(14)	A1(5)	Low Front Panel Write 2. Pulses low to send bit patterns to control byte number 2.
LINR5	A8(22)	A9(21)	Low Interface Read Status. Pulses low to read the Interface status.
LINRM	A8(15)	A9(17)	Low Interface Read M. Pulses low to read data from M RAM (A9U12).
LINWP	A8(21)	A9(22)	Low Interface Write P. Pulses low when data is sent to the P RAM (A9U11).
LIVW1	A8(20)	A9(23)	Low Interface Write 1. Pulses low to send bit patterns to the Interface control byte number 1.

Table 8-2. Signal Names (Continued)

MNEMONIC	FROM	TO	FUNCTION
LINW2	A8($\overline{19}$)	A9($\overline{24}$)	Low Interface Write 2. Pulses low to send bit patterns to the interface control byte number 2.
LIRQ	A1(3) A8(17, $\overline{17}$)	A7(17, $\overline{17}$) A7(17, $\overline{17}$) A13 Test Socket (4)	Low Interrupt Request. Active low maskable interrupt. HP-IB and front panel switches can activate the line. Brought out to motherboard test socket as a service aid.
LLO/IF	A6($\overline{8}$)	A11(2, $\overline{2}$)	Low Local Oscillator/Intermediate Frequency signal from A8 Decoder circuit to A11 Signal Switch circuit. When this signal is Low the LO/4 input is selected and when this signal is High the IF input is selected by A11 switching circuits.
LNMI	A7($\overline{16}$)	A13 Test Socket (1)	Low Non-Maskable Interrupt. Active low non-maskable interrupt to A7U1 MPU. Used as service aid only (brought out to motherboard test socket).
L RST	A7($\overline{14}$)	A8($\overline{6}$) A13 Test Socket (6)	Low Reset signal from A7 Microprocessor circuit to A8 Decoder/HP-IB to reset the Listen FF. Activated during power-up or by service aid (A13 test socket, pin 6) only
LR/W	A7($\overline{7}$)	A13 Test Socket (9)	Low Read/Write. Microprocessor read/write line. Low read; high write. Brought out to test socket on motherboard for service aid.
LSEL0 LSEL1 LSEL2	A7($\overline{4}$) A7(5) A7($\overline{5}$)	A8($\overline{3}$) A8($\overline{3}$) A8($\overline{4}$)	Low Select 0, 1, and 2 signals from A7 Microprocessor to A8 Decoder circuits to select address decoders and control the flow of data between the MPU and peripheral circuits.
LSQW1	A8($\overline{10}$)	A10(3)	Low Sequence Write 1. Pulses low to control the pseudorandom sequence logic on A10.
LVAGC	A6($\overline{1}$)	A8(6)	Low Valid Auto Gain Control. Low when valid AGC from prescaler.
LSYWL	A8($\overline{16}$)	A4(6)	Low Synthesizer Write Least-Significant Byte. Pulses low when a new synthesizer code is sent from A7 MPU. Clocks MSD data into counters on A4 Programmable Divider.
LSYWM	A8($\overline{18}$)	A4(7)	Low Synthesizer Write Most-Significant Byte. Pulses low when a new synthesizer code is sent from A7 MPU. Clocks LSD data into counters on A4 Programmable Divider.
MLAS TIME	P1(42)	A9(17)	Measurement Time. Signal from 5345A to 5355A indicates that the mainframe is in the measurement phase. Signal sent via rear panel connector to A9 Interface circuits.
PI ARM	A9(16)	P1(41)	Plug-In Arm. Low signal from A9 Interface circuit that arms the 5345A (overridden by P1INH ARM).
PI CLK	A9(5)	P1(16)	Plug-In Clock. The 5345A generates a burst of 16 high going pulses whenever data is transmitted between the 5355A and the 5345A.
PI CLK EN	P1(21)	A9(10)	Plug-In Clock Enable. Signal from 5345A to A9 Interface circuits. A low "window" is generated by the 5345A whenever a string of data is transmitted between the 5345A and the 5355A.
PI DATA	A9(3)	P1(14)	Plug-In Data. Activate low whenever the 5355A has new data for display (at least once every measurement cycle).

Table 8-2. Signal Names (Continued)

MNEMONIC	FROM	TO	FUNCTION
PI FUNC A PI FUNC B PI FUNC C	A9(14) A9(1) A9(2)	A11(1, 1), P1(36) P1(11) P1(12)	Plug-In Function. Signals from A9 Interface to operate counter according to selected function of plug-in.
PI GATE	A9(19)	W5(13)	Plug-In Gate. Low in PULSE mode to force equivalent of EXT GATE switch position on 5345A rear panel.
PIGT B PIGT C	A9(13) A9(10)	P1(28) P1(30)	Plug-In Gate Time B and C. Signals from A9 Interface that select counter's gate time when enabled by PIGT SEL. Code lines B and C are the complement of each other while PIGT A [P1(9)] and PIGT D [P1(29)] are grounded on the 5355A A1s Motherboard.
PIGT SEL	A9(1)	P1(10)	Plug-In Gate Time Select. Enables counter to accept gate time codes from plug-in.
PIINH ARM	A9(15)	P1(40)	Plug In Inhibit Arm. Low signal from A9 Interface circuit inhibits counter from arming.
PI SEL	P1(18, 39)	A9(14)	Plug-In Select. Low signal from 5345A to A9 Interface to indicate plug-in function is selected.
PI XMT	P1(5)	A9(6)	Plug-In Transmit. Control signal from 5345A to A9 Interface circuit. Low enables plug-in to transmit mantissa and decimal point data to the 5345A. High enables 5345A to transmit data to the 5355A plug-in.
PROC BUSY	P1(32)	A9(16)	Processor Busy. Low signal from 5345A to A9 Interface circuit during 5345A process cycle. High during 5345A display and HP-IB output cycles.
PRS GATE	A6(12)	A3(11)	Prescaler Gate. Signal from A6 Prescaler to A3 Filter/Detector that provides the Gate Out signal to the 5345A during prescaler operation.
PULSE OUT	A3(9)	REAR PANEL VIA A13E5	Pulse Out. This signal is the detected envelope supplied from A3 Filter/Detector to the rear panel connector for monitoring pulse width.
RFC1	5356	A9(24)	Head Code 1. Frequency Converter Head code line. High level signal adds 1 and low adds 0 to the number displayed on power-up.
RFC2	5356	A9(25)	Head Code 2. Frequency Converter Head code line. High level signal adds 2 and low adds 0 to number displayed on power-up.
RFC3	5356	A9(27)	Head Code 3. Frequency Converter Head code line. High level signal adds 4 to the code and low adds 0 to the number displayed on power up.
RST	P1(38)	A9(13) A7(10)	Reset. Low signal from 5345A to A9 Interface that resets the plug-in circuits and indicates the 5345A is being reset.
SEL A+B	P1(18)	A13	Active low to enable input channels A and B via the plug-in. This line is shorted to PI SEL P1(39) on the 5355A Motherboard.
SIGN —	A9(8)	P1(19)	Sign Minus. Low signal from A9 Interface to 5345A to indicate the sign of plug-in data and light the display's minus sign.

Table B-2. Signal Names (Continued)

MINEMONIC	FROM	TO	FUNCTION
SYNTH+4 (LO/4)	A4(19)	A11(15)	Synthesizer Divide-by-Four. Signal from A4 Programmable Divider to A11 Signal Switch. Measured alternately with the IF to determine harmonic number in CW and determine calibration factor in pulse mode.
VCO TUNE	A5(20)	A14J6 VIA A13E2	Voltage Controlled Oscillator (VCO) Tunes signal from A5 DC Amplifier/Compensator that provides the dc tuning voltage for the voltage controlled oscillator (VCO).
$\phi 1$	A4(16, 16)	A5(12)	Phase 1. Signal from +M circuit of A4 Programmable Divider to drive the Phase Detector in A5 DC Amp/Comp circuit. Combines with the 100 kHz Reference from +C circuit of A10 board to generate the VCO tuning voltage.
5 MHz	A10(21)	A7(1)	5 Megahertz. Clock signal generated on A10 board (derived from 10 MHz signal from the 5345A) and sent to A7 Microprocessor clock logic.
10 MHz	5345A VIA A13E4	A10(23)	10 Megahertz. Reference signal from 5345A to +C circuit on A10 board. Used to generate 5 MHz clock for A7 Microprocessor, 1 MHz for PRSG circuits and 100 kHz for the phase detector on A5 DC Amp/Comp board.
100 kHz REF	A10(25)	A5(2) A4(1) (not used)	100 Kiloherzt Reference. Signal from A10 board +C circuit to Phase Detector in A5 DC Amp/Comp. Combines with $\phi 1$ signal from A4 +M circuit to generate the VCO error voltage.

8-13. 5345A MODIFICATION, SERIAL PREFIX 1744A AND BELOW

8-14. When performing pulsed rf measurements with the 5355A, an external BNC cable is connected between the GATE OUTPUT Jack of the 5355A and the GATE CONTROL INPUT of the 5345A. The 5345A's rear panel switch is always set to the INTERNAL position. Whenever the plug-in makes a pulsed rf measurement, an electrical connection automatically causes the switch to effectively change to the EXT GATE position (if the 5345A has a serial prefix 1808A or higher).

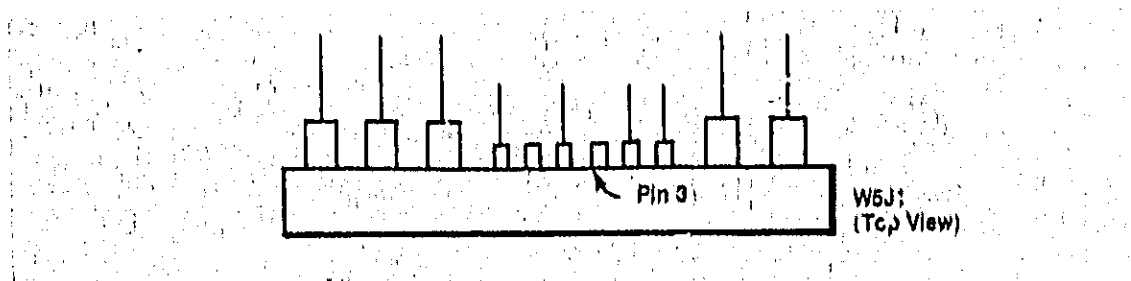
8-15. 5345A's with serial prefix 1744A and below do not have the ability to electrically change the switch position and must be modified. The change is accomplished on the 5345A by adding a wire between plug-in connector W5J1 pin 3 and the rear panel GATE CONTROL switch on the same lug as the existing WHT-BRN-GRA wire. This line name becomes PI EXT GATE. Perform the following procedures to make this modification.

WARNING

REMOVE POWER CABLE FROM 5345A TO AVOID
ELECTRICAL SHOCK.

- Remove top and bottom covers.
- Remove the four screws holding the plate that covers the plug-in connectors and remove the plate.
- Remove two side panels located at the rear of each side frame.
- Remove the three screws on the right side frame and the four screws on the left side frame that attach to the sheet metal.
- Remove the six screws on the rear panel that hold the panel in place. NOTE: one of these screws holds a clip for the wiring harness.

- f. Spread the side frames and pull the rear panel free so the top of the panel can be rotated downward to expose wiring.
- g. Solder a wire between W5J1 pin 3, shown below (use heat shrink tubing) and the rear panel GATE CONTROL switch on the same lug as the existing WHT-BRN-GRA wire. This line name becomes PTEXT GATE.



8-16. OVERALL BLOCK DIAGRAM THEORY

8-17. The 5355A plug-in to the 5345A provides automatic measurement of signals in the frequency range of 0.4 to 1.6 GHz, applied to the front panel BNC input. Signals in the range of 1.5 to 18 GHz are measured by use of the 5356A Frequency Converter Head and signals in the range of 1.5 to 26.5 GHz are measured by use of the 5356B Frequency Converter Head. Signals in the range of 1.5 to 40 GHz are measured by use of the 5356C Frequency Converter Head. The 5356A/B/C heads have a 5½-foot cable that connects to the multipin RF HEAD INPUT connector of the 5355A.

8-18. A detailed block diagram of the 5355/5356 is shown in Figure 8-27. Input signals in the 0.4 to 1.6 GHz range are sent to the A6 Prescaler which supplies a 50 to 200 MHz (+8) output to the A3 Filter Detector. Input signals in the 1.5 to 40 GHz range are sent through the 5356A/B/C Frequency Converter Head which supplies the down-converted IF to the A2 IF Amplifier. The 5355A automatically acquires the input CW or pulsed rf signal and under control of its microprocessors algorithm, routes the down-converted IF to the 5345A mainframe to be counted and displayed.

8-19. The signal applied to the 5356A/B/C is sampled by a microwave sampler at a rate determined by a programmable frequency synthesizer circuit in the 5355A. This circuit is comprised of A4 Programmable Divider, A5 DC Amplifier/Compensator, and A14 Voltage Controlled Oscillator.

8-20. The frequency synthesizer, which is phase-locked to the 10 MHz quartz reference from the 5345A, drives the Sampler Driver (step recovery diode) in the 5356A/B/C to produce useable harmonics up to over 40 GHz. The harmonics of the synthesizer are mixed with the unknown input frequency in the Sampler, whose output is sent through a preamplifier to A2 IF Amplifier.

8-21. The synthesizer, under control of the microprocessor, is swept over the range of 885 to 1056 MHz until the A3 Filter Detector signals the microprocessor that an IF exists in the range of 78 to 375 MHz. After determining which harmonic of the synthesizer mixed with the unknown to produce the IF, the IF signal is measured in Channel A of the 5345A counter to the desired resolution. The microprocessor then computes the unknown from the following relation:

$$f_x = N \cdot f_s \pm f_{IF}, \text{ where}$$

N = harmonic of f_s that is mixing with f_x to produce f_{IF}
 f_s = synthesizer frequency
 f_{IF} = down-converted IF

8-22. To determine harmonic number N , the synthesizer is incremented by 4 MHz and the change in IF is measured by the 5345A. $N = \Delta f_{IF} / 4 \text{ MHz}$. If the IF increases, then f_{IF} is subtracted from $N \cdot f_0$. If the IF decreases, f_{IF} is added. For CW measurements, the 4 MHz change in synthesizer frequency is controlled by a pseudorandom sequence for high FM tolerance. The pseudorandom changing of synthesizer frequency is done in synchronism with the switching of the down-converted IF between Channel A and Channel B of the 5345A. The results accumulated in the two channels of the counter are used by the microprocessor to determine N and the sign of the IF.

8-23. The GATE OUT signal from A3 Filter Detector is sent to the rear panel of the 5355A. This signal is connected (by cable supplied) to the GATE CONTROL INPUT of the 5345A for pulsed rf measurements, so the 5345A is gated-off only while a burst is present in the IF. To position the GATE OUT signal in the middle of the burst, the IF is sent through a delay line following A3 Filter Detector. This allows the counter to ignore the first and last 15 ns portions of the burst which may contain transients that could invalidate a measurement.

8-24. The PULSE OUT signal from A3 Filter Detector is sent to the rear panel of the 5355A. This output is an envelope of the IF and may be used to trigger a delaying pulse generator for frequency profile measurements, VCO transient response measurements and other dynamic frequency measurements where the GATE OUT signal of the 5355A is not used.

8-25. The IF OUT signal is the down-converted 70 to 375 MHz signal supplied by the A11 Signal switch circuit to the rear panel of the 5355A for monitoring purposes.

8-26. Control circuits of the 5355A are A1 Front Panel, A7 Microprocessor, A8 Decoder/HP-IB, and A12 HP-IB Interface. Pushbutton keys on the front panel control local operation via the microprocessor. The A8 and A12 HP-IB circuits provide remote control of operation via the microprocessor.

8-27. The theory of operation of each assembly is described in detail in the following paragraphs.

8-28. DETAILED CIRCUIT THEORY

8-29. A1 Front Panel Control Assembly

8-30. The front panel control assembly contains seven pushbutton switch-indicators, three status indicators (REMOTE, LISTENING, and SIGNAL) and three IC's (U1, U2, and U3). As shown in Figure 8-28, the A1 circuits are interfaced to A7 microprocessor via the data bus and A8 Decoder.

8-31. Whenever one of the front panel switches is pressed, an interrupt is sent to the A7 Microprocessor via the LIRQ (Low Interrupt Request) line. In addition, one of the inputs to the 3-state driver U1 becomes active. After receiving LIRQ, the microprocessor sends LFPRS (Low Front Panel Read Status) to U1 to determine which switch was pressed, via the data bus.

8-32. The three lines that control the IC's, (LFPW1, LFPW2, and LFPRS) contain a unique address from the microprocessor. Table 8-3 shows the state of the data lines that indicate which switch was pressed (one or more). The address for each control signal is shown in the table.

8-33. When the microprocessor writes to A1, the addresses are LFPW1 and LFPW2 (Low Front Panel Write 1 or 2). Table 8-3 shows the state of the data lines that causes the various LEDs to illuminate. The HRMT (High Remote) and HLLO (High Local Lockout) shown in Table 8-3 are also shown in Figure 8-28 (U2 pins 12 and 15, respectively). When HRMT goes high the switches are deactivated due to the low LIRQ being held high. (The LOCAL switch is not connected to this line so it is still effective.) When HLLO (U2, pin 15) goes high the LOCAL switch S2 becomes disabled

Table 8-3. Front Panel Decoded Signals

Signal	Hexa- decimal Code	D7	D6	D5	D4	D3	D2	D1	D0
LFPRS	0000		H *Input Select Switch	H Pulse Switch	H Manual Switch	H CW Switch	H Offset Switch	H Offset Freq Switch	H Manual Freq Switch
LFPW1	0006	L Offset Freq LED	L Manual Freq LED	H IRMT	H ILLO		L Remote LED		L Input Select LED
LFPW2	0008	L Pulse LED	L CW LED	L Signal LED	L Manual LED	L Offset LED	L Listening LED		

*NOTE: Input Select Switch generates LIRQ only.

8-34. A2 IF Limiter Amplifier Assembly

8-35. The IF Limiter Amplifier is comprised of four major sections: input attenuator, filter, three stage amplifier, and an AGC amplifier as shown in the block diagram, Figure 8-27. The IF input signal from the 5356 converter head enters the board into a PIN diode attenuator circuit (Figure 8-2) that keeps this signal at a constant level output to the amplifiers. The PIN diodes function as variable resistors at microwave frequencies. By controlling the dc bias, the rf resistance can be varied. In this circuit, a constant bias voltage is applied to CR13 and the AGC voltage is applied to CR12. The AGC voltage decreases as the input signal level increases. This changes the bias on CR12 and causes the signal path resistance to increase. As the current through this path decreases, the current increases through PIN diode. CR10 and CR13 to ground, to attenuate the input signal. The opposite effect occurs when the AGC voltage increases due to a decrease in input signal level, to maintain a constant level out of the attenuator circuit.

8-36. The signal from the attenuator as shown in schematic diagram, Figure 8-29, enters a 3-stage low-pass filter comprised of varactors CR6, CR7, CR8, capacitors C30, C37, C39, resistors R32, R38, R39, and variable resistors R35, R36, and R40. The variable resistors are initially set for a filter cutoff frequency of 525 MHz when the tuning voltage at pin 1 is +12V. (This tuning voltage is from the A5 DC Amp/Comp circuit and it changes in value to track the change in VCO frequency. The variable tuning voltage assures the correct cutoff frequency in the filter to correspond with the VCO.)

8-37. In CW operation the tuning voltage varies from +12 to +5V and causes the filter cutoff frequency to vary between 528 and 442.5 MHz when resistors R35, R36, and R40 are adjusted correctly. In pulse operation, the filter cutoff frequency decreases to 375 MHz. This action occurs due to the decrease in tuning voltage caused by the increased resistance of FET Q5. Transistor Q6 controls FET Q5 by the application of the HCWHD/LCWPRSC signal going low at pin 4 of the A2 board.

8-38. AGC Circuit

8-39. The IF signal from U1 is also sent to an AGC circuit that is identical to that found on the A6 board, refer to paragraph 8-86, except for transistor Q1. This board does not use AGC when operating in the CW mode. The HCWHD/LCWPRSC line is high in CW and causes Q1 to disable the AGC function. The AGC is not desirable in CW because the amplifiers were designed to operate at saturation. AGC is needed in the PULSED RF mode to eliminate any noise or signal-counting between bursts.

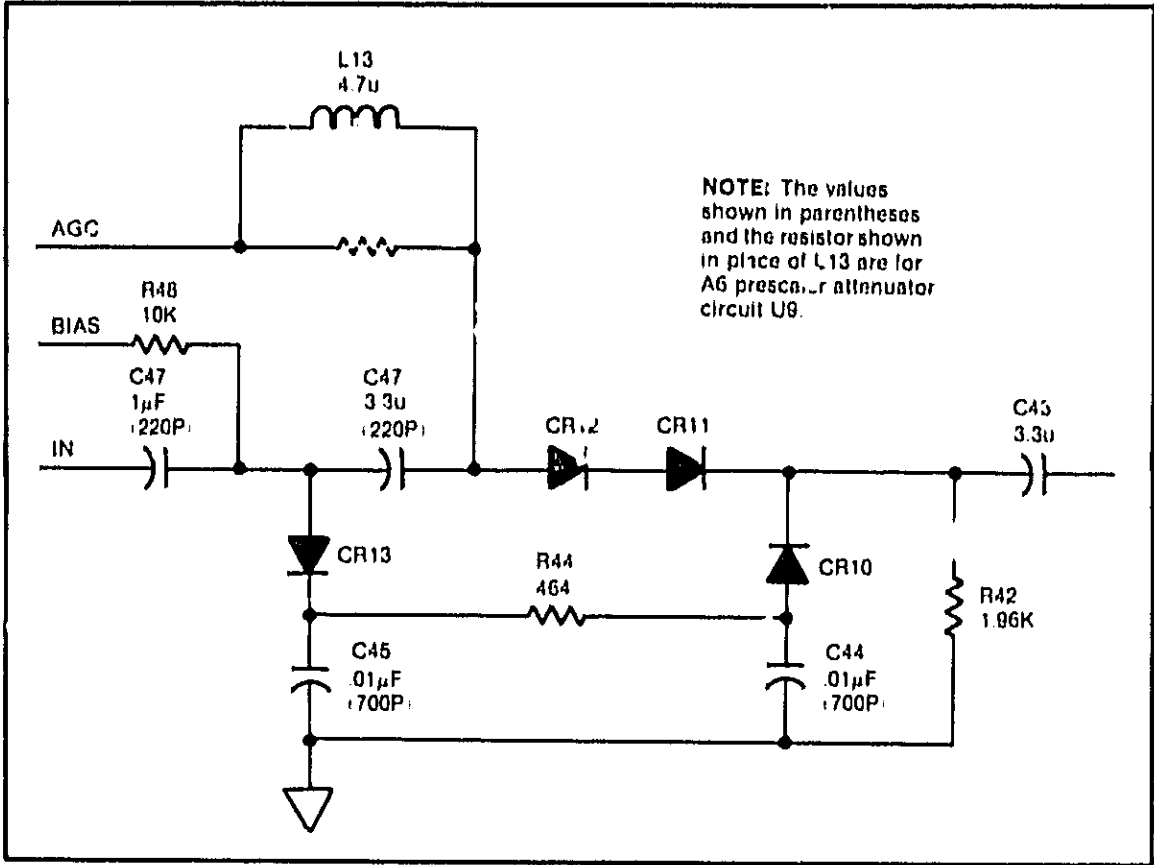
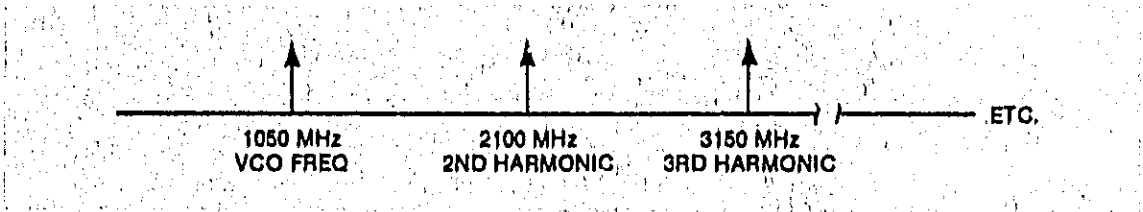


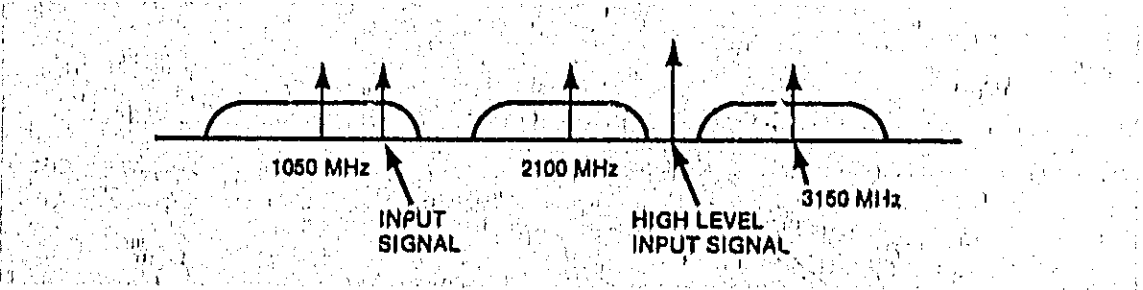
Figure B-2. PIN Attenuator Schematic Diagram

B-40. Three-Stage Filter Circuit

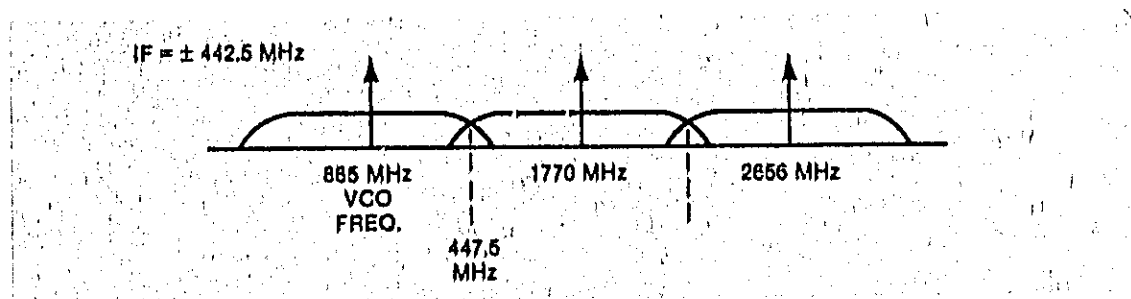
B-41. Since the input signal can mix with either the VCO's fundamental frequency or its harmonics, the IF bandwidth must reflect changes in the VCO frequency. For example, assume the VCO is set to 1050 MHz, the spectrum would appear as follows:



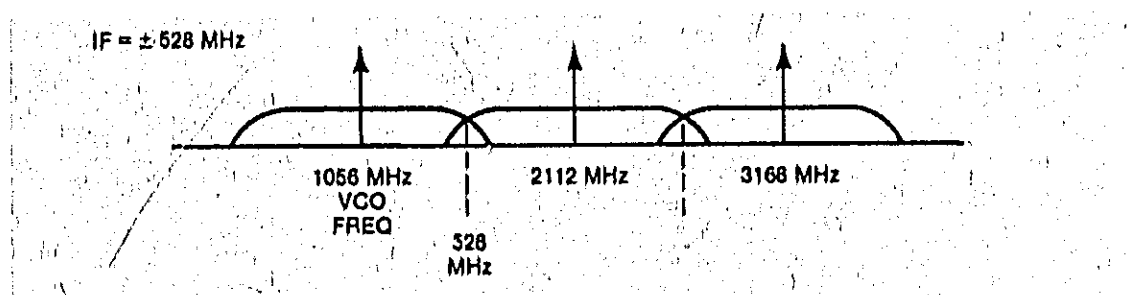
Assume an IF bandwidth of only 450 MHz when two input signals are present, as shown below:



8-42. Notice that the lower-level signal falls within the IF bandwidth and will be counted. The higher-level signal, however, falls outside the IF and will be ignored. This would defeat the plug-in's automatic amplitude discrimination feature which always attempts to measure the highest level input signal. To retain the automatic amplitude discrimination feature, the bandwidth is changed as a function of VCO frequency, so that the IF of each VCO harmonic will overlap. The range of the VCO is between 885 to 1056 MHz. At the lowest frequency the harmonics are placed 900 MHz apart, so the IF bandwidth is chosen to be half that value, as shown below:



8-43. At the highest frequency the harmonics are placed 1050 MHz apart; again, the IF bandwidth is chosen at half that value, as shown below:



8-44. It is not desirable to always use the higher IF bandwidth, since at the lowest VCO frequency the bandwidths would overlap and create confusion as to which harmonic was being mixed with the input signal. The voltage at A2(15) will vary from +5V to +12V as the VCO frequency changes. This voltage will cause the varactor in the appropriate filter to tune over a given range. Thus, the filters will track the changes in VCO frequency. After an IF has been detected, the filter is set to the cut-off frequency and the VCO is adjusted to place the IF signal within that bandwidth in preparation of the N determination routine.

8-45. A3 Filter Detector Assembly

8-46. The filter detector circuit has three major purposes:

- Selects either the IF signal from A2 IF Limiter Amplifier or the signal from A6 Prescaler by means of a relay (K1). The selected signal goes through A11 Signal Switch to the rear panel.
- Generates a gate signal coincident with the IF signal to gate the 5345A in the PULSED RF mode.
- Determines when the IF signal is within the proper bandpass and presents this information to the microprocessor via the data bus.

8-47. BLOCK DIAGRAM. As shown in Figure 8-3, the Filter Detector circuit selects either the IF output signal or the A6 Prescaler signal for the measurement channel. An IF output is provided through a delay line to the A11 Signal Switch circuit and the EXT GATE signal is sent via the rear panel and a cable to the 5345A. The filter circuits are adjusted to pass the required IF bandwidth and the logic detector circuits develop data for lines D0 through D4 to indicate the presence

and type of signal. The EXT GATE signal tells the 5345A when to count. The delay line that follows A3 must pass the IF (up to 375 MHz). Its purpose is to delay the pulse burst so the gate will be centered within the burst frequency. This avoids transients at each side of the burst that could cause incorrect measurements.

B-48, Buffer U1 provides limiting, so the input signal to the bandpass filter and voltage comparator U6 will be constant. The adjustment of this circuit is made by inserting 78 MHz and adjusting the variable resistor on voltage comparator U6. This becomes the reference for the high end. The signal is set to 375 MHz and the bandpass filter is adjusted to give the same level that was achieved at 78 MHz.

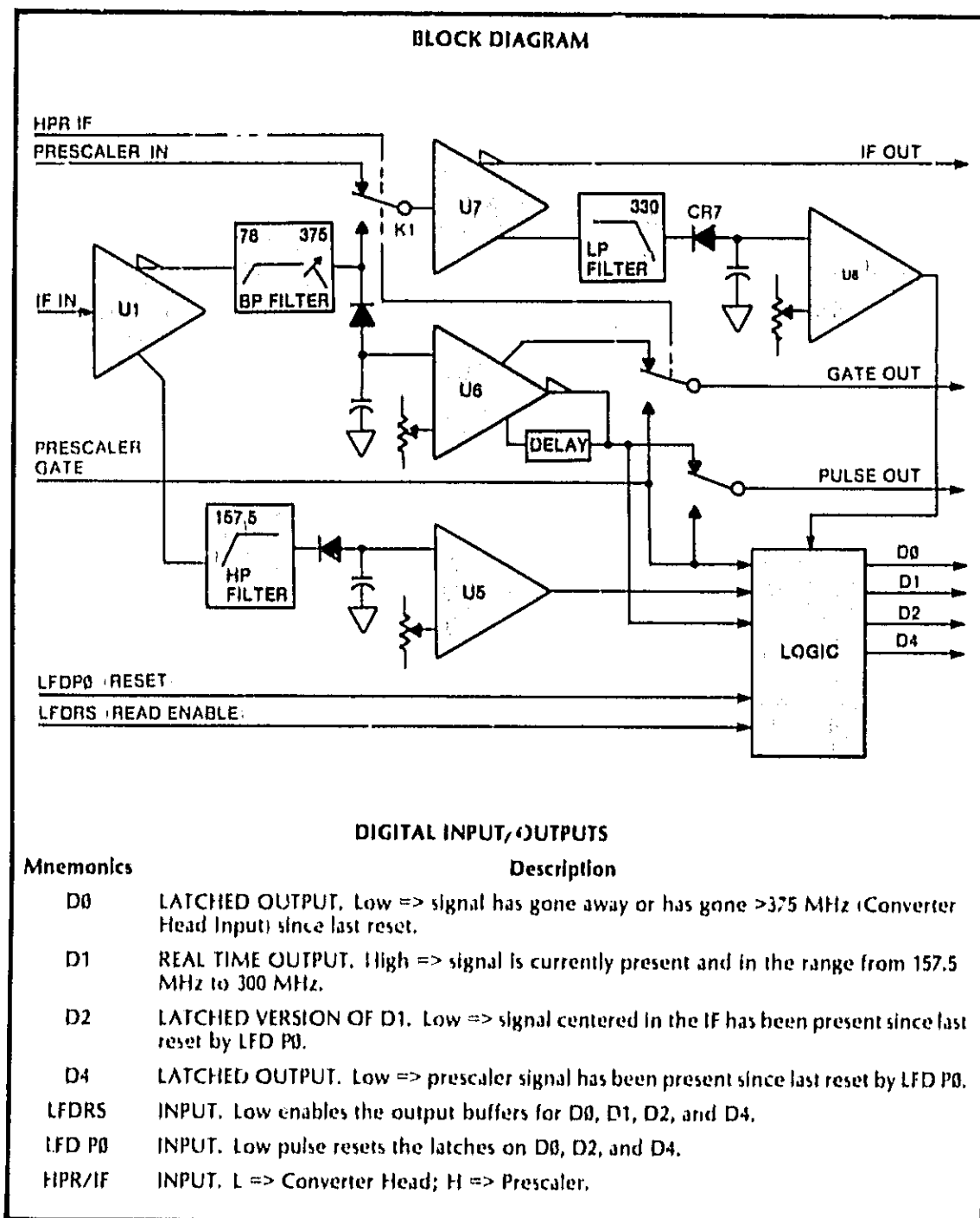
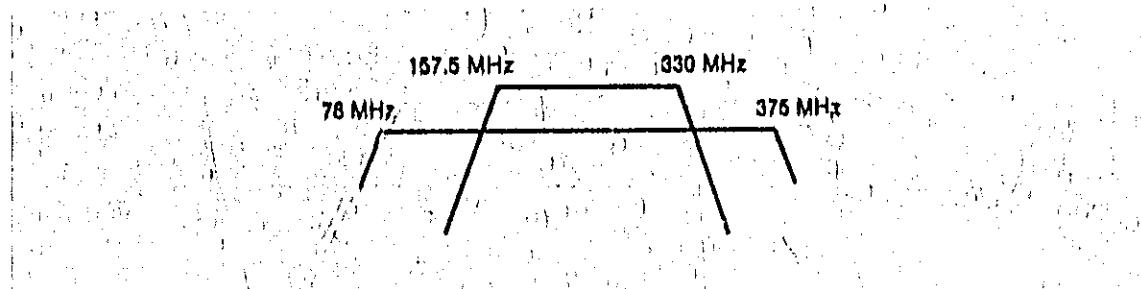


Figure 8-3. A3 Filter-Detector

8-49. The signal selected by relay K1 goes through buffer U7. The noninverted IF output of U7 goes through a 56 ns delay line, through the A11 Signal Switch assembly, and then to the IF OUT rear panel jack. The inverted output of U7 goes through a 330 MHz (± 2.5 MHz) low pass filter which sets the upper corner of the center IF band as shown below. It is detected in peak detector CR7 and fed to voltage comparator U8, which is adjusted like voltage comparator U6. The lower corner of the center bandwidth comes off the inverting side of buffer U1 and goes to voltage comparator U5.



8-50. **CIRCUIT ANALYSIS.** The IF input from J1 is buffered and, with normal input levels, amplified into limiting by U1 as shown in Figure 8-30. It is important that, with normal input levels, the output of U1 is saturated so that a constant signal level is presented to the filters and detectors. If this output level is not constant, the apparent corner frequencies of the IF passband will vary with input signal level due to the level detection scheme that is used. One output of U1, (pin 8) goes to the 5-pole highpass filter with a corner frequency of 157.5 MHz. The output of the filter is detected by diode CR2 and stored in capacitor C11. Comparator U5 determines whether the level out of the detector is above or below the reference voltage on pin 4. Thus, by varying this reference via variable resistor R10, the effective corner frequency of the filter can be changed. This detection scheme is used in two other places on this board.

8-51. The other output of U1, pin 5, goes through cascaded highpass ($f_c = 78$ MHz) and lowpass ($f_c = 375$ MHz) filters and then to a detector (CR6, C24, and U6). The output of the filter also goes to relay K1, which acts as the switch between the IF and prescaler inputs, and then to buffer amplifier U7. One output of U7 (pin 5) provides the IF output to the A11 Signal Switch assembly. The other output (pin 8) goes through a 330 MHz lowpass filter to the third detector.

8-52. The outputs of the three detector comparators (U5, U6, and U8) are TTL levels and indicate whether an IF input signal is present in the passband of the associated filter. Digital IC's U3 and U4, combine and latch these signals to present the desired information to the microprocessor. U2 is an inverting three-state driver that puts the digital outputs on the data bus when input LFDR5 is low. These digital outputs are:

- D0: A low level on this latched output indicates that the input signal has gone away or, for the high frequency input, that the IF has gone outside the guardband of 78 to 375 MHz since the latch was last reset.
- D1: This is a real-time output that applies to the high frequency channel only. A high level indicates that the IF is currently present in the center passband, 157.5 to 330 MHz.
- D2: This is a latched version of D1. A low level indicates that the IF has been present in the center passband at some time since the latch was last reset.
- D4: This is a latched output which is similar to D2 except that it applies to the prescaler input instead of the high frequency input. A low level indicates that a valid input level has been present in the prescaler channel at some time since the latch was last reset.

The three latches are all reset by a low level on the LFDP0 input.

8-53. Comparator U6, following the 70—375 MHz bandpass section, is also used to generate the gate signal for the 5345A mainframe. The fact that the comparator contains two independently enabled outputs is used to generate a gate pulse 20–30 ns shorter than the detected rf burst. This is done by delaying the inverting output with an RC network and using this delayed signal to enable the noninverting output, which becomes the gate output after transistors Q3, Q4, and Q6 translate the level to the –1V signal required by the 5345A. The inverting output of U6 is also delayed and used to enable comparator U8 in order to assure that a valid signal indication cannot be given before a gate output is present.

8-54. When the prescaler input is selected, the gate signal comes from the prescaler board and not from U6. U4A and U4B may be used to delay the prescaler gate signal so that it has the same relative timing relationship as the high frequency gate. Transistors Q5 and Q7 are used to switch between the two gate signals. They are driven by transistors Q2 and Q1, which also drive K1, the bandswitch relay.

8-55. Due to differences in the three-peak detectors, it is possible that U5 and U8 could indicate to the microprocessor via D1 (CW mode) and D2 (PULSE mode) that there is a signal present in the center bandpass before U6 can generate a gate in the pulse mode. Therefore, U6 pin 9 must go high to enable U8 via pin 13, thus ensuring the gate pulse occurs first.

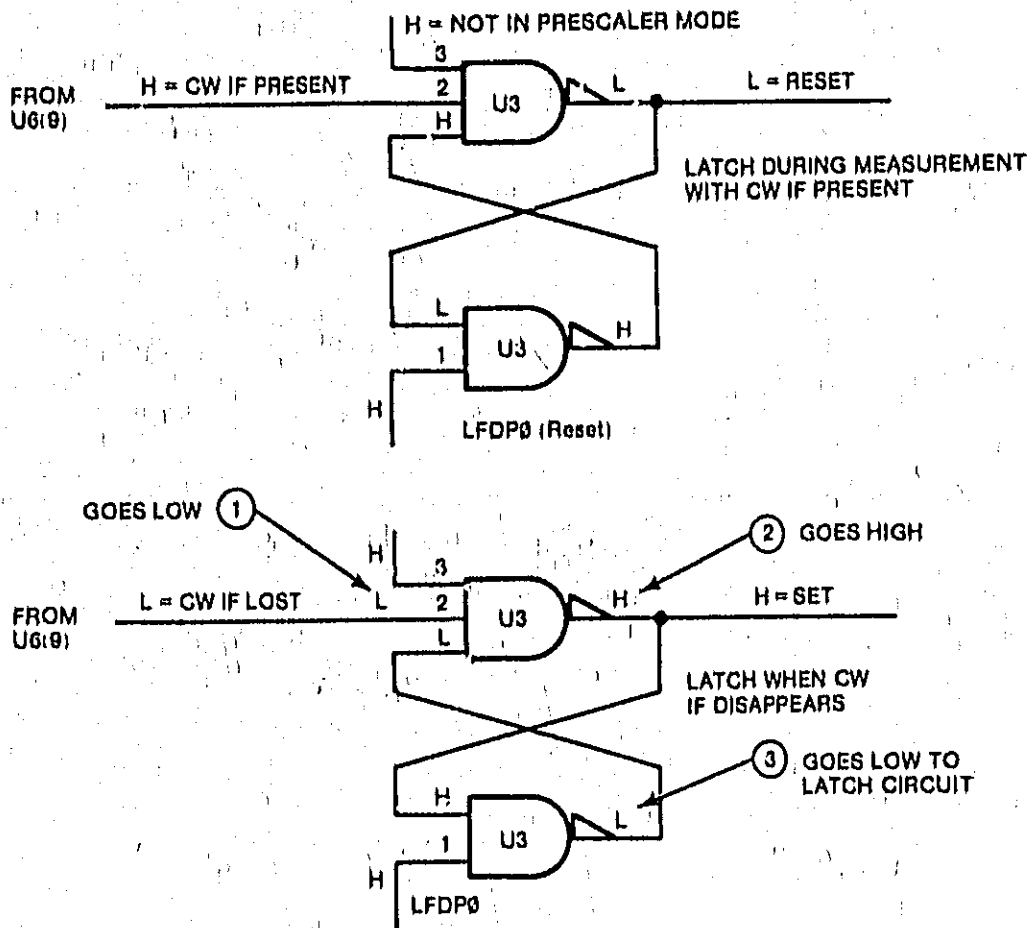
8-56. In Comparator U6 pin 8 is the enable line for pin 9. It is used to drive the output high when the prescaler is selected, so that D0 is then controlled by the prescaler gate signal instead of by U6.

8-57. The D1 line is used in the CW mode. In CW, the processor will set the VCO to a given frequency and will then pull LFDRS low and read the status (D1) to see if there is an indication of a signal present. If there is a signal present, it will step the VCO 4 MHz and check again to see if the signal is present. If the signal is present in both cases, it will then make a measurement.

8-58. The D2 line goes high with latch U3B. This also is center band information. It indicates that there was a signal in the center band since the last time LFDP0 (latch reset) was pulsed.

8-59. The D0 line is used in CW mode to determine if the IF signal was lost during the measurement. A detailed explanation is provided in the following paragraph.

8-60. The D0 line description: After it has been determined there is a signal present in the IF range, the processor will first reset A3 Filter Detector circuit (LFDP0) and enable the counter to count. When the counter comes back with a reading, the processor will check the status of A3 (LFDRS) to ensure the signal did not disappear during the measurement. If the signal had been lost during that time, U6 pin 9 would go Low to set U3A, as shown below:



8-61. The D4 line is used for the same purpose as D2, except it is used for the prescaler mode.

8-62. The state of LFDP0 depends on the mode of operation. In the acquisition mode, LFDP0 is set low everytime before the processor checks the board. The processor sets the VCO frequency, resets these circuits, then checks to see if the conditions are met. In the pulse mode, it keeps checking (without pulsing LFDP0) for up to 20 ms because there can be a minimum repetition rate of the input signal of 20 ms.

8-63. A4 Programmable Divider (+M) Assembly

8-64. As shown in the overall block diagram, Figure 8-27, the A4 Programmable Divider receives the output of the buffer amplifier of A14 VCO, divides it by 4 and provides one output to the +M circuit and another to the A11 Signal Switch circuit. The +M circuit is programmed by the MPU to determine the synthesizer frequency. The +M output is sent to the phase detector in A5 DC Amplifier/Compensator.

8-65. **CIRCUIT ANALYSIS.** The 885.2–1056 MHz signal from the A14 VCO enters A4 and is divided by four in U14 as shown in Figure 8-31. One output of U14 (pin 11) goes to the +M circuits of the board, while the other goes to the A11 Signal Switch board where it can be sent to the mainframe for counting. U12 operates as either a divide by 10 or divide by 11 circuit. The ECL output of U12 enters U10(7) where it is divided by four. The output of U10 re-enters U12 and is converted to TTL before being sent to the remainder of the divider circuits. Since U12 and U10 always work together, they comprise a divide by 40 or divide by 41 circuit. If the VCO frequency is set to 1 GHz, for example, the output of U12 will be 6.25 MHz or 6.097 MHz; a total division of 160 or 164. The divider chain formed by U12, U10, U8, U9, U5, and U7 divides the output of U14(11) by M. The output of the divider chain goes from U7 through U13 to the A5 Phase Detector where it is compared to a 100 kHz reference frequency. The phase error output of A5 causes the A14 VCO to go to that frequency which, when divided by M, produces a 100 kHz output.

8-66. Presettable decade counters U8 and U9 form the least-significant digit (LSD) that control the number of times U12/U10 will divide by 41 before switching over for the remainder of the cycle and then dividing by 40. U8 can be preset with number 0 through 9, while U9 is preset with numbers 6 through 9. If the VCO is programmed to a frequency that requires U12/U10 to only divide by 40, in order to achieve the 100 kHz signal necessary to lock (atypical), then U8 and U9 will be preset to a count of "99". This causes the carry output of U9 to be high and forces U12/U10 to count by 40 for the entire cycle. (U12 pin 9 is the 40/41 control line.) If the LSD circuit is preset to any number other than 99, the carry output will be Low and cause U12/U10 to divide by 41. This circuit continues to divide by 41 until U8 and U9 count up to 99. At this point, U9(15) goes High and causes U12/U10 to divide by 40 for the remainder of the cycle. It also disables U8 and U9 from any further counting.

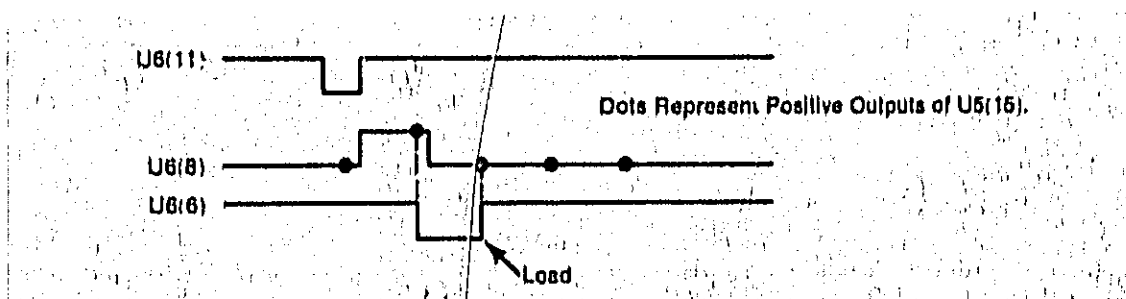
8-67. Counters U5 and U7 form the most-significant digit (MSD). They are presettable decade counters that complete the +M chain. U5 can be preset with numbers from 0–9, while U7 is preset with numbers 3 and 4. Since the output of U12 clocks all four decades, the manner in which U5 and U7 are preset ensures that the MSD will always continue to count after the LSD counters have stopped. This allows +40 counts to enter the MSD. The cycle ends when the MSD count reaches 98 (U5=8, U7=9). At this time, both inputs to U13A are High and the output is synchronized with the output of U12 in U13B, C and D to output the 100 kHz pulse to the phase detector. The reason the MSD outputs with a count of 98 instead of 99 is because it takes one clock pulse from U12 to load the preset number into the counters. Therefore the U12/U10 circuit has already divided the signal once by 40 or 41. To compensate for the one division that has already occurred, the MSD outputs one count sooner.

8-68. The processor loads each counter with a 4-digit, positive-true, BCD encoded number. This number is the 9's complement of the division factor needed to achieve the 100 kHz output when the VCO is at a specified frequency. For example, if the +M circuit was required to divide by 41 thirty times before switching to the divide-by-40 mode, U8 and U9 would be loaded with the number 69 (U8=9, U9=6). The number 69 is the 9's complement of thirty. Therefore, U8 and U9 will receive 30 pulses before U9's carry output goes High (LSD count = 99) to stop the divide-by-41 mode and start the divide-by-40 mode. This same general technique is used in the MSD counter circuit, with the aforementioned exceptions. If these circuits were down counters, they could be loaded directly (without the 9's complement) and then count down to zero.

8-69. **LOAD CIRCUITS.** The number loaded into the M counters is stored in latches U1 through U4. Only six of the processor's eight data lines are needed to load in any of the acceptable numbers. To prevent misloading of information due to the processor's inability to quickly present two sets of numbers, the storage circuits of U2 and U4 use a "handshake" routine that begins with an output of U13(8). The number for the MSD is loaded first. Data lines D0 through D4 and D7 are presented to the inputs of U4, and the processor clocks them into storage by forcing the SYNTH HIGH line to the High state. Data line D7 is not used in

the MSD. The data on lines D0 through D3 will eventually be clocked into U5, while D4 forces U7 to a code of 3 or 4. The processor then places the LSD information on the bus, and it is clocked into U2 when the SYNTH LOW and FLAG line returns High after being pulsed Low. The data on lines D0 through D3 will eventually be clocked into U8, while D4 and D7 forces U9 to codes of 6 through 9.

8-70. Flip-flops U6A and B and the carry output of U5 control the loading of these numbers into U1 and U3. Initially, the output of U6A is High and U6B output is Low. When the SYNTH LOW and FLAG line returns High to clock U2, it also clocks U6(B) to a High state. In the timing diagram below, the dots represent output pulses of U5 pin 15. The next carry output from U5 pin 15 clocks U6A pin 6 Low, which sets U6B(8) High. One more output from U5(15) clocks U6A(6) High, which transfers data from U2 and U4 into U1 and U3. New data is now presented to the inputs of the counters. This information will not be clocked into the counters until U13(3) goes Low at the end of the division cycle (this is the counter's load line) and all four counters receive a parallel clock pulse from U12(7).



8-71. Two Modulus Prescaler Technique

8-72. The amount the VCO frequency can change is a function of the plug-in's software and the converter head being used. Each model of the converter head is coded. When decoded by the plug-in, a specific set of tables is called up in software. The VCO will step through its frequencies in a nonlinear manner, i.e., smaller step sizes at the higher end (1056 MHz). The minimum change is 400 kHz. The two modulus divider technique is required to achieve the resolution needed to set the VCO at the desired frequency. To illustrate the need for the second modulus, the following example shows division by 40 only and then how division by 41 can help.

8-73. Assume a VCO frequency of 996 MHz. The output of U14 is: $996 \text{ MHz} \div 4 = 249 \text{ MHz}$. The division factor necessary to get 100 kHz is:

$$M = \frac{249 \text{ MHz}}{100 \text{ kHz}} = 2490 \text{ counts}$$

If the input to the M counter were always divided by 40, the result would be:

$$\frac{2490}{40} = 62.25$$

Since dividers can only divide by integer values, the integer value would be 62. Using this value and working backwards, $62 \times 40 = 2480$ counts, not 2490. Therefore a VCO frequency of 996 MHz could not be set correctly using only a $\div 40$ circuit.

8-74. Notice, however, that the result is only 10 counts off: $2490 - 2480 = 10$. If it were possible to add 10 more counts to the $\div M$ circuit before it gives an output pulse, the $\div M$ counter would then have the correct number of counts. This can be done by dividing by 41 ten times instead of by 40. The LSD counter would be preset to 89, which is the 9's complement of ten: $10 \times 41 = 410$ counts. The remaining counts must still be accumulated in the MSD circuit: $2490 - 410 = 2080$. These counts would be divided by 40: $\frac{2080}{40} = 52$, which is a usable integer. Counting by 41 ten times and then by 40 fifty-two times gives exactly 2490 counts $[(10 \times 41) + (40 \times 52) = 2490]$ in the $\div M$ circuit and allows the VCO to be set to 996 MHz.

8-75. A5 DC Amplifier Loop/Compensator

8-76. As shown in the overall block diagram, *Figure 8-27*, the A5 DC Amp/Loop Comp assembly receives the 100 kHz reference signal from A10 (+C) and the $\phi 1$ signal from A4 (+M) circuit. The Gain Control from the +M circuit is also sent to A5. The 100 kHz reference signal is derived from the 10 MHz signal from the 5345A. The $\phi 1$ signal is programmed by A7 MPU to determine the synthesizer frequency. The $\phi 1$ signal is compared with the 100 kHz reference signal in U3 Phase Detector on A5 and is processed by the DC Amp/Comp circuits to provide the tuning voltage (correction error) for the A14 VCO. The other output of A5 is the IF tuning voltage to the tuned filter in A2 IF Amplifier. This tuning voltage tracks the change in VCO frequency to ensure the correct cutoff frequency in the filter.

8-77. **CIRCUIT ANALYSIS.** The input to Phase Detector U3 is shown in *Figure 8-32*. Both inputs should be 100 kHz with the pin 3 reference signal in the form of wide pulses and pin 1 as narrow pulses ($\phi 1$). The signals are in phase. The output from pins 2 to 4 and 11 to 13 are driving an internal charge pump which generates a charge depending upon the phase error. The output from pins 5 and 10 provide current to operational amplifier U4. Resistor R3 is a bleeder resistor to force U3 to operate slightly offset from zero phase error, to prevent set-reset racing.

8-78. When the output of U3 phase detector is locked (zero phase error) the output voltage should be approximately 1.5 volts at capacitor C3. The + input (pin 3) of U4 is at a voltage equal to the locked output of the U3 phase detector. The 100 kHz spike output of U4 is filtered by elliptical filter L1, C2, C4, and C6 to provide the tuning voltage to the VCO.

8-79. The output of the filter is sent also to operational amplifier U7 to provide the IF tuning voltage of from 5 to 12 volts, dc. This voltage provides tuning of the input filter on A2 assembly.

8-81. The pseudorandom sequence is applied via A5 to switch the A14 VCO during the N determination routine. The pseudorandom sequence (A/B switch) is applied via U1 open-collector NAND gates and variable resistors R8 and R9. The variable resistors provide a means of combining the pseudorandom sequence signal with the VCO tuning voltage and maintaining a constant VCO sensitivity over its frequency range. This provides accuracy in N determination.

8-82. Resistors R9 and R17 provide a voltage divider at U1(11) to maintain a constant Δf over the frequency band. Variable resistor R8 maintains capacitor C6 at a constant level and is adjusted to prevent ramping up or down of the output.

8-83. The Gain Control Signal from A4 Programmable Divider controls the gain of op amp U4 via bilateral switch U2.

8-84. A6 Prescaler Assembly

8-85. As shown in the overall block diagram, *Figure 8-27*, the 0.4 to 1.6 GHz input is applied through a fuse to a PIN attenuator in the A6 Prescaler circuit. The π type attenuator maintains the input impedance over the full range (30 dB) for a constant VSWR. The signal is amplified and divided by eight for output to A3 Filter Detector. Another output of the amplifier is detected by a diode and applied to the AGC circuit. The amplifier supplies the PRS Gate signal which is applied to A3 Filter Detector circuit.

8-86. **CIRCUIT ANALYSIS.** As shown in *Figure 8-33*, the input signal enters J1 and feeds the limiter circuit of PIN diodes CR12 and CR13, which provide a dc return for the front panel fuse. The signal then enters a high-pass filter (≥ 400 MHz), capacitors CR54, CR55, C59, C60, and CR53, and inductors L12, L13, and L14. The signal then enters U9, which is a PIN diode attenuator circuit (the internal circuit of this IC is shown in *Figure 8-21*). This attenuator operates the same as the one described in paragraph 8-35. U8 is a 1.6 GHz, two-stage amplifier with 22 dB gain. Next is an impedance matching network consisting of capacitors C41, C39, C37, and resistors R47 and R31.

U7 is a 1.6 GHz binary while U6 further divides the signal by four, giving a total division of eight for the output.

8-87. AGC CIRCUIT. The AGC circuit is used in CW and PULSED RF modes. It is used in pulsed rf measurements to get a satisfactory on/off ratio of the burst. The signal is tapped off between capacitors C41 and C39 (between U7 and U8) and is sent to the detector circuit consisting of diode CR10 and capacitor C38. The resultant dc is sent to a fast differential amplifier, transistors Q4 and Q3, that can switch high current and provide gain. Emitter follower Q2 provides a low impedance to diode CR9 to charge capacitor C34. Diode CR9 is a high-impedance, reverse-bias diode that allows the rectified rf burst to charge storage capacitor C34, but prevents that capacitor from discharging. U5 is a unity gain amplifier that sends part of its output signal back to transistor Q3, through resistors R23, R48, and capacitor C32. This feedback locks the AGC and prevents any drift that is present in diode CR9 from adversely affecting the overall accuracy of the AGC circuit. (Also, resistors R35 and RT1 provide compensation for detector diode CR10.) U3 is the final stage in the AGC circuit. It provides gain and controls the gain of the PIN diode attenuator circuit U9. The greater the amplitude of the rf burst, the less the AGC voltage that is sent to U9. As the AGC voltage decreases, the signal attenuation within U9 increases. This whole technique tends to keep the rf burst to a level just above where it can be counted, while keeping the off portion of the burst compressed to a point below the input sensitivity, thereby preventing the counting of noise.

8-88. GATE OUTPUT CIRCUIT. During pulsed rf measurements, the prescaler provides the gate pulse for the counter's external gate. The rf burst is detected in CR10 and C38. The dc signal is then fed to differential amplifier Q4 and Q3. Emitter follower Q2 sends the signal to amplifier U1 which converts the signal to TTL before sending it to A3 Filter Detector and then out of the rear panel as the GATE OUT pulse. The minimum pulse width of an rf burst in the prescaler mode is 100 ns. Resistor R3 and capacitor C2 delay the output of U1 by 30 ns. This has the effect of subtracting 15 ns off the front and back portion of each PRS GATE pulse, regardless of its width.

8-89. ARMING CIRCUIT. In CW operation the circuit is designed so that with no input signal, the U4 output places a more positive voltage on the input of binary U7. This reduces the input sensitivity of binary U7 and prevents it from counting low level input signals that would cause it to miscount. If the signal's input level increases, it will reach a point where an output will appear from U6. This signal is coupled back to a detector circuit, diode CR8 and capacitor C27, which presents a dc level to one input of operational amplifier U4. This level switches U4's output to a less positive level and sets the binary to its highest sensitivity. Once the output of U6 is detected this process is instantaneous and ensures that U7 will not count an input signal until its level is high enough to allow correct counting. In the CW mode, the yellow LED (connected to U4(11)) is on when armed, (e.g., insufficient input level), and off when U6 has sent a signal through detector CR8 to switch U4 to the more sensitive position.

8-90. The HDSEN line is used in the CW mode to reset differential amplifier U4 before every measurement. If, for example, a high level input signal has set U4 (via U6 and CR8) so that the binary U7 is at its most sensitive position and then the input signal is lost, this line resets U4 to its original state, which makes U7 less sensitive.

8-91. In the PULSED RF mode, the HCWHD/LCWPRSC (High CW Head/Low CW Prescaler) line stays high and forces U4 output to its less positive state, which sets the binary of U7 to its more sensitive position. Under these conditions, the binary may very well oscillate. This is not a problem, however, because the signal is counted only while the gate pulse is present. This pulse, of course, is detected off the input burst so the proper signal is always present when gating occurs.

8-92. LEVEL DETERMINATION CIRCUIT. Because the binary U7 can miscount at low level input signals, the level determination circuit ensures that no counting will occur until sufficient input level has been reached. The proper amount of level is set by the AGC circuit. The level is set by applying an rf input level that yields an AGC voltage of +11.5V at TP2. R8 is then adjusted until the green LED, DS1 (output of U2), just comes on, i.e., the LV AGC line just goes low. This ensures that any input signal within that frequency range must reach this minimum level before it can be counted. If this level is not reached, the AGC line will be above +11.5V and the LV AGC line will be High, which instructs the microprocessor not to make a measurement.

8-93. A7 Microprocessor Assembly

8-94. The 5 MHz clock signal from A10 (+C) circuit is sent to A7U9 Clock Driver. The signal is divided by 4 to supply 1.25 MHz to U1 Microprocessor, as shown in the block diagram, Figure 8-4.

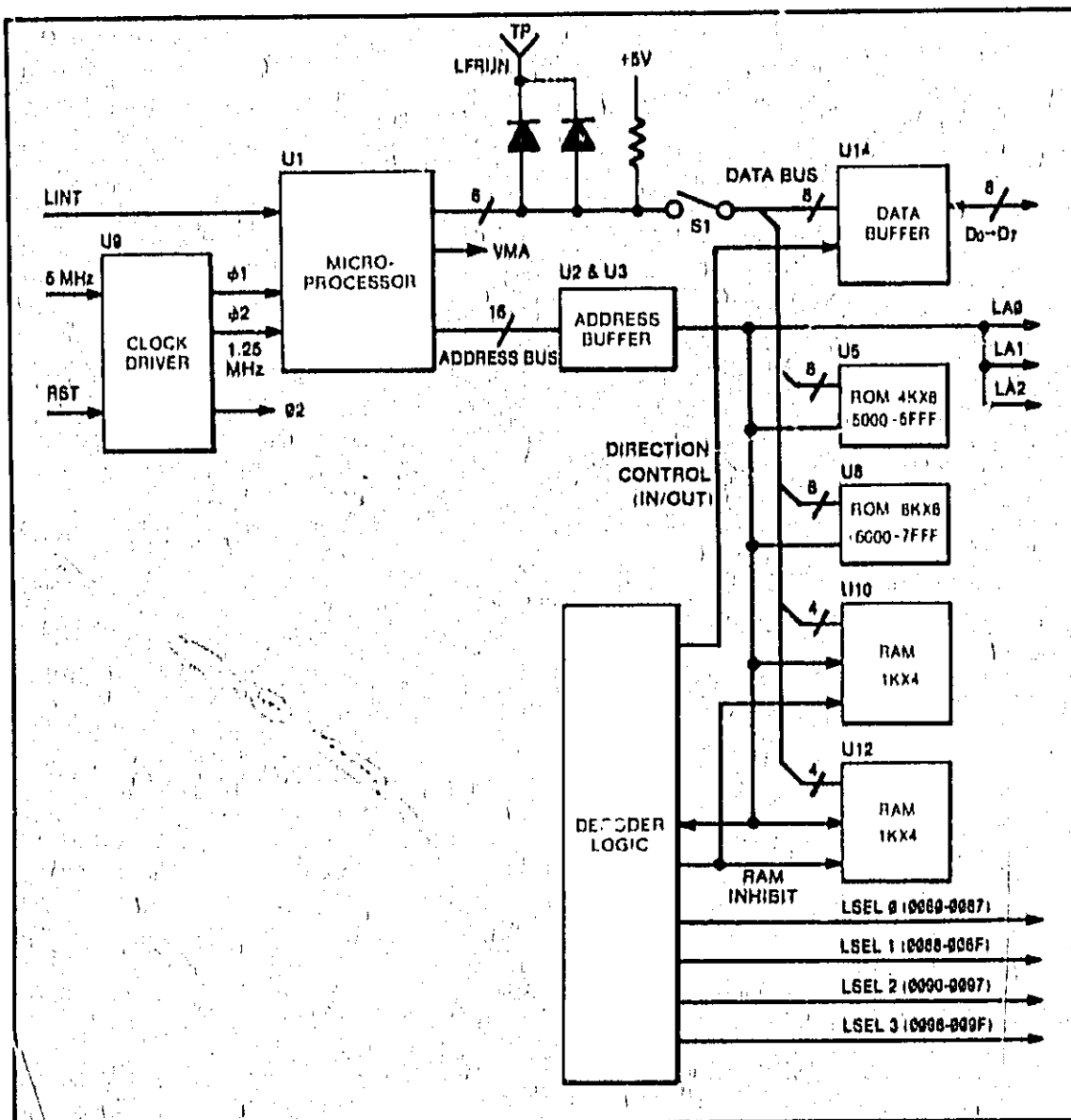


Figure 8-4. A7 Microprocessor Assembly Block Diagram

8-95. Microprocessor U1 has 16 address lines for a 16-bit address bus and 8 data lines for an 8-bit bidirectional data bus. The address lines are connected to two ROMs (one 4K and one 8K) and two RAMs via buffer-inverters U2 and U3.

8-96. The decoder logic decodes the address lines to supply 4 select lines (LSEL0-LSEL3) each of which controls 8 addresses provided by three address lines (LA0-LA2). The address lines and select lines are decoded on A8 Decoder assembly.

8-97. Data Bus switch S1 allows the bus lines to be opened for the freerun mode used in signature analysis troubleshooting.

8-98. CIRCUIT ANALYSIS. The A7 Microprocessor (MPU) assembly shown in Figure 8-34 contains in ROM the operating algorithm of the instrument. This assembly controls the measurement cycle, performs numerical computations for frequency measurements, and interfaces with many of the other assemblies.

8-99. The A7 MPU assembly uses the Motorola 6816 MPU (U1). The application in the HP 5355A is described in the following paragraphs.

8-100. The HP 5355A uses U1 for control and computation purposes. An expanded block diagram of U1 is shown in Figure 8-5. The 16-bit address bus allows the MPU to address up to 64K memory locations (not all used in 5355A). The data bus is 8 bits wide and is bidirectional. Data on the bus is read into the internal MPU registers when the Read/Write control line is low. All operations are synchronized to a two-phase nonoverlapping 1.25 MHz clock, $\phi 1$, and $\phi 2$. Each instruction requires at least two-clock cycles for execution. The 5355A utilizes the following additional 6800 control lines as indicated:

- a. **RESET** — This input is used to reset and start the MPU from a power-down condition, resulting from a power failure or an initial start-up of the processor. If a positive edge is detected on the input, this will signal the MPU to begin the reset sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFF, FFFF) locations in memory will be used to load the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$.
- b. **DATA BUS ENABLE (DBE)** — This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it would be driven by the $\phi 2$ clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.
- c. **INTERRUPT REQUEST ($\overline{\text{IRQ}}$)** — This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupt may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory. The $\overline{\text{FAL}}$ line must be in the high state for interrupts to be recognized. The $\overline{\text{IRQ}}$ has a high impedance internal pullup; however, a 3 K Ω external resistor to Vcc should be used for wire-OR and optimum control of interrupts.
- d. **VALID MEMORY ADDRESS (VMA)** — This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be

utilized for enabling peripheral interfaces. This signal is not three-state. One standard TTL load and 30 pF may be directly driven by this active high signal.

- e. READ/WRITE (R/W) — This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-state Control going high will turn Read/Write to the off (high impedance) state. Also, when the processor is halted, it will be in the off state. The output is capable of driving one standard TTL load and 130 pF.

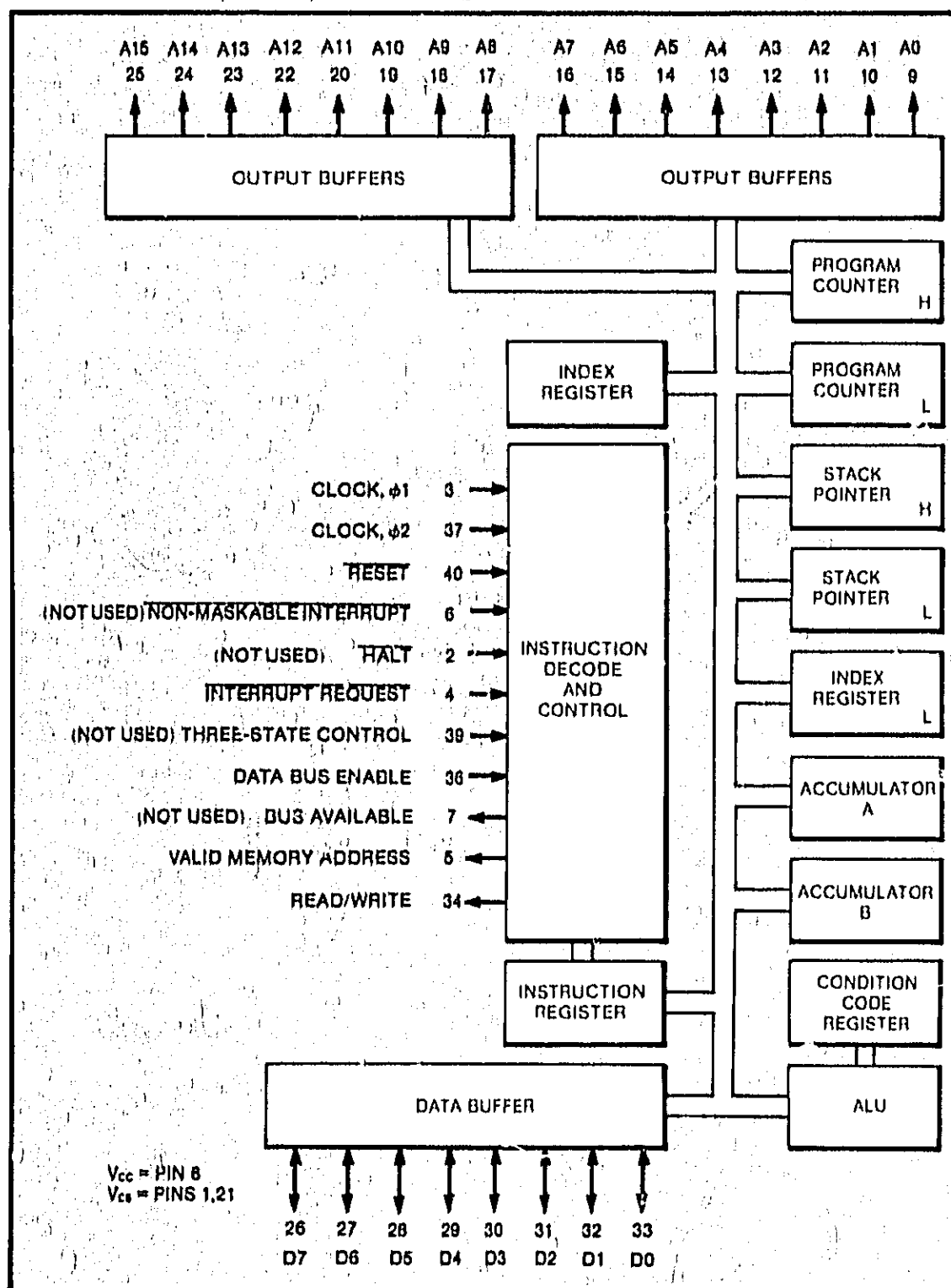


Figure 8-5. A7U1 Expanded Block Diagram

8-101. MPU U1 is driven by a two-phase clock, $\phi 1$ at U1(3) and $\phi 2$ at U1(37). As shown in Figure 8-25, the two-phase clock is derived from the 5 MHz input at XA7(TT).

8-102. The address outputs of U1 pass through three-state inverting line drivers U2 and U3 which are always enabled. (U2 direct memory access (DMA) applications, which are not implemented in the 5355A, Bus Available goes high indicating that the MPU has stopped and that the address bus is available.) The address lines drive RAMs U10 and U12 and ROMs U5 and U8.

8-103. To address a location in RAM, the enable inputs must be low (pins 8 and 10 of U10 and U12). The address inputs then select one of the 1024 locations in RAM. In a similar manner, memory selections are made in ROMs U5 and U8. The memories are controlled by the VMA (valid memory address) and R/W (read/write) signals from U1 microprocessor and LA13 and LA14 address lines, decoded by U15A and associated circuits.

8-104. The bidirectional data bus (D0-D7) read or write direction is controlled by bus driver U14. The control signals to U14 come from FF U11A and associated circuits, which receive the RD EN, WRT EN signals from the decoder logic and the HB ϕ 2 clock from clock driver U9. The HDBE (high data bus enable) signal from FF U11B resets U11A.

8-105. The address lines are decoded by decoder logic (U17A, U13, and U15) to develop LSEL0—LSEL3 signals which are combined with LA3—LA2 outputs on A8 Decoder assembly for further decoding. The MPU treats another assembly just like a memory location. To pass information between the register of the MPU and the registers of an external assembly, the program reads data from (or writes to) the location associated with the assembly. Address decoding circuitry decodes the address output from the MPU and generates a signal which enables the register on the assembly. For example, to read data from the A1 Front Panel Control assembly, LIRQ goes low which enables the three-state bus driver A1U1 to drive the data bus and send keyboard information back to the MPU.

8-106. The eight bidirectional data bus lines coming out of U1 pass through eight-section switch S1, which allows each line in the data bus to be opened for troubleshooting purposes. Resistor pack R5, with individual pull-up resistors connected to the data lines, together with two lines connected to ground via CR1 and CR2 (these lines connected to ground only when LFRERUN (TP2) is grounded), cause a CLB (clear accumulator B) instruction to be presented to the MPU when the switch (S1) is opened and LFRERUN is grounded. This causes the MPU to continuously increment the address on the bus from the least significant address (0000) to the most significant address (FFFF) for diagnostic purposes when using the 5004A Signature Analyzer. LFRERUN being grounded forces the Clear B instruction. With S1 opened, feedback is broken between the ROM outputs and the MPU inputs which is a necessary condition for taking signatures with the 5004A. In addition, when S1 is closed and LFRERUN (TP2) grounded, bus driver U14 outputs can be dynamically checked. Grounding TP2 sets U11(5) high, this places a low on U14 enable inputs to enable the drivers.

8-107. The memory assignments are summarized in Figure 8-6.

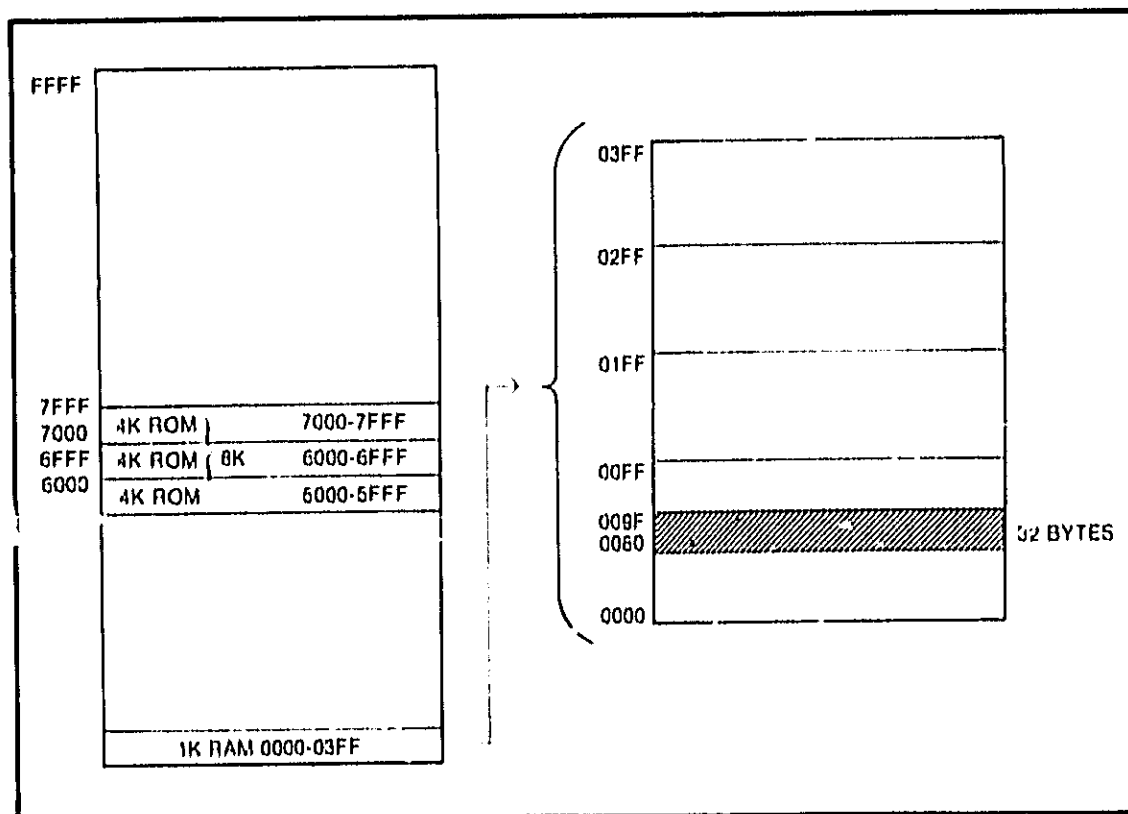


Figure 8-6. 5355A Memory Allocation

B-108. A8 Decoder/HP-IB Assembly

B-109. The A8 assembly consists of two separate groups of circuits: (1) decoder circuits, and (2) HP-IB circuits.

B-110. The decoder circuits, as shown in the block diagram, Figure 8-7, (U22, U25, and U24) receive the LSEL (low select) lines from the address decoder on the A7 microprocessor assembly, along with address lines LA0, LA1, and LA3. The address lines are decoded by each decoder into eight address lines. The address lines are connected via the data bus on the motherboard to control other boards (peripherals to the MPU). The decoders select the buffers that control the flow of data between the MPU and peripherals.

B-111. The HP-IB circuits include the Handshake (listen only) circuits, Data Buffers and control and address recognition.

B-112. CIRCUIT ANALYSIS. As shown in the schematic diagram, Figure 8-35, (sheet 1) address lines LA0, LA1, and LA2 are connected to the inputs of decoders U22, U25, and U24, which are enabled by LSEL0, LSEL1, and LSEL2, respectively, in addition to HBφ2. At the selected time, one of the decoder outputs goes low to initiate a function on another assembly. The output mnemonic and assembly designation is shown on the schematic. In addition, one output of the decoders is used to enable the other buffers on the board.

B-113. Three-state Buffer U13 receives the Stored ATN signal from the HP-IB circuit, the LVAGC signal from Prescaler A6 and HSQBY signal from A10 Pseudorandom Sequence Generator and is enabled by LDCRS from decoder U22 to pass the information to the Data Bus.

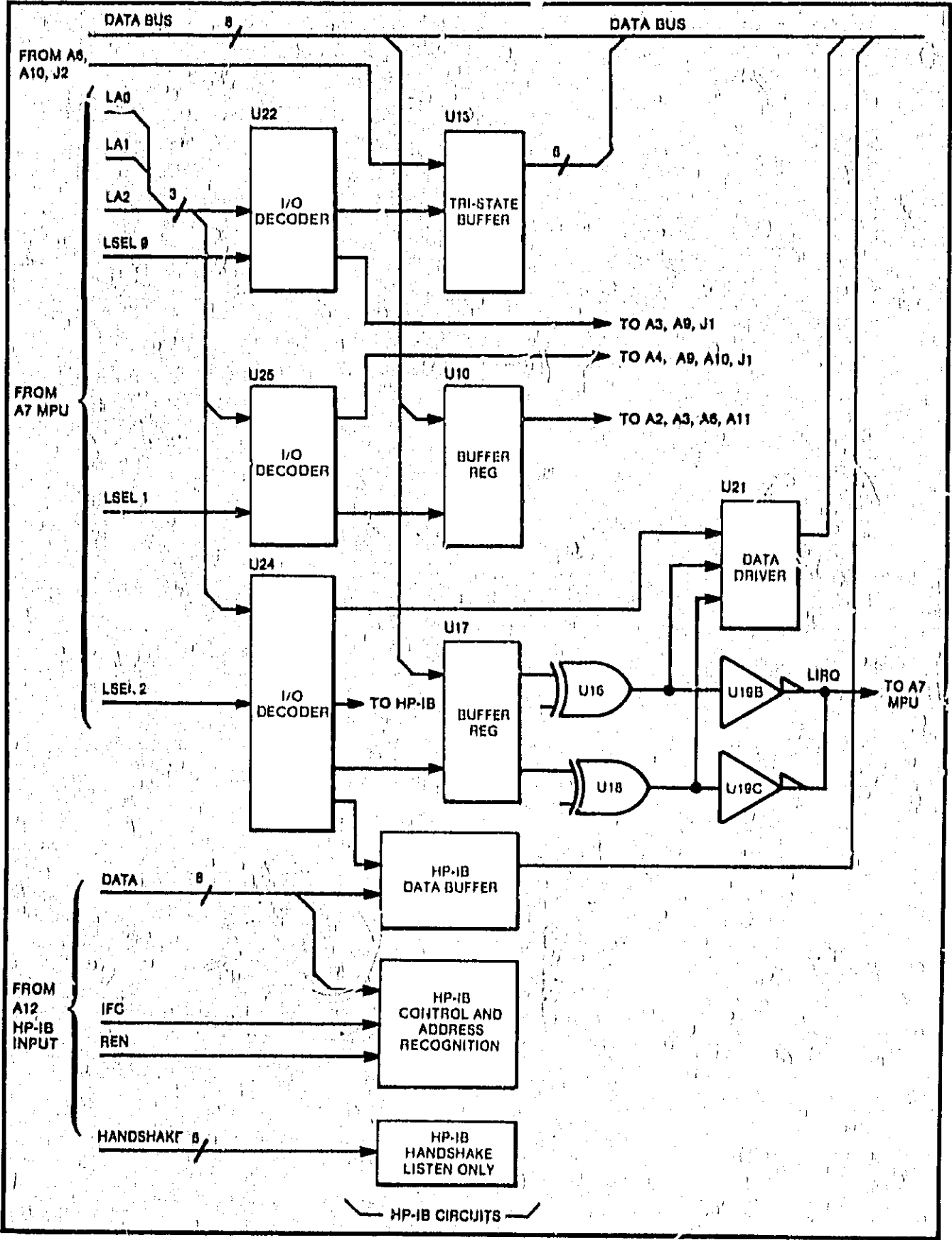


Figure 8-7. A8 Decoder/HP-IB Assembly Block Diagram

8-114. Buffer Register U10 stores data from the Data Bus and sends the signals to the circuits shown on the schematic, under control of the MPU.

8-115. Three-state Buffer Register U17, Data Driver U21, and associated circuits process HP-IB information and monitor RFC1, 2, and 3 signals (codes) from the 5356 Frequency Converter Head.

8-116. During the initialization routine (power-up), Buffer Register U17 is loaded with information (bit pattern) that prevents an interrupt until a condition occurs that requires an interrupt. If, for example, the 5355A is programmed to go to remote, gates U18B and U15C and inverter U19C would generate an interrupt (LIRQ) to A7 microprocessor (MPU). The MPU determines, via Data Driver U21 (change in logic state), which peripheral generated the interrupt, then Buffer Register U17 is updated.

8-117. HP-IB CIRCUITS. As shown in Figure 8-35, (sheet 2) the HP-IB data inputs from A12 HP-IB Input assembly are sent to three-state buffer U4. The data is output to the Data Bus when U4 is enabled by a decoded output of U24 (LHBRCl) and by comparator U7.

8-118. The handshake circuits consist of JK flip-flop U12 and associated circuits connected from/to A12 HP-IB Input board. The control lines from A12 (IFC, REN) go through FF U5 and to interrupt circuits shown on sheet 1. The address recognition inputs are processed by FFs U11, U6, and associated circuits and sent to the interrupt logic.

8-119. A9 Interface Assembly

8-120. The A9 Interface assembly, shown in Figure 8-36, contains three major groups of circuits that interface the 5355A plug-in with the 5345A mainframe: (1) Control Registers, (2) Enable Logic, and (3) Data Storage circuits.

8-121. CONTROL REGISTERS. The U15, U16, U17, and U18 registers store control bytes from the Data Bus. The majority of the output control bits go to the 5345A to provide the functions labeled on the schematic, except for three internal lines labeled 6800 XMT, DATA EN and OLD DISPLAY.

8-122. The write address LINW1 (Low Interface Write 1) from A8 Decoder clocks the registers U15 and U18; LINW2 clocks U16 and U17. The function of each of the data bits and the controlling address pulse is shown in Table 8-4, which uses the function names shown on the schematic. The functions are single control lines that go to the 5345A via umbilical connector P1, except for the three lines internal to A9 (6800 XMT, DATA EN and OLD DISPLAY), which are further described in Table 8-5.

Table 8-4. A9 Interface Data Bus Functions

Decoded Address Pulse	DATA BITS							
	D7	D6	D5	D4	D3	D2	D1	D0
LINW1	PI GATE	PI ARM	6800 XMT DATA EN OLD DISP A9 INTERNAL CONTROL LINES (See Table 8-5)			PI INH ARM	INH PROC	DISP STR
LINW2	DISPLAY MINUS SIGN	PI FUNC C	PI FUNC B	PI GT SEL		PI DATA	PI FUNC A	PI GT C PI GT B
LINWP (16 bytes)	DP D	DP C	DP B	DP A	DR D	DR C	DR B	DR A
LINRM (16 bytes)	DP D	DP C	DP B	DP A	DR D	DR C	DR B	DR A
LINRS	RST	PT SEL	MEAS TIME	PROC BUSY				

Table 8-5. A9 Internal Control of Data Flow

NOTE		
In this table RAM A9U11 is labeled P (plug-in data) and RAM A9U12 is labeled M (mainframe data). MPU A7U1 is labeled 6800, H=High, L=Low.		
6800 XMT (TP7)	DATA EN (TP1)	DATA FLOW
H	L	P→5345→M* (5345 Processing cycle controlled by PI CLK, PI CLK EN, PI XMT)
H	H	M→P (5345 Display Cycle controlled by LINRM, LINWP)
L	H	M→6800 (5345 Display Cycle controlled by LINRM)
H	H	6800→P (5345 Display Cycle controlled by LINWP)

*M Stores old display if "OLD DISPLAY" control is HIGH.

M stores measurement result if "OLD DISPLAY" control is LOW.

B-123. The logic gates connected to the output of register U15 are used to allow the PROC BUSY signal to select the output function for either the display cycle or processing cycle.

B-124. To read status, the LINRS (Low Interface Read Status) line is used to enable driver U14. The signal names shown on the schematic diagram at the input to U14 show the 5345A mainframe status sent to each input line.

B-125. In Table 8-4, for LINWP (Low Interface Write P) the upper 4 bits, D7-D4, are binary coded decimal point data (0-15). The lower 4 bits (D3-D0) represent BCD digits, which are stored in RAMs U11 and U12. The upper 4 bits are stored in registers U13 and U20. LINRM (Low Interface Read M) has the same bit structure as shown in the table.

B-126. ENABLE LOGIC. The combination of logic gates U1, U4, U5, U6, U8, and U10 provides clock signals to binary counter U9 and register U13. Enable signals are supplied to Data Storage RAMs U11 and U12 by the combinational logic which is controlled by signals from the input registers and from the 5345A (PI CLK and PI CLK EN), as shown on the schematic diagram. The data storage circuit operation is described in the following paragraphs.

B-127. DATA STORAGE CIRCUITS. Data (mantissa) from the 5345A is stored in 16 × 4 RAM U12 and data (mantissa) from the 5355A is stored in 16 × 4 RAM U11. Decimal point data (exponent) from the 5345A is stored in register U20 and decimal point data (exponent) from the 5355A is stored in register U13. The combinational logic described previously controls the flow of the data between the plug-in and mainframe. In addition, the flow of data between the data storage circuits and the A7 MPU is controlled by this logic.

B-128. The flow of data controlled by the A9 internal control lines is shown in Table 8-5. This table shows the data flow between RAM A9U11 (plug-in data storage) RAM A9U12 (mainframe data storage) and the 5345A. In addition, the flow between the RAMs and MPU A7U1 is shown. The logic states of the A9 control lines and the signals external to A9 that control the flow are shown in the table. For example, the first entry in the table shows that during the processing cycle of the 5345A, the data stored in RAM A9U11 goes to the 5345A, and the result from the 5345A goes to RAM A9U12. Then the 5345A processing is inhibited to allow the 5355A to process the data in A9U12. As shown in the table, the data stored in M (A9U12) will be the old (last) display data if control line OLD DISPLAY is high, however, if OLD DISPLAY is low

the data stored will be the result of a measurement at the end of the processing cycle. The table shows data flow control between the RAMs and A7 MPU (6800), for which DATA EN is high. Note that these transfers of data occur only during a display cycle.

8-129. A low CLD DISPLAY signal from U15(14) presets both sections of FF U5. After the 5345A processing cycle occurs, the M RAM (A9U12) will contain a measurement result. When the OLD DISPLAY signal is high, a data transfer occurs. PI CLK EN goes low then high and clocks U5B. After the third data transfer, U5(5) output goes low to U19(5) to inhibit the data transfer and prevent the measurement result from transfer to the M RAM. Thus, at the end of the processing cycle, the M RAM will contain the old display data. This action allows the 5355A plug-in to refresh the display after each processing cycle.

8-130. A10 Pseudorandom Sequence Generator and +C Assembly

8-131. As shown in the overall block diagram, *Figure 8-27*, this board has three main functions:

- a. To provide the 5 MHz clock for the microprocessor.
- b. To provide the 100 kHz reference for the phase detector.
- c. To generate the pseudorandom sequence for switching the VCO during the N determination routine.

8-132. CLOCK CIRCUITS. The internal standard 10 MHz signal from the 5345A enters A10, as shown in *Figure 8-37*, as an analog signal and is converted to TTL in U16. U15 provides two outputs of this signal: a divide-by-2 and a divide-by-10 output. The +2 output sends 5 MHz to the microprocessor board (A7). The +10 (1 MHz) output is again divided by 10 in U14 and becomes the 100 kHz reference for the phase detector. The 1 MHz signal also clocks the switching and gating circuits of U6 and U5.

8-133. The 1 MHz signal is also sent via U13, and U2, to U1, which divides the signal by 10. After the signal is gated by the deadtime pulse from U9D, it clocks U3 and U4 shift registers and U8 counter in the pseudorandom sequence generator.

8-134. PSEUDORANDOM SEQUENCE GENERATION. During acquisition in the CW mode, after a countable signal has been detected and the sweep stopped, the harmonic number N must be computed. The procedure is to first modulate the VCO by ± 2 MHz in a pseudorandom manner and measure the VCO frequency (Δf_0) in the 5345A's A-B mode. The procedure is repeated for a second pseudorandom sequence, and the Δf is measured in the same manner. N equal $|\Delta f / \Delta f_0|$. The switching between counters A and B is done in a pseudorandom fashion to prevent coherence between FM on the unknown signal and the switching rate between counters. This prevents an incorrect computation of N . Two different lengths are possible: 1) the normal or short pseudorandom sequence (PRS) lasts for ≈ 22.53 milliseconds (counter A and B in the mainframe are open for 10.24 ms each, plus 2.048 ms of "dead" time). This short PRS gives a worst case FM tolerance of 15 MHz peak-to-peak; or 2) the long PRS, which is selected by simultaneously pushing the 5355A front panel CW and PULSE pushbuttons, lasts for a total time of 360.4 milliseconds (counter A and B are open for 163.83 ms each, plus ≈ 32.6 ms of "dead" time). This long PRS gives an FM tolerance of 60 MHz peak-to-peak.

8-135. To begin the pseudorandom sequence, the microprocessor writes to A10 and sets U12 to the appropriate states. U12(15) is high before the sequence starts. U12 pins 10 and 12 also go High during the sequence. In the normal (short) PRS, U12(5) is High and U12(2) is Low. U12(7) is always Low and causes U1 to always divide by 10 (100 kHz output).

8-136. The PRS generator consists of shift registers U3 and U4, 4-bit binary counter U8, and logic gates U7, U9, and U11. Gates U10(C&D) and U11(A&B) comprise the Start/Reset logic. Just prior to the start of the sequence, U7C(8) is Low and U10C(8) and U12(12) are Low to clear U8, U3, and U4. When U12(12) goes High to start the sequence, it causes U10C(8) to go High and releases the previous clear state. Since the "load" line of U3(9) is Low, the first clock pulse will load a "5" or a "1" into U8 depending on the logic state of the C input. (High = short PRS = "5", Low = long PRS = "1".) To generate the sequence, data is shifted through the shift registers U4 and U3. Feedback taps exclusively "OR" two of the shift register outputs to generate the next input logic state. This feedback generates the PRS. For the short PRS, U11D(12) is High and U9B is used to perform the exclusive "OR" function (U9A is not used for the short PRS). For the long PRS, U11C(9) is High and U9A performs the exclusive "OR". The data is then fed back to the input of the shift register at U4(1, 2) via U7C and B.

8-137. The short PRS is 11 bits long and stops after 10 consecutive Lows in the sequence are entered into U4. The long PRS is 15 bits long and stops after 14 consecutive Lows in the sequence are entered into U4. The detection of the number of consecutive Lows in the sequence is performed by presettable counter U8. For the short PRS, "5" is preset into U8. When a Low appears in the sequence (High at U8 pin 9), the U8 counter is incremented by the PRS clock at U8(2). When a High appears in the sequence (Low at U8 pin 9), the counter reloads the "5" and begins counting up again from this initialized state. Because of the feedback technique, this process of U8 counting and then reloading continues for most of the sequence until finally the feedback is such that 10 consecutive Lows enter the shift register. This means that U8(9) has been High for 10 consecutive clock pulses, which allows it to count up and not be reset to a count of 5. After 10 consecutive Highs at U8(9) have occurred, U8 has counted to "15" and the carry output at U8(15) then enables U10A so that the 10th clock causes U10A(3) to go Low. This resets the latch formed by U11A and U10D so that U10C(8) goes Low to reset U3 and U4 to stop the sequence.

8-138. The operation is similar for the long PRS: this time "1" is preset in U8 so that the carry output of U8 goes High after 14 consecutive Low have entered the shift registers during the PRS. Once done, the carry out of U8 sets the latch so that U10C(8) goes Low to clear the PRS generator and stop the sequence. During the long prs, gates U9A and U11C are used for the feedback and U9B and U11D are not needed.

8-139. DEAD TIME CIRCUIT. The A/B SWITCH line switches logic states in a pseudorandom fashion. When this line is High it causes circuits on the A11 board to pass either the IF signal or the +4 VCO signal to Channel A for counting in the mainframe. When Low, the signal is counted in the B channel. When switching from one channel to the other, the gate should be closed to prevent the mainframe from counting any transients that may occur. This is accomplished with the A/B GATE line and the dead time circuitry. To prevent miscounting, 2 microseconds of dead time are added to each transition in the pseudorandom sequence, allowing signals to the counters to be turned off during the transition from counter A to counter B, as shown in Figure 8-8.

8-140. The dead time in the A/B GATE signal is generated by D flip-flops U6A, U6B, exclusive "OR" U9D, and D flip-flop U5B. The dead time is generated when U9D(11) (DT line) goes High for two periods of the 1 MHz clock. With DT High, U2C is disabled and the output of U2A remains Low to disable the pseudorandom sequence during this time.

8-141. Assume that U7C(8) and U6 pins 5 and 9 are Low (see Figure 8-9). U9D(11) and U5B(9) will also be Low. When U7C(8) goes High, DT goes High immediately because of U9D. This disables U2C and stops the PRS clock. The next 1 MHz clock pulse from U13E clocks the High into U6A and also causes the A/B GATE to go High, which stops the mainframe from counting. The next 1 MHz clock pulse places the High on U9D(12) and U9C(10). This causes the DT line to return Low to allow the PRS clock to restart, and it also causes the A/B SWITCH line to change state via U9C. The next 1 MHz clock pulse keeps the DT line at the same logic state but clocks the output of U5B Low (mainframe is gated on for counting).

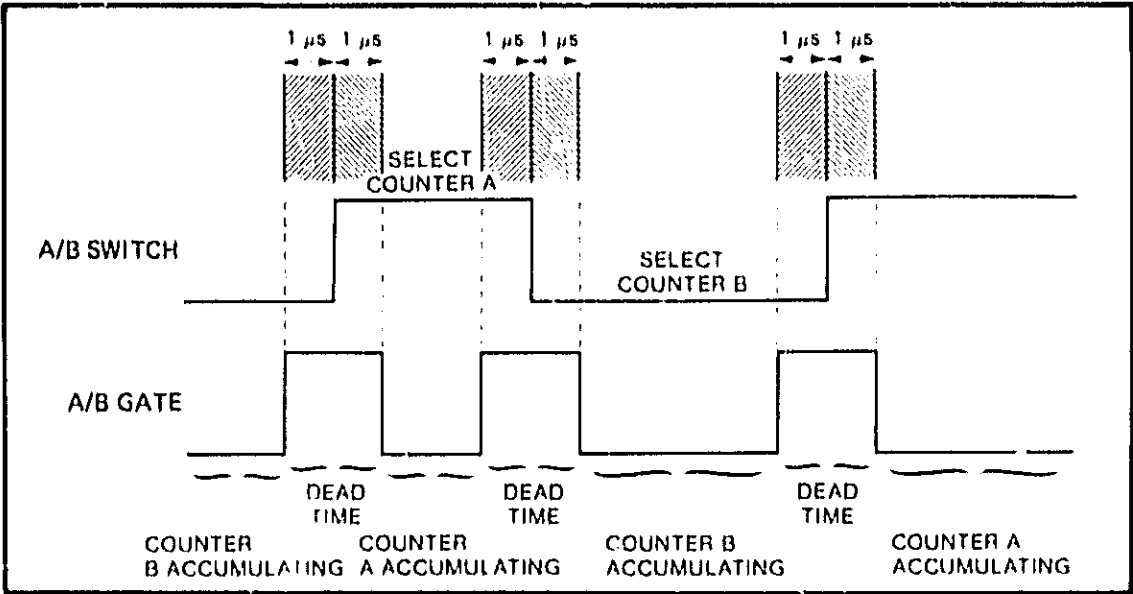


Figure 8-8. A/B Gate and A/B Switch Signal Timing Diagram

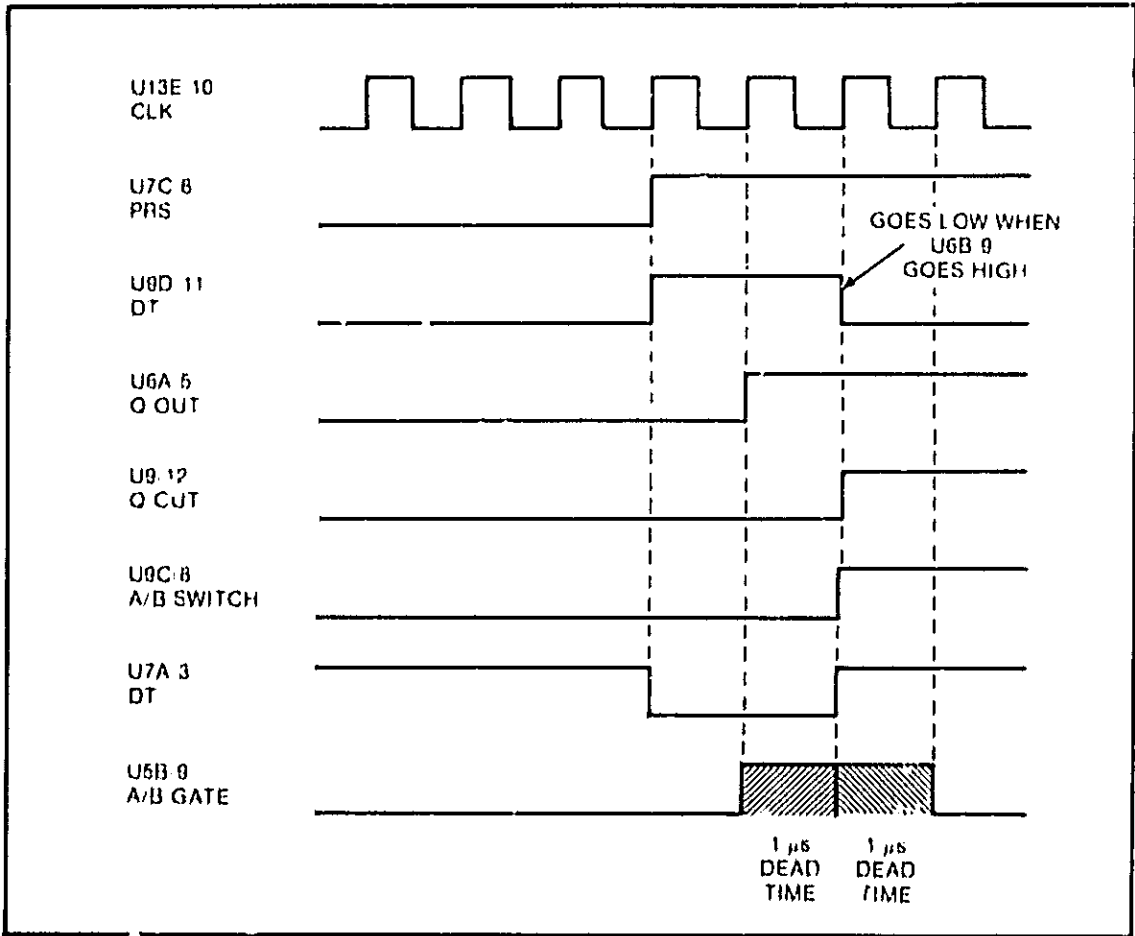


Figure 8-9. Deadtime Timing Diagram

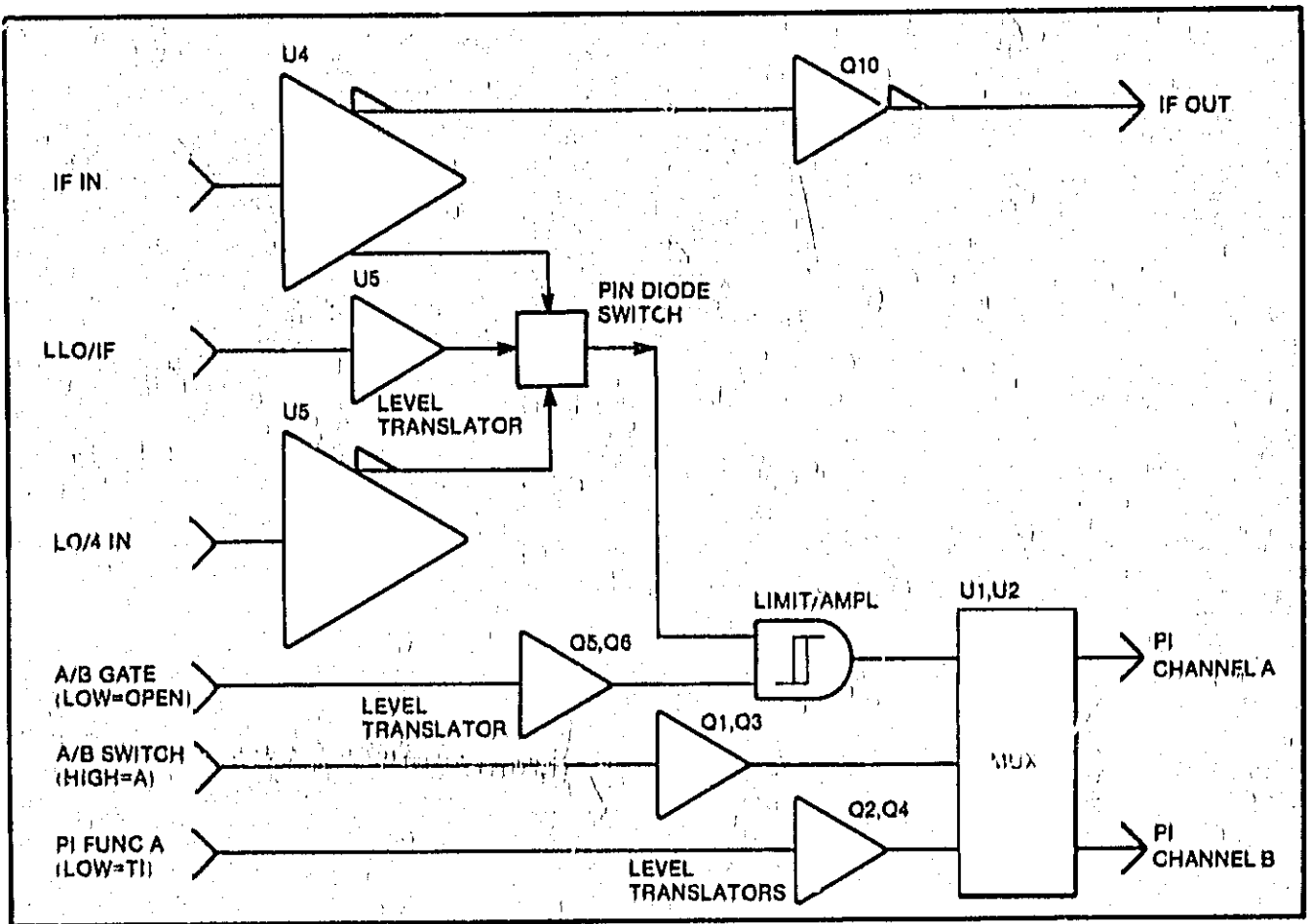


Figure 8-10. A11 Signal Switch Assembly Block Diagram

8-142. A11 Signal Switch Assembly

8-143. As shown in the block diagram, Figure 8-10, the A11 board performs three main functions:

- a. Selects which signal goes to the 5345A, either the IF from the A3 board or the LO+4 from A4 board. There are two reasons for sending the LO+4 signal to the mainframe:
 1. In the CW mode, the pseudorandom sequence (PRS) is used to determine the harmonic number. Because of the way the PRS is applied, it is not known exactly what the Δf_0 is (the LO is switched outside of its bandwidth, so it is not locked), it is not fixed. To get around this, the counter runs the PRS and measures the Δf ; then runs it again and measures the Δf_0 (the VCO FREQ +4). It is assumed the change in the f_0 will be the same both times. The harmonic number (N) is $\Delta f / \Delta f_0$.
 2. In PULSE mode, the 5345A uses external gate. However, the 5345A has a gate offset, (there is a differential propagation delay in opening and closing the gate), which causes a constant error in the measured frequency for frequency average type measurements (i.e., PULSE mode). The error will depend on frequency and pulse width. To help eliminate this error, the counter performs a calibration where it measures the VCO frequency, gating it on and off with the internally generated gate. The total calibration number takes 10 measurements. Each successive measurement adds to the number until the final number is reached.

The first reading is uncalibrated. During the calibration, the 5345A displays a "C" (in the most significant digit position). After 10 measurements, the unit will maintain that calibration factor until it loses the signal and has to reacquire, or the pulse width changes by more than 12%.

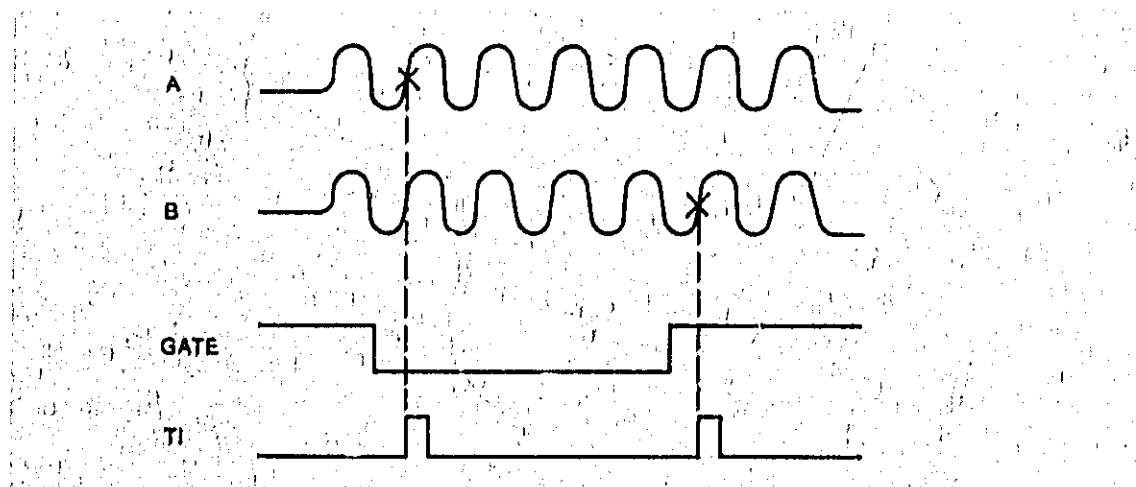
- b. Must be able to switch the signal (either IF or fo) to 5345 A Channel or B Channel to perform A-B (Δ) function
- c. Provide IF output monitor.

8-144. CIRCUIT ANALYSIS. The IF signal enters J1 from A3, as shown in Figure 8-38, goes through buffer U4 and transistor Q10 (output ≈ 0 dBm). The IF OUT goes to the rear panel IF OUT jack via coax cable (for monitoring purposes). The noninverting output of U4 and the VCO $\div 4$ output signal at U5(5) go to PIN diode switch network CR1-CR6. One of these signals is passed to U3 Limiter/Amp depending on the state of the LLO/IF line. This TTL level is converted to voltages capable of driving the PIN diodes. If the IF signal is to be passed, Q8 collector will be -1.5 V, which turns CR5 off and allows CR3 and CR1 to conduct. Q9 collector will be $+0.6$ V, which turns CR6 on (short to ground) and biases CR4 and CR2 off.

8-145. U3 Limiter/Amp is used for two purposes: 1) It is used as an RF to EECL converter, i.e., the input is an RF signal and the output is an EECL logic signal. 2) It gates the signal on and off. When running the PRS, the counter must be inhibited from counting while the signal is switching between the A and the B channels. The signal is gated on and off at U3 pin 7. U3 is gated off 1μ s before the signal is switched from A to B (or vice versa). The GATE line goes through TTL to EECL translator Q6 and Q5.

8-146. U2 and U1 are EECL multiplexers that pass the input signal (either IF or VCO $\div 4$) to the A and B channels of the 5345A. Both multiplexers can pass the input signal simultaneously (PI FUNC A line = Low) or they can switch to one channel and then the other (A/B SWITCH line: L=B, H=A).

8-147. PULSE WIDTH CHECK. During a pulsed RF measurement, the pulse width is checked to ensure it doesn't change by more than 12%. Since the 5345A cannot measure the pulse width directly, it makes a TI holdoff measurement by sending the IF to both channels and using the external gate pulse as the holdoff pulse, as shown below:



8-148. A12 HP-IB Input Assembly

8-149. The A12 assembly provides an interface between the Hewlett-Packard Interface Bus (HP-IB) and the A0 Decoder/HP-IB assembly.

8-150. The A12 assembly, shown in *Figure 8-39*, contains the HP-IB connector and is mounted inside the 5355A rear panel. A pc connector mounted on this board receives connector A8P1.

8-151. The input data and control lines from the HP-IB connector go through inverters (U1 and U2) to change the negative-true bus logic to positive-true logic for processing by the HP-IB circuits on A8 assembly. Resistor packs R1 and R2 provide pull-up resistors for these lines.

8-152. Address switch S1 is connected to one set of binary weighted inputs of comparator U3. Data lines DIO1 through DIO4 are connected to the other set of inputs. When an address on the lines matches the switch settings of the address switch, the U3(6) output goes to the Listen FF on A8 HP-IB circuits to initiate the listen mode of the 5355A.

8-153. A13 Motherboard

8-154. The motherboard, *Figure 8-26*, contains pc connectors XA2 through XA11 for plug-in assemblies A2 through A11. Assembly A1 is the Front Panel Control assembly and A12 is the HP-IB Input assembly, which is mounted inside the rear panel. Voltage regulators A13U1 and A13U2 are installed to provide clean, noise-free -5.2 and +15 volts to A14 VCO and to the 5356 frequency converter head, as shown in *Figure 8-11*. These regulators are needed to insure stable performance from the A14 VCO and noise-free operation from the 5356 converter head.

8-155. Connector P1 at the rear of the motherboard connects to the 5345A mainframe. The signals and interconnections are described in *Table 8-2*.

8-156. The "E" terminals on the motherboard connect to cables with the labels listed below:

Motherboard Terminal	Cable Label
E5	E5W12 PULSE OUT to J4
E6	E6W11 GATE OUT to J3
E4	E4W8 to J9 (umbilical connector to 5345A)
E1	-5.2V E1W5 -5.2 to A14C5
E2	+15V E2W6 +15 to A14C6
E3	A13E3W4 to A14J6
E7	A13E7W14 to A3J2

8-157. The motherboard connections to the multipin connector J2 on the front panel are as shown in *Figure 8-11*.

8-158. A14 Voltage Controlled Oscillator (VCO) Assembly

8-159. As shown in the block diagram, *Figure 8-27*, the A14 VCO receives a dc error voltage from A5 DC Amplifier/Compensator and provides two outputs. One output (RF) is sent to the 5356 Frequency Converter Head as a local oscillator signal. The other output is the phase-locked loop (PLL) signal to the +4 circuit on A4 Programmable Divider. The -5.2 and +15 volts for A14 are supplied by regulators U1 and U2 on A13 motherboard.

8-160. The dc error voltage (2-10V) to the VCO is the tuning voltage (VT) input shown in *Figure 8-40*. The transfer function of the VCO is the tuning voltage in versus frequency out. The VCO (U1) operates in the frequency range of 900--1050 MHz and is amplified approximately 10 dBm by Power Amplifier U2. One of the outputs of U2 (RF) is sent via front panel multipin connector J2 to the 5356 Frequency Converter Head as the local oscillator signal (labeled VCO). The other output (PLL) is sent via a 20 dB isolation pad (resistors R2 and R3) and buffer U3 to the +4 circuit on A4 Programmable Divider. The +4 circuit output goes to the +M circuit on A4 which is programmed by A7 Microprocessor and determines the synthesizer frequency.

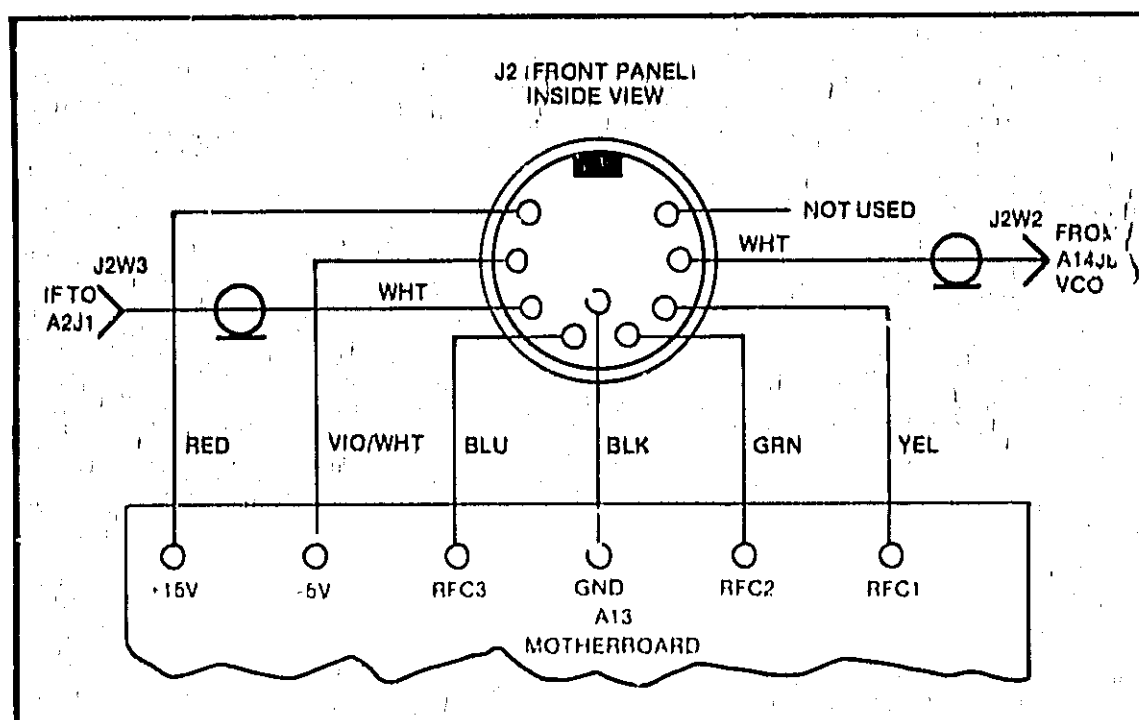


Figure 8-11. Multipin Connector J2 (Front Panel) Connections to A13 Motherboard

8-161. 5356A, B OR C FREQUENCY CONVERTER HEAD

8-162. There is an upper limit to the frequencies at which automatic microwave frequency measurements may be made when connecting a coaxial cable between the source and the counter. This is because the cable's losses are generally greater for higher frequencies, thus demanding more sensitivity from the counter, while microwave counters become less and less sensitive at higher frequencies. Thus a frequency is reached where not enough signal reaches the counter to trigger it properly. These conditions dictate using a waveguide instead of a coaxial cable. However, waveguides are suitable only for certain frequency bands, e.g., K-band (18-26.5 GHz) or R-band (26.5-40 GHz). Moreover, they are expensive and lack the mechanical flexibility of the coaxial cable.

8-163. Frequency Converter Heads Models 5356A/B/C, Figure 1-1, combine the convenience of coaxial cables with the broad frequency band of a microwave counter (1.5-40 GHz), and can be used for either CW or pulse measurements. These heads convert microwave frequencies to intermediate frequencies (IF) using the sampling technique. The sampling frequency input to the head and the IF output from it are connected by an attached 1.68-metre cable to the 5355A Automatic Frequency Converter. The microwave input frequency to the head is calculated from measurements of the IF and the answer is displayed on the 5345A Counter. The down-conversion is performed completely in the head and only the IF is connected to the 5355A.

8-164. To cover the frequency band up to 40 GHz, four different connectors are available: N, SMA, APC-3.5 and waveguide. Three models and two options are available to suit various applications. Table 8-6 shows the frequency ranges of the five heads.

8-165. The heads have male connectors because sources generally have female connectors. The 5356A has an N-type connector and is useful up to 18 GHz. The 5356B has an SMA connector, and can be used up to 26.5 GHz. To strengthen the SMA male connector, a special collar was designed to protect it. The collar also makes it easier for the user to connect it to the source. Some users prefer a K-band waveguide from 18 to 26.5 GHz; the 5356B Option 001 has a WR-42 connector to meet this need. The APC-3.5 connector, which is mode-free to 34 GHz, is used up to

40 GHz in the 5356C. The effect of this connector's moding between 34 and 40 GHz is taken into account by reducing the specified sensitivity by 5 dB in this region. A special collar is used for the APC-3.5 connector to strengthen it and to protect it from damage. Waveguide connector WR-28 is also offered, for using only R-band (26.5 to 40 GHz).

Table 8-6. Model 5356A/B/C Frequency Ranges and Connectors

FREQUENCY	HEAD	CONNECTOR	*HEAD CODE
1.5-18 GHz	5356A, Option 001	N	0
1.5-26.5 GHz	5356B	SMA	1
18-26.5 GHz	5356B, Option 001	Waveguide (WR-42)	2
1.5-40 GHz	5356C	APC-3.5	4
26.5-40 GHz	5356C, Option 001	Waveguide (WR-28)	5

*NOTE: Head code is displayed on the 5345A on power up.

8-166. 5356 Simplified Block Diagram

8-167. Figure 8-12 shows a simplified block diagram of the 5356A/B/C. The input voltage-controlled oscillator (VCO) frequency to the 5356A/B/C varies from 885.2 MHz to 1056 MHz and the output IF to the 5355A varies from 1 MHz to 528 MHz. The IF output is proportional to the RF input within the 5356A/B/C's dynamic range. All of the components in the head are built in thin-film microcircuit configurations.

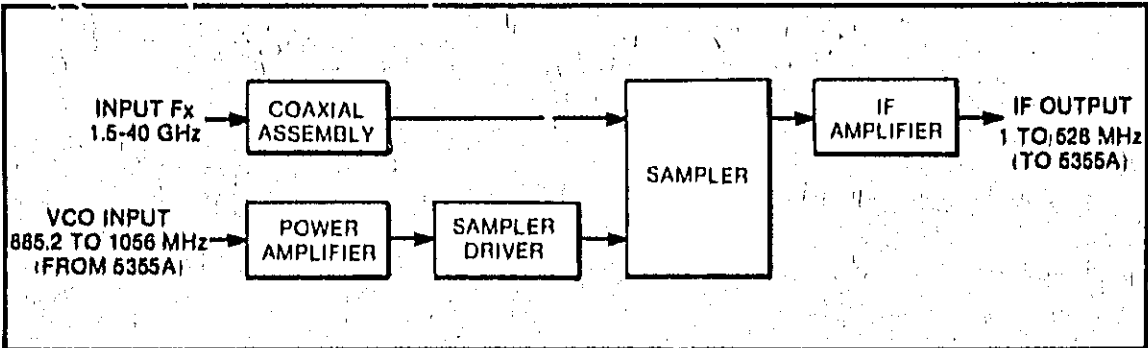


Figure 8-12. 5356 Simplified Block Diagram

8-168. The coaxial assembly shown in Figure 8-12 is replaced by a high-pass filter for the 5356A Option 001. Since the 5356/5355 is a pulse counter, the input pulse may contain a video signal. This signal may be so large that it overloads the counter, especially since the IF gain is about 80 dB. To attenuate such video signals, Model 5356A Option 001 has a high-pass filter between the input connector and the sampler. The filter's maximum insertion loss from 1.5 to 18 GHz is 1 dB, and its minimum insertion loss below 100 MHz is more than 35 dB.

8-169. Power Amplifier

8-170. The power amplifier is housed in a TO-8 package using a thin-film alumina substrate. It consists of two stages, a gain stage and a power stage. The amplifier is driven to saturation so that its output is insensitive to input variations. The IF amplifier is housed in a TO-12 package using a thin-film sapphire substrate. It also consists of two stages.

8-171. Head Construction

8-172. The head casting consists of an upper half and a lower half. The sampler and the two printed circuit boards are mounted on the lower half. Heat sink materials are attached to the upper half to dissipate the heat from the power amplifier and the IF amplifier. There is also a heat sink on the lower half for the power amplifier. As a result, the temperature rise is less than 9°C. The heat sink materials also serve as shock absorbers for mechanical vibrations. The casting is designed to accept the different input connectors: N, SMA, APC-3.5, waveguide WR-42, and waveguide WR-28. The casting is also designed for improved EMI (electromagnetic interference) performance. All of the parts inside the head can be disassembled easily, using a screwdriver and an SMA wrench. As a result, the 5356A/B/C is easy to disassemble for troubleshooting.

8-173. Sampler Driver

8-174. The heart of the frequency converter head is the sampler driver. Figure 8-13 shows a schematic diagram. The driver is built in a coaxial package. Inductors L3, L2 and capacitors C3, C2 form a matching network to match the impedance seen at C1 to 50 ohms. L1 is drive inductance and C1 is tuning capacitance. The step-recovery diode has a very fast rise time that generates a comb of harmonics of the VCO frequency. One of the comb frequencies is heterodyned with the input microwave frequency to produce an IF output in the proper range.

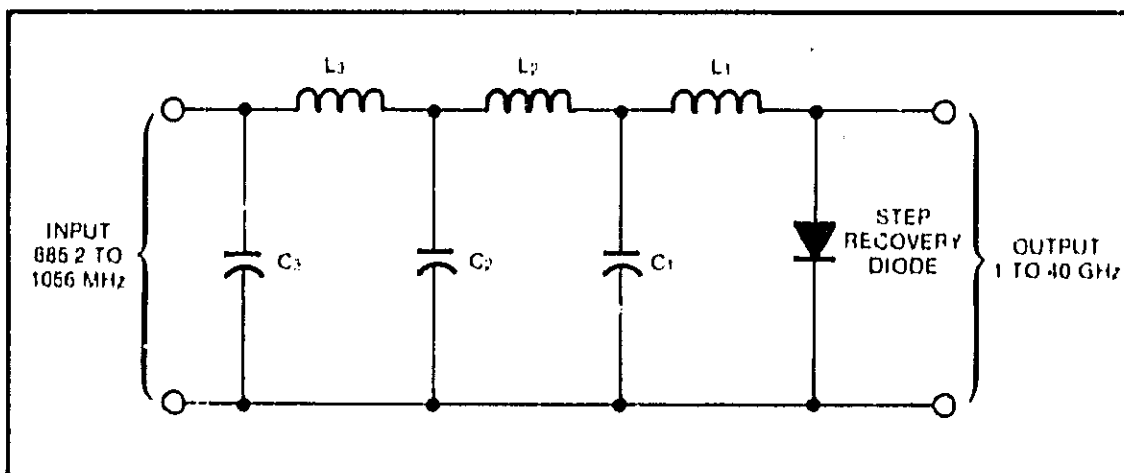


Figure 8-13. Sampler Driver Used in the 5356A/B, C

8-175. Sampler

8-176. Figure 8-14 shows a schematic diagram of the sampler. It consists of a thin-film hybrid mounted in an aluminum package. Two versions of the sampler are used. The 5356C 40-GHz sampler is the same basic design as the 5356A/B with slightly different component values. For the 5356C, R1 and R2 are chosen to maximize the sampler's dynamic range up to 40 GHz.

8-177. The sampler's IF output is designed to be insensitive to sampler driver variations. The minimum output from the sampler driver is enough to drive the sampler into saturation. Therefore the IF output is also insensitive to temperature variations.

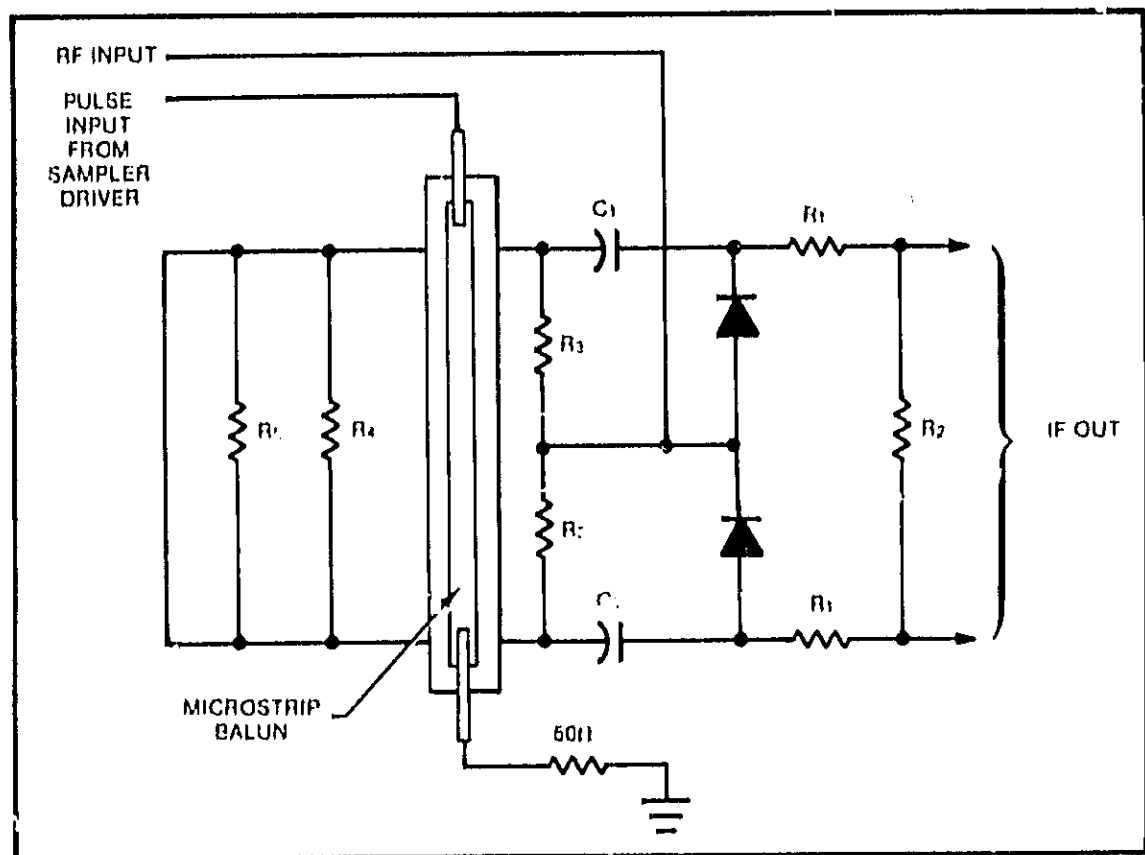


Figure 8-14. 40 GHz Sampler Used In the 5356C

8-178. 5355A/5356 Compatibility

8-179. The interface between the 5355A and 5356 is analog, since the VCO signal comes from the 5355A to drive the power amplifier in the 5356, and the IF comes from the 5356 to drive the IF amplifier in the 5355A. To guarantee complete compatibility the following conditions apply.

- The IF output from the 5356 is insensitive to the level of the VCO input from the 5355A. The lowest VCO input power level at any frequency is sufficient to drive the power amplifier to saturation. Thus the output of the sampler driver is insensitive to the 5355A VCO level.
- The IF output from the 5356 to the 5355A is sufficient to guarantee the minimum sensitivity of the combined system. The counter sensitivity is defined as the 5356 conversion efficiency (RF to IF) plus the 5355A IF sensitivity. The 5355A IF sensitivity is adjusted to meet the required specifications and the 5356 conversion efficiency is tested from 1.5 to 40 GHz to assure that it meets the necessary levels.
- The input of the 5355A is unconditionally stable so that it will not oscillate with any 5356. Also, the output of the 5356 is unconditionally stable with any 5355A. This is especially important since the IF gain of the combined system can exceed 80 dB.

8-180. As shown in Figure 8-41, the microwave input signal is applied through connector J1 and a coax cable assembly, to U1 Sampler. In the 5356A Option 001, the coax cable assembly is replaced with a high-pass filter. (This filter is provided for users whose RF burst signals are generated by a PIN attenuator. The video component of the RF burst must be filtered.) The signal is sampled at a rate determined by the programmable frequency synthesizer in the 5355A. The synthesizer, which is phase-locked to the 10 MHz quartz reference in the 5345A, drives U2 Sampler Driver via amplifier A1U1 in the 5356A/B/C. The U2 Sampler Driver (step recovery diode)

produces useable harmonics up to over 40 GHz for U1 Sampler. The U1 Sampler output, consisting of sum and difference frequencies produced by the harmonics mixing with the input frequency, is amplified by IF Amplifier A2U1 in the 5356A/B/C to supply the IF output.

8-181. The IF output is sent to A2 IF Limiter Amplifier in the 5355A via the 1.68 metre (5½-foot) cable attached to the 5356A/B/C. The cable connector mates with the multipin connector on the front panel of the 5355A. The cable (see *Figure 8-11*) connects the 5355A VCO output to the 5356A/B/C in addition to operating voltages and head code wires. The head code wires are connected to the floating or ground terminals labeled ID1, ID2, and ID3 to establish the head code.

8-182. Operating voltages are supplied to the 5356 by voltage regulators U1 and U2 on A13 motherboard, as shown in *Figure 8-27*.

8-183. EXTENDER BOARD SERVICE KIT

8-184. The 05355-60100 Extender Board Service Kit contains seven extender boards and four coax cables, as shown in *Figure 8-15*, designed as an aid in troubleshooting the HP Model 5355A Automatic Frequency Converter. A replacement parts list and operating information for the 05355-60100 Extender Board Kit is provided in the following paragraphs. Also included is a schematic diagram and theory of operation of the 05355-60025 extender board.

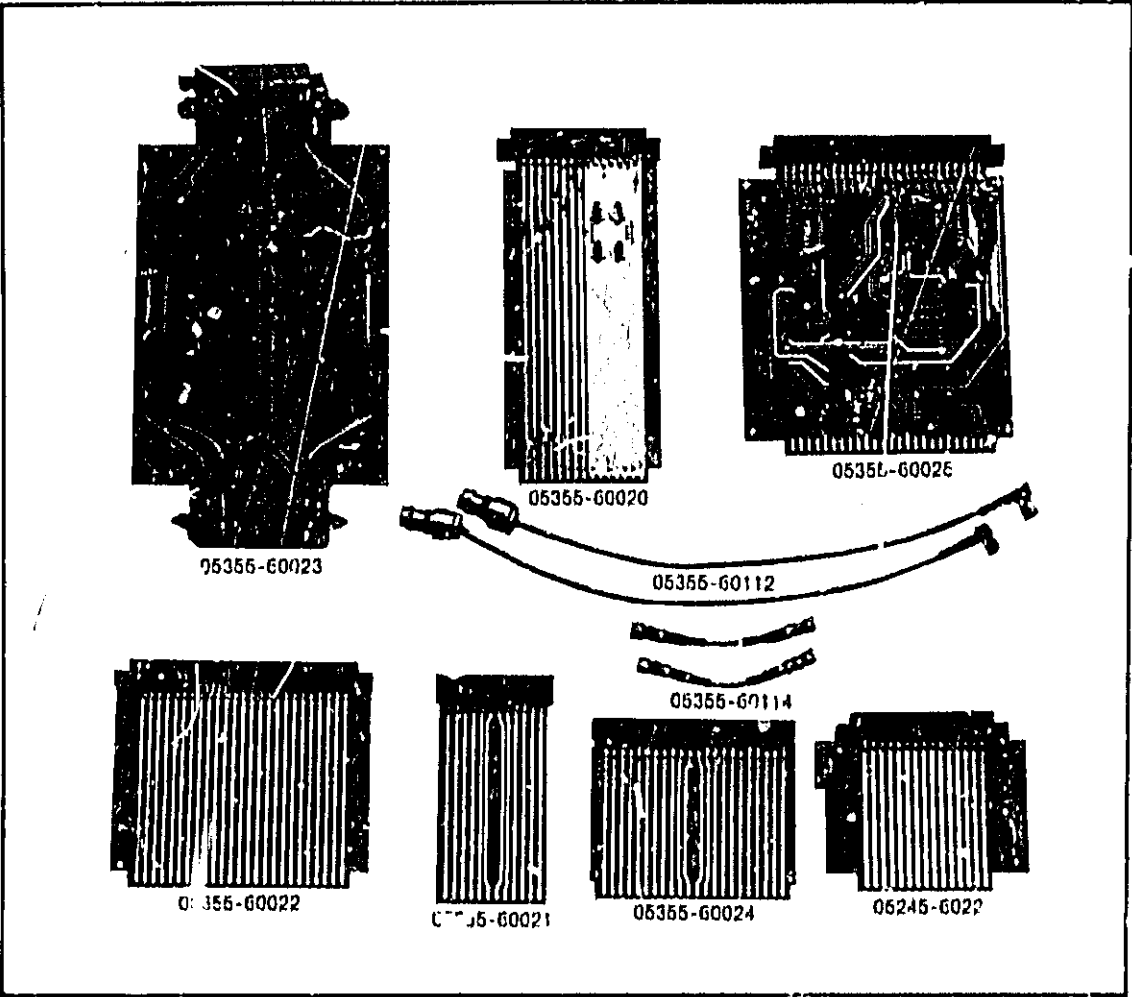


Figure 8-15. 05355-60100 Extender Board Kit

8-185. Equipment Supplied

8-186. Table 8-7 lists the boards contained in the 05355-60100 Extender Board kit with their general descriptions and usage.

Table 8-7. 05355-60100 Kit Contents

HP Part No.	Qty.	Description and Use
05245-6022	1	15 pin X2 extender board for A2 and A11 assemblies.
05355-60020	1	15 pin X2 extender board for A6 assembly. Used for troubleshooting but not adjustment of A6. Jacks are available for connection of test equipment to +B output and gate output signals. The 05355-60114 cables are normally installed to complete these signal paths. (See Figure 8-16)
05355-60021	1	12 pin X2 extender board for A8 assembly.
05355-60022	1	25 pin X2 extender board for A9 and A10 assemblies.
05355-60023	1	Plug-in extender. Extends plug in from mainframe to allow adjustment of A6 Prescaler assembly through plug-in side frame.
05355-60024	1	22 pin X2 extender board for A3, A4, and A5 assemblies.
05355-60025	1	25 pin X2 extender board for A7 assembly.
05355-60112	2	12 inch SMC (f) to BNC (f) cables for aid in making troubleshooting connections.
05355-60114	2	3 inch SMC (f) to SMC (f) cables for providing normal signal path connection of +B output and gate output on A6 Extender Board 05355-60020. Cables can be removed to provide test equipment connection to A6 Extender board jacks. (See Figure 8-16.)

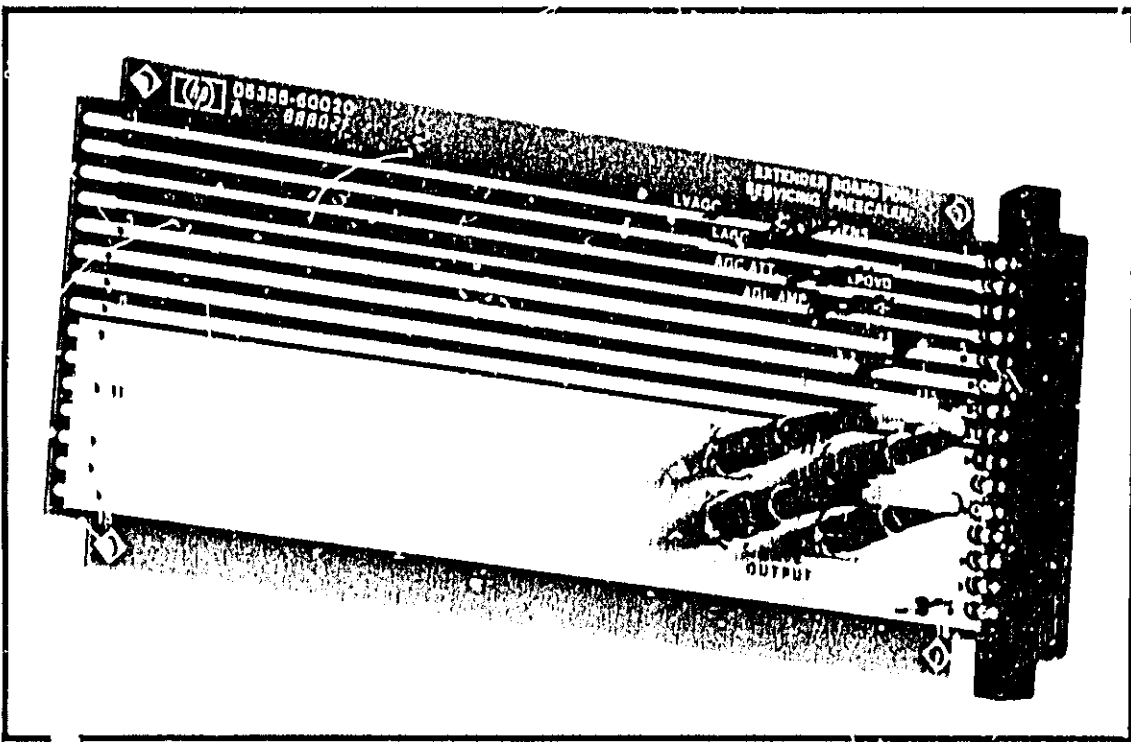


Figure 8-16. 05355-60114 Cables Installed on 05355-60020 Extender Board (for A6 Assembly)

B-187. Replaceable Parts

B-188. The only replaceable parts in the 05355-60100 kit are those components on the 05355-60025 board. Table B-8 lists the HP part number and description of those parts. Refer to Section VI for ordering information.

Table B-8. Replaceable Parts for 05355-60025

REF. DES.	HP PART NUMBER	C. D.	QTY.	DESCRIPTION	MFR. CODE	MFR. PART NUMBER
	05355-60025	9		SERVICE BOARD (A7 MPU EXTENDER) (SERIES 1840)	28480	05355-60025
C1	0160-3879	7	2	CAPACITOR-FXD .01UF $\pm$ 20% 100VDCW CER	28480	0160-3879
C2	0160-3879	7		CAPACITOR-FXD .01UF $\pm$ 20% 100VDCW CER	28480	0160-3879
R1	1810-0280	8	1	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R2	1810-0272	8	1	NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
S1	3101-1856	5	3	SWITCH-SL 8-1A DIP-SLIDE-ASSY .1A 50VDCW	28480	3101-1856
S2	3101-1675	6	1	SWITCH-TGL SUBMIN DPST .5A 120VACW/DC PC	28480	U101-1675
S3	3101-1856	5		SWITCH-SL 8-1A DIP-SLIDE-ASSY .1A 50VDCW	28480	3101-1856
S4	3101-1856	5		SWITCH-SL 8-1A DIP-SLIDE-ASSY .1A 50VDCW	28480	3101-1856
U1	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U2	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U3	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U4	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U5	1820-1187	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
MISCELLANEOUS PARTS						
	0360-0535	0	5	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
	1251-2413	7	1	CONNECTOR-PC EDGE 25-CONT/ROW 2-ROWS	28480	1251-2413
	1990-0486	6	8	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486

B-189. Operation

B-190. The following paragraphs describe the general operation of the 05355-60025 extender board (for A7 assembly). Included is a description of the LEDs (and their meaning on power up) as well as the individual circuitry on the board. Figure B-17 shows the signals present at TPU5 and TPU8. Figure B-18 is the schematic diagram of the 05355-60025 extender board.

SERVICE INFORMATION CON'T

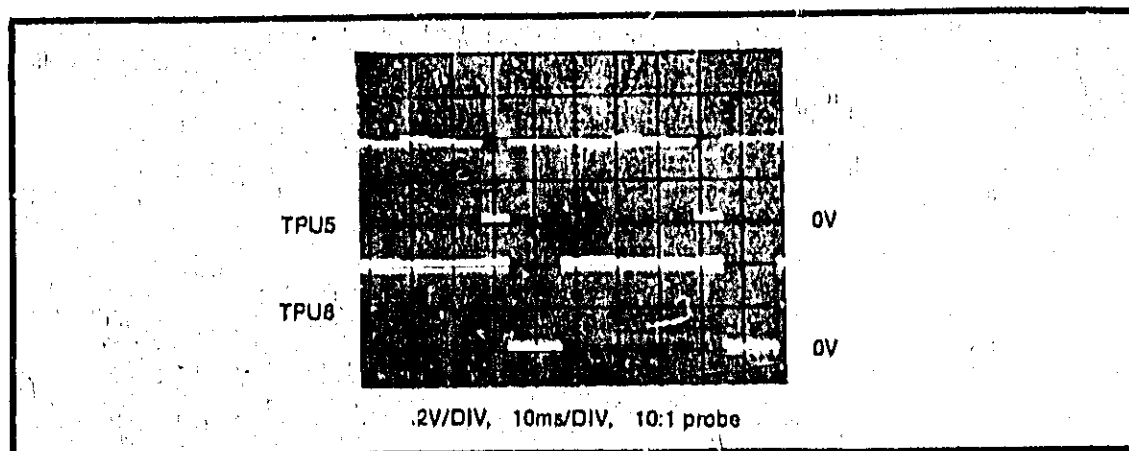


Figure 8-17. TPU5 and TPU8 Waveforms

NOTE

The reference designation "SW" is used for switches in the following information to match the labels on the board.

8-191. The 05355-60025 is an extender board that is primarily used for troubleshooting the A7 Microprocessor Assembly. Additionally, this board can be used to call up diagnostic routines and allow testing of other assemblies by using signature analysis. Specific uses of some of the components are as follows:

- a. SW1: Permits isolation of the three address lines and four select lines from the rest of the instrument.
- b. SW2: Performs the power-up reset function for the microprocessor.
- c. SW3: Used to call up certain diagnostic routines used in troubleshooting other assemblies. The switch settings are listed in the individual troubleshooting procedures. See paragraph 8-193 for a detailed description.
- d. SW4: Permits isolation of the 8-line data bus from the rest of the instrument.
- e. LEDs
D0
thru
D7: Provide a visual indication of results of the power-up diagnostic routines. These LEDs provide first-hand information in case a failure has made the 5345A display ineffective. These LEDs indicate the following conditions:
 - (1) D0 LED on: A7U10 RAM passed.
 - (2) D1 LED on: A7U12 RAM passed.
 - (3) D2 LED on: A7U5 ROM passed.
 - (4) D3 LED on: A7U8 ROM passed.
 - (5) D4 LED on: VCO passed at 885.2 MHz.
 - (6) D5 LED on: VCO passed at 970.8 MHz.
 - (7) D6 LED on: VCO passed at 1056 MHz.
 - (8) D7 LED off: 5345A is not in self-check. If the LED is on, the 5345A is in self-check and the VCO cannot be checked, i.e., D4, D5, and D6 will be off.

8-192. Decoder U1 controls the read/write function for other circuits on the board. Data can be written into latch U4 to light specific LEDs. When addressed to read, U1 enables U3 to output the settings of SW3 onto the Data bus. U2 and U5 decode the address lines to generate signals which bracket the addresses of each ROM. The signal at TPU5 is Low only when ROM A7U5 is enabled. Likewise, the signal at TPU8 is Low only when ROM A7U8 is enabled. If the A7 Microprocessor is put into freerun, the following signals should be observed at TPU5 and TPU8 (see Figure 8-17).

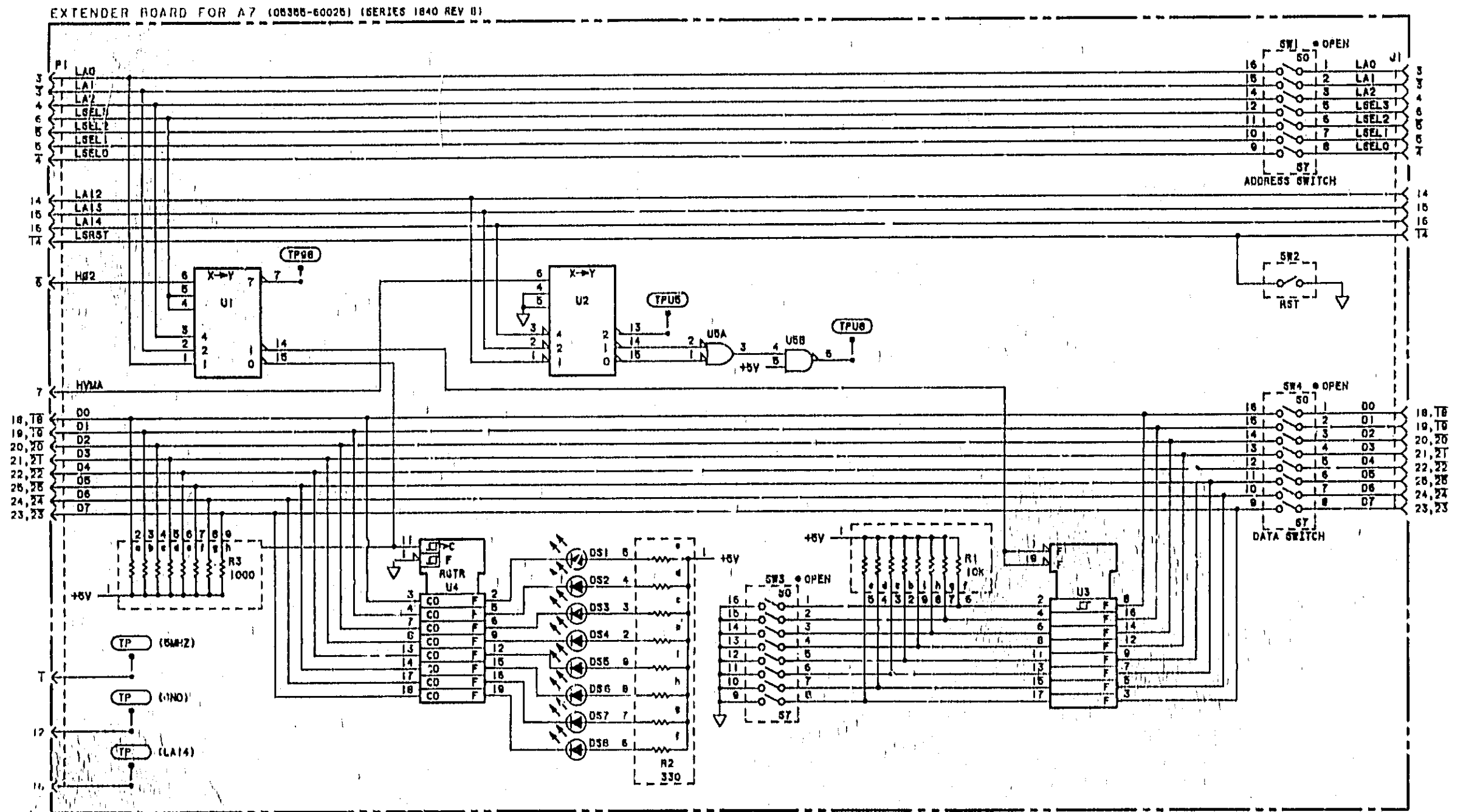


Figure 8-18. 05355-60025 Extender Board Schematic Diagram

B-193. Detailed Description of SW3 Usage (05355-60025 Board)

B-194. SW3 has eight sections (S0 through S7) which are used to call up certain diagnostic routines used in troubleshooting other assemblies. Shown below is a summary of the diagnostics and their application. Each troubleshooting procedure also lists the switch settings needed to apply the procedure.

NOTE

The normal position of SW3 switches is away from the dot that is marked on the switch. This position is the closed position. To enable a diagnostic, the switch is moved toward the dot. The switch position in use is the one activated closest to the bottom of SW3. Any other switches thrown toward the dot are "don't care" switches. This scheme is followed to allow easier activation of the individual switches on SW3. There is only one exception to this, and it will be pointed out in the discussion below.

SW3 switch sections usage:

- S0: This switch is used to activate a routine to allow signature analysis on the A8 HP-IB/Decoder board. The microprocessor repeatedly addresses U25, U22, and U24 so that these I.C.'s may be checked.
- S1: This switch is used to activate a routine to allow signature analysis on A8U10. Again, the microprocessor repeatedly addresses this IC so that the signature analyzer may be used.
- S2: This switch is used to activate a routine to allow signature analysis on A8, U15, 16, 17, 18, 19, and 21. The microprocessor repeatedly writes to U17, and then reads this from U21. The other IC's involved are gating used for decoding.
- S3: This switch is used to activate a routine to allow signature analysis on the A1 Front Panel assembly. The microprocessor repeatedly writes to registers U2 and U3, and then reads from U1. This is done at a rate to allow signature analysis.
- S4: This switch is used to activate a routine to allow signature analysis on the A9 Interface assembly. The IC's checked are U14 through U18. Sections of U6 and U7 are also checked. The microprocessor repeatedly addresses these IC's in a software loop to allow signature analysis.
- S5: This switch is involved in two tests, both of which do the same thing, except at different speeds. This is the only case where two switches are used in conjunction with each other, as explained in "b", below.
 - a. The first use of this switch is to call up a routine to allow signature analysis on A9, U11 and U13. Decimal point data is written into RAM U13, while a specific set of characters are written into U11, all at high speed to allow the use of the signature analyzer.
 - b. The second use of this switch is in combination with switch S0. When both of these switches are thrown, the same test as part A is generated, but at a much slower rate to allow human visual checks of the 5345A display. The procedure to use during this check is explained in the troubleshooting procedure.
- S6: This switch is used to activate a routine to allow signature analysis on the logic used on the A3 Filter Detector. The IC's checked are U2 and U3, when using the RF converter head input.
- S7: This switch is used to activate a routine to allow signature analysis on the same logic as for S6, but when using the Prescaler input.

8-195. TROUBLESHOOTING

8-196. Detailed troubleshooting procedures are provided in *Tables 8-10* through *8-21*, as described in paragraph 8-198. Prior to performing the detailed procedures, a preliminary power-up error code check should be performed, as follows:

- a. With the 5355A plugged into the 5345A, apply power and observe **both** front panels for the following error code indications on power-up.

(1) 5345A Display (ROM and VCO Test):

Code	Error in 5355A
----74----	A7U5 ROM parity error
----78----	A7U8 ROM parity error
----83----	VCO Failure, Low Range (885.2)
----86----	VCO Failure, Midrange (970.8)
----89----	VCO Failure High Range (1056)

(2) 5355A front panel error indicators (RAM test) are shown in *Figure 8-19*.

- b. If preliminary power up sequence passes, the diagnostic modes shown in *Table 8-9* may be used to isolate the area of failure. These diagnostics, combined with the overall procedures set forth in *Table 8-10* should allow the technician to rapidly reach the area of difficulty.
- c. A comprehensive visual inspection of the 5355A should be carried out **prior** to detailed troubleshooting. Power supply checks may be in order if indicated by burning odors, dim displays, or general lack of 5345A/5355A action.

5355A Error Indicators (RAM Test)

NOTE

When LISTENING LED flashes, a bad RAM is indicated as specified below:

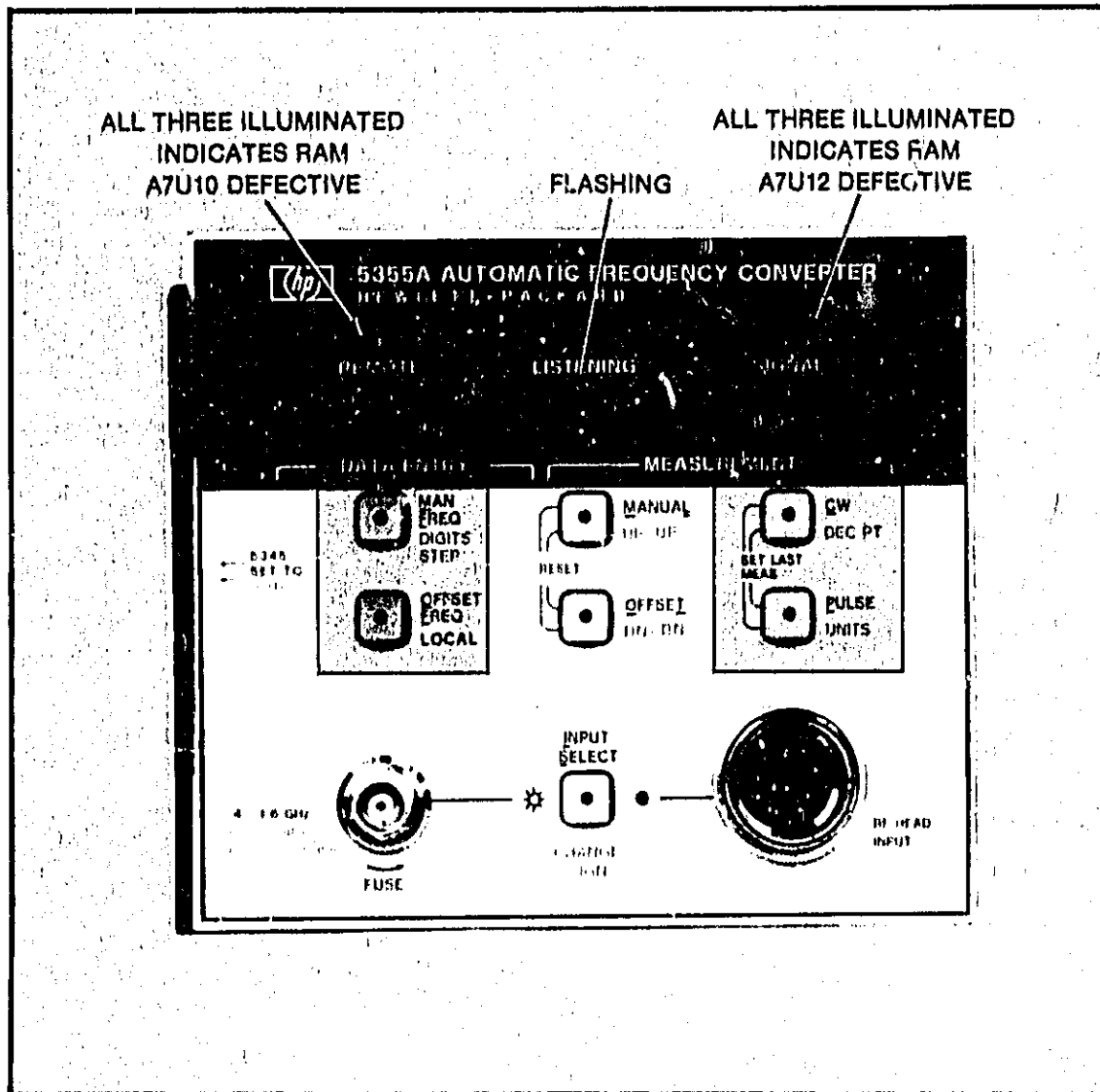


Figure 8-19. RAM Test Error Indicators

8-197. Detailed Operating Procedures for Table 8-9, Diagnostic Mode 09 (Synthesizer Frequency Set)

NOTE

Table 8-9, Diagnostic Modes For Troubleshooting, is self-explanatory except for Mode 09. To perform Mode 09 proceed as follows:

- a. From power up condition, press blue and gold keys simultaneously until 5345A displays `-----09-----`.
- b. Press blue key for offset DATA ENTRY. Key indicator will light. Display will be `-1. GHz`.
- c. Press INPUT SELECT/CHANGE SIGN key to turn off `'--'` sign.
- d. Set up the desired synthesizer frequency as an offset frequency. The units MHz or GHz are also required to be set.
- e. Press OFFSET key for off. Key light will go out.
- f. Press MANUAL measurement key to cause VCO to go to frequency commanded.

8-198. Troubleshooting Procedure

8-199. Troubleshooting procedures are given in *Table 8-10 through 8-21* as listed below. These procedures check the 5355A plugged into the 5345A mainframe and connected to the 5356A Frequency Converter Head.

8-200. These procedures are arranged to go from simple to more complex circuit assemblies, using the front panel indications. Thus, it is important to follow the procedures to ensure checking for all possible troubles.

8-201. *Table 8-10* provides an overall troubleshooting procedure using the power-up diagnostic and the keyboard check. The remaining tables check these modes or circuits:

- Table 8-11. Troubleshooting the Prescaler Input: CW Mode*
- Table 8-12. Troubleshooting the Prescaler Input: PRF Mode*
- Table 8-13. Troubleshooting the 5355A RF Head Input: MANUAL/CW Mode*
- Table 8-14. Troubleshooting the 5355A RF Head Input: AUTO/CW Mode*
- Table 8-15. Synthesizer Loop Troubleshooting*
- Table 8-16. A1 Front Panel Troubleshooting*
- Table 8-17. A8 Decoder/HP-IB Troubleshooting*
- Table 8-18. A7 Microprocessor Troubleshooting*
- Table 8-19. A9 Interface Troubleshooting*
- Table 8-20. A3 Filter/Detector Troubleshooting*
- Table 8-21. Frequency Converter Head Troubleshooting*

NOTE

If the 5355A or the 5356 is returned for repair, calibration or certification, both of these instruments should be returned together.

Table 8-9. Diagnostic Modes for Troubleshooting

NOTE

IN LOCAL operation the diagnostic modes listed below are obtained in numerical sequence by pressing the gold MAN FREQ and blue OFFSET FREQ keys simultaneously. Observe the display for the mode number listed below to determine the diagnostic mode of the 5355A each time the keys are pressed. If diagnostic mode (1-10) is started in one column, the sequence will stay in that column. Press reset on 5345A and set desired operational mode on 5355A to restart sequence. In REMOTE operation, the diagnostic modes are programmed by use of the codes shown in Table 3-9. Once the diagnostic routine is entered in one column (1 through 4), the routine cannot jump to a different column. To change columns, the 5345A reset button must be pressed and the 5355A placed in the operational mode desired.

MODE 1 second display each time Gold and Blue key is pressed	0.4—1.6 GHz INPUT		RF HEAD INPUT	
	Column 1 CW	Column 2 PULSE	Column 3 CW	Column 4 PULSE
DIAGNOSTIC MODES				
====0====	Displays 885.2 MHz self-check frequency (synthesizer set to 1 GHz).		Displays synthesizer frequency to 100 kHz resolution.	
====02====	NA	Displays ratio of measured pulse width to reference pulse width.	Displays calculated N number. Ignore annunciator and round to nearest integer. (-) sign means add IF.	
====03====	NA	• Displays reference pulse width, †	Displays (A-B) counts from synthesizer during N determination.	Displays calibration factor. Ignore annunciator.
====04====	NA	• Displays measured pulse width,	Displays (A-B) counts from IF during N determination.	Displays ratio of measured pulse width to reference pulse width.
====05====	Displays prescaler frequency; i.e., input frequency divided by 8.		Displays IF frequency.	• Displays measured pulse width.
====06====	NA	Displays calibration factor. Ignore annunciator.	NA	• Displays reference pulse width, †
====07====		NA	NA	Displays IF, during N determination.
====08====		NA	NA	Displays IF ₃ during N determination.
====09====		NA	Manual mode frequency measurements with synthesizer set to frequency entered in offset mode. (See paragraph 8-197 for detailed operating procedures.)	
====10====		NA	Displays IF frequency produced by synthesizer set to frequency entered in offset mode.	

NOTES:

† Reference pulse width is measured during calibration only.

• Pulse width measurements are displayed by annunciators equivalent to time, as follows:

Display	Time
kHz	ns
MHz	μs
GHz	ms

Table 8-10. Overall Troubleshooting Procedure

5345A Setup:

FUNCTION to PLUG-IN
GATE TIME to 1 ms
Input Amplifier switch to SEP

5355A Setup:

Connect 5356A Frequency Converter Head to plug-in but do not apply signal to the head.

1. **POWER UP DIAGNOSTIC** — Turn 5345A POWER switch to ON position. All front panel lights of plug-in should light momentarily. The 5345A display will lamp test briefly and then display the code of the attached converter head, as shown in table below.

Converter Head	Code No.
5356A	0
5356A Option 001	0
5356B	1
5356B Option 001	2
5356C	4
5356C Option 001	5

NOTE

If converter head is not attached, a code will not be displayed and the 5355A will power-up with the INPUT SELECT light on (PRESCALER mode). See paragraph 8-196 for error indications.

- a. If the 5355A powered up properly, go to Step 2. If not, troubleshoot, in order, the A7 MPU (Table 8-18), A8 Decoder/HP-IB (Table 8-17), A1 Front Panel (Table 8-16), and A9 Interface (Table 8-19).
- b. The power-up sequence exercises the synthesizer at three different frequencies: 885.2, 970.8, and 1056 MHz. Check A4, A5, A14, and A10 (Table 8-15). Additionally, A11 acts to pass the synthesizer output to the 5345A. Check A11 (Tables 8-11, 8-12, and 8-14). For further information, see Table 8-18, step 2.
2. **KEYBOARD CHECK** — Perform the keyboard check outlined in Table 3-7. If the 5355A operates properly, go to Step 3. If not, troubleshoot the A8 Decoder/HP-IB (Table 8-17), A1 Front Panel (Table 8-16), and A9 Interface (Table 8-19) assemblies in that order.
3. **PRESCALER INPUT: CW MODE** — Select the PRESCALER mode of operation by pushing the  key. Inject a .4 to 1.6 GHz CW signal into the prescaler input (front panel BNC). See Table 7-1 for the proper level. If the counter displays a correct reading of the input frequency, go to Step 4. If not, go to Table 8-11.
4. **PRESCALER INPUT: PRF MODE** — Connect a BNC cable (supplied) from the rear panel GATE jack of the 5355A to the rear panel GATE CONTROL INPUT jack of the 5345A.
 - a. Pulse modulate the signal source to give bursts of RF. (If using an 8620C Sweep Oscillator, set its rear panel switch to give 1 kHz square wave modulation. Signal light will come on.)
 - b. With the plug-in still set to CW, the 5345A should not take a measurement. If it does measure the signal, go to Table 8-12. (Be sure the signal is pulsed RF and not CW.)
 - c. Push the  key. If the counter displays a correct reading, go to Step 5. If not, go to Table 8-12.

Table 8-10. Overall Troubleshooting Procedure (Continued)

5. FREQUENCY CONVERTER HEAD INPUT: MANUAL/CW MODE — Select this mode of operation by pushing



and



keys. Input Select light should be out. A 5356 converter head must be connected

to the 5355.

- Enter the desired manual center frequency, for example, 1.9 GHz; and then push  key (see Section III for keyboard explanation).
- Inject a CW signal through the 5356 that is within 50 MHz of the frequency just set with the keyboard. See Table 1-7 for the proper level.
- If the counter displays a correct reading of the input frequency, go to Step 6. If not, perform the troubleshooting procedure in Table 8-12.

6. FREQUENCY CONVERTER HEAD INPUT: AUTO/CW MODE — Select this mode of operation by pushing



the  key (light within key should go out). If the counter displays a correct reading of this and other selected frequencies within the measurement range, go to Step 7. If not, go to Table 8-14.

7. FREQUENCY CONVERTER HEAD INPUT: AUTO/PRF MODE — Pulse modulate the signal source to give bursts of RF. (Use a pulse generator and 11720A Pulse Modulator; or if using an 8620C Sweep Oscillator, set its rear panel switch to give 1 kHz square wave modulation). With the plug-in still set to CW, the 5345A should not take a measurement. (Signal light will come on. Be sure the signal is pulsed RF and not CW.)

- If the 5345A does measure the signal, go to Table 8-20, step 1.
- If the 5345A does not measure the signal, go to Table 8-20, Step 2.

8. HP-IB OPERATION

- Perform all steps in this table prior to this step to ensure proper operation. This is important because the HP-IB operation is implemented by many circuit elements contained on several boards and many of these are tested in prior tests.
- Perform the HP-IB Verification Program as shown in Section IV. If this program performs properly, the HP-IB operation can be considered correct. If the program does not perform properly, proceed to Table 8-17, Part II.

9. ASSEMBLY NUMBER VERSUS TROUBLESHOOTING TABLE NUMBER.

Assembly No.	Table No.	Assembly No.	Table No.
A1	8-16	A8	8-17
A2	8-13, 8-20	A9	8-19
A3	8-11, 8-12, 8-13, 8-20	A10	8-15
A4	8-15	A11	8-11, 8-12, 8-14
A5	8-15	A12	8-17
A6	8-11, 8-12	A13	None
A7	8-18	A14	8-15
		5356	8-13, 8-14, 8-21

Table 8-11 Troubleshooting the Prescaler Input: CW Mode

1. Verify A6 Prescaler operation and associated signals by checking the following points. Place A6 on extender 05355-60020. Apply 800 MHz at zero dBm to A-1.6 GHz Input.
 - a. A6(2): TTL Low. If High, check A8U10.
 - b. A6(1): TTL, pulsing (60 μ s). If not, check A8U10.
 - c. Check center pin of A3J2 with oscilloscope; should be prescaler input signal +8. If not, check front panel input fuse and then troubleshoot A6 Prescaler. A3J2 can be reached at top center edge of A3 board. If no signal is present, three possible problems exist:
 - (1) The AGC loop is faulty, not allowing any signals to pass through U9 attenuator. Resolve by proceeding to Step d. If OK, return here.
 - (2) High frequency IC's U8, U7 or U6 have failed. Resolve by proceeding to Step f.
 - (3) Binary bias circuit U4, arming circuit Q1 or hysteresis adjustment R44 is not set properly or has failed.

CAUTION

Do not use continuity tester to check fuse. Use an ohmmeter on a scale that provides less than 100 mA to prevent blowing the fuse.

- d. A6(7): TTL Low. Green LED dark. If Low, ensure that A8U13 can pass the level to the microprocessor. (This step can be postponed with the idea that the problem can be found in the remaining portion of this procedure. If a definite fault is not located, be sure to check A8U13.) If High, troubleshoot the A6 Prescaler.
 - (1) Check U2 thus: TP2 should be approximately 12-13 volts with no signal applied, causing A6(7) to be low. If this voltage is present and A6(7) is high, check adjustment effect of R8. Replace U2. Check associated parts.
 - (2) If TP2 is not 12-13 volts, check entire AGC loop (U3, U5, Q2, Q3, Q4) using dc voltages shown in the table below. Apply signal levels and check those points shown in the table.

NOTE

The junction of CR9, C34, and U5(3) is a very high impedance point and cannot be voltage checked. To do so, even with a high z input meter, will load the circuit and give false readings. Check level at TP3 and U5(6) to determine possible failure of CR9, C34, and U5.

- (3) Check other circuit sections using dc voltage table.
- (4) Replace faulty components and readjust AGC bias (R42) per paragraph 5-30.

AGC LOOP VOLTAGES VS RF INPUT LEVEL

Conditions: RF Input — 800 MHz CW
RF level as indicated in table
A6 board installed on 05355-60020 extender

Check Point	RF Input level			
	0 dBm	-10 dBm	-20 dBm	-30 dBm
Q4 BASE	-.05	-.06	-.08	-.12
Q3-Q4 EMITTER	-.78	-.78	-.80	-.85
Q3 COLL/Q2 BASE	3.8	3.7	3.4	2.4
TP3	3.07	2.99	2.7	1.7
U5(6)	2.8	2.77	2.48	1.46
U3(2)	2.8	2.84	2.84	2.27
U3(6)	2.7	3.83	8.08	14.0
TP2/U9(1)	2.67	3.69	7.55	12.8

Table 8-11. Troubleshooting the Prescaler Input: CW Mode (Continued)

- e. A6(T2): TTL Low. If not troubleshoot A6,
 - (1) Check dc voltages around U1.
 - (2) Check effectiveness of R6 "PR5 GATE".
 - (3) Replace U1 and/or associated components as required.
- f. High frequency circuit checks. Proceed as follows to check overall circuit gains:
 - (1) Set up spectrum analyzer with 20:1 resistive probe (HP 10020A or equivalent).

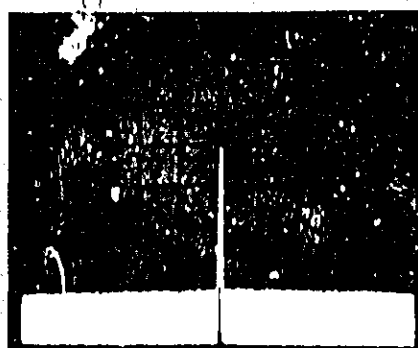
NOTE

The spectrum analyzer is being used in these checks as a sensitive power meter. The 20:1 resistive probe prevents circuit loading.

- (2) Set AGC LEVEL (R5) maximum clockwise. This locks out the AGC circuit and allows U9 attenuator to run wide open (no attenuation).
- (3) Connect signal source to J1 (or through the front panel connector) and set at 500 MHz.
- (4) Set signal level to read -30 dB on spectrum analyzer, as shown below: (See POINT A in block diagram in next step.)

8565A SETTINGS

Resolution Bandwidth: 1 MHz
Ref Level: 0 dBm
Input Atten: 10 dB
Scale: 10 dB/div
Freq Span/div: 50 MHz
Input Probe: 20:1 resistive divider



600 MHz SIGNAL

SIGNAL AS VIEWED AT POINT A IN BLOCK DIAGRAM

Hint: Probing must be done from rear of board. Use ground probe adapter on resistive divider probe. Use care in probing around chip capacitors as they crack easily.

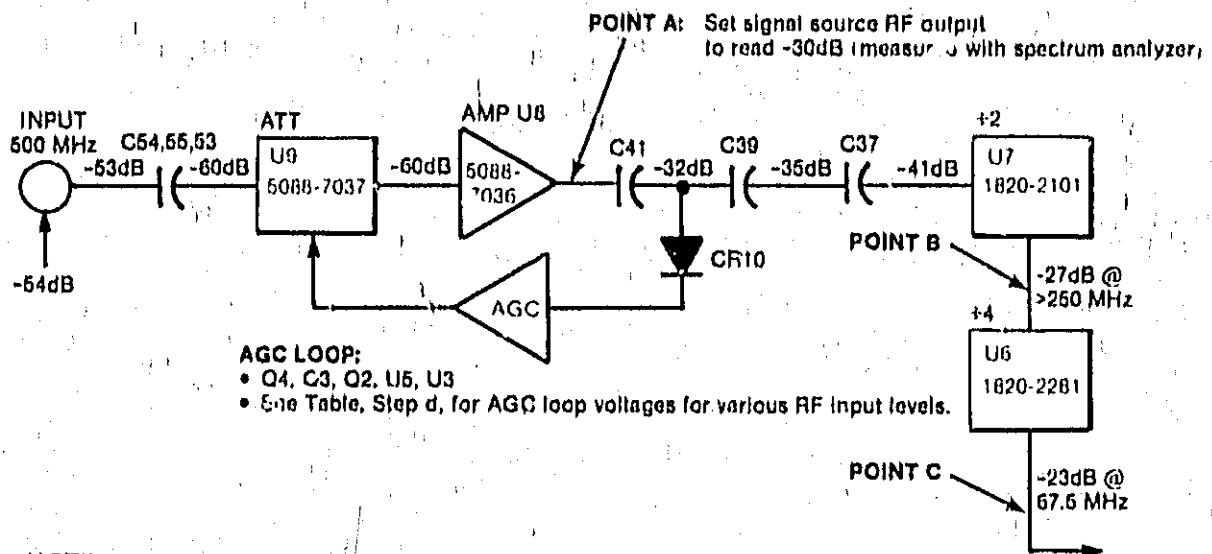
NOTE

This -30 dB setting is not meant to be -30 dBm. The 20:1 resistive probe does not present a 50-ohm load to the circuit, so accurate power measurements in dBm are not possible. This point is merely a reference for other measurements. Approximate input power (for information) is -27 dBm.

Table 8-11. Troubleshooting the Prescaler Input: CW Mode (Continued)

(5) Check the circuit levels as shown in Input Circuit block Diagram below.

A6 INPUT CIRCUIT BLOCK DIAGRAM:



NOTE

- See Schematic for DC Voltage Table and Component Locator.

The values shown in block diagram may vary by ± 3 dB. The circuit levels shown are referenced to the level set in step (4). See photos.

SIGNAL AS VIEWED AT POINT B, BLOCK DIAGRAM

5355A SETTINGS
Resolution Bandwidth: 1 MHz
Ref Level: 0 dBm
Input Attent: 10 dB
Scale: 10 dB/div
Freq Span/div: 50 MHz
Input Probe: 20:1 resistive divider

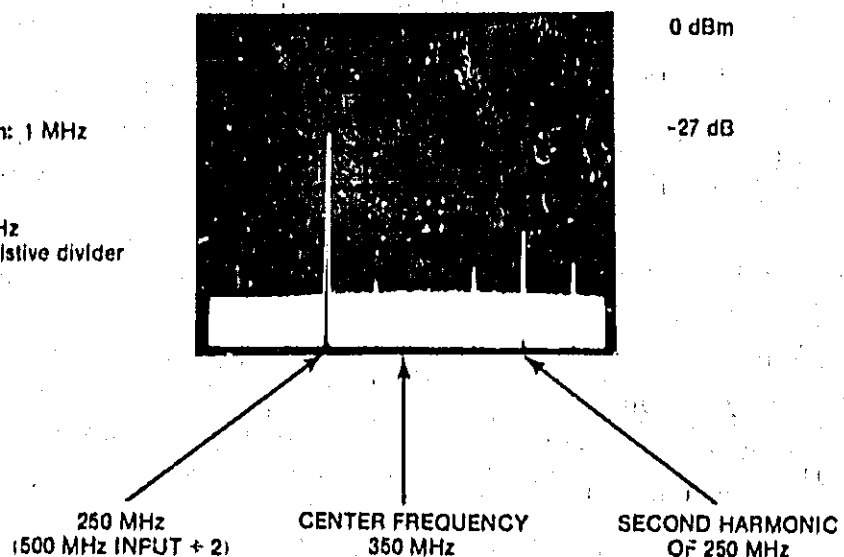


Table 8-11. Troubleshooting the Prescaler Input: CW Mode (Continued)

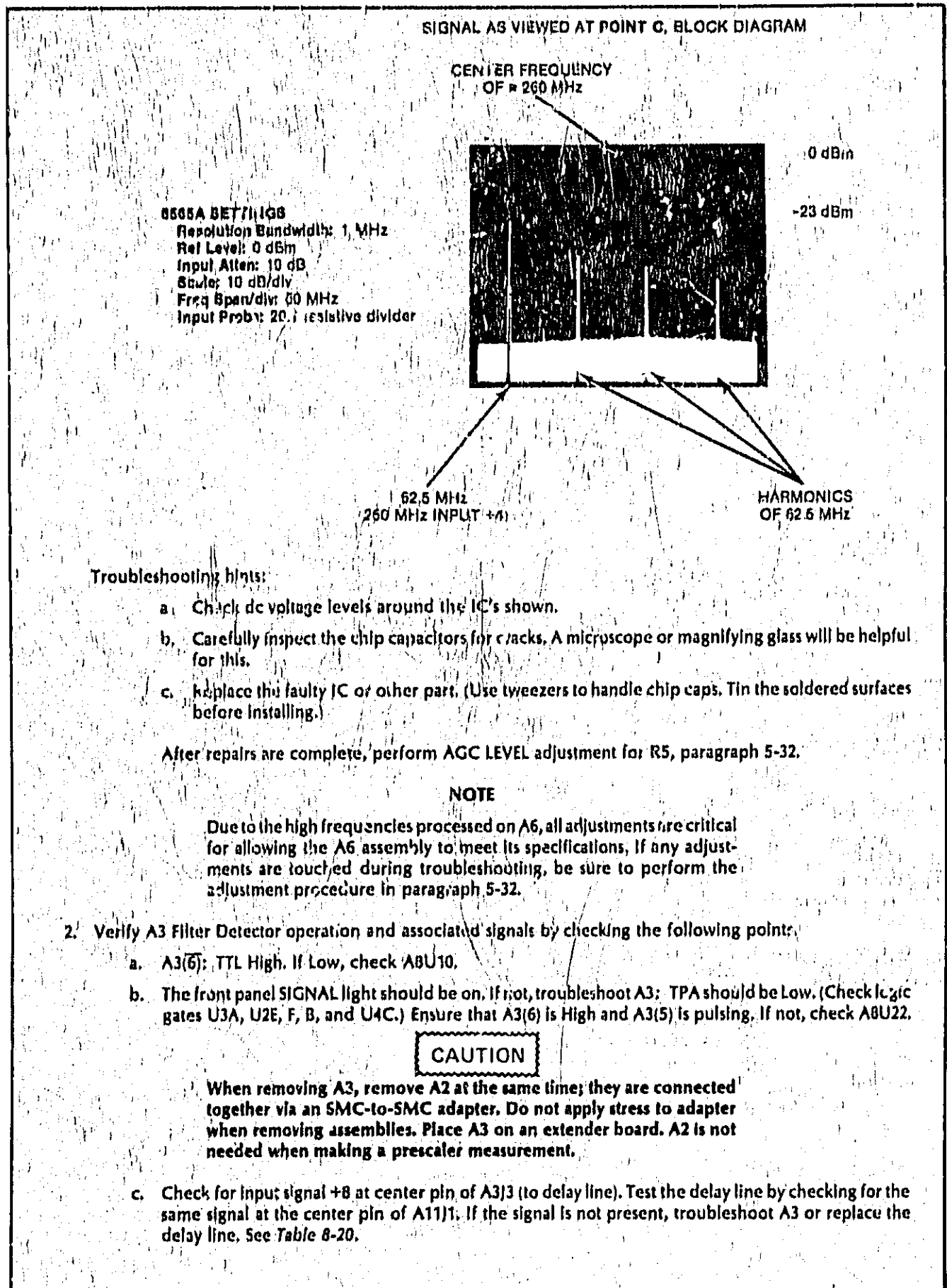


Table 8-11. Troubleshooting the Prescaler Input: CW Mode (Continued)

CW A11

3. Verify A11 Signal Switch operation and associated signals by checking the following points:
 - a. A11(2): TTL High. If Low, check A8U10. Should go low when RF HEAD INPUT is selected.
 - b. A11(9): TTL Low. If High, ensure that A10U5 has been reset; A10(3) must pulse High. If not, check A8U25.
 - c. A11(11): TTL High. If Low, check static levels of A10U6, U9; and U12.
 - d. A11(7): TTL High. If Low, problem is on A9.
 - e. A11 Output Signals: Check for Input signal +8 at center pin of A11J4 (CH A) and at rear panel IF OUT Jack.
 - f. See Table 8-12 for more information.

NOTE

Replace SMC-to-SMC adapter between A3 and A2 when finished.

Table 8-12. Troubleshooting the Prescaler Input: PRF Mode

1. Verify the A6 Prescaler operation and associated signals by checking the following points. Place A6 on extender 05355-60020.
 - a. Apply a pulsed RF Input to the .4-1.6 GHz Jack and place the 5355A in pulse measurement mode.
Hint: Using an 8620C sweeper, switch on 1 kHz square wave modulation (on rear panel of 8620C) to obtain a pulsed signal for testing.

NOTE

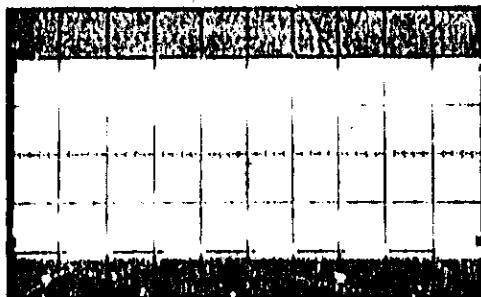
The 5355A will respond if in CW measurement mode during a pulse input. However, the displayed frequency will not be correct. Place the 5355A into pulse mode.

- b. A6(2): TTL High. If Low, check A8U10.
- c. A6(1): TTL Low. If High, check A8U10.

PRF A6

Table 8-12. Troubleshooting the Prescaler Input: PRF Mode (Continued)

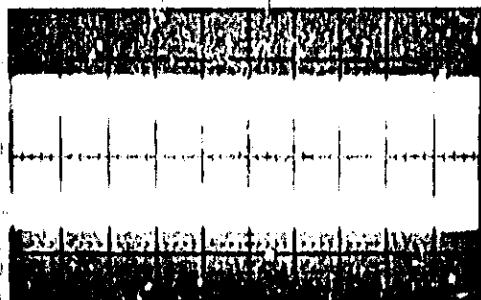
- d. Check the output signal of prescaler at A6(T0) with an oscilloscope (275 MHz bandwidth). Ideally, this signal should appear like bursts of RF. However, the prescaler is set to maximum sensitivity and oscillates between bursts. This does not effect the measurement because the gate signal occurs only during the burst. The following waveforms show the prescaler output under different input conditions. Check the output at different input frequencies, since the signal will look like CW if the prescaler output signal and the oscillation are at the same frequency. Refer to Table 8-11, step c.



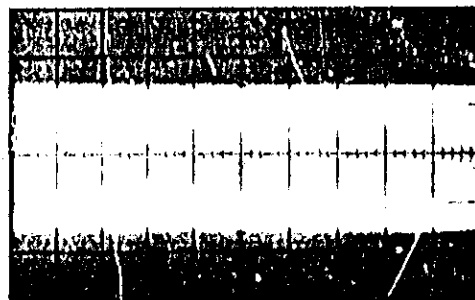
NO PRESCALER INPUT



INPUT FREQ. NEAR OSCILLATION



PRF JUST VISIBLE



HIGHER END OF BAND

*NOTE: These waveforms will vary depending upon frequency applied.

- e. A6(T1): TTL Low. If not, troubleshoot A6. Refer to Table 8-11, step d.
- f. A6(T2): TTL Pulsing. If not, troubleshoot IC U1, thus:
 - (1) Monitor action of U1 at TP1. PRF of signal = PRF of input RF pulse.
 - (2) Check dc levels at TP3. Voltage at TP3 must go more positive than the level at U1 (3) for U1 comparator to change states.
 - (3) Replace U1 and/or associated components.

2. Verify A3 Filter Detector operation and associated signals by checking the following points:

- a. The front panel SIGNAL light should be ON. If not, troubleshoot A3: TPA and TPB should be pulsing with A3(11) gate signal. As A3(11) goes Low, TPB goes High. (Check logic gates U3A, U2E, F, B, A, and U4C. Ensure that buffers U2A and B can output to the bus.)

CAUTION

When removing A3, remove A2 at the same time; they are connected together via an SMC-to-SMC adapter. Do not apply stress to adapter when removing assemblies. Place A3 on an extender board. A2 is not needed when making a prescaler measurement.

- b. Using an oscilloscope, check for pulsing signal (~0 to -1V) at the rear panel GATE OUT jack. This is the detected pulsed RF signal that is used to gate the counter. If this signal is not present, check A3Q3 through Q7 and A3U4A and B. See Table 8-13 for more information.

Table 8-12. Troubleshooting the Prescaler Input: PRF Mode (Continued)

3. Verify A11 Signal Switch operation and associated logic by checking the following points:
 - a. Connect alligator to BNC clip leads to one end of a BNC cable and connect the clip leads to A11TP6 and common (⏏). Connect other end of BNC cable to the Channel A jack of the 5345A.
 - (1) Set the counter controls to FREQ A, 1 ms, LEVEL to PRESET, X1, AC, SEP.
 - (2) The counter should measure the VCO frequency divided by four exactly 221,300 MHz. If not, check the signal coming into the board at A11(15) in the same manner.
 - (3) If the signal is not present there or if it is the wrong frequency, return the FUNCTION switch to PLUG-IN and perform the troubleshooting in Table 8-75 (leave the cable connected).
 - b. A11(2 and 1): TTL Pulsing, Explanation: Since the Prescaler worked properly in the CW mode, the IF path into Channel A (U4, CR3, CR5, CR1, U3, and U1) is probably good. (U1 may not respond to a different enable.) In the pulsed RF mode, this board helps perform two other functions.
 - (1) It is used in calibrating out errors in the 5345A gating by gating the known LO/4 signal (221.3 MHz) to the counter and then noting what the counter actually measured. Any difference is used as a calibration factor.
 - (2) The plug-in monitors any change in the width of the input burst by gating the LO/4 signal by the signal to both A and B channels and performing a T.I. holdoff measurement (see A11 theory).
 - c. If A11 pins 1 and 2 do not pulse, it may be that the program stopped because the counter did not receive a Channel B signal from the plug-in. If this is true, the program will stop so that both A11(1 and 2) will be Low. In this case, A11TP7 should be EECL High (H = 0V, L = -0.6V) so the LO/4 signal can pass through both multiplexers.
 - d. The following table is provided to help determine if the board is good, should the enable lines be in some other state.

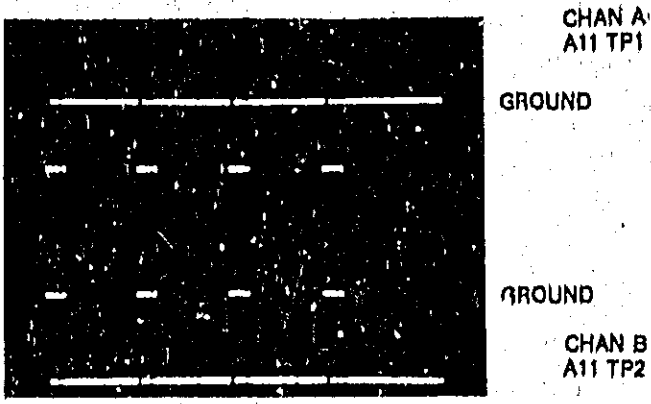
A11 Signal Switch Checks

A11(2) LLO/IF	A11(9) A/B GATE	A11(11) A/B SWITCH	A11(1) PI FUNC A	COMMENTS
H	L	H	H	Prescaler: CW Mode — Passes IF signal to Channel A for measurement.
L	L	H	H	Prescaler: PRF Mode — Passes LO/4 signal to Channel A for calibration.
H	L	H	H	Passes IF signal to Channel A for measurement.
L	L	H	L	Passes LO/4 signal to both channels for pulse width check.
H	L	H	H	Head: MANUAL/CW Mode — Passes IF signal to Channel A for measurement.
L	L*	H	H	Head: AUTO/CW Mode — Passes LO/4 signal to Channel A when LO is LO+2 MHz.
L	L*	L	H	Passes LO/4 signal to Channel B when LO is LO-2 MHz.
H	L*	H	H	Passes IF signal to Channel A when LO is LO+2 MHz.
H	L*	L	H	Passes IF signal to Channel B when LO is LO-2 MHz. (The above is the PRSQ routine for N determination.)
H	L	H	H	Passes IF signal to Channel A for measurement.
H	L	H	H	Head: AUTO/PRF Mode — Passes IF signal to Channel A once for LO and once for LO+4 MHz for N determination.
L	L	H	H	Passes LO+4 MHz/4 signal to Channel A for calibration.
H	L	H	H	Passes IF signal to Channel A for measurement.
L	L	H	L	Passes LO/4 signal to both channels for pulse width check.

*NOTE: Will change state to stop gating as A/B Switch changes state. This is part of the pseudorandom sequence.

Table 8-12. Troubleshooting the Prescaler Input: PRF Model (Continued)

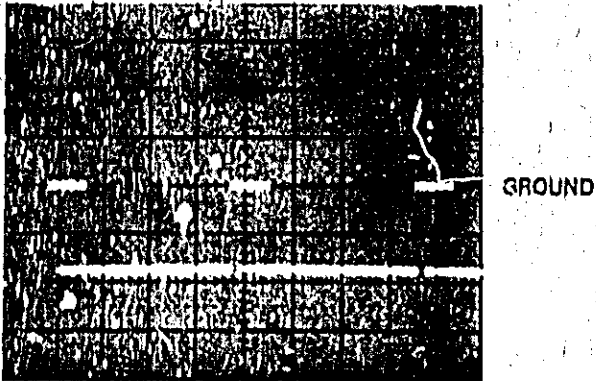
e. Troubleshoot A11 using photos below and dc voltages shown on A11 schematic.



Vert: A and B .05V/div, X10 probe in use, dc coupled
Horiz: .2 ns/div

NOTE

TP1 and 2 are only active (pulsing) during N determination, in response to the pseudorandom sequence (PRSQ) causing A/B switch to be active.



Vert: .05V/div, X10 probe in use, dc coupled
Horiz: 1 ns/div

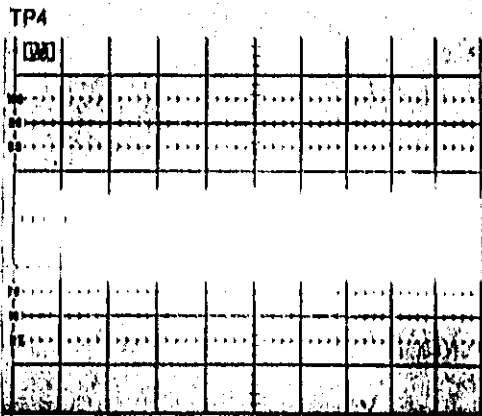
NOTE

This signal is in response to A/B gate, and serves to enable U3 limiter/amp.

Table B-12. Troubleshooting the Prescaler Input: PRF Model (Continued)

NOTE

The Low CH A and CH B signal at TP7 is the enable signal to MUX U1 and U2 only when the 5345A is in PLUG-IN function. TP7 is at -.7V (EECL low). At other 5345A function positions, this test point is at 0V (EECL high), which disables U1 and U2.



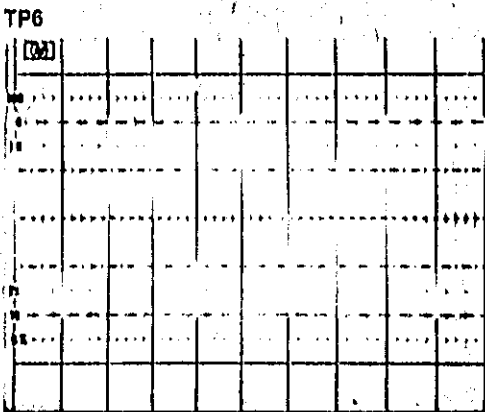
Vert: .05V/div, X10 probe, dc coupled
Horiz: .02 μs/div

NOTE

Photo was taken with RF signal applied to 5356 Head, Input 4 GHz, level not critical (~-10 dBm), 5355A in manual mode, center frequency 4.0 GHz.

NOTE

Amplitude may vary widely from that shown on photo due to scope probe, exact input signal frequency, etc. Best use of this point is for checking presence of signal. TP5 is of similar usefulness and will display a signal similar to TP4.



Vert: .02V/div, X10 probe, ac coupled
Horiz: .1 μs/div

NOTE

This signal is the VCO output +4. The photo was taken with the 5355A in manual mode, center frequency of 1.6 GHz. 5356 head should be installed, no signal applied.

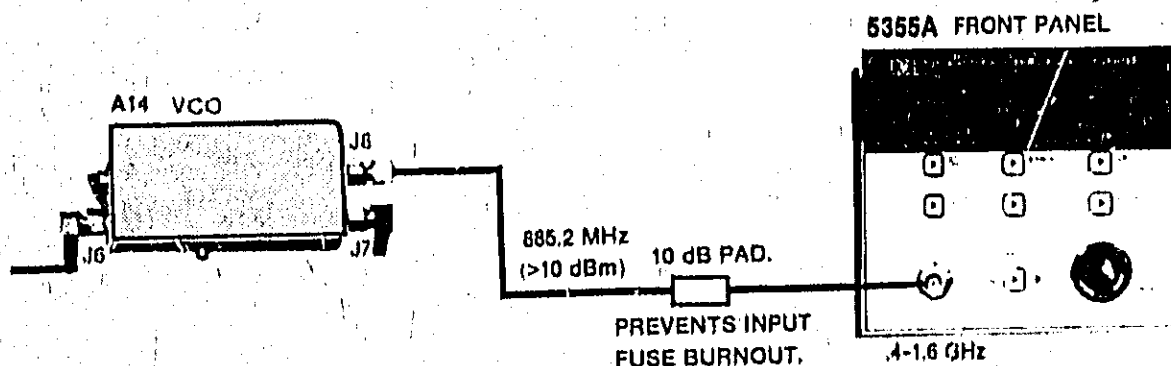
- f. If A11 seems to be working properly, the problem is in A8U10 or on the A9 board.

NOTE

When finished, replace SMC-to-SMC adapter between A2 and A3.

Table 8-13. Troubleshooting the 5355A RF Head Input: MANUAL/CW Mode

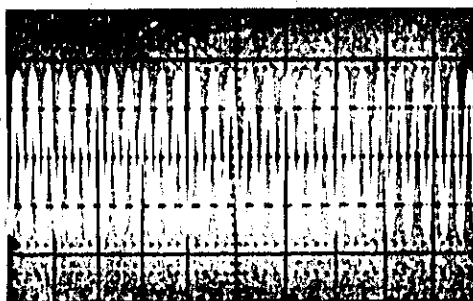
1. Verify if the failure is in the 5355A plug-in or the 5356 converter head, as follows:
 - a. If another 5355A or 5356 is available, swap units and repeat steps Steps 1 through 5 of Table 8-10. Troubleshoot the 5355A, using the steps shown in this table. Troubleshoot the 5356 using Table 8-21.
 - b. If no other 5355A or 5356 units are available, check the 5355A as described in Steps 2 and 3 of this table. If this check proves okay, check the 5356 per Table 8-21.
2. Verify that the VCO signal is being sent to the 5356 by performing a prescaler measurement of the VCO frequency at A14J8. Counter should read 885.2 MHz (power level is >10 dBm).



NOTE

If signal is not present, repair the A14 assembly. Refer to Table 8-15.
Otherwise, reconnect the cable to A14J8 and continue with step 3.

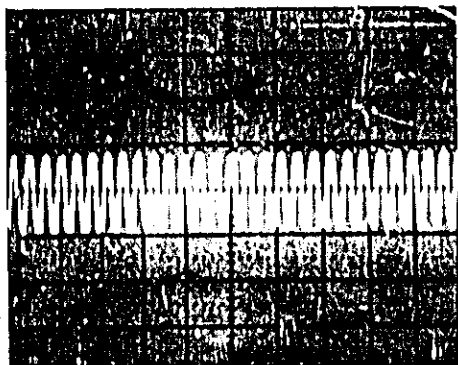
3. Select a 1.9 GHz manual center frequency (MCF) and then enter the MANUAL MEASUREMENT mode. A 5356 converter head must be installed to enable the manual measurement mode. Disconnect cable at A2J1 and inject an IF signal (CW) into A2J1: 160 to 325 MHz at -15 dBm. The displayed frequency should vary from about 1.952 GHz to about 1.787 GHz as the injected signal is changed from 160 to 325 MHz. Conclusions:
 - a. If the counter measures these frequency correctly but cannot measure the frequency under normal conditions at 1.9 GHz (MCF), the problem is in the 5356. See Table 8-21 for 5356 procedures.
 - b. If, under normal measurement conditions, the unit will not work at 1.9 GHz MCF but works properly at other manual center frequencies, the problem is probably in A4, A5, or possibly A14. See Table 8-15, Synthesizer Loop Troubleshooting.
 - c. If the counter fails the test outlined in Step 3a above, set the injected signal to 275 MHz and continue with Step 4.
4. Verify A2 IF Amp operation and associated signals by checking the following points with same setup.
 - a. A2(4): TTL High, if Low, check A3U10.
 - b. Using 275 MHz bandwidth oscilloscope, check for IF signal at center conductor of SMC-to-SMC adapter that is connected between A3 and A2. TPC is the same point. Set input to A2J1 at -15dBm for all signal checks that follow.



IF OUTPUT AT A2J2
.02V/div., 10 ns/div., ac, X10 probe

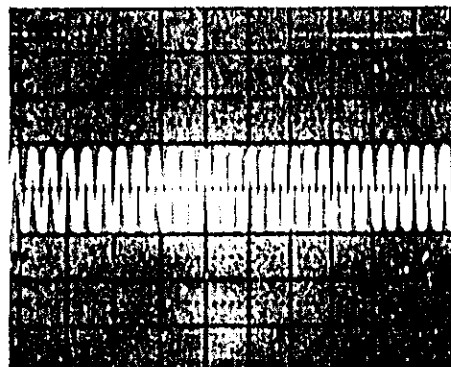
Table 8-13. Troubleshooting the 5355A RF Head Input: MANUAL/CW Mode (Continued)

- c. Using same setup, check TP8 and TPA for waveforms shown below (will be affected by scope cable movement):



TP8

Horiz: 10 ns/div.
Vert: .01V/div., X10 probe



TPA

Horiz: 10 ns/div.
Vert: .01V/div., X10 probe

If signal is not present, troubleshoot A2. Refer to dc voltage chart on A2 schematic. If signal is present, proceed to Step d.

- d. AGC CIRCUIT. To quickly check AGC action, observe voltage level at TPE. Set 5355A in PULSE mode and MANUAL measurement. Observe that:

DC voltage with -40 dBm applied to A2J1 is 10V.

DC voltage with -10 dBm applied to A2J1 is 2.1V, with a smooth change when varying the RF input.

If this does not occur, proceed with voltage checks, as follows:

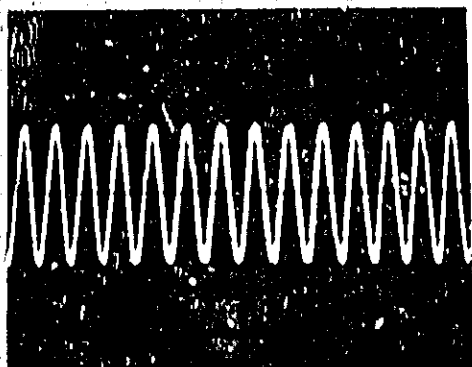
- (1) Apply the input signal as per Step 3, page 8-60. Observe RF level in voltage chart on A2 schematic.
- (2) Set the 5355A in PULSE mode, and MANUAL mode. Reason:
 - AGC circuit is active only in PULSE mode.
 - MANUAL mode stops the synthesizer sweep for quieter IF measurements.
- (3) Observe notes with readings on A2 schematic.
- (4) To check that PULSE mode has indeed enabled the AGC circuit, check that A2(4) is low.
- (5) When checking the "NO RF INPUT" dc voltages, short the input at A2J1 with a 50-ohm termination. This will further quiet the circuits, enabling steady dc voltage readings.
- (6) DC voltage checks may indicate some reading instability. Scope observations will indicate some noise on the signal. This is due to the A2 board being on its extender, thus losing good RF grounding. A heavy ground strap with clips, connected between A2 ground plane and the 5355A chassis may quiet the noise.

5. Verify A3 Filter Detector operation and associated circuits with the following procedure.

- a. Remove IF signal from A2J1 and reconnect original cable to A2J1.
- b. Disconnect adapter between A3 and A2 and place A3 on an extender board.
- c. Inject IF signal into A3J1: 275 MHz at 0 dBm.
- d. A3(6): TTL Low. If not, check A8U10.

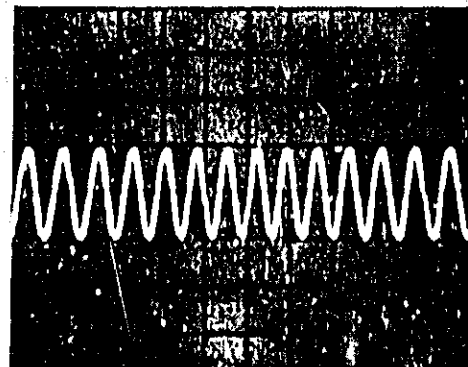
Table 8-13. Troubleshooting the 5355A RF Head Input: MANUAL/CW Mode (Continued)

- e. The front panel SIGNAL light should be steady state on. If not, troubleshoot the IF signal path on A3. Normal operation: TPA, B, F, G, H, and K, and should be TTL Low. TPC and J should be TTL High. Also check U2 output buffers. Use waveforms shown below and dc voltages on A3 schematic.



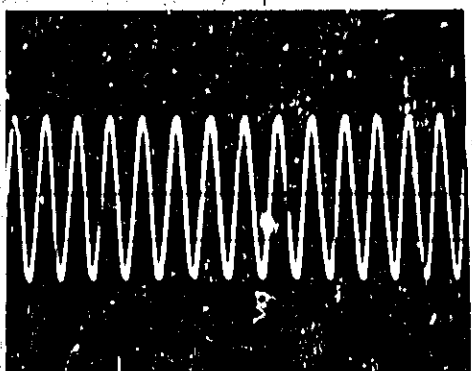
INPUT AT J1
0 dBm 275 MHz applied

Horiz: 5 ns/div. (use 50 ns/div. with X10 magnification of sweep)
Vert: .01V/div., X10 probe, dc coupled, high Z input



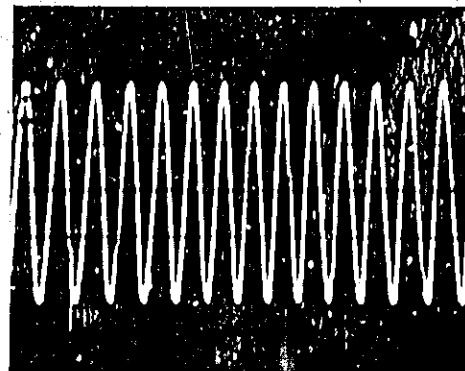
SIGNAL AT TPD

Horiz: 5 ns/div. (use 50 ns/div. with X10 magnification of sweep)
Vert: .02V/div., X10 probe, ac coupled, high Z input



SIGNAL AT TPI

Horiz: 5 ns/div. (use 50 ns/div. with X10 magnification of sweep)
Vert: .01V/div., X10 probe, dc coupled, high Z input



SIGNAL AT J3 — IF OUTPUT

Horiz: 5 ns/div. (use 50 ns/div. with X10 magnification of sweep)
Vert: .01V/div., X10 probe, dc coupled, high Z input

- f. Check for 275 MHz signal at center pin of A3J3 (to delay line). If the signal is not present, troubleshoot A3: U1, CR3-5, and K1.

NOTE

If any parts are replaced, check adjustment procedures, Section V.

6. Verify Synthesizer Loop operation by performing troubleshooting in Table 8-15.

Table 8-14. Troubleshooting the 5355A RF Head Input: AUTO/CW Mode

GENERAL. The main difference between this mode and the manual mode is the pseudorandom sequence the plug-in performs during the N determination routine. Another difference is that the synthesizer must sweep through all of its possible frequencies in order to find a harmonic that can mix with the input signal and provide an IF signal. This exercises the A4 +M circuits to a greater degree than in previous measurements.

1. Connect a 5356 RF converter head to the 5355A and apply an RF input. Place the A10 board on its extender. Verify A10PRSQ operation and associated circuits with the following procedure. The pseudorandom sequence is generated before each of the first three measurements and then before every 11th measurement. This will continue until the input frequency changes by 40 MHz or more, or is removed, or the 5345A "RESET" button is pressed. Therefore, after the initial measurements, it will take a few seconds for the readings to change. Pushing the 5345A RESET button or turning the RF input off and back on will reinitialize the sequence.

NOTE

5355A must acquire the signal (i.e., SIGNAL light on) before PRS will run.
If SIGNAL light is not on, check A3 troubleshooting (Table 8-20).

- a. A10(3): Normally TTL High, will pulse Low every time a PRS is generated. If not, check A8U25.
- b. Connect 5004A Signature Analyzer as follows:

START to TP3 (A10 pin 1)
STOP to TP3 (A10 pin 1)
CLOCK to TP7

- c. Set 5004A control as follows:

START to 
STOP to 
CLOCK to 

- d. For the short PRS, check for these signatures:

TP6 (A10 pin 18) — 24C3
A10(18) — 5U7A

NOTE

To set long PRS, press PULSE and CW pushbuttons at the same time.
To return to short PRS, press RESET on 5345A.

- e. For the long PRS, check for these signatures:

TP6 (A10 pin 18) — A867
A10(18) — 4475

If these signatures are not correct, troubleshoot A10, using signal tracing by using signatures in tables below. Waveform photos may also help in localizing the fault.

A10 Signature Analysis Table

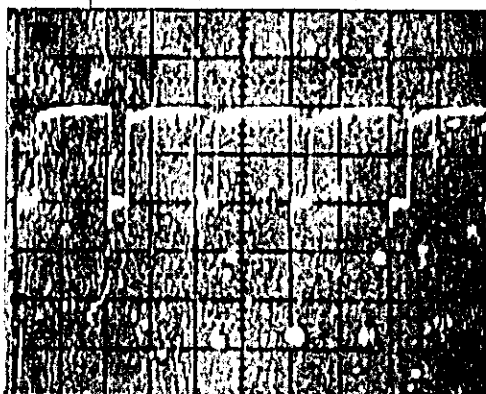
MAIN TEST POINTS	SHORT PRS	LONG PRS
TP1	0931	293H
TP2	6AC4	HP91
TP5	C67P	09U8

HEAD INPUT
AUTO/CW

Table B-14. Troubleshooting the 5355A RF Head Input: AUTO/CW Model (Continued)

Individual IC Signal Path Signatures Table

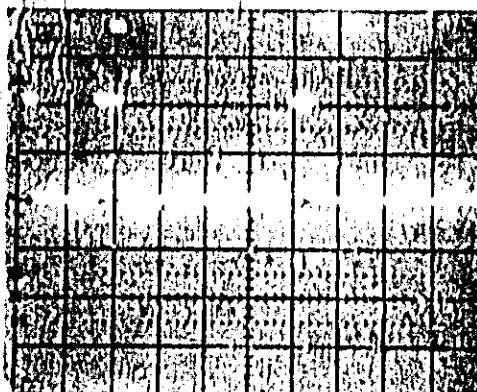
PIN NO.	SHORT PRS	LONG PRS	PIN NO.	SHORT PRS	LONG PRS
U1-8	13H9	UA55	U6-4	U879	7UOP
U1-9	3A02	H252	U6-5	C11U	2UF1
U1-11	3A02	H252	U6-9	HFFA	H769
U3-1, 2	H6FP	S109	U8-1	U879	7UOP
U3-5	4413	OAP7	U8-2 (or TP1)	0931	293H
U3-8	0931	293H	U8-5	U879	0000
U3-9 (or TP1)	U879	7UOP	U8-9 (or TP2)	6AC4	HP91
U3-12	4F4B	50UL			
U4-1, 2	92FH	A19U	U9A-3	1PF1	HP91
U4-3	528D	1P6A	U9B-6	6AC4	1F72
U4-4	2PA7	1695	U9C-9	U879	7UOP
U4-8	0931	293H			
U4-9	U879	7UOP	U10A-3	U879	7UOP
U4-13	H6FP	5109			
			U11A-2	U879	7UOP
U5-9	5U7A	4475	U11A-3	U879	7UOP
			U11C-8	U879	A19U
			U11C-11	92FH	7UOP



TP2: CLK
Vert: 2V/div, X10 probe, dc coupled
Horiz: 5 μ s/div

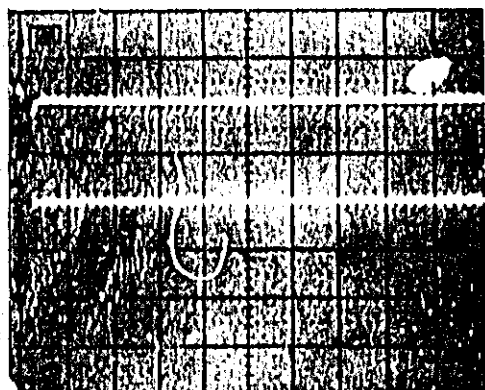


TP1: PRS clock-only visible during PRS generation
Vert: .2V/div, X10 probe, dc coupled
Horiz: 5 μ s/div

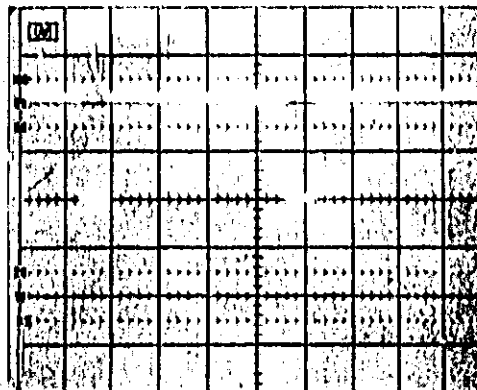


TP3: HSOBY (high sequence busy) — only visible during PRS generation
Vert: .2V/div, X10 probe, dc coupled
Horiz: .1 s/div

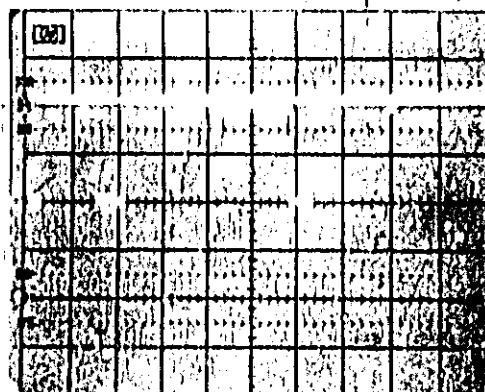
Table 8-14. Troubleshooting the 5355A RF Head Input: AUTO/CW Model (Continued)



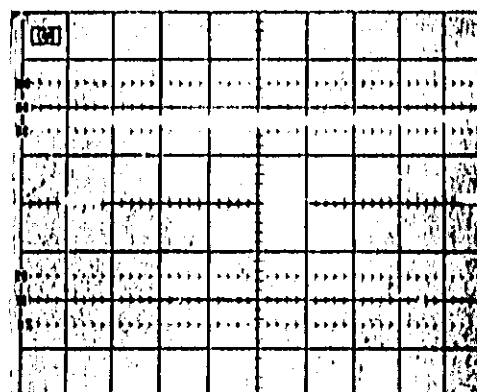
TP2: Only visible during PRS generation
Vert: .2V/div, X10 probe, dc coupled
Horiz: 5 μ s/div



TP4: Only visible during PRS generation
Vert: .2V/div, X10 probe, dc coupled
Horiz: .1 s/div



TP5: Dead time — only visible during PRS generation
Vert: .2V/div, X10 probe, dc coupled
Horiz: .1 s/div



TP6: A/B switch — only visible during PRS generation
Vert: .2V/div, X10 probe, dc coupled
Horiz: .1 s/div

- f. A10I1 should pulse High during the sequence (this will be OK if signatures are correct). Ensure that A8U13 can pass this level to the microprocessor.

2. Verify A4 +M operation by performing the test outlined in Step 4 of Table 8-15. If the test is positive, return to this point.
3. Verify A11 Signal Switch operation and associated circuits by checking the following points.
 - a. A11 pins 9 and 11: TTL pulsing. If not, check A10U5.
 - b. Check that TP1 and TP2 toggle at EECL levels (H=0V, L=-1.6V). If not check A11Q1 and A11Q3.
 - c. Set plug-in to prescaler mode and connect a CW signal to the front panel Jack (~1 GHz). Jumper A11TP1 to common (∇). Check for input signal +8 at center pin of A11J3 (CH B). If signal is not present, replace A11U2.
 - d. If the plug-in works properly at some frequencies but not others, it may be because of a problem or misadjustment in the voltage-variable filters (CR5-7) on A2 or because A3 is misadjusted.
 - e. If the previous steps have not located the problem, perform the adjustment procedure of A5 to ensure proper operation of the VCO drive during the pseudorandom sequence.

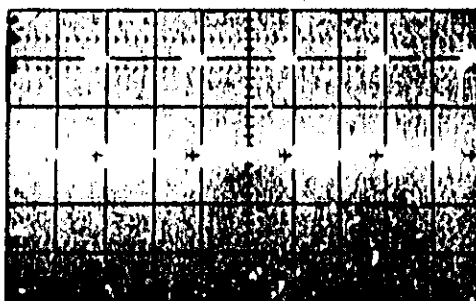
Table 8-15. Synthesizer Loop Troubleshooting

GENERAL. This procedure provides a comprehensive test of the synthesizer circuits: A4 Programmable +M, A5 DC Amp/Loop Comp, A10 +C, and A14 VCO. If the plug-in has passed the "Prescaler Input: PRF Mode" test but failed the "5355A RF Head Input: MANUAL/CW Mode" test, special concern should be given the data-loading circuits on the A4 board and the output of A14J8 (see Step 2d).

1. Verify the A10 +C circuit operation with the following procedure.

(Remove top and bottom covers.)

Use an oscilloscope to check for presence of 100 kHz reference signal (TTL levels) at A10TP9 (see waveform below). If signal is not present, check circuits of A10, U13, U14, U15 and U16 may be at fault.

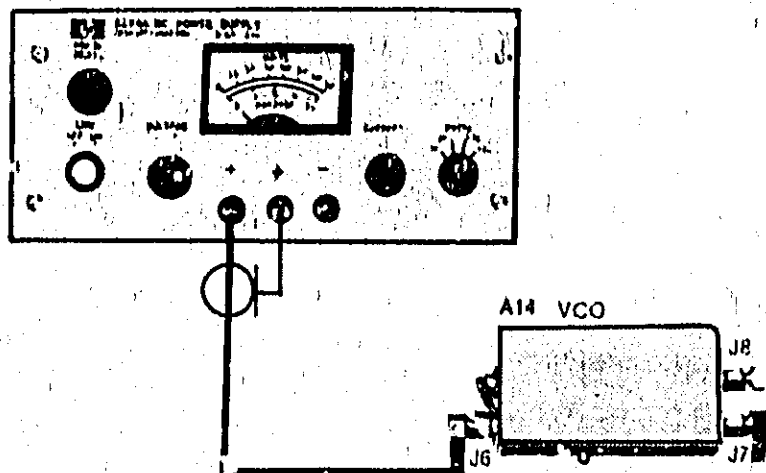


.2V/div., 5 ns/div., dc

2. Verify the A14 VCO and A4 +4 circuit operation with the following procedure.

- a. Disconnect the dc control line of the VCO at A14J6 and connect a dc power supply to A14J6 as shown below:

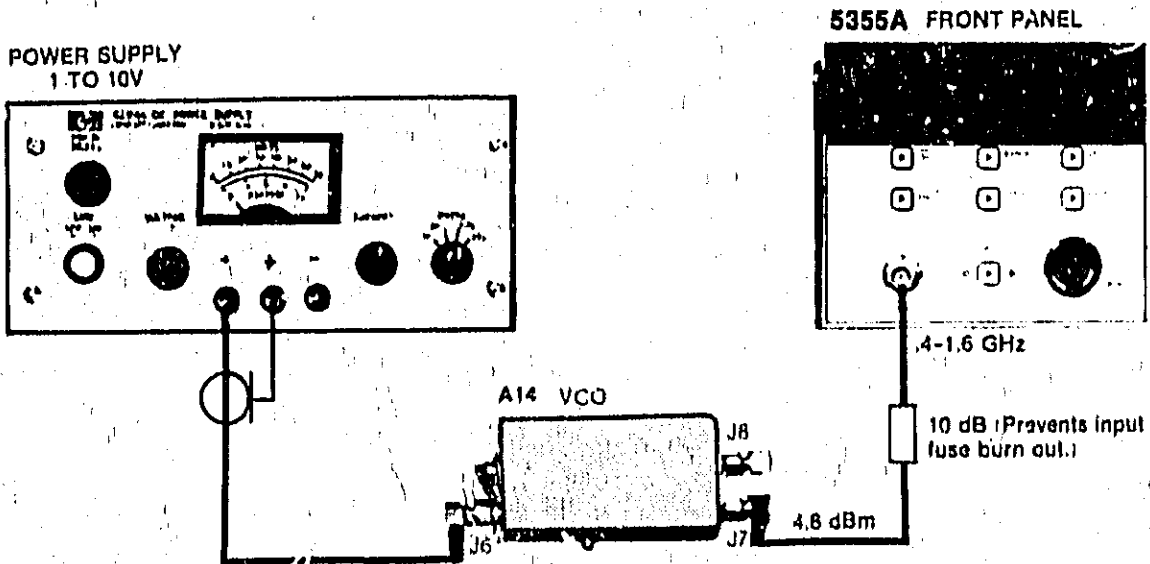
POWER SUPPLY
1 TO 10V



- b. Connect alligator to BNC clip leads to one end of a BNC cable. Connect clip leads to A11TP6 and common (▽). Connect other end of BNC cable to the Channel A Jack of the 5345A. Set the counter controls to FREQ A, 1 ms, LEVEL to PRESET, λ 1, AC, SEP.

Table B-15. Synthesizer Loop Troubleshooting (Continued)

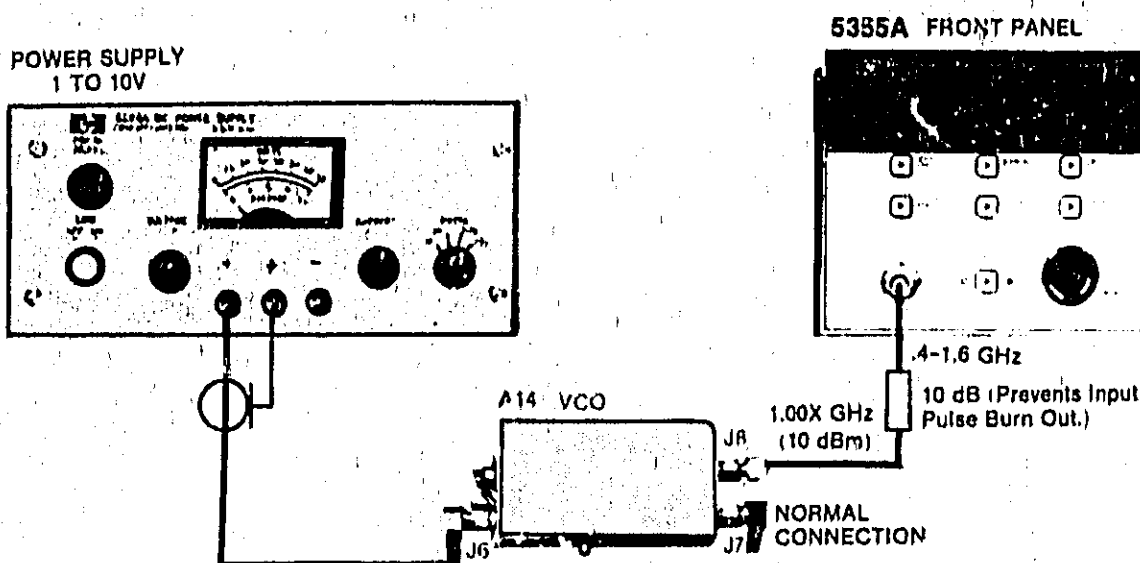
- c. Slowly vary the power supply from about +1.5V to +12V. The LO/4 frequency should vary from at least 221 MHz to 264 MHz. Continue to Step 2d if this works properly. If it does not, check the VCO frequency directly by removing the cable at A14J7 and running a cable from A14J7 to the plug-in's prescaler input via a 10-dB pad as shown below. Vary the power supply and allow the prescaler to count the VCO frequency (return 5345A FUNCTION switch to PLUG-IN). It should vary at least 885.2 to 1056 MHz. NOTE: Power level should be 4 to 8 dBm. Repair either A4 +4 circuit or A14 VCO. For information on A4, see page B-72. For information on A14, see Step 3, page B-68.



NOTE

Step d need not be done if the "Prescaler Input; PRF Mode" test failed and you are entering this table from that point. If so, proceed to Step 3.

- d. Use the same procedure outlined in the second part of Step c and check the output of A14J8 using a 10 dB pad as shown below. NOTE: power level should be >10 dBm.



- e. Leave setup connected.

Table 8-15. Synthesizer Loop Troubleshooting (Continued)

3. **A14 VCO TROUBLESHOOTING AND REPAIR PRELIMINARY INFORMATION.** If the VCO signal is not present, read the following information prior to performing the troubleshooting procedures.

Use Spectrum Analyzer. To be sure of proper VCO output, a spectrum analyzer should be used. This may help solve an intermittent miscount problem. Carefully look at the spectrum analyzer figures 3 and 4 and check the VCO output, noise floor level, and spurious signals.

Check Head. The VCO output may be correct, and the frequency converter head may be at fault. If the VCO is verified as working properly, refer to frequency converter head troubleshooting procedure, Table 8-21.

VCO Cover. When VCO signal output quality or frequency checks are being done, the VCO assembly should have its cover installed. The cover provides shielding and assists in holding the IC's U1 and U2 in their sockets.

Parts Replacement. IC U3 is the only part that requires removal of the VCO circuit board for replacement. IC's U1 and U2 are plug-in items. Observe key tab location when removing and reinstalling. Other components should be removable from the top of the board.

Board Removal. To remove the circuit board from the housing, carefully vacuum remove the solder from the feedthrough studs. Remove the two pozidriv screws and lift out the circuit board. Reverse the procedure to reinstall.

A14 Troubleshooting Procedure. After verifying in Step 2 of this table that the VCO signal is not present, connect a spectrum analyzer to J0. Observe input power limitations on spectrum analyzer and pad accordingly. Compare display with that shown in Figures 1, 2, and 3 for preliminary checks. Analyze as follows:

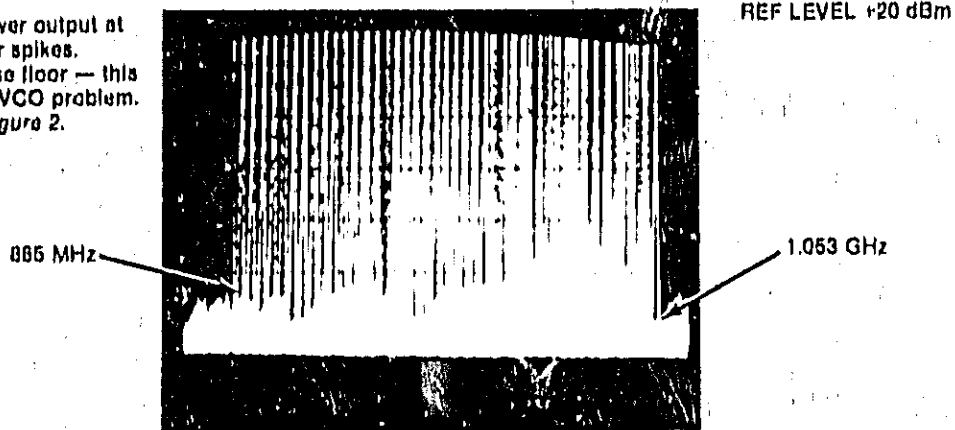
- a. If signal appears as Figure 1 (A14)6, but edge frequencies are wrong, U3 may have failed. (U3 is in feedback loop for VCO frequency control). Complete the procedures outlined in this table before replacing U3.
- b. If amplitude in Figure 1 is low, U2 is probably bad. Replace U2.
- c. Refer to Figure 3. Place 5355A in MANUAL mode and using DATA ENTRY keys, set various center frequencies between 1.5 and 1.9 GHz. Observe frequency shift of VCO output. If there is no control possible, U1 MAY have failed. Complete the procedures outlined in this table before replacing any parts.
- d. All the tests above may have checked out okay, but VCO signal purity may not be correct. This can cause miscounting in the RF head input. Using Figures 4, 5, and 6, check the VCO purity as follows:
 - (1) Set the VCO to 981.2 MHz, using diagnostic mode 09. This is the midband VCO frequency. Refer to Table 8-9 for procedure to use for setting VCO frequency.
 - (2) Figure 4 shows a sketch of the minimum VCO with proper output. Note noise floor level with respect to signal level. Figure 5 shows an actual photo of VCO signal that is also correct. Figure 6 shows an incorrect VCO output. Note noise floor level.

Hints: The spectrum analyzer sweep is very slow when set up as described in the photos. For best results, a spectrum analyzer with variable persistence and/or storage capability should be used. An HP 8565A spectrum analyzer was used for these photos.

- (3) If a miscount occurs at a particular input frequency, use diagnostic mode 01 to determine VCO frequency in use at time of miscount. Remove RF signal input and set up test per Step 1. Using diagnostic 09 per Step d(1), set VCO frequency and have a close look at it. If faulty signal is observed on spectrum analyzer, replace VCO. (Keep in mind that the signal used for spectrum analysis is the signal that drives the RF head. To check the 5355A with a live signal, the VCO output must be connected to the RF head connector.)

Table 8-15 Synthesizer Loop Troubleshooting (Continued)

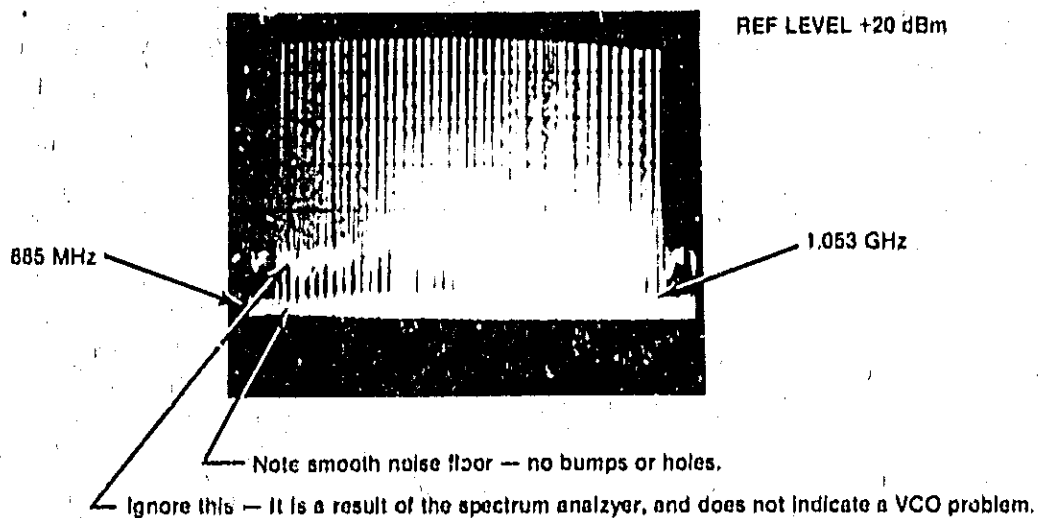
Note smooth power output at VCO; no holes or spikes.
Note ragged noise floor — this could indicate a VCO problem. Compare with Figure 2.



Input Atten: 40 dB
Scale: 10 dB/div
Center Freq: 967 MHz
Resolution Bandwidth: 300 kHz
Freq Span/Div: 20 MHz

5355A in AUTO mode — synthesizer is sweeping.
5356A head installed, no signal applied.
B and C heads will give different pictures, due to the different number of VCO steps used for those heads.

Figure 1. A14J8 Improper Signal



Input Atten: 40 dB
Scale: 10 dB/div
Center Freq: 967 MHz
Resolution Bandwidth: 300 kHz
Freq Span/div: 20 MHz

Figure 2. A14J8 Proper Signal

Table 8-15. Synthesizer Loop Troubleshooting (Continued)

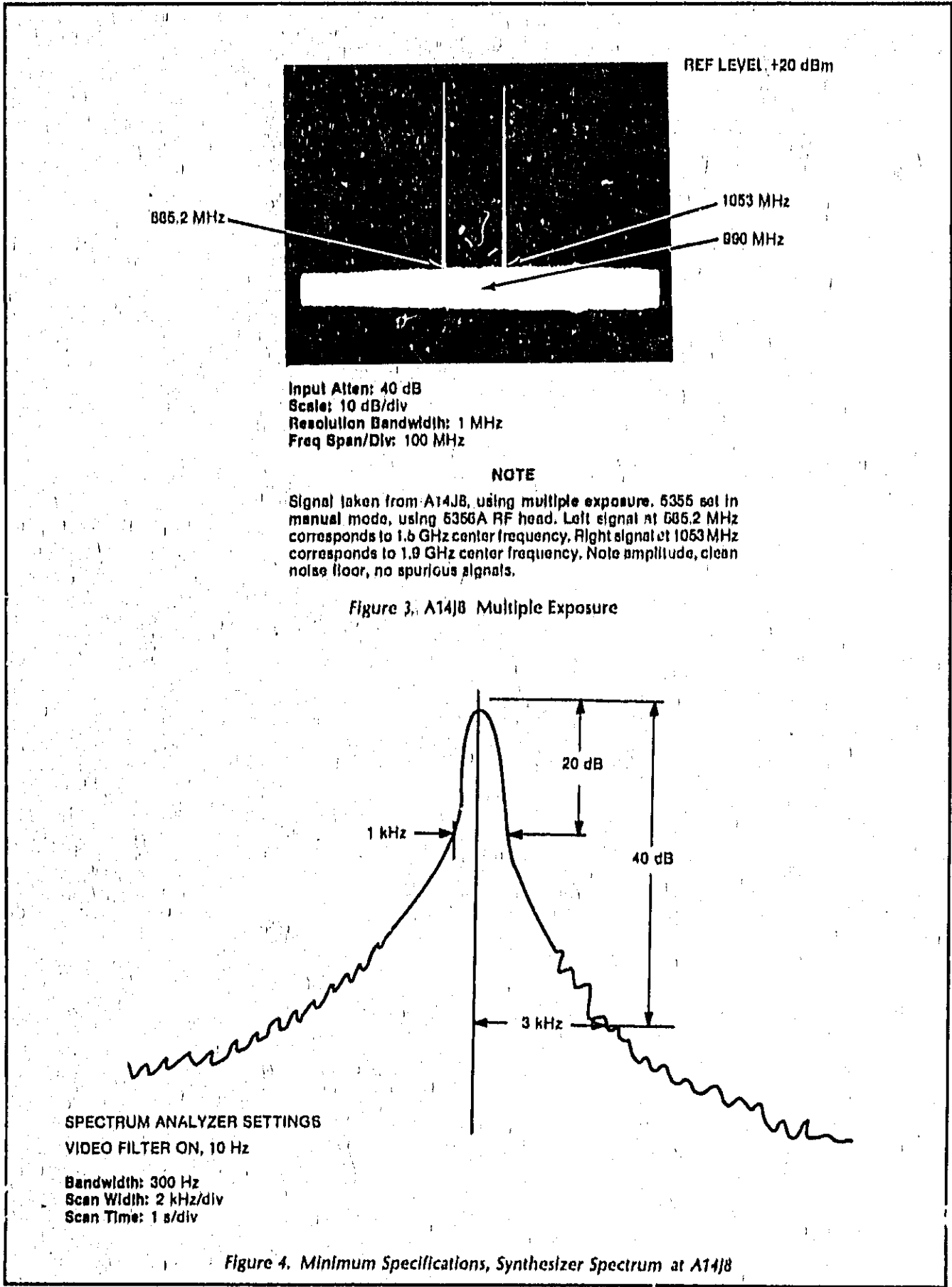
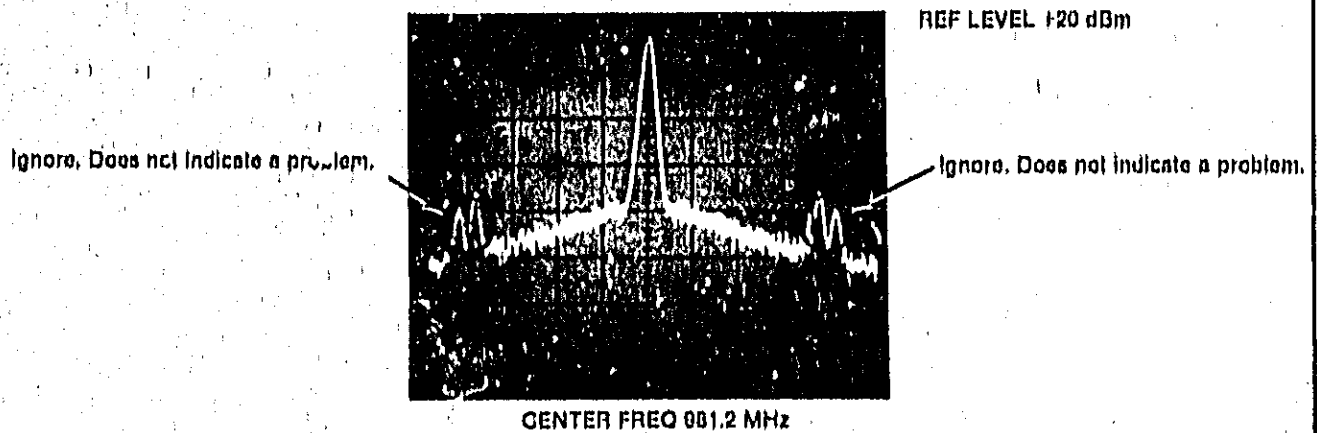


Table 8-15. Synthesizer Loop Troubleshooting (Continued)



Input Att: 40 dB
Scale: 10 dB/div
Resolution Bandwidth: 300 Hz
Freq Span/Div: 2 kHz
Video Filter: 10 Hz

(Note noise floor in respect to signal.)

Figure 5. Proper VCO Signal
(Compare with Specifications shown in Figure 4)

This is a problem area.
Spec sketch says 40 dB down at 3 kHz.
This VCO is only 30 dB down.

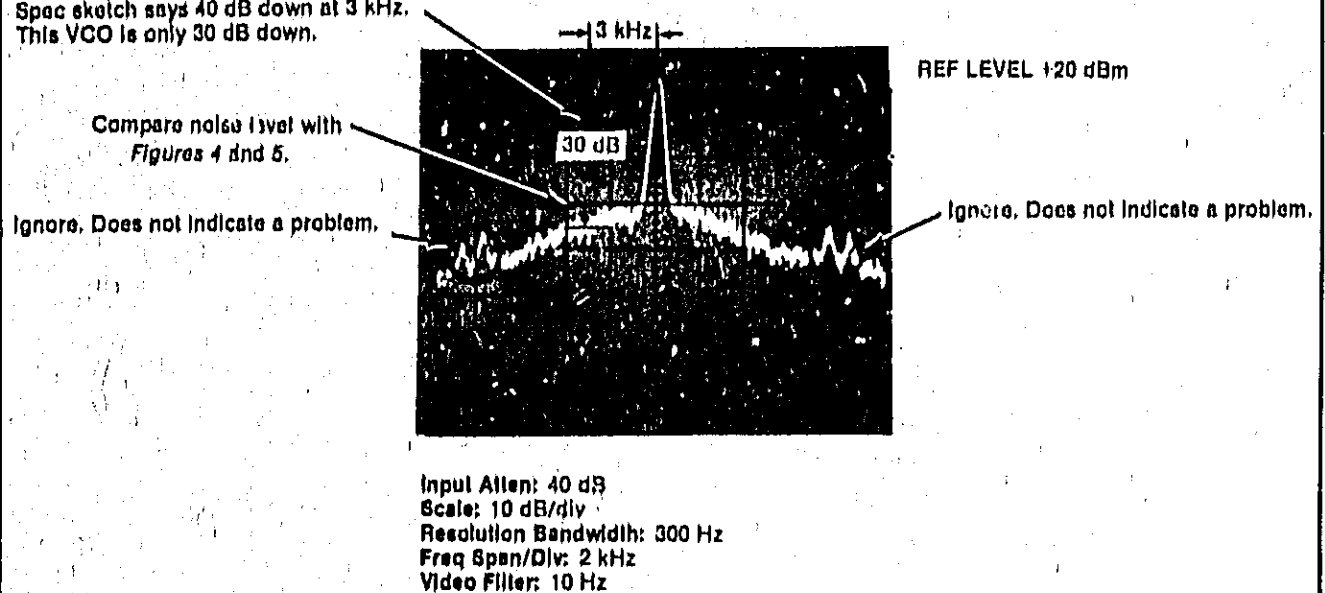


Figure 6. Improper VCO Signal

Table 8-15. Synthesizer Loop Troubleshooting (Continued)

4. Verify A4 Programmable +M operation and associated signals by checking the following points.
 - a. Connect setup as shown in Step 2d and adjust power supply to read 1.000X GHz.
 - b. Setup the plug-in so that the only key lit is CW.
 - c. A4 pins 6 and 7: TTL pulsing. If not, check A8U25.
 - d. Push the plug-in  key (enters 1.5 GHz as the manual center frequency).
 - e. Set the 5345A controls to FREQ A, 1 MΩ, X10, AC SEP. Connect a 10:1 oscilloscope probe to the Channel A Jack and to A5TP2 of the plug-in (the +M output of A4). Adjust the LEVEL control for a stable reading. The counter should read 112.9 kHz.*
 - f. Enter other manual center frequencies and measure the output frequency of the +M. Compare these readings to those in the table below.
- Procedure:
- (1) Set 5345A FUNCTION switch to PLUG-IN.
 - (2) Push  key (light ON).
 - (3) Select manual center frequency with UP/DN keys.
 - (4) Push  key (light off) to exit data entry mode. The  light should be on.
 - (5) Set 5345A FUNCTION switch to FREQ A to read +M frequency.
 - (6) Repeat procedure for each entry and measurement.

A4 (+M) Checks												
FOR TROUBLESHOOTING PURPOSES ONLY												
MANUAL FREQ	A4U1						A4U3				5345A* DISPLAY (+M)	
	2	10	12	15	7	5	10	5	7	2		15
1.5 GHz	L	H	H	L	L	H	L	L	H	L	L	112.9 kHz
5.0 GHz	H	L	L	L	L	H	L	L	L	L	L	105.1 kHz
9.9 GHz	H	H	L	L	L	H	L	H	H	L	H	98.58 kHz
15.0 GHz	L	L	L	L	L	H	L	L	L	H	H	101.6 kHz
19.2 GHz	L	L	H	L	L	H	H	H	H	L	H	100.2 kHz
22.6 GHz	H	L	L	H	H	L	L	H	H	L	H	98.42 kHz
26.5 GHz	L	L	H	L	H	H	L	H	H	L	H	99.01 kHz

*Since these readings are a function of the 1 GHz VCO frequency, they will vary slightly with power supply resolution and VCO drift.

Table 8-15. Synthesizer Loop Troubleshooting (Continued)

- g. If the counter measures these frequencies, the A4 board is working properly. If not, troubleshoot A4. Use waveform photos below and dc voltages on schematic as an aid to troubleshooting. Observe the following conditions:
- All boards inserted and coax cables attached.
 - A4 on its extender board, VCO lead connected at A4J1.
 - RF head installed.
 - No signal applied.
 - DC voltage checks taken with MANUAL MEASUREMENT mode active. This stops the VCO, for stable readings.

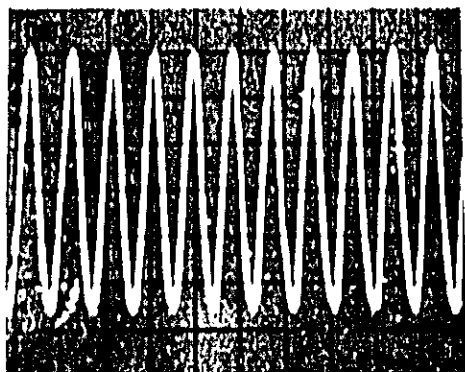


PHOTO 1

+4 OUT (T0)

Set 5355 in manual mode, 1.5 GHz center frequency.

Vert: .01V/div, X10 probe in use, dc coupled
Horiz: .05 μ s/div, X10 mag

NOTE

Position of scope probe lead will affect scope presentation and level.

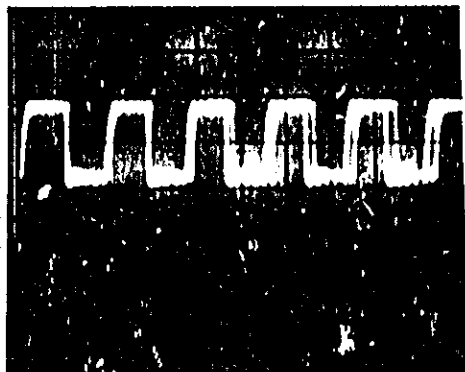


PHOTO 2

TP1

Set 5355 in manual mode, 1.5 GHz center frequency.

Vert: .2V/div, X10 probe in use, dc coupled
Horiz: .1 μ s/div

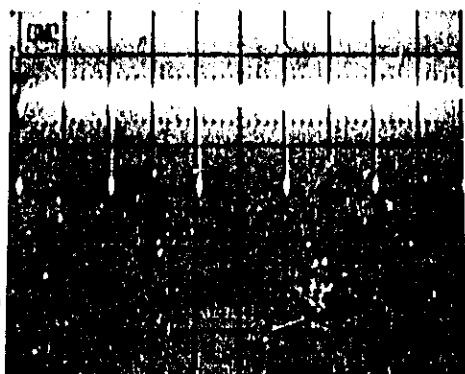


PHOTO 3

16,16 01 OUTPUT

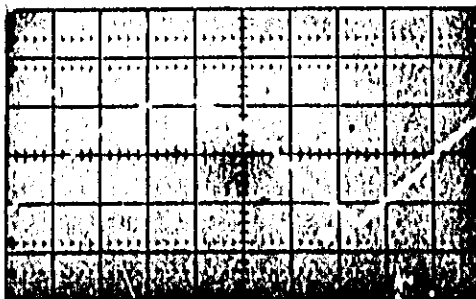
Set 5355 in manual mode, 1.5 GHz center frequency.

Vert: .2V/div, X10 probe in use, dc coupled
Horiz: 5 μ s/div

- h. Return boards and cables to their original configuration (also adapter between A2 and A3).

Table B-15. Synthesizer Loop Troubleshooting (Continued)

5. The problem appears to be on the A5 DC Amp/Loop Comp board. With the plug-in set to the prescaler mode, the synthesizer should be locked with a VCO output of 1 GHz. Or, with no input signal in the converter head mode, the synthesizer should be searching and the A5 output should look like the waveform below.



.2V/div., 20 ms/div., dc
Waveform was moved up with POSITION control.

Troubleshoot the A5 board in either of these modes. Also, see A5 Adjustment Procedure in Section V. Use waveform photos below and dc voltages on schematic as an aid to troubleshooting.

Conditions:

- RF head is installed; no signal applied.
- All boards in place and connected.
- A5 on its extender board.
- Place 5355 in MANUAL MEASUREMENT mode. This stops the synthesizer sweep and enables stable voltage readings.
- Photos 1, 2, 3 taken with conditions as above.
- Photos 4, 5 taken with 5355A in AUTOMATIC mode to enable synthesizer sweep.

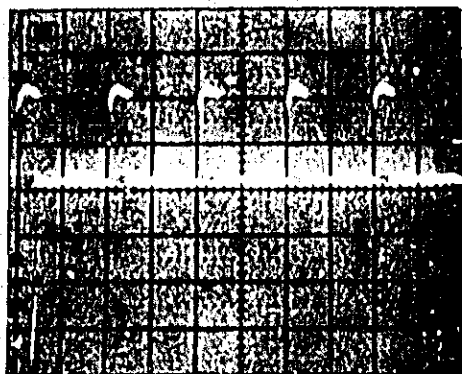


PHOTO 1

U313, or TP1

Vert: .2V/div, X10 probe in use, dc coupled
Horiz: 5μs/div

Table 8-15. Synthesizer Loop Troubleshooting (Continued)

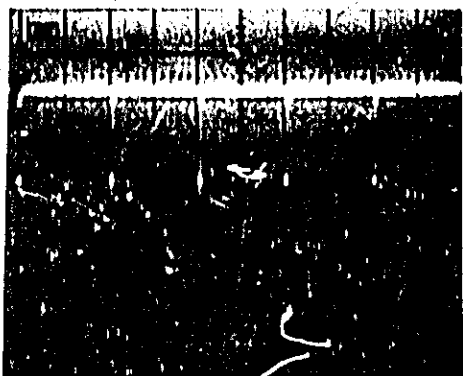


PHOTO 2

U3(1) or TP2
Vert: .2V/div, X10 probe in use, dc coupled
Horiz: 5µs/div

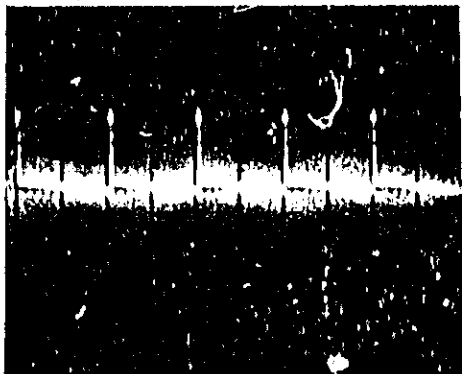


PHOTO 3

U3(10) PHASE DET OUTPUT, AC COUPLED
Vert: .05V/div, X10 probe in use, ac coupled
Horiz: 5µs/div

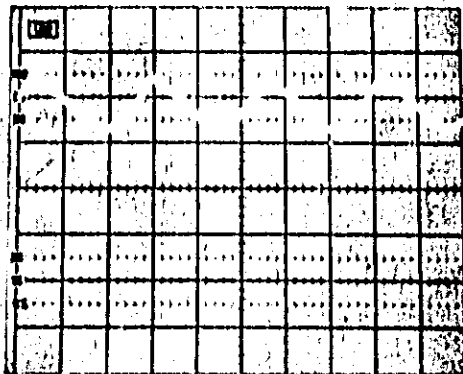


PHOTO 4

TP4 IF TUNING
Vert: .5V/div, X10 probe in use, dc coupled
Horiz: .05 s/div

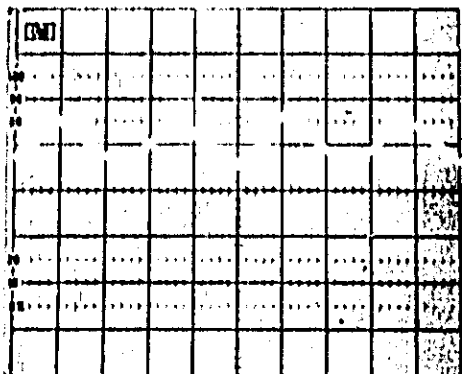


PHOTO 5

TP5 VCO TUNE
Vert: .5V/div, X10 probe, dc coupled
Horiz: .05 s/div

NOTE

Perform adjustment procedures (Section VI) for A5 if any parts on A5 are replaced.

Table B-16. A1 Front Panel Troubleshooting

NOTE

This procedure requires the use of the HP 5004A Signature Analyzer and the A7 Extender Test Board (05355-60025). Place A7 on its extender board.

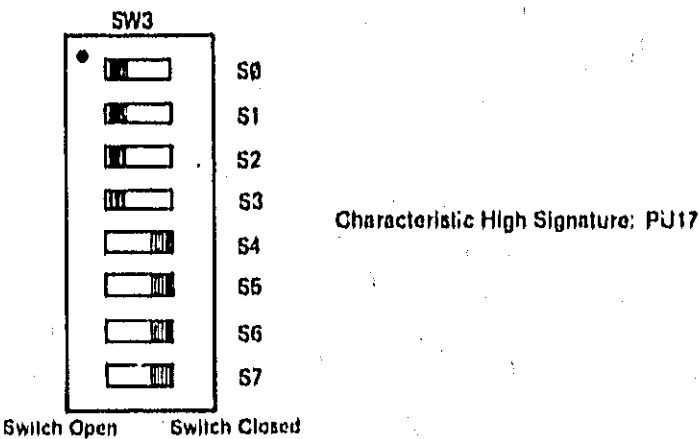
Connect 5004A as follows:

START/STOP lead to TP98 on A7 Extender Test board.
CLOCK lead to A7TP5, and GND to $\varnothing$.

Set 5004A control as follows:

START to 
STOP to 
CLOCK to 

On A7 Extender Test board, set "S3" of SW3 as shown and push the red toggle switch to generate a reset. This allows signature analysis of U1, U2, and U3 on the A1 board.



If a pushbutton switch on the 5355A front panel is suspected to be bad, the data lines can be easily checked on the A7 Extender Board without removing the front panel. Use the following signatures.

Data Line Name	A1 Test Point	Pushbutton Name	Signature with Button In	Signature with Button Out
D1	U1(3)	OFFSET FREQ	9APr	9A64
D8	U1(5)	MAN FREQ	PF85	PF04
D2	U1(7)	OFFSET	2862	28P3
D4	U1(14)	MANUAL	8AF4	8A45
D5	U1(16)	PULSE	FP41	FPF0
D3	U1(18)	CW	C2C5	C234
D6	U1(12)	INPUT SELECT	C80F	C88H

The following signatures primarily check the latches that drive the pushbutton LEDs. Two exceptions are U2 pins 12 and 15.

A1 Test Point	Signature	A1 Test Point	Signature
U3(2)	62CH	U2(2)	A4U9
U3(5)	4F8F	U2(5)	2H45
U3(7)	2PCF	U2(7)	780C
U3(10)	1795	U2(10)	386P
U3(12)	FH0F	U2(12)	A04F
U3(15)	C6HA	U2(15)	0034

If the observed signatures don't match these shown, troubleshoot and replace the appropriate IC.

Table B-17. AB Decoder/HP-IB Troubleshooting

NOTE

The Part I procedure is only for the decoder section of this board. The procedure requires the use of the 5004A Signature Analyzer and the A7 Extender Test Board (05355-60025). RF head must be installed, except where noted. (Place A7 and A8 on their appropriate extender boards.)

PART I. DECODER SECTION:

1. Connect 5004A as follows: START/STOP leads to TP90 on A7 Extender Test board (05355-60025), CLOCK lead to A7TP5, and GND lead to ∇ .

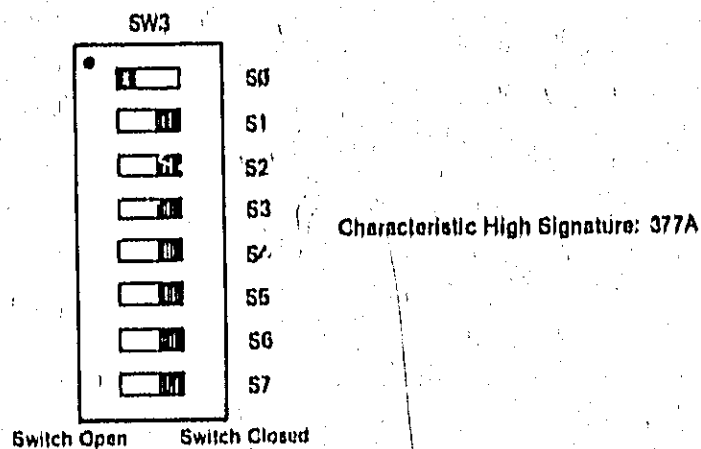
Set 5004A controls as follows:

START to 
STOP/CLOCK to 
GND to ∇

NOTE

Start with first SW3 switch (S0) and set in numerical sequence. Don't power down during test. The following steps depend on the circuit conditions set by the SW3 switches. If power down is necessary, begin again at this point and repeat all switch settings.

On A7 Extender Test board, set SW3 switches as shown and push the red toggle switch to generate a reset. This allows signature analysis of AB U22, 24, and 25.



A8 Test Point	Signature	A8 Test Point	Signature	A8 Test Point	Signature
U22(7)	3AA1	U24(7)	PP9C	U25(7)	51H4
U22(9)	AUHF	U24(9)	50U9	U25(9)	054F
U22(11)	25H1	U24(12)	F3U0	U25(11)	UAC4
U22(12)	249F	U24(13)	F20F	U25(12)	H635
U22(13)	U7A3			U25(13)	F439
U22(14)	630P	U23(2)	76UP	U25(14)	8419
U22(15)	3039			U25(15)	42HH

Table 8-17. AB Decoder/HP-IB Troubleshooting (Continued)

2. On A7 Extender Test board, set SW3 switches as shown and push the red toggle switch to generate a reset. This allows signature checks on A8 U10.

SW3

S0
S1
S2
S3
S4
S5
S6
S7

Switch Open Switch Closed

Characteristic High Signature: A0PP

A8 Test Point

U10(3)
U10(4)
U10(6)
U10(11)
U10(13)
U10(14)

Signature

UA2C
70P1
319B
7963
31PH
09PC

3. On A7 Extender Test board, set SW3 switches as shown and push the red toggle switch to generate a reset. This allows signature checks of U15, U16, U17, U18, U19, U21.

SW3

S0
S1
S2
S3
S4
S5
S6
S7

Switch Open Switch Closed

Characteristic High Signature: P6L3

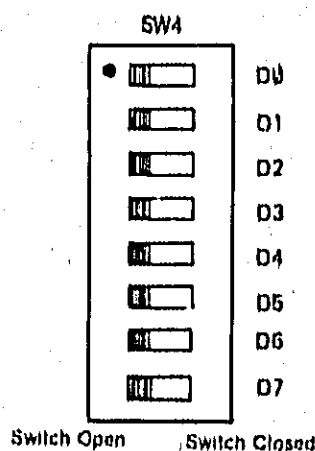
A8 Test Point	Signature	A8 Test Point	Signature
U17(5)	470U	U21(5)	9PPH
U17(2)	CU3U	U21(18)	260C
U17(16)	426H	U21(3)	8AUU
U17(15)	FU4F	U21(7)	653A
		U21(9)	PPAH
		U21(12)	CFAA
		U21(14)	PPPP
		U21(16)	8ACP

A8 Test Point	Signature with 5356A Head	Signature without 5356A Head
U16(3)	CU3U	57FF
U16(6)	470U	AUUF
U18(6)	FU4F	FU4F
U18(11)	AA9P	AA9P
U15(11)	P609	U64A
U15(8)	PA87	PA87
U19(4) (TP2)	7086	190A

Replace the appropriate IC if readings disagree with those shown.

Table 8-17. AB Decoder/HP-IB Troubleshooting (Continued)

4. To complete the troubleshooting to the decoder section, buffer U13 must be checked by either replacing it with a known good IC or by checking it manually with a logic probe and pulser. To do this, remove the converter head, return the SW3 switch on the A7 extender test board to its original (nonservice mode) position, open all A7 data switches (see SW4 below), jumper A0 U13(15) to ψ to enable U13, and push the reset toggle switch. Pulse the input of each inverter and check the output.



NOTE

When finished, return switches to original positions.

PART II. AB HP-IB INTERFACE SECTION

This procedure checks each HP-IB line, using the 59401A Bus System Analyzer.

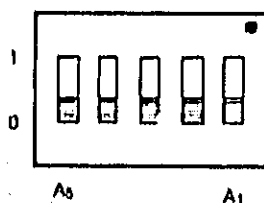
Using the AB schematic diagram, this procedure will lead you through each IC block as a method to localize the failed part. An oscilloscope or logic probe may be used as a tracing aid.

The first test is designed to prove the handshake parts of the HP-IB interface, by setting up an address and checking the handshake lines. The second test is designed to prove the data lines by setting up address checks to stimulate each data line.

Handshake Circuits: The following procedure will allow troubleshooting of the handshake circuits U1, U2, U3, U5, U6, U7, U8, U9, U11 and U12.

1. Set up the 5355A as follows (note: no HP-IB related actions are needed on the 5345A counter):
Set 5355A address to decimal 00, octal code 040 (on rear of 5355A). (See page 8-81 for Table of Address Codes, Table 8-17A.)

POSITION SWITCHES AS SHOWN



2. Set up 59401A Bus System Analyzer as follows (connect HP-IB cable between 5355A and 59401A):
REN: ON (REN lamp ON)
TALK/LISTEN: TALK
HALT/SLOW/FAST: HALT
COMP: OFF
MEMORY: OFF (BUS lamp ON)
ATN: ON (ATN and NDAC lamps ON)
DIO: 00/100/000 (or octal code 040)
EXECUTE: Push

Table 8-17. A8 Decoder/HP-IB Troubleshooting (Continued)

3. If the handshake circuits are operating properly, the REMOTE and LISTENING lamps on the 5355A will be lighted. If they are, proceed to addressing checks. If they are not lighted, proceed as follows:
4. While pressing and releasing the EXECUTE pushbutton, carefully note the action of the indicator lamps on the 59401A. These lamp indications can tell much about the operation of the handshake circuits.

NOTE

Prior to pressing EXECUTE, the ATN (attention), REN (remote enable), and NDAC (not data accepted) lamps should be on.

ANALYSIS: NDAC and NRFD (not ready for data) lamps are driven by signals from the 5355A. Observing them can give a clue as to where to suspect a fault in the 5355A. See Figure 8-20 and Figure 8-21 for a graphical and flow chart presentation of the handshake process.

Press and hold EXECUTE. Observe DAV (data valid) and NRFD lamps on and NDAC off. If this action does not occur, troubleshoot these areas of A8 to find the fault:

Handshake flip-flop U12
Listen flip-flop U11
Associated gates U9, U15, U8, U3, U2

5. To have available a repetitive addressing loop to allow oscilloscope troubleshooting of the handshake circuits, the memory feature of the 59401 may be utilized as follows:
 - a. Set MEMORY to ON.
 - b. Press EXECUTE to load the octal code address 040 into the memory cells. The memory has 32 locations; the current location is shown on the 59401A display. Press EXECUTE repeatedly to load all memory locations.
 - c. Set MEMORY off.
 - d. Set FAST/SLOW/HAUT to SLOW. The 59401A will now address the 5355A repeatedly at two per second. With the switch in FAST position, addressing will take place at system speed, i.e., as fast as the 59401A and 5355A can respond to each other.
6. Using an oscilloscope or 10525T Logic Probe and the A8 Schematic Diagram as a guide, signal trace through the circuits looking for a stuck output, etc. Replace the faulty circuit element(s).

Addressing Checks: To check out the address lines and all combinations of addressing, the 59401A and 5355A may be set at each address as shown in Table 8-17A. As a short cut, 041 and 076 may be used. Octal code 040, used previously, checks all address lines low. Octal code 041 will check line 1 high, while octal code 076 will check lines 2 through 6 high. Follow the 59401A setup described in Handshake Circuits to perform this test. Observe 59401A handshake lights will light, but 5355A remote and listen lamps won't light if fault exists.

1. If one of the codes listed above does not work, set in other codes using Table 8-17A in an attempt to isolate the faulty address line.
2. Troubleshoot A12 U1, U2, and U3 using the capability of the 59401A to influence each data line high or low. With an oscilloscope, check the above IC's. Replace any faulty components. Proceed to next step if the fault still exists.
3. Check A8 U4 IC. This may be done by using the loop test routine described in Step 5, Handshake Circuits.
 - a. Set up various address codes in the 59401A.
 - b. Using an oscilloscope, monitor U4 pin 1 with Channel A. Check the U4 output pins with Channel B.
 - c. Read the output lines when Channel A is low.

ANALYSIS: The output of A8 U4 is the microprocessor data bus in the 5355A. These lines will have activity on them unrelated to HP-IB operation. Therefore, it is important to read U4 output in synchronism with the U4 strobe line pin 1.
 - d. Check all outputs of U4 for each address condition as supplied by settings on the 59401A. Replace if faulty. Beware of stuck data bus lines.

Table B-17. AB Decoder/HP-IB Troubleshooting (Continued)

Table B-17A. Table of Address Codes

NOTE

Select the listen address from the table below and set the address switches to the corresponding positions.

ADDRESS SWITCHES



ASCII CODE CHARACTER	5355A ADDRESS SWITCHES					5-BIT DECIMAL CODE	59401A OCTAL CODE
LISTEN	A6	A5	A4	A3	A2	A1	
SP	0	0	0	0	0	0	040
!	0	0	0	0	1	1	041
"	0	0	0	1	0	0	042
#	0	0	0	1	1	1	043
\$	0	0	1	0	0	0	044
%	0	0	1	0	1	1	045
&	0	0	1	1	0	0	046
'	0	0	1	1	1	1	047
(	0	1	0	0	0	0	050
)	0	1	0	0	1	1	051
*	0	1	0	1	0	0	052
+	0	1	0	1	1	1	053
,	0	1	1	0	0	0	054
-	0	1	1	0	1	1	055
.	0	1	1	1	0	0	056
/	0	1	1	1	1	1	057
0	1	0	0	0	0	0	060
1	1	0	0	0	1	1	061
2	1	0	0	1	0	0	062
3	1	0	0	1	1	1	063
4	1	0	1	0	0	0	064
5	1	0	1	0	1	1	065
6	1	0	1	1	0	0	066
7	1	0	1	1	1	1	067
8	1	1	0	0	0	0	070
9	1	1	0	0	1	1	071
:	1	1	0	1	0	0	072
;	1	1	0	1	1	1	073
<	1	1	1	0	0	0	074
=	1	1	1	0	1	1	075
>	1	1	1	1	0	0	076

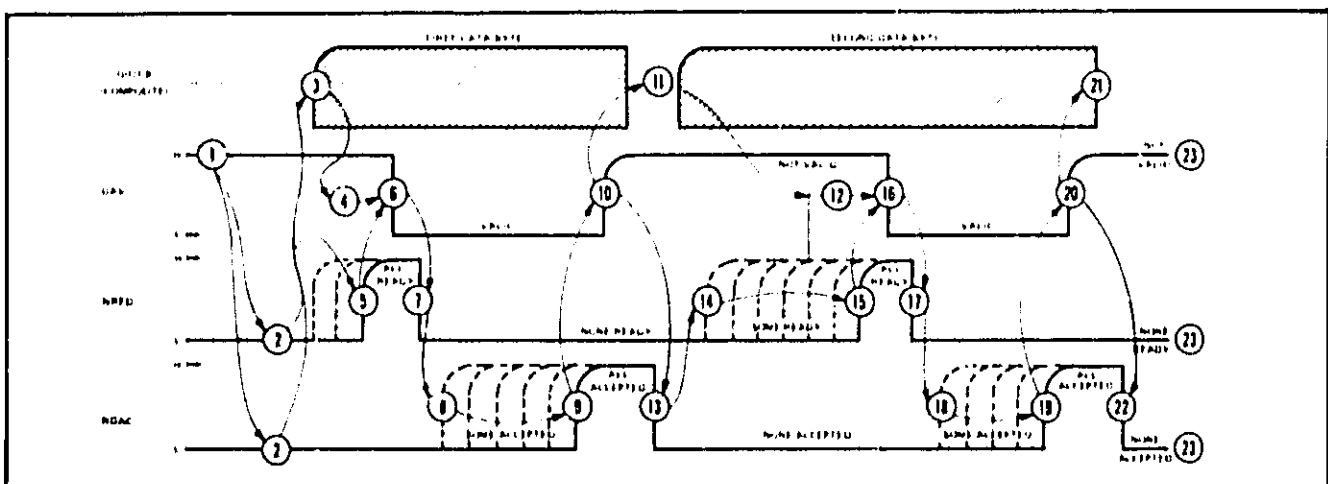


Figure 8-20. Signal Line Timing Sequence for One Talker and Multiple Listeners Using Handshake Process

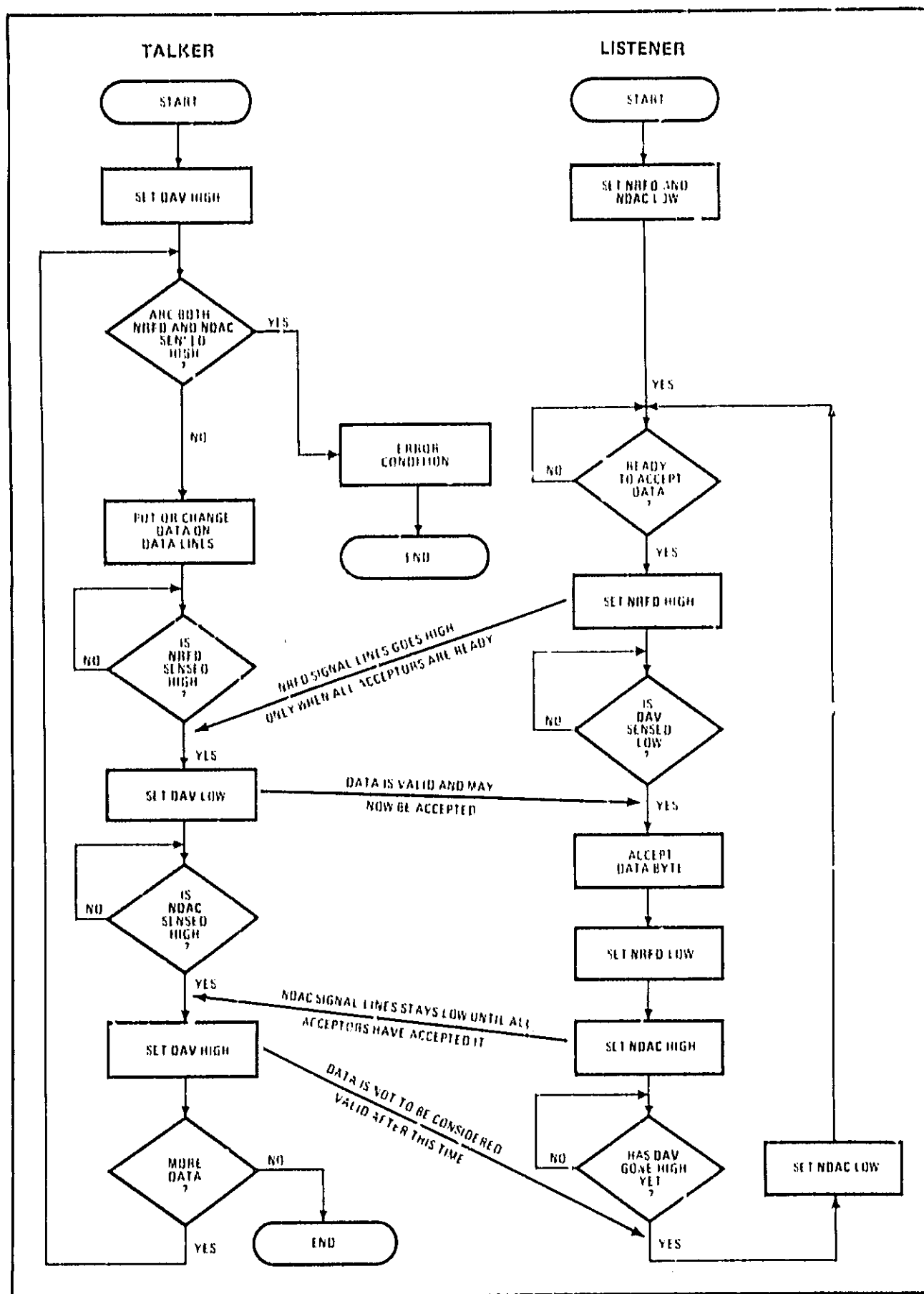


Figure 8-21. Logical Flow of Events for Source and Acceptor When Transferring Data Using Handshake Process

Table B-1B. A7 Microprocessor Troubleshooting

1. Place the A7 Microprocessor Assembly on the extender board, IIP P/N 05355-60025 which is shown below. Turn on the 5345A. Note on DIP switches:

Toward dot = OPEN

Away from dot = CLOSED

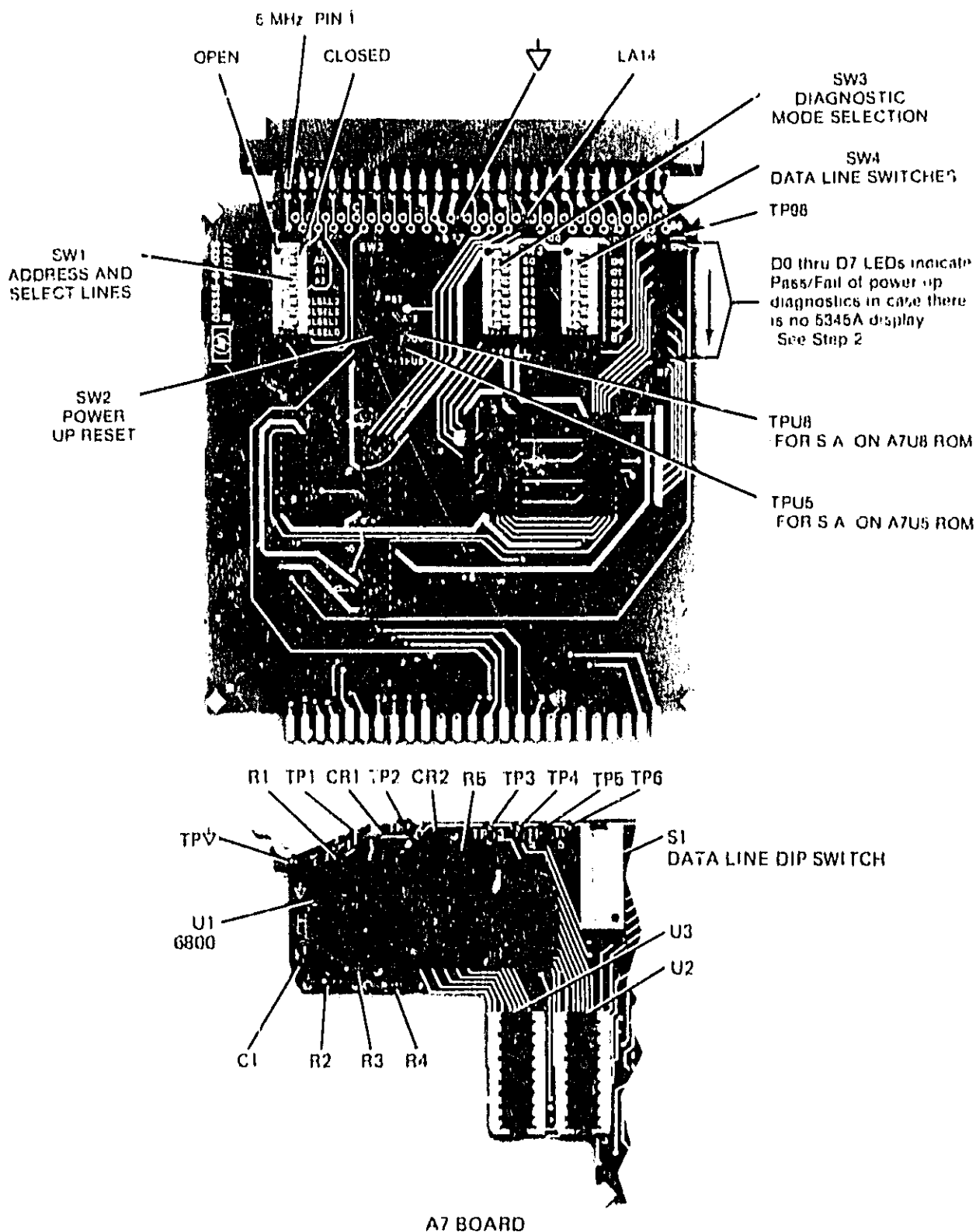


Table 8-18. A7 Microprocessor Troubleshooting (Continued)

2. Observe carefully the D0 through D7 LED's. They have the following significance:

NOTE

Prior to replacing an IC, check the LED that does not light.
(The LED may have failed.)

- D0 LED on: A7U10 RAM has passed the power up test. Replace this IC if D0 is not on.
D1 LED on: A7U12 RAM has passed the power up test. Replace this IC if D1 is not on.
D2 LED on: A7U5 ROM has passed. If the interface exchange is taking place between the 5355A and the 5345A, the error code 74 will be displayed on the 5345A if A7U5 has failed. Replace this IC if D2 is not on.
D3 LED on: A7U8 ROM has passed the power up test. If the interface exchange is taking place between the 5355A and the 5345A, the error code 78 will be displayed on the 5345A if A7U8 has failed. Replace this IC if D3 is not on.

ANALYSIS: In the following 3 tests, the 5355A and the 5345A operate together to check the operation of the synthesizer in the 5355A. The sequence of events is as follows:

- The 5355A commands the synthesizer to 885.2 MHz. (The synthesizer consists of A4, A5, and A14).
- This synthesizer signal is routed from the 5355A via A11 to the 5345A to be measured. The gate lamp on the 5345A may be seen to flash on and off as the measurement is made.
- After measurement, the 5345A responds to the 5355A that the measurement was made and the results are compared with what the 5355A commanded of its synthesizer.
- If okay, the test will proceed to the next frequency. If not okay, the error code will be displayed, and the LED on the extender board will not be lighted.

NOTE

It is evident that the synthesizer signal passes through several circuits and checks before the test can be considered passed. It is important to check the synthesizer circuits, using Table 8-15 as a guide. If this action fails to find the trouble, check the interface connectors and wiring between the 5355A and the 5345A.

- D4 LED on: The VCO has passed the 885.2 MHz checkpoint in the power up test. If the interface exchange is taking place between the 5355A and the 5345A, the error code 83 will be displayed, if the VCO has failed to pass this check. In any event, if D4 is not on, the VCO must be checked as discussed in ANALYSIS above.
- D5 LED on: The VCO has passed the 970.8 MHz checkpoint in the power up test. If the interface exchange is taking place between the 5355A and the 5345A, the error code 86 will be displayed if the VCO has failed to pass this check. In any event, if D5 is not on, the VCO must be checked as discussed in ANALYSIS above.
- D6 LED on: The VCO has passed the 1056.0 MHz checkpoint in the power up test. If the interface exchange is taking place between the 5355A and the 5345A, the error code 89 will be displayed if the VCO has failed to pass this check. In any event, if D6 is not on, the VCO must be checked as discussed in ANALYSIS above.
- D7 LED off: This is the proper response if the 5355A has powered up properly. If D7 is on, it indicates that the 5345A is in SELF CHECK. The error code 88 will be displayed for 10 seconds, and the gate lamp on the 5345A will be seen flashing. The LED's on the front panel of the 5355A will also stay on. The reason for this action is this: when the 5345A is in SELF-CHECK, the A and B channels are connected together, and the VCO check cannot be done. The gate lamp flashing indicates that the 5345A is attempting to do the VCO measurements but cannot in SELF-CHECK. After 10 seconds, the power up routine times out.

Table 8-18. A7 Microprocessor Troubleshooting (Continued)

3. To perform signature analysis on the A7 assembly, proceed as follows:
 - a. Place the 5004A START and STOP leads on the LA14 test pin of the A7 extender board.
 - b. Place the CLOCK lead of the 5004A on TP5 of the A7 board.
 - c. Place the GND lead on the ground test pin.
 - d. Open the data line switches on the A7 board by setting all switches to the right side of package (toward the black dot).
 - e. Jumper A7 TP2 to ground to initiate microprocessor freerun.
 - f. Set the 5004A for negative slope on START, STOP, and CLOCK (all pushbuttons should be in).
 - g. Turn on the 5345A.
4. Place the 5004A data probe on +5V and verify that the characteristic 1's signature is 0001. If 0001 is not displayed on the 5004A, the U1 microprocessor is not freerunning (or U3 driver is not passing A14 from U1). If 0001 is displayed, go to Step 4. If not, continue with Step 3a.
 - a. Check power-up circuitry: logic probe on U9(14). Push SW2 RESET switch on extender board. The reset line should go Low and stay Low for about half a second after the switch is released before going to a TTL High. If not, suspect U9 and associated circuitry.
 - b. Remove jumper between A7TP2 and ψ . Close A7 data line switches by setting switches away from dot. Check U1 microprocessor control lines after power-up:
 - U1(6) NONMASKABLE INTERRUPT — HIGH
 - U1(2) HALT — HIGH
 - TP1 INTERRUPT REQUEST — HIGH. Press any button on 5355A and verify that this point goes Low. Press RESET on 5345A and verify this point goes Low. If this point doesn't go Low, troubleshoot A1 Front Panel, and 5345A/5355A interface.
 - U11B(8) DATA BUS ENABLE — PULSING

NOTE

The following photos were taken with the jumper between TP2 and ψ removed. Be sure to connect jumper again once the waveforms have been examined.

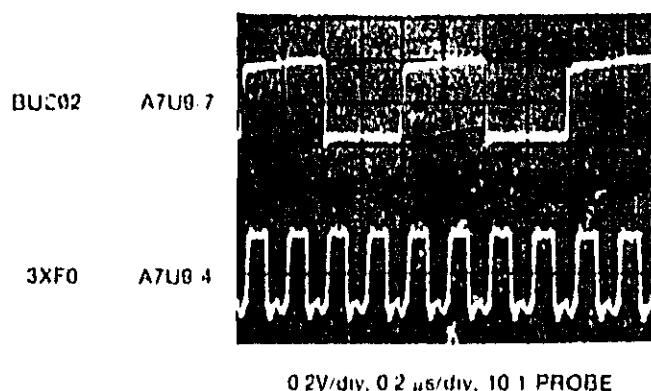
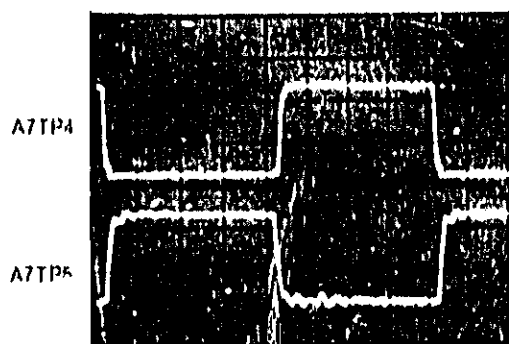


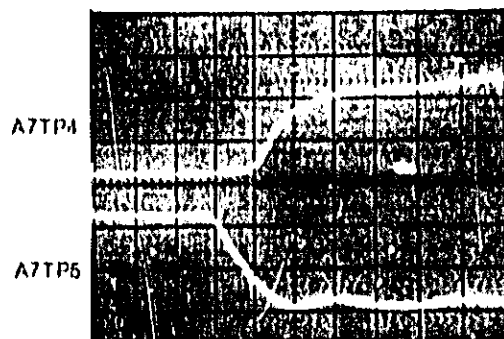
Table 8-18. A7 Microprocessor Troubleshooting (Continued)

- c. Check processor clock operation using a dual channel oscilloscope. Connect scope probes to TP4 and TP5 (01 and 02). Waveforms should appear as in photos below.



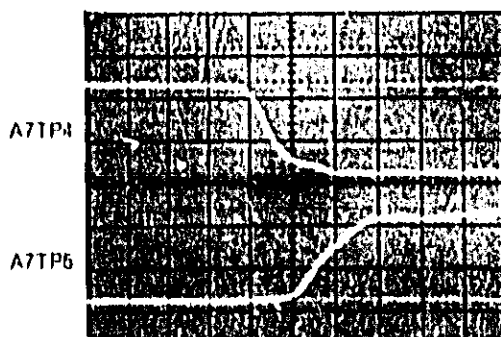
0.2V/div, 0.1 μs/div, 10:1 PROBE

LEADING EDGE



0.2V/div, 10 ns/div, MIXED SWEEP, 10:1 PROBE

TRAILING EDGE



0.2V/div, 10 ns/div, MIXED SWEEP, 10:1 PROBE

- d. If these signals are present, check diodes CR1 and CR2.
e. The problem appears to be a bad microprocessor (U1) or U3 is not passing the A14 line on U3(16).

5. Push SW2 RESET switch on A7 extender board. Place the 5004A data probe on the following address signal points and check for proper freerun signatures:

U2(5)	5554	U3(5)	2H71
U2(7)	CCCC	U3(7)	HPP1
U2(9)	7F7H	U3(9)	1292
U2(3)	5H20	U3(3)	HAP6
U2(18)	0AFC	U3(12)	3C97
U2(6)	UPFF	U3(14)	3B26
U2(14)	52F9	U3(16)	755C
U2(12)	HC88	U3(18)	0000 (Low, should toggle with TP2 jumper removed. Replace jumper when finished.)

If these signatures are correct, go to Step 6. If not, continue with Step 5a.

Table B-18. A7 Microprocessor Troubleshooting (Continued)

- a. Check the following signatures on the MPU side of buffer/drivers U2 and U3. Correct or incorrect signatures should isolate the problem to either U1 or one or more of the buffer/drivers U2, U3.

U2(15)	5555	U3(15)	2H70
U2(13)	CCCC	U3(13)	1HPP0
U2(11)	7F7F	U3(11)	1293
U2(17)	5H21	U3(17)	1HAP7
U2(2)	0AFA	U3(8)	3C96
U2(4)	UPFH	U3(6)	3B27
U2(6)	52FB	U3(4)	755P
U2(10)	HC89	U3(5)	0001 (High, toggle with TP2 jumper removed. Replace jumper when finished.)

- b. A signature may be incorrect because that particular address line is being held low or high by another assembly connected to the address bus. (Only LA0, LA1, and LA2 go to other assemblies.) To check for this possibility, isolate these address lines from the other assemblies by opening the address bus switches on the A7 extender board. These are the top three switches of SW1 labeled A0, A1, A2.

6. The A7 logic circuitry will be checked in subgroups. Check each subgroup according to the following procedures. If any signature is incorrect, check the circuitry for that particular subgroup.

Subgroup I (U15B, U13, U17A, U4C, D):

- a. Check for the following signatures:

U15B(12)	7205
U15B(11)	5811H
U15B(10)	031A
U15B(9)	8876

- b. Place the logic probe on TP6. TP6 should now be High. Momentarily remove the jumper from TP2. TP6 should toggle with the jumper removed. Replace jumper.
- c. If these two tests are OK, proceed to Subgroup II; otherwise, troubleshoot Subgroup I. (SW1 on the A7 extender board can help isolate the LSEL lines in case a logic state is held by another board.)

Subgroup II (U6A, B, C, D, U16A, B, C, D, U15A):

- a. Check for the following signatures:

U6B(6)	29A6
U16A(12)	F56A
U6C(8)	12U3

- b. If the signatures are correct, proceed to Subgroup III; otherwise, troubleshoot Subgroup II using the signatures given immediately below:

U15A(4)	29A6
U15A(5)	5FL8
U15A(7)	6411P
U17B(6)	A1C4
U17D(11)	29A7
U16B(6)	3C97
U7A(1)	F56C

Subgroup III (U7C, D, U11A, B, U4A, F, U17B, C, U16C):

- a. Check the following points.

U7C(10)	Low
U4A(2)	A1C4
U11A(1)	0001 (toggling)

If these checks are correct, continue with step b. If not, use the following signatures to aid in troubleshooting.

Table B-18. A7 Microprocessor Troubleshooting (Continued)

U4A(1)	A1C5
U16C(11)	A1C4
U16C(10)	0001 (toggling)
U16C(9)	High
U11A(5)	High

- b. Jumper U7B(4) to ψ . (Do not use an extender pin clip on U7.) Monitor U7C(10) with 5004A data probe. Momentarily remove jumper from TP2 and push SW2 reset switch on extender board. 5004A should read "A1C5". A correct signature indicates that U7C is good and that U11A S, DC, and C inputs are functional. (U11A pin 1 should be High and pin 2 should be Low.) Replace TP2 jumper.

- c. With jumpers still connected, place an extender clip on U4 and jumper U4B(4) to ψ . Monitor U7C(10) with 5004A data probe. Remove jumper from TP2, push SW2 reset switch on extender board, and check the following points.

U7C(10)	A1C5
U11A(6)	A1C5
U11A(5)	A1C4

- d. If the signatures are correct, proceed to Step e. If not, use the following signatures to aid in troubleshooting — TP2 jumper removed.

U7D(13)	A1C4
U7D(12)	A1C5
U17C(9)	A1C4

- e. When finished, remove all jumpers except the one on TP2. TP2 should still be jumpered to ψ . Continue with Step 7.

7. The following procedure checks ROM U5.

- a. Place the 5004A START and STOP leads on the TPU5 test pin of the A7 extender board. Leave the other leads connected as before. Push the 5004A START button in (∇) and set the STOP slope to ∇ , out. The CLOCK slope is still set to ∇ . The A7U5 ROM output signatures should be as follows.

U5(9)	5A71
U5(10)	7024
U5(11)	1934
U5(13)	63FP
U5(14)	192P
U5(15)	9HP2
U5(16)	76H4
U5(17)	15U9

8. The following procedure checks ROM U8. Set up the 5004A as described in step 6 and connect the START/STOP leads to TPU8 of the A7 extender board. The A7U8 ROM output signatures should be as follows.

U8(9)	9738
U8(10)	A62A
U8(11)	333U
U8(13)	20A0
U8(14)	U8U7
U8(15)	0F55
U8(16)	0AHC
U8(17)	F32B

9. The circuits that remain to be checked are the Driver/Receiver U14 and RAM's U10 and U12. The RAM's should have been tested in the power up diagnostic, although a stuck data bus line would prevent any such test. Verifying the proper operation of U14 is most easily done by replacing the IC (U14 is in a socket).

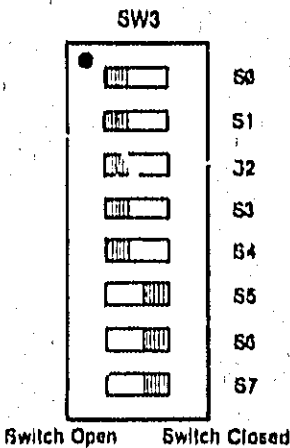
NOTE

When troubleshooting has been completed, be sure to remove jumper wires and set A7 data bus switches to their closed position for normal operation.

Table 8-19. A9 Interface Troubleshooting

A9

1. Check 5345A mainframe: A14 board P/N should be 05345-60044; A15 board P/N should be 05345-60045.
2. Place A7MPU and A9 Interface boards on their respective extender boards.
3. On A7 extender test board, set SW3 switches as shown and push the red toggle switch to generate a reset. This allows signature analysis of A9U14 through U18, U16 and U7 are also checked.



4. Connect 5004A Signature Analyzer as follows:
START/STOP leads to TP98 on A7 extender board,
CLOCK lead to A7TP5.
GND lead to ∇ on the A7 extender board.
Data probe GND lead to ∇ on the A7 extender board.

NOTE

Do not connect the ground leads to other than where described. Incorrect signatures may result.

Set 5004A controls as follows:

START to $\swarrow$

STOP/CLOCK to $\searrow$

The characteristic High signature is F834.

Check the following test points.

Test Point	Signature	Test Point	Signature
U18(2)	UC63	U15(3)	A26F
TP1 (U18 pin 3)	3357	U15(6)	P730
TP7 (U18 pin 6)	79AP	U15(11)	6CU1
U18(7)	C19A	U15(14)	2P52
U18(10)	U1CP		
U18(15)	8650		
CR1 Anode	8650		
CR1 Cathode	8650		

Table B-19. A9 Interface Troubleshooting (Continued)

Check that GATE CONTROL switch on rear of 5345 is set to INTERNAL position. Move switch to EXT GATE position; CR1 anode signature should now be "0000" (Low). U10(15) signature should not change. Return switch to INTERNAL position.

Test Point	Signature	Test Point	Signature
U17(3)	F800	U16(2)	2H45
U17(6)	6070	U16(3)	P571
U17(11)	C03U	U16(6)	7C5H
U17(14)	U05A	U16(10)	A4U9
U7(2)	593C	U7(1)	910U
		U6(10)	toggle
		U6(11)	toggle
		U6(9)	593C

If bad,
check
these
points

5. Check operation of U14 by the following method. (Data lines are available for probing on the A7 extender board; back of 5W4.)

D7 (U14 pin 3): Signature should be 3PA9.

With 5345A RESET button held in, signature should change to 3P28.

D6 (U14 pin 5): Signature should be 3514.

With 5345A FUNCTION switch set to FREQ A, signature should change to 3595.

Return FUNCTION switch to PLUG-IN.

D5 (U14 pin 7): Signature should be OP31.

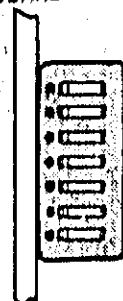
With 5345A FUNCTION switch set to START and Input switch set to CHECK, signature should change to OPCO.

Return FUNCTION to PLUG-IN, Input to SEP.

D4 (U14 pin 9): On 5345A A14 board, set BKPT-7 switch (rear switch of switch pack).

Signature should be A7F1.

5345A A14
BOARD



BREAKPOINT SWITCH
NORMAL POSITION

FRONT OF
5345A

NOTE

This signature should be slightly unstable. The next step will verify operation.

With 5345A RESET switch held in, signature should change to A740.

Return 5345A A14 BKPT-7 switch to normal position.

Table 8-19. A9 Interface Troubleshooting (Continued)

6. Check for the following signatures by using the correct setup method for each signature set. Use both methods.

Signature set A: These signatures are checked while the 5345A RESET button is held in. This forces the PROC BUSY line High and PTXMT High.

Signature set B: These signatures are checked with a jumper between TP1 and TP4 on the 5345A A15 board. This forces the PROC BUSY line Low.

Test Point	Signature Set A	Signature Set B
U3A(2)	Low	High
U7B(4)	Low*	—
U2C(8)	386P	Toggles
U2A(3)	2U04	6A58
U2D(11)	2U04	6A58
U6A(12)	A3F5	High
U10A(3)	F800	Low
U7E(10)	0034	F834
U3F(12)	Low*	Toggles
U3E(10)	U05A	Toggles
U2B(6)	386P	Toggles
U14(11)	High	Toggles
U14(13)	High	Toggles

*This line should toggle when RESET is released.

When finished, remove jumper between TP1 and TP4 in the 5345A.

7. Jumper A9 pin 10 (or U3 pin 13) to ground and check the following points with the 5345A RESET button held in.

Test Point	Signature
U19B(8)	386P
CR2 anode	386P

Leave jumper connected.

8. Jumper A9 pin 6 (or U7 pin 3) to ground and check the following points.

Test Point	Logic State
U14(11)	Low
U14(13)	Low
U19B(8)	High

Remove all jumpers.

9. On A7 extender test board, set SW3 switches as shown and push the red toggle switch SW2 to generate a reset.

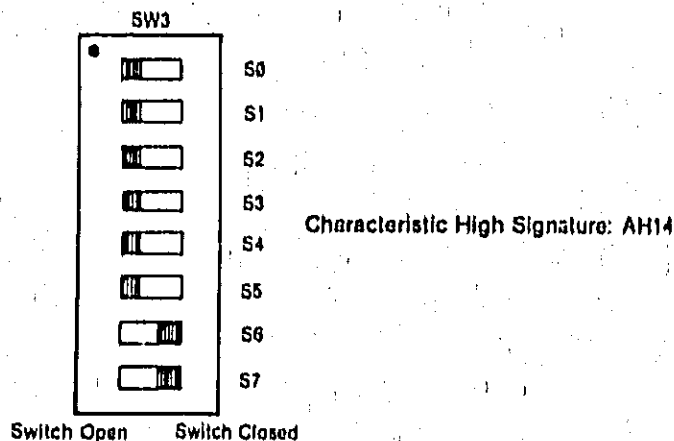


Table 8-19. A9 Interface Troubleshooting (Continued)

10. Set up signature analyzer as follows:

START/STOP leads to TP08 on A7 extender board

CLOCK lead to 5345A A15 TP7

GROUND lead to ∇ on A7 extender board

START to ⏏ , STOP/CLOCK to ⏏

11. Jumper 5345A A15 TP3 to TP4 to disable 5345A processor clock

Jumper 5345A A15 TP9 to 5355A A7 TP5 to provide the 5345A clock from the 5355A clock.

The characteristic high signature is A385.

The clock rate and thus reaction time of the 5004A is slow. Allow enough time to reach a stable signature situation. Check the following signatures:

A9 Signatures

U7C(6)	0000	U1B(8) — TP6	23U7
U3B(4)	PHH0	U10D(11)	23U7
U3C(6)	A247	U9(14)	920F
U4A(6) — TP4	6FA7	U9(13)	4CP6
U1A(12)	2235	U9(12)	A5C3
U7C(8)	A385	U9(11)	F529
U10C(8) — TP5	2235	U11(5)	4P92
U8A(6)	U60A	U11(7)	912H
U6B(6)	8A30	U11(9)	1UF5
U5A(5)	27F6	U11(11)	3531
U19A(6)	23U7	U13(13)	2986
U8B(8)	1198	U13(12)	PF4C
U7F(12) — TP2	C21H	U13(11)	2H02
U10B(6)	A1AU	U13(10)	U11A
U7D(8)	022A	U19(8)	A385
U4B(8)	A385		

NOTE

If the previous steps failed to uncover a failure on A9, run the following test. This test may also be used as a confidence test for the RAMs on A9.

12. On A7 extender test board, set SW3 switches as shown and push the red toggle switch SW2 to generate a reset. SW1 and SW4 should be closed (away from dot).

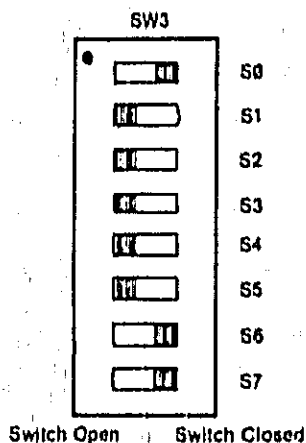


Table 8-19. A9 Interface Troubleshooting (Continued)

Explanation:

The plug-in is now set up to run a test routine that will check the proper operation of U13 and U11. Decimal point data is sent to U13 and a specific set of characters is written into RAM U11. These are then displayed on the 5345A in a rotating format: the decimal point moves right to left while the characters move left to right. The character set is:

0 1 2 3 4 5 6 7 8 9 . = 4 5 E b*

* b = blank

Not all characters can be seen at one time since there are 16 characters (16 RAM locations) and only 11 digits of display. Pushing the red toggle switch SW2 on the A7 extender board will start the decimal point at the LSD. See the following test pattern display for all possible display states.

13. Results of test routine:

- If the test pattern is properly displayed, U11, U13, and their drive circuits are functioning correctly. In this case, go to Step 13e of this procedure.
- If the test failed, either completely or partially, it is important to get the decimal point part of the routine working first. Unless the decimal point is moving across the display in all places, the remaining troubleshooting will not be reliable.
- If the decimal point is incorrect, the problem is probably in U13 or its associated drive circuits. Verify the proper operation of U13 by swapping U13 and U20, or by replacing U13 with a known good IC. Then run the test pattern again. If the decimal point sequence in the display is still bad, continue with Step 5.
- If the decimal point routine is correct, but the character routine is not, verify proper operation of U11 by swapping it with U12, or replace U11 with a known good IC. Then run the test pattern again. If the character sequence in the display is still bad, continue with Step 5. If not, replace the faulty IC.
- At this point, it is assumed the test routine is working properly. If so, check operation of U20 and U12 by turning off power to counter and swapping U13 with U20 and U11 with U12. (U11 and U13 have been proved good with this test.) Turn on counter. If U20 and U12 are good, the test routine will run as before. If so, continue with Step 5. If not, replace the faulty IC.

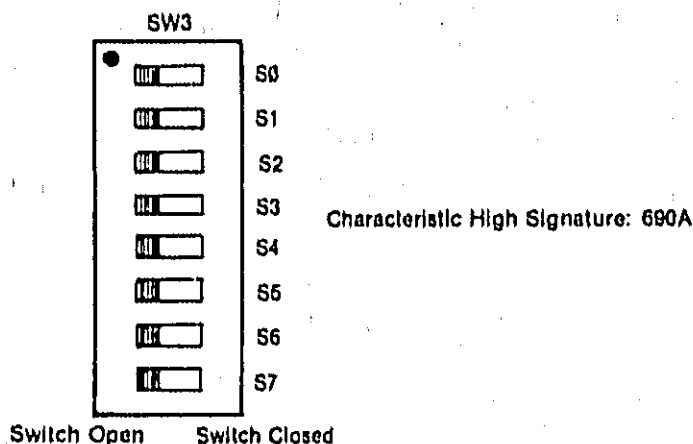
	11	10	9	8	7	6	5	4	3	2	1	← DISPLAY POSITIONS
1	4	5	6	7	8	9	.	=	4	5	E	← WHEN RESET PUSHED, THE DISPLAY WILL START HERE.
2	3	4	5	6	7	8	9	.	=	4	5	
3	2	3	4	5	6	7	8	9	.	=	4	
4	1	2	3	4	5	6	7	8	9	.	=	
5	0	1	2	3	4	5	6	7	8	9	.	
6		0	1	2	3	4	5	6	7	8	9	
7	E		0	1	2	3	4	5	6	7	8	
8	5	E		0	1	2	3	4	5	6	7	
9	4	5	E		0	1	2	3	4	5	6	
10	=	4	5	E		0	1	2	3	4	5	
11	.	=	4	5	E		0	1	2	3	4	
12	9	.	=	4	5	E		0	1	2	3	
13	8	9	.	=	4	5	E		0	1	2	
14	7	8	9	.	=	4	5	E		0	1	
15	6	7	8	9	.	=	4	5	E		0	
16	5	6	7	8	9	.	=	4	5	E		

Table 8-20. A3 Filter Detector Troubleshooting

CAUTION

A2 and A3 are connected together by an SMC-to-SMC adapter. Do not apply stress to adapter when removing assemblies.

1. If the 5345A does measure the signal (Step 7a, Table 8-10) remove A2 and A3 together. Remove the SMC adapter and place A3 on an extender board. Inject a pulsed RF signal into A3J1 of about 200 MHz (within the IF bandwidth) at 0 dBm. If the counter measures this signal while still in CW mode, check for toggling at TPJ. Check for a TTL High at TPA. Also check U2 buffer output on the D0 line.
2. If the 5345A does not measure the signal, (Step 7b, Table 8-10) push the PULSE button. The counter should now make a measurement and display the correct frequency. If the unit miscounts at higher input levels, check the AGC circuits on A2. See Table 8-13, Step 3d. These circuits are active only in this mode. If the unit fails to make a measurement, use the following procedure to troubleshoot A3.
 - a. Carefully remove A2 and A3 together.
 - b. Remove the adapter and place A3 on an extender board. Inject a pulsed RF signal into A3J1 of about 200 MHz (within the IF bandwidth) at 0 dBm. Check for toggling at TPJ, TPA, and TPC.
3. The following procedure is primarily concerned with the logic gates that provide status information to the processor. In checking these gates, input signals are used that also exercise other portions of the board. Although this provides a good test of the board, it does not test the circuits fully: IF outputs, GATE OUT, and bandwidth, for example.
4. Connect 5004A as follows: place A7 on extender test board 05355-60025, connect START/STOP leads to TP96 of A7 extender test board, CLOCK lead to A7TP5, and GND lead to ∇ .
5. Set 5004A controls as follows:
 START to f
 STOP/CLOCK to f
6. On A7 extender test board, set SW3 switches as shown and push the red toggle switch to generate a reset. This allows signature checks of A3 U2 and U3, under RF HEAD INPUT conditions.



Using an 8620C Sweep Oscillator (if possible), inject a 1.5 GHz signal into the converter head and check for the following signatures as indicated.

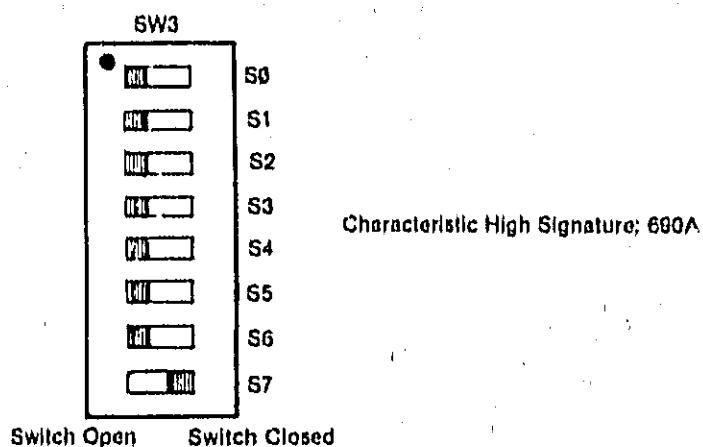
NOTE

Input frequency must be 1.5 GHz or the following procedure will not work properly. Signatures can be checked from bottom of instrument.

Table 8-20. A3 Filter Detector Troubleshooting (Continued)

Test Point	Signature With CW RF On	Signature With CW RF Off	Signature With Pulsed RF Input (8620C Rear Panel 1 kHz Switch)
D1, A3(4)	High	923A	Toggling
D0, A3(4)	High	923A	923A
D2, A3(5)	923A	High	923A

7. On A7 extender test board, set SW3 switches as shown and push the red toggle switch to generate a reset. This allows signature checks of A3 U2 and U3 under prescaler input conditions.



Using an 8620C Sweep Oscillator (if possible), inject a 1.5 GHz signal into the prescaler input and check for the following signatures as indicated.

Test Point	Signature With CW RF On	Signature With CW RF Off	Signature With Pulsed RF Input (8620C Rear Panel 1 kHz Switch)
D4, A3(3)	923A	High	923A
D0, A3(4)	High	923A	923A

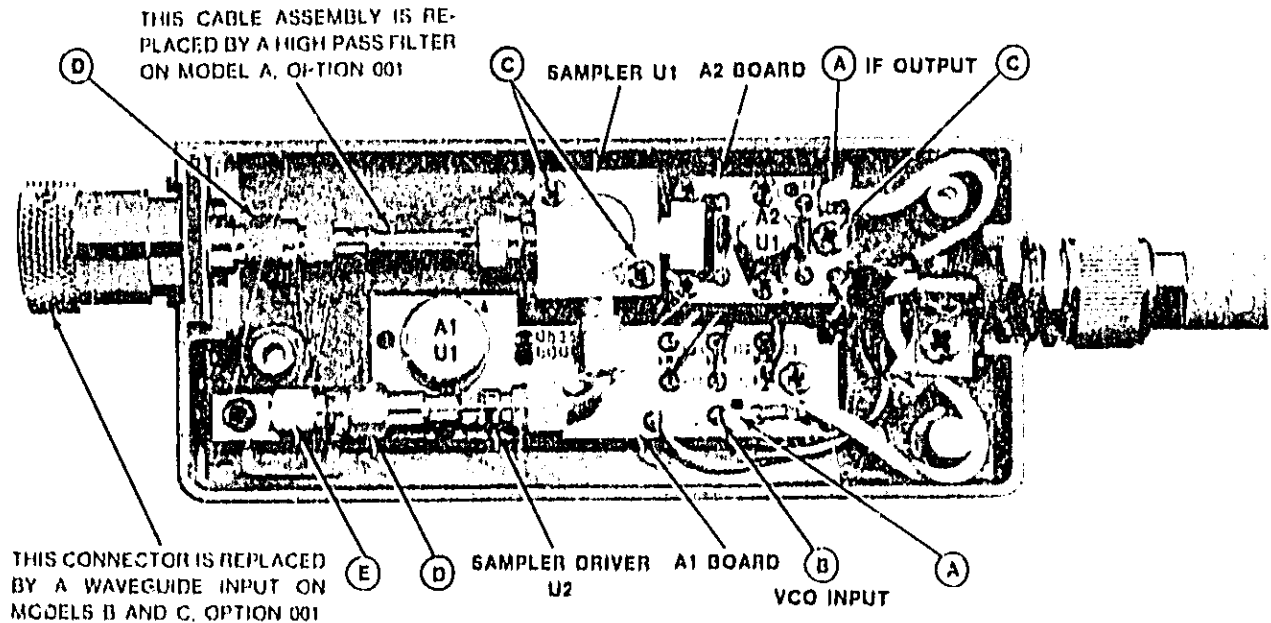
Table B-21. 5356A/B/C Frequency Converter Head Troubleshooting

1. Remove the 5356 cable connector from the 5355A input connector and inspect the connector pins for bent or pushed in contacts. Of particular importance are the two coaxial contacts, as these carry high frequency signals (VCO output and IF input) between the 5355A and the 5356. If any pins are bent, carefully straighten them with needle-nose pliers or a sharp pointed tool. If a pin is bent more than once, breakage will probably occur. If the pin is just off-center, straighten it with a pair of tweezers.

NOTE

This connector is NOT field repairable. If any pins are broken, the entire head must be returned to the factory for repair. This is due to the special crimping tools required for repair. An alternative to this is to replace the entire cable. Observe proper connections and ground clamps inside the head during cable replacement.

2. Disassemble the 5356 as described below: See photo below for an internal view of the 5356.



- a. Remove the three socket-head screws holding the two halves of the 5356 together.
- b. LOOSEN the hex nut between the cable strain relief and the 5356 housing.
- c. Remove the top half of the housing to expose the internal circuitry.
- d. Carefully inspect the assemblies for foreign matter, especially near the coaxial connections. Any dirt, flux, or other debris can cause failure of the 5356 exhibited by poor sensitivity. Note points "A" in the 5356 photo.
- e. The 5356 is supplied +15 and -5 volts by the 5355A. Any shorts in the 5356 cable or inside the 5356 itself will cause the 5355A to malfunction. If the 5355A will operate in PRESCALE mode with the 5356 head removed, but won't operate with it installed, suspect a shorted cable or a wiring fault in the 5356. Refer to the 5356 schematic diagram, Figure B-41.

Table 8-21. 5356A/B/C Frequency Converter Head Troubleshooting (Continued)

3. Connect the 5356 to the 5355A and check the VCO signal (supplied to the 5356 by the 5355A) as follows:
 - a. Connect a spectrum analyzer at the point where the coaxial cable connects to A1 board in the 5356, point "B", in 5356 photo.
 - b. Set the 5355A into the MANUAL mode, and set a MANUAL center frequency of 1.5 GHz.
 - c. The spectrum analyzer should display a signal of 805.2 MHz at approximately +10 dBm.
 - d. Other VCO frequencies may be checked by setting a center frequency of 2.7 GHz for a VCO frequency of 981.2 MHz, and 1.9 GHz for 1056.0 MHz.
 - (1) If the signal is present, proceed to Step 4.
 - (2) If the signal is NOT present, suspect the cable, connector, or the 5355A itself. See Table 8-15.

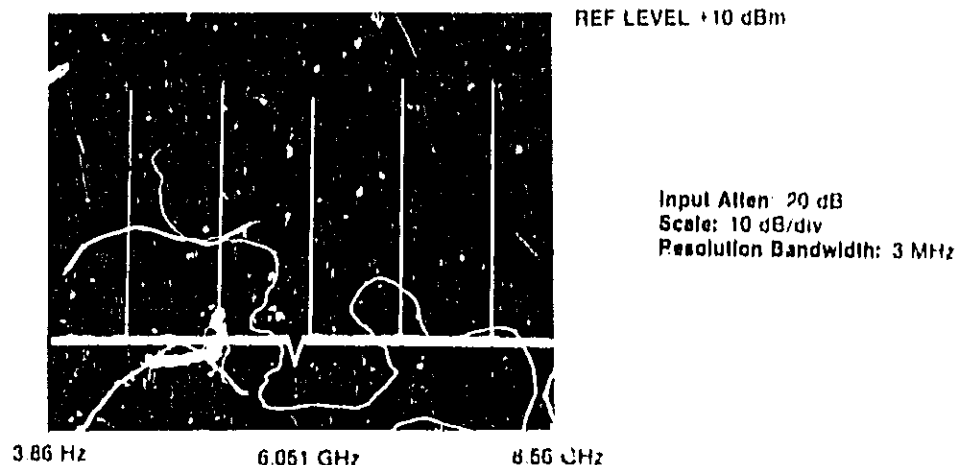
4. Check the output of A1U1, as follows:

- a. Remove U1 (sampler) and U2 (sampler driver) as a unit, as follows:
 - (1) Remove two pozidriv screws retaining U1, photo point "C".
 - (2) Remove the pozidriv screw near A2C5, photo point "C".
 - (3) LOOSEN the coaxial fitting at the input to U2, photo point "D". Loosen coaxial fitting at 5356 input connector, photo point "D". Don't remove completely. Rotate the U1/U2/A2 assembly upward, if the 5356 is equipped with a coaxial input. If waveguide equipped, rotation is not necessary.
 - (4) Disconnect A2 from U1 by pulling the two assemblies apart in a STRAIGHT LINE. DO NOT TWIST OR PULL AT AN ANGLE — TO DO SO WILL DAMAGE THE CONNECTOR!!!
 - (5) Remove the input connector assembly (coax or waveguide) at the input of U1.

NOTE

Observe Waveguide support blocks — don't misplace them, as they will be needed at reassembly.

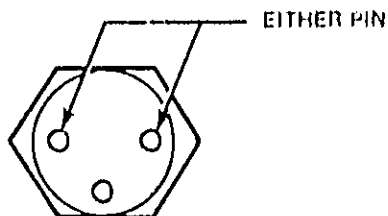
- (6) Continue loosening the coax fitting at the input to U2. Remove U1 and U2 as a unit.
 - (7) Check the signal at the output of A1 with the spectrum analyzer, photo point "E". Observe a signal of $\approx +20$ dBm.
 - b. If the signal is present, proceed to Step 5.
 - c. If the signal is NOT present, replace amplifier A1U1. Amplifier U1 is socket mounted, and easily unplugs for replacement.
5. To check U2 sampler driver, separate U2 from sampler U1 at U1, and reinstall at coax connection on the A1 board, photo point "E". Leave the 90 degree bend on U2 to facilitate connection to the spectrum analyzer.
- a. Using the spectrum analyzer, observe a harmonic comb signal similar to that shown below. Place 5355A in MANUAL mode.



- b. If NO harmonic comb is present, replace U2 sampler driver.
- c. If the harmonic comb is present, proceed to Step 6.

Table 8-21. 5356A/B/C Frequency Converter Head Troubleshooting (Continued)

6. This step will isolate amplifier A2U1 or the sampler U1 as the defective component. Proceed as follows:
 - a. Inject a 300 MHz signal at -40 dBm into A2J1. Use a 10 to 50 pF capacitor to couple the signal, to guard against the possibility of dc levels upsetting either the bias to A2U1 or the signal generator. See figure below.



- b. Check for the presence of a signal at the input to A2 in the 5355A. Refer to the overall block diagram, Figure 8-27. Disconnect the cable between the 5355A RF HEAD INPUT connector and the A2 assembly in the 5355A at A2J1. Couple the spectrum analyzer to this cable. For A and B model heads the level should be 25 dB above the test signal applied. For C model head the level should be 30 dB above the test signal applied.
 - c. If the signal is present, carefully inspect the coax connection. (Inspect the video filter that is used in the 5356A option 001). If all these checks prove okay, replace the sampler U1.
 - d. If the signal is NOT present, troubleshoot 5356 A2 to find the fault.

Table 8-21A. 5356 Frequency Ranges and Connectors

FREQUENCY	HEAD	CONNECTOR	HEAD CODE	*HEAD CODE WIRING		
				C ID1 YELLOW	B ID2 GREEN	A ID3 BLUE
1.5--18 GHz	5356A (and 5356A, Option 001)	N	0	0	0	0
1.5--26.5 GHz	5356B	SMA	1	0	0	1
18--26.5 GHz	5356B Option 001	WG WR-42	2	0	1	0
1.5--40 GHz	5356C	APC-3.5	4	1	0	0
26.5--40 GHz	5356C Option 001	WG WR-28	5	1	0	1

*NOTE:

- 1 = floating lead
0 = grounded lead

8-202. LOGIC SYMBOLS

8-203. Logic symbols used in this manual conform to the American National Standard ANSI Y32.14-1973 (IEEE Std. 91-1973). This standard supersedes MIL-STD-806B. In the following paragraphs logic symbols are described. For further descriptions refer to IEP Logic Symbology manual, part number 5951-6116.

8-204. Logic Concepts

8-205. The binary numbers 1 and 0 are used in pure logic where 1 represents true, yes, or active and 0 represents false, no, inactive. These terms should not be confused with the physical quantity (e.g., voltage) that may be used to implement the logic, nor should the term "active" be confused with a level that turns a device on or off. A truth table for a relationship in logic shows (implicitly or explicitly) all the combinations of true and false input conditions and the result (output). There are only two basic logic relationships, AND and OR. The following illustrations assume two inputs (A and B), but these can be generalized to apply to more than two inputs.

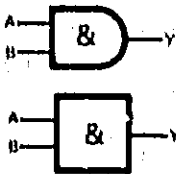
AND Y is true if and only if A is true and B is true (or more generally, if all inputs are true).
Y=1 if and only if A=1 and B=1
 $Y=A \cdot B$

OR Y is true if and only if A is true or B is true (or more generally, if one or more input(s) is (are) true).
Y=1 if and only if A=1 or B=1
 $Y=A + B$

TRUTH TABLE

A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

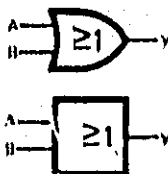
EQUIVALENT
SYMBOLS



TRUTH TABLE

A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

EQUIVALENT
SYMBOLS



8-206. Negation

8-207. In logic symbology, the presence of the negation indication symbol $\circ$ provides for the presentation of logic function inputs and outputs in terms independent of their physical values, the 0-state of the input or output being the 1-state of the symbol referred to the symbol description.

EXAMPLE 1



TRUTH TABLE

A	B	Z
1	1	0
1	0	1
0	1	1
0	0	1

EXAMPLE 2



TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

EXAMPLE 3



TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

EXAMPLE 4



TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

- EXAMPLE 1 says that Z is not true if A is true and B is true or that Z is true if A and B are not both true. $Z = \overline{AB}$ or $Z = \overline{A} \overline{B}$. This is frequently referred to as NAND (for NOT AND).
- EXAMPLE 2 says that Z is true if A is not true or if B is not true. $Z = \overline{A} \overline{B}$. Note that this truth table is identical to that of Example 1. The logic equation is merely a DeMorgan's transformation of the equations in Example 1. The symbols are equivalent.
- EXAMPLE 3 $Z = A + B$ or $Z = \overline{\overline{A} \overline{B}}$ and,
- EXAMPLE 4 $Z = \overline{\overline{A} \overline{B}}$, also share common truth table and are equivalent transformations of each other. The NOT OR form (Example 3) is frequently referred to as NOR.

NOTE

In this manual the logic negation symbol is NOT used.

8-208. Logic Implementation and Polarity Indication

- 8-209. Devices that can perform the basic logic functions, AND and OR, are called gates. Any device that can perform one of these functions can also be used to perform the other if the relationship of the input and output voltage levels to the logic variables 1 and 0 is redefined suitably.
- 8-210. In describing the operation of electronic logic devices, the symbol H is used to represent a "high level", which is a voltage within the more-positive (less-negative) of the two ranges of voltages used to represent the binary variables. L is used to represent a "low level", which is a voltage within the less-positive (more-negative) range.
- 8-211. A function table for a device shows (implicitly or explicitly) all the combinations of input conditions and the resulting output conditions.
- 8-212. In graphic symbols, inputs or outputs that are active when at the high level are shown without polarity indication. The polarity indicator symbol $\triangle$ denotes that the active (one) state of an input or output with respect to the symbol to which it is attached is the low level.

NOTE

The polarity indicator symbol " $\triangle$ " is used in this manual.

- EXAMPLE 5 assume two devices having the following function tables.

DEVICE #1
FUNCTION TABLE

A	B	Y
H	H	H
H	L	L
L	H	L
L	L	L

DEVICE #2
FUNCTION TABLE

A	B	Y
H	H	H
H	L	H
L	H	H
L	L	L

- POSITIVE LOGIC by assigning the relationship $H=1, L=0$ at both input and output, Device #1 can perform the AND function and Device #2 can perform the OR function. Such a consistent assignment is referred to as positive logic. The corresponding logic symbols would be:

DEVICE #1



DEVICE #2



NEGATIVE LOGIC alternatively, by assigning the relationship $H=0, L=1$ at both input and output, Device #1 can perform the OR function and Device #2 can perform the AND function. Such a consistent assignment is referred to as negative logic. The corresponding logic symbols would be:



B-213. MIXED LOGIC. The use of the polarity indicator symbol ($\triangle$) automatically invokes a mixed-logic convention. That is, positive logic is used at the inputs and outputs that do not have polarity indicators, negative logic is used at the inputs and outputs that have polarity indicators.

**EXAMPLE 6
FUNCTION TABLE**

A	B	Z
H	H	L
H	L	H
L	H	H
L	L	H

This may be shown either of two ways:

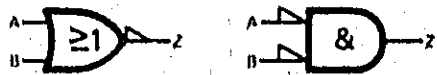


Note the equivalence of these symbols to examples 1 and 2 and the fact that the function table is a positive-logic translation ($H=1, L=0$) of the NAND truth table, and also note that the function table is the negative-logic translation ($H=0, L=1$) of the NOR truth table, given in Example 3.

**EXAMPLE 7
FUNCTION TABLE**

A	B	Z
H	H	L
H	L	L
L	H	L
L	L	H

This may be shown either of two ways:



Note the equivalence of these symbols to examples 3 and 4 and the fact that the function table is a positive-logic translation ($H=1, L=0$) of the NOR truth table, and also note that the function table is the negative-logic translation ($H=0, L=1$) of the NAND truth table, given in Example 1.

B-214. It should be noted that one can easily convert from the symbology of positive-logic merely by substituting a polarity indicator ($\triangle$) for each negative indicator ($\circ$) while leaving the distinctive shape alone. To convert from the symbology of negative-logic, a polarity indication ($\triangle$) is substituted for each negation indicator ($\circ$) and the CR shape is substituted for the AND shape or vice versa.

B-215. It was shown that any device that can perform OR logic can also perform AND logic and vice versa. DeMorgan's transformation is illustrated in Example 1 through 7. The rules of the transformation are:

1. At each input or output having a negation ($\circ$) or polarity ($\triangle$) indicator, delete the indicator.
2. At each input or output not having an indicator, add a negation ($\circ$) or polarity ($\triangle$) indicator.
3. Substitute the AND symbol $\text{D-shape with } \&$ for the OR symbol $\text{D-shape with } \geq 1$ or vice versa.

These steps do not alter the assumed convention; positive-logic stays positive, negative-logic stays negative, and mixed-logic stays mixed.

B-216. The choice of symbol may be influenced by these considerations: (1) The operation being performed may best be understood as AND or OR. (2) In a function more complex than a basic gate, the inputs will usually be considered as inherently active high or active low (e.g., the J and K inputs of a J-K flip-flop are active high and active low, respectively). (3) In a chain of logic, understanding and the writing of logic equations are often facilitated if active low or negated outputs feed into active low or negated inputs.

B-217. Other Symbols

B-218. Additional symbols are required to depict complex logic diagrams, as follows:



Dynamic input activated by transition from a low level to a high level. The opposite transition has no effect at the output.



Dynamic input activated by transition from a high level to a low level. The opposite transition has no effect at the output.



Exclusive OR function. The output will assume its indicated active level if and only if one and only one of the two inputs assumes its indicated active level.



Inverting function. The output is low if the input is high and it is high if the input is low. The two symbols shown are equivalent.



Noninverting function. The output is high if the input is high and it is low if the input is low. The two symbols shown are equivalent.



OUTPUT DELAY. The output signal is effective when the input signal returns to its opposite state.



EXTENDER. Indicates when a logic function increases (extends) the number of inputs to another logic function.



FLIP-FLOP. A binary sequential element with two stable states; a set (1) state and a reset (0) state. Outputs are shown in the 1 state when the flip-flop is set. In the reset state the outputs will be opposite to the set state.



RESET. A 1 input will reset the flip-flop. A return to 0 will cause no further effect.



SET. A 1 input will set the flip-flop. A return to 0 will cause no further action.



TOGGLE. A 1 input will cause the flip-flop to change state. A return to 0 will cause no further action.



J INPUT. Similar to the S Input except if both J and K (see below) are at 1, the flip-flop changes state.



K INPUT. Similar to the R Input (see above).



D INPUT (Data). Always dependent on another input (usually C). When the C and D inputs are at 1, the flip-flop will be set. When the C is 1 and the D is 0, the flip-flop will reset.



Address symbol has multiplexing relationship at inputs and demultiplexing relationship at outputs.

8-219. Dependency Notation "C" "G" "V" "F"

8-220. Dependency notation is a way to simplify symbols for complex IC elements by defining the existence of an AND relationship between inputs, or by the AND conditioning of an output by an input without actually showing all the elements and interconnections involved. The following examples use the letter "C" for control and "G" for gate. The dependent input is labeled with a number that is either prefixed (e.g., 1X) or subscripted (e.g., X₁). They both mean the same thing. The letter "V" is used to indicate an OR relationship between inputs or between inputs and outputs with this letter (V). The letter "F" indicates a connect-disconnect relationship. If the "F" (free dependency) inputs or outputs are active (1) the other usual normal conditions apply. If one or more of the "F" inputs are inactive (0), the related "F" output is disconnected from its normal output condition (it floats).



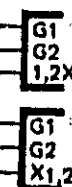
The input that controls or gates other inputs is labeled with a "C" or a "G", followed by an identifying number. The controlled or gated input or output is labeled with the same number. In this example, "1" is controlled by "G1".



When the controlled or gated input or output already has a functional label (X is used here), that label will be prefixed or subscripted by the identifying number.



If a particular device has only one gating or control input then the identifying number may be eliminated and the relationship shown with a subscript.



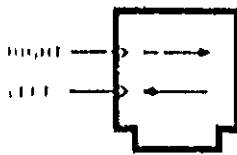
If the input or output is affected by more than one gate or control input, then the identifying numbers of each gate or control input will appear in the prefix or subscript, separated by commas. In this example "X" is controlled by "G1" and "G2".

B-221. Control Blocks

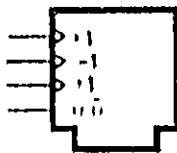
B-222. A class of symbols for complex logic are called control blocks. Control blocks are used to show where common control signals are applied to a group of functionally separate units. Examples of types of control blocks follow.



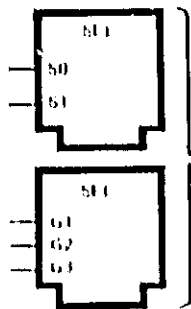
Register control block. This symbol is used with an associated array of flip-flop symbols to provide a point of placement for common function lines, such as a common clear.



Shift register control block. These symbols are used with any array of flip-flop symbols to form a shift register. An active transition at the inputs causes left or right shifting as indicated.



Counter control block. The symbol is used with an array of flip-flops or other circuits serving as a binary or decade counter. An active transition at the +1 or -1 input causes the counter to increment one count upward or downward, respectively. An active transition at the +1 input causes the counter to increment one count upward or downward depending on the input at an up/down control.



Selector control block. These symbols are used with an array of OR symbols to provide a point of placement for selection (S) or gating (G) lines. The selection lines enable the input designated 0, 1, ..., n of each OR function by means of a binary code where S0 is the least significant digit. If the 1 level of these lines is low, polarity indicators (∇) will be used. The gating lines have an AND relation with the respective input of each OR function: G1 with the inputs numbered 1, G2 with the input numbered 2, and so forth. If the enabling levels of these lines is low, polarity indicators (∇) will be used.



Output selector control block. This symbol is used with a block symbol having multiple outputs to form a decoder. The selection lines enable the output designated 0, 1, ..., n of each block by means of a binary code where S0 is the least significant digit. If the 1 level of these lines is low, polarity indicators (∇) will be used.

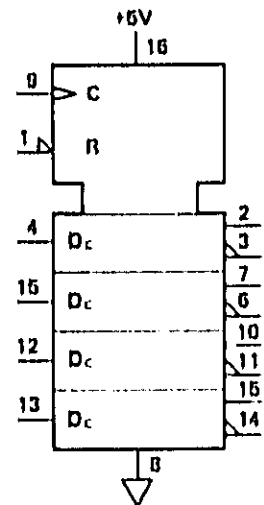
B-223. Complex Logic Devices

B-224. Logic elements can be combined to produce very complex devices that can perform more difficult functions. A control block symbol can be used to simplify understanding of many complex devices. Several examples of complex devices are given here. These examples are typical of the symbols used in schematic diagrams in this manual.

Description

QUAD D-TYPE FLIP-FLOPS

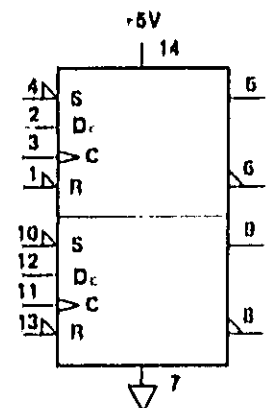
Data at the D_c inputs is transferred to the outputs on the positive-going edge of the clock pulse (pin 9). A low signal at the reset (pin 1) will clear all FFs.



Description

DUAL D-TYPE FLIP-FLOP

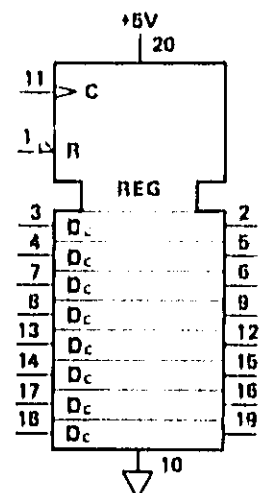
The dual D-type flip-flop consists of two independent D-type flip-flops. The information present at the data (D_c) input is transferred to the active-high and active-low outputs on a low-to-high transition of the clock (C) input. The data input is then locked out and the outputs do not change again until the next low-to-high transition of the clock input. The set (S) and reset (R) inputs override all other input conditions: when (S) is low, the active-high output is forced high; when reset (R) is low, the active-high output is forced low. Although normally the active-low output is the complement of the active-high output, simultaneous low inputs at the set and reset will force both the active-low and active-high outputs to go high at the same time on some D-type flip-flops. This condition will exist only for the length of time that both set and reset inputs are held low. The flip-flop will return to some indeterminate state when both the set and reset inputs are returned to the high state.



Description

OCTAL D-TYPE FLIP-FLOP

Data at the D_c input of each flip-flop is transferred to the output on the positive-going edge of the clock pulse. A low signal at the reset (pin 1) will clear all flip-flops.

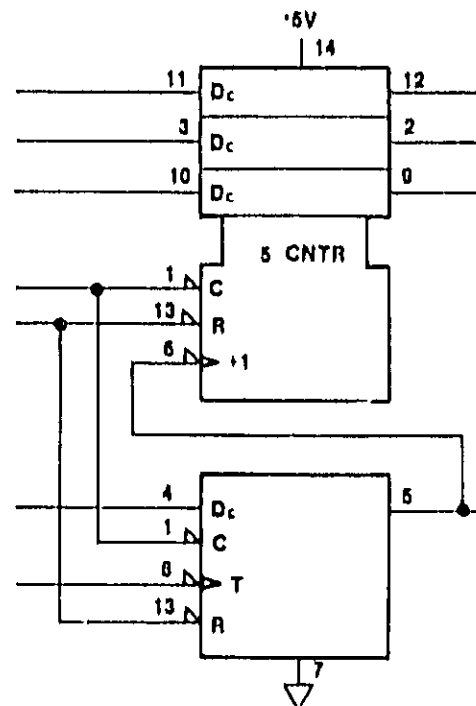


Model 5355A Service

Description 50/30 MHz PRESETTABLE DECADE COUNTER/LATCH

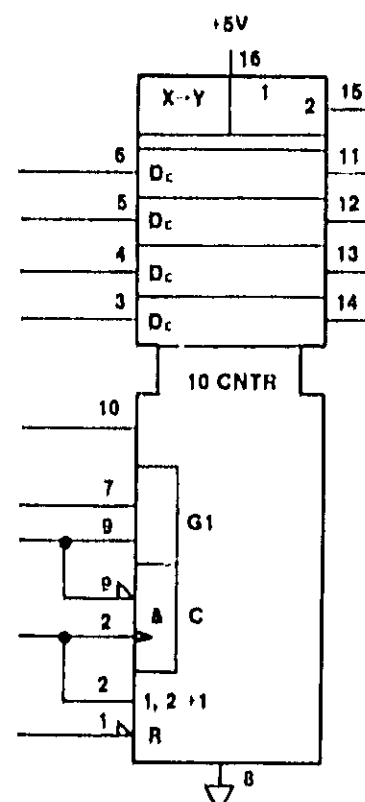
The Decade Counter consists of a divide-by-2 and a divide-by-5 counter formed by connecting pin 5 to pin 6 and taking the output from pin 12.

The outputs may be preset to any state by making "C" active low and entering the desired data at the "D_c" inputs. The outputs at pins 5, 9, 2, and 12 will then correspond to the data inputs independent of the state of the count-up clocks at pins 6 and 8. An active high signal at pin 1 then enables the counter by latching the parallel data into the counter. The count-up clock at pin 8 clocks the ÷2 counter and pin 6 clocks the ÷5 counter. When the counter is clocked at pins 8 or 6, the outputs will change on the negative-going edge of the signal. An active low at the "R" (reset) input (pin 13) causes all the outputs to go low independent of the counting state.



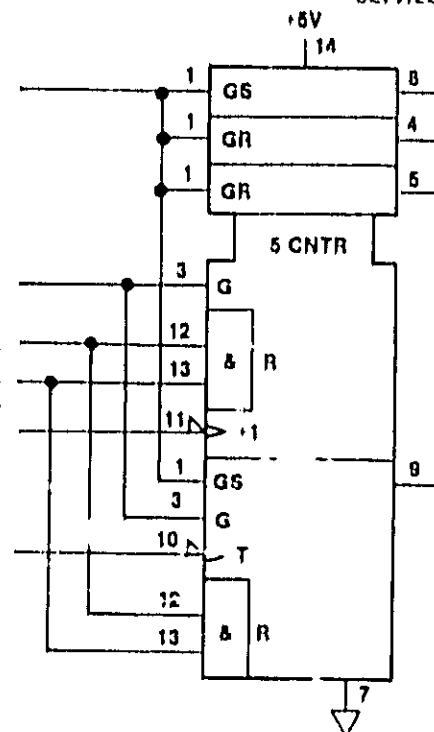
Description SYNCHRONOUS DECADE COUNTER

This synchronous presettable decade counter has four master slave flip-flops that are triggered on the positive-going edge of the clock pulse (pin 2). A LOW at the load input (pin 9) disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels at the enable inputs (pins 7 and 10). The clear function (pin 1) is asynchronous and a low level clear input sets all outputs low regardless of the levels of the clock, load or enable inputs. Both count enable inputs (pins 7 and 10) must be HIGH to count and the pin 10 input is fed forward to enable the carry output (pin 15).



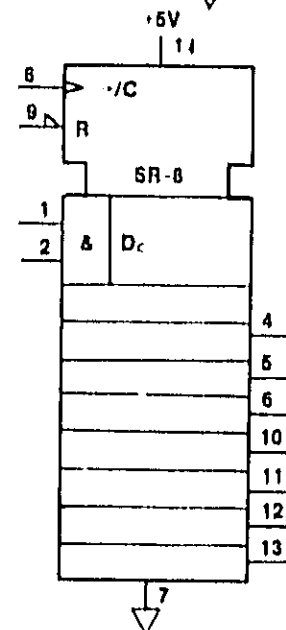
Description DECADE COUNTER

The decade counter has four master slave flip-flops and gating for which the count cycle length is divided-by-5. This counter has a gated zero reset and a gated set-to-nine input. To use the maximum count length, the pin 11 input is connected to the pin 9 output. The input count pulses are applied to the T input at pin 10. A symmetrical divide-by-10 count can be obtained by connecting the pin 8 output to the pin 10 input and applying the input count to the pin 11 input to obtain a divide-by-10 square wave at the pin 9 output.



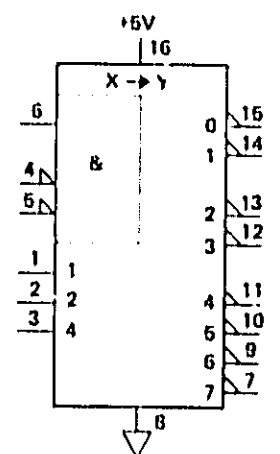
Description 8-BIT PARALLEL OUT SERIAL SHIFT REGISTER

This 8-bit shift register has gated serial inputs and an asynchronous clear. A LOW at one or both gated serial inputs (pins 1, 2) inhibits entry of data and resets the first FF to the low level at the next clock pulse (pin 8). A high-level input (pin 1 or 2) enables the other input which will then determine the state of the first FF. Data is serially shifted in and out of the 8-bit register during the positive-going transition of the clock pulse. Clear is independent of the clock and occurs when pin 9 is LOW.



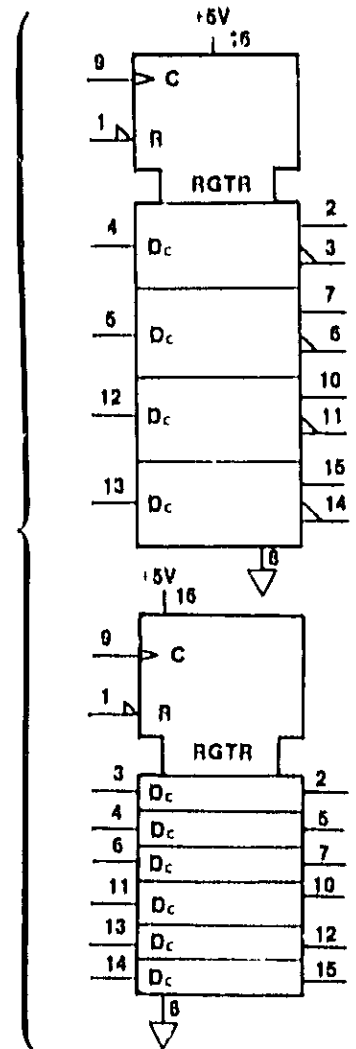
Description DECODER

The binary-weighted inputs are decoded to provide the output when enable input pins 4 and 5 are low and 6 is high.



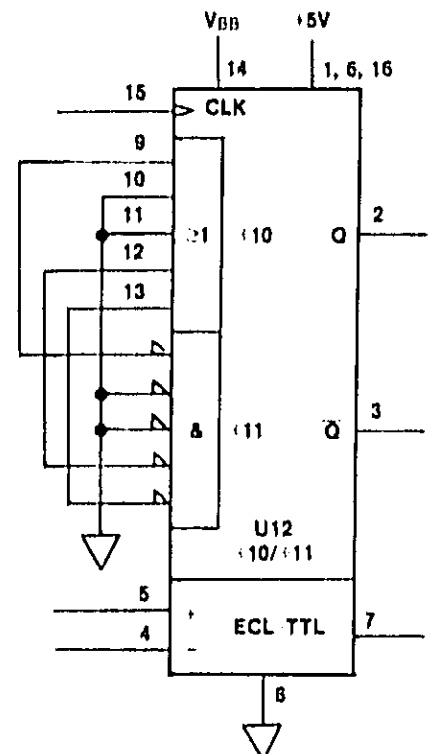
Description
HEX/QUAD D-TYPE FLIP-FLOPS

Information at the D inputs is transferred to the outputs on the positive-edge of the clock pulse (pin 9). Clock triggering occurs at a particular voltage level. The hex FFs have single outputs, the quad FFs have complementary outputs.



Description
2-MODULUS PRESCALER

The 2-modulus prescaler will divide-by-10 or 11. Division by 10 occurs when any one or all of the gate inputs (pins 9, 10, 11, 12, 13) are high. Division by 11 occurs when all of these inputs are low. Pins 4 and 5 provide a differential input to a separate circuit which acts as an ECL to TTL translator with output at pin 7.



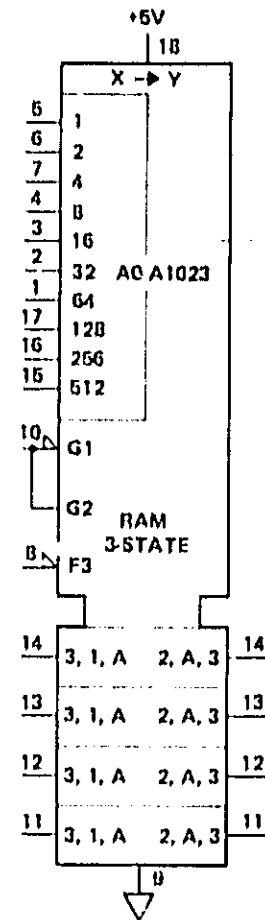
Description

RAM (WITH IDENTICAL INPUT/OUTPUT PINS)

Random-Access memory with possible access to 1024 locations. Address selection is determined by the 10 address input codes in the upper left corner of the control block. These address codes are weighted to correspond to the possible addresses (A0-1023).

G1 and G2 are the read and write enables. A low on Pin 10 will enable G1 or the input function. A high on Pin 10 will enable G2 or the output function. F3 is the three-state enable line. A low on pin 8 will enable data to be read and written.

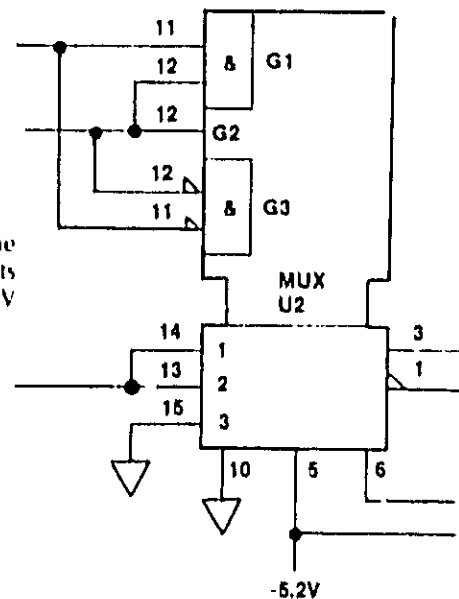
The output lines are noted in the lower right portion of the symbol. "3" indicates that these outputs are enabled by a low on F3. "2" indicates that information will be written out of the chip when G2 is enabled at the memory location addressed.



Description

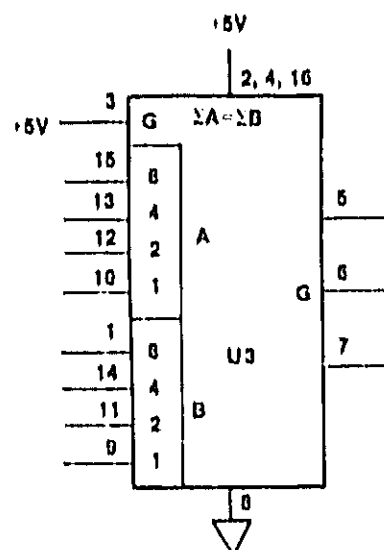
3 INPUT MULTIPLEXER

One of the three inputs (1, 2, or 3) at pins 14, 13, or 15, respectively, will be output according to the logic state of the control lines (pins 11 and 12). The outputs (pins 3 and 1) are complimentary, open collector. Pin 6 is connected to -5.2V through a resistor for external biasing.



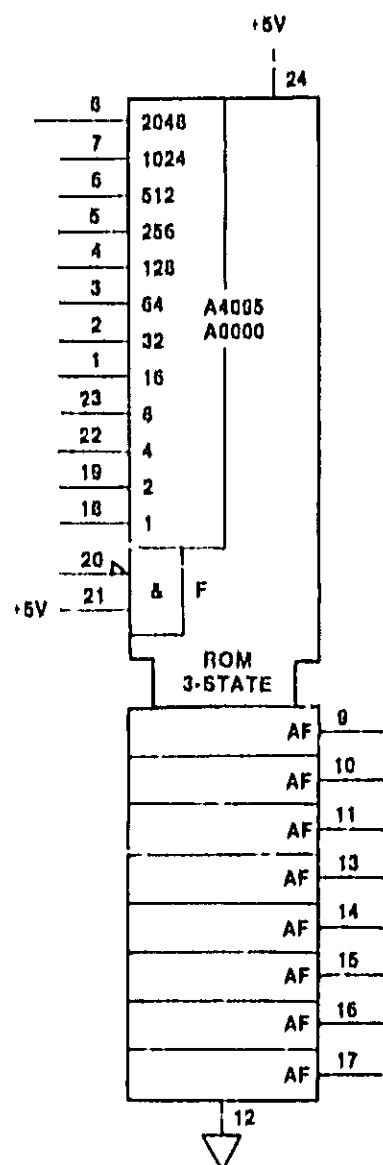
Description **4-BIT MAGNITUDE COMPARATOR**

The comparator compares the 4-bit weighted inputs at A and B which (in this application), represents a comparison of the address switch settings with the HP-IB DIO1 through DIO4 lines. When a match occurs ($A=B$), the LISTEN output (pin 6) is sent to the HP-IB circuits to initiate the listen mode.



Description **4K x 8 ROM**

Read Only Memory with 4096 addresses. Address selection is determined by the 12-bit address input in the upper left corner of the control block. A high on pin 21 and a low on pin 20 enables the three-state (F) outputs for the addressed memory location.



B-225. ASSEMBLY LOCATIONS

B-226. Figures B-22, B-23, B-24, B-25, and B-26 show the front, rear, top, bottom and motherboard (top), respectively of the 5355A. The front and rear views show reference designator of the front and rear panel controls, connectors and indicators. The top view shows assembly locations and adjustments. The remaining photos show the bottom and top view of the motherboard.

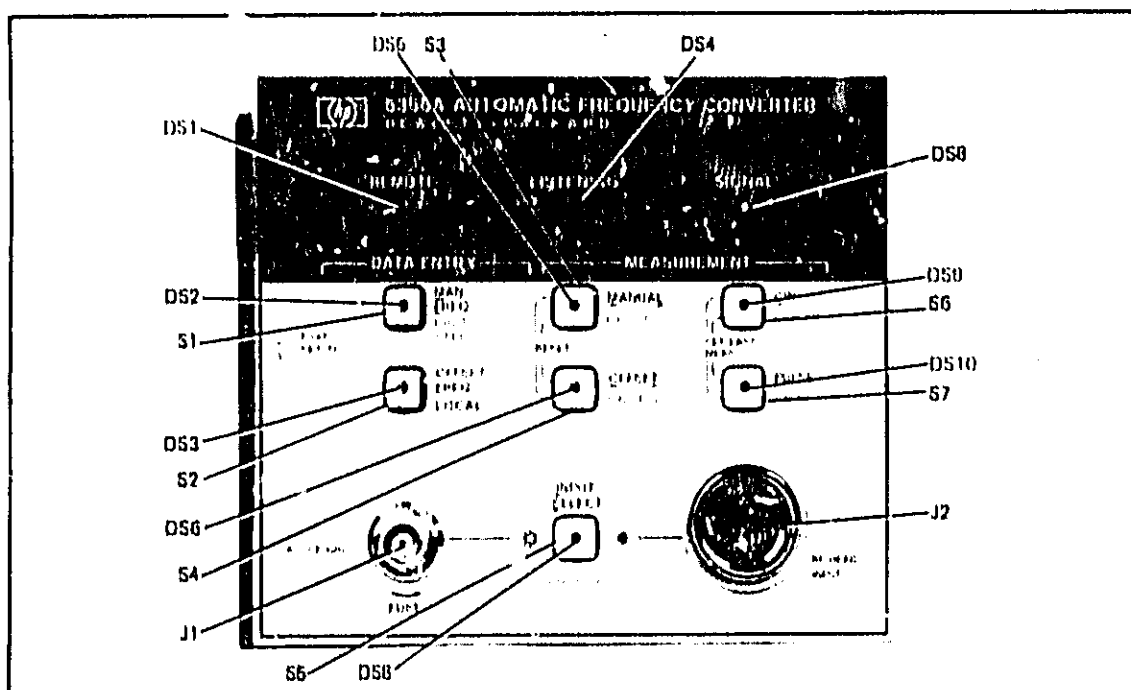


Figure B-22. 5355A Front View

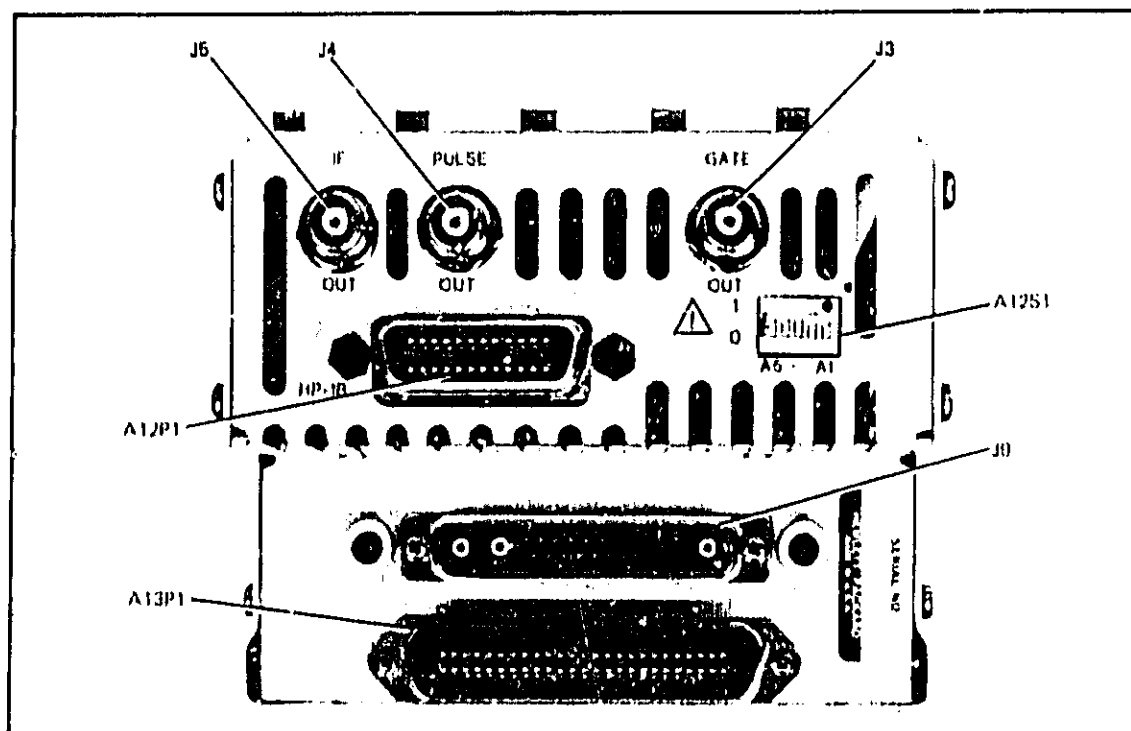


Figure B-23. 5355A Rear View

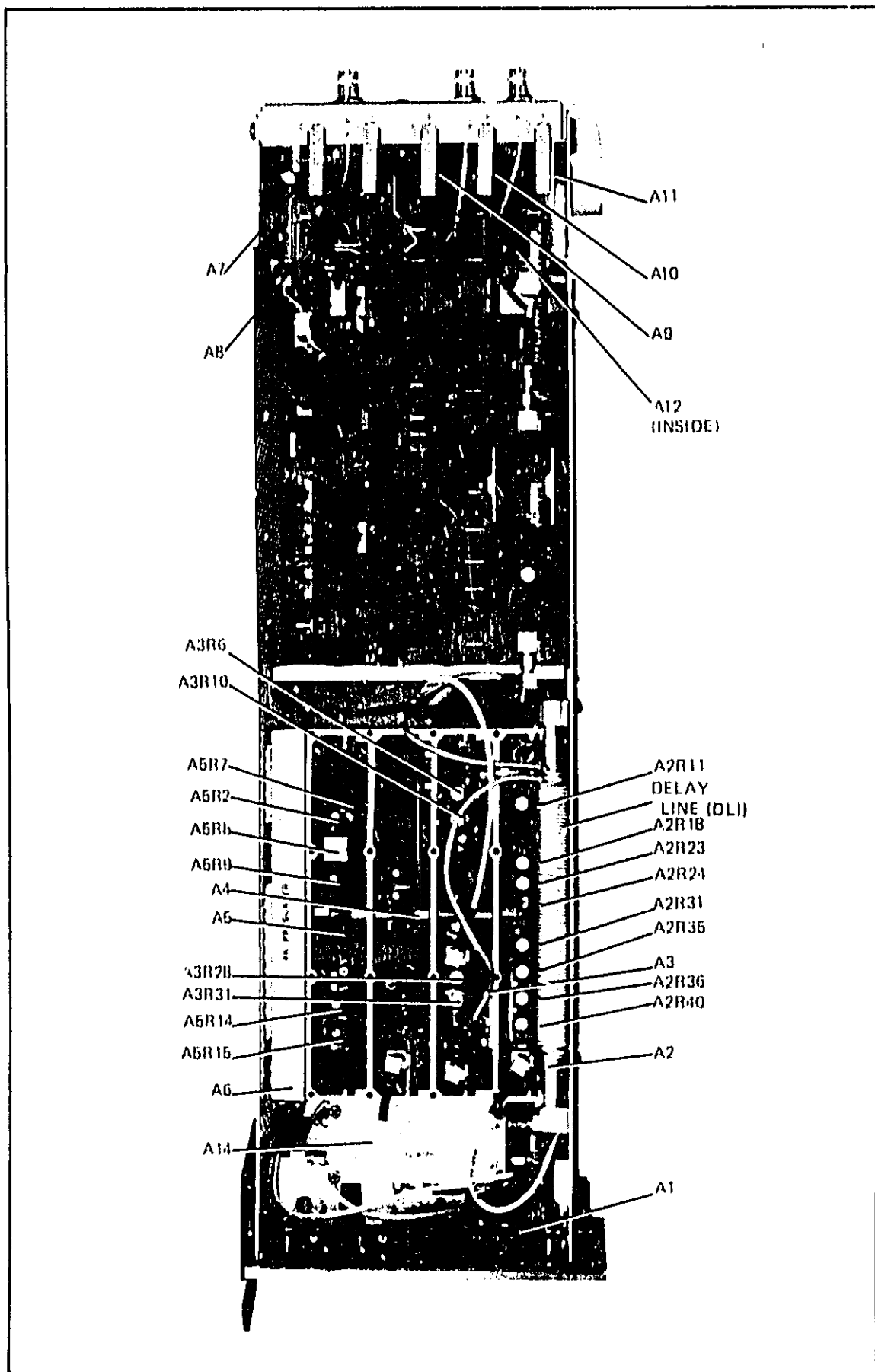


Figure 8-24. 5355A Top View (Assembly Locations and Adjustments)

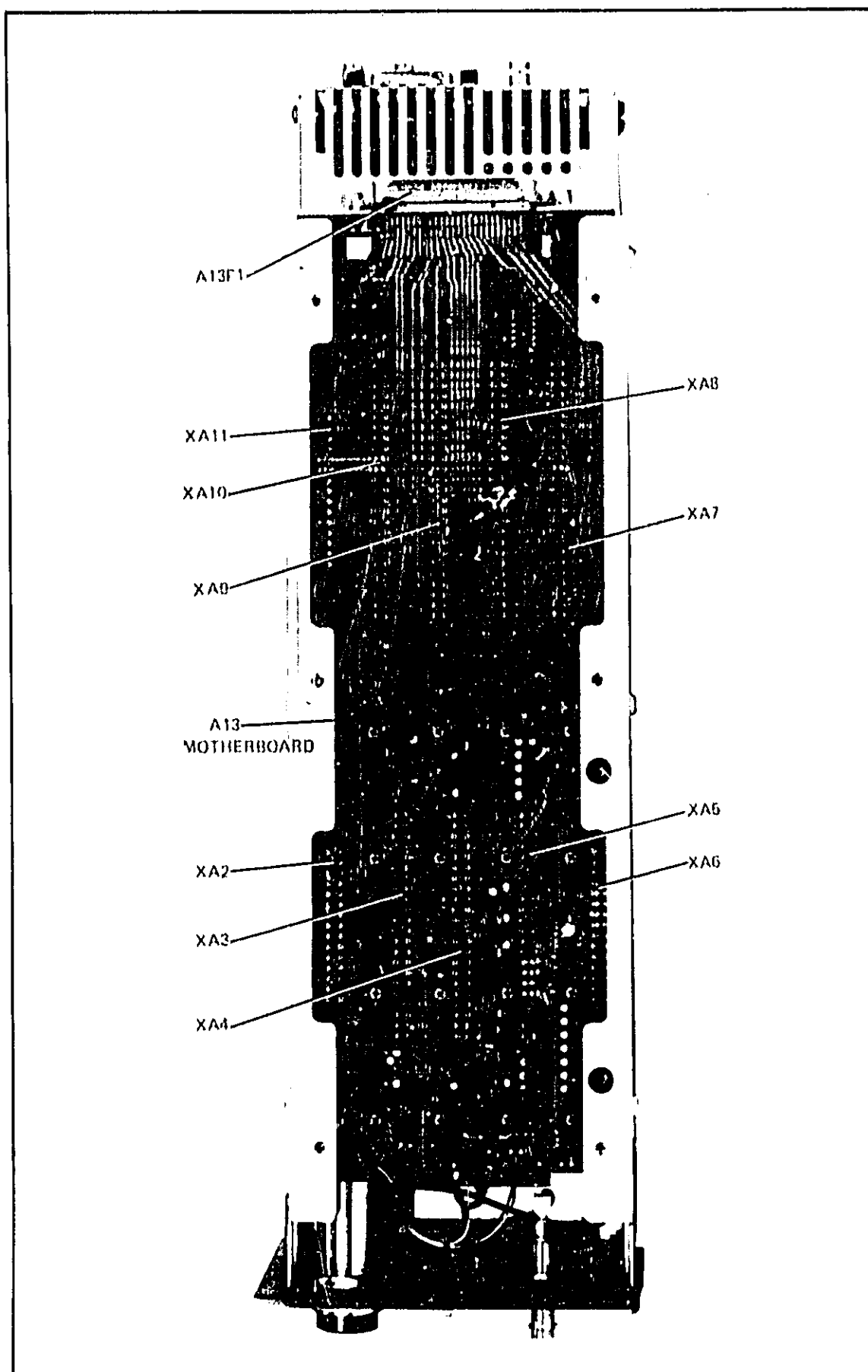


Figure 8-25. 5355A Bottom View

**REFERENCE
DESIGNATIONS**

A13
C1-C4 J1-J2 P1 U1, U2 XA2-XA11

TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfr or Industry Part Number
U1	1826-0215	MC7905.2CT
U2	1826-0106	MC7815CP

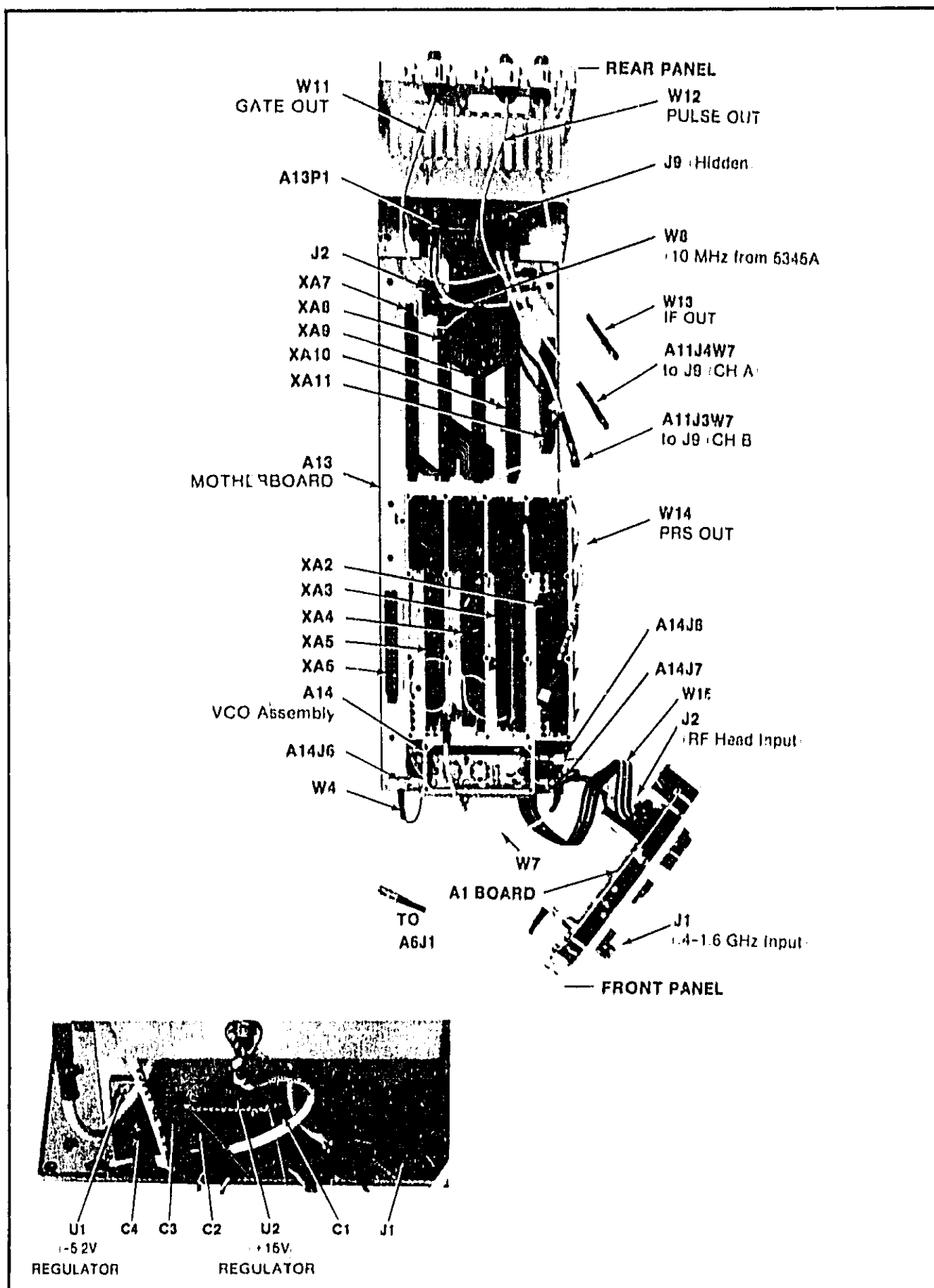


Figure 8-26. A13 Motherboard and Related Parts

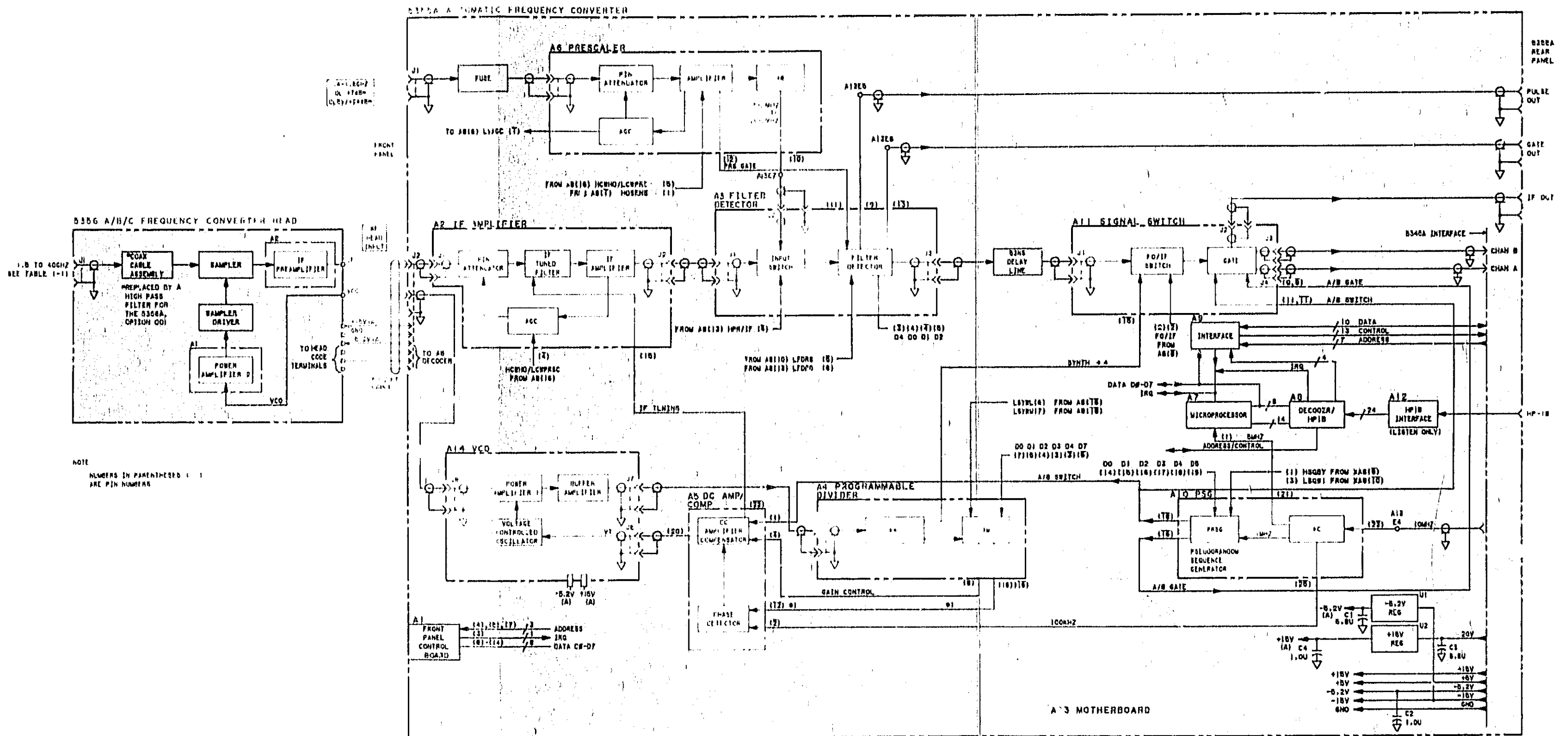


Figure 8-27. Overall Block Diagram

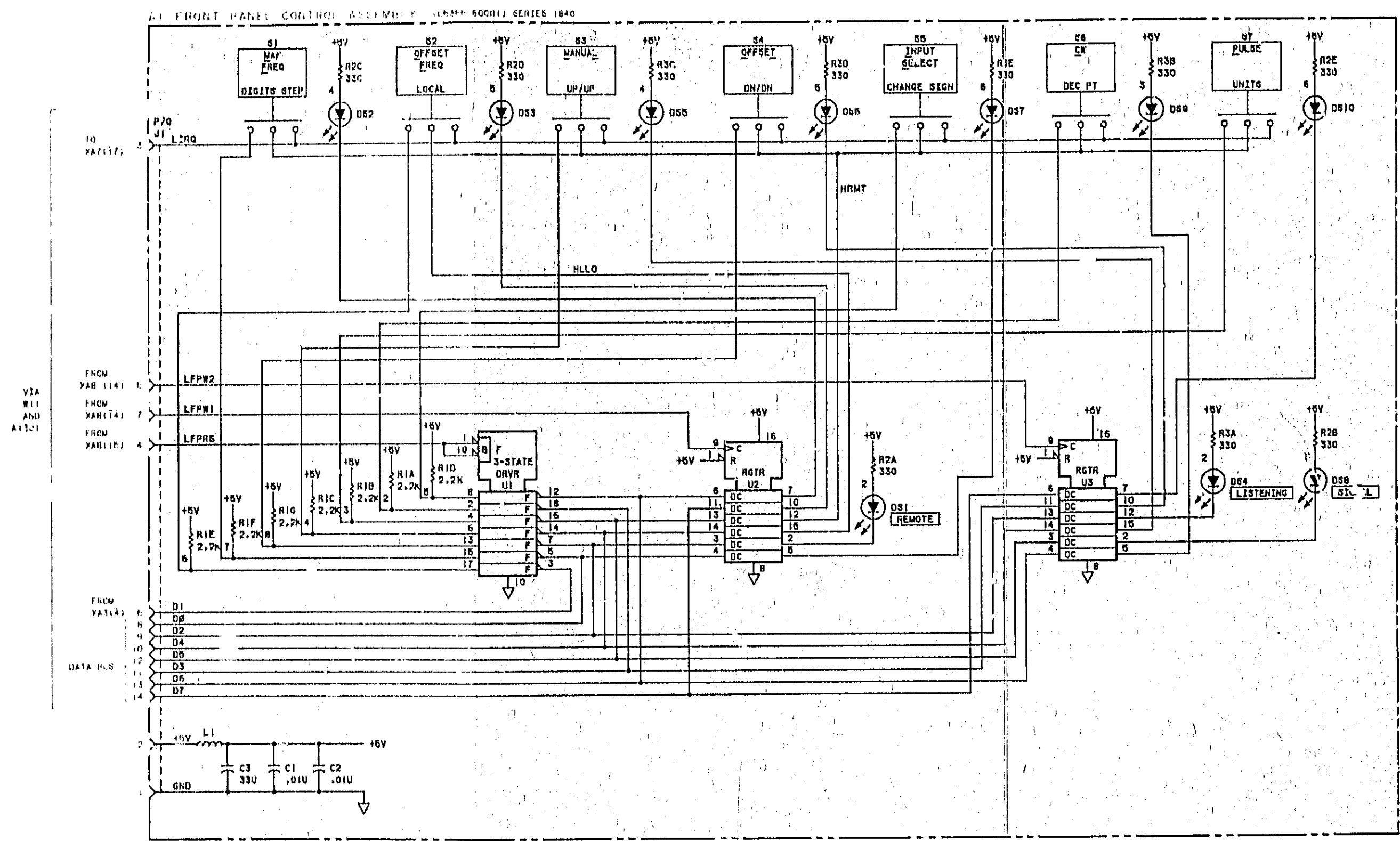
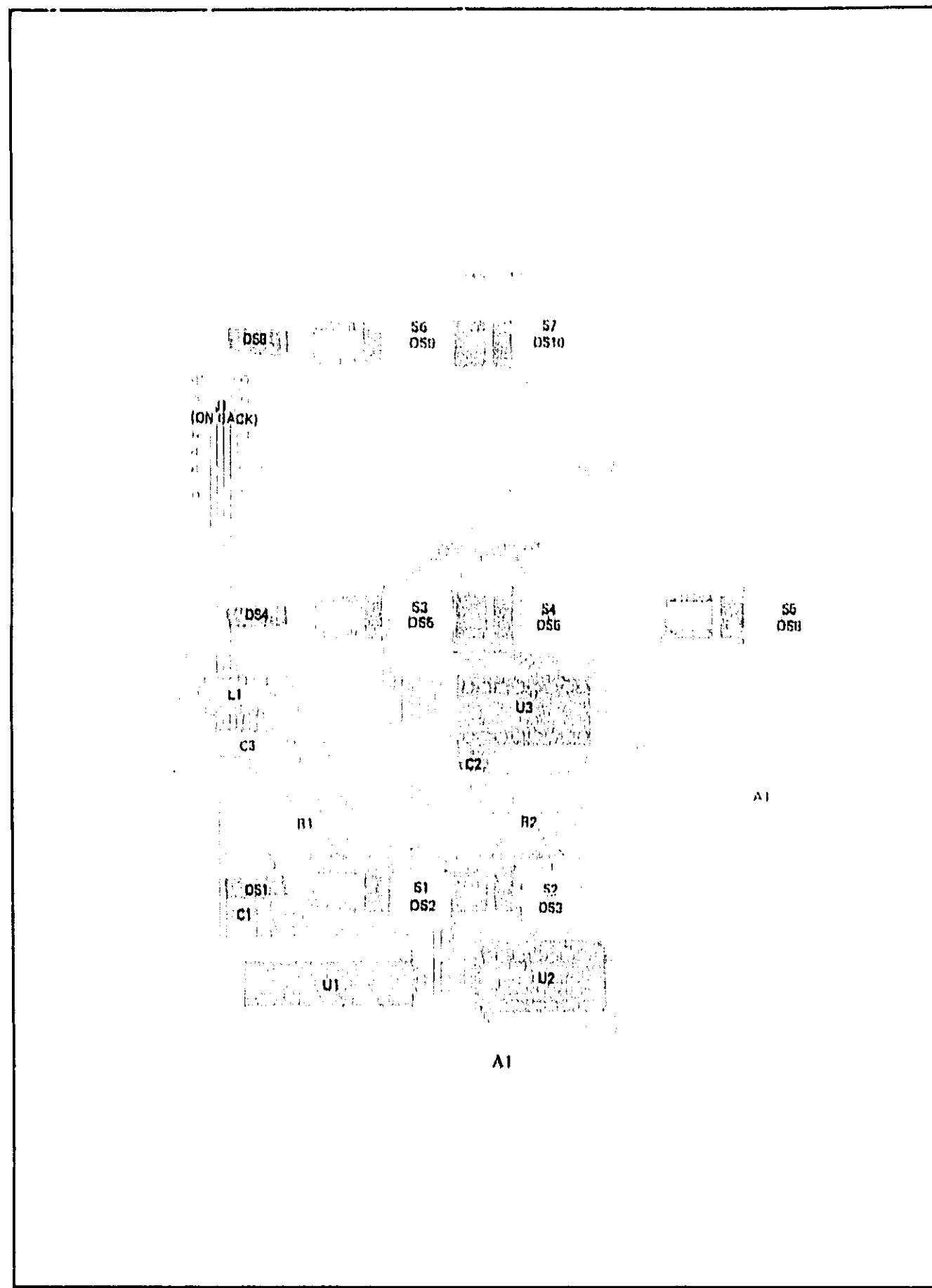
**REFERENCE
DESIGNATIONS**

A1
C1-C3 DS1-DS10 J1 L1 R1-R3 S1-S7 U1-U3

TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfr or Industry Part Number
U1	1820-1917	Same
U2, 3	1820-1196	Same

Part of Figure 3-28. A1 Front Panel Control Assembly



- NOTES
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED, ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
 2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN MICROFARADS; INDUCTANCE IN MICROHENRIES.

Figure 8-28. A1 Front Panel Control Assembly

REFERENCE DESIGNATIONS

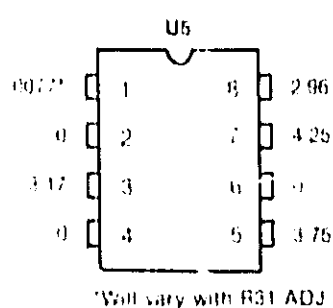
A2
C1-C49
CR1-CR14
J1, J2
L1-L13
Q1-Q6
R1-R50
RT1
TP1A-TP1F
U1-U5
VR1, VR2

TABLE OF ACTIVE ELEMENTS

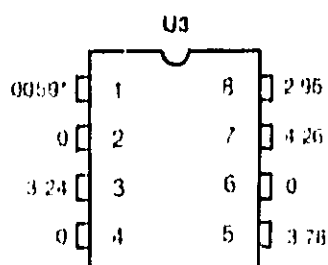
Reference Designation	HP Part Number	Mfr or Industry Part Number
CR1	1901-0856	Same
CR2, 3, 4	1901-0579	Same
CR5	1901-1080	Same
CR6, 7, 8	0122-0245	IN5139
CR9	1901-0057	Same
CR10	1901-0639	Same
Q1, Q6	1854-0071	Same
Q2, 3	1854-0345	2N5179
Q4	1854-0215	2N3904
Q5	1855-0250	3N215
U1, 3, 5	1826-0372	Same
U2	1826-0208	LM301N
U4	1820-0493	LM307N
VR1	1826-0282	MC79L12ACP
VR2	1826-0276	MC78L05ACP

A2 DC VOLTAGE CHECKS

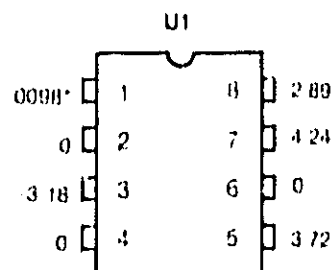
DC voltage readings
no signal applied at A2J1 Head installed, CW and AUTO mode



*Will vary with R31 ADJ



*Will vary with R23 ADJ



*Will vary with R18 ADJ

Part of Figure 8-29 A2 IF Amplifier Assembly

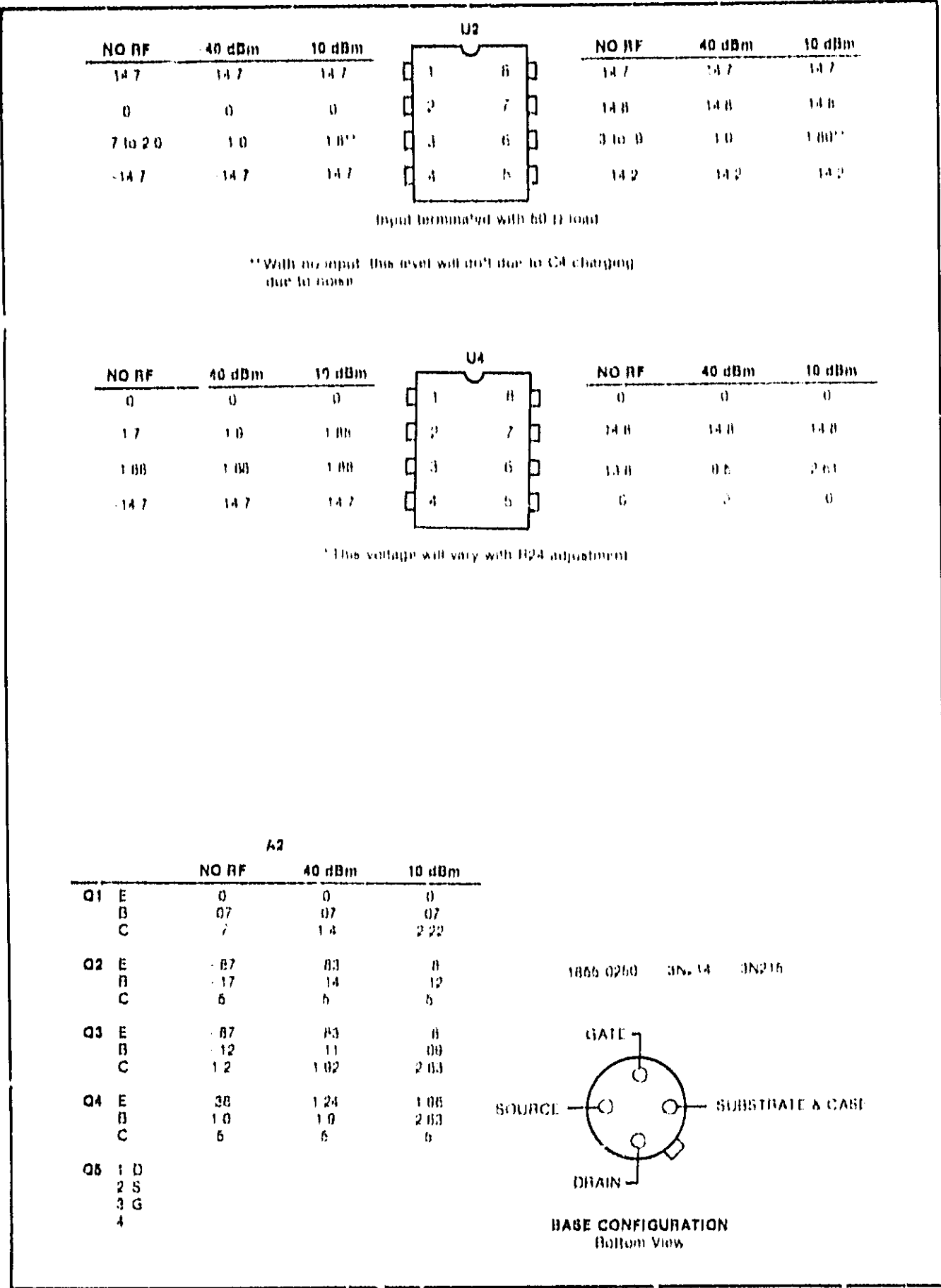


Figure 8-29. A2 H Amplifier Assembly

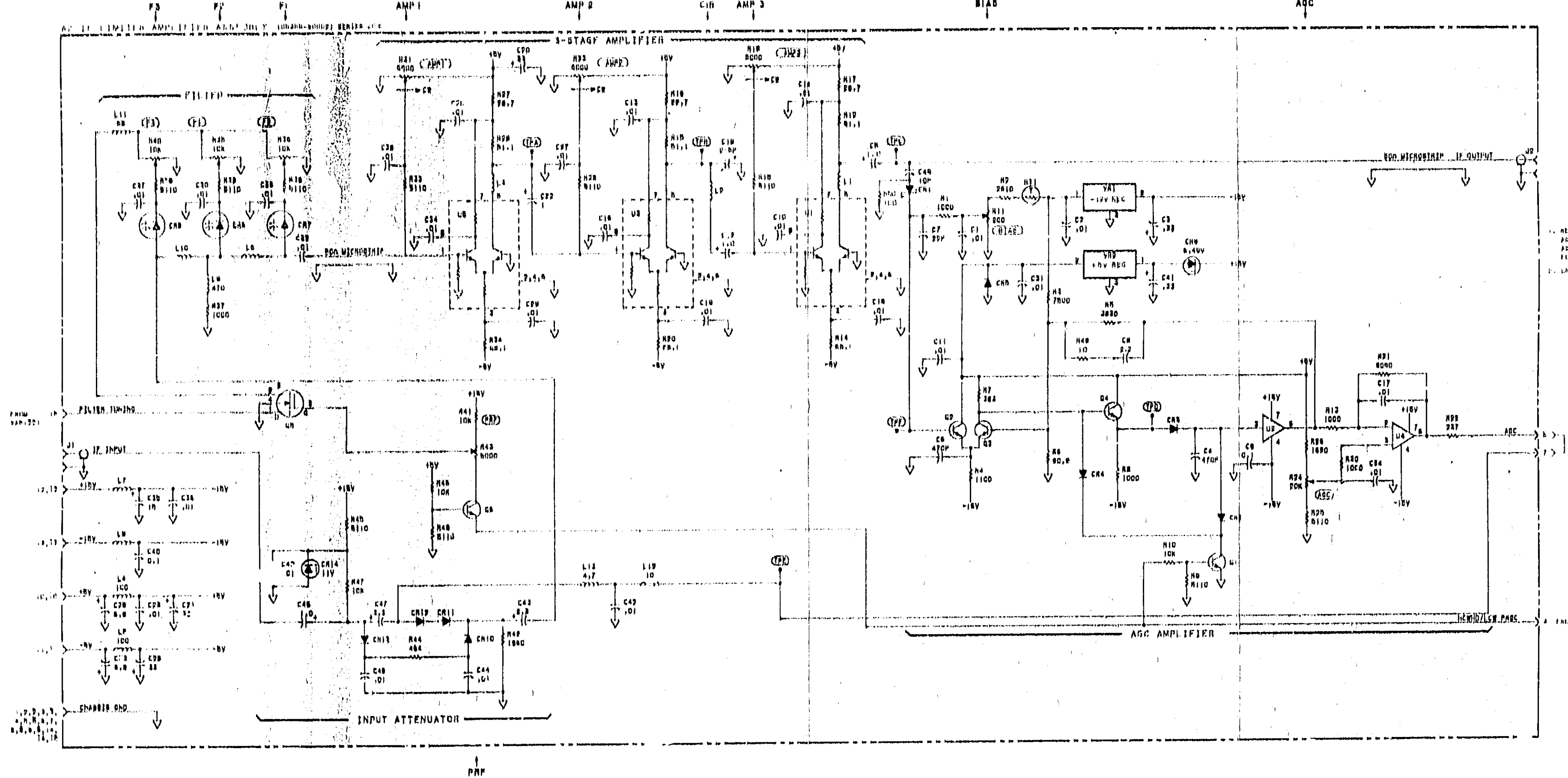
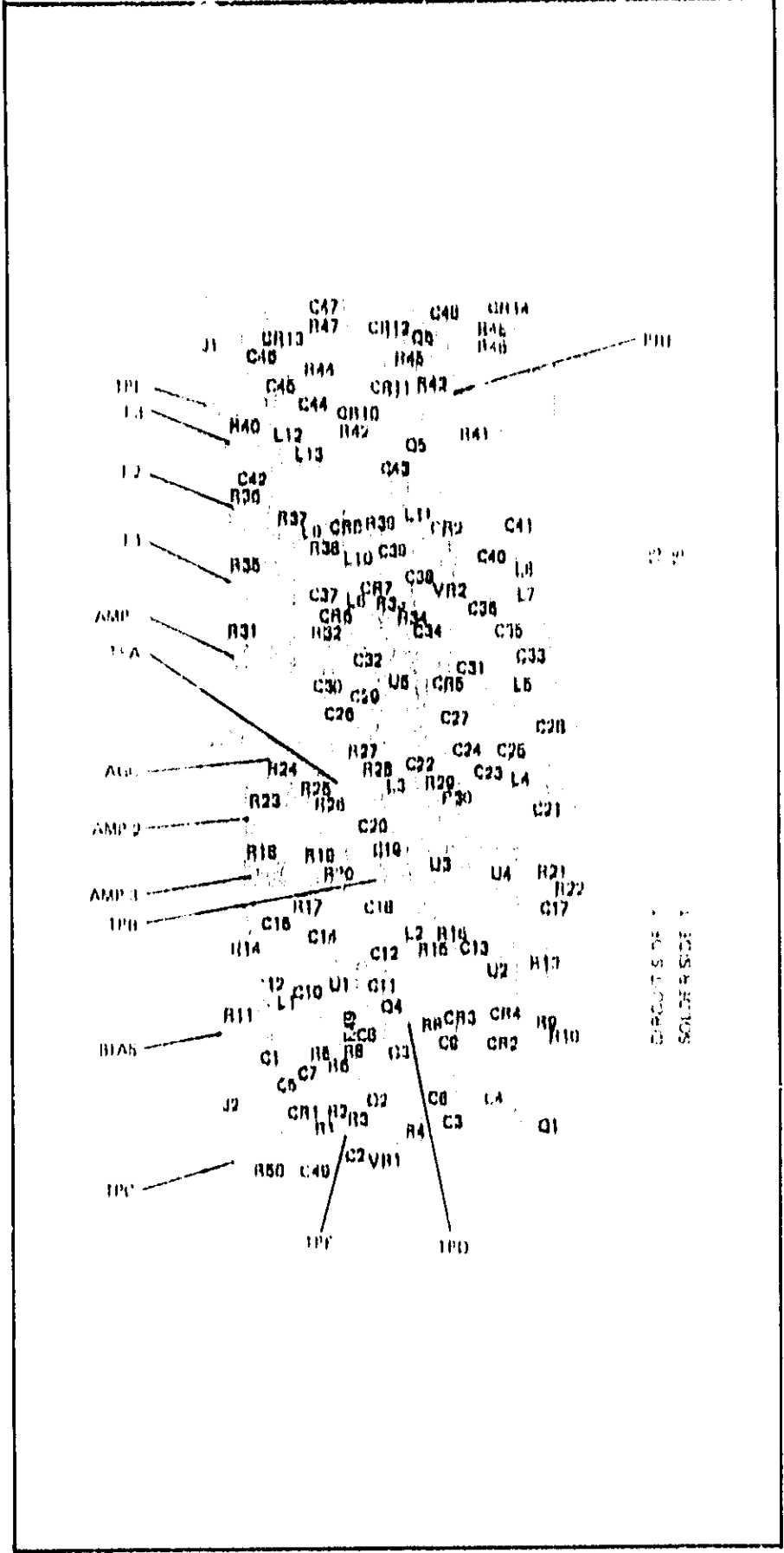


Figure 8-29. A1 H Amplifier Assembly

REFERENCE
DESIGNATIONS

A3
C1-C49
CR1-CR7
J1-J3
K1
L1-L14
Q1-Q8
R1-R40
U1-U8

TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfr or Industry Part Number
CR1	1901-0040	Same
CR2, 6 7	1901-0852	Same
CR3, 5	0122-0245	IN5139
CR4	0122-0287	Same
Q1, 2, 5, 7, 8	1854-0215	2N3824
Q3, 4	1854-0379	Same
Q6	1854-0019	Same
U1, 7	1026-0372	Same
U2	1820-1492	SN74LS368AN
U3	1820-1440	SN74LS279N
U4	1820-1208	SN74LS32N
U5, 6, 8	1826-0548	LM161J

Part of Figure 8-30. A3 Filter Detector Assembly

REFERENCE DESIGNATIONS

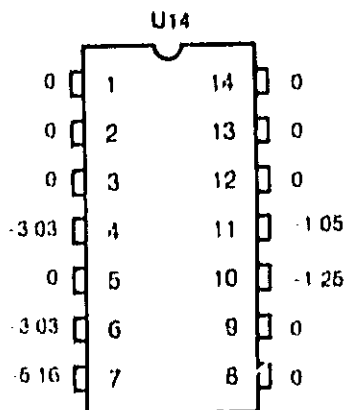
A4
C1-C24
CR1
J1
L1-L4
R1-R12
U1-U14

TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfr or Industry Part Number
CR1	1902-0126	Same
U1-U4	1820-1196	SN74LS174N
U5, 7, 8, 9	1820-1429	SN74LS160AN
U6	1820-1112	SN74LS74AN
U10	1820-0817	MC10131P
U11	1820-1199	SN74LS04N
U12	1820-1888	MC12013L
U13	1820-1197	SN74LS00N
U14	1820-2292	SP8611BDG

A4 DC VOLTAGES

- All boards inserted and coax cables attached
- A4 on its extender board VCO lead connected at A4J1
- RF head installed
- No signal applied
- DC voltage checks taken with MANUAL MEASUREMENT MODE active
This stops the VCO for stable readings.



Other IC's are digital logic IC's

Part of Figure 8-31. A4 Programmable Divider Assembly

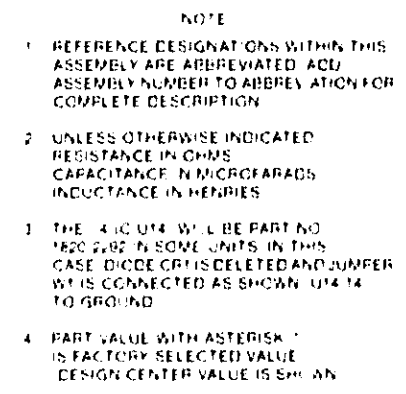
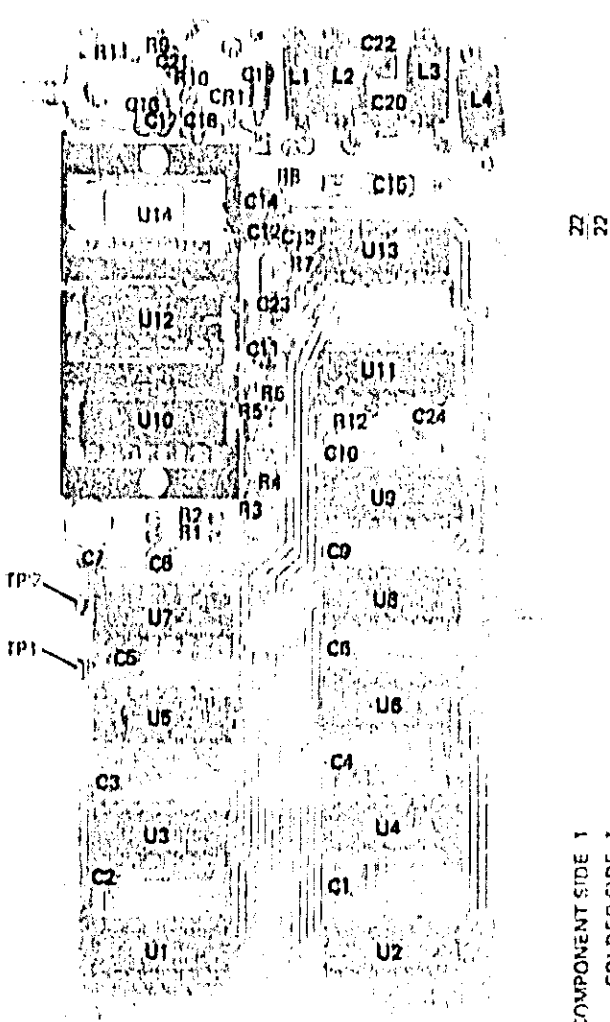


Figure 8-31. A4 Programmable Divider Assembly

REFERENCE DESIGNATIONS

A5
C1-C15
CR1
L1
R1-R19
U1-U8

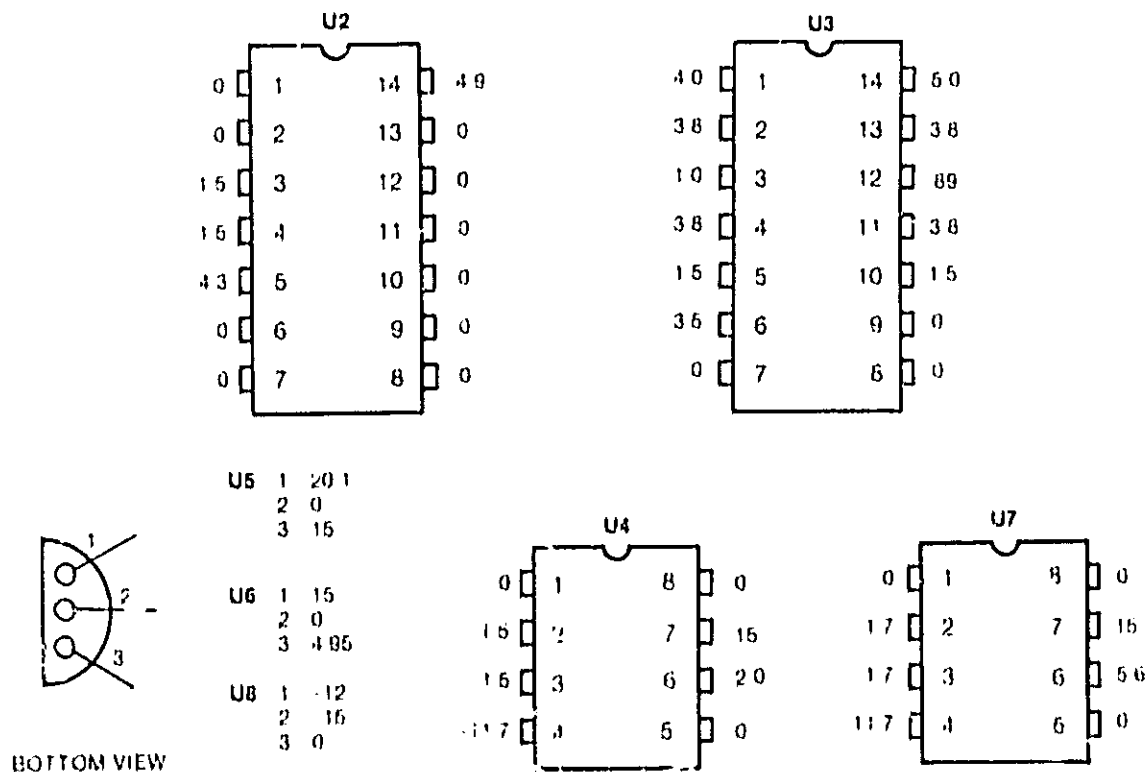
TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfr or Industry Part Number
CR1	1901-0539	Same
U1	1820-1417	SN74LS26N
U2	1820-1325	CD4066AE
U3	1820-0630	MC4044F
U4, U7	1820-0493	LM307N
U5	1826-0274	MC77L15ACP
U6	1826-0276	MC78L05ACP
U8	1826-0282	MC79L12ACP

A5 DC VOLTAGES

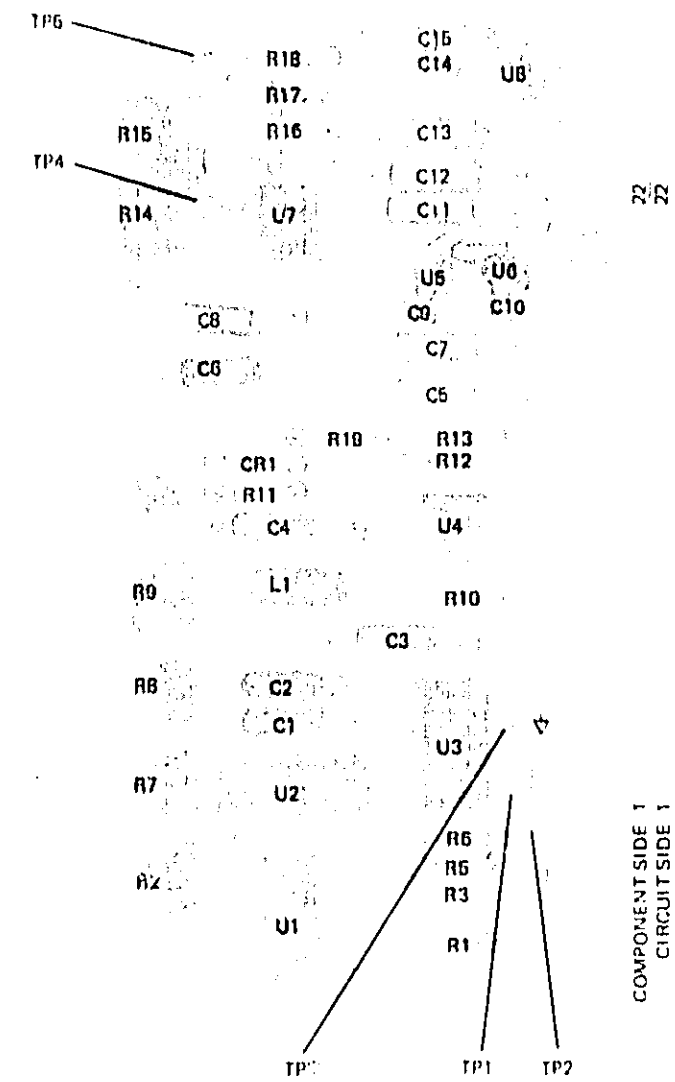
CONDITIONS

- RF head is installed, no signal applied
- All boards in place and connected
- A5 on its extender board
- Place 5355 in MANUAL measurement mode. This stops the synthesizer sweep and enables stable voltage readings

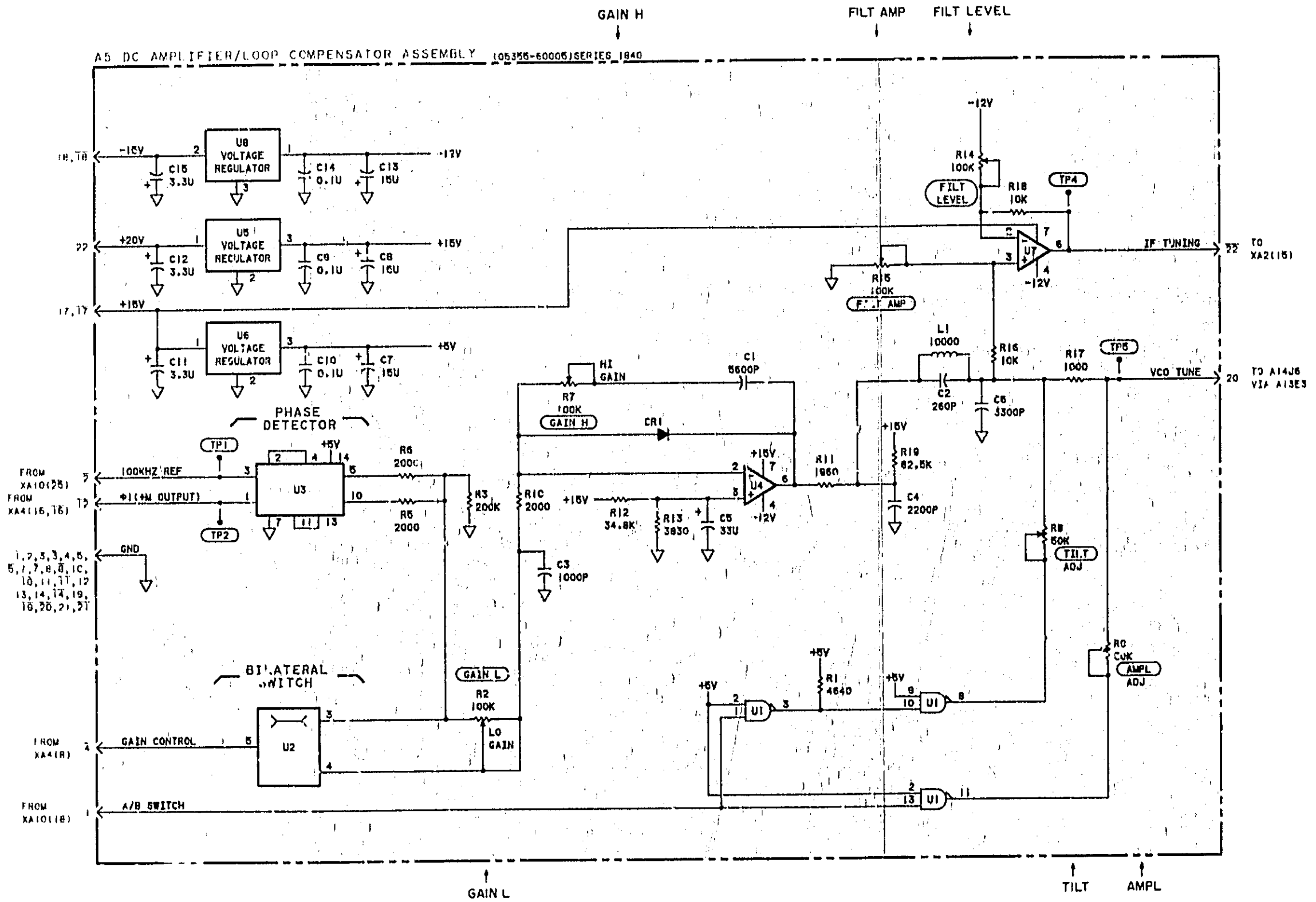


Part of Figure 8-32 A5 DC Amplifier Loop Compensator Assembly

SERVICE INFORMATION CONT



A5



- NOTES:
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
 2. UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS;
CAPACITANCE IN FARADS;
INDUCTANCE IN HENRIES

Figure 8-32. A5 DC Amplifier/Loop Compensator Assembly

REFERENCE DESIGNATIONS

A6
C1-C61
CR1-CR14
DS1, DS2
J1
L1-L15
Q1-Q4
R1-R48
RT1
TP1-TP5
U1-U9
VR1-VR3
W1, W2

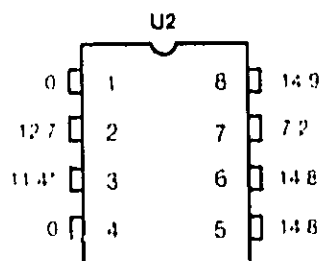
TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfr or Industry Part Number
CR1	1901-1080	Same
CR2, 3	1902-0057	Same
CR4-7, 11	1901-0040	Same
CR8, 10	1901-0856	Same
CR9	1901-0579	Same
CR12, 13	1901-0639	Same
CR14	1902-0025	Same
Q1	1853-0036	Same
Q2	1854-0215	2N3904
Q3, Q4	1854-0345	2N5179
U1, U4	1826-0548	LM161J
U2	1826-0065	SN72311P
U3	1820-0493	LM307N
U5	1826-0208	LM310N
U6	1820-2281	Same
U7	1820-2101	Same
U8	5088-7036	Same
U9	5088-7037	Same
VR1	1826-0285	MC79L05C
VR2	1826-0282	MC79L12ACP
VR3	1826-0276	MC78L05ACP

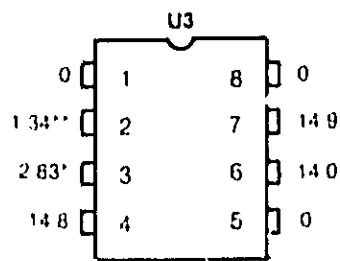
A6 DC VOLTAGES

CONDITIONS

- No signal applied to 4-16 GHz input.
- No RF head installed
- A6 on extender board 05355-60020 coax jumpers in place on extender board

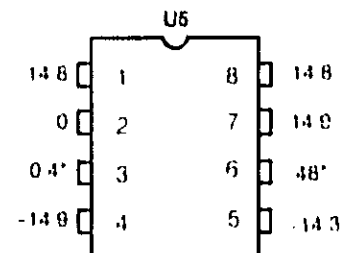


*Will vary with setting of R8



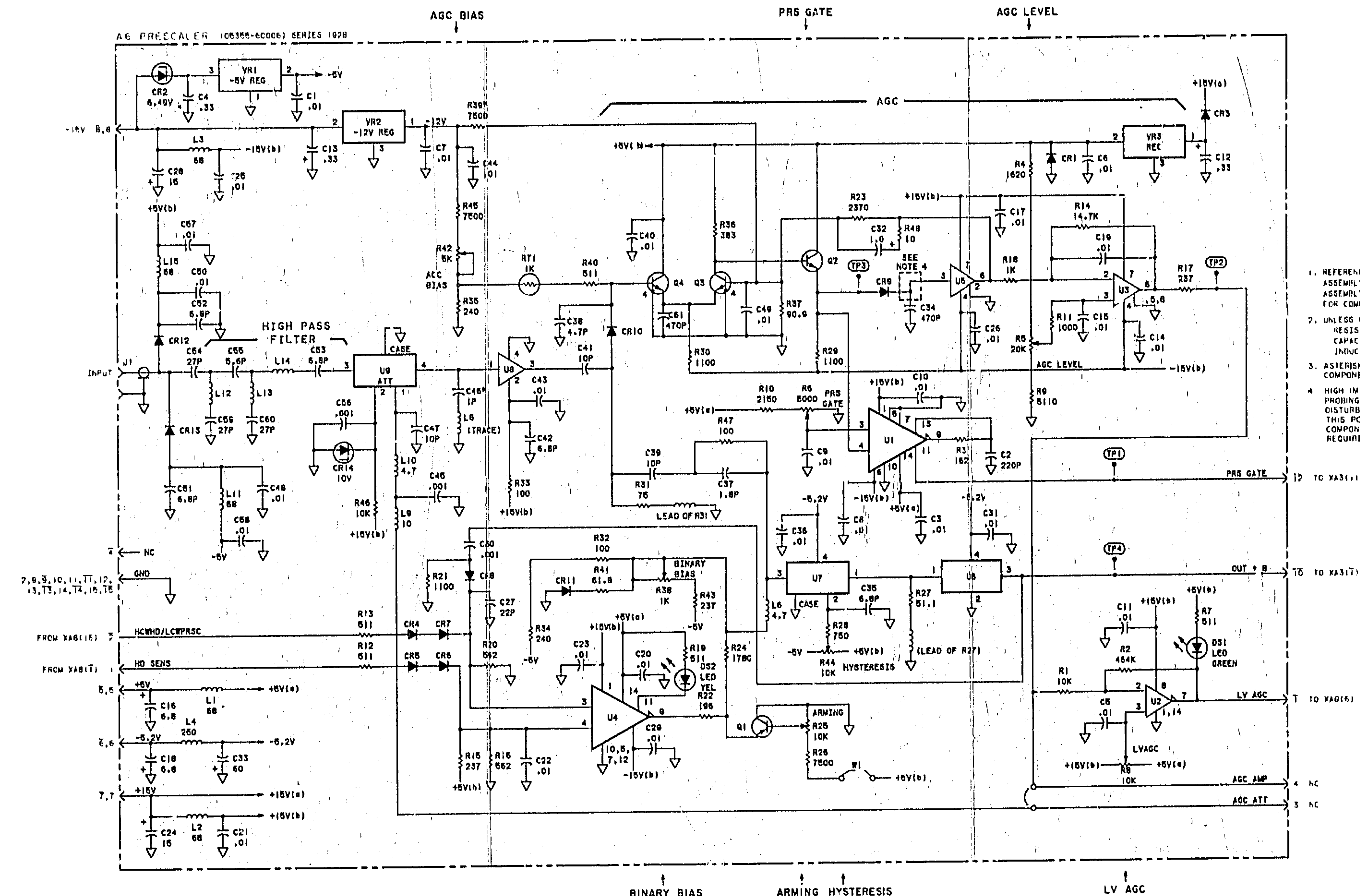
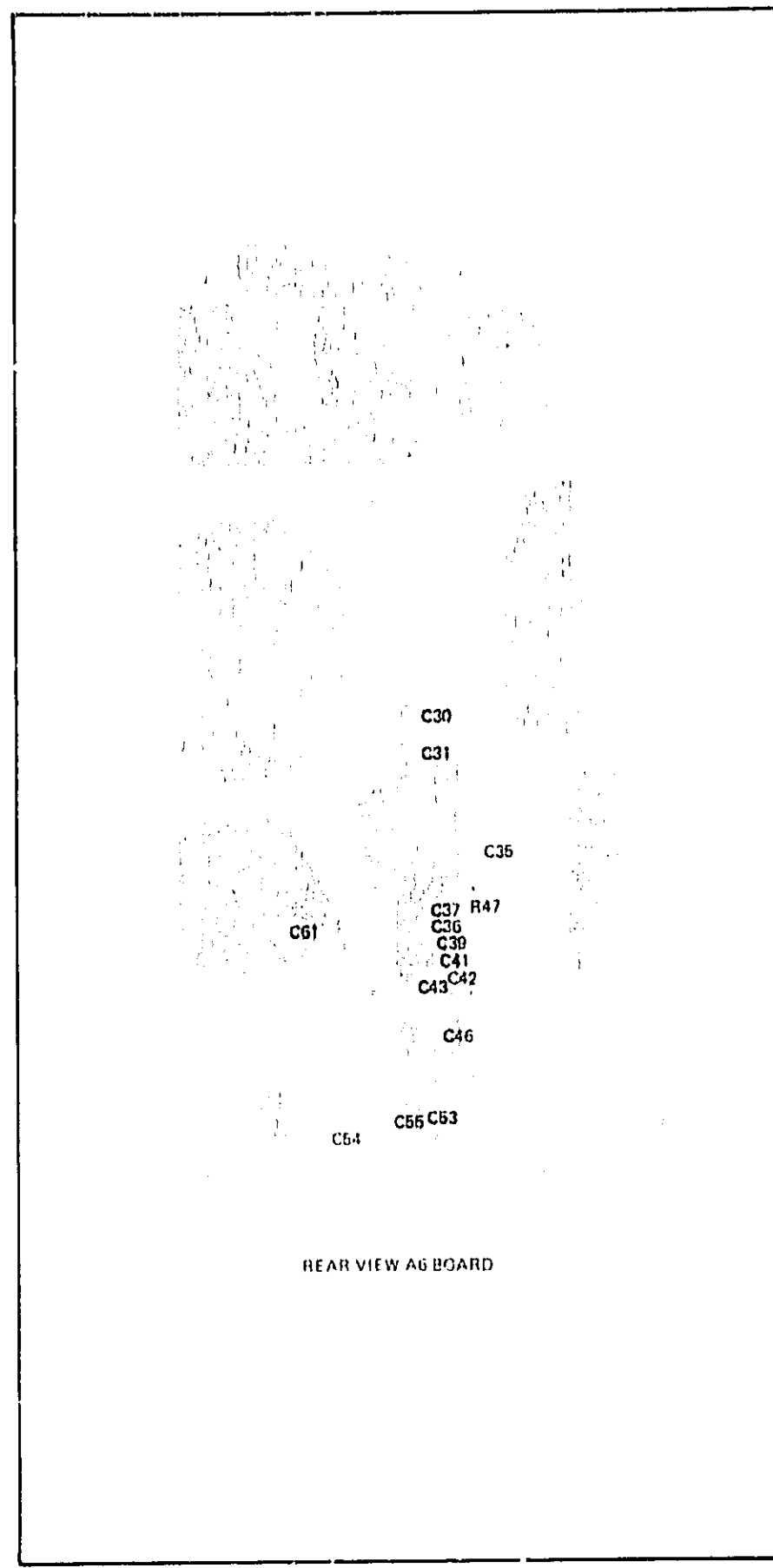
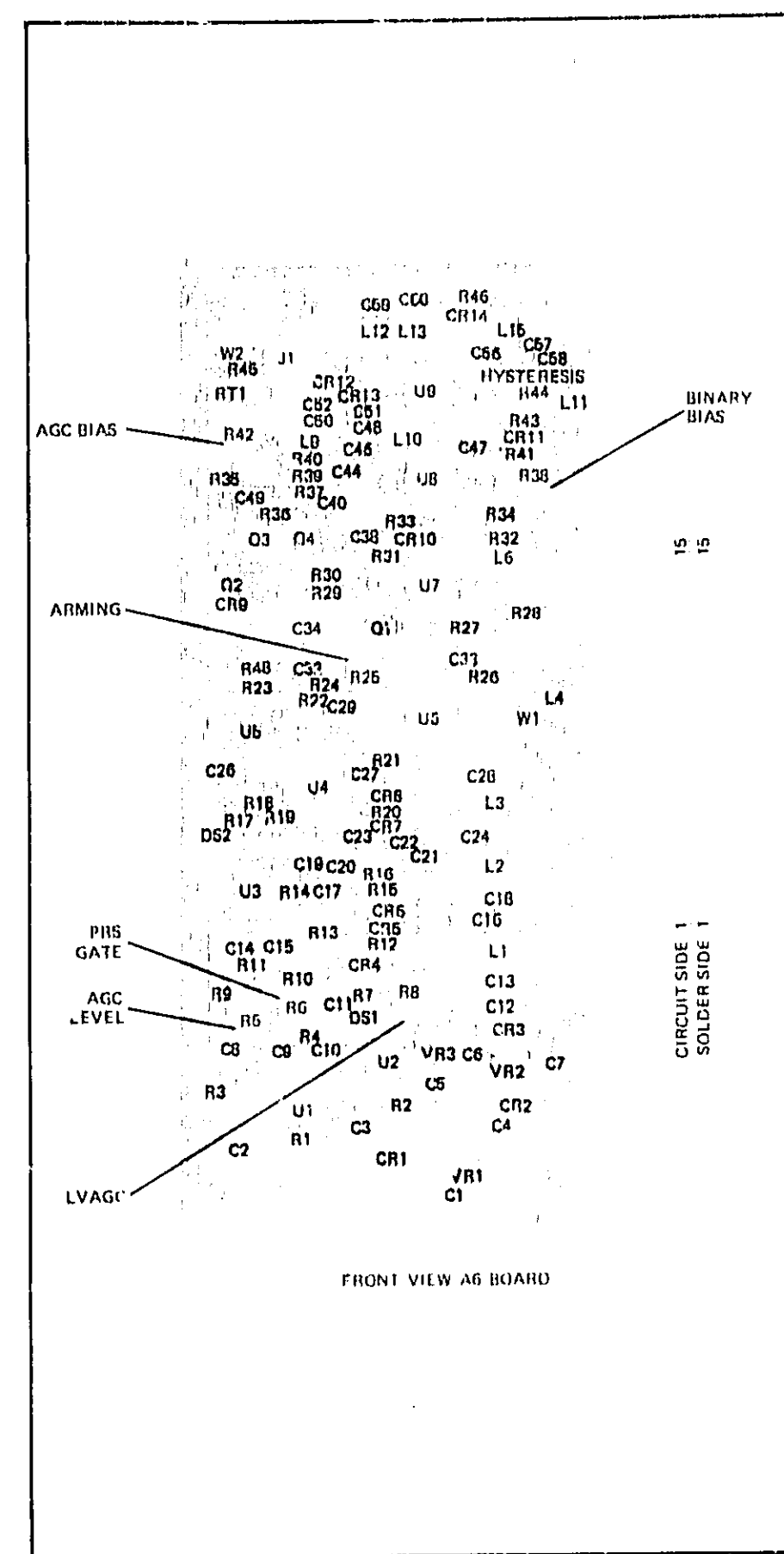
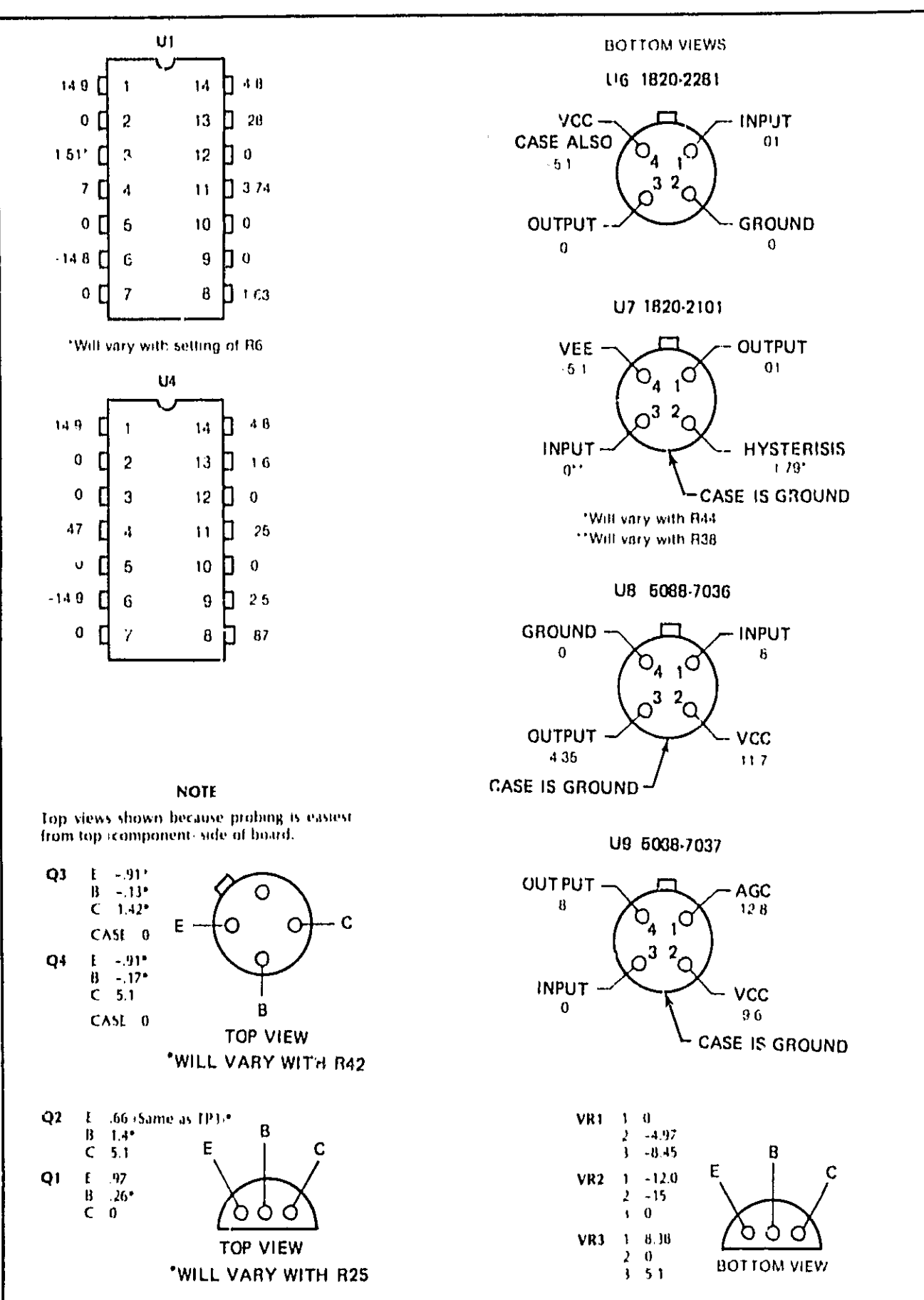
*Will vary with setting of R5

**Will vary with R42



*Will vary with R42

Part of Figure 8-33. A6 Prescaler Assembly



NOTES

1. REFERENCE DESIGNATIONS WITHIN THE ASSEMBLY ARE ABBREVIATED. THE ASSEMBLY NUMBER IS THE ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN MICROFARADS; INDUCTANCE IN MICROHENRIES.
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUE $\pm 50\%$
4. HIGH IMPEDANCE CIRCUIT POINT. PROBING WITH TEST EQUIPMENT WILL DISTURB CIRCUIT ACTION. CLEAN THIS POINT OF FLUX RESIDUE IF COMPONENT REPLACEMENT IS REQUIRED.

Figure 8-33. A6 Prescaler Assembly

Figure 8-33. A6 Prescaler Assembly

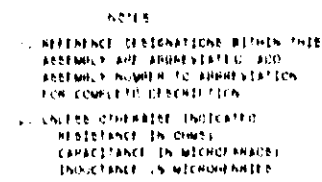
REFERENCE
DESIGNATIONS

A7
C1-C10 CR1-CR4 L1 R1-R10 S1 TP1-RP11 U1-U17 XU1-XU3, XU5 XU8, XU10, XU12, XU14

TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfr or Industry Part Number
CR1-CR4	1901-0535	Same
U1	1820-2137	MC68A00P
U2, 3	1820-1917	SN74LS240N
U4	1820-1199	SN74LS04N
U5	1818-0894	TMS4732NL (Masked)
U6, U17	1820-1197	SN74LS00N
U7	1820-1144	SN74LS02N
U8	1818-0885	MK36000N-4 (Masked)
U9	1820-2036	MC6875L
U10, U12	1818-0438	TMS2114-45NL
U11	1820-1112	SN74LS74AN
U13	1820-1207	SN74LS30N
U14	1820-2075	SN74LS245N
U15	1820-1281	SN74LS139N
U16	1820-1202	SN74LS10N

Part of Figure 8-34. A7 Microprocessor Assembly



8-131

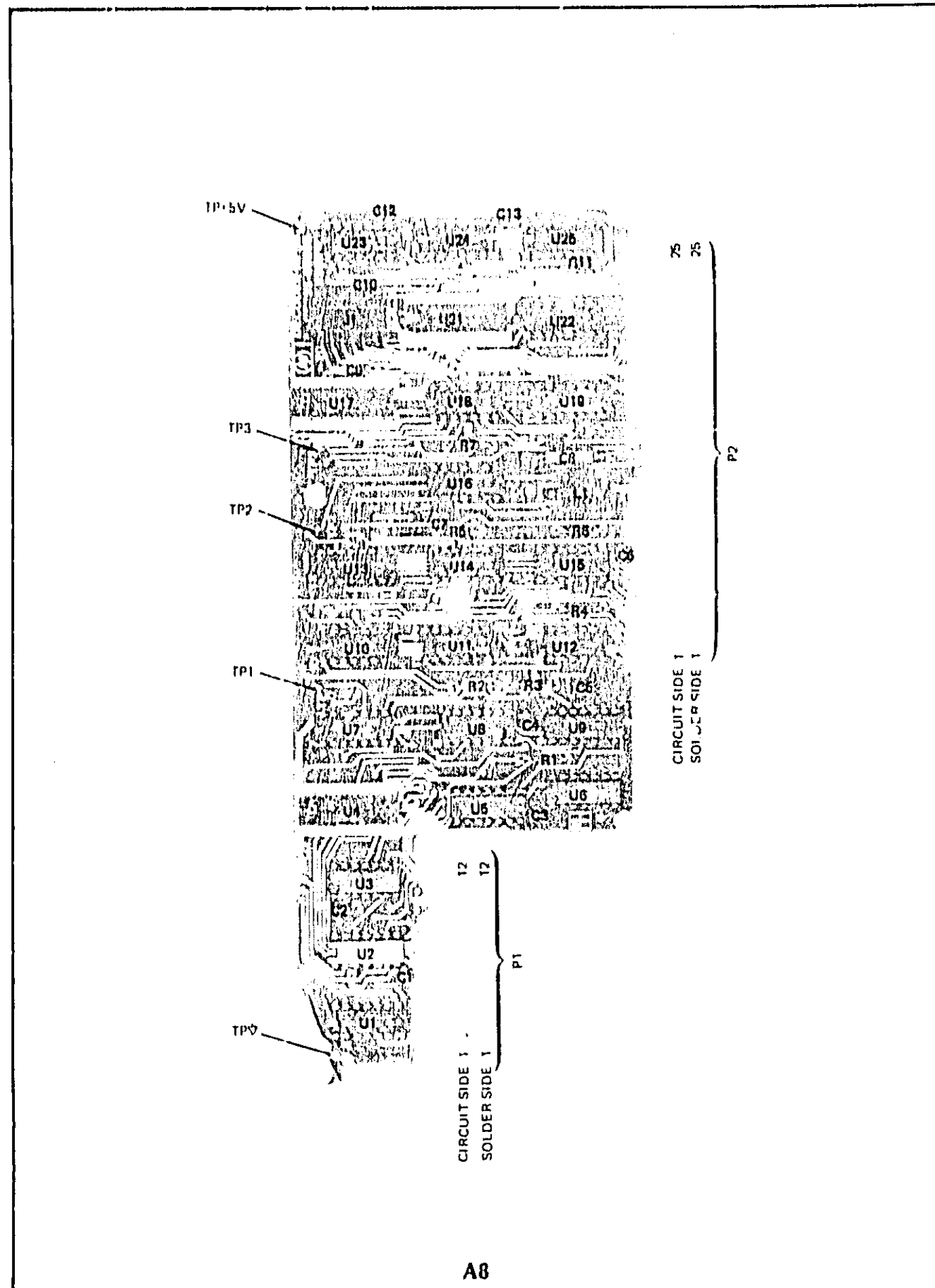
**REFERENCE
DESIGNATIONS**

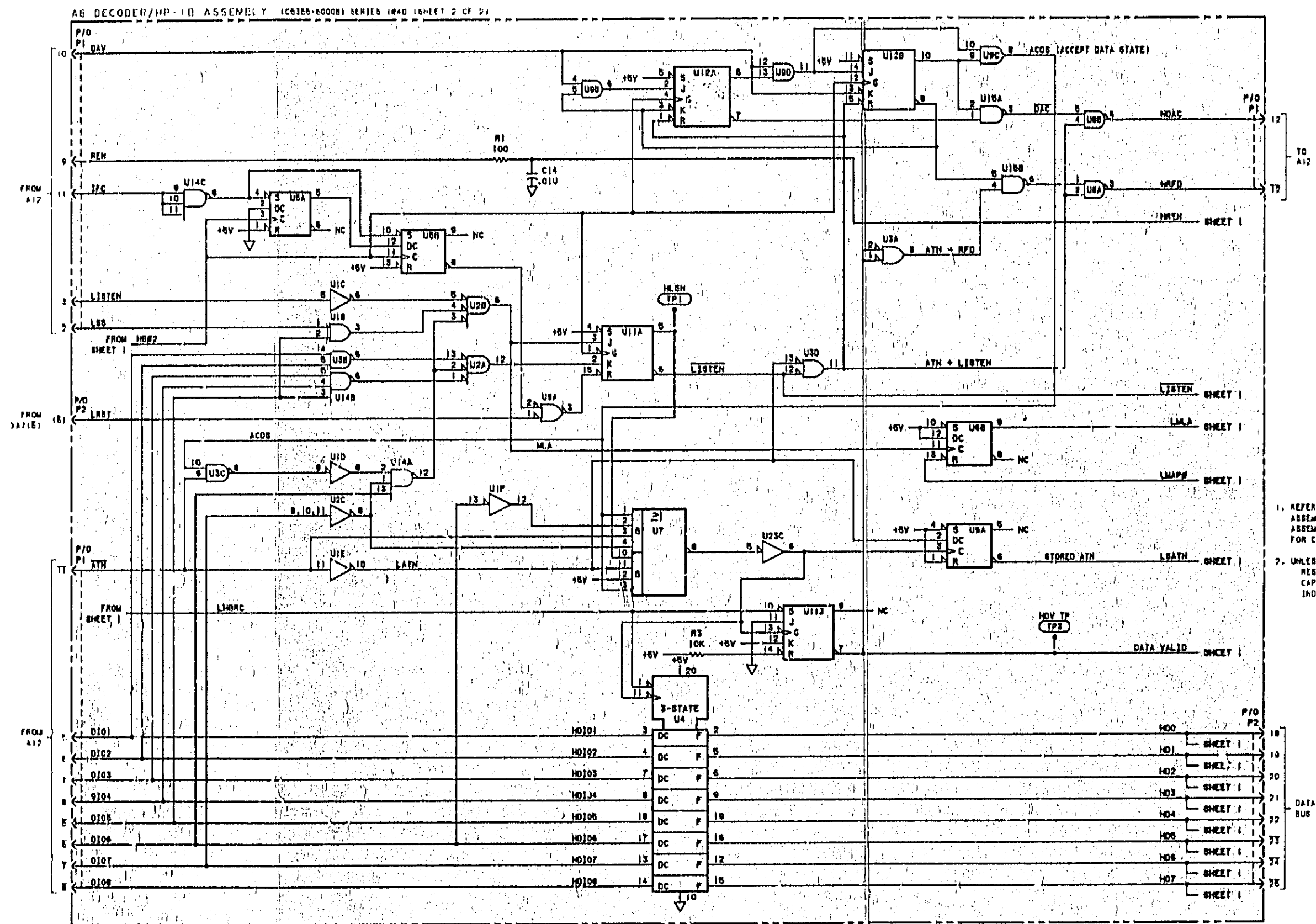
A8
C1-C13 L1 R1-R7 TP1-TP3 U1-U25

TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfr or Industry Part Number
U1, U23	1820-1199	SN74LS04N
U2	1820-1206	SN74LS27N
U3, U15	1820-1107	SN74LS00N
U4, U17	1820-1997	SN74LS374N
U5, U6	1820-1112	SN74LS74AN
U7	1820-1284	SN74LS55N
U8	1820-0621	SN7438N
U9	1820-1201	SN74LS08N
U10	1820-1190	SN74LS174N
U11	1820-1212	SN74LS112AN
U12	1820-1282	SN74LS109AN
U13	1820-1255	SN74368N
U14	1820-1202	SN74LS10N
U16, U18	1820-1211	SN74LS86N
U19	1820-1200	SN74LS05N
U20	NOT ASSIGNED	
U21	1820-1917	SN74LS240N
U22, U24, U25	1820-1216	SN74LS138N

Part of Figure 8-35. A8 Decoder/HF-IB Assembly





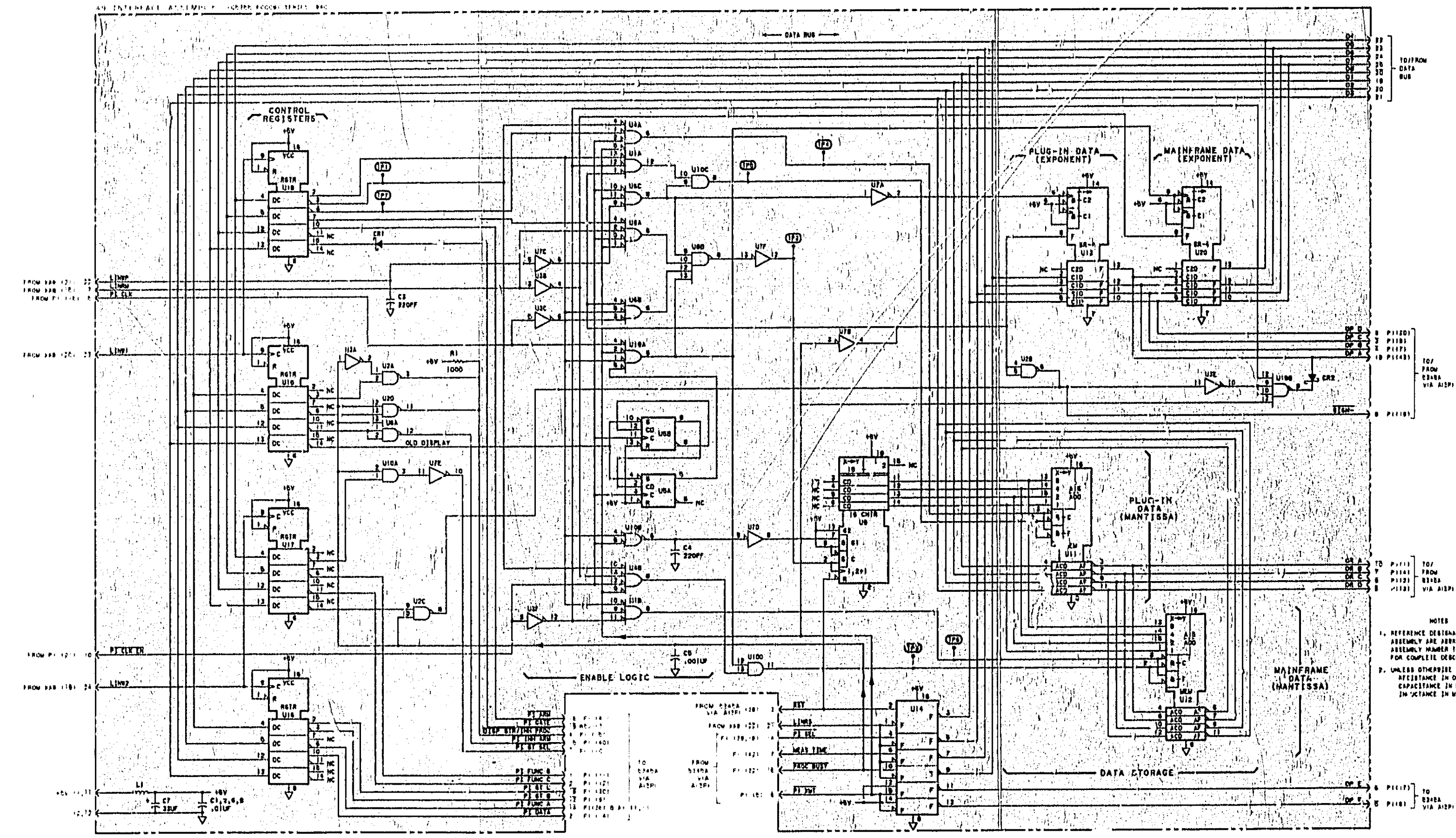
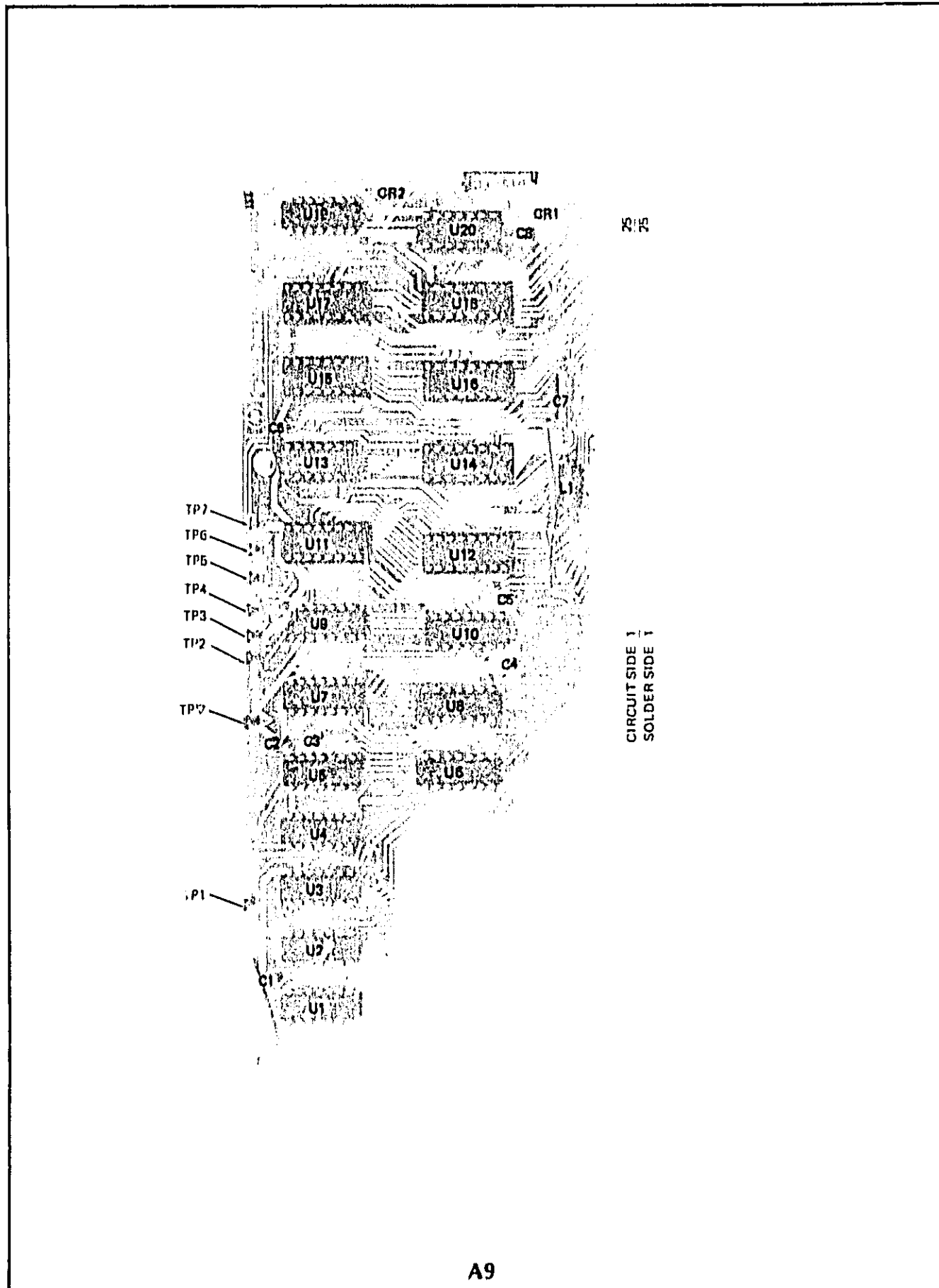
**REFERENCE
DESIGNATIONS**

A9
C1-C8 CR1, CR2 L1 R1 U1-U20

TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfr or Industry Part Number
CR1, CR2	1901-0535	Same
U1, U6	1820-1202	SN74LS10N
U2	1820-1198	SN74LS03N
U3	1820-1199	SN74LS04N
U4, U8	1820-1204	SN74LS20N
U5	1820-1112	SN74LS74AN
U7	1820-1416	SN74LS14N
U9	1820-1430	SN74LS161AN
J10	1820-1201	SN74LS08N
U11, U12	1816-1089	DM74LS189N
U13, U20	1820-1296	SN74LS295BN
U14	1820-1492	SN74LS368AN
U15, U16, U17	1820-1195	SN74LS175N
U19	1820-1415	SN74LS13N

Part of Figure 8-36. A9 Interface Assembly



NOTES
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS CAPACITANCE IN MICROFARADS DIMENSIONS IN MILLIMETERS.

Figure 8-36. A9 Interface Assembly

**REFERENCE
DESIGNATIONS**

A10
C1-C9 L1-L3 R1-R3 U1-U16

TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfr or Industry Part Number
U1, U14, U15	1820-1442	SN74LS290N
U2	1820-1202	SN74LS10N
U3, U4	1820-1433	SN74LS164N
U5, U6	1820-1112	SN74LS74AN
U7, U10, U11	1820-1197	SN74LS00N
U8	1820-1430	SN74LS161AN
U9	1820-1211	SN74LS86N
U12	1820-1196	SN74LS174N
U13	1820-1199	SN74LS04N
U16	1826-0132	UA760DC

Part of Figure 8-37. A10 Pseudorandom Sequence Generator Assembly

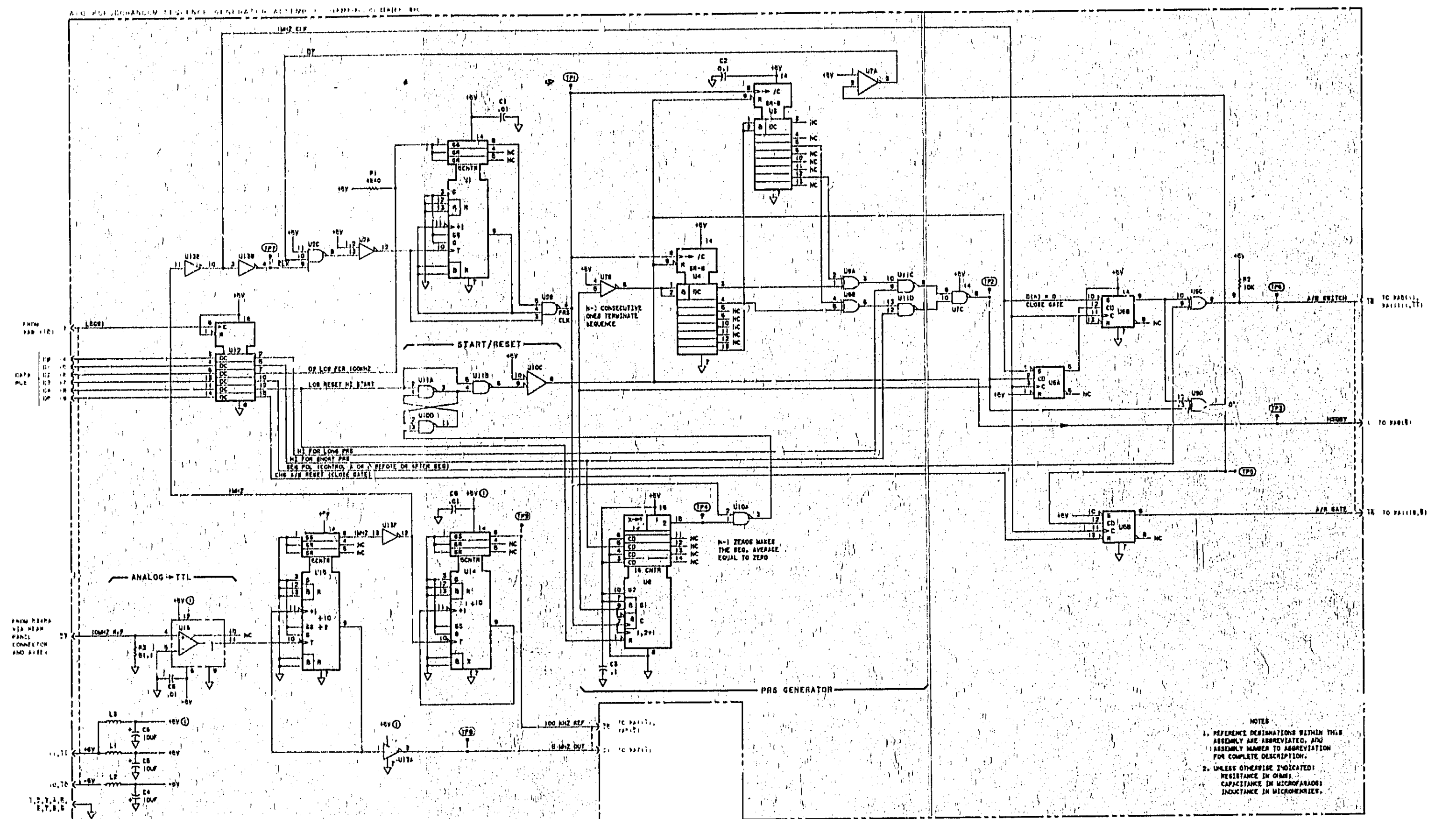
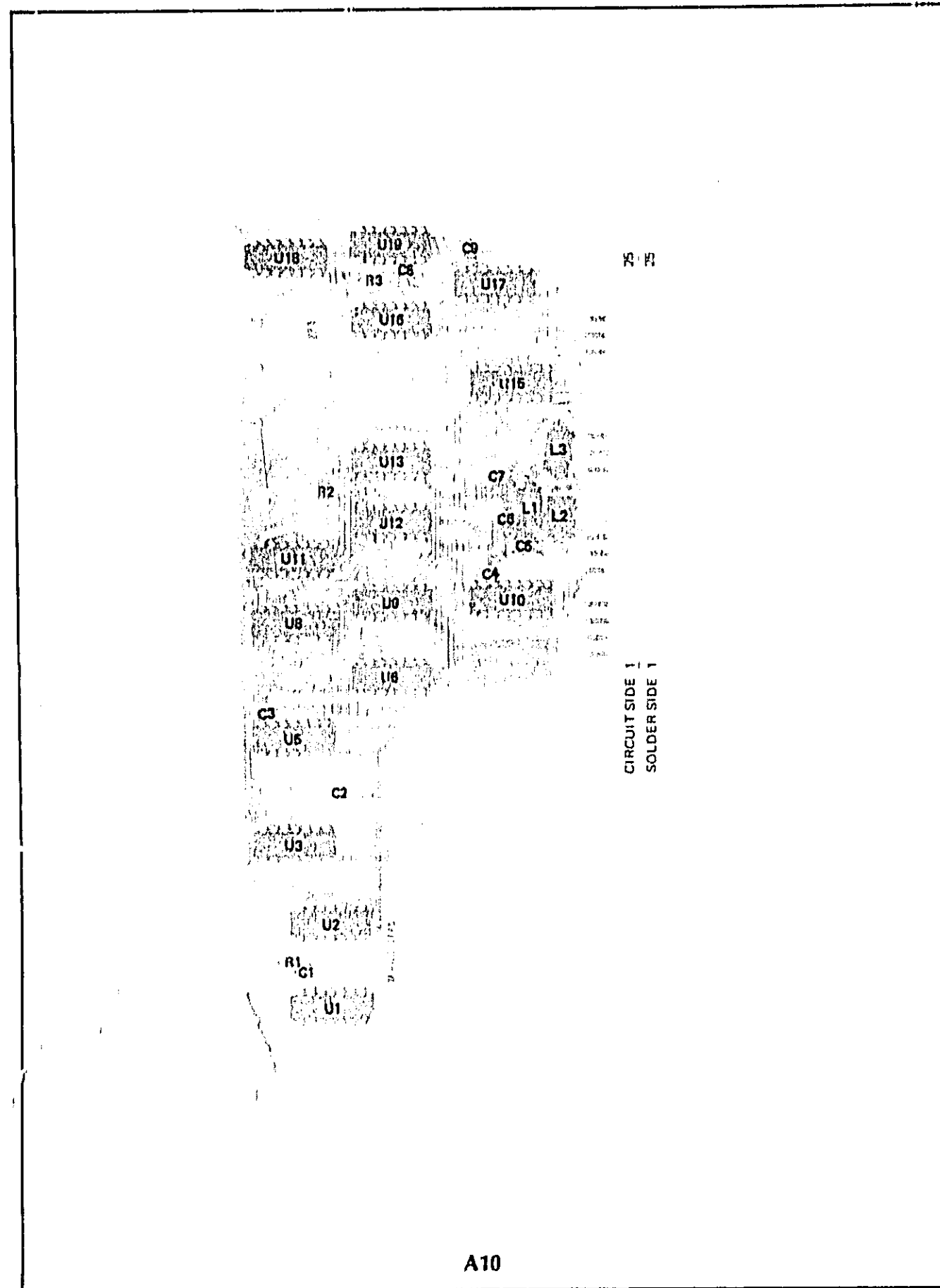


Figure 8-37. A10 Pseudorandom Sequence Generator Assembly

**REFERENCE
DESIGNATIONS**

A11
C1-C20
CR1-CR6
J1-J4
L1-L4
Q1-Q10
R1-R56
TP1-TP10
U1-U5

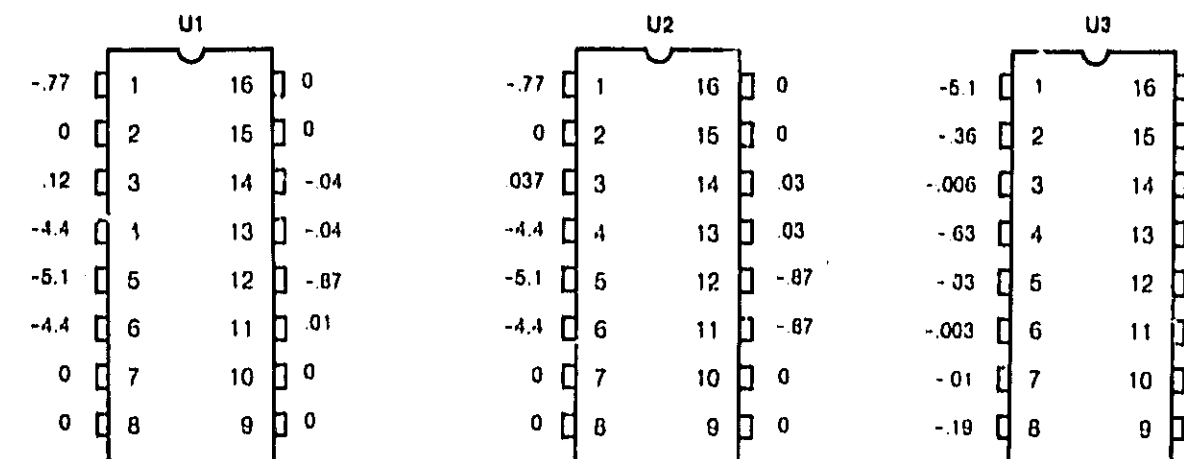
TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfr or Industry Part Number
C1-CR6	1901-1097	Same
Q1-Q6	1854-0215	2N3904
Q7-Q9	1853-0058	832248
Q10	1854-0345	2N5179
U1, U2	1820-2112	Same
U3	1820-0982	Same
U4, U5	1826-0372	Same

Part of Figure 8-38, A11 Signal Switch Assembly

A11 VOLTAGES CONDITIONS FOR VOLTAGE CHECKS, unless otherwise noted

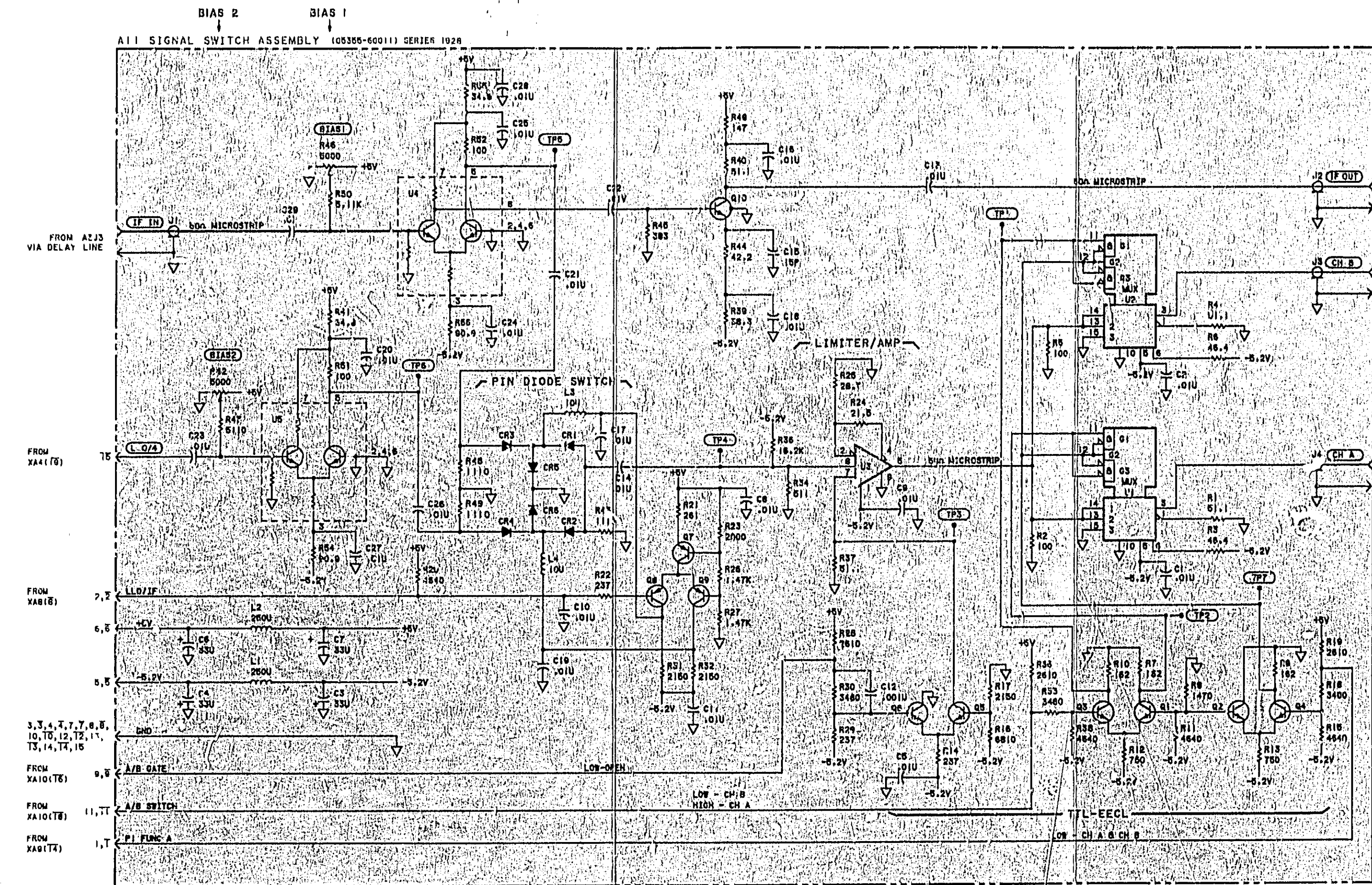
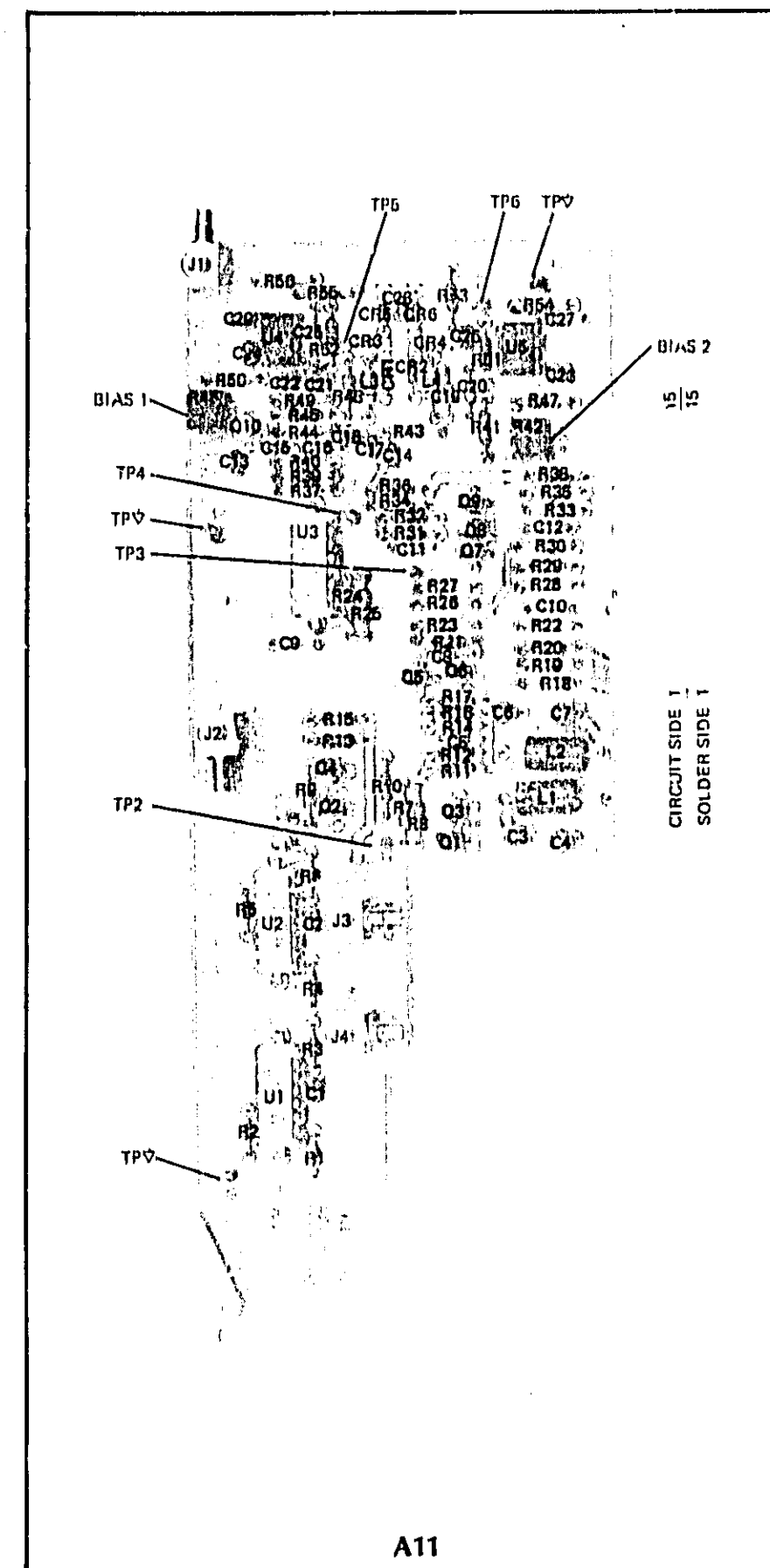
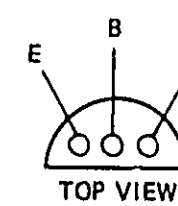
- No signals applied, except where noted.
- RF head input installed.
- RF head input active.
- 5355A in MANUAL mode to enable readings free from PRS variations.



*Will vary with setting of J4C

*Will vary with setting of R47

Q1	Q2	Q3	Q4
E -1.04	E -1.03	E -1.04	E 1.03
B -1.23	B -1.23	B -3.3	B -3.6
C -0.1	C 0	C -3.7	C -8.7
Q5	Q6	Q7	Q8
E -2.02	E -2.02	E 3.63	E 2.16
B -1.32	B -2.06	B 2.97	B 4.9
C 6.7	C 0	C 2.16	C -1.63
Q9	Q10		
E 2.16	E -9.06		
B 1.60	B -1.26		
C .78	C 2.03		
	CAS 0		



- NOTES
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
 2. UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN MICROFARADS
INDUCTANCE IN MICROHENRIES.

Figure 8-38. A11 Signal Switch Assembly

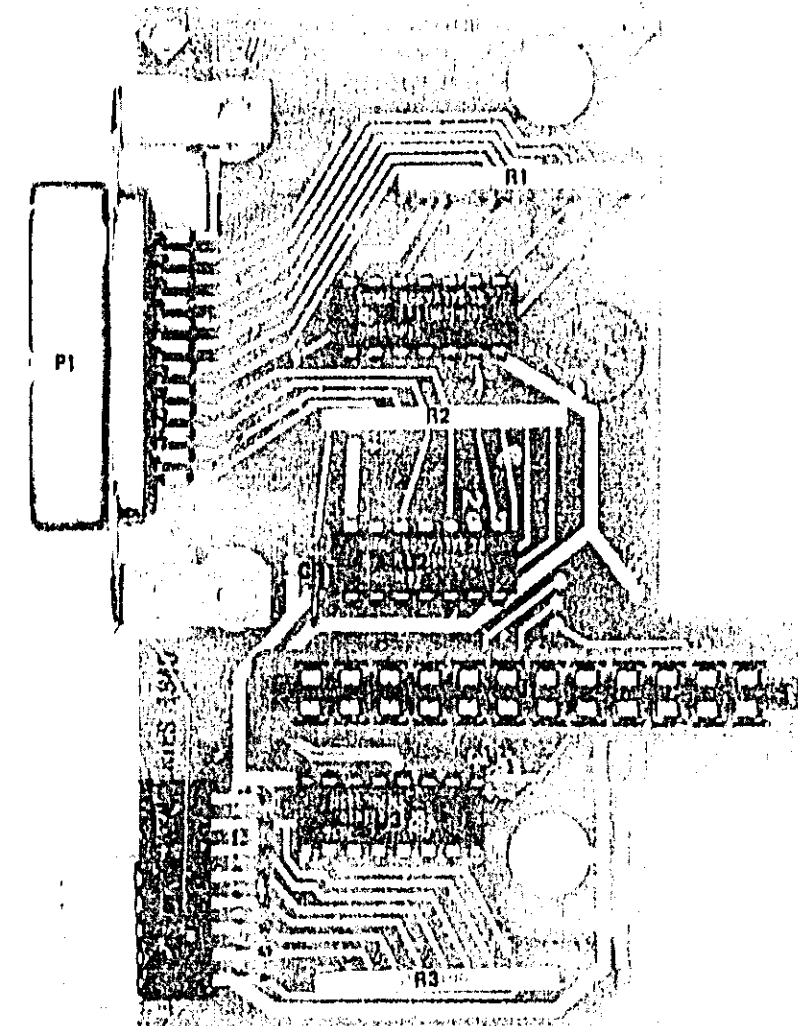
REFERENCE
DESIGNATIONS

A12
CR1 J1 P1 R1-R3 S1 U1-U3

TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfr or Industry Part Number
CR1	1901-0535	Same
U1, U2	1820-1109	SN74LS04N
U3	1820-1419	SN74LS85N

Part of Figure 8-39. A12 HP-IB Input Assembly



A12

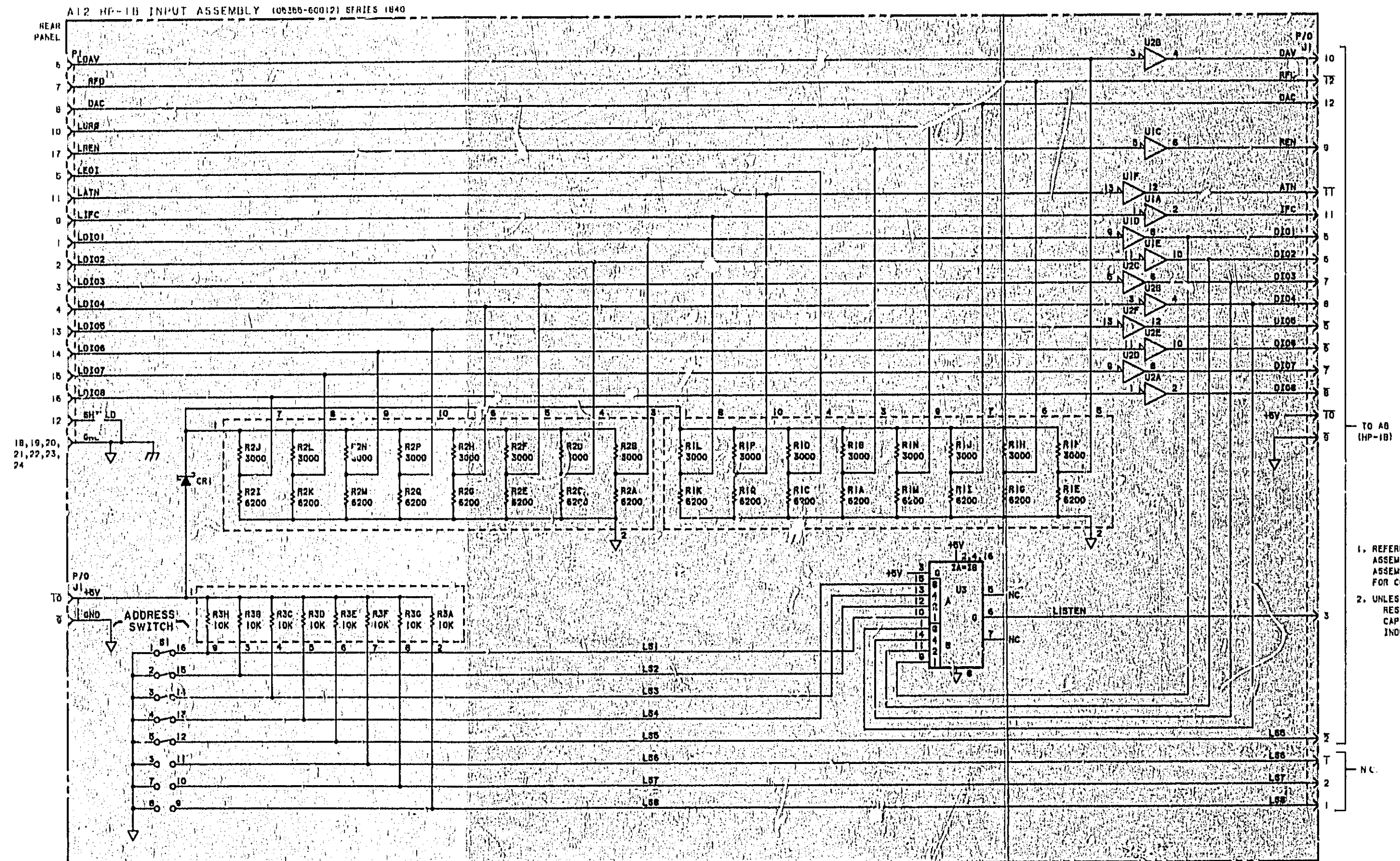


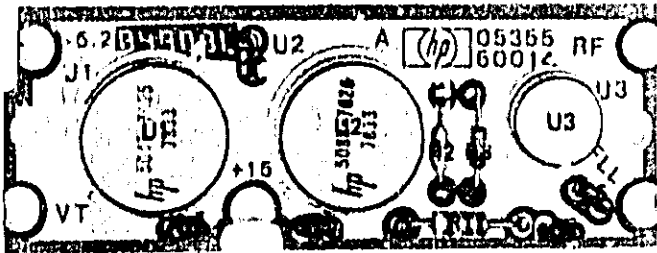
Figure 8-39. A12 HP-IB Input Assembly

REFERENCE
DESIGNATIONS

A14
C1-C5
R1-R3
U1-U3

TABLE OF ACTIVE ELEMENTS

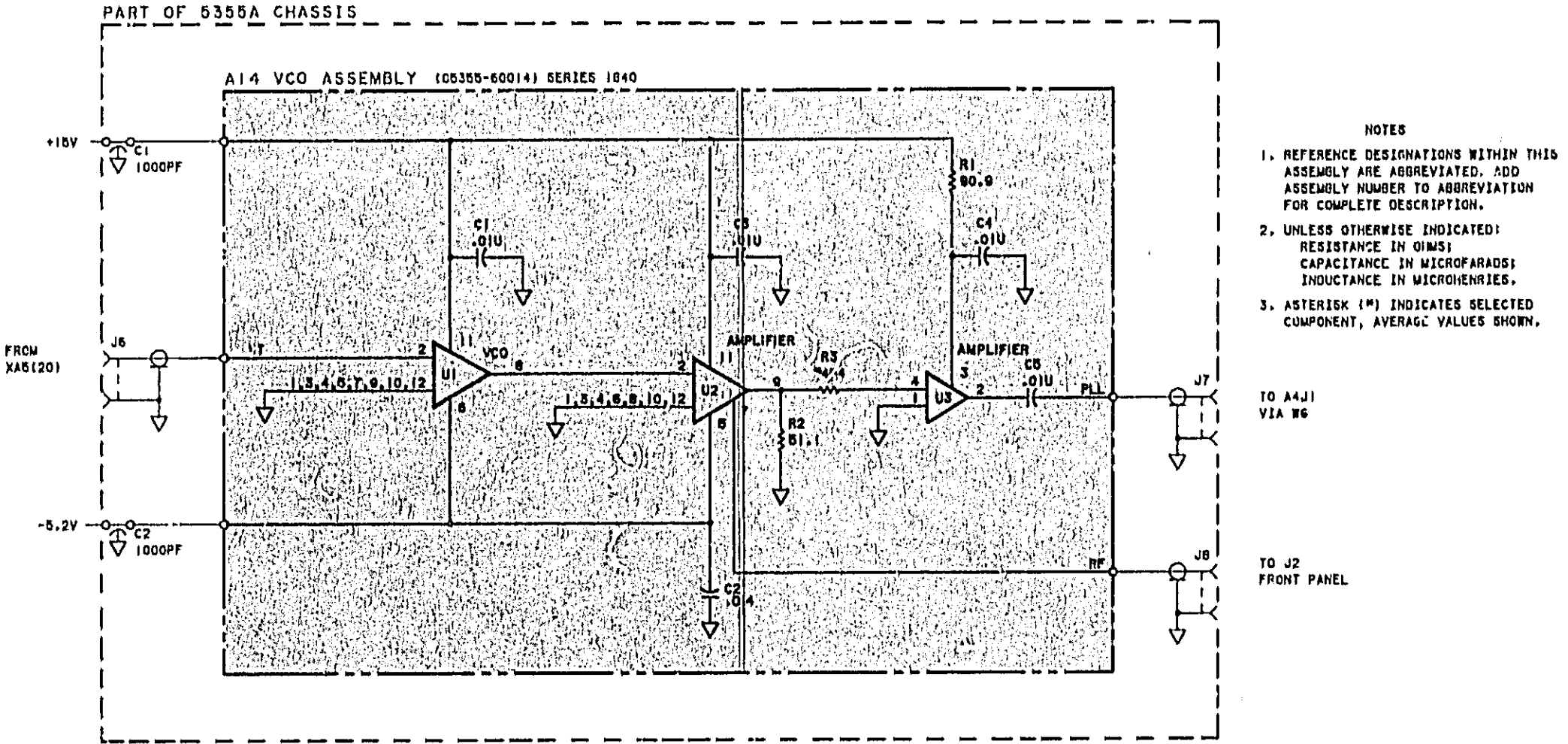
Reference Designation	HP Part Number	Mfr or Industry Part Number
U1	5088-7025	Same
U2	5088-7026	Same
U3	5088-7017	Same



NOTE:
U1 AND U2—PLUGGED IN
U3—SOLDERED IN

A14

Figure 8-40. A14 Voltage Controlled Oscillator Assembly



- NOTES
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
 2. UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS;
CAPACITANCE IN MICROFARADS;
INDUCTANCE IN MICROHENRIES.
 3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN.

TO A4J1
VIA W6

TO J2
FRONT PANEL

Figure 8-40. A14 Voltage Controlled Oscillator Assembly

REFERENCE DESIGNATIONS

A1	A2	CHASSIS PARTS
C1, C2 J1 U1	C1-C5 J1 R1, R2 U1	J1 U1 U2

TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfr or Industry Part Number
	A1	
U1	5088-7027	Same
	A2	
U1	5068-7017	Same
	CHASSIS PARTS	
U1	5088-7031	Same
U2	5088-7029	Same

Part of Figure 8-41, 5356A/B/C Frequency Converter Head Assembly

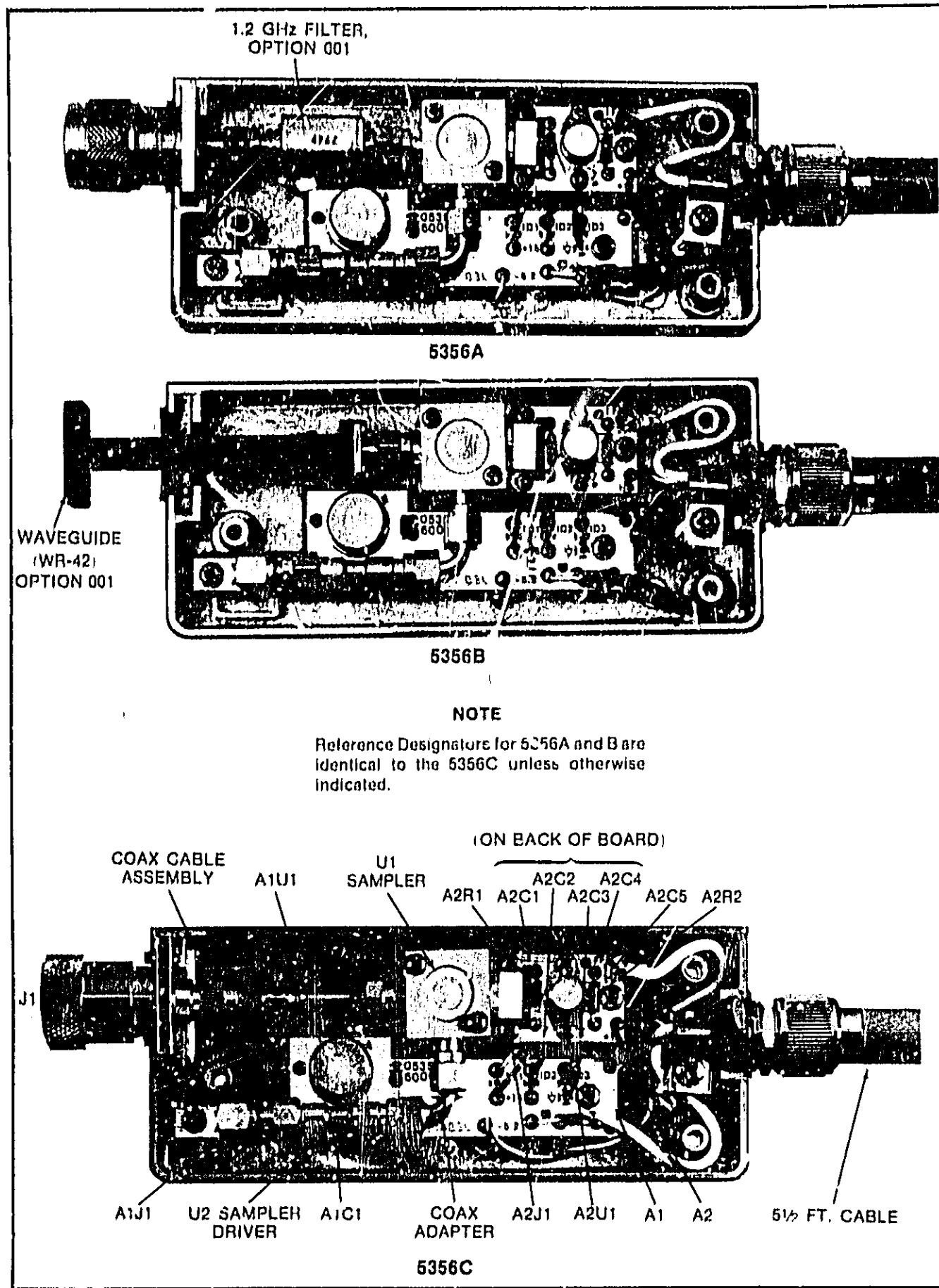
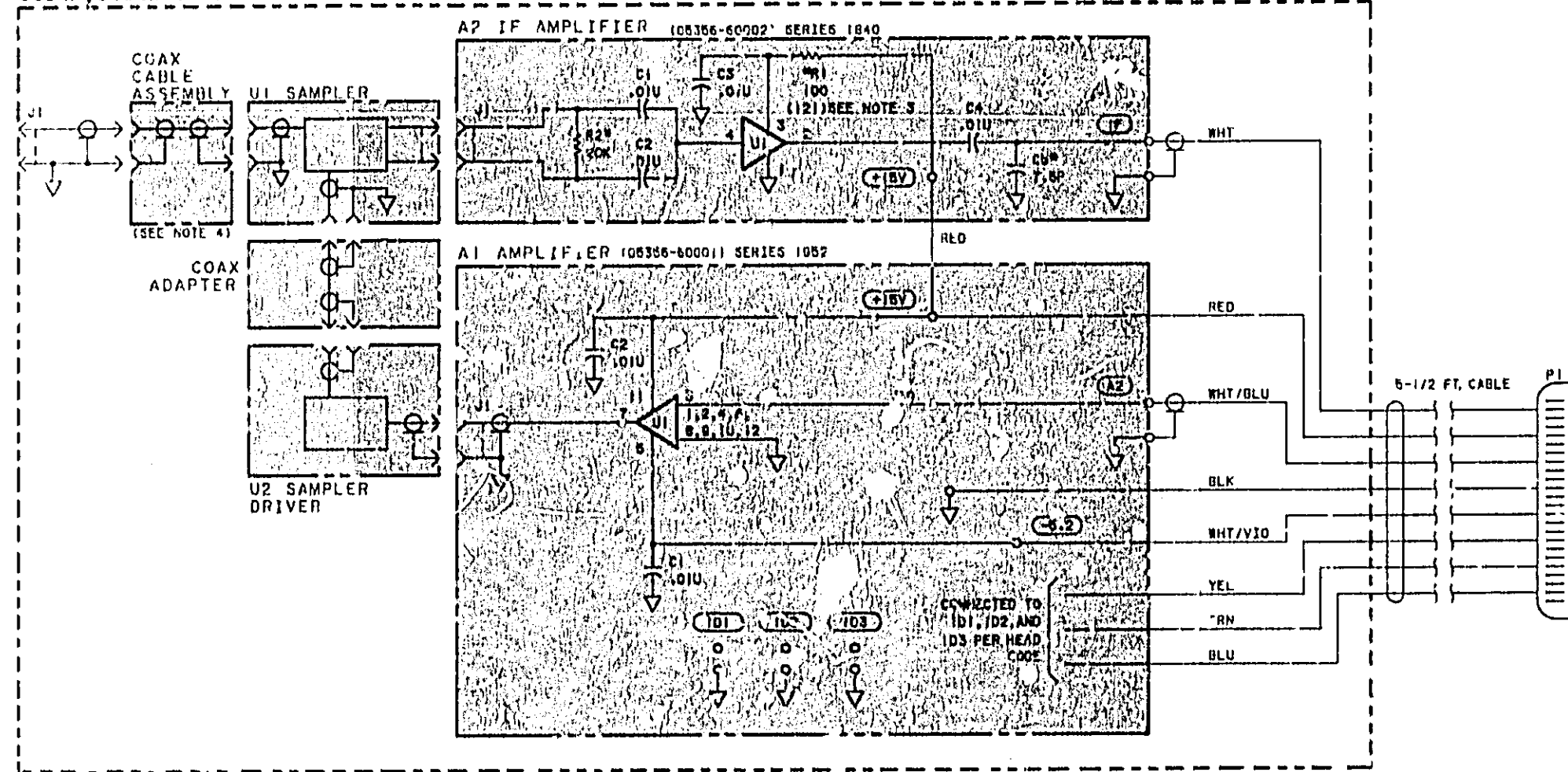


Figure 8-41. 5356A/B/C Frequency Converter Head Assembly

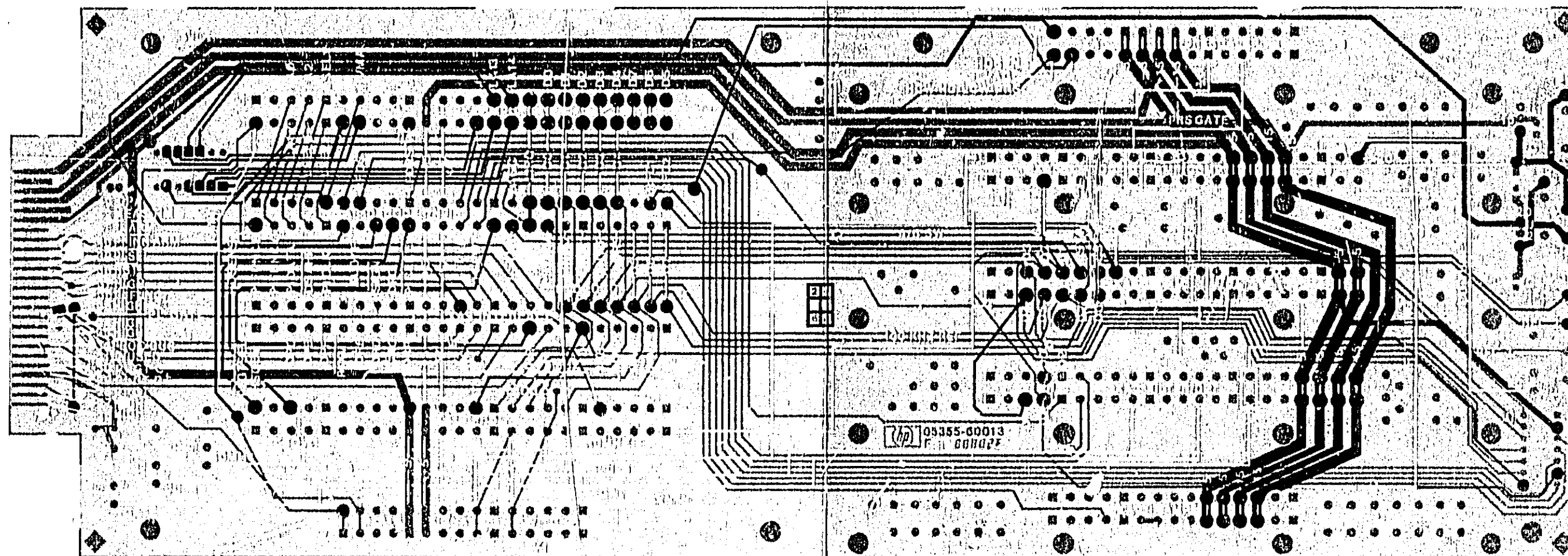
5356A, 5356B OR 5356C FREQUENCY CONVERTER HEAD ASSEMBLY



NOTES:

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS;
CAPACITANCE IN FARADS;
INDUCTANCE IN HENRIES
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT, AVERAGE VALUE SHOWN. THE AVERAGE VALUE OF R1 FOR THE 5356C IS 121 OHMS
4. THE COAX CABLE ASSEMBLY IS REPLACED WITH A 1.2 GHz HIGH-PASS FILTER FOR OPTION 001, 5356A

Figure 8-41. 5356A/B/C Frequency Converter Head Assembly



LAYERS NOT SHOWN

- 1 Component Side Ground Plane
- 3 Intermediate Layer Ground Plane
- 4 Intermediate Layer Ground Plane

LAYERS SHOWN

- Intermediate Layer Circuit
- Intermediate Layer Circuit
- Circuit Side (Traces)
- Circuit Side (Nomenclature)

A13 MOTHERBOARD INTERCONNECTIONS

MANUAL CHANGES

MANUAL UPDATING CHANGES

CHANGE DATE: May 22, 1985

***** MANUAL UPDATING COVERAGE*****

* This supplement adapts your manual *
* to instruments with serial numbers *
* prefixed through 2429. *

***** MANUAL IDENTIFICATION*****

* Instrument: HP 5355A *
* Automatic Frequency Converter *
* with 5356A/B/C Frequency *
* Converter Heads *
* Operating & Service Manual *
* Manual Part No: 05355-90013 *
* Manual Microfiche: 05355-90014 *
* Manual Print Date: DEC 1980 *

ABOUT THIS SUPPLEMENT

The information in this supplement is provided to correct manual errors and to adapt the manual to instruments containing changes after the manual print date.

Change and correction information in this supplement is itemized by page numbers corresponding to the original manual pages. The pages in this supplement are organized in numerical order by manual page number.

Manual updating supplements are revised as often as necessary to keep manuals as accurate as possible. Hewlett-Packard recommends that you periodically request the latest edition of this supplement. Free copies are available from all HP offices. When requesting copies quote the model number, print date, and part number listed at the top of this page.

HOW TO USE THIS SUPPLEMENT

Insert this title page in front of the title page in your manual.

Perform all changes specified for "All Serials", and all changes through the Series Prefix of your instrument or board.

Insert any complete replacement pages provided into your manual in the proper location.

If your manual has been updated according to the last edition of this supplement, you need only perform those changes pertaining to the new series prefix. See List of Effective Pages on the reverse side of this page. New information affecting "All Serials" will be indicated by a "N" in the left margin.



MANUAL CHANGES MODEL 5355A (05355-90013)

SERIES PREFIX OR SERIAL NUMBER	PAGES CHANGED
All Serials	1-3, 1-4, 3-7, 3-18, 3-19, 4-17, 5-4, 5-20, 6-21, 6-22, 8-19, 8-56, 8-66, 8-123, 8-139, 8-141, 8-145
2020A 2024A	6-5, 6-8, 6-12, 6-13, 6-23, 8-9, 8-14, 8-123, 8-145
2048A (5355A) 2048A (5356A,C)	6-8, 6-23, 8-123, 8-145 6-26, 8-147
2052	See Next Page of these manual changes.
2102 2116	6-5, 6-12, 8-121, 8-129
2118 (5356A)	6-26
2118 (5356B)	6-27, 8-147
2118 (5356C)	3-18, 3-19, 6-7, 6-24
2132	1-3, 1-4, 5-20, 6-5, 6-8, 6-9, 6-12, 6-13, 6-24, 8-113, 8-115, 8-123, 8-129
2242	3-18, 3-19, 6-7, 6-23, 6-24, 8-145
2429	3-7, 3-18, 6-19, 6-20, 8-140

(5355A) 2020A-2024A=10894, 10897, 10914, 10245/2048A=11389, 11395, 11416, 9860/
2052A=11421/2102-2116A=10848/2118A=11422, 11564, 12169, 11422, 11564, 12169/2132A=
11423, 12097, 11432, 11436/2132A=13104, 13649, 14534/2242A=15385, 16483/2429A=16312
1688!

MANUAL CHANGES MODEL 5355A (05355-90013)

Instruments with the following prefixes also include changes for series 2020A.

1952A00198	2016A00324
2016A00316	2016A00326
2016A00318	2016A00328
2016A00319	2016A00330
2016A00320	2016A00332
2016A00321	2016A00334
2016A00322	2016A00337

Change all references to frequency range 0.4-1.6 GHz to 0.4-1.5 GHz for the following instruments with series prefix 2048 and all instruments with series 2052 or higher:

2048A00416 thru 2048A00419
 00421
 00426
 00429 thru 2048A00432
 00435
 00437
 00440

Page: occurrences:	Page: occurrences:	Page: occurrences:
iv 6	4-3 5	8-19 2
viii 5	4-4 5	8-20 1
1-0 1	4-5 1	8-46 1
1-2 7	4-6 1	8-48 1
1-3 2	4-18 5	8-49 1
1-4 1	4-24 3	8-51 1
1-5 3	4-25 2	8-55 1
3-1 3	4-39 1	8-59 1
3-2 1	5-26 2	8-60 1
3-4 2	5-27 2	8-67 2
3-5 2	5-29 4	8-111 1
3-8 2	5-31 2	8-115 1
3-25 1	5-35 1	8-117 1
4-2 6	8-8 1	8-128 1
front cover 1	back cover fold out 2	

MANUAL CHANGES MODEL 5355A (05355-90015)

SERIAL PREFIX OR
SERIES NUMBER

CHANGES

Page 1-3, Table 1-1. Model 5355A Specifications:

All Serials	>Delete the asterisk(*) next to 5355A, under PULSE MODE column. >Delete the Min Pulse Width, in the 5355A column, to 150ns. >Delete, at the bottom of the page, "Specifications apply only to external gating of 5345/5355".
2132A	>Change the MAN MODE specification from "60ns" to "75ns" in the area labeled "PULSE MODE" "Pulse Width" "MIN". >Change the "PULSE MODE" "Accuracy" specification (lower right-hand corner) from "(.00EYT GATE WIDTH)" to "(.12/EXT GATE WIDTH)".

Page 1-4, Table 1-1. Model 5355A Specifications:

All Serials	>Change maximum Operating Temperature to 55 degrees.
2132A	>Change 40ns to 65ns under DEFINITIONS, rms jitter=.

Page 3-7. Operation and Programming:

All Serials	>Add to the end of paragraph 3-29: "It should be noted that the 5355A, when used in conjunction with the 5356C Frequency Converter Head, will always be in the special FM mode. Use of the special FM mode with the 5356C head is necessary to ensure proper harmonic number determination at frequencies above 26.5 Ghz."

SERIAL PREFIX OR
SERIES NUMBER

CHANGES

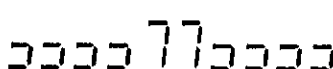
Page 3-18. Operation and Programming:

All Serials >Add note following paragraph 3-54:

NOTE

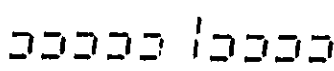
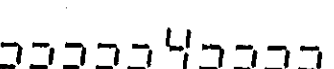
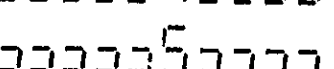
The 5355A, when used in conjunction with the 5356C Frequency Converter Head, will always be in the special FM mode.

2242A >Replace the Display/Error Condition table with the following table:

DISPLAY	ERROR CONDITION
 (CW Automatic only)	5345A rear panel GATE CONTROL INPUT switch in wrong position. Should be in INTERNAL position.
	Harmonic number (n)=0 due to a low input frequency or due to the CHECK/COM A/SEP switch on 5345A front panel in CHECK position. Should be in COM A or SEP
	Indicates the CHECK/COM A/SEP switch on 5345A front panel in CHECK position. Should be in COM A or SEP.

Page 3-19, Paragraph 3-56. CONVERTER CODES:

2242A >Replace the Display/Head Installed table with the following table:

DISPLAY	HEAD INSTALLED
	5356A (1.5—18 GHz)
	5356B (1.5—26.5 GHz)
	5356B Option 001 (18-26.5 GHz)
	5356C (1.5—40 GHz)
	5356C Option 001 (26.5-40 GHz)

MANUAL CHANGES MODEL 5355A (05355-90013)

SERIAL PREFIX OR
SERIES NUMBER

CHANGES

Page 4-17. Performance Tests:

All Serials Paragraph 4-30. TEST 2. MANUAL MODE:
 >Change "60 ns PULSE WIDTH" to "75 ns PULSE WIDTH".
 Step a. waveform figure:
 >Change "60" to "75" in both occurrences.
 >Change "-9.2 dB" to "-8.2 dB".

Page 5-4. Adjustments:

All Serials >Change display from =====I===== to =====IC=====
 in paragraph f.

Page 5-5. Adjustments:

All Serials >Change display from =====I===== to =====I=====
 in paragraph i.

Page 5-20. Adjustments:

All Serials >Change "A2J3" to "A3J3" in paragraph 5-24, step a.
 >Change "A2J2" to "A3J2" in paragraph 5-24, step a.
 >Change paragraph 5-24, step b to read as follows:

 b. Set 8640A for CW output of 200 MHz at -20 dBm. Press
 the Manual measurement key. Observe that the 5355A
 Signal light comes on and the 5345A displays 1 57 GHz.

 >Change "77.5" to "107.5" and "79.5" to "109.5" in step c.

2132A

Step C, top of page:
>Change A3R23 (78) to A3R23 (108).

Paragraph 5-24, FINAL TUNING OF FILTERS:
>Change 80 MHz to 110 MHz in step c.
>Change 77.5 to 107.5 and 79.5 to 109.5 in step e.
>Change 78 MHz to 108 MHz in step i.

Page 6-4. Table 6-2. A1 Front Panel Control Assy Replaceable Parts:
(05355-60001)

2242

Delete 1200-0473 SOCKET-IC 16-CONT DIP-DIP-SLDR.
Delete 1200-0525 SOCKET-IC 20-CONT DBL STRP DIP-SLDR.

6

MANUAL CHANGES MODEL 5355A (05355-90013)

SERIAL PREFIX OR
SERIES NUMBER

CHANGES

Page 6-5, Table 6-2, A2 Limiter Amplifier Assembly Replaceable Parts:

- 2020A >Add an asterisk (*) to part designator A2CR1 to indicate a factory-selected part.
>Add "1901-0852 preferred part" for A2CR1 (1901-0856 is still an acceptable part for A2CR1).
- 2102A >Change A2 (05355-60002) SERIES to 2102.
>Change A2C4 from 0160-4743 to 0160-4279 CAPACITOR-FXD 470pF 400V.
- 2132A >Delete A2CR1, 1901-0856, Alternate Part.

Pages 6-8/6-9, Table 6-2, A3 Filter Detector Assembly Replaceable Parts:

- 2020A >Add an asterisk (*) to A3C8 to indicate a factory-selected value. (Typical value 3.9 to 4.3 pf).
- 2048A >Change A3 (05355-60003) SERIES from 1952 to 2048.
>Add an asterisk (*) to A316 to indicate a factory-selected value.
>Change A3C16 from 0160-3875 (22pF) to 0160-4254 CAPACITOR-FXD 24pF 200V.
- 2132A >Change A3 (05355-60003) SERIES to 2132.
>Change A3C10 and A3C18 to 0160-4493 CAPACITOR-FXD 27PF 200VDC CER 0+-30.
>Change A3C16 to 0160-4385 CAPACITOR-FXD 15PF 200VDC CER 0+-30.
>Change A3C34 to 0160-4511 CAPACITOR-FXD 220 PF +-5% 200VDC CER.
>Change A3L3 and A3L4 to 05355-80001, coil 40nH.
>Delete A3L14 9100-2250 INDUCTOR RF-CH-MLD 180NH 10%.
>Change A3R20 to 2100-3941 RV 10K 4-TURN POTENTIOMETER.
>Change A3R23 to 2100-2061 RESISTOR-TRMR 200 10% C TOP-ADJ 1-TRN.
>Change the number "78" below A3R23 to "108".
>Change *A3R32 and *A3R40 to 0698-7223 RESISTOR 287 1% .05W F TC=0+-100.
>Add A3R41 0698-7206 RESISTOR 56.2 1% .05W TC=+-100.

MANUAL CHANGES MODEL 5355A (05355-90013)

SERIAL PREFIX OR
SERIES NUMBER

CHANGES

Pages 6-12/6-13, Table 6-2. A6 Prescaler Assembly Replaceable Parts:

- 2020A >Change A6 (05355-60006) SERIES to 2020.
>Add an asterisk (*) to Reference Designators A6CR8 and A6CR10 to indicate factory-selected parts.
>Add "1901-0852 preferred part" for A6CR8 and A6CR10. (1901-0856 is still an acceptable replacement part for A6CR8 and A6CR10.)
>Change A6R38 from 2100-1986 (1K) to 2100-3888 RV 1K 10% 4-Turn.
>Change A6R44 from 2100-1738 (10K) to 2100-3216 RV 10K 10% 4-Turn.
- 2102A >Change A6 (05355-60006) SERIES to 2102.
>Change A6C34 from 0160-4743 to 0160-4279 CF 470pF 400V.
- 2132A >Change A6 from 05355-60006 to 05355-60026 Series 2132.
>Add A6C62 and A6C63 0180-0228 CAPACITOR-FXD 22UF +1H_10% 15VDC.
>Change A6R42 to 2100-3216 RESISTOR-TRMR 10K 10% C TOP-ADJ 4-TURN.
>Add heat sinks to transistors Q3 and Q4 (spread to allow clearance).
>Add A6R49 0698-7248 RESISTOR 3.16K 1% .05W F TC=0+-100.
>Add A6R50 0698-7212 RESISTOR 100 1% .05W F TC=0+-100.
>Add A6Q5 1854-0246 TRANSISTOR NPN.
>Change A6R3* to 0698-7222 RESISTOR 261 1% .05W TC=0+-100.

Page 6-15, Table 6-2. A7 Microprocessor Assembly Replaceable Parts:

- 2242A >Delete A7XU2, XU3, XU14 1200-0525 IC-SOCKET-IC 20-PIN.
>Delete A7U10, U12, 1200-0539 IC-SOCKET 18-PIN.

Pages 6-19/6-20, Table 6-2. A11 Signal Switch Assembly Replaceable Parts:

- 2429A >Change A11 (05355-60011) SERIES to 2429.
>Change A11U3 from 1820-0982 to 1DD8-0502 IC-DIG SPECIAL.

Page 6-21, Table 6-2. A12 HP-IB Input Assembly Replaceable Parts:

- All Serials >Change A12P1 from 1251-3283 to 1252-0324 CONNECTOR, 24-PIN.

MANUAL CHANGES MODEL 5355A (05355-90013)

SERIAL PREFIX OR
SERIES NUMBER

CHANGES

Page 6-22, Table 6-2, A13 Motherboard Replaceable Parts:

All Serials >Delete A13J2 1200-0548 SOCKET-IC 14-CONT DIP DIP-SLDR,
Qty 8,
>Change A13J1 quantity from 2 to 1.

Page 6-23, Table 6-2, A14 Voltage Control Oscillator VCO Assy Replaceable Parts:

2020A >Change A14 (05355-60014) SERIES from 2016 to 2020.
>Add A14R4 0698-8382 RESISTOR 25 OHMS.

NOTE

This chip Resistor is soldered on the back of the board and is not recommended as field serviceable.

>Add A14R5* factory selected typical value 51.1 Ohms.

2048A >Change A14 (05355-60014) SERIES to 2048.
>Change A14R2 to 0698-8630 RESISTOR 50-OHM (Not replaceable).
>Delete 0360-0089 Solder Lug.

2132A The following instruments with series number 2132 include changes listed for Series 2242.

2132A00895	2132A00916
00896	00917
00902	00919 thru 00921
00904 thru 00906	00923
00910 thru 00914	00924

2242A >Change A14 (05355-60014) SERIES to 2242.
>Add R6* 0698-7277 RESISTOR 51.1K 1% .05W F TC=0+-100.

>Change *R6 from 0698-7277 to 0698-7284 RESISTOR 100K 1% .05W F TC=0+-100.

MANUAL CHANGES MODEL 5355A (05355-90013)

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Page 6-24, Table 6-2. Replaceable Parts - Chassis Parts:

All Serials >Add 5021-3769 HANDLE-DRAWER LATCH.

2102A The following instruments with serial prefix 2102A have the delay line changes listed for Series 2132.

2102A00046	2102A00475	2102A00485
00467	00479	00486
00471	00480	00488
00472	00483	00490
00474	00484	

2132A >Change DL1 to 05355-80018 60ns DELAY LINE.
>Add DL2 05355-80019 14ns DELAY LINE.
>Delete W14 05355-60111 Cable Assembly Prs Out.

2242A >Change J2 from 5020-3529 to 08410-20065 Nut-Hex.
>Change INSULATOR-XSTR THRM-CNDCT from 0340-0864 to 0340-0620.

Page 6-26, Table 6-3. 5356A 18GHz Frequency Converter Head Replaceable Parts:

5356A,C 2048A >Change A1 (05356-60001) SERIES to 2048A.
>Add A1R1* 0698-5378 RESISTOR 100 10% .1W C TC=0+-200.

5356A,C 2118A >Add Option 006; 5088-7049 26.5GHz Limiter.
>Add 1250-1742, Option 006 Adapter Connector.

5356A 2118A >Change A1 (05356-60001) SERIES to 2118.
>Change A1R1* to 0698-7212 RESISTOR 100 1% .05W F TC=0+-100.

Page 6-27, Table 6-4. 5356B 26.5GHz Frequency Converter Head Replaceable Parts:

5356B 2118A >Add Option 006; 5088-7049 26.5GHz LIMITER.
>Add 05356-20208 OPTION 005 COLLAR-CONNECTOR.
>Add 05356-20209 OPTION 006 SUPPORT COLLAR.

A1 Amplifier:
>Change A1R1* from 0757-0401 to 0698-7212 RESISTOR 100 1% .05W F TC=0+-100.

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CHANGES

Page 6-28, Table 6-5. Model 5356C 40 GHz Frequency Converter Head
Replaceable Parts:

5356A,C 2048A >Change A1 (05356-60001) SERIES to 2048A.
>Add A1R1* 0698-5378 RESISTOR 100 10% .1W C TC=0+-200.
(Factory-selected value, typical value shown)

Page 8-9, Paragraph 8-25:

2020A >Change "75 to 375 MHz" to "108 to 375 MHz" in first line.

Page 8-13, Paragraphs 8-48, 8-51, and 8-53.

2132A >Change 78MHz to 108MHz.

Page 8-14, Paragraphs 8-52:

2020A >Change 78 to 375MHz to 108 to 375 MHz, in part D0,
second line.

Page 8-15, Paragraph 8-53:

2020A >Change 78 to 375MHz to 108 to 375MHz, in the first line.

Page 8-19, Paragraph 8-86. Circuit Analysis:

All Serials >Change CR53, CR54 and CR55 to C53, C54 and C55.

Page 8-56, Table 8-12. Troubleshooting the Prescaler Input: PRF Mode -

All Serials >Change the descriptions for the photos in step "1.d" as
follows:
"No Prescaler Input" should read "PRF Just Visible"
"PRF Just Visible*" should read "No Prescaler Input".
"Input Freq. Near Oscillation" should read "Higher End of
Band*".
"Higher End of Band*" should read "Input Freq. Near
Oscillation".

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Page 8-66, Table 8-15. Synthesizer Loop Troubleshooting:

All Serials Step 1, Oscilloscope settings under CRT figure:
 >Change setting from 5ns/div to 5 us/div.

Page 8-115, Figure 8-26. A13 Motherboard and Related Parts:

All Serials >Delete W14.

Page 8-121, Figure 8-29. A1 IF Amplifier Assembly Schematic Diagram:

2102A >Change A1 SERIES at top of schematic diagram to 2102.

Page 8-123, Figure 8-30. A3 Filter Detector Assembly Schematic Diagram:

All Serials >Change the part number in the upper left-hand corner of
 the schematic from (05355-60007) to (05355-60003).

2020A >Change A3 SERIES to 2020A.
 >Add and asterisk (*) to C8 to indicate a factory-selected
 value.

2048A >Add an asterisk (*) adjacent to C16 to indicate a factory-
 selected value.
 >Change C16 from 22pF to 24pF.

2102A The following instruments with serial prefix 2102A
 have the delay line changes listed for Series 2132.

2102A00046	2102A00475	2102A00485
00467	00479	00486
00471	00480	00488
00472	00483	00490
00474	00484	

2132A >Add "14ns delay line" in front of "A13E7" at the Prescaler
 Input, on the left side of the schematic.
 >Change C10 and C18 value to 27pF.
 >Change C16 value to 15pF.
 >Change C34 value to 220pF.
 >Change L3 and L4 value to 40nH.
 >Delete L14.
 >Change R23 value to 200 ohms.
 >Change R32 and R40 value to 287 Ohm*.
 >Add R41 between K1(7) and C49.
 >Change "78" to "108" on component locator, below R23.

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Page 8-129, Figure 8-33. A6 Prescaler Assembly Schematic Diagram:

- 2102A >Change A6 SERIES to 2102.
- 2132A >Change A6 from 05355-60006 to 05355-60026, Series 2116.
>Add C62, 22uf from U1 Pin 14 to ground.
>Change the value of R3* to 261 ohms.
>Add R42 to 10K.
>Add the emitter follower circuit shown in Figure 1, between U1(11) and TP1.

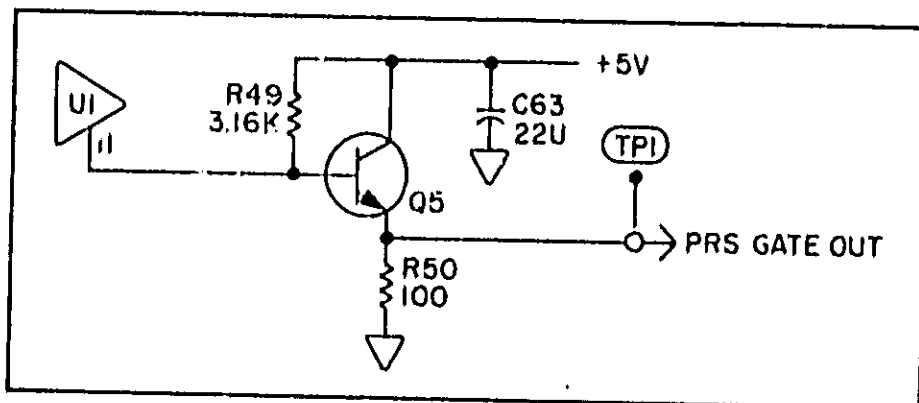


Figure 1. Emitter Follower Circuit (Part of A6)

Page 8-139, Figure 8-37. A10 Pseudorandom Sequence Generator Assembly:

- All Serials >Replace A10 Component Locator with new A10 Component locator supplied in these manual changes.
>Change A10 schematic diagram reference designations as follows: C6 should be C7
C5 should be C6
C4 should be C5

Pages 8-140/8-141. Figure 8-38, A11 Signal Switch Assembly:

- All Serials >Change R39 value to 237 ohms.
- 2429A >Change A11 SERIES to 2429.

Table of Active Elements:

- >Change U3 from 1820-0982 to 1DD8-0502.

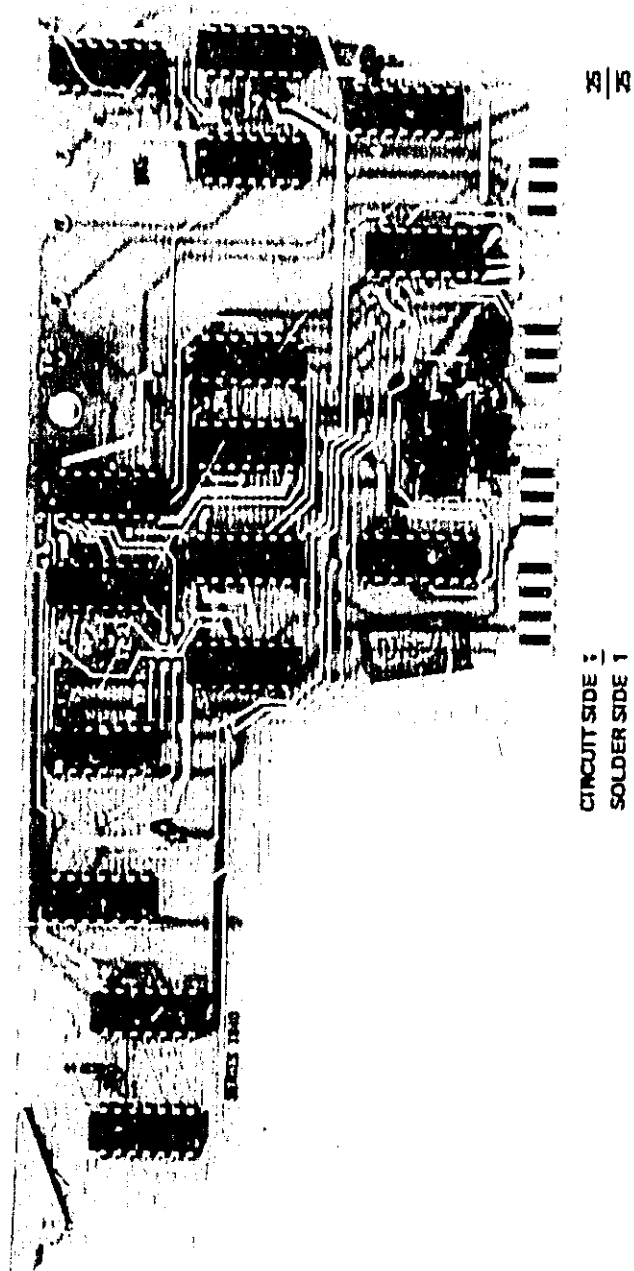


Figure 8-37
A10 Pseudorandom Sequence Generator Component Locator

Part of Page 8-139

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SERIES NUMBER

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Page 3-145, Figure 8-40. A14 Voltage-Controlled Oscillator Assembly:

2020A

- >Change A14 SERIES from 2016 to 2020.
- >Add R4 (25 Ohms) in series with U2 Pin 7 and J8 one inch to the left of the node marked RF.

NOTE

This chip resistor is soldered on back of board, and is not recommended as field serviceable.

- >Add R5 from ground to the line between U2 Pin 7 and J8 to the left of the node marked RF. Label it 51-ohm, factory-selected. R5 is factory-installed if required. Typical values range from 23.7-ohms to 110-ohms. If R5 is installed it is soldered from J8 to a solder lug attached to the circuit board by the screw near U3.

2048A

- >Change A14 SERIES to 2048.
 - >Change A14R2 to 50-ohm.
 - >Add under A14 component locator:
- NOTE: A14 photo does not show series 2048 changes.

Page 8-145, Figure 8-40. A14 Voltage-Controlled Oscillator Assembly (Cont'd):

All Serials

- >Change A14 component locator reference designation R2 to R3 and R3 to R5.

2132A

Instruments with the following serial numbers include changes listed for Series 2242.

2132A00895

00896

00902

00904 thru 00906

00910 thru 00914

2132A00916

00917

00919 thru 00921

00923

00924

2242A

- >Change A14 SERIES to 2242.
- >Add *R6 51.1K between U1Pin2 and C1 at the 15V line.
- >Change *R6 value from 51.1K to 100K.

Page 8-147, Figure 8-41. 5356A/B/C Frequency Converter Head Assembly:

All Serials

5356C Component Locator:

- >Change "A2R1" to "A2R2" and "A2R2" to "A2R1".

5356A/C 2048

- >Change SERIES to 2048.
- >Add A1R1* (100 ohms) from U1(7) to common.

5356B 2118

- >Change SERIES to 2118.
- >Add A1R1* (100 ohms) from U1(7) to common.