Errata

Title & Document Type: 5343A Microwave Frequency Counter Operating and Service Manual

Manual Part Number: 05343-90007

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HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

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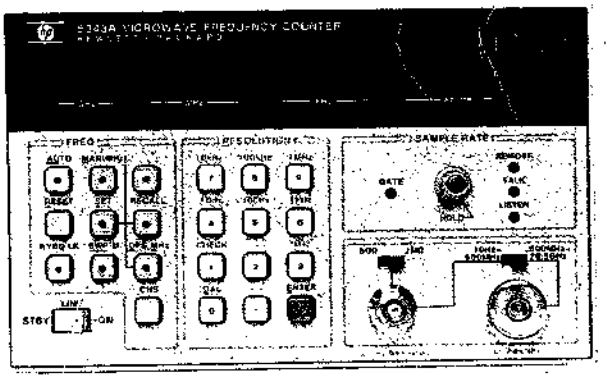
Agilent Technologies

OPERATING & SERVICE MANUAL

5343A Microwave Frequency Counter

General Information
Installation
Operation
Performance Tests
Adjustments
Replaceable Parts
Manual Changes
Service



HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

5343A
Microwave Frequency Counter

SERIAL PREFIX 2014A

This manual applies to Serial Prefix 2014A, unless accompanied by a Manual Change Sheet indicating otherwise.

HEWLETT PACKARD

First Edition — April 1980

MANUAL PART NUMBER 05343-90007
Microfiche Part Number 05343-90008

Printed: APR 1980

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF TABLES

LIST OF FIGURES

LIST OF FIGURES (Continued)

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This manual provides operating and service information for the Hewlett-Packard Model 5343A Microwave Frequency Counter, as shown in *Figure 1-1.*

1-3. SPECIFICATIONS

1-4. Specifications of the 5343A are listed in *Table 1-1.*

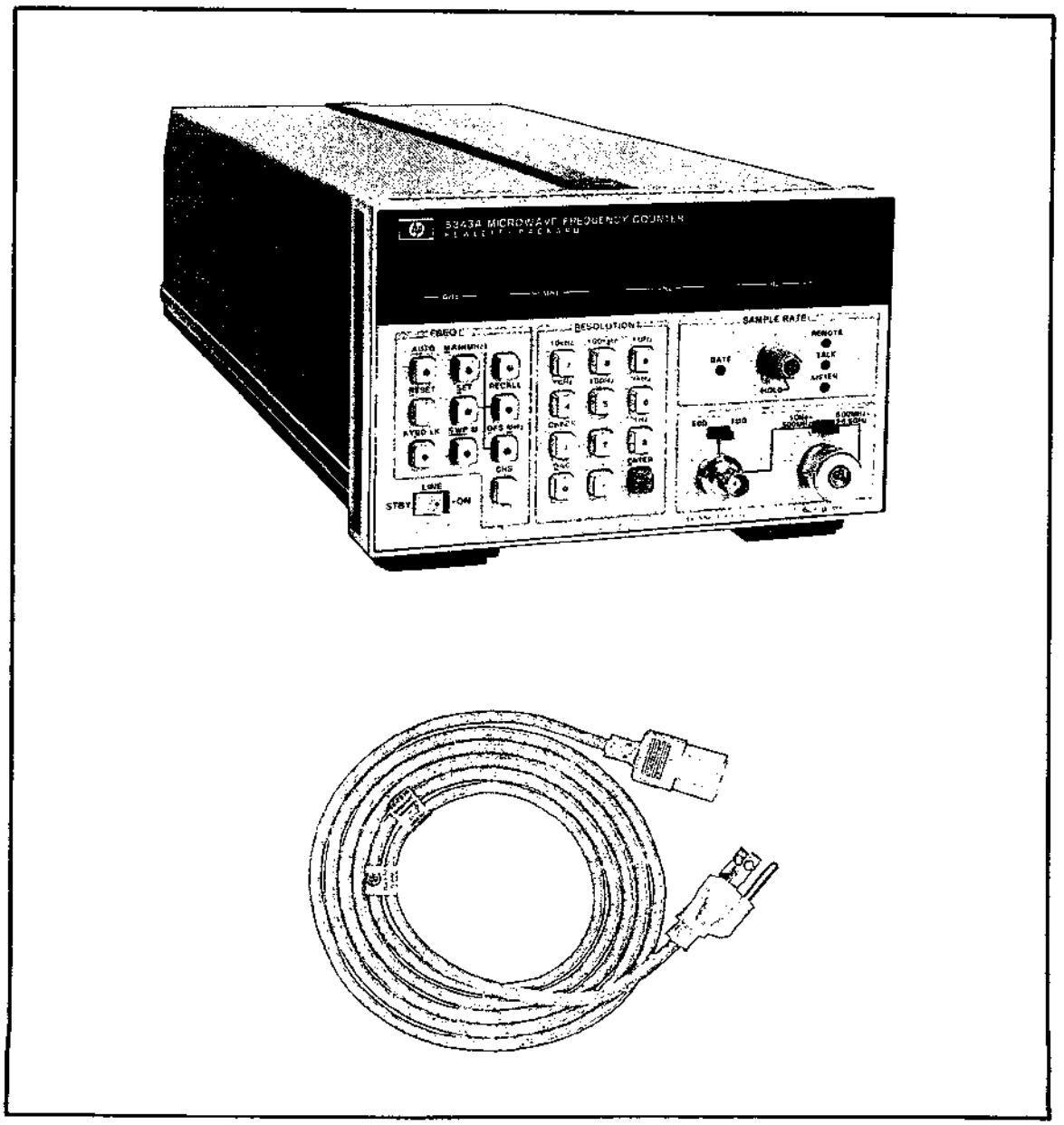


Figure 1-1. Model 5343A Microwave Frequency Counter

Table 1-1. Model 5343A Specifications

INPUT CHARACTERISTICS

INPUT 1:
Frequency Range: 500 MHz—26.5 GHz
Sensitivity:
500 MHz—12.4 GHz −33 dBm
12.4 GHz—18.0 GHz −28 dBm
18.0 GHz—26.5 GHz −23 dBm
Maximum Input: +7 dBm
Dynamic Range:
500 MHz—12.4 GHz 40 dB
12.4 GHz—18.0 GHz 35 dB
18.0 GHz—26.5 GHz 30 dB
Damage Level: +25 dBm, peak
Impedance: 50 ohms, NOMINAL
Connector: APC-3.5 male with collar (SMA compatible)
SWR:
500 MHz—10 GHz <2:1 TYPICAL
10 GHz—18 GHz <3:1 TYPICAL
18 GHz—26.5 GHz <3:1 TYPICAL
Coupling: dc to load, ac to instrument.
FM Tolerance: Switch selectable on rear panel. For modulation rates from dc to 10 MHz.
Wide: 50 MHz p-p worst case
Normal: 20 MHz p-p worst case
Narrow: 6 MHz p-p worst case
AM Tolerance: Any modulation index provided the minimum signal level is not less than the sensitivity specification.
Modes of Operation:
Automatic: Counter automatically acquires and displays highest level signal within sensitivity range.
Manual: Center frequency entered to within ±40 MHz of true value (±25 MHz typical below 825 MHz).
Acquisition Time:
Automatic Mode:
Narrow FM: 200 ms worst case
Normal FM: 530 ms worst case
Wide FM: 2.4 s worst case
Manual Mode:
80 ms after frequency entered.
Automatic Amplitude Discrimination: Automatically measures the largest of all signals present, providing that signal is: 6 dB (TYPICAL) above any signal within 500 MHz; 20 dB (TYPICAL) above any signal, 500 MHz–26.5 GHz.

INPUT 2:
Frequency Range: 10 Hz to 520 MHz Direct Count
Sensitivity: 50Ω: 10 Hz to 520 MHz, 25 mV rms;
1 MΩ: 10 Hz to 25 MHz, 50 mV rms.
Impedance: Selectable: 1 MΩ, <50 pF or 50Ω NOMINAL.
Coupling: ac
Connector: Type BNC female
Maximum Input: 50Ω: 3.5V rms (+24 dBm) 5V dc fuse protected; 1 MΩ: 200V dc +5.0V rms.

TIME BASE

Crystal Frequency: 10 MHz
Stability: Aging rate: $<1 \times 10^{-7}$ per month
Short Term: $<1 \times 10^{-9}$ for 1 s averaging time
Temperature: $<\pm 1 \times 10^{-6}$ over the range of 0°C to 50°C.
Line Variation: $<\pm 1 \times 10^{-7}$ for 10% change from nominal
Ouptut Frequency: 10 MHz, ≥2.4V square wave (TTL compatible); 1.5V p-p into 50Ω available from rear panel BNC.
External Time Base: Requires 10 MHz, 2.0V p-p sine wave or square wave into 1 KΩ, via rear panel BNC connector. Switch selects either internal or external time base.

OPTIONAL TIME BASE OPTION 001

Option 001 provides an oven-controlled crystal oscillator time base 10544A (see separate data sheet), that results in better accuracy and longer periods between calibration.
Crystal Frequency: 10 MHz
Stability: Aging Rate: $<5 \times 10^{-10}$/day after 24-hour warm-up.
Short-Term: $<1 \times 10^{-10}$ for 1 s averaging time
Temperature: $<7 \times 10^{-9}$ over the range 0°C to 50°C
Line Variation: $<1 \times 10^{-10}$ for 10% change from nominal.
Warm-Up: $<5 \times 10^{-9}$ of final value 20 minutes after turn-on, at 25°C.

DIGITAL-TO-ANALOG CONVERTER OPTION 004

Option 004 provides the ability to convert any three consecutive displayed digits into an analog voltage output. A display of 000 produces 0V output; 999 produces 9.99V full scale.
Accuracy: ±5 mV, ±0.3 mV/°C (from 25°C)
Conversion Speed: <50 μs to ±10% of full scale reading
Resolution: 10 mV
Output: 5 mA. Impedance <1.0 ohm
Connector: Type BNC female on rear panel.

GENERAL

Accuracy: ±1 count ± time base error.
Resolution: Front panel pushbuttons select 1 Hz to 1 MHz.
Residual Stability: When counter and source use common time base or counter uses external higher stability time base $<4 \times 10^{-11}$ rms TYPICAL.
Display: 11 digit LED display, sectionalized to read GHz, MHz, kHz, and Hz.
Self-Check: Selected from front panel pushbuttons. Measures 75 MHz for resolution chosen.
Frequency Offset: Selected from front panel pushbuttons. Displayed frequency is offset by entered value to 1 Hz resolution.
Sample Rate: Variable from less than 20 ms between measurements to HOLD which holds display indefinitely.
IF Out: Rear panel BNC connector provides 25 MHz to 125 MHz output of down-converted microwave signal.
Multiply Routine: Selected from front panel pushbuttons. Measured frequency is multiplied by any integer up to 99. Then offset can be added or subtracted for y = mx ±b result.
Totalize: Input 2 can totalize at rate up to 520 MHz. Readout on the fly is controlled by front panel or HP-IB.
External Trigger: TTL type low level or contact closure to ground (>50 μs TYPICAL) at rear panel connector (A) initiates measurements when in sweep mode.
Sweep Mode: Selected from front panel pushbutton. Allows interface to appropriate sweeper for start, stop, and marker frequency measurements.
Operating Temperature: 0°C to 50°C.
Power Requirements: 100/120/220/240V rms (+5, −10%), 48–66 Hz; 100 VA max.
Accessories Furnished: Power cord, 229 cm (7½ ft.).
Size: 133 mm H × 213 mm W × 498 mm D
(5¼" × 8⅜" × 19⅝")
Weight: Net 9.1 kg (20 lbs.). Shipping 12.7 kg (28 lbs.).

1-5. SAFETY CONSIDERATIONS

1-6. This product is a Safety Class I instrument (provided with a protective earth terminal). Safety information pertinent to the operation and servicing of this instrument is included in appropriate sections of this manual.

1-7. INSTRUMENT IDENTIFICATION

1-8. Hewlett-Packard instruments have a 2-section, 10-character serial number (0000A00000), which is located on the rear panel. The four-digit serial prefix identifies instrument changes. If the serial prefix of your instrument differs from that listed on the title page of this manual, there are differences between this manual and your instrument. Instruments having higher serial prefixes are covered with a "Manual Changes" sheet included with this manual. If the change sheet is missing, contact the nearest Hewlett-Packard Sales and Service Office listed at the back of this manual. Instruments having a lower serial prefix than that listed on the title page, are covered in Section VII.

1-9. ACCESSORIES

1-10. *Table 1-2* lists accessory equipment supplied and *Table 1-3* lists accessories available.

Table 1-2. Equipment Supplied

DESCRIPTION	HP PART NUMBER
Detachable Power Cord 229 cm (7½ feet long)	8120-1378

Table 1-3. Accessories Available

DESCRIPTION	HP PART NUMBER
Bail Handle Kit	5061-2002
Rack Mounting Adapter Kit (Option 908)	5061-0057
Rack Mounting Adapter Kit with slot for access to front connectors from rear.	K70-59992A
Transit Case	9211-2682
Service Accessory Kit (refer to paragraph 1-16)	Model 10842A
APC-3.5 Connector Adapter (Female-to-female)	1250-1709
Signature Analyzer	Model 5004A

1-11. DESCRIPTION

1-12. The 5343A Microwave Frequency Counter measures the frequency of signals in the range of 10 Hz to 26.5 GHz, with a basic sensitivity of -33 to -23 dBm. Signals in the frequency range of 10 Hz to 520 MHz are measured by the direct count method. Signals in the frequency range of 500 MHz to 26.5 GHz are down-converted to an IF by a heterodyne conversion technique for application to the counter circuits. The unique conversion technique employed results in high sensitivity and FM tolerance in addition to automatic amplitude discrimination. The counted IF is added to the local oscillator frequency to determine the unknown frequency for display.

1-13. OPTIONS

1-14. Options available with the 5343A are described in *Table 1-1* and paragraph 3-62. If an option is included in the initial order, it will be installed at the factory and ready for operation upon receipt. If an option is ordered for field installation it will be supplied as a retrofit kit. Refer to Section II for kit part numbers and installation instructions.

1-15. SERVICE EQUIPMENT AVAILABLE

1-16. Extender boards are available for servicing printed circuit assemblies while extended from the instrument. The extender boards allow assemblies to be extended from their plug-in connectors for monitoring with appropriate test equipment. Extender boards for each assembly are supplied in Service Accessory Kit 10842A.

1-17. RECOMMENDED TEST EQUIPMENT

1-18. The test equipment listed in *Table 1-4* is recommended for use during performance tests, adjustments, and troubleshooting. Substitute test equipment may be used if it meets the required characteristics listed in the table.

Table 1-4. Recommended Test Equipment

INSTRUMENT	REQUIRED CHARACTERISTICS	USE*	RECOMMENDED MODEL
Oscilloscope	100 MHz bandwidth	T,A,OV,P	HP 1740A
Signal Generator	10 Hz—10 MHz 10 MHz—2.4 GHz 2 GHz—18 GHz 12 GHz—26 GHz	T,A,OV,P	HP 652A HP 8620C/86222A HP 8620C/86290A HP 938A
Spectrum Analyzer	RF inputs from 1 MHz—500 MHz	T,A,P	HP 141T/8552A/8554B
DC Voltmeter	20V Range, 0.05V Resolution	T,A	HP 3465A
AC Voltmeter	10 MHz-350 MHz	T,A	HP 3406A
Logic State Analyzer	HP 1740A compatibility	T	HP 1607A (use with HP 1740A)
Signature Analyzer	5343A compatibility	T	HP 5004A
Power Splitter	DC—18 GHz	OV,P	HP 11667A
Logic Pulser	TTL compatibility	T	HP 546A
Current Tracer	1 mA—1 A range	T	HP 547A
Logic Probe	TTL compatibility	T	HP 545A
Step Attenuator Step Attenuator	DC—18 GHz 10 dB steps DC—18 GHz 1 dB steps	OV,P OV,P	HP 8495B HP 8494B
AP Clips (4)	Clip for 14 pin/16 pin IC's	T	HP P/N 1400-0734
Isolation Transformer	115/230 IN - Isolated 115/230 OUT	T	Allied Electronics P/N 705-0165
Variable Transformer	120V/240V	T	927-6010 (120V) 927-6120 (240V)
Extender Boards	2 × 10 pin 2 × 12 pin 2 × 15 pin 2 × 18 pin (2) 2 × 22 pin (2) 2 × 24 pin A14 Extender A15 Extender	T	HP P/N 05342-60030 HP P/N 05342-60031 HP P/N 05342-60032 HP P/N 05342-60033 HP P/N 05342-60034 HP P/N 05342-60035 HP P/N 05342-60036 HP P/N 05342-60039
Power Meter	10 MHz—18 GHz 18 GHz—26.5 GHz	A,OV,P P	HP 436A HP 432A
Power Sensor	10 MHz—18 GHz	A,OV,P	HP 8481A
Thermistor Mount	18 GHz—26.5 GHz	P	HP K486A
50Ω Termination	DC—18 GHz	P	HP 909A (Option 012)
Microwave Amplifier	1 GHz, >+20 dBm Output	P	HP 489A
Signal Generator	100 MHz, +20 dBm	P	HP 8601A
Swept Frequency Analyzer	100 MHz—18 GHz	P	HP 8755B
15 MHz—18 GHz Modulator	HP 8755B compatibility	P	HP 11665B
15 MHz-18 GHz Detectors (2 required)	0.1—18 GHz	P	HP 11664A
Oscilloscope Mainframe	HP 8755B compatibility	P	HP 182T
Directional Coupler	2—18 GHz	P	HP 11692D
Directional Coupler	100—500 MHz	P	HP 778D
Signal Generator Mainframe	(Two Microwave sources needed for automatic amplitude discrimination test)	P	HP 8620C Mainframe
Desktop Computer	Control HP-IB	P,OV (Opt. 011)	HP 9825A

*T = Troubleshooting OV = Operational Verification
A = Adjustments P = Full Performance Testing

SECTION II
INSTALLATION

2-1. INTRODUCTION

2-2. This section contains information for unpacking, inspection, storage, and installation.

2-3. UNPACKING AND INSPECTION

2-4. If the shipping carton is damaged, inspect the instrument for visible damage (scratches, dents, etc.). If the instrument is damaged, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately (offices are listed at the back of this manual). Keep the shipping carton and packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for repair or replacement of your instrument without waiting for the claim against the carrier to be settled.

2-5. INSTALLATION REQUIREMENTS

CAUTION

Before connecting the instrument to ac power lines, be sure that the voltage selector is properly positioned as described below.

2-6. LINE VOLTAGE REQUIREMENTS. The 5343A is equipped with a power module that contains a printed-circuit line voltage selector to select 100- 120-, 220-, or 240-volt ac operation. Before applying power, the pc selector must be set to the correct position and the correct fuse must be installed as described below.

2-7. Power line connections are selected by the position of the plug-in circuit card in the module. When the card is plugged into the module, the only visible markings on the card indicate the line voltage to be used. The correct value of line fuse, with a 250-volt rating, must be installed after the card is inserted. This instrument uses a 0.75A fuse (HP Part No. 2110-0360) for 100/120-volt operation; a 0.375A fuse (HP Part No. 2110-0421) for 220/240-volt operation.

2-8. To convert from one line voltage to another, the power cord must be disconnected from the power module before the sliding window covering the fuse and card compartment can be moved to expose the fuse and circuit card. See *Figure 2-1.*

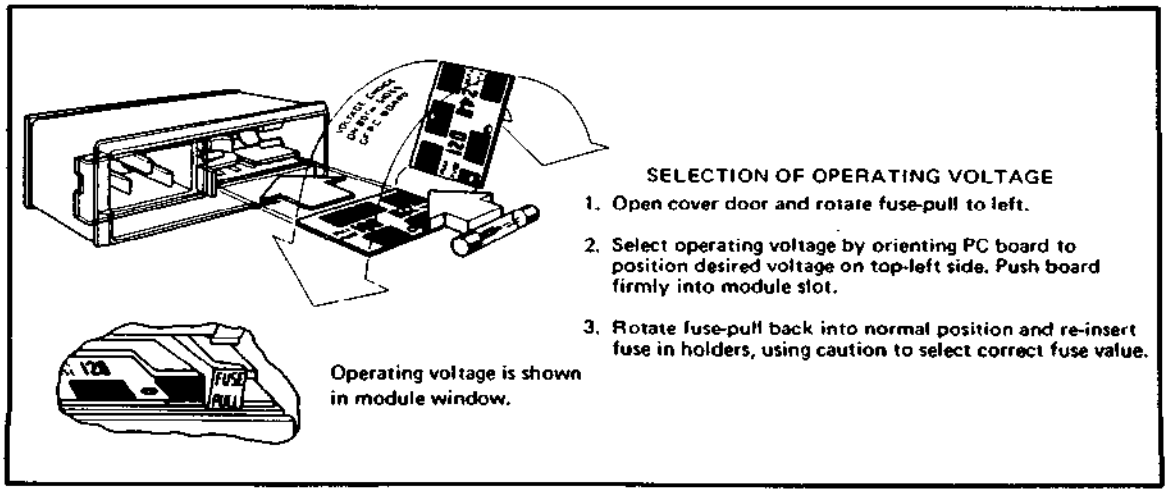


Figure 2-1. Line Voltage Selection

2-9. Power Cable

2-10. The 5343A is shipped with a three-wire power cable. When the cable is connected to an appropriate ac power source, this cable connects the chassis to earth ground. The type of power cable plug shipped with each instrument depends on the country of destination. Refer to *Figure 2-2* for the part numbers of the power cable and plug configurations available.

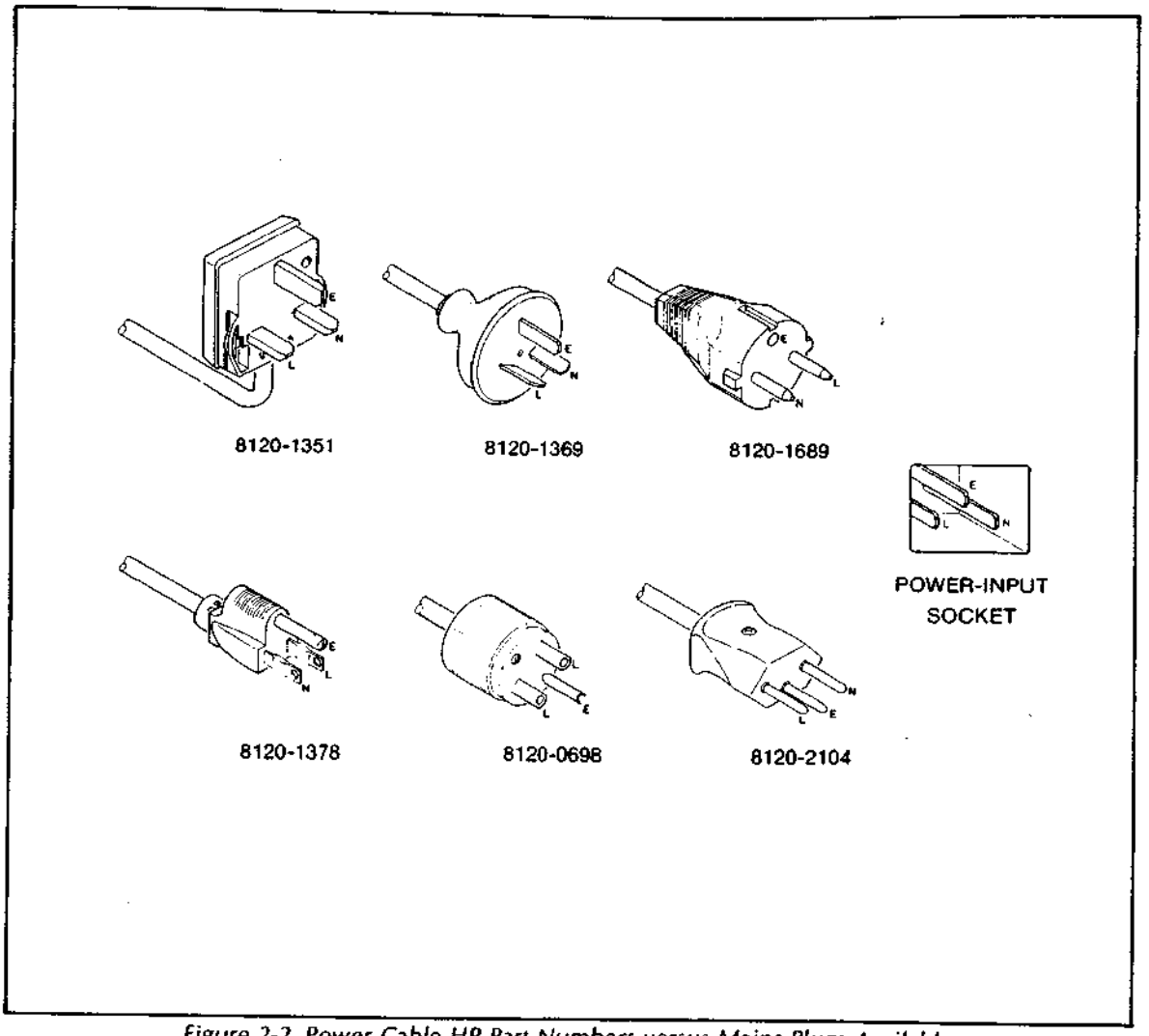


Figure 2-2. Power Cable HP Part Numbers versus Mains Plugs Available

WARNING

BEFORE SWITCHING ON THIS INSTRUMENT, THE PROTECTIVE EARTH TERMINALS OF THIS INSTRUMENT MUST BE CONNECTED TO THE PROTECTIVE CONDUCTOR OF THE (MAINS) POWER CORD. THE MAINS PLUG SHALL ONLY BE INSERTED IN A SOCKET OUTLET PROVIDED WITH A PROTECTIVE EARTH CONTACT. THE PROTECTIVE ACTION MUST NOT BE NEGATED BY THE USE OF AN EXTENSION CORD (POWER CABLE) WITHOUT A PROTECTIVE CONDUCTOR (GROUNDING).

2-11. Operating Environment

2-12. TEMPERATURE. The 5343A may be operated in temperatures from 0°C to +50°C.

2-13. HUMIDITY. The 5343A may be operated in environments with humidity up to 95%. However, it should be protected from temperature extremes which cause condensation in the instrument.

2-14. ALTITUDE. The 5343A may be operated at altitudes up to 4,600 metres (15,000 feet).

2-15. STORAGE AND SHIPMENT

2-16. Environment

2-17. The instrument may be stored or shipped in environments within the following limits:

TEMPERATURE	-40°C to +75°C
HUMIDITY	Up to 95%
ALTITUDE	7,620 metres (25,000 feet)

2-18. The instrument should also be protected from temperature extremes which cause condensation within the instrument.

2-19. Packaging

2-20. ORIGINAL PACKAGING. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also, mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-21. OTHER PACKAGING. The following general instructions should be used for repacking with commercially available materials:

a. Wrap instrument in heavy paper or plastic. (If shipping to Hewlett-Packard office or service center, attach tag indicating type of service required, return address, model number, and full serial number.)

b. Use strong shipping container. A double-wall carton made of 350-pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3- to 4-inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container. Protect control panel with cardboard.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

2-22. FIELD INSTALLATION OF OPTIONS

2-23. Procedures for field installation of Options 001, 004, and 011 are described in the following paragraphs.

2-24. Part Numbers for Ordering Option Kits

2-25. To obtain the necessary parts for installation of an option, order by part number as listed below.

Option	Name	Part Number
001	High Stability Time Base	HP Model 10544A
004	Digital-to-Analog Converter	05343-60106 (Kit)
011	HP-IB I/O	05342-60015 (HP-IB Assy.) 05342-60029 (HP-IB Input Assy.)

2-26. Installation of 10 MHz Oscillator Option 001

2-27. Option 001 consists of oven-controlled crystal oscillator time base 10544A, which has a pc card connector. Option 001 is installed in the same connector on the motherboard as the standard oscillator (A24). See *Figure 8-21*. To install Option 001, proceed as follows:

a. Remove the standard oscillator from A24 connector after removing the attaching screw at the top of the board.

b. Install Option 001 oscillator into A24 connector. 2360-0113

c. Attach Option 001 oscillator to the motherboard by means of two 6/32 × 5/16 pan head screws. Install the screws from the bottom of the motherboard, using star washers.

2-28. Installation of Digital-to-Analog Conversion (DAC) Option 004

2-29. Option 004 consists of an A2 Display Driver Assembly (05343-60008) that contains DAC circuitry added to the standard A2 circuit. Interconnecting wires are included with the Option 004 retrofit kit (05343-60106). Procedures for installation of Option 004 are as follows:

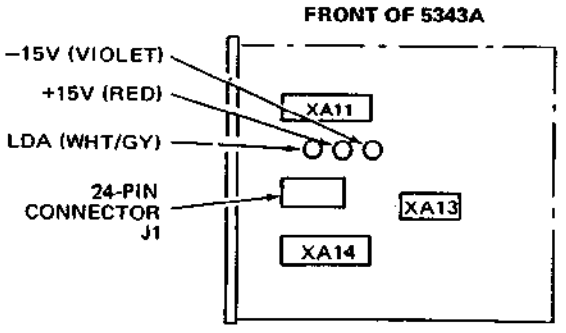
a. Remove top and bottom covers, front frame and A1–A2 assemblies. Refer to paragraph 8-28.

b. Replace the original A2 board (05343-60002) with Option 004 A2 board (05343-60008) and reassemble unit.

c. At bottom of 5343A, connect coax cable to the connector at the bottom rear of A2 board labeled D/A OUTP. Solder the other end of this cable to the DAC OUT connector on the rear panel. See *Figure 8-21*.

d. Connect the white/gray wire to the pin (push-on) labeled LDA at bottom rear of A2 Display Driver board. Solder other end of wire to LDA terminal on A22 Motherboard as shown in figure below.

e. Connect red wire (+15V) and violet wire (–15V) to the proper terminals (push-on pins) on A2 Display Driver board. Connect other end of these wires to terminals on A22 Motherboard as shown in figure below.



A22 Motherboard, Partial Bottom View

f. Reassemble instrument and perform operational verification procedures in paragraph 4-16.

2-30. Installation of HP-IB Option 011

2-31. Option 011 consists of printed-circuit assembly A15 and interconnection board A29. The interconnection board mounts inside the 5343A rear panel and is connected to A22 Motherboard via a cable strap. Procedures for installation of Option 011 are as follows.

a. Remove top and bottom covers and top panel from the 5343A.

b. Insert A15 assembly into A15 slot. See *Figure 8-21* for location.

c. If 5343A is equipped with Option 001 Oscillator, remove oscillator assembly by removing two attaching screws from A22 Motherboard.

NOTE

In the following step, make sure that the address switch is located as shown in *Figure 8-20*.

d. Insert the A29 Interconnection board (05342-60029) into the rear panel slots provided (from inside). Screw the two mounting studs (0380-0644) and washers (2190-3171) into the HP-IB connector to attach the board to the rear panel.

e. Connect the plug of the cable strap from A29 to J2 on A22 Motherboard with arrow on installed plug pointing toward front panel.

f. Refer to the following paragraphs for HP-IB interconnection data and to paragraph 3-70 for programming information.

g. Perform the operational verification procedures in paragraph 4-17.

2-32. HP-IB Interconnections

2-33. HEWLETT-PACKARD INTERFACE BUS. Interconnection data concerning the rear panel HP-IB connector is provided in *Figure 2-3*. This connector is compatible with the HP 10631A/B/C/D HP-IB cables. The HP-IB system allows interconnection of up to 15 (including the controller) HP-IB compatible instruments. The HP-IB cables have identical "piggy back" connectors on both ends so that several cables can be connected to a single source without special adapters or switch boxes. System components and devices may be connected in virtually any configuration desired. There must, of course, be a path from the calculator (or other controller) to every device operating on the bus. As a practical matter, avoid stacking more than three or four cables on any one connector. If the stack gets too large, the force on the stack produces great leverage which can damage the connector mounting. Be sure each connector is firmly (finger tight) screwed in place to keep it from working loose during use.

2-34. CABLE LENGTH RESTRICTIONS. To achieve design performance with the HP-IB, proper voltage levels and timing relationship must be maintained. If the system cable is too long, the lines cannot be driven properly and the system will fail to perform properly. Therefore, when interconnecting an HP-IB system, it is important to observe the following rules:

a. The total cable length for the system must be less than or equal to 20 metres (65 feet).

b. The total cable length for the system must be equal to or less than 2 metres (6.6 feet) times the total number of devices connected to the bus.

c. The total number of instruments connected to the bus must not exceed 15.

NOTE

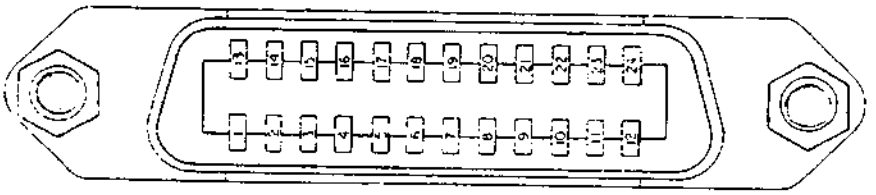
For information on HP-IB Extenders and Common Carrier Interface, refer to your nearest Hewlett-Packard Sales and Service office, listed at the back of this manual.

2-35. 5343A Listen Address

2-36. The 5343A contains a rear panel HP-IB Instrument address selection switch. There are five switches designated (A_5, A_4, A_3, A_2, A_1) which are used to select the address. Instructions for setting and changing the listen address are provided in Section III of this manual along with programming codes.

2-37. HP-IB Descriptions

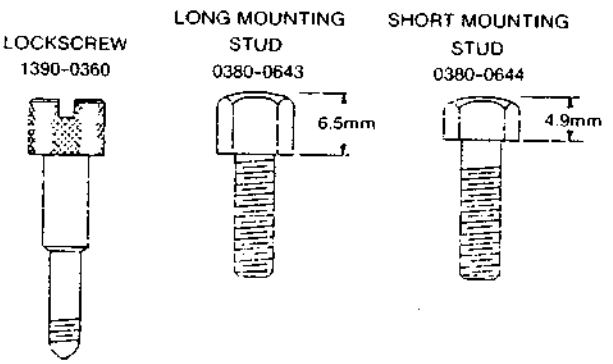
2-38. A description of the HP-IB is provided in Section III of this manual. A study of this information is necessary if the user is not familiar with the HP-IB concept. Additional information concerning the design criteria and operation of the bus is available in IEEE Standard 488-1975, titled *"IEEE Standard Digital Interface for Programmable Instrumentation"*.



PIN	LINE	
1	DIO1	
2	DIO2	
3	DIO3	
4	DIO4	
13	DIO5	
14	DIO6	
15	DIO7	
16	DIO8	
5	EOI	
17	REN	
6	DAV	
7	NRFD	
8	NDAC	
9	IFC	
10	SRQ	
11	ATN	
12	SHIELD-CHASSIS GROUND	
18	P/O TWISTED PAIR WITH PIN 6	THESE PINS ARE INTERNALLY GROUNDED
19	P/O TWISTED PAIR WITH PIN 7	
20	P/O TWISTED PAIR WITH PIN 8	
21	P/O TWISTED PAIR WITH PIN 9	
22	P/O TWISTED PAIR WITH PIN 10	
23	P/O TWISTED PAIR WITH PIN 11	
24	ISOLATED DIGITAL GROUND	

CAUTION

The 5343A contains metric threaded HP-IB cable mounting studs as opposed to English threads. Metric threaded HP 10631A, B, C, or D HP-IB cable lockscrews must be used to secure the cable to the instrument. Identification of the two types of mounting studs and lockscrews is made by their color. English threaded fasteners are colored silver and metric threaded fasteners are colored black. DO NOT mate silver and black fasteners to each other or the threads of either or both will be destroyed. Metric threaded HP-IB cable hardware illustrations and part numbers follow.



Logic Levels

The Hewlett-Packard Interface Bus logic levels are TTL compatible, i.e., the true (1) state is 0.0V dc to 0.4V dc and the false (0) state is +2.5V dc to +5.0V dc.

Programming and Output Data Format

Refer to Section III, Operation

Mating Connector

HP 1251-0293; Amphenol 57-30240.

Mating Cables Available

HP 10631A, 0.9 metres (3 ft.)
HP 10631B, 1.8 metres (6 ft.)
HP 10631C, 3.7 metres (12 ft.)
(HP 10631D, 0.5 metres (1.5 ft.)

Cabling Restrictions for Standard System

1. A Hewlett-Packard Interface Bus System may contain no more than 1.8 metres (6 ft.) of connecting cable per instrument.
2. The maximum accumulative length of connecting cable for any Hewlett-Packard Interface Bus System is 20.0 metres (65.5 ft.).

Figure 2-3. Hewlett-Packard Interface Bus Connection

SECTION III
OPERATION

3-1. INTRODUCTION

3-2. This section contains operating information including operating characteristics, descriptions of controls and indicators, and operating procedures.

3-3. OPERATING CHARACTERISTICS

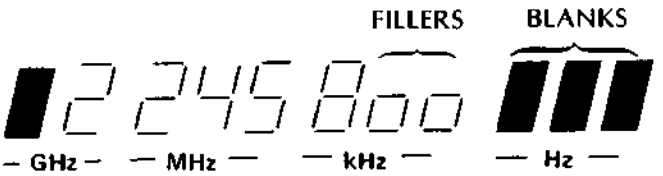
3-4. The following paragraphs describe the operating ranges and modes, resolution, sample rate, AM and FM characteristics, and auto-amplitude discrimination. Front panel controls and indicators are described in *Figure 3-1*, rear panel controls and connectors are described in *Figure 3-2*. Operating procedures are explained in *Figure 3-3*. DAC operation (Option 004) is described in *Figure 3-4*. HP-IB operation (Option 011) is described in paragraph 3-70.

3-5. Operating Ranges

3-6. There are two basic operating ranges: 10 Hz to 500 MHz and 500 MHz to 26.5 GHz. Frequencies in the lower range are measured directly while measurements in the 500 MHz to 26.5 GHz range are made indirectly by a harmonic heterodyne down-conversion technique. Provision is made to select either range by a front-panel slide switch. A separate input connector is provided for each range. When the range switch is in the 10 Hz—500 MHz position, the signal at the BNC connector is routed to the direct count circuits of the 5343A. In this range, input impedance is selectable via the 50Ω—1 MΩ switch. When the range switch is in the 500 MHz—26.5 GHz range, the input signal is applied via the front-panel APC-3.5 connector to the down-conversion circuits of the 5343A.

3-7. Resolution Keys

3-8. The best case resolution is the value represented by the least significant digit (LSD) in the display. In the 5343A, a maximum resolution of 1 Hz can be selected (by the pushbutton keys on the front panel labeled in blue, preceded by the blue key being pressed). The display is divided into four sections for ease of determining GHz, MHz, kHz, and Hz resolution. Half-sized ▯'s are used as space fillers within a section to improve interpretation of the display. For example, a signal measured to 100 kHz resolution will be displayed thus:



The two filler ▯'s in the kHz section indicate immediately that the 8 represents hundreds of kilohertz. The Hz section is blanked.

3-9. The pushbutton keys on the front panel under the RESOLUTION label are used for other purposes when the blue key is not in effect (has not been pressed). When the blue key has not been pressed, the keys are defined by the black number on the keys and are used to enter frequency offsets and manual center frequencies as described in *Figure 3-1*.

3-10. CHECK, DAC, and ENTER keys

3-11. The CHECK, DAC, and ENTER keys are used as described in *Figure 3-1.*

3-12. FREQ Keys

3-13. Two of the pushbutton keys on the front panel under the FREQ label are used to select the automatic or manual mode of operation. The other keys in this section of the keyboard control the use of the RESOLUTON keys. Use of these keys is described in detail in *Figure 3-1.*

3-14. Automatic Mode

3-15. The automatic mode of operation is selected by pressing the AUTO key. Input signals in the 500 MHz—26.5 GHz range are acquired, measured, and displayed automatically. When power is initially turned on, the 5343A goes into this mode automatically.

3-16. Manual Mode

3-17. The manual mode of operation is selected by pressing the MAN (MHz) key. To operate in this mode, input signals in the 500 MHz—26.5 GHz range must be known to within 40 MHz (25 MHz for frequencies below 825 MHz) and this frequency (called the manual center frequency) must be entered into the display prior to the measurement. Use of the manual mode is described in detail in *Figure 3-3.*

3-18. Offset Frequencies

3-19. It is sometimes desirable to add or subtract a constant to/from a frequency measurement. For example, by measuring a radio IF and knowing the LO, the counter can display the RF input when the LO frequency is entered as a positive offset. It may be easier to tune an oscillator to a specific frequency if the desired frequency is entered as a negative offset and the oscillator tuned until the counter reads zero. Frequency offsets are described in *Figure 3-3.*

3-20. Sweep Mode

3-21. The sweep mode of operation is selected by pressing the SWP M key. This mode allows measurement of an external, compatible sweeper signal applied to the front panel input of the 5343A. A control interface for the sweeper is provided by the SWP INTFC A B connectors on the rear panel of the 5343A. Connector A receives a negative true TTL pulse (minimum pulse width of 50 μs) from the sweeper (or other source) to initiate a measurement by the 5343A. Connector B outputs a negative true TTL pulse to lock the source signal frequency during the measurement. The measurement is displayed on the 5343A. Sweep Mode procedures are contained in *Figure 3-3.*

3-22. Frequency Multiplication

3-23. The frequency multiplier mode provides a means of multiplying the display frequency by a factor selected on the keyboard. The numbered RESOLUTION keys are used to select an integer from 2 through 99. When the integer factor is entered, the display is multiplied by this factor. Procedures for use of this mode are contained in *Figure 3-3.* The entered factor can also be used with automatic offset entries.

3-24. Totalize

3-25. The totalize mode operates in the 10 Hz to 520 MHz range and allows input pulses to be accumulated and displayed. The displayed count can be stopped and observed at any instant by pressing and holding any one of the RESOLUTION keys, except the 0 key which resets. During this time (while the count is displayed and the key held in) the internal circuits keep on counting and the accumulated count will be displayed upon release of the key. The display will count up to a maximum of 1,600,000,000 before it resets and starts over from 0. The display may be reset by pressing the 0 key (RESOLUTION).Totalize mode procedures are listed in *Figure 3-3.*

3-26. Digital-to-Analog Converter (DAC) Operation

3-27. When DAC Option 004 is installed, any three consecutive digits of the display can be selected and converted to a corresponding analog voltage output. The voltage is available at the BNC connector on the rear panel (labeled DAC OUT) and is between 0 and 9.99 volts dc. For example, if the selected digits are 000 the output is 0 volts and if the selected digits are 999 the output is 9.99 volts dc. Operating procedures are listed in *Figure 3-4.*

3-28. SET, RESET, RECALL, and CHS Keys

3-29. The SET, RESET, RECALL, and CHS keys allow offsets and center frequencies to be entered, reset the measurement process, recall previous values, and change the sign of offsets as described in *Figure 3-3.*

3-30. SAMPLE RATE Control

3-31. The SAMPLE RATE control adjusts the deadtime between the end of one measurement and the start of the next measurement. The duration of the measurement is determined by the resolution selected. The SAMPLE RATE is variable between <20 ms and HOLD. In HOLD position the display will hold the measurement displayed indefinitely.

3-32. GATE, REMOTE, TALK, and LISTEN Indicators

3-33. The GATE indicator is lit during the measurement interval (gate time) when the counter's gate is open and accumulating counts.

3-34. The REMOTE indicator is lit when the 5343A is in remote operation. (Option 011 described in paragraph 3-71.)

3-35. The TALK indicator is lit when the 5343A is in the TALK mode and the LISTEN indicator is lit when the 5343A is in the LISTEN mode (Option 011 must be installed).

3-36. AM Tolerance

3-37. The 5343A will measure carrier frequencies containing amplitude modulation to any modulation index provided the minimum voltage of the signal is not less than the sensitivity specification of the 5343A.

3-38. FM Tolerance

3-39. The 5343A will measure carrier frequencies which are modulated in frequency, such as a microwave radio carrier. The FM tolerance is the worst case FM deviation which can be present without affecting the counters ability to acquire the signal. If the deviations about the carrier are symmetrical, then the counter averages out the deviations to measure the actual carrier frequency. The FM tolerance is determined by the position of the ACQ TIME (acquisition time) switch on the rear panel. The MED (medium) position provides FM tolerance of 20 MHz peak-to-peak. The SLOW position provides a tolerance of 50 MHz peak-to-peak but results in slower acquisition time (2.4 seconds compared to 530 milliseconds for MED (medium) position). The FAST position provides FM tolerance of 6 MHz peak-to-peak with acquisition time of 200 ms.

NOTE

Most measurements should be made with the rear panel ACQ TIME switch in FAST or MED position. The SLOW position should be used only when the input signal has significant amounts of FM (>20MHz p-p). Incorrect measurements may result if the SLOW position is used with a stable input (non-FM) signal which has been locked to the counter's time base.

3-40. Automatic Amplitude Discrimination

3-41. The automatic amplitude discrimination feature allows the 5343A to acquire and display the highest level signal within its sensitivity range. The highest level signal must be 20 dB (typical) greater in amplitude than any other signal present. This feature is useful for discriminating against spurious signals and harmonics.

3-42. MAXIMUM INPUT SIGNAL POWER

CAUTION

Do not exceed +25 dBm (peak) of input power at the APC-3.5 connector (500 MHz—26.5 GHz). Damage to the internal sampler may occur. Refer to paragraph 3-43 for detailed explanation.

3-43. The 5343A will function within specifications for 500 MHz—26.5 GHz signal inputs up to +7 dBm. Under no circumstances should the input level to the 5343A exceed +25 dBm. If the input power exceeds this level, damage to the internal sampler may occur and the sampler is expensive to replace. Measurements from +7 to +25 dBm are not recommended as false readings may occur. When signal levels exceed +7 dBm external attenuators should be used to attenuate the signal.

NOTE

The BNC connector contains a fuse which may be removed for replacement as described in paragraph 3-44.

3-44. The 10 Hz—520 MHz direct count input BNC connector contains a fuse to provide for a maximum input level of 3.5V rms (+24 dBm). The fuse may be replaced by turning the connector with a BNC Tee and removing the fuse. (See *Figure 6-1.*)

3-45. INPUT CABLE CONSIDERATIONS

3-46. Consideration should be given to input cable losses at higher frequencies. For example, a 6-foot section of RG-214/U coaxial cable has about 15 dB loss at 18 GHz. At 25 GHz the losses in the RG-214/U would be prohibitive but the loss in a 6-foot section of semi-rigid RG-141A/U would be about 4.8 dB. Such losses must be taken into consideration along with the sensitivity specifications given in *Table 1-1*.

3-47. CONTROLS, INDICATORS, AND CONNECTORS

3-48. *Figure 3-1* describes the front panel controls, indicators, and connectors. *Figure 3-2* describes the rear panel connectors and controls.

WARNING

BEFORE THE INSTRUMENT IS SWITCHED ON, ALL PROTECTIVE EARTH TERMINALS, EXTENSION CORDS, AUTOTRANSFORMERS AND DEVICES CONNECTED TO IT SHOULD BE CONNECTED TO A PROTECTIVE EARTH GROUNDED SOCKET. ANY INTERRUPTION OF THE PROTECTIVE EARTH GROUNDING WILL CAUSE A POTENTIAL SHOCK HAZARD THAT COULD RESULT IN PERSONAL INJURY.

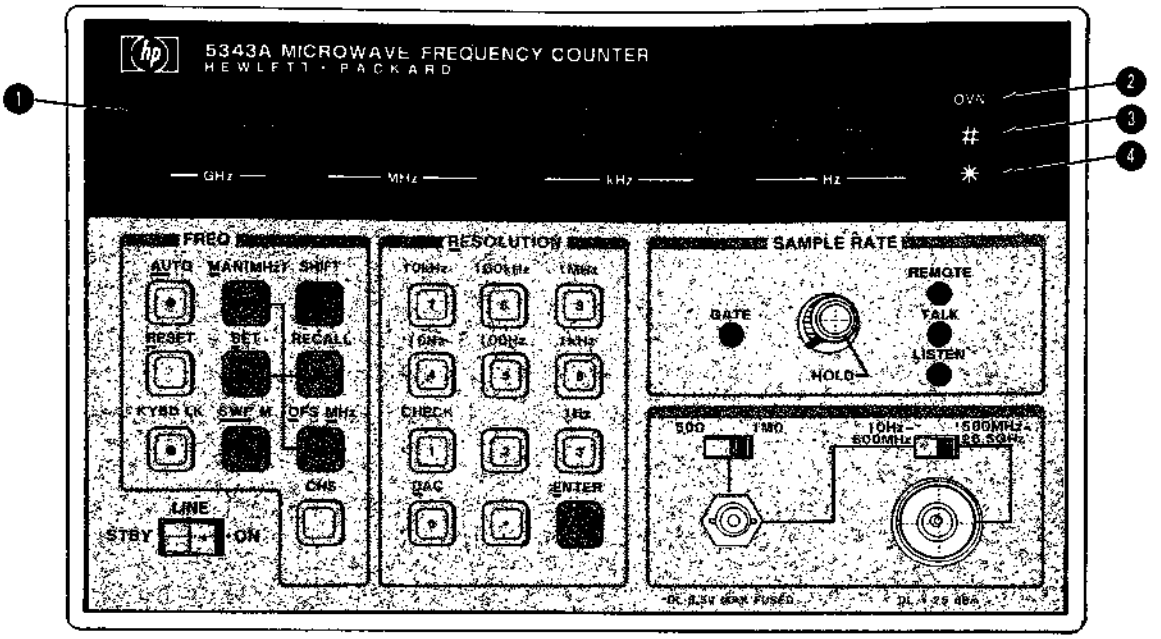
ONLY FUSES WITH THE REQUIRED RATED CURRENT AND SPECIFIED TYPE SHOULD BE USED. DO NOT USE REPAIRED FUSES OR SHORT CIRCUITED FUSEHOLDERS. TO DO SO COULD CAUSE A SHOCK OR FIRE HAZARD.

CAUTION

Before the instrument is switched on, it must be set to the voltage of the power source, or damage to the instrument may result. (Refer to paragraph 2-6.)

3-49. OPERATING PROCEDURES

3-50. *Figure 3-3* illustrates operating procedures for the standard 5343A. Self-check procedures are also given in *Figure 3-3*. An operators keyboard check is given in paragraph 3-51. Operating procedures for DAC Option 004 are listed in *Figure 3-4*.



DISPLAY

Digits:

The display contains 11 digit positions, two digits for frequencies in GHz and three digits each for MHz, kHz, and Hz.

Annunciators:

1 —Sign indicator	When lighted, indicates a negative frequency offset has been entered into display (MHz).
2 OVN indicator	Oven monitor indicates when crystal oscillator oven is on (warming). When warmed-up, light goes out (Option 001 only).
3 # indicator	When lighted, indicates the rear panel ACQ TIME switch is in MED (medium) position. This position provides FM tolerance of 20 MHz p-p.
4 * indicator	When lighted, indicates the rear panel ACQ TIME switch is in SLOW position. This position provides FM tolerance of 50 MHz p-p.

NOTE

When neither of the above indicators (# or *) are lit, the rear panel ACQ TIME switch is in FAST position. This position provides FM tolerance of 6 MHz p-p, with a fast acquisition time. Refer to paragraph 3-38.

FREQ Keys

The FREQ keys select the mode of operation and control the display.

NOTE

Some keys are equipped with center indicators that serve as "prompters" to the user. A blinking indicator states a "ready" condition for the key function that was selected and the instrument is waiting for a mode or number to be entered. A steady "on" indicator states that the key function that was selected is in operation.

AUTO key	Selects the automatic mode of operation to acquire and display input signal frequencies in the 500 MHz—26.5 GHz range. The instrument goes into this mode when power is turned on.
MAN (MHz) key	Selects manual mode for input signal frequencies in the 500 MHz—26.5 GHz range. Input signal frequency must be known (within 40 MHz) and entered into display via the black-numbered keys.
SHIFT key	Pressing this key activates the blue-labeled functions of the RESOLUTION keys.
RESET key	Clears the display and restarts a measurement. Clears any blinking lights in key center indicators.

Figure 3-1. Front Panel Controls and Indicators

SET key	Must be pressed prior to selecting OFS MHz or MAN (MHz). The SET condition is indicated by lighted segments ☰☰ in the GHz digits of the display. This indicates that a center frequency or offset frequency may be entered into the display.
RECALL key	Recalls stored memory information into display. The MAN (MHz), or OFS MHz keys, if **held in** after RECALL is pressed, will result in a display of previously entered or computed information.

NOTE

Information stored in memory (by digit keys) after MAN (MHz) key is pressed is available for display until AUTO mode is selected. Then the center frequency determined by the automatic measurement overrides the manual information.

KYBD LK key	Pressing this key disables all keyboard functions except the RESET key.
SWP M	Pressing this key initiates the SWEEP mode to control and measure the output of a compatible sweep generator. The key indicator flashes to indicate SWEEP mode and the MPU searches for a trigger from the sweep generator.

NOTE

An offset value is an arbitrary value selected for entry into the display to be added or subtracted from a measured value.

OFS MHz key	After pressing the SET key, the OFS MHz key is pressed prior to entering an offset value via the digit keys. (Digit keys are labeled in black numbers under RESOLUTION.) Indicates selection of frequency offset mode when lighted and adds frequency offset to measured frequency.

RESOLUTION keys:

The resolution keys select the display resolution (according to the blue labeling above each key) after the blue key is pressed. The keys are defined by the black number on the key when entering offsets and manual center frequencies.

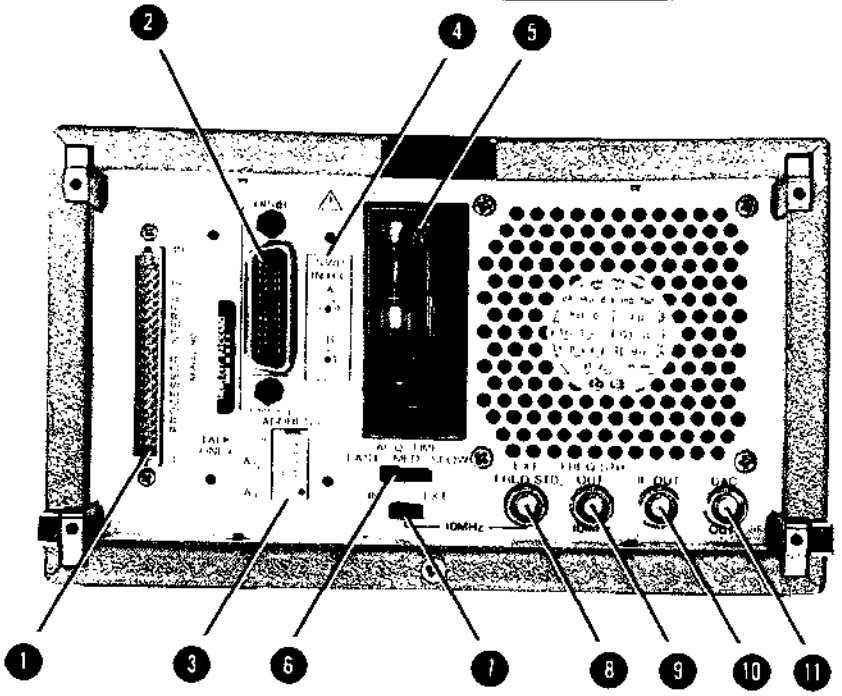
CHECK key	After pressing the blue key, the CHECK key is pressed to perform a self-check of the instrument. The display will indicate 75 MHz for proper operation. Press RESET to exit self-check.

NOTE

The instrument **must not have an input signal connected** at the 500 MHz—26.5 GHz input to perform the self-check.

ENTER key	Used to enter digits for manual center frequencies or offsets into memory via black-numbered keys. After the digits have been selected, ENTER key is pressed to signal the end of the digit sequence.
LINE switch	In ON position, applies power to all circuits except the crystal oven (Option 001 installed). The crystal oven connects through a separate transformer, a thermal circuit breaker and fuse directly to the ac line. This allows the oven to maintain its operating temperature and accuracy when the LINE switch is in STBY position, thereby eliminating warmup delays.
SAMPLE RATE control	Adjusts the interval between measurements from 20 ms to HOLD. When rotated to HOLD will hold display indefinitely.
GATE indicator	Indicates when counters main gate is open and measurement is in progress.
REMOTE indicator	Illuminates when counter is in REMOTE operation.
TALK indicator	Illuminates when counter is in TALK mode.
LISTEN indicator	Illuminates when counter is in LISTEN mode.
50Ω—1 MΩ switch	Selects input impedance for adjacent 10 Hz—500 MHz input connector.
10 Hz—500 MHz, 500 MHz—26.5 GHz switch	Selects either LOW or HIGH frequency range input connector.
BNC Input connector	Accepts 10 Hz—520 MHz input for direct count measurements. Measurements made at this input require that the range switch is set to the 10 Hz—500 MHz position. Sensitivity is listed in *Table 1-1*. The internal fuse may be replaced as described in paragraph 3-44.
APC-3.5 Input connector	Input for measurements in the 500 MHz—26.5 GHz range. Measurements made at this input require that the range switch is set the 500 MHz—26.5 GHz position. Sensitivity is listed in *Table 1-1*.

Figure 3-1. Front Panel Controls and Indicators (Continued)



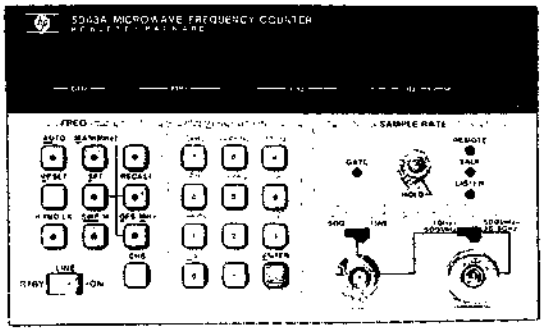
1. PROCESSOR INTERFACE connector A22W4J1. Not used. This connector is part of cable W4 which is connected to A22 Motherboard as an interface to the A14 Microprocessor address and data lines. This interface is provided for future use with companion instruments.
2. Position of digital input/output connector when instrument is equipped with Hewlett-Packard Interface Bus (HP-IB) Option 011. Refer to paragraph 3-70 for details.
3. Position of ADDRESS switch when instrument is equipped with Hewlett-Packard Interface Bus (HP-IB) Option 011. Refer to paragraph 3-74 for details.
4. SWP INTFC A B. Interface connectors for a compatible, external sweeper. During the SWEEP mode (SWP M key pressed and indicator flashing) connector A is used to receive a trigger from the sweeper to start a measurement. Connector B is used to send a lock signal to lock the sweeper frequency during the measurement.
5. AC Power Module. Input power module consisting of an IEC approved connector, a fuse (0.75 amp for 100/200-volt operation, 0.375 for 220/240-volt operation) and a pc card line voltage selector. Refer to paragraph 2-6 for details.
6. ACQ TIME (acquisition time) selector switch. Selects a fast, medium, or slow pseudorandom sequence (prs). The MED position provides a medium prs (or narrow mode) with FM tolerance of 20 MHz p-p. The SLOW position provides a long prs (or wide mode) with FM tolerance of 50 MHz p-p. The FAST position provides a short prs with FM tolerance of 6 MHz p-p. Refer to paragraph 3-38.

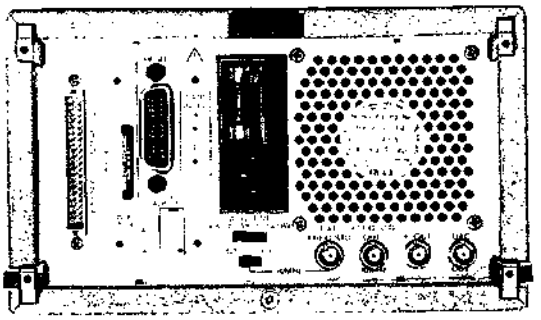
NOTE

Most measurements should be made with the rear panel FAST/MED/SLOW switch in the FAST or MED position. The SLOW position should be used only when the input signal has significant amounts of FM (>20 MHz p-p).

7. INT/EXT selector switch. Selects the internal 10 MHz crystal oscillator signal or an external 10 MHz source for the time base circuit. The external source must be connected to the adjacent connector (8).
8. EXT FREQ STD connector. Accepts 10 MHz external time base signal when INT/EXT switch is in EXT position.
9. FREQ STD OUT connector. Supplies a 10 MHz square wave output at 1.5 volts peak-to-peak.
10. IF OUT connector. Provides the intermediate frequency (IF) output of the Preamplifier circuit for test or monitor of the IF.
11. DAC connector. Provides the output voltage of the digital-to-analog converter when DAC Option 004 is installed.

Figure 3-2. Rear Panel Controls and Connectors





PRELIMINARY PROCEDURES

1. On rear panel:
   a. Set INT/EXT switch to INT position.
   b. Set ACQ TIME switch to MED. Refer to paragraph 3-38 for detailed description.
   c. On ac power module, check for proper fuse (0.75 amp for 100/120-volt operation, 0.375 amp for 220/240-volt operation) and check position of pc line voltage selector (refer to paragraph 2-6 for detailed description).
   d. For remote operation, refer to paragraph 3-70 for explanation of HP-IB programming and address switch settings on rear panel (for 5343A's equipped with Option 011).
2. On front panel, set LINE switch to ON position.

CAUTION

Do not exceed +25 dBm (peak) of input power at the APC-3.5 connector (500 MHz—26.5 GHz). Damage to the internal sampler may occur.

CAUTION

The 10 Hz—520 MHz direct count input BNC connector is fuse-protected for a maximum input level of 3.5V rms (+24 dBm).

3. Connect input signal to appropriate input connector according to frequency requirements (BNC for 10 Hz—520 MHz, APC-3.5 for 500 MHz—26.5 GHz) and set frequency range switch accordingly.
4. For input signals connected to BNC connector (10 Hz—520 MHz): set the 50Ω—1 MΩ switch as required. This switch has no effect on input signals connected to the APC-3.5 connector (500 MHz—26.5 GHz).
5. Press blue key, then press blue-labeled RESOLUTION key for desired resolution.

NOTE

Half-sized □'s are used as fillers in the display to facilitate display interpretation.

Figure 3-3. Operating Procedures

6. Adjust SAMPLE RATE control for desired interval between measurements.

KEY INDICATORS

Indicator LED's in the center of some keys are used as "prompters" by the operator, as follows:

Blinking Indicator

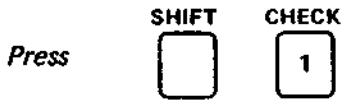
A blinking LED in a key is a "ready" condition for that key function. It indicates it is waiting for an entry via the keyboard. To clear the condition, press RESET.

Steady Indicator

A steady "on" LED in a key is an indication that the key function is in effect. To clear the condition, press the key. (The AUTO key is cleared by pressing MAN (MHz) and vice versa.)

SELF-CHECK PROCEDURE

Perform the self-check as follows (no input signal connected and SAMPLE RATE full ccw):

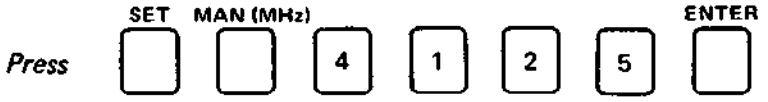


Counter Display:

(To exit from CHECK mode, press RESET)

TO SET MANUAL CENTER FREQUENCY

Example — To measure a 4.125 (±0.050) GHz signal in manual mode, connect signal to APC-3.5 connector and:



NOTE

The manual center frequency is entered (and displayed) with 1 MHz resolution and must be within 40 MHz of the input signal frequency (connected to 500 MHz—26.5 GHz connector).

TO ENTER OFFSET FREQUENCY

Example — To add 12.5 MHz to the measured frequency:

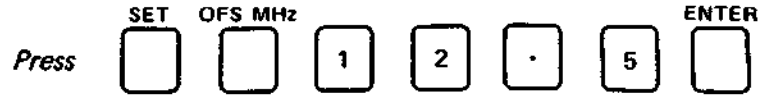


Figure 3-3. Operating Procedures (Continued)

Example — To subtract 12.5 MHz from the measured frequency:

Press [SET] [OFS MHz] [1] [2] [·] [5] [CHS] [ENTER]

TO RECALL OFFSETS OR CENTER FREQUENCY

Example — To recall a center frequency:

Press [RECALL] *Press and hold* [MAN (MHz)]

(Displays center frequency to 1 MHz resolution)

Example — To recall an offset frequency:

Press [RECALL] *Press and hold* [OFS MHz]

(Displays offset)

TO REMOVE OFFSETS

Example — To remove offset from display:

Press [OFS MHz]

LED in key goes out, function is off and display shows actual measured frequency. (Offset is still stored in memory and can be added to the measurement by pressing OFS MHz again.)

AUTOMATIC OFFSETS

Example — To "HOLD" a measurement and use it as a negative offset in subsequent measurements:

Rotate SAMPLE RATE cw to HOLD

Press [SET] [OFS MHz] [SHIFT]

Rotate SAMPLE RATE ccw to normal

NOTE

The measured frequency will now be negatively offset by the frequency captured when in HOLD.

Figure 3-3. Operating Procedures (Continued)

RESET

Pressing RESET key clears the display and initiates a new measurement without clearing stored values of offset or center frequencies. Clears any blinking ready state) key indicators, but does not clear steady state indicators. 5343A maintains current operating modes.

TOTALIZE

Example — Connect a signal (10 Hz to 520 MHz range) to the BNC connector.

Press SET SET 9

- Counter displays accumulating pulses. A small letter ⊏ is displayed as most significant digit and GATE indicator is lit during this mode.
- To stop displayed count, **press and hold** any RESOLUTION key, except 0.

  Counter keeps on accumulating pulses internally. Release the held key to observe accumulated count.
- Press the 0 key to reset the count.
- Display counts up to a maximum of 1,600,000,000 and resets.
- Press RESET to exit TOTALIZE mode. Counter returns to FREQUENCY mode, 1 Hz resolution.
- To exit TOTALIZE mode during keyboard lock, press RESET twice. (Once to remove keyboard lock, once to exit TOTALIZE mode.)

NOTE

Previously entered offset frequencies are lost when TOTALIZE mode is engaged.

TOTALIZE DURING DAC FUNCTION

To operate the Option 004 DAC function during the TOTALIZE mode press RESET to exit totalize, then select DAC mode (see *Figure 3-4*), and return to TOTALIZE.

Figure 3-3. Operating Procedures (Continued)

FREQUENCY MULTIPLIER

Example — To multiply a displayed frequency by an integer (such as 5):

Press [SET] [.] (Decimal point) Display: F.

Press [5] Display: F . 5

Press [ENTER] Display: Frequency mutliplied by 5 (blue key indicator lights)

- Press [RESET] to remove multiply factor. Press [RECALL] and press and hold [MAN (MHz)] to display measurement (MHz) and retain multiply factor.
- Integer range is from 2 to 99
- Display overflows at all 9's
- Press [RECALL], *press and hold* [.] (decimal point) to view entered factor
- Entered factor stays active when automatic offset is entered
- The multiply mode functions in either frequency range
- If overrange occurs, press [RESET] to recover measurement.

SWEEP MODE

Example — To control measurement of an external, compatible sweeper:

Press [SWP M] (key indicator blinks slowly to indicate SWEEP mode is in effect.)

NOTE

The sweeper must be compatible with the control interface connections (SWP INTFC A B) on the rear panel of the 5343A.

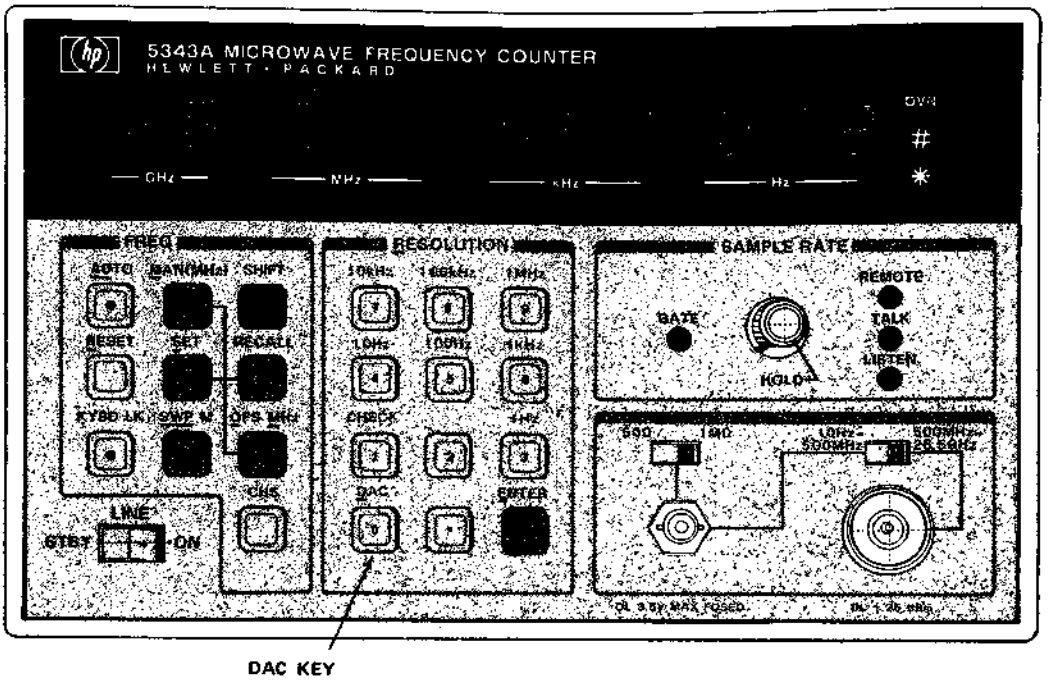
- The SWP INTFC A connector receives a negative-true TTL pulse of at least 50 μs width to trigger the 5343A measurement.
- The SWP INTFC B connector provides a negative-true pulse to the source to lock the frequency during the measurement.

Press [SWP M] key during SWEEP mode to disable.

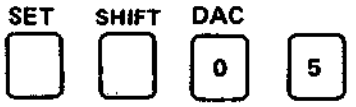
NOTE

The 5343A is locked in automatic during SWEEP mode. The **MAN (MHz)** key has no effect. Other key functions operate normally.

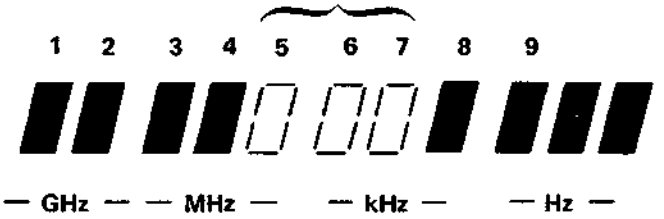
Figure 3-3. Operating Procedures (Continued)



The DAC key is effective only when DAC Option 004 is installed. Selects any three consecutive displayed digits to convert to voltage. The position of the most significant digit of selected digits is determined by the black numbered key. For example.



To select digits as follows:



A dc voltage of 0 to 10 volts, corresponding to the selected digits, will be present at the DAC OUT connector on the rear panel. Selected digits 000 produces 0V output, 999 produces 9.99V output.

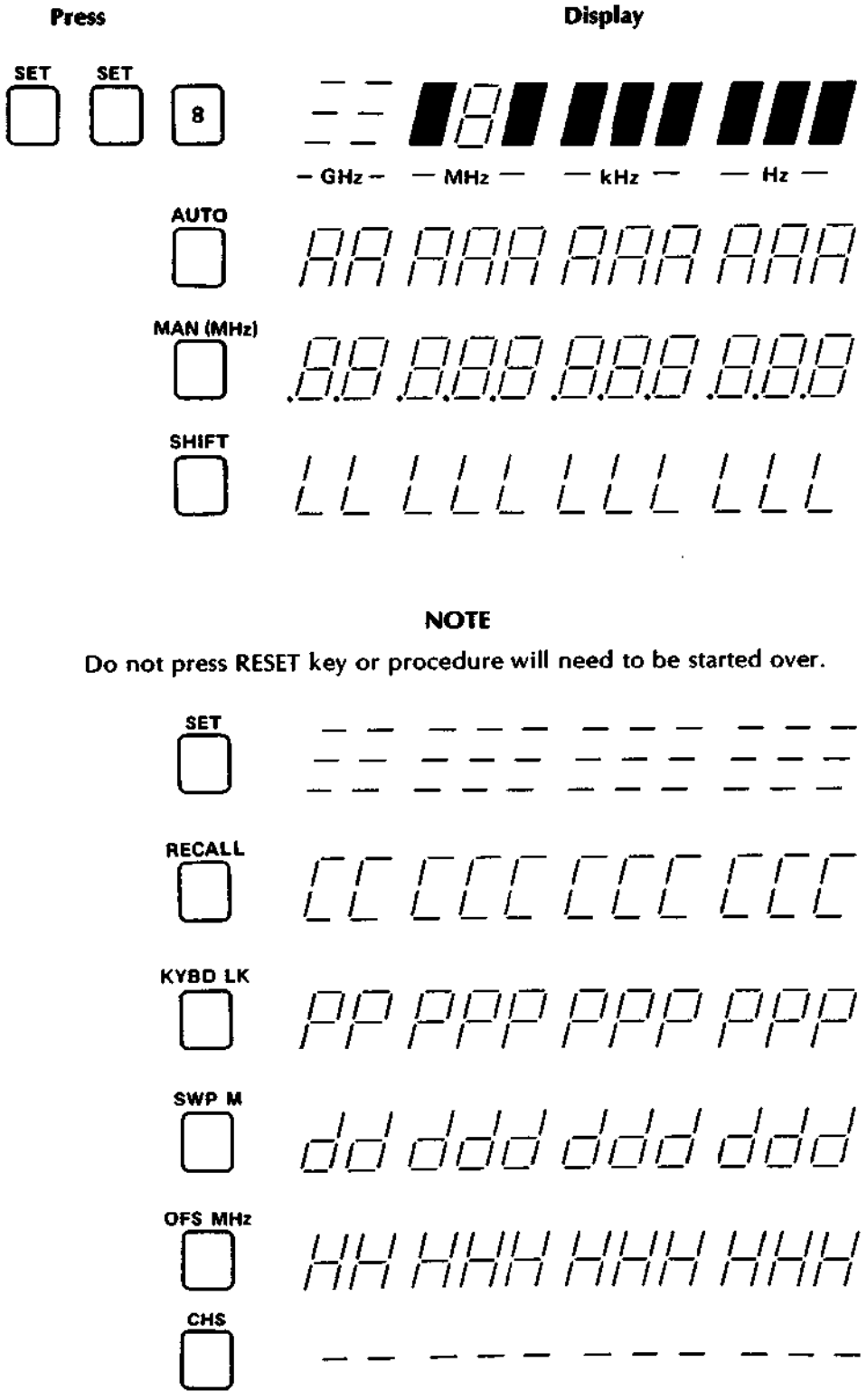
NOTE

Use the manual mode, minimum required resolution (1 MHz is lowest) and as fast a sample rate as possible to obtain the smoothest output.

Figure 3-4. DAC Operation (Option 004)

3-51. OPERATOR KEYBOARD CHECK

3-52. Check for proper operation of the keyboard and display by pressing the keys listed and observing display. To exit from keyboard check mode, press RESET.



NOTE

Do not press RESET key or procedure will need to be started over.

Operator Keyboard Check (continued)

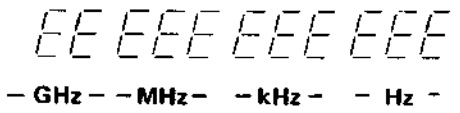
Press	Display
7	7 77 777 7777
8	8 88 888 8888
9	9 99 999 9999
4	4 44 444 4444
5	5 55 555 5555
6	6 66 666 6666
1	1 11 111 1111
2	2 22 222 2222
3	3 33 333 3333
0	0 00 000 0000
.	. . . .
ENTER	r r r r r r r r r r

3-53. ERROR CODE DISPLAYS

3-54. Error codes are displayed by the 5343A to indicate circuit malfunctions in the instrument and to indicate operator (procedure) errors.

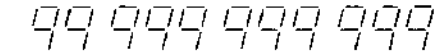
3-55. Instrument Error Displays

3-56. When power is applied to the 5343A, check-sum routines are automatically performed. If a routine fails, an error code is displayed to indicate the circuit fault area as follows:

Display	Fault Area
 – GHz – – MHz – – kHz – – Hz –	RAM A16U11 or A16U14
	ROM A16U6
	ROM A16U9

3-57. Signal Error Displays

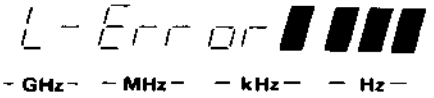
3-58. The display indicates when the applied signal is insufficient or excessive in level or limits, as follows:

Operating Mode	Range Switch	Insufficient Signal Level Display
*Frequency	10 Hz—500 MHz	 – GHz – – MHz – – kHz – – Hz –
*Frequency	500 MHz—26.5 GHz	 – GHz – – MHz – – kHz – – Hz –
		Overrange (due to offset)
Frequency	10 Hz—500 MHz and 500 MHz—26.5 GHz	

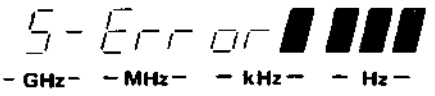
*Shown for 1 Hz resolution. Digit shifts one position to left for each step decrease in resolution.

3-59. Limit Errors and Sequence Errors

3-60. A limit error (for example, setting a manual center frequency less than 500 MHz) will be displayed as:


– GHz – – MHz – – kHz – – Hz –

3-61. A sequence error (for example, pressing a digit key before pressing a function key) will be displayed as:


– GHz – – MHz – – kHz – – Hz –

3-62. OPTIONS

3-63. The operating characteristics of the 5343A are affected by the addition of any of the options described in the following paragraphs.

3-64. Time Base Option 001

3-65. Option 001 provides an oven-controlled crystal oscillator time base (Model 10544A) that results in higher accuracy and longer periods between calibration (refer to *Table 1-1*). The oven temperature is maintained when the 5343A LINE switch is in either the ON or the STBY position (provided the instrument is connected to the power mains). When the OVN indicator in the display is lit, the oven is on (warming). When the oven is at the proper temperature, the OVN indicator goes out.

3-66. HP-IB Interface Option 011

3-67. The Hewlett-Packard Interface Bus (HP-IB) Option 011 allows the functions of the 5343A to be controlled remotely and allows measurement data to be ouptut to the bus. Programming information for Option 011 is given in paragraphs 3-70 through 3-90.

3-68. Digital-to-Analog Converter (DAC) Option 004

3-69. The DAC option allows selection of any three consecutive digits in the display and conversion of these digits to an analog voltage. The analog voltage is available at a rear panel connector. The digits are converted to a voltage of from 0 to 10 volts, corresponding to the digits selected. Digits 000 produce 0 volts, digits 999 produce 9.99 volts, fullscale into 15 kilohms. Refer to *Figure 3-4* for operating information.

3-70. HP-IB PROGRAMMING (OPTION 011)

3-71. The capability of a device connected to the HP-IB is specified by its interface functions. *Table 3-1* lists the interface functions of the 5343A using the terminology of IEEE Standard 488-1975 (Appendix C). Interface functions provide the means for a device to receive, process, and send messages over the HP-IB. Option 011 HP-IB installation procedures and interconnections are described in Section II.

Table 3-1. HP-IB Interface Capability

Interface Function Subset Identifier	Interface Function Description
SH1	Complete source handshake capability.
AH1	Complete acceptor handshake capability.
T1	Talker (basic talker, serial poll, talk only mode, does not unaddress to talk if addressed to listen).
L2	Listener (basic listener, no listen only mode, does not unaddress to listen if addressed to talk).
SR1	Service request capability.
RL1	Complete remote/local capability.
PP0	No parallel poll capability.
DC1	Device clear capability.
DT1	Device trigger capability.
C0	No controller capability.
E1	One unit load.

3-72. Basic Bus Messages

3-73. There are 12 basic messages which can be sent over the interface. *Table 3-2* lists each bus message, a description of the message, how the 5343A uses that message, and examples of 9825A implementation of the messages.

3-74. Bus Address Selection

3-75. The 5343A must be assigned a bus address. *Table 3-3* gives the allowable address switch settings.

3-76. Program Code Set

3-77. *Table 3-4* gives the program code set for the 5343A. Frequency mode selection, manual center frequency setting, frequency offset mode selection, frequency offset setting, resolution selection, range selection, acqusition time selection, and automatic offsets are all analogous to the corresponding front panel operations described previously.

3-78. There are four sample rate modes T0–T3, as shown in *Table 3-4*. In T0, the sample rate is determined by the setting of the front panel SAMPLE RATE control. In T1, the counter is in HOLD. To trigger a measurement, a trigger message must be sent. In T2, the counter ignores any sample rate run-down and initiates a new measurement as soon as the previous measurement is over. In T3, the counter takes a measurement and holds until the next T3 or trigger message.

3-79. Output Modes

3-80. In the "output only when addressed" mode, the counter pulls SRQ at the end of a measurement and then checks to see if it has been addressed to talk. If not, SRQ is cleared and it starts the next measurement. If it has been addressed to talk, it outputs the measurement, clears SRQ, and starts the next measurement. In the "wait until addressed" output mode, the counter pulls SRQ at the end of a measurement and waits in a loop until it has been addressed to talk. When it is addressed to talk, it outputs the measurement, clears SRQ and starts the next measurement.

NOTE

If the counter is placed in the HOLD (T1) mode, triggered, then addressed to talk, be sure to use the Wait Until Addressed (ST2) output mode. If not, then for short gate times the measurement may be completed before the controller addresses the counter to talk and the counter will discard the measurement result and hangup the bus.

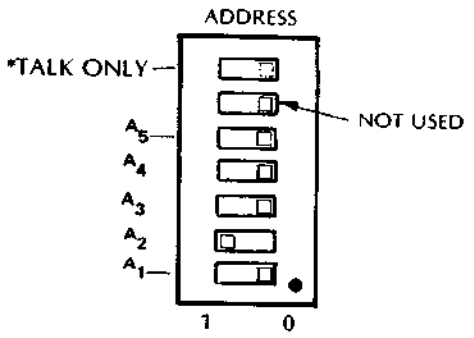
3-81. PROGRAM CODE STRINGS. The 5343A executes each complete program code as it is received just as if the microprocessor were receiving the data from the front panel keyboard. Program code strings should be in the same order as they would be if being entered from the front panel. When a data byte is sent to the 5343A HP-IB Option 011, the HP-IB interface stores the byte and sends an interrupt to the microprocessor which reads in the byte. If the byte does not complete a program code, then the microprocessor looks for the next byte(s) until a complete code is sent (for example, SR5 is a complete code but SR is not). After a complete code is received, the microprocessor executes the code and begins the measurement. If more codes are in the string, another interrupt is generated. For example, if the string "SR5AU" is sent by the controller, the "S" is the first byte received and stored by the 5343A HP-IB interface. The interface generates an interrupt to the microprocessor and the "S" is read by the MPU. Since S is not a complete code, the microprocessor looks until the complete code is sent and received. After "R" and then "5" are sent, the microprocessor sets the resolution accordingly and then goes to the beginning of the measurement. When the controller sends "A", an interrupt is generated and "A" is read by the microprocessor. It then looks for the complete code to be sent which in this case is "AU". The microprocessor again goes to the start of the measurement cycle.

Table 3-2. 5343A Bus Message Usage

Message	Description	5343A Use	Sample 9825 Statements (5343A set to Address 02)
Data	Transfers device-dependent information from one device to one or more devices on the bus.	Sends measurement data. See paragraph 3-77 for output format. Accepts program codes. See *Table 3-4* for code set.	red 702, A wrt 702, "AUSR4"
Trigger	Causes a group of selected devices to simultaneously initiate a set of device-dependent actions	Starts a new measurement.	trg 7 or trg 702
Clear	Causes an in .crument to be set to a predefined state (a certain range, function, etc.).	Same as front panel RESET. Clears internal count and starts new measurement.	clr 7 or clr 702
Remote	Permits selected devices to be set to remote operation, allowing parameters and device characteristics to be controlled by Bus Messages.	5343A goes to remote if REN is true and addressed to listen. In absence of program data, remote operation is according to the state of the front panel settings just prior to going to remote.	rem 702
Local	Causes selected devices to return to local (front panel) operation.	Goes to local front panel control. In absence of front panel data, local operation is according to the state of the remote data just prior to going to local.	lcl 702
Local Lockout	Disables local (front panel) controls of selected devices.	Disables front panel RESET. 5343A remains in remote.	llo 7
Clear Lockout and local	Returns all devices to local (front panel) control and simultaneously clears the Local Lockout Message.	Local lockout cleared and returns to local front panel control	lcl 7
Require Service	Indicates a device's need for interaction with the controller.	Pulls on SRQ to indicate end of a measurement.	rds(7)→A if bit (7, A) (bit 7=1 if SRQ true)
Status Byte	Presents status information of a particular device; one bit indicates whether or not the device currently requires service, the other 7 bits (optional) are used to indicate the type of service required.	In serial poll mode, 5343A outputs decimal 80 (01010000) to indicate end of measurement.	rds (702)→A (if A=80, then 5343A is ready to output)
Status Bit	A single bit of device-dependent status information which may be logically combined with status bit information from other devices by the controller.	Does not use	—
Pass Control	Passes bus controller responsibilities from the current controller to a device which can assume the Bus supervisory role.	Does not use	—
Abort	Unconditionally terminates Bus communications and returns control to the system controller.	Clears Talk, Listen, Serial Poll Enable registers on 5343A HP-IB interface. Front panel annunciators do not change, however.	cli 7

Table 3-3. Address Selection

Rear panel address switch:



(Shown in addressable mode, and address 02)

*If the 5343A is in TALK ONLY mode and it is desired to return to the addressable mode, set TALK ONLY switch to 0 and press RESET on front panel.

ASCII CODE CHARACTER		ADDRESS SWITCHES					5-BIT DECIMAL CODE
LISTEN	TALK	A_5	A_4	A_3	A_2	A_1	
SP	@	0	0	0	0	0	00
!	A	0	0	0	0	1	01
"	B	0	0	0	1	0	02
#	C	0	0	0	1	1	03
$	D	0	0	1	0	0	04
%	E	0	0	1	0	1	05
&	F	0	0	1	1	0	06
'	G	0	0	1	1	1	07
(	H	0	1	0	0	0	08
)	I	0	1	0	0	1	09
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
,	L	0	1	1	0	0	12
—	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
0	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	S	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	U	1	0	1	0	1	21
6	V	1	0	1	1	0	22
7	W	1	0	1	1	1	23
8	X	1	1	0	0	0	24
9	Y	1	1	0	0	1	25
:	Z	1	1	0	1	0	26
;	[	1	1	0	1	1	27
<	\	1	1	1	0	0	28
=	]	1	1	1	0	1	29
>	~	1	1	1	1	0	30

Table 3-4. Option 011 HP-IB Program Code Set

MODE

1. FREQUENCY MODE SELECT

AUTO	**AU**
MANUAL	**M**

2. TOTALIZE

Totalize Mode off	**CM0**
Totalize Mode on	**CM1**
Totalize Mode clear	**CMC**

3. SWEEP

Sweep Mode off	**SWP0**
Sweep Mode on	**SWP1**

FUNCTION

1. RESET ..... **R**

(Display is blanked and new measurement initiated. If in Hold (T1), then measurement is not completed but stays in Hold. Does not return control to local.)

2. SET MANUAL CENTER FREQUENCY ..... **SMXXXXXE**

(X's represent nonfixed length data string of up to 5 characters. Decimal points cause entire string to be ignored. + signs and spaces are allowable. Number is in MHz and must be less than 26.5 GHz or will be ignored.)

Example: SM10000E for 10 GHz center frequency
SM775E for 775 MHz center frequency
SM+5250E for 5.25 GHz center frequency

3. FREQUENCY OFFSET MODE SELECT

Frequency Offset off	**OM0**
Frequency Offset on	**OM1**

4. SET FREQUENCY OFFSET ..... **SOM±XXXXX.XXXXXXE**

(X's represent nonfixed length data string representing offset frequency in MHz. Spaces are ignored.)

Example: SOM10.7E for 10.7 MHz positive offset
SOM−4000.25E for 4.00025 GHz negative offset.

5. AUTOMATIC OFFSETS

Automatic Frequency offset	**SOMB**

6. RESOLUTION

1 Hz	**SR3**
10 Hz	**SR4**
100 Hz	**SR5**
1 kHz	**SR6**
10 kHz	**SR7**
100 kHz	**SR8**
1 MHz	**SR9**

7. RANGE

10 Hz—500 MHz	**L**
500 MHz—26.5 GHz	**H**

8. CHECK MODE **SR1**

(No input can be present at RF connector. Be sure to send RESET command (R) before making other measurements.)

Table 3-4. Option 011 HP-IB Program Code Set (Continued)

9. FM TOLERANCE (ACQUISITION TIME)

6 MHz p-p FM (Fast or Short Time)	**QS**
20 MHz p-p FM (Medium Time)	**QM**
50 MHz p-p FM (Slow or Long Time)	**QL**

10. SET MULTIPLICATION FACTOR ..... **S.XXE**

(XX Represents data string of up to two characters.)

Example: S.2E (for multiplication factor of 2.)
S.34E (For multiplication factor of 34.)

11. POWER-UP CONDITIONS

Return to power-up state ..... **P**

NOTE

Sample rate and output modes are not under P-code control. 5343A goes to Auto, 1 Hz resolution, and resets all special functions (Kybd lock, Sweep, Multiplication factor to 1).

12. SELECT DIGITAL-TO-ANALOG CONVERTER (OPTION 004)

Select DAC ..... **SBDX**

(X Represents front panel character position 1 to 9. Position 1 is the left most digit. The digit selected and the two to its right are those converted.)

SAMPLE RATE COMMANDS

1. SAMPLE RATE

Front panel sample rate	**TØ**
Hold	**T1***
Fast sample (no delay)	**T2**
Sample then hold	**T3**

*Send trigger command *(trg 7 or trg 702)* to start measurement. If 5343A is in remote and addressed to listen and other than Hold (T1), the trigger command causes the 5343A to automatically go to Sample then Hold (T3).

OUTPUT MODES

1. OUTPUT MODE

No output to bus	**STØ**
Output only when addressed	**ST1**
Wait until addressed	**ST2**

3-82. OUTPUT IN TOTALIZE. The trigger commands (trg 7 or trg 7Ø2) will not be effective when the 5343A is operating in TOTALIZE (CM) mode. To output in TOTALIZE mode, an output (ST) command must be entered prior to enabling TOTALIZE. When operating in TOTALIZE mode, it is necessary to return to AUTO mode, enable an output (ST) command, then return to TOTALIZE.

3-83. The only commands accepted in TOTALIZE are system commands such as CMØ, CM1, CMC, etc. The input must be applied to the 10 Hz—520 MHz BNC only.

3-84. SWEEP MODE. In SWEEP mode, the SAMPLE RATE control has no effect. The 5343A will accept all commands except Manual (M), set Manual Center Frequency (SMXXXXXE) and Sample Rate (TØ–T3). The SWP M key indicator blinks slowly during the SWEEP mode, while the 5343A awaits a trigger from the external source via rear panel connector SWP INTFC A.

3-85. AUTOMATIC OFFSETS. The automatic frequency offset code (SOMB) is generally used to take a measurement, zero the counter, and take another measurement. The 5343A must have time to take the first measurement, then apply the automatic offset command before the next measurement is made. The method for doing this is to use a "wait" statement between the measurement command string and the SOMB command string, as follows:

```
rem 702, wrt 702 "AUSR3"
wait 1000
wrt 702 "SOMB"
```

NOTE

If this wait time is not implemented, the "SOMB" command will cut off the measurement and the value desired for offset use will be lost.

3-86. Output Formats

3-87. The 5343A outputs measurement data in the following fixed length formats:

NOTE

The following output formats pertain to input signals of specified sensitivity (*Table 1-1*). For less sensitive input signals, refer to paragraph 3-91.

a. NO OFFSET, FREQUENCY ONLY

SP F SP SPXXXXX.XXXXXX E Ø6 CR LF

frequency — space — carriage return — line feed

b. FREQUENCY OFFSET

SP FS ±XXXXX.XXXXXX E + Ø6,

offset

c. OVERLOAD

SP F SP SP 99999.999999 E + Ø9 CR LF

(caused by excessive input level)

d. DISPLAY OVERFLOW

SP F SP SP 99999.999999 E + Ø6 CR LF

(caused by offset which makes display overflow)

e. INSUFFICIENT SIGNAL

SP F SP SP ØØØØØ.ØØØØØØ E + Ø6, CR LF

3-88. When the 5343A is in remote, the front panel REMOTE indicator lights. When the 5343A is addressed to talk, the front panel TALK indicator will light. When the 5343A is addressed to listen the LISTEN indicator will light.

3-89. 9825A PROGRAM EXAMPLES

3-90. The following 9825A program examples are illustrative of 5343A programming:

EXAMPLE 1

```
0: wrt 702,"AUSR
 7T1ST2"
1: trg 702;red
 702,A;dsp A
 wait 500
2: sto 1
3: end
*3802
```

This program assumes the range switch was set to 0.5—26.5 GHz before the program was executed. The program puts the 5343A in AUTO, 10 kHz resolution, HOLD, and "wait until addressed" output mode. Program takes a measurement (trg 702) and reads it into the A register. After waiting 500 ms, the program loops back to the next trigger, then read statement. Observe the action of the GATE, REMOTE, TALK, and LISTEN lamps.

EXAMPLE 2

```
0: wrt 702,"AUSR
 4T2ST1"
1: red 702,A
 cmd 7,"_";dsp
 A;wait 500
2: sto 1
3: end
*5923
```

This program also assumes the range switch was previously set to the 0.5—26.5 GHz position. The program puts the counter in AUTO mode, 10 Hz resolution, fast sample, and "only if addressed" output mode. The program takes a measurement, unaddresses the 5343A as a talker (cmd 7, "—") so that the counter will continue making measurements at a fast rate, and waits 500 ms until reading the next measurement.

EXAMPLE 3

```
0: wrt 702,"SM10
 00ESR30NT0ST1"
1: red 702,A
 prt A
2: sto 1
3: end
*1421
```

This program sets a manual center frequency of 1 GHz (input frequency ≅1.003 GHz), 1 Hz resolution, 0.5—26.5 GHz range, medium acquisition time mode, front panel sample rate control, and "output only if addressed". Each reading is printed on the 9825A printer. Input frequency is approximately 998 MHz.

Printout

```
998858006.00
998857912.00
998857820.00
998857713.00
998857611.00
998857499.00
998857392.00
998857271.00
```

EXAMPLE 4

This program selects AUTO mode, 1 Hz resolution, front panel SAMPLE RATE, high frquency input, medium acquisition time, frequency offset "on", sets frequency offset at 2000 MHz, and "output only when addressed." The measured value is offset by 2000 MHz, output to and printed by the calculator. Input frequency is approximately 998 MHz.

```
0: wrt 702,"AUSR
 3T0H0M0M1S0M200
 0EST1"
1: red 702,A
 prt A
2: sto 1
3: end
*20097
```

Printout

```
2998833179.00
2998832993.00
2998832811.00
2998832649.00
2998832509.00
2998832386.00
2998832253.00
2998832118.00
```

EXAMPLE 5

This program selects AUTO mode, 1 MHz resolution, front panel SAMPLE RATE, high frequency input, medium acquisition time, sets a multiplication factor of 3, and output "only when addressed." The measured value, as multiplied by a factor of 3, is output to and printed by the calculator. Input frequency is approximately 998 MHz.

```
0: wrt 702,"AUSR
 3T0H0MS.3EST1"
1: red 702,A
 prt A
2: sto 1
3: end
*30806
```

Printout

```
2994231504.00
2994230988.00
2994230436.00
2994230079.00
2994229698.00
2994229329.00
```

EXAMPLE 6

```
0: wrt 702,"CM1S
 T1"
1: red 702,A
 prt A
2: wait 100
3: sto 1
4: end
*24054
```

This program selects TOTALIZE mode and "output only when addressed." The next line (1) reads this into the A register and it is printed. The "wait" statement gives the 9825A Printer a chance to print the count. The printout is of a low frequency pulse generator operating at about 2 Hz.

Printout

```
  0.00
  1.00
  3.00
  4.00
  6.00
  7.00
  9.00
 10.00
 12.00
 14.00
 15.00
 17.00
 18.00
 20.00
 21.00
 23.00
```

EXAMPLE 7

```
0: wrt 702,"AUSR
 3T0N"
1: wait 2000
2: wrt 702,"SOMB
 HST1"
3: red 702,A
 prt A
4: sto 2
5: end
*17005
```

The program uses the automatic offset feature. Line 0 sets AUTO mode to allow automatic signal acquisition to 1 Hz resolution and front panel SAMPLE RATE control. Once acquisition takes place, MANUAL mode is used to shorten measurement time. A 2-second "wait" statement allows time for the 5343A to do this. Line 2 commands automatic offset, high frequency input, and "output only when addressed." Lines 3, 4, and 5 handle the read and print details, and loop back. The printout shows drift of an 8640B Signal Generator set at about 1 GHz. Numbers are in Hz.

Printout

```
-213.00
-126.00
-135.00
-130.00
-134.00
-130.00
-140.00
-131.00
```

EXAMPLE 8

```
0: wrt 702,"AUSR
 ST0S8D3"
1: red 702,A;
 prt A
2: gto 1
3: end
*10363
```

This program demonstrates use of the programmable Digital-to-Analog Converter. Line Ø selects AUTO mode, 1 Hz resolution, front panel SAMPLE RATE, and sets the DAC to convert digits 3, 4, and 5. A DVM attached to the DAC OUT connector on the rear panel of the 5343A would indicate 9.99V for the "999" in digits 3, 4, and 5. For the "ØØØ" in digits 3, 4, and 5, the DVM would indicate ØV.

Printout

```
 9996527Ø9.ØØ
 9996519Ø4.ØØ
 9996515Ø7.ØØ
 9996511Ø9.ØØ
 9998388Ø3.ØØ
1ØØØ1113Ø4Ø.ØØ
1ØØØ1111Ø59.ØØ
1ØØØ1111231.ØØ
1ØØØ1111187.ØØ
1ØØØ1111Ø62.ØØ
```

3-91. HP-IB PROGRAMMING NOTES

3-92. The HP-IB output is affected by input signal level as follows:

a. For input signal levels greater than or equal to specified sensitivity, the 5343A outputs measurement data as described in paragraph 3-86.

b. For input signal levels less than the actual sensitivity by 0.1 dB or more (or for no input), the counter outputs zeros when addressed to talk.

c. For input signal levels just on the edge of the counter's actual sensitivity (approximately a 0.1 dB band), the detectors which indicate sufficient signal level for counting may become intermittent resulting in very long acquisition times. The counter's display holds the previous reading during the prolonged acquisition but the counter will not output any data when addressed to talk. This will hang up the program at the read statement. To overcome this problem, use the procedure:

(1) To over the problem described in subparagraph c above, when using the 9825A, use the "time" statement and "on err" statement to branch around the read statement if it takes longer than a specified number of milliseconds to complete an I/O operation. The following example program can be used when there is more than one read statement in the program. If there is only one read statement, then statement 2 could be deleted and the end of statement 7 could simply cause the program to go to the statement after the read (in this case, "gto 6"):

EXAMPLE

```
0: dev "ctr";702
1: gto "begin"
2: "er ret":jmp
 er1-1
3: "begin":time
 1000;on err
 "er"
4: wrt "ctr",
 "AUSR4HQMT1"
5: trg "ctr";
 red "ctr";A
6: wait 500;prt
 A;jmp -1
7: "er":if ern=4
 ;0→Atime 1000;
 on err "er";
 gto "er ret"
8: end
*12982
```

Since this statement is in line 2, the program jumps to the statement after the read statement.

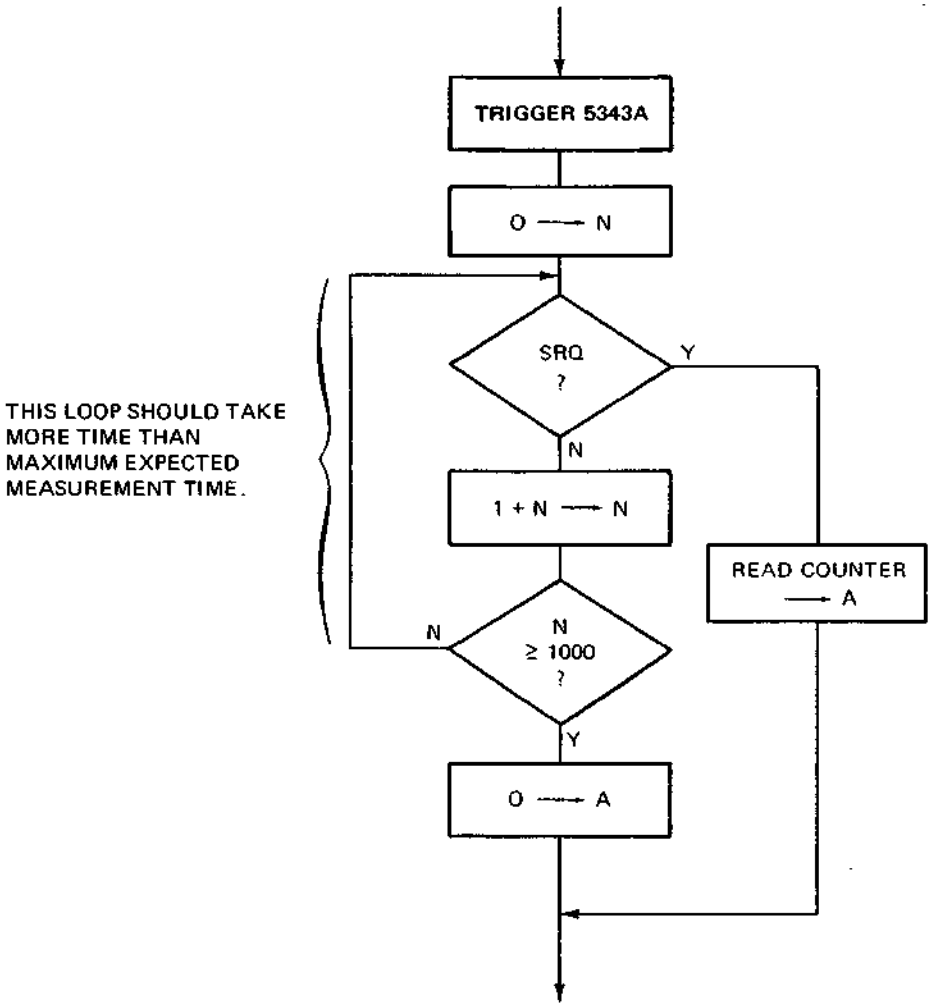
Error 4 is time out error. Reset time and error jump.

Printout

```
10000039130.00
10000039030.00
10000038920.00
          0.00
          0.00
          0.00
          0.00
          0.00
10000038180.00
10000038070.00
10000037950.00
```

When the 5343A took more than 1 second to make the measurement, zeros are output.

3-92. c. (2) To overcome the problem described in subparagraph c above, when using any controller (other than the 9825A), check SRQ to see if a measurement has been complete. Allow an adequate number of iterations on the SRQ check to permit the counter to complete the measurment and pull SRQ low. A flow diagram of such an algorithm is:



SECTION IV
PERFORMANCE TESTS

4-1. INTRODUCTION

4-2. The procedures in this section test the electrical performance of the 5343A using the specifications in *Table 1-1* as performance standards. Those specifications which are inherent to the design (obvious during operation) are not covered in these tests. For example, worst case acquisition time is determined by the period of the sweep and the length of the pseudo-random sequence. If the counter acquires the signal, it must have acquired it in a time less than specified.

4-3. OPERATIONAL VERIFICATION

4-4. The abbreviated checks given in paragraphs 4-12 through 4-15 can be performed to give a high degree of confidence that the 5343A is operating properly without performing the complete performance test. The operational verification should be useful for incoming QA, routine maintenance, and after instrument repair. The Option 004 DAC test is contained in paragraph 4-16. The Option 011 HP-IB Verification Program is described in paragraph 4-17.

4-5. COMPLETE PERFORMANCE TEST

4-6. The complete performance test is given in paragraphs 4-24 through 4-33. All tests can be performed without access to the inside of the instrument.

4-7. EQUIPMENT REQUIRED

4-8. Equipment required for the complete test and operation verification is listed in *Table 1-4*. Any equipment which satisfies the critical specifications given in the table may be substituted for the recommended model numbers.

4-9. TEST RECORD

4-10. Results of the operational verification may be tabulated on the Operational Verification Record, *Table 4-1*. Results of the performance test may be tabulated on the Performance Test Record, *Table 4-5*.

4-11. OPERATIONAL VERIFICATION PROCEDURES

4-12. Self-Check

a. Select 1 Hz resolution, AUTO mode, and 500 MHz—26.5 GHz range. Set self-check mode and verify counter displays 75.000 000 MHz ±1 count.

b. Set 5343A to 10 Hz—500 MHz range. Connect rear panel FREQ STD OUTPUT to front panel BNC input. Select 50Ω impedance. Verify that the 5343A counts 10.000 000 MHz ±1 count.

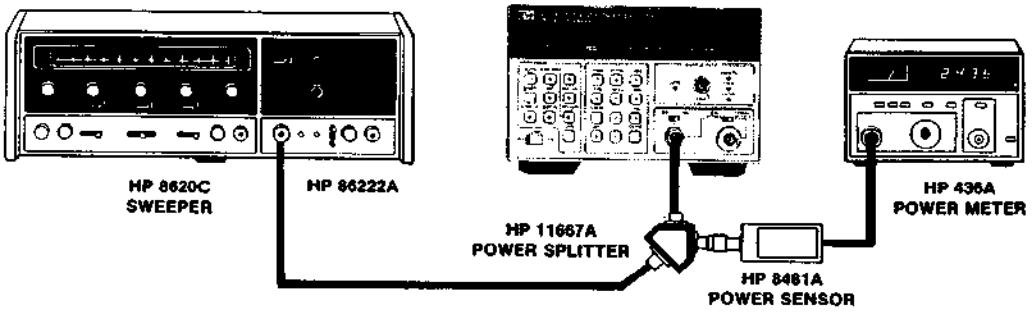
Table 4-1. Operational Verification Record

5343A S/N _____ Date _____

PARAGRAPH NUMBER	TEST	RESULTS PASS	RESULTS FAIL
4-12	Self-Test		
4-13	10 Hz—500 MHz Input Sensitivity Test (50Ω/1 MΩ): 50Ω: 10 MHz 50Ω: 100 MHz 50Ω: 520 MHz 1 MΩ: 25 MHz		
4-14	500 MHz—26.5 GHz Input Sensitivity Test: 500 MHz—12.4 GHz 12.4 GHz—18 GHz 18 GHz—26.5 GHz		
4-16 (Opt. 004 only)	DAC Output Test		
4-17 (Opt. 011 only)	HP-IB Verification		

4-13. 10 Hz—500 MHz Input Sensitivity Test, 50Ω/1 MΩ

Setup:



- Set the 5343A to 10 Hz—500 MHz range and 50Ω.
- Set 8620C to 10 MHz and a level of –19.3 dBm (25 mV rms) as measured on the 436A Power Meter. Measure actual sensitivity and verify that the 5343A counts at 10 MHz, 100 MHz, 520 MHz, and record on operational verification record (*Table 4-1*).
- Disconnect 11667A and connect 8481A directly to 86222A output. Set 8620C to 25 MHz at a level of –19.3 dBm (25 mV rms).
- Disconnect 8481A from 86222A output. Switch 5343A to the 1 MΩ position. Connect 86222A output to 5343A 10 Hz—500 MHz input (86222A supplies 25 mV rms into 50Ω or 50 mV rms into 1 MΩ).
- Verify that the 5343A counts 25 MHz at 50 mV rms and record on operational verification record (*Table 4-1*).

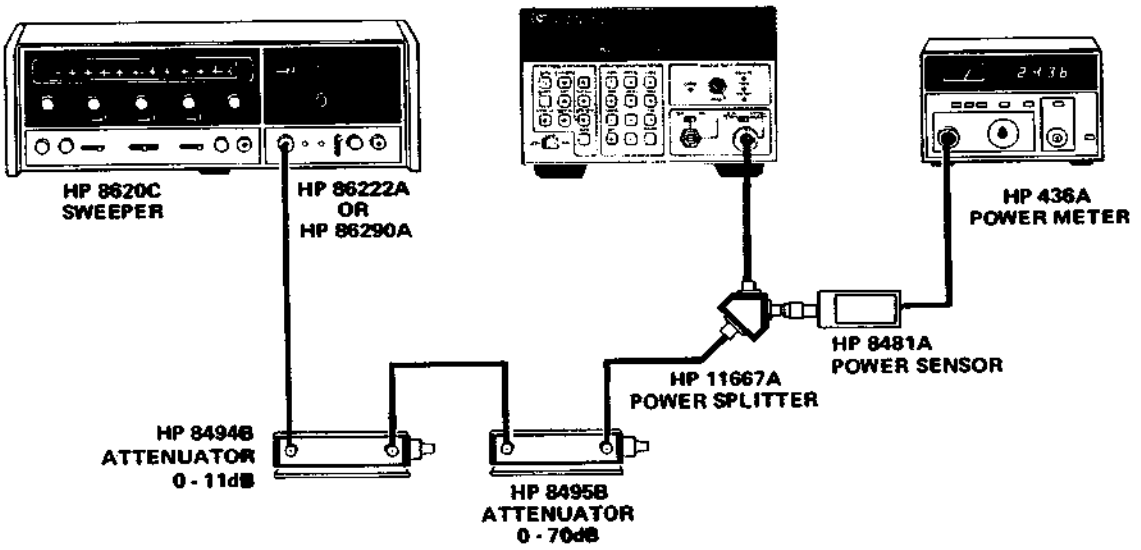
4-14. 500 MHz—26.5 GHz Input Sensitivity Test

4-15. The following test is in two parts, Setup a. for 500 MHz—18 GHz and Setup b. for 18 GHz—26.5 GHz.

Specifications: Sensitivity = -33 dBm, 500 MHz—12.4 GHz
= -28 dBm, 12.4 GHz—18 GHz
= -23 dBm, 18 GHz—26.5 GHz

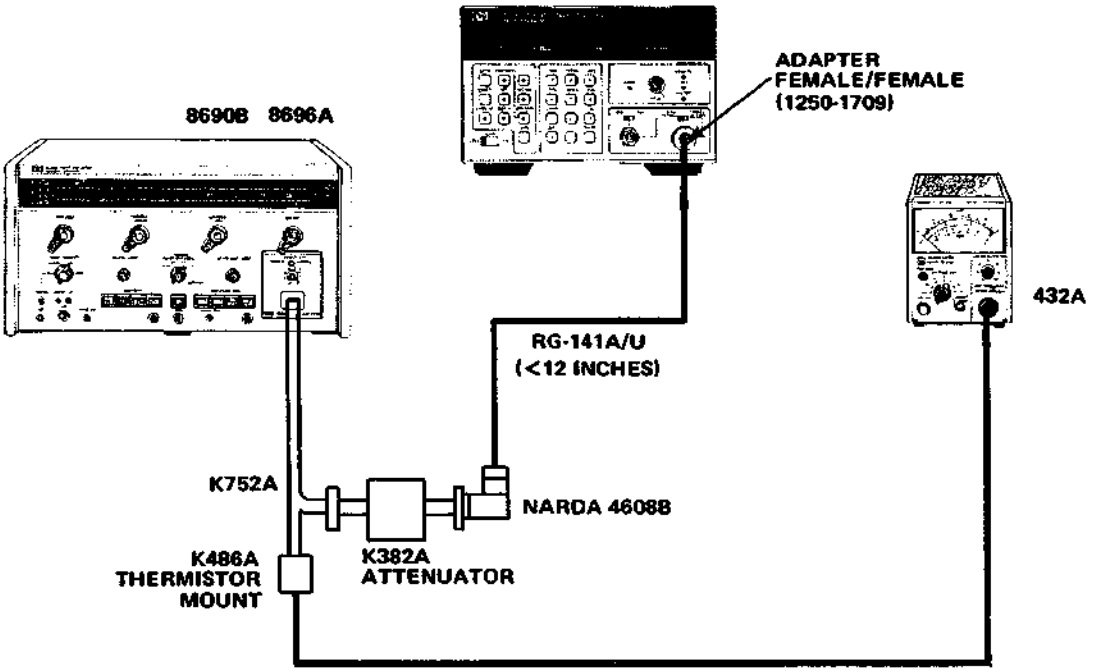
Description: The 5343A is set to the 500 MHz—26.5 GHz range and a signal at the rated sensitivity is applied to the APC-3.5 connector. The frequency is slowly varied over the range of 500 MHz to 12.4 GHz and the 5343A is checked for proper counting. The output level of the test generator is set to the second value, the frequency is slowly varied from 12.4 GHz to 18 GHz, and the 5343A checked for proper counting. The test setup is changed to Setup b. to test the -23 dBm, 18 GHz to 26.5 GHz input.

Setup a. 500 MHz—18 GHz:



- Set the 5343A to the 500 MHz—26.5 GHz range, AUTO mode.
- Connect the equipment as shown in Setup a.
- Set the 8620C with the appropriate plug-in (86222A for 500 MHz to 2 GHz, 86290A for 2 GHz—18 GHz) and the 8495B step attenuator to the rated sensitivity as measured on the 436A.
- Slowly increase the 8620C frequency over the range and verify that the 5343A counts properly.
- Measure actual sensitivity at 500 GHz, 1 GHz, 5 GHz, 10 GHz, 12.4 GHz, 15 GHz, 17 GHz, and 18 GHz. (Check actual applied power each time frequency is changed.) Enter on operational verification record (*Table 4-1*).

Setup b. 18 GHz—26.5 GHz



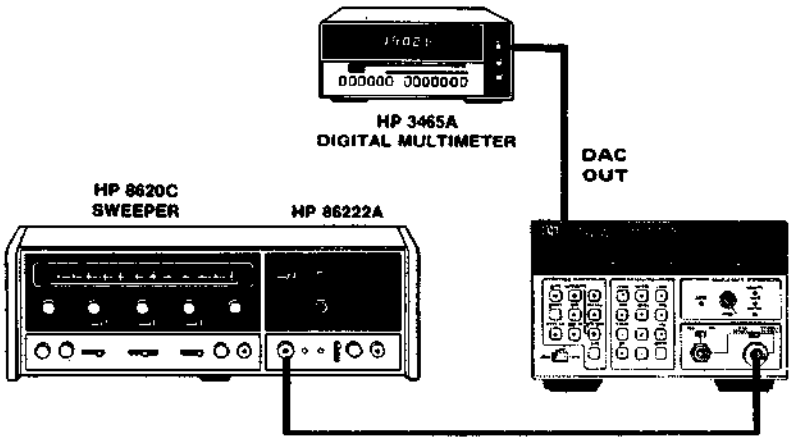
- 5343A settings are same as in Setup a.
- Set 8690B SWEEP SELECTOR to cw, 8696A Power Level 0 or Leveled Power.
- Set K382A attenuator to 40 dB.
- Apply power to 8690B and set frequency to 18 GHz; set output to 0 dBm on 432A.
- Adjust calibration factor on 432A as required.
- Adjust K382A attenuator for a reading of –25 dB.
- Slowly increase the 8690B frequency from 18 to 26.5 GHz and verify that the counts properly.
- Measure actual sensitivity at 18, 20, 22, 24, and 26 GHz and enter results on operational verification record (*Table 4-1*).

4-16. Option 004 Digital-To-Analog Converter (DAC) Output Test

Specification: Accuracy = ±5 mV, ±0.3 mV/°C (from 25°C).

Description: The 5343A is set to the 500 MHz—26.5 GHz range and a 999 MHz signal is applied to the APC-3.5 connector. A DVM is connected to the DAC OUT connector on the rear panel. The front panel keyboard is used to select digits 999 and the DVM observed for an indication of 9.99 volts dc. Then the 000 digits are selected and the DVM observed for 0 volts dc.

Setup:



- Set the 5343A to the 500 MHz—26.5 GHz range, AUTO mode.
- Connect DVM to DAC OUT, set DVM to 20V range.
- Set the generator to 999 MHz as indicated on 5343A display.
- On 5343A keyboard, press:

SET SHIFT DAC 0 3

- Observe DMV for indication of 9.99 ±0.01. Enter on operational verification record (*Table 4-1*).
- On 5343A keyboard, press:

SET SHIFT DAC 0 6

- Observe DVM for 0 ±0.01. Enter on operation verification record (*Table 4-1*).
- On 5343A keyboard, press:

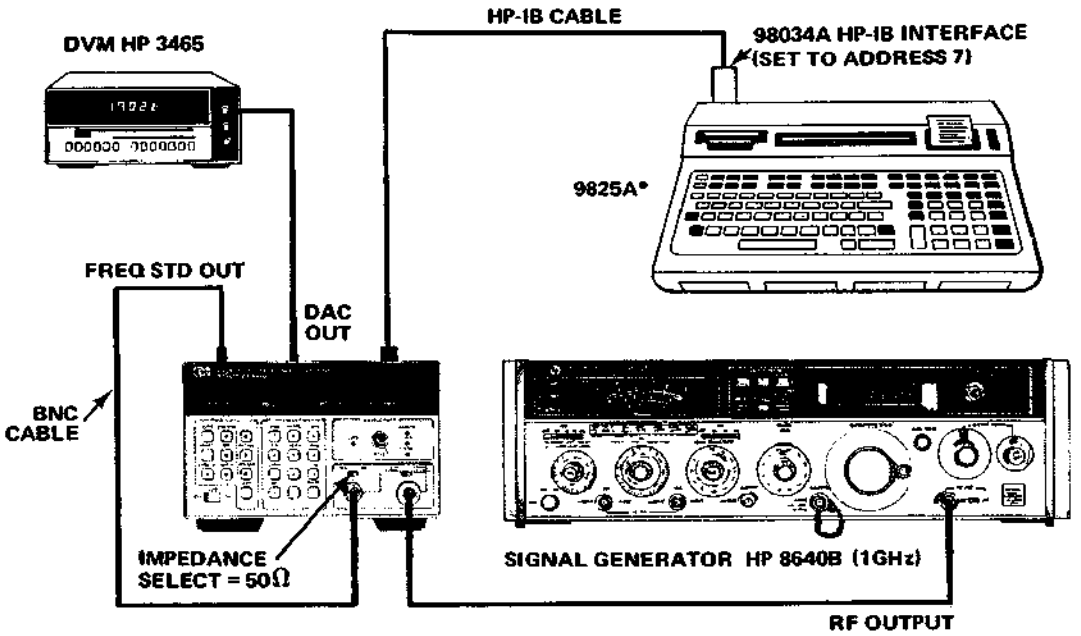
SET SHIFT DAC 0 5

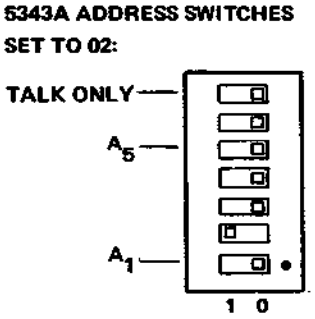
- Observe DVM for 9.00 ±0.01. Enter on test record (*Table 4-1* or *Table 4-5* as applicable.

4-17. Option 011 HP-IB Verification Program

4-18. The 9825A program listed in *Table 4-2* exercises the 5343A through various operating modes, described below, via its HP-IB Interface. If the 5343A successfully completes all phases of the verification program, then there is a high probability that the HP-IB Interface (A15 assembly) is working properly. If the 5343A does not respond as described, refer to HP-IB troubleshooting in Section VIII.

4-19. To perform the verification, set up the 5343A as shown below (DVM used for Option 004 (DAC) only) and set its rear panel address switches to address 02. Set the 8640B to 1 GHz.





*9825 should have either the 98213A General I/O ROM or the 98214A Plotter-General I/O-Extended I/O ROM

4-20. The program listed in *Table 4-2* may be keyed into the 9825A or may be loaded from a HP-IB Verification Cassette, HP P/N 59300-10001, (Revision J or later) which also contrains HP-IB verification programs for the 59300 series of instruments. To run the program on the cassette, insert the cassette into the 9825A, load file 0, and press RUN. Enter "5343" when the instrument model number is requested and select code "702" when select code is requested. The 9825A will then load the 5343A verification program into memory.

4-21. Apply power to the 5343A and verify that the counter powers up in AUTO mode and REMOTE off. Verify that the range switch is placed in the 500 MHz—26.5 GHz position. Set SAMPLE RATE control full ccw.

4-22. The program goes through 16 check points for the standard instrument and an additional 2 check points for the DAC Option 004. The information in *Table 4-3* tells what occurs during each test and what should be observed by the operator if the test has been successfully completed. At the conclusion of each test, the program stops and display the current check point. To advance to the next test, simply press CONTINUE. If it is desired to repeat a test, set the variable L to 1 via the keyboard (1→L EXECUTE). To go on to the next test after looping, set L back to Ø when the program halts (Ø→L EXECUTE). Record on operational verification record (*Table 4-1*), or performance test record (*Table 4-5*) as applicable.

4-23. *Table 4-4* is a sample printout from the 9825A.

Table 4-2. Model 9825A Program

```
0: dim C$[40];dsp "MODEL 5343A Frequency Counter";wait 2000
1: "code":ent "select code?(7XX)..CONTINUE",S
2: if S=721;dsp "error:calculator address";wait 1000;gto "code"
3: if S>730;dsp "out of address range-high";wait 1000;gto "code"
4: if S<700;dsp "out of address range-low";wait 1000;gto "code"
5: dev "ctr",S;prt "5343A HP-IB TEST";spc 2
6: prt "_____","CHECK POINT 1"
7: rem "ctr";beep
8: prt "*REMOTE ON","*LISTEN ON","*AUTO ON";spc 2
9: dsp "CHECK POINT 1___press CONTINUE";stp
10: if L=1;gto 7
11: prt "_____","CHECK POINT 2";spc 2
12: wrt "ctr","M";beep
13: dsp "MANUAL MODE";wait 5000
14: wrt "ctr","AU";beep
15: prt "*MANUAL off","*AUTO on";spc 2
16: dsp "CHECK POINT 2--Press CONTINUE"
17: stp
18: if L=1;gto 12
19: prt "_____","CHECK POINT 3";spc 2
20: wrt "ctr","OM1";beep;dsp "FREQ OFFSET mode";wait 5000
21: wrt "ctr","OM0";beep
22: prt "*OFS[MHZ]  off";spc 2
23: dsp "CHECK POINT 3--Press CONTINUE"
24: stp
25: if L=1;gto 20
26: prt "_____","CHECK POINT 4";spc 2
27: wrt "ctr","L";beep;dsp "Low Range";wait 5000
28: red "ctr",A
29: wrt "ctr","H";beep;dsp "High Range";wait 5000
30: red "ctr",B
31: prt "*Low Range=",A,"*High Range=",B;spc 2
32: dsp "CHECK POINT 4--Press CONTINUE"
33: stp
```

Table 4-2. Model 9825A Program (continued)

```
34: if L=1;gto 27
35: prt "_____","CHECK POINT 5";spc 2
36: wrt "ctr","QS";beep;dsp "Short Acquisition Time";wait 5000
37: wrt "ctr","QM";beep;dsp "Medium Acquisition Time";wait 5000
38: wrt "ctr","QL";beep;dsp "Long Acquisition Time" wait 5000
39: wrt "ctr","QS"
40: prt "*ASTERISK  off","*POUND SIGN off";spc 2
41: dsp "CHECK POINT 5--Press CONTINUE"
42: stp
43: if L=1;gto 36
44: prt "_____","CHECK POINT 6";spc 2
45: dsp "Disconnect Microwave Input(Cont)";stp
46: 3→X
47: fmt 1,"SR",f.0,"SR1";wrt "ctr.1",X;beep
48: X+1→X;wait 3000;if X=10;gto +2
49: gto -2
50: prt "*RES 1 MHZ"
51: dsp "CHECK POINT 7--Press CONTINUE"
52: spc 2;stp
53: if L=1;gto 46
54: prt "_____","CHECK POINT 7";spc 2
55: prt "Enter Manual","Center Frequency";spc 2
56: ent X;fmt 3,"SM",f.0,"E"
57: if X<5e2 or X>1.8e4;prt "LIMIT ERROR";gto -2
58: wrt "ctr.3",X
59: spc 1;prt "Recall Center","Freq";spc 1;fxd 0
60: prt "Does Center Freq=",X
61: dsp "CHECK POINT 8--Press CONTINUE";spc 2;stp
62: if L=1;gto 55
63: prt "_____","CHECK POINT 8","Enter frequency"
64: prt "Offset[MHZ]";spc 2
65: ent X;fmt 4,"SOM",f.6,"E";wrt "ctr.4",X
66: fxd 6;prt "Recall OFS[MHZ]";spc 1;prt "Does OFS[MHZ]=",X
67: dsp "CHECK POINT 9--Press CONTINUE";spc 2;stp
68: if L=1;gto 64
69: prt "_____","CHECK POINT 9";spc 2
70: dsp "Reconnect Microwave Input";wait 3000
71: dsp "Press CONTINUE";stp
72: wrt "ctr","AUOM0HSR9T1"
73: trg "ctr";wait 4000;trg "ctr";beep;wait 4000;trg "ctr";beep
74: prt "2 Measurements--Hold";spc 2
75: wrt "ctr","RESR9T0";prt "Vary SR Pot";spc 2
76: dsp "Press CONTINUE";stp
77: wrt "ctr","T2"
78: prt "Fast Sample";spc 2;dsp "Press CONTINUE";stp
79: wrt "ctr","T3";beep;wait 4000;wrt "ctr","T3";beep;wait 4000
80: wrt "ctr","T3";beep
81: prt "3 Measurements--sample then hold";spc 2
82: dsp "CHECK POINT 10--Press CONTINUE";stp
83: if L=1;gto 72
84: prt "_____","CHECK POINT 10";spc 2
85: wrt "ctr","AUHSR3T0ST1";dsp "Only if Addressed";wait 5000
86: red "ctr",A;beep;prt "Freq=",A
87: wrt "ctr","ST2"
88: dsp "Wait Until Addressed";wait 5000;beep
89: red "ctr",A;prt "Freq=",A;spc 2
```

Table 4-2. Model 9825A Program (continued)

```
90: dsp "CHECK POINT 11--Press CONTINUE";stp
91: if L=1;gto 85
92: prt "_____________","CHECK POINT 11"
93: wrt "ctr","ST1"
94: prt "Enter","Multiplication","Factor";spc 2
95: ent X;fmt 2,"S.",f.0,"E"
96: if X<1 or X>99;prt "LIMIT ERROR";gto -2
97: wrt "ctr.2",X
98: prt "Note Counter","Readout";spc 2
99: dsp "CHECK POINT 12--Press CONTINUE";stp
100: if L=1;gto 94
101: prt "_____________","CHECK POINT 12"
102: wrt "ctr","RE";wait 200
103: wrt "ctr","AUCM1"
104: prt "Totalize Mode On","Observe Counter Display";spc 2
105: wait 5000
106: wrt "ctr","CM0";prt "Totalize Mode","Off";spc 2
107: dsp "CHECK POINT 13--Press CONTINUE";stp
108: if L=1;gto 103
109: prt "_____________","CHECK POINT  13";spc 2
110: wrt "ctr","SWP1"
111: prt "Sweep Mode On";spc 2
112: wait 8000
113: wrt "ctr","SWP0";prt "Sweep Mode Off";spc 2
114: dsp "CHECK POINT 14--Press CONTINUE";stp
115: if L=1;gto 110
116: prt "_____________","CHECK POINT 14";spc 2
117: wrt "ctr","ST2"
118: rds("ctr")+A;dsp A;prt "Status=",A;spc 2
119: trg "ctr";beep;wait 2000
120: rds("ctr")+A;dsp A;prt "Status=",A;spc 2
121: wrt "ctr","ST1"
122: dsp "CHECK POINT 15--Press CONTINUE";stp
123: if L=1;gto 117
124: prt "_____________","CHECK POINT 15";spc 2
125: lcl "ctr";beep
126: prt "REMOTE   OFF";spc 2;dsp "CHECK POINT 16--Press  CONTINUE";stp
127: if L=1;gto -2
128: prt "_____________","CHECK POINT 16";spc 2
129: rem "ctr";dsp "REMOTE ON"
130: llo 7;beep;prt "Local Lockout on";spc 2
131: dsp "Press CONTINUE";stp
132: lcl 7;prt "Return to LOCAL";spc 2
133: prt "REMOTE off";spc 2
134: if L=1;gto 129
135: ent "D/A OPTION INSTALLED?(YES or NO)",C$;if C$="YES";gto +2
136: dsp "END";prt "END";spc 2;stp
137: spc 4;prt "D/A OPTION 004";spc 2
138: prt "_____________","CHECK POINT 1";spc 2
139: rem "ctr";wrt "ctr","AUSBD3T0";beep
140: dsp "Connect DVM to D/A Output(Cont)";stp
141: dsp "Set input to 1000 Mhz(Cont)";stp
142: prt "Note D/A output;0.00 volts?";spc 2
143: prt "_____________","CHECK POINT 2";spc 2
144: dsp "Press--CONTINUE";stp
145: dsp "Set input to 999 Mhz(Cont)";stp
146: prt "Note D/A output;9.99 V?";spc 2
147: if L=1;gto 135
148: dsp "End Of Test";prt "End Of Test";spc 2;wait 5000
*32301
```

Table 4-3. Model 9825A Program Description

CHECK POINT	TEST	OBSERVE ON 5343A
		NOTE Read description below prior to pressing CONTINUE.
1	Remote	Front panel REMOTE, LISTEN, AUTO should light.
2	Manual/Auto	Front panel MANUAL should light for approximately 5 seconds while AUTO goes off. At conclusion of test, AUTO light should be on.
3	Frequency Offset-On/Off	Front panel OFS (MHz) should light for approximately 5 seconds then go off.
4	Range, Low/High,	The counter should display a low range count of 10 MHz (low range input signal) for approximately 5 seconds and then a high range count of 1 GHz (high range input signal). The TALK lamp should also light as 5343A transmits measurements to the 9825A.
5	Acquisition Time Short/Medium/Long	Front panel # sign should light for approximately 5 seconds to indicate medium acquisition time, then front panel asterisk (*) should light for about 5 seconds, to indicate long acquisition time.
		NOTE Remove high frequency input signal (500 MHz—26.5 GHz) during steps 6, 7, and 8.
6	Resolution - 1 Hz to 1 MHz	The counter should display the 75 MHz check frequency (CF) with resolution from 1 Hz to 1 MHz. Each beep from calculator decreases resolution by one decade. There is approximately a 3-second wait between each change.
7	Set Manual Center Frequency	When the 9825A displays X?, enter a manual center frequency (on the 9825A keyboard) in MHz (no decimal points), between 500 MHz and 18000 MHz. Press CONTINUE. Verify that the counter was set to this manual center frequency by pressing RESET, RECALL, then press and hold MANUAL. For example, if 12345 is entered (12.345 GHz manual frequency), then 12.345 GHz should be displayed by the counter when the manual center frequency is recalled.
8	Set Offset Frequency	When the 9825A displays X?, enter a frequency offset in MHz (decimal points allowed). Press CONTINUE. Verify that the counter was set to this frequency offset by pressing RESET, RECALL, then press and hold OFS (MHz). For example, if 1234.5678987 is entered, then 12.345678987 GHz should be displayed by the counter when the frequency offset is recalled.
		NOTE Reconnect high frequency input signal (500 MHz—26.5 GHz) at this point.
9	Sample Rate — Hold, Front Panel Control, Fast Sample, Sample and Hold	For each beep of the calculator, observe that the 5343A GATE lights. After the second measurement, the 5343A is programmed for front panel control. Vary the front panel SAMPLE RATE pot and observe the change in GATE delay. Press CONTINUE and the 5343A is programmed for fast sample. Verify that the front panel pot has no effect (there is minimum time between measurements). Press CONTINUE and the 5343A is programmed for Sample and Hold. Before each beep from the 9825A, the 5343A is sent T3 which takes one measurement and holds.
		NOTE Resolution is set to 1 MHz to enable faster gate times and better visibility of control action.

Table 4-3. Model 9825A Program Description (continued)

CHECK POINT	TEST	OBSERVE ON 5343A
10	Only If/Wait Until Addressed	At the start of this test, the 5343A is placed in the ONLY IF addressed mode. The GATE light should continually light, indicating that measurements are continually being made until the 5343A is addressed to talk. The counter is addressed to talk and the value is printed. The counter is then placed in WAIT UNTIL addressed. The GATE light should go out after the first measurement and remain out, indicating that the first measurement is being saved until the counter is addressed to talk. It is then addressed to talk and the value is printed by the printer. Note action of the TALK lamp.
11	Multiply	When the 9825A prints "enter x" enter a multiplication factor (on the 9825A keyboard) between 1 and 99 (no decimal points allowed). Verify that the counter reads "x" times the original input frequency, i.e., if 1 GHz is applied, the counter should read 3 GHz. **NOTE** The "RESET, RECALL, decimal point" keyboard routine to recall the entered factor will not work. When RESET is pressed, the factor is RESET to 1.
12	Totalize	When the 9825A prints "Totalize Mode on", the 5343A is "open gate" (observe GATE lamp is on) and the pulse generator output is totalized on the display. This continues for approximately 5 seconds.
13	Sweep	When 9825A prints "Sweep Mode on", observe slow blinking SWP M key indicator and blank display. This will occur for 8 seconds; at that point, the 9825A will command "Sweep Mode off" and print this command.
14	Status Byte	The 5343A is put in HOLD and serial poll mode. Its status byte is displayed by the 9825A. After approximately 5 seconds, the 5343A is triggered and a measurement is taken. The status byte displayed by the 9825A should change from 0 to 80, indicating that the 5343A has taken a measurement.
15	Go To Local	LCL 702 is issued. The front panel REMOTE light should go off. Listen light will still be on.
16	Local Lockout	The 5343A is returned to remote control and the local lockout command is issued. When the 9825A displays "press CONTINUE", press RESET on the 5343A and verify that the counter remains in REMOTE. Press CONTINUE on the 9825A and lcl 7 is issued. Verify that the 5343A goes to local.
DAC Option 004	DAC Lower Limit	When 9825A displays "DAC Option installed?" Press YES, CONTINUE. When 9825A displays "connect DVM to DAC output", connect a digital voltmeter to the DAC OUT jack. Set DVM to DCV, 20V range. Press CONTINUE and the 9825A will display "set input to 1000 MHz". Adjust the input signal frequency to 1000 MHz. Program sets digits 3, 4, and 5 to be converted (counting from left end of display). Thus, a 5343A display of 1000 MHz should result in a DVM reading of zero volts.
Checkpoint 2	DAC Upper Limit	Set input frequency to 999 MHz. DVM output should change to 9.99V. Adjust frequency across the range of 1000 to 999 MHz to verify tracking of DAC.

Table 4-4. Sample Printout

```
5343A HP-IB TEST


---------------
CHECK POINT 1
*REMOTE ON
*LISTEN ON
*AUTO ON


---------------
CHECK POINT 2

*MANUAL off
*AUTO on


---------------
CHECK POINT 3

*OFS[MHZ]  off


---------------
CHECK POINT 4

*Low Range=
     10000000.00
*High Range=
   1000262404.00


---------------
CHECK POINT 5

*ASTERISK  off
*POUND SIGN off


---------------
CHECK POINT 6

*RES 1 MHZ


---------------
CHECK POINT 7

Enter Manual
Center Frequency


Recall Center
Freq

Does Center Freq
=          12345


---------------
CHECK POINT 8
Enter frequency
Offset[MHZ]

Recall OFS[MHZ]

Does OFS[MHZ]=
     1234.567899


---------------
CHECK POINT 9

2 Measurements--
Hold .

Vary SR Pot

Fast Sample

3 Measurements--
sample then hold


---------------
CHECK POINT 10

Freq=
 1.000262211e 09
Freq=
 1.000262212e 09


---------------
CHECK POINT 11
Enter
Multiplication
Factor

Note Counter
Readout


---------------
CHECK POINT 12
Totalize Mode On
Observe Counter
Display

Totalize Mode
Off


---------------
CHECK POINT 13

Sweep Mode On

Sweep Mode Off


---------------
CHECK POINT 14

Status= 0.000000

Status=
       80.000000


---------------
CHECK POINT 15

REMOTE   OFF


---------------
CHECK POINT 16

Local Lockout on

Return to LOCAL

REMOTE off

END

D/A OPTION 004


---------------
CHECK POINT 1

Note D/A output;
0.00 volts?


---------------
CHECK POINT 2

Note D/A output;
9.99 V?

End Of Test
```

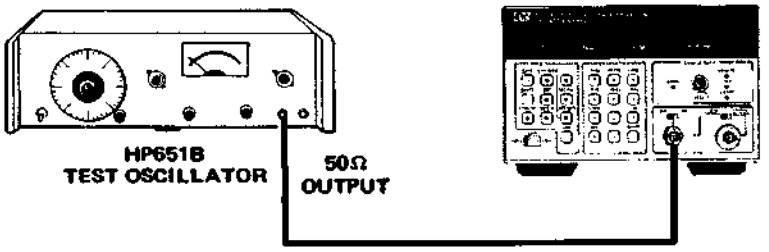
4-24. PERFORMANCE TEST PROCEDURES

4-25. 10 Hz—500 MHz Input Sensitivity Test, 50Ω

Specification: 50Ω position, sensitivity = 25 mV rms for frequencies from 10 Hz—520 MHz.

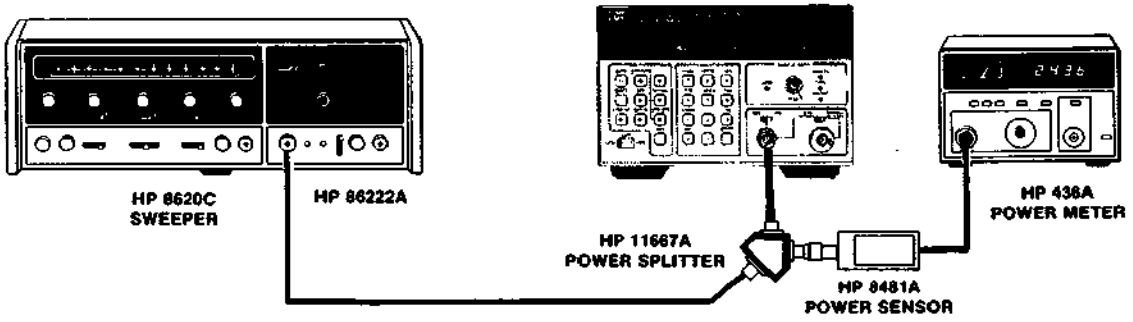
Description: The 5343A is set to the 10 Hz—500 MHz range and a signal at the rated sensitivity is applied to the BNC input. The frequency is slowly swept up to 10 MHz at constant level and the 5343A reading is checked for the proper count. For the range of 10 MHz to 520 MHz, a different genrator is used.

Setup a: 10 Hz—10 MHz



- Set the 5343A to 50Ω, 10 Hz—500 MHz range, 1 Hz resolution.
- Set 651B to 10 Hz and 25 mV rms.
- Increase the frequency of the 651B and verify that the 5343A counts proper frequency from 10 Hz to 10 MHz.
- Measure actual sensitivity by decreasing the 651B level until the 5343A gives an unstable count at these frequencies: 10 Hz, 1 kHz, 500 kHz, 5 MHz, 10 MHz. Enter on performance test record (*Table 4-5*).

Setup b: 10 MHz—520 MHz

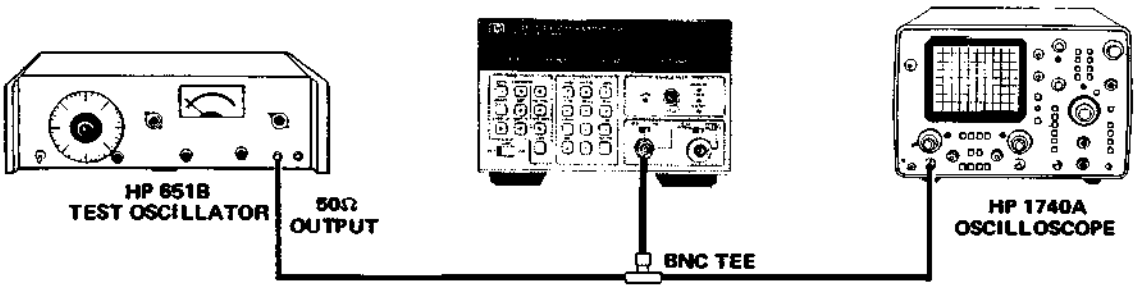


- 5343A settings remain unchanged.
- Set 436A power meter for AUTO range and dBm mode.
- Set the 86222A for INT leveling and adjust the output power level for a 436A reading of –19.3 dBm (25 mV rms into 50Ω).
- Increase the frequency of the 8620C over the range of 10 MHz to 520 MHz and verify that the 5343A counts proper frequency. Use 436A to verify input power.
- Measure actual sensitivity at 50 MHz, 250 MHz, 520 MHz, and enter on performance test record (*Table 4-5*).

4-26. 10 Hz—500 MHz Input Sensitivity Test, 1 MΩ

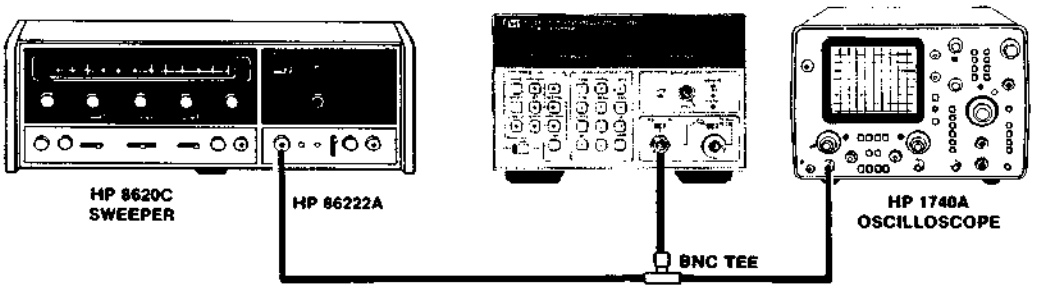
Specification: 1 MΩ position, sensitivity = 50 mV rms for frequencies from 10 Hz—25 MHz.

Setup a. 10 Hz—10 MHz



- Set the 5343A to 1 MΩ, 10 Hz—500 MHz range.
- Set the 651B to 10 Hz and adjust level for 141 mV p-p signal (50 mV rms).
- Increase the frequency of the 651B and verify that the 5343A counts proper frequency from 10 Hz to 10 MHz.
- Measure actual sensitivity at 10 Hz, 1 kHz, 500 kHz, 5 MHz, and 10 MHz by monitoring p-p voltage on oscilloscope. Enter on performance test record (*Table 4-5*).

Setup b. 10 MHz—25 MHz



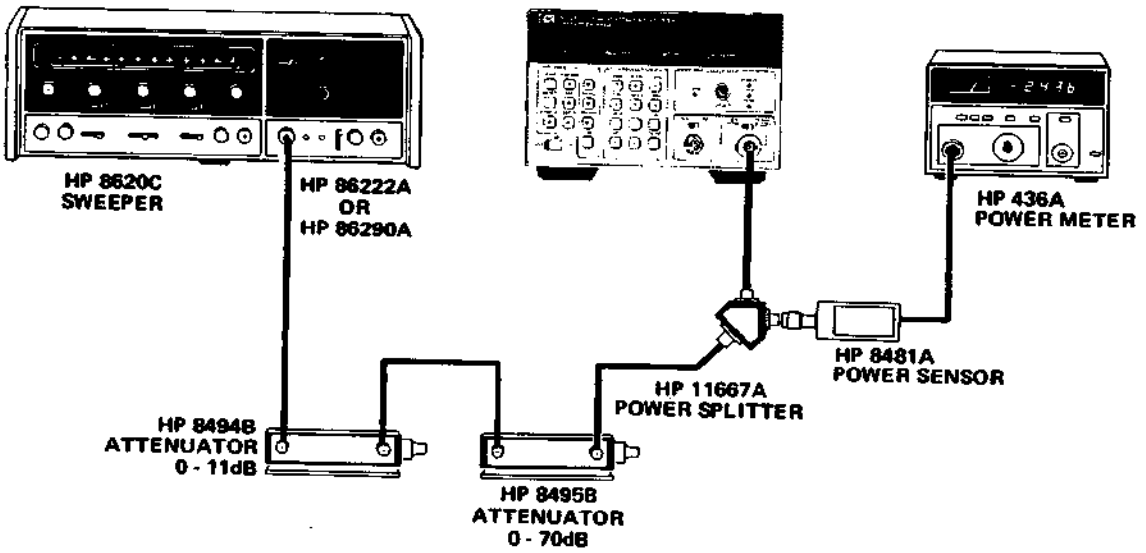
- 5343A settings remain unchanged.
- Adjust 86222A output for a 141 mV p-p (50 mV rms) reading on the 1740A.
- Increase the frequency of the 8620C from 10 MHz—25 MHz and verify that the counter counts properly. Monitor the output level on the oscilloscope for 141 mV p-p (50 mV rms) over the range.
- Measure actual sensitivity at 15 MHz, 25 MHz, and enter on performance test record (*Table 4-5*).

4-27. 500 MHz—26.5 GHz Input Sensitivity Test

Specifications: Sensitivity = -33 dBm, 500 MHz—12.4 GHz
= -28 dBm, 12.4 GHz—18 GHz
= -23 dBm, 18 GHz—26.5 GHz

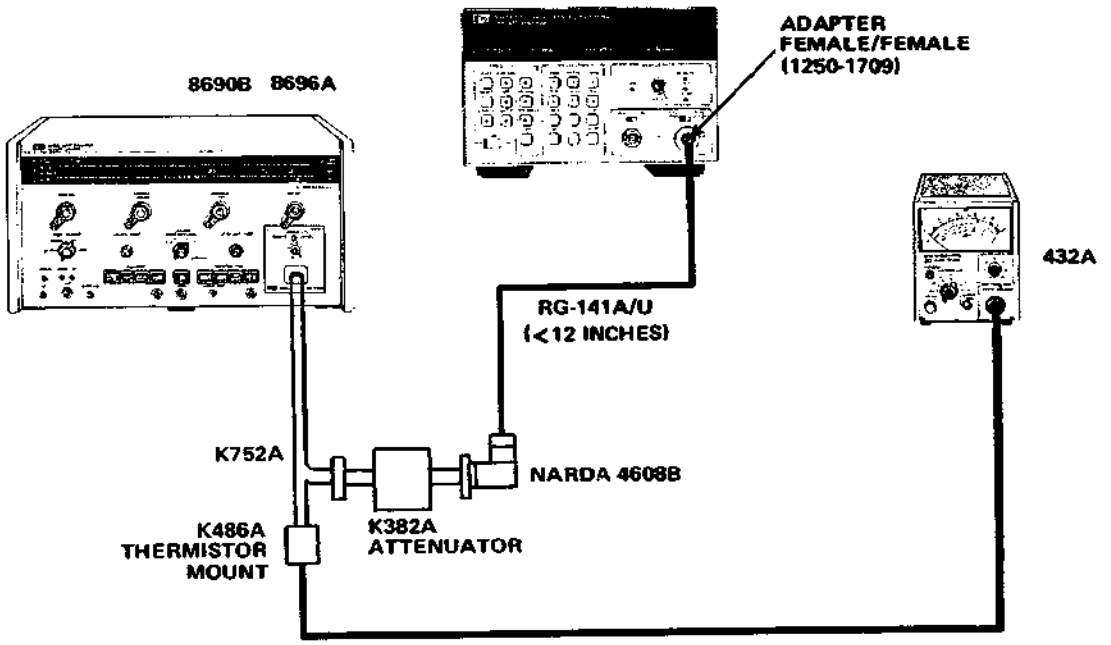
Description: The 5343A is set to the 500 MHz—26.5 GHz range and a signal at the rated sensitivity is applied to the APC-3.5 connector. The frequency is slowly varied over the range of 500 MHz to 12.4 GHz and the 5343A is checked for proper counting. The output level of the test generator is set to the second value, the frequency is slowly varied from 12.4 GHz to 18 GHz, and the 5343A checked for proper counting. The test setup is changed to Setup b. to test the -23 dBm, 18 GHz to 26.5 GHz input.

Setup a. 500 MHz—18 GHz:



- Set the 5343A to the 500 MHz—26.5 GHz range, AUTO mode.
- Connect the equipment as shown in Setup a.
- Set the 8620C with the appropriate plug-in (86222A for 500 MHz to 2 GHz, 86290A for 2 GHz—18 GHz) and the 8495B step attenuator to the rated sensitivity as measured on the 436A.
- Slowly increase the 8620C frequency over the range and verify that the 5343A counts properly.
- Measure actual sensitivity at 500 GHz, 1 GHz,5 GHz, 10 GHz, 12.4 GHz, 15 GHz, 17 GHz and 18 GHz. (Check actual applied power each time frequency is changed.) Enter on performance test record (*Table 4-5*).

Setup b. 18 GHz—26.5 GHz



- 5343A settings are same as in Setup a.
- Set 8690B SWEEP SELECTOR to cw, 8696A Power Level Ø or Leveled Power.
- Set K382A attenuator to 40 dB.
- Apply power to 8690B and set frequency to 18 GHz; set output to Ø dBm on 432A.
- Adjust calibration factor on 432A as required.
- Adjust K382A attenuator for a reading of -25 dB.
- Slowly increase the 8690B frequency from 18 to 26.5 GHz and verify that the 5343A counts properly.
- Measure actual sensitivity at 18, 20, 22, 24, and 26 GHz and enter results on performance test record (*Table 4-5*).

4-28. FM Tolerance Test

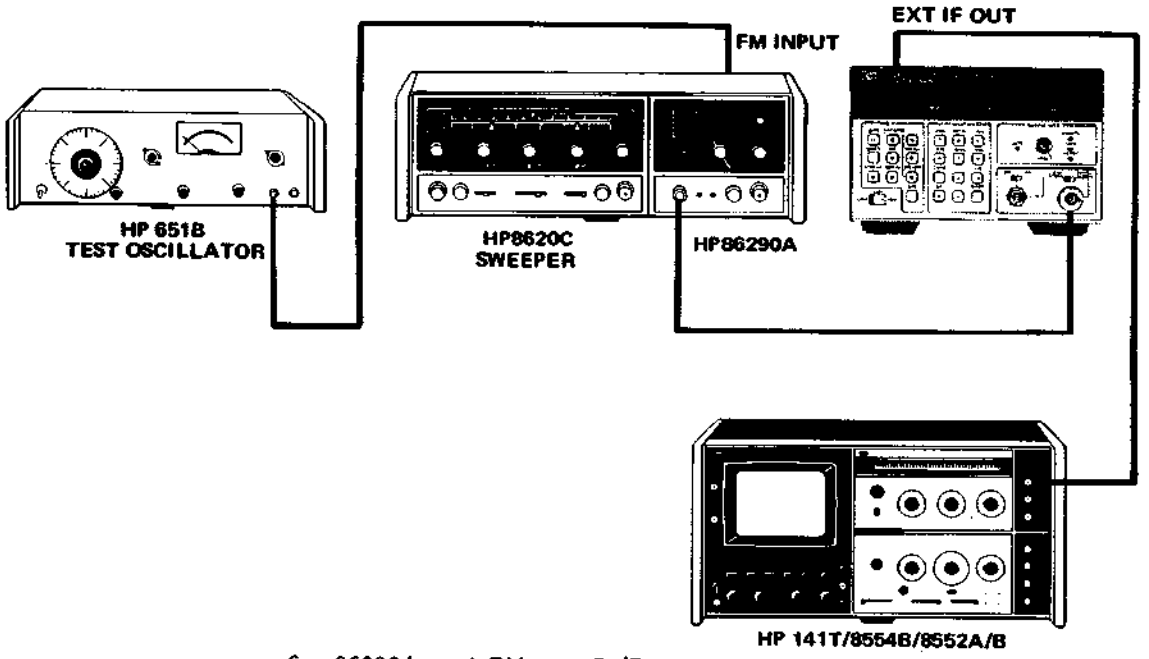
Specifications: 6 MHz peak-to-peak (FAST)
20 MHz peak-to-peak (MEDIUM)
50 MHz peak-to-peak (SLOW)

Description: The FM tolerance specification indicates the worst case FM deviation which can be present on a carrier that the counter can acquire and count. If the deviations are symmetrical about the carrier, then the counter averages out the deviations and displays the carrier frequency.

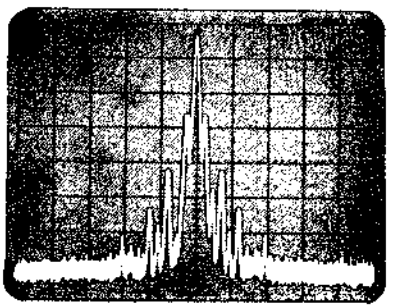
A rear panel switch controls the acquisition time (fast, medium, slow).

In this test, a function generator is used to FM the 8620C and the output is examined on a spectrum analyzer to measure the peak-to-peak deviation. The amplitude of the modulating waveform is adjusted for a 6 MHz p-p deviation, a 20 MHz p-p deviation, and a 50 MHz p-p deviation.

Setup:



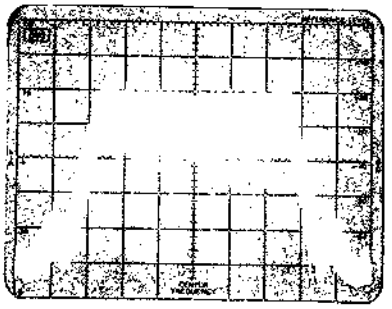
- Set 86290A to 4 GHz at -5 dBm.
- Put 5343A in 500 MHz—26.5 GHz range and AUTO mode. Observe IF OUT on the spectrum analyzer. Set 5343A to MANUAL mode to setup peak-to-peak deviation.



2 MHz/div.
100 kHz BW
Ref Level = 0 dBm

IF ≅ 75 MHz
PRS = 6 MHz (Fast)
Signal = EXT IF out showing no modulation

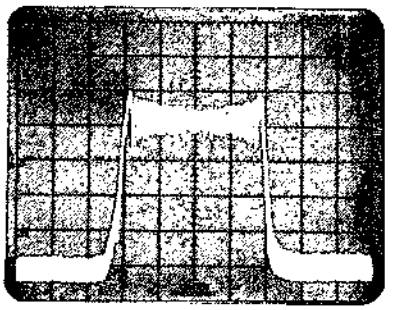
- Set the 5343A rear panel ACQ TIME switch to FAST (6 MHz p-p FM) position.
- Apply modulating signal to EXT FM input on the rear panel of 86290A. Use a 100 kHz sine wave of sufficient amplitude to give 6 MHz p-p FM deviation as shown. (Modulating rate for this photo was 100 kHz.) Record on performance test record (*Table 4-5*).
- Switch the counter from MANUAL to AUTO to verify that the counter will acquire and count the signal. Turn RF off and back on at 8620C sweeper as a further check in acquiring and counting the signal.



1 MHz/div.
30 kHz BW
Ref Level = 0 dBm

IF ≅ 75 MHz
PRS = 6 MHz (Fast)
Signal = EXT IF out showing 6 MHz p-p FM Deviation

- If deviations are symmetrical about center frequency, the 5343A will average out the deviations and display the 4.0 GHz center frequency.
- Return to MAN mode. Increase amplitude of modulating waveform to produce a 20 MHz p-p deviation as shown below (f_m = 100 kHz). Record on performance test record (*Table 4-5*).

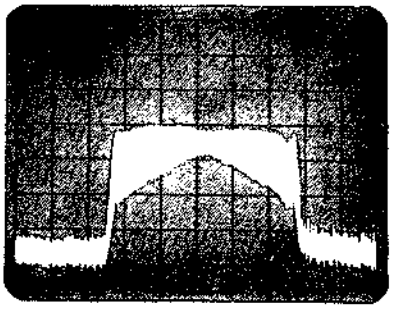


5 MHz/div.
100 kHz BW
Ref Level = 0 dBm

IF ≅ 75 MHz
PRS = 20 MHz (Medium)
Signal = EXT IF out showing 20 MHz p-p FM Deviation

- Switch rear panel ACQ TIME switch to MED. Switch counter from MAN to AUTO. Verify that the counter will acquire and count the signal.
- If deviations are symmetrical about the center frequency, the 5343A will average out the deviations and display the 4.0 GHz center frequency. For this case, the deviation is not symmetrical about the center frequency. To verify that the counter has passed the test, check that the displayed frequency is within 300 MHz of 4 GHz (if the N number computed is off by 1 due to excessive FM, then the displayed frequency will be off by 300 to 350 MHz).

- Return to the MAN mode. Increase amplitude of modulating waveform to produce a 50 MHz p-p deviation as shown below (f_m = 100 kHz). Record on performance test record (*Table 4-5*).



10 MHz/div.
300 kHz BW
Ref Level = 0 dBm

IF ≅ 75 MHz
PRS = 50 MHz (Slow)
Signal = EXT IF out showing 50 MHz p-p FM Deviation

- Set rear panel switch to slow. Switch counter from MAN to AUTO. Verify that the counter will acquire and count the signal.

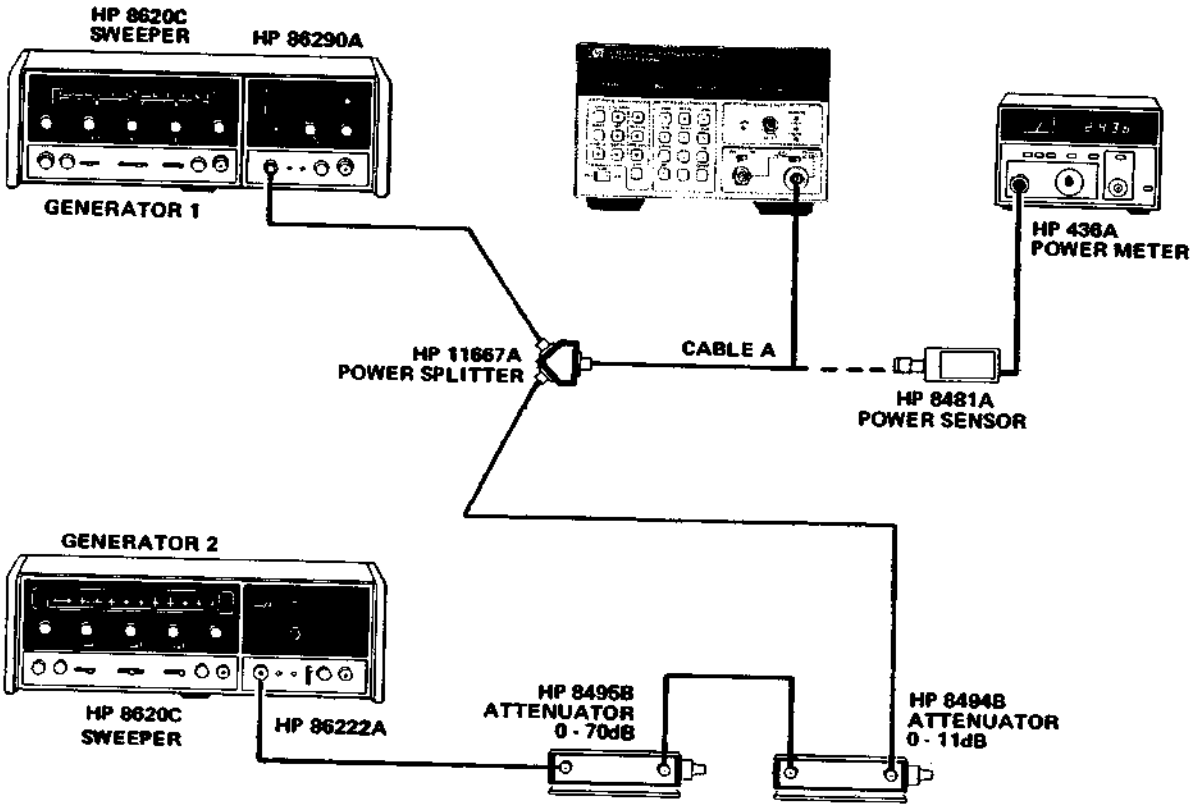
- If deviations are symmetrical about the center frequency, the 5343A will average out the deviations and display the 4.0 GHz center frequency. For this case, the deviation is not symmetrical about the center frequency. To verify that the counter has passed the test, check that the displayed frequency is within 300 MHz of 4 GHz (if the N number computed is off by 1 due to excessive FM, then the displayed frequency will be off by 300 to 350 MHz).

4-29. Automatic Amplitude Discrimination Test

Specification: The 5343A measures the largest of all signals present, providing that the signal is 6 dB above any signal within 500 MHz; 20 dB above any signal not within 500 MHz.

Description: In this test, two microwave generators are used to provide two signals into the 5343A. The relative level of the two signals is adjusted to the specification and the 5343A must count the higher amplitude signal.

Setup:



- Set generator 1 to 18 GHz and at a level to deliver -5 dBm to the 5343A. To set this level, disconnect generator 2 from the 11667A and terminate that input port of the 11667A with a 909A (Option 012) 50Ω termination. Connect the 8481A to the 5343A end of cable A and adjust the 86290A output for a -5 dBm reading.
- Set generator 2 to 500 MHz and at a level to deliver -25 dBm to the 5343A. To set this level, disconnect generator 1 from the 11667A input (reconnect generator 2 to 11667A) and terminate the generator 1 input of the 11667A with a 909A 50Ω termination. Connect the 8481A to the 5343A end of cable A and adjust 86222A for a 0 dBm reading. Dial in 25 dB attenuation using step attenuators.
- Connect both generators to the 11667A inputs. Connect cable A to the 5343A. Verify that the 5343A counts 18 GHz. Increase the level of generator 2 until the 5343A counts incorrectly — measure that level (by using the same procedure described above) or simply read the attenuator dials, and record on test record.

- Set generator 1 to 2.5 GHz and at a level to deliver -5 dBm to the 5343A using the technique described above. Set generator 2 to 2.0 GHz and at a level to deliver -11 dBm to the 5343A using the technique described above. Connect both generators to the 11667A and cable A to the 5343A. Verify that the 5343A counts 2.5 GHz. Increase generator 2 level until counter counts incorrectly — measure that level and record on test record (*Table 4-5*).

4-30. Digital-to-Analog Converter (DAC) Output Test (Option 004)

4-31. Perform the procedures in paragraph 4-16.

4-32. HP-IB Verification Test (Option 011)

4-33. Perform the procedures in paragraph 4-17.

Table 4-5. Performance Test Record

5343A S/N _____ Date _____

PARAGRAPH NO.	TEST	RESULTS
4-25	10 Hz—500 MHz Input Sensitivity (50Ω): 10 Hz 1 kHz 500 kHz 5 MHz 10 MHz 50 MHz 250 MHz 520 MHz	_____ 25 mV rms _____ ↓ _____ _____ _____ _____ _____ _____
4-26	10 Hz—500 MHz Input Sensitivity (1 MΩ): 10 Hz 1 kHz 500 kHz 5 MHz 10 MHz 15 MHz 25 MHz	_____ 50 mV rms _____ (141 mV p-p) _____ ↓ _____ _____ _____ _____
4-27	500 MHz— 26.5 GHz Input Sensitivity: 500 MHz 1 GHz 5 GHz 10 GHz 12.4 GHz 15 GHz 17 GHz 18 GHz 26.5 GHz	_____ -33 dBm _____ ↓ _____ _____ _____ _____ -28 dBm _____ ↓ _____ _____ -23 dBm
4-28	FM Tolerance: FAST (6 MHz p-p) MED (20 MHz p-p) SLOW (50 MHz p-p)	Pass _____ Pass _____ Pass _____
4-29	Automatic Amplitude Discrimination: 17.5 GHz separation 500 MHz separation	_____ 20 dB _____ 6 dB
4-30 (Option. 004)	DAC Output Test	_____
4-31 (Option 011)	HP-IB Verification	_____

SECTION V
ADJUSTMENTS

5-1. INTRODUCTION

5-2. This section describes the adjustments required to maintain the 5343A's operating characteristics within specifications. Adjustments should be made when required, such as after a performance test failure or when components are replaced that may affect an adjustment.

5-3. *Table 5-1* is a list of all adjustable components in the 5343A and indicates the order in which adjustments should be performed.

5-4. EQUIPMENT REQUIRED

5-5. The test equipment required for the adjustment procedures is listed in *Table 1-4*, Recommended Test Equipment. Substitute instruments may be used if they meet the critical specifications.

5-6. FACTORY SELECTED COMPONENTS

5-7. Factory selected components are identified by an asterisk (*) in parts lists and schematic diagrams. Refer to paragraph 8-36 for replacement information.

5-8. ADJUSTMENT LOCATIONS

5-9. Adjustment locations are identified in the component locators in the Section VIII schematic diagrams and in the top view of the instrument, *Figure 8-21*.

5-10. SAFETY CONSIDERATIONS

5-11. This section contains warnings that must be followed for your protection and to avoid damage to the equipment.

WARNING

MAINTENANCE DESCRIBED HEREIN IS PERFORMED WITH POWER SUPPLIED TO THE INSTRUMENT, AND PROTECTIVE COVERS REMOVED. SUCH MAINTENANCE SHOULD BE PERFORMED ONLY BY SERVICE-TRAINED PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED (FOR EXAMPLE, FIRE AND ELECTRICAL SHOCK). WHERE MAINTENANCE CAN BE PERFORMED WITHOUT POWER APPLIED, THE POWER SHOULD BE REMOVED.

BEFORE ANY REPAIR IS COMPLETED, ENSURE THAT ALL SAFETY FEATURES ARE INTACT AND FUNCTIONING, AND THAT ALL NECESSARY PARTS ARE CONNECTED TO THEIR PROTECTIVE GROUNDING MEANS.

Table 5-1. Adjustments

NAME	REFERENCE DESIGNATOR	NAME	POWER	ORDER
1. Power Supply Adjustments				Should be done first in following order:
	A21R27	—	Set frequency of switching regulator to 20 kHz.	(1)
	A21R17	—	Sets reference voltage against which +5V (D) is compared.	(2)
	A19R5	—	Sets current level at which shutdown occurs.	(3)
2. Main Synthesizer Adjustment	A8R22	—	Sets free-run frequency of A8 Main VCO.	Can be done anytime
3. Offset Synthesizer Adjustments				Should be done after Main Synthesizer adjustment in following order:
	A4R1	—	Sets free-run frequency of A4 OFFSET VCO.	(1)
	A6R1, A6R2	—	Set center and extremes of triangular search waveform on A6.	(2)
4. IF Adjustments				Can be done anytime in following order:
	A25A1R7	"BAL"	Maximizes gain through A25U2.	(1)
	A25A1C19	—	Sets rolloff at 175 MHz	(2)
	A11R1	"AMP"	Maximize gain through A11U2.	(3)
	A12R2	"B1"	Maximize gain through A12U2.	(4)
	A12R13	"B2"	Maximize gain through A12U4.	(5)
	A12R7	"OFS"	Sets level detector so counter counts 1 GHz, -33 dBm.	(6)
5. Direct Count Adjustment	A3R8	—	Adjust for maximum sensitivity.	Can be done anytime
6. Digital-to-Analog (DAC) Adjustments-(Option. 004)	A2R25	GAIN	Adjust maximum (9.99V) DAC output.	Can be done anytime
	A2R27	OFFSET	Adjusts minimum (0V) DAC output.	

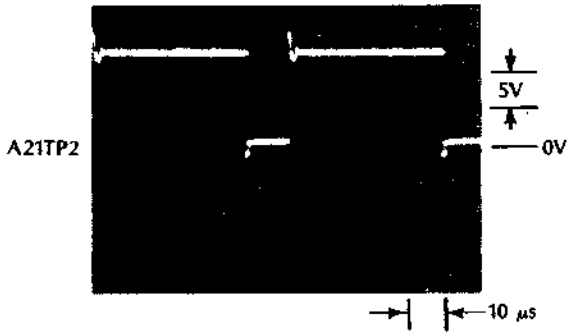
5-12. ADJUSTMENT PROCEDURES

5-13. Power Supply Adjustments

5-14. Adjust resistor A21R27 (20 kHz frequency) as follows:

a. Place A21 on extender board. Monitor A21TP2 with an oscilloscope.

b. Adjust A21R27 (bottom, right side pot) for a 50 (±1) μs period as shown:



5-15. Adjust resistor A21R17, +5V (D) as follows:

With a 3465A Multimeter in the DAC VOLTS FUNCTION and 20V range, measure the dc voltage of the -5.2V supply at XA21(5, $\overline{5}$). Adjust A21R17 for a -5.20 (-0.1, +0.05)V dc.

WARNING

PRIOR TO MAKING THE FOLLOWING ADJUSTMENT ON THE A19 PRIMARY POWER ASSEMBLY, THE 5343A MUST BE ISOLATED FROM THE POWER MAINS BY USE OF AN ISOLATION TRANSFORMER, SUCH AS AN ALLIED ELECTRONICS 705-0165 (115/230V AC). CONNECT THE ISOLATION TRANSFORMER BETWEEN THE AC POWER SOURCE AND THE AC POWER INPUT TO THE 5343A.

5-16. After adjusting resistors A21R27 and A21R17 (paragrahps 5-14 and 5-15), adjust resistor A19R5 (over-current threshold) as follows:

NOTE

The following adjustment requires the use of a variable transformer to vary the ac line voltage, such as an Allied Electronics 927-6010 (120V) or 927-6120 (240V). Insert this transformer between the isolation transformer and the 5343A.

a. Ensure that all printed circuit assemblies are installed (including options on hand) so the power supply is properly loaded.

b. Check the pc line voltage selector (paragraph 2-6) for correct position before applying power.

c. Ajust the variable transformer to supply a voltage that is 10 percent lower than the nominal power mains voltage in use.

d. Insert an insulated screwdriver through a hole in the plastic strip along the top edge of A19 and adjust resistor R5 fully counterclockwise.

e. Adjust resistor R5 clockwise slowly until the red LED on A21 board turns on and the green LED on the A20 board turns off. Then adjust R5 counterclockwise just to the point where the red LED goes off and the green LED comes back on.

f. Turn off the 5343A power switch, then back on to check the results of the adjustment.

g. If the red LED stays on, repeat the adjustment.

5-17. Main Synthesizer Adjustment

5-18. Adjust resistor A8R22 (Main VCO free-run frequency) as follows:

a. Put 5343A in 10 Hz—500 MHz range, 50Ω. Using cable with BNC on one end, clip leads on the other, connect XA5($\overline{10}$), the Main OSC signal, to the direct count input of the 5343A and measure the main VCO frequency.

b. With a clip lead, ground A9TP1.

c. Adjust A8R22 for a 325 (±2) MHz reading.

d. Remove ground on A9TP1.

5-19. Offset Synthesizer Adjustments

5-20. Offset Synthesizer adjustments are made on assemblies A4 and A6 as follows:

a. Adjust A4R1 (Offset VCO free-run frequency) as follows:

1. Put 5343A in 10 Hz—500 MHz range, 50Ω. Using cable with BNC on one end, clip leads on the other, connect XA4($\overline{10}$), the Offset OSC signal, to the direct count input of the 5343A and measure the Offset VCO frequency.

2. With a clip lead, ground A6TP1.

3. Adjust A4R1 for a 325 (±2) MHz reading.

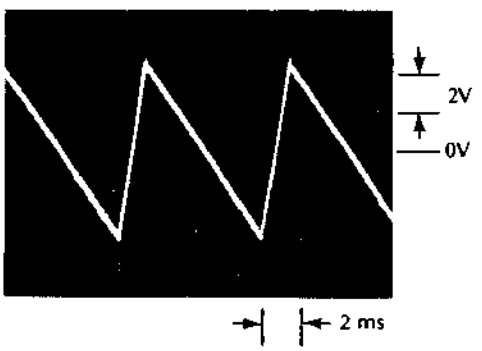
4. Remove ground on A6TP1.

b. Adjust A6R1, A6R2 (search sweep) as follows:

1. Remove the A7 Assembly from the 5343A.

2. Connect scope probe to A6TP1.

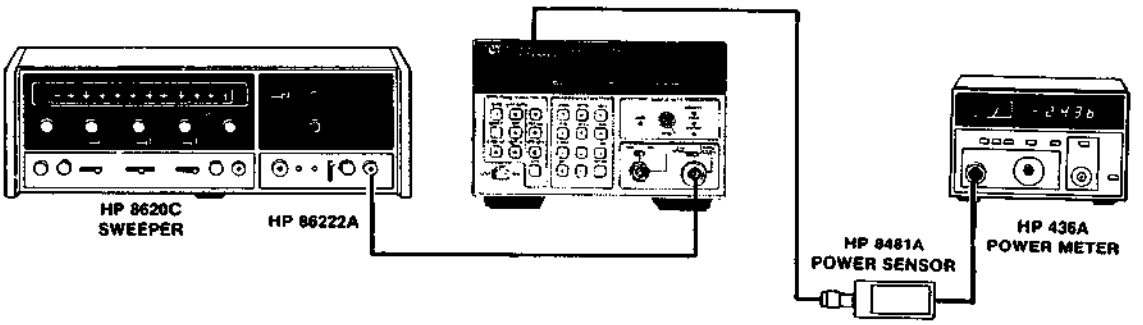
3. Adjust A6R1 and A6R2 to obtain an 8V peak-to-peak (±0.8V) triangular waveform, centered around 0V, as shown. When adjusted properly, the period will be 7.5 (±2) ms.



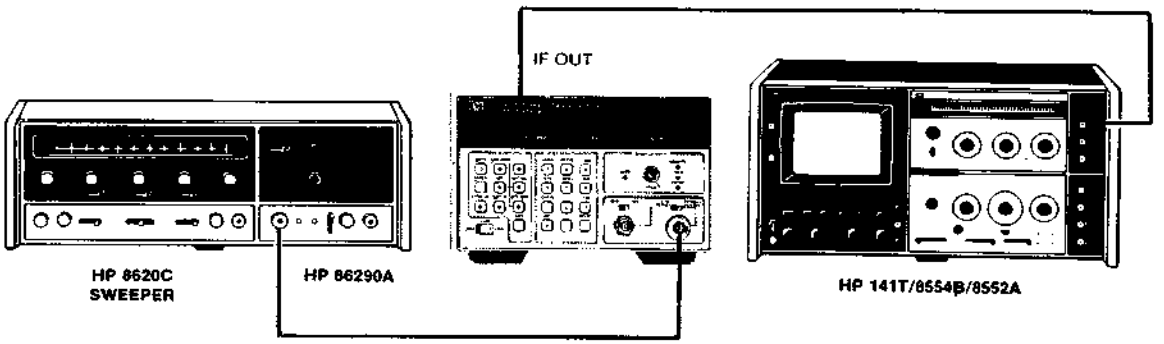
5-21. IF Adjustment

5-22. Adjust resistor A25A1R7 "BAL" by connecting the equipment as shown below and perform step a.

a. Set 8620C to 75 MHz at -15 dBm. While monitoring the rear panel IF OUT power with the 436A Power Meter, adjust A25A1R7 "BAL" for maximum signal level as read on the 436A.



5-23. Adjust capacitor A25A1C19 (175 MHz rolloff) by connecting the equipment as shown below and proceed:



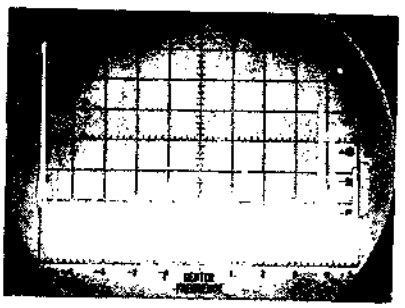
a. Set 5343A in AUTO mode, HOLD, and diagnostic mode 7 (SET, SET 7). Counter should display 350.5 MHz indicating that the MAIN VCO is at 350.5 MHz.

b. Transpose IF OUT INT and IF OUT EXT cables on A25A1 (cables connected to A25A1J3 and J4). This causes the IF output of A25A1 to be routed to the rear panel connector of the 5343A for ease in connecting the signal to the spectrum analyzer.

c. Set the spectrum analyzer for a center frequency of 100 MHz, 20 MHz/div., 300 kHz BW.

d. Adjust the frequency of the 86290A (level ~-15 dBm) for an IF around 10 MHz as seen on the spectrum analyzer. Now change the 86290A frequency such that the IF increases. As the IF approaches 175 MHz, the amplitude will roll off. The amplitude at 175 MHz must be adjusted to be 10 (±1) dB less than the amplitude at 50 MHz (amplitude is essentially flat from below 1 MHz out to 160 MHz).

e. To adjust 86290A so that the IF is precisely 175 MHz, increase the 86290A frequency until the IF produced by the Nth harmonic of the VCO mixing with the input is just equal in amplitude to the IF produced by the (N±1)th harmonic of the VCO mixing with the input. Since the VCO harmonics are spaced by 350 MHz, this only occurs when both IF's are equal to 175 MHz as seen in the following:

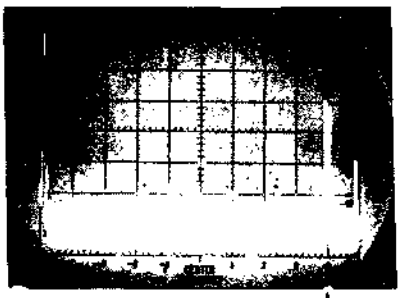


IF OUT
20 MHz/div.
100 MHz center freq.

1st line (closest to reference) is IF produced by Nth harmonic of VCO.

2nd line is IF produced by (N±1)th harmonic of VCO.

These are equal in amplitude at 175 MHz.



IF OUT
20 MHz/div.
100 MHz center freq.

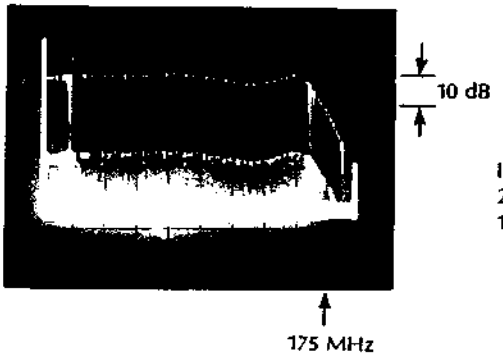
As 86290A frequency is changed, the two IF's both approach 175 MHz and become equal in amplitude.

Note this point on spectrum analyzer. The response at this point must be 10 (±1) dBm down.

NOTE

In the following step, needle-nose pliers can be used to adjust A25A1C19 in the casting in those cases where C11 is oriented the wrong way for using a tuning wand.

f. Sweep the 86290A over a narrow range so that the IF covers approximately 10 MHz to 200 MHz. Adjust A25A1C19 so that the response at 175 MHz is 10 (±1) dB down from flat part of response as shown:



IF OUT
20 MHz/div.
100 MHz center freq.

g. Return IF OUT INT and IF OUT EXT cables to original position.

5-24. Adjust resistor A11R1 ("Amp" Gain) as follows:

a. Apply 75 MHz at -20 dBm to the 500 MHz—26.5 GHz input of 5343A.

b. Monitor the IF LIM signal at XA11($\overline{12}$) with an RF voltmeter such as the 3406A or an HP 1740A oscilloscope. Adjust A11R1 for maximum output signal.

5-25. Adjust resistors A12R2, A12R13 (Gain) as follows:

a. Connect a 75 MHz, -50 dBm signal to the 500 MHz—26.5 GHz input to the 5343A.

b. Monitor the IF COUNT signal at XA12($\overline{8}$) with an RF voltmeter such as the 3406A (or an HP 1740A oscilloscope) and adjust A12R2, "B1", and A12R13, "B2", for maximum observed output as indicated by the voltmeter.

5-26. Adjust resistor A12R7 (Sensitivity) as follows:

a. Set 5343A to AUTO. Adjust A12R7 maximum ccw.

b. Apply a 1 GHz, -33 dBm signal to the 500 MHz—26.5 GHz input of the 5343A.

c. Set 5343A to MANUAL.

d. Measure the dc voltage at A12TP1 and record _____ .

e. Disconnect the 1 GHz signal from the 5343A input.

f. Measure the dc voltage at A12TP2 and adjust A12R7, "OFS", for same voltage as recorded in step d. within ±5 mV.

g. Set 5343A to AUTO.

h. Remove test leads and verify that counter counts 1 GHz at -33 dBm.

5-27. Direct Count Adjustment

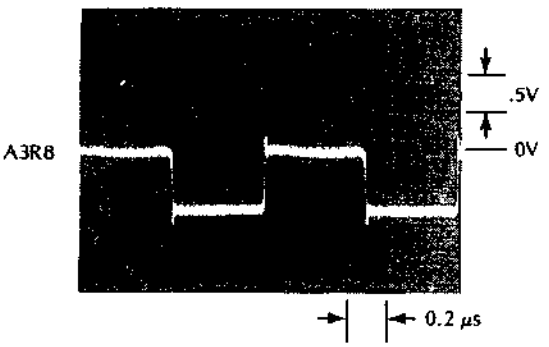
5-28. Adjust resistor A3R8 (Balance) as follows:

a. Set 5343A to 10 Hz—500 MHz range and 50Ω.

b. Apply a 1 MHz sine wave signal at a level of 25 mV rms.

c. Monitor A3TP1 (output of U5) on scope and adjust A3R8 for a 50% duty cycle.

d. Decrease input level further and adjust A3R8 for 50% duty cycle. Keep decreasing level and adjusting A3R8 to the point where the counter no longer counts.



5-29. Oscillator Adjustments

5-30. A24 Standard Oscillator. Adjust the standard oscillator as follows:

a. Connect the rear panel FREQ STD OUT of the 5343A to the input of a high resolution frequency counter (reciprocal taking) such as an HP 5345A. The 5345A should be referenced to an external frequency standard such as the HP 5061A Cesium Beam by connecting the external standard to the external oscillator input of the 5345A.

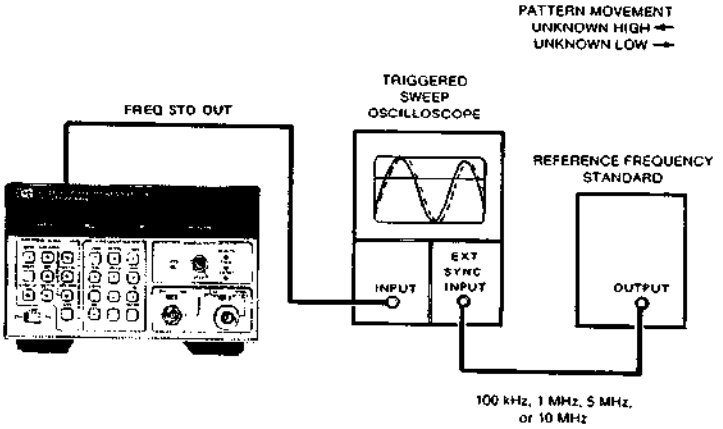
b. Remove the A24 oscillator and note the frequency offset marked on the label. If operation of the counter will be over the full temperature range, then the 10 MHz oscillator must be offset by the marked amount in order to keep the oscillator frequency within the manufacturer's temperature specification. For example, if +3.6 Hz is marked on the label, then the oscillator is adjusted for a frequency of 10.0000036 MHz at 25°C. If operation is solely at 25°C, then the offset can be ignored.

c. Reinstall A24 and adjust the oscillator for a 5345A display of the frequency determined in step b.

5-31. Option 001 Oven Oscillator (10544A). Adjust the optional oscillator as follows:

NOTE

Allow 24-hour warmup for oven before this adjustment.



a. Connect reference frequency standard to the external sync input of the oscilloscope.

b. Connect rear panel FREQ STD OUT of the 5343A to Channel A of the scope.

c. Adjust oscillator frequency for minimum sideways movement of the 10 MHz displayed signal.

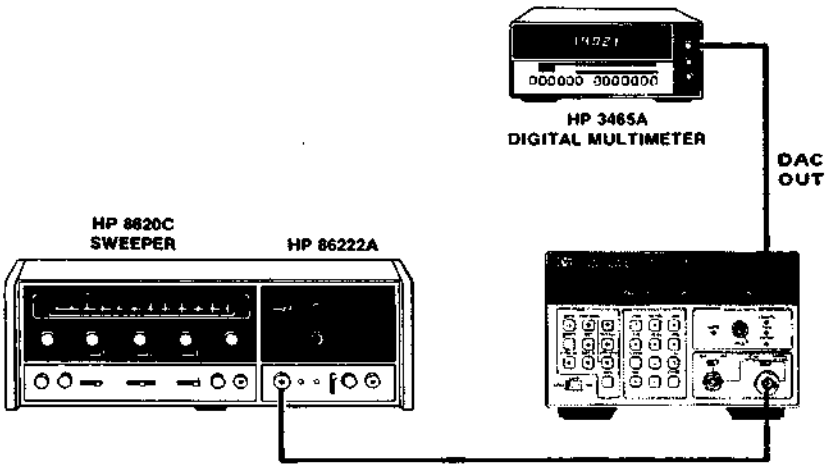
d. By timing the sideways movement (in CM per second), the approximate offset can be determined based on the oscilloscope sweep speed as shown in the following:

MOVEMENT	SWEEP SPEED			NOTES
	1 μs/cm	0.1 μs/cm	0.01 μs/cm	
1 cm/s	1×10^{-6}	1×10^{-7}	1×10^{-8}	TIME SCOPE TRACE MOVEMENT WITH SECOND HAND OF WATCH OR CLOCK
1 cm/10 s	1×10^{-7}	1×10^{-8}	1×10^{-9}	
1 cm/100 s	1×10^{-8}	1×10^{-9}	1×10^{-10}	

For example, if the trace moves 1 centimetre in 10 seconds and the sweep speed is 0.01 μs/cm, the oscillator signal is within 1×10^{-9} of the reference frequency.

5-32. OPTION 004 DIGITAL-TO-ANALOG (DAC) ADJUSTMENTS

5-33. Set up the equipment as shown below, and proceed:

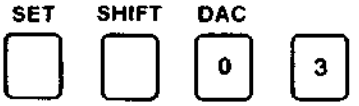


a. Set the 5343A to the 500 MHz—26.5 GHz range, AUTO mode.

b. Connect DVM to DAC OUT, set DVM to 20V range.

c. Set the generator to 999 MHz as indicated on 5343A display.

d. On 5343A keyboard, press:

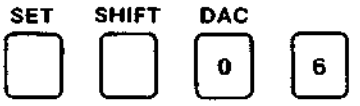


NOTE

The DAC variable resistor adjustments "OFFSET" (R26) and "GAIN ADJ" (R25) are located at the top rear of the A2 Display Driver Assembly. Remove the top cover of the 5343A to gain access to these adjustments located below the top of the front frame.

e. Adjust "GAIN ADJ" and observe DVM for indication of 9.99 volts, dc.

f. On 5343A keyboard, press:



g. Adjust "OFFSET" and observe DVM for Ø volts, dc.

h. Repeat steps d and f and observe DVM for proper indication. Readjust, if necessary.

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION

6-2. This section contains information for ordering parts. *Table 6-1* is a list of exchange assemblies, and *Table 6-2* lists abbreviations and reference designations used in the parts list and throughout the manual. *Table 6-3* lists all replaceable parts for the standard 5343A in reference designator order. *Tables 6-4, 6-5,* and 6-6, list replaceable parts for Options 001, 004, and 011, respectively. *Table 6-7* contains the names and addresses that correspond to the manufacturer's code numbers.

6-3. EXCHANGE ASSEMBLIES

6-4. *Table 6-1* lists assemblies within the instrument that may be replaced on an exchange basis. Exchange, factory repaired, and tested assemblies are available only on a trade-in basis; therefore, the defective assemblies must be returned for credit. For this reason, assemblies required for spare parts stock must be ordered by the new assembly part number.

Table 6-1. Exchange Assemblies

NAME	NEW HP PART NO.	EXCHANGE HP PART NO.
U1 Sampler	5088-7045	5088-7545
Option 001 Oven Oscillator	10544-60011	10544-60511

6-5. ABBREVIATIONS AND REFERENCE DESIGNATIONS

6-6. *Table 6-2* lists abbreviations and reference designations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviation are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lower case and upper case letters.

6-7. REPLACEABLE PARTS LIST

6-8. *Tables 6-3* through 6-6 are the lists of replaceable parts and are organized as follows:

a. Electrical assemblies and their components in alphanumerical order by reference designation.

b. Chassis-mounted parts in alphanumerical order by reference designation (*Table 6-3* only).

c. Miscellaneous parts.

6-9. The information given for each part consists of the following:

a. The Hewlett-Packard part number.

b. Part number check digit (CD).

c. The total quantity (Qty) in each assembly.

d. The description of the part.

e. A typical manufacturer of the part in a five-digit code.

f. The manufacturer's number for the part.

6-10. The total quantity for each assembly is given only once — at the first appearance of the part number in the list for that assembly (A1, A2, etc.).

Table 6-2. Abbreviations and Reference Designations

REFERENCE DESIGNATIONS

A	= assembly	DL	= delay line	K	= relay	T	= transformer
AT	= attenuator; isolator; termination	DS	= annunciator; signaling device (audible or visual); lamp; LED	L	= coil; inductor	TB	= terminal board
B	= fan; motor	E	= miscellaneous electrical part	M	= metre	TC	= thermocouple
BT	= battery	F	= fuse	MP	= miscellaneous mechanical part	TP	= test point
C	= capacitor	FL	= filter	P	= electrical connector (movable portion); plug	U	= integrated circuit; microcircuit
CP	= coupler	H	= hardware	Q	= transistor; SCR; triode thyristor	V	= electron tube
CR	= diode; diode thyristor; varactor	HY	= circulator	R	= resistor	VR	= voltage regulator; breakdown diode
DC	= directional coupler	J	= electrical connector (stationary portion); jack	RT	= thermistor	W	= cable; transmission path; wire
				S	= switch	X	= socket
						Y	= crystal unit-piezo-electric
						Z	= tuned cavity; tuned circuit

ABBREVIATIONS

A	= ampere	HD	= head	NE	= neon	SPST	= single-pole, single-throw
ac	= alternating current	HDW	= hardware	NEG	= negative	SSB	= single sideband
ACCESS	= accessory	HF	= high frequency	nF	= nanofarad	SST	= stainless steel
ADJ	= adjustment	HG	= mercury	NI PL	= nickel plate	STL	= steel
A/D	= analog-to-digital	HI	= high	N/O	= normally open	SQ	= square
AF	= audio frequency	HP	= Hewlett-Packard	NOM	= nominal	SWR	= standing-wave ratio
AFC	= automatic frequency control	HPF	= high pass filter	NORM	= normal	SYNC	= synchronize
AGC	= automatic gain control	HR	= hour (used in parts list)	NPN	= negative-positive-negative	T	= timed (slow-blow fuse)
AL	= aluminum	HV	= high voltage	NPO	= negative-positive zero (zero temperature coefficient)	TA	= tantalum
ALC	= automatic level control	Hz	= hertz	NRFR	= not recommended for field replacement	TC	= temperature compensating
AM	= amplitude modulation	IC	= integrated circuit	ns	= nanosecond	TD	= time delay
AMPL	= amplifier	ID	= inside diameter	NSR	= not separately replaceable	TERM	= terminal
APC	= automatic phase control	IF	= intermediate frequency	nW	= nanowatt	TFT	= thin-film transistor
ASSY	= assembly	IMPG	= impregnated	OBD	= order by description	TGL	= toggle
AUX	= auxiliary	in	= inch	OD	= outside diameter	THD	= thread
AVG	= average	INCD	= incandescent	OH	= oval head	THRU	= through
AWG	= american wire gauge	INCL	= include(s)	OP AMPL	= operational amplifier	TI	= titanium
BAL	= balance	INP	= input	OPT	= option	TOL	= tolerance
BCD	= binary coded decimal	INS	= insulation	OSC	= oscillator	TRIM	= trimmer
BD	= board	INT	= internal	OX	= oxide	TSTR	= transistor
BE CU	= beryllium copper	kg	= kilogram	oz	= ounce	TTL	= transistor-transistor logic
BFO	= beat frequency oscillator	kHz	= kilohertz	Ω	= ohm	TV	= television
BH	= binder head	kΩ	= kilohm	P	= peak (used in parts list)	TVI	= television interference
BKDN	= breakdown	kV	= kilovolt	PAM	= pulse-amplitude modulation	TWT	= traveling wave tube
BP	= bandpass	lb	= pound	PC	= printed circuit	U	= micro (10-6) used in parts list)
BPF	= bandpass filter	LC	= inductance-capacitance	PCM	= pulse-code modulation; pulse-count modulation	UF	= microfarad (used in parts list)
BRS	= brass	LED	= light-emitting diode	PDM	= pulse-duration modulation	UHF	= ultrahigh frequency
BWO	= backward-wave oscillator	LF	= low frequency	pF	= picofarad	UNREG	= unregulated
CAL	= calibrate	LG	= long	PH BRZ	= phosphor bronze	V	= volt
ccw	= counterclockwise	LH	= left hand	PHL	= phillips	VA	= voltampere
CER	= ceramic	LIM	= limit	PIN	= positive-intrinsic-negative	Vac	= volts ac
CHAN	= channel	LIN	= linear taper (used in parts list)	PIV	= peak inverse voltage	VAR	= variable
cm	= centimeter	lin	= linear	pk	= peak	VCO	= voltage-controlled oscillator
CMO	= coaxial	LK WASH	= lockwasher	PL	= phase lock	Vdc	= volts dc
COEF	= coefficient	LO	= low; local oscillator	PLO	= phase lock oscillator	VDCW	= volts, dc, working (used in parts list)
COM	= common	LOG	= logarithmic taper (used in parts list)	PM	= phase modulation	V(F)	= volts, filtered
COMP	= composition	log	= logarithm(ic)	PNP	= positive-negative-positive	VFO	= variable-frequency oscillator
COMPL	= complete	LPF	= low pass filter	P/O	= part of	VHF	= very-high frequency
CONN	= connector	LV	= low voltage	POLY	= polystyrene	Vpk	= volts peak
CP	= cadmium plate	m	= metre (distance)	PORC	= porcelain	Vp-p	= volts peak-to-peak
CRT	= cathode-ray tube	mA	= milliampere	POS	= positive; position(s) (used in parts list)	Vrms	= volts rms
CTL	= complementary transistor logic	MAX	= maximum	POSN	= position	VSWR	= voltage standing wave ratio
CW	= continuous wave	MΩ	= megohm	POT	= potentiometer	VTO	= voltage-tuned oscillator
cw	= clockwise	MEG	= meg (10⁶) (used in parts list)	p-p	= peak-to-peak	VTVM	= vacuum-tube voltmeter
D/A	= digital-to-analog	MET FLM	= metal film	PP	= peak-to-peak (used in parts list)	V(X)	= volts, switched
dB	= decibel	MET OX	= metal oxide	PPM	= pulse-position modulation	W	= watt
dBm	= decibel referred to 1 mW	MF	= medium frequency; microfarad (used in parts list)	PREAMPL	= preamplifier	W/	= with
dc	= direct current	MFR	= manufacturer	PRF	= pulse-repetition frequency	WIV	= working inverse voltage
deg	= degree (temperature interval or difference)	mg	= milligram	PRR	= pulse repetition rate	WW	= wirewound
... °	= degree (plane angle)	MHz	= megahertz	ps	= picosecond	W/O	= without
°C	= degree Celsius (centrigrade)	mH	= millihenry	PT	= point	YIG	= yttrium-iron-garnet
°F	= degree Fahrenheit	mho	= conductance	PTM	= pulse-time modulation	Zo	= characteristic impedance
°K	= degree Kelvin	MIN	= minimum	PWM	= pulse-width modulation		
DEPC	= deposited carbon	min '	= minute (time) = minute (plane angle)	PWV	= peak working voltage		
DET	= detector	MINAT	= miniature	RC	= resistance capacitance		
diam	= diameter	mm	= millimetre	RECT	= rectifier		
DIA	= diameter (used in parts list)	MOD	= modulator	REF	= reference		
DIFF AMPL	= differential amplifier	MOM	= momentary	REG	= regulated		
div	= division	MOS	= metal-oxide semiconductor	REPL	= replaceable		
DPDT	= double-pole, double-throw	ms	= millisecond	RF	= radio frequency		
DR	= drive	MTG	= mounting	RFI	= radio frequency interference		
DSB	= double sideband	MTR	= meter (indicating device)	RH	= round head; right hand		
DTL	= diode transistor logic	mV	= millivolt	RLC	= resistance-inductance-capacitance		
DVM	= digital voltmeter	mVac	= millivolt, ac	RMO	= rack mount only		
ECL	= emitter coupled logic	mVdc	= millivolt, dc	rms	= root-mean-square		
EMF	= electromotive force	mVpk	= millivolt, peak	RND	= round		
EDP	= electronic data processing	mVp-p	= millivolt, peak-to-peak	ROM	= read-only memory		
ELECT	= electrolytic	mVrms	= millivolt, rms	R&P	= rack and panel		
ENCAP	= encapsulated	mW	= milliwatt	RWV	= reverse working voltage		
EXT	= external	MUX	= multiplex	S	= scattering parameter		
F	= farad	MY	= mylar	s	= second (time)		
FET	= field-effect transistor	μA	= microampere	... "	= second (plane angle)		
F/F	= flip-flop	μF	= microfarad	S-B	= slow-blow fuse (used in parts list)		
FH	= flat head	μH	= microhenry	SCR	= silicon controlled rectifier; screw		
FIL H	= fillister head	μmho	= micromho	SE	= selenium		
FM	= frequency modulation	μs	= microsecond	SECT	= sections		
FP	= front panel	μV	= microvolt	SEMICON	= semiconductor		
FREQ	= frequency	μVac	= microvolt, ac	SHF	= superhigh frequency		
FXD	= fixed	μVdc	= microvolt, dc	SI	= silicon		
g	= gram	μVpk	= microvolt, peak	SIL	= silver		
GE	= germanium	μVp-p	= microvolt, peak-to-peak	SL	= slide		
GHz	= gigahertz	μVrms	= microvolt, rms	SNR	= signal-to-noise ratio		
GL	= glass	μW	= microwatt	SPDT	= single-pole, double-throw		
GND	= ground(ed)	nA	= nanoampere	SPG	= spring		
H	= henry	NC	= no connection	SR	= split ring		
h	= hour	N/C	= normally closed				
HET	= heterodyne						
HEX	= hexagonal						

NOTE

All abbreviations in the parts list will be in upper case.

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

6-11. ORDERING INFORMATION

6-12. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number, the check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your order.

6-13. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Office.

6-14. DIRECT MAIL ORDER SYSTEM

6-15. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices — to provide these advantages, a check or money order must accompany each order.

6-16. Mail order forms and specific ordering information is available through your HP office. Addresses and phone numbers are located at the back of this manual.

6-17. OPTION RETROFIT KITS

6-18. To order a retrofit kit for field installation of Options 001, 004, or 011 refer to paragraph 2-25 for the part number of the option kit.

6-19. INPUT CONNECTOR A1J2 AND FUSE F2

6-20. Input connector A1J2 is a special connector designed to house fuse F2 as shown in *Figure 6-1.*

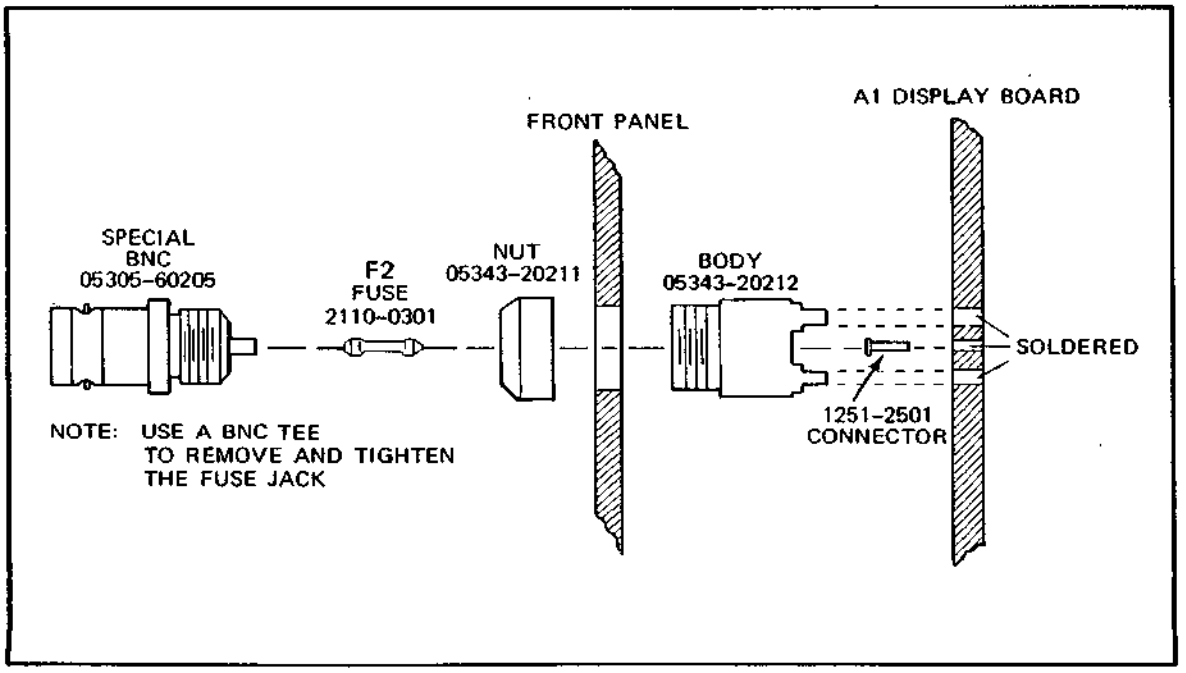


Figure 6-1. Details of Input Connector A1J2 and Fuse F2 Mounting

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	05343-60004	0	1	KEYBOARD DISPLAY (SERIES 1932)	28480	05343-60004
A1C1	0160-4256	6	1	CAPACITOR-FXD .047UF +-20% 200VDC CER	16546	CW30 B 473M
A1C2	0160-3879	7	1	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1DS1	1990-0670	0	8	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0670
A1DS2	1990-0670	0		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0670
A1DS3	1990-0670	0		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0670
A1DS4	1990-0670	0		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0670
A1DS5	1990-0670	0		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0670
A1DS6	1990-0670	0		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0670
A1DS7	1990-0670	0		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0670
A1DS8	1990-0670	0		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0670
A1DS9				NOT ASSIGNED		
A1DS10	1990-0517	4		LED-VISIBLE LUM-INT=3MCD IF=20MA-MAX	28480	5082-4655
A1DS11	1990-0540	3	11	DISPLAY-NUM-SEG 1=CHAR .43-H	28480	5082-7650
A1DS12	1990-0540	3		DISPLAY-NUM-SEG 1=CHAR .43-H	28480	5082-7650
A1DS13	1990-0540	3		DISPLAY-NUM-SEG 1=CHAR .43-H	28480	5082-7650
A1DS14	1990-0540	3		DISPLAY-NUM-SEG 1=CHAR .43-H	28480	5082-7650
A1DS15	1990-0540	3		DISPLAY-NUM-SEG 1=CHAR .43-H	28480	5082-7650
A1DS16	1990-0540	3		DISPLAY-NUM-SEG 1=CHAR .43-H	28480	5082-7650
A1DS17	1990-0540	3		DISPLAY-NUM-SEG 1=CHAR .43-H	28480	5082-7650
A1DS18	1990-0540	3		DISPLAY-NUM-SEG 1=CHAR .43-H	28480	5082-7650
A1DS19	1990-0540	3		DISPLAY-NUM-SEG 1=CHAR .43-H	28480	5082-7650
A1DS20	1990-0540	3		DISPLAY-NUM-SEG 1=CHAR .43-H	28480	5082-7650
A1DS21	1990-0540	3		DISPLAY-NUM-SEG 1=CHAR .43-H	28480	5082-7650
A1DS22	1990-0517	4		LED-VISIBLE LUM-INT=3MCD IF=20MA-MAX	28480	5082-4655
A1DS23	1990-0517	4		LED-VISIBLE LUM-INT=3MCD IF=20MA-MAX	28480	5082-4655
A1DS24	1990-0517	4		LED-VISIBLE LUM-INT=3MCD IF=20MA-MAX	28480	5082-4655
A1DS25	1990-0517	4		LED-VISIBLE LUM-INT=3MCD IF=20MA-MAX	28480	5082-4655
A1DS26	1990-0517	4		LED-VISIBLE LUM-INT=3MCD IF=20MA-MAX	28480	5082-4655
A1DS27	1990-0517	4		LED-VISIBLE LUM-INT=3MCD IF=20MA-MAX	28480	5082-4655
A1DS28	1990-0517	4	8	LED-VISIBLE LUM-INT=3MCD IF=20MA-MAX	28480	5082-4655
A1J1	1250-0257	1	2	CONNECTOR-RF SMB M PC 50-OHM	28480	1250-0257
A1J2	05343-20212	8	1	BODY-BNC	28480	05343-20212
A1J3	1250-0257	1		CONNECTOR-RF SMB M PC 50-OHM	28480	1250-0257
A1J4	1251-2501	4	1	CONNECTOR-SGL CONT SKT .022-IN-BSC-BZ	28480	1251-2501
A1Q1	1853-0318	3	13	TRANSISTOR PNP SI PD=500MW FT=60MHZ	04713	MPS6562
A1Q2	1853-0318	3		TRANSISTOR PNP SI PD=500MW FT=60MHZ	04713	MPS6562
A1Q3	1853-0318	3		TRANSISTOR PNP SI PD=500MW FT=60MHZ	04713	MPS6562
A1Q4	1853-0318	3		TRANSISTOR PNP SI PD=500MW FT=60MHZ	04713	MPS6562
A1Q5	1853-0318	3		TRANSISTOR PNP SI PD=500MW FT=60MHZ	04713	MPS6562
A1Q6	1853-0318	3		TRANSISTOR PNP SI PD=500MW FT=60MHZ	04713	MPS6562
A1Q7	1853-0318	3		TRANSISTOR PNP SI PD=500MW FT=60MHZ	04713	MPS6562
A1Q8	1853-0318	3		TRANSISTOR PNP SI PD=500MW FT=60MHZ	04713	MPS6562
A1Q9	1853-0318	3		TRANSISTOR PNP SI PD=500MW FT=60MHZ	04713	MPS6562
A1Q10	1853-0318	3		TRANSISTOR PNP SI PD=500MW FT=60MHZ	04713	MPS6562
A1Q11	1853-0318	3		TRANSISTOR PNP SI PD=500MW FT=60MHZ	04713	MPS6562
A1Q12	1853-0318	3		TRANSISTOR PNP SI PD=500MW FT=60MHZ	04713	MPS6562
A1Q13	1853-0318	3		TRANSISTOR PNP SI PD=500MW FT=60MHZ	04713	MPS6562
A1R1	0698-5075	8	13	RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A1R2	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A1R3	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A1R4	1810-0080	6	2	NETWORK-RES 8-SIP500.0 OHM X 7	28480	1810-0080
A1R5	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A1R6	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A1R7	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A1R8	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A1R9	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A1R10	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A1R11	1810-0080	6		NETWORK-RES 8-SIP500.0 OHM X 7	28480	1810-0080
A1R12	0698-8354	2	1	RESISTOR 270 5% .125W CC TC=-330/+800	01121	BB2715
A1R13	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A1R14	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A1R15	0698-1021	8	1	RESISTOR 1K 10% .125W CC TC=-330/+800	01121	BB1021
A1R16	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A1R17	0698-3381	5	1	RESISTOR 150 5% .125W CC TC=-330/+800	01121	BB1515
A1R18	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A1S1	3101-2220	9	2	SWITCH-SLIDE	28480	3101-2220
A1S2	3101-2220	9		SWITCH-SLIDE	28480	3101-2220

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				A1 MISCELLANEOUS PARTS		
	0624-0097	9	2	SCREW-TPG 4-40 .188-IN-LG PAN-MD-POZI	28480	0624-0097
	1251-0600	0	2	CONNECTOR-SGL CONT PIN 1.18-MM-BSC-BZ SG	28480	1251-0600
	5041-0276	5	2	KEY CAP-PEARL GRAY	28480	5041-0276
	5041-0285	6	2	KEY CAP-PEARL GLP	28480	5041-0285
	5041-0318	6	5	KEY CAP-PUT GLP	28480	5041-0318
	5041-0342	6	1	KEY CAP-SG QUARTER	28480	5041-0342
	5041-0450	7	1	KEY CAP-BLUE, QUARTER	28480	5041-0450
	5041-0784	0	1	KEY CAP-#5	28480	5041-0784
	5041-0785	1	2	KEY CAP-6 OR 9	28480	5041-0785
	5041-0786	2	1	KEY CAP-#7	28480	5041-0786
	5041-0787	3	1	KEY CAP-#8	28480	5041-0787
	5041-0788	4	1	KEY CAP-#0	28480	5041-0788
	5041-0789	5	1	KEY CAP-#.	28480	5041-0789
	5041-0802	3	1	KEY CAP-#1	28480	5041-0802
	5041-0803	4	1	KEY CAP-#2	28480	5041-0803
	5041-0804	5	1	KEY CAP-#3	28480	5041-0804
	5041-0805	6	1	KEY CAP-#4	28480	5041-0805
	05342-00014	5	1	SHIELD-INPUT	28480	05342-00014
	05342-20104	6	1	BLOCK-ANNUNCIATOR	28480	05342-20104

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	05343-60005	1	1	DISPLAY DRIVER (SERIES 1932)	28480	05343-60005
A2C1	0180-0106	9	1	CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X0006B2
A2C2	0180-0230	0	2	CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A2C3	0160-3879	7	11	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C5	0180-1743	2	1	CAPACITOR-FXD .1UF+-10% 35VDC TA	56289	150D104X9035A2
A2C6	0160-3878	6	2	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A2C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C9	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C10	0160-0570	9	1	CAPACITOR-FXD 220PF +-20% 100VDC CER	20932	5024EM100RD221M
A2C11	0160-0571	0	1	CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A2C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C13	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C14	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C15	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C16	0180-1714	7	1	CAPACITOR-FXD 330UF+-10% 6VDC TA	56289	150D337X9006B2
A2C17	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C18	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C19	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A2C20	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A2J1	1200-0565	9	1	SOCKET-IC 24-CONT DIP-SLDR	28480	1200-0565
A2Q1	1854-0560	9	1	TRANSISTOR NPN SI DARL PD=310MW	04713	MPS A12
A2R1	0757-0420	3	1	RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A2R2	2100-3607	5	1	RESISTOR-VAR CONTROL CCP 1M 10% LIN (NOT SUPPLIED WITH A2 BOARD, MUST BE ORDERED SEPARATELY)	01121	HP4N102P105UZ
A2R3	0683-4725	2	9	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R4	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R5	1810-0279	5	2	NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
A2R6	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A2R7	0698-3430	5	8	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R8	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R9	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R10	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R11	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R12	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R13	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R14	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R15	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R16	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
A2R17	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R18	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R19	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A2R20	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R22	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R23	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R24	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R27	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R34	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A2TP1	1251-0600	0	5	CONNECTOR-SGL CONT PIN 1.14-MM-SSC-SZ SQ	28480	1251-0600
A2TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-SSC-SZ SQ	28480	1251-0600
A2TP4	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-SSC-SZ SQ	28480	1251-0600
A2TP5	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-SSC-SZ SQ	28480	1251-0600
A2TP6	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-SSC-SZ SQ	28480	1251-0600
A2U1	1820-0539	1	2	IC BFR TTL NAND QUAD 2-INP	01295	SN7437N
A2U2	1820-0468	5	2	IC DCDR TTL BCD-TO-DEC 4-TO-10-LINE	01295	SN7445N
A2U3	1820-1443	A	1	IC CNTR TTL LS BIN ASYNCHRO	01295	SN74LS293N
A2U4	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A2U5	1820-1049	0	1	IC BFR TTL NON-INV HEX	01295	SN74367N
A2U6	1820-0539	1		IC BFR TTL NAND QUAD 2-INP	01295	SN7437N
A2U7	1820-0628	9	2	IC TTL 64-BIT RAM 60-NS 0-C	01295	SN7489N
A2U8	1820-0468	5		IC DCDR TTL BCD-TO-DEC 4-TO-10-LINE	01295	SN7445N
A2U9	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A2U10	1820-1200	5	1	IC INV TTL LS HEX	01295	SN74LS05N
A2U11	1820-0515	3	1	IC MV TTL MONOSTBL RETRIG/RESET DUAL	04713	MC8602P
A2U12	1820-0628	9		IC TTL 64-BIT RAM 60-NS 0-C	01295	SN7489N
A2U13	1820-1254	9	2	IC BFR TTL NON-INV HEX 1-INP	27014	DM8095N
A2U14	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A2U17	1820-1254	9		IC BFR TTL NON-INV HEX 1-INP	27014	DM8095N

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2U18	1820-1428	9	1	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
A2U19	1820-1112	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A2U20	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A2U23	1820-1885	2	1	IC RGTR TTL LS D-TYPE QUAD	27014	DM74LS173N
A2W1	8159-0005	0	1	WIRE 22AWG W PVC 1X22 80C	28480	8159-0005
				A2 MISCELLANEOUS PARTS		
	0380-0336	1	4	SPACER-RVT-ON .312-IN-LG .152-IN-ID	00000	ORDER BY DESCRIPTION

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3R21	0698-6242	3	5	RESISTOR 1.2K 5% .125W CC TC=-350/+857	01121	BB1225
A3R22	0698-6294	5		RESISTOR 47K 5% .125W CC TC=-486/+875	01121	BB4735
A3R23	0698-5183	9	1	RESISTOR 4.3K 5% .125W CC TC=0+882	01121	BB4325
A3R24	0698-6242	3		RESISTOR 1.2K 5% .125W CC TC=-350/+857	01121	BB1225
A3R25	0698-5179	3	1	RESISTOR 1.6K 5% .125W CC TC=-350/+857	01121	BB1625
A3R26	0698-3374	6	1	RESISTOR 20 5% .125W CC TC=+270/+540	01121	BB2005
A3R27	0698-6242	3		RESISTOR 1.2K 5% .125W CC TC=-350/+857	01121	BB1225
A3R28	0698-6241	2	3	RESISTOR 750 5% .125W CC TC=-330/+800	01121	BB7515
A3R29	0698-5176	0		RESISTOR 510 5% .125W CC TC=-330/+800	01121	BB5115
A3R30	0698-8373	5		RESISTOR 470K 5% .125W CC TC=-600/+1137	01121	BB4745
A3R31	0757-0316	6		RESISTOR 42.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-42R2-F
A3R32	0698-7080	9	2	RESISTOR 27 5% .125W CC TC=+270/+540	01121	BB2705
A3R33	0757-0276	7	1	RESISTOR 61.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-6192-F
A3R34	0698-5174	8	2	RESISTOR 200 5% .125W CC TC=-330/+800	01121	BB2015
A3R35	0698-6242	3		RESISTOR 1.2K 5% .125W CC TC=-350/+857	01121	BB1225
A3R36	0698-5176	0		RESISTOR 510 5% .125W CC TC=-330/+800	01121	BB5115
A3R37	0698-6241	2		RESISTOR 750 5% .125W CC TC=-330/+800	01121	BB7515
A3R38	0698-6241	2		RESISTOR 750 5% .125W CC TC=-330/+800	01121	BB7515
A3R39	0698-7080	9		RESISTOR 27 5% .125W CC TC=+270/+540	01121	BB2705
A3R40	0757-0316	6		RESISTOR 42.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-42R2-F
A3R41	0698-8354	2	1	RESISTOR 270 5% .125W CC TC=-330/+800	01121	BB2715
A3R42	0698-1021	8	2	RESISTOR 1K 10% .125W CC TC=-330/+800	01121	BB1021
A3R43	0698-1021	8		RESISTOR 1K 10% .125W CC TC=-330/+800	01121	BB1021
A3R44	0698-6242	3		RESISTOR 1.2K 5% .125W CC TC=-350/+857	01121	BB1225
A3R45	0683-5605	9	1	RESISTOR 56 5% .25W FC TC=-400/+500	01121	CB5605
A3R46	0698-5180	6		RESISTOR 2K 5% .125W CC TC=-350/+857	01121	BB2025
A3R47	0698-5174	8		RESISTOR 200 5% .125W CC TC=-330/+800	01121	BB2015
A3R48	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A3TP1	1251-0600	0	3	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A3TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A3TP3	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A3U1	1820-0736	0	2	IC CNTR ECL BIN DUAL	28480	1820-0736
A3U2	1820-1224	3	1	IC RCVR ECL LINE RCVR TPL 2-INP	04713	MC10216P
A3U3	1A26-0139	9	1	IC 1458 OP AMP 8-DIP-P	01928	CA1458G
A3U4	1820-0736	0		IC CNTR ECL BIN DUAL	28480	1820-0736
A3U5	1820-0982	8	3	IC DIFF AMPL 16-DIP-C	28480	1820-0982
A3U6	1820-0982	8		IC DIFF AMPL 16-DIP-C	28480	1820-0982
A3U7	1820-0982	8		IC DIFF AMPL 16-DIP-C	28480	1A26-0982
				A3 MISCELLANEOUS PARTS		
	0380-0970	9	1	STANDOFF-HEX .375-IN-LG 6-40THD	28480	0380-0970
	1251-3205	7	2	CONNECTOR-SGL CONT SKT .022-IN-BSC-SZ	28480	1251-3205
	3050-0105	6	2	WASHER-FL MTLC NO. 8 .125-IN-ID	28480	3050-0105
	05342-20101	3	1	SCREW, GROUND	28480	05342-20101

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8	05342-60004	9	1	OFFSET VCO ASSEMBLY (SERIES 1720)	28480	05342-60004
A8C1	0180-0210	6	1	CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A8C2	0180-1701	2	4	CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A8C3	0180-1701	2		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A8C4	0160-3878	6	15	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C5	0180-1701	2		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A8C6	0180-1701	2		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A8C7	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C8	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C9	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C10	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C11	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C12	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C13	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C14	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C15	0180-0228	6	1	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A8C16	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C17	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C18	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C19	0160-3877	5	3	CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A8C20	0160-3877	5		CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A8C21	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C22	0160-3872	0	1	CAPACITOR-FXD 2.2PF +-.25PF 200VDC CER	28480	0160-3872
A8C23	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C24	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C25	0160-3877	5		CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A8CR1	1902-3171	7	1	DIODE-ZNR 11V 5% DO-7 PD=.4W TC=+.062%	28480	1902-3171
A8CR2	0122-0065	7	2	CAPACITOR;VOLTAGE VAR;29 PF/-3V	28480	0122-0065
A8CR3	0122-0065	7		CAPACITOR;VOLTAGE VAR;29 PF/-3V	28480	0122-0065
A8E1	9170-0016	8	1	CORE-SHIELDING BEAD	28480	9170-0016
A8L1	9100-2268	9	7	COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L2	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L3	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L4	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L5	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L6	9100-2247	8	2	COIL-MLD 100NH 10% Q=34 .095DX.25LG-NOM	28480	9100-2247
A8L7	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L8	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L9	9100-2247	8		COIL-MLD 100NH 10% Q=34 .095DX.25LG-NOM	28480	9100-2247
A8Q1	1854-0071	7	1	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A8Q2	1854-0345	8	1	TRANSISTOR NPN 2N5179 SI TO-72 PD=200MW	04713	2N5179
A8R1	2100-2489	9	1	RESISTOR-TRMR 5K 10% C SIDE-ADJ 1-TRN	30983	ET50X502
A8R2	0698-3380	4	1	RESISTOR 75 5% .125W CC TC=-270/+540	01121	BB7505
A8R3	0698-5426	3	1	RESISTOR 10K 10% .125W CC TC=-350/+857	01121	BB1031
A8R4	0698-5178	2	1	RESISTOR 1.5K 5% .125W CC TC=-350/+857	01121	BB1525
A8R5	0698-5174	8	1	RESISTOR 200 5% .125W CC TC=-330/+800	01121	BB2015
A8R6	0698-5999	5	3	RESISTOR 4.7K 5% .125W CC TC=-350/+857	01121	BB4725
A8R7	0698-5999	5		RESISTOR 4.7K 5% .125W CC TC=-350/+857	01121	BB4725
A8R8	0698-5172	6	2	RESISTOR 13 5% .125W CC TC=-270/+540	01121	BB1305
A8R9	0698-5999	5		RESISTOR 4.7K 5% .125W CC TC=-350/+857	01121	BB4725
A8R10	0698-5075	8	2	RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A8R11	0698-3376	8	2	RESISTOR 43 5% .125W CC TC=-270/+540	01121	BB4305
A8R12	0698-3378	0	2	RESISTOR 51 5% .125W CC TC=-270/+540	01121	BB5105
A8R13	0698-7212	9	1	RESISTOR 100 1% .05W F TC=0+-100	24546	C3-1/8-T0-100R-G
A8R14	0698-3376	8		RESISTOR 43 5% .125W CC TC=-270/+540	01121	BB4305
A8R15	0698-5172	6		RESISTOR 13 5% .125W CC TC=-270/+540	01121	BB1305
A8R16	0698-5996	2	1	RESISTOR 560 5% .125W CC TC=-330/+800	01121	BB5615
A8R17	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A8R18	0698-3378	0		RESISTOR 51 5% .125W CC TC=-270/+540	01121	BB5105
A8U1	1826-0372	2	2	IC 5 GHZ LIMITER/AMP	28480	1826-0372
A8U2	1826-0372	2		IC 5 GHZ LIMITER/AMP	28480	1826-0372
				A8 MISCELLANEOUS PARTS		
	0363-0133	0	2	CONTACT-FINGER .13-WD .09-FREE-HGT BE-CU	28480	0363-0133
	0380-0970	9	1	STANDOFF-HEX .375-IN-LG 4-40THD	28480	0380-0970
	05342-20101	3	1	SCREW, GROUND	28480	05342-20101

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5	05342-60005	0	1	RF MULTIPLEXER ASSEMBLY (SERIES 1720)	28480	05342-60005
A5C1	0160-3878	6	10	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C2	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C3	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C4	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C5	0160-0210	6	2	CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A5C6	0160-3029	9	2	CAPACITOR-FXD 7.5PF +-.5PF 100VDC CER	28480	0160-3029
A5C7	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C8	0160-3876	4	2	CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A5C9	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C10	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C11	0160-3879	7	4	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C12	0160-0576	5	3	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A5C13	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A5C14	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A5C15	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C16	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C17	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C18	0160-0210	6		CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A5C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C20	0160-3029	9		CAPACITOR-FXD 7.5PF +-.5PF 100VDC CER	28480	0160-3029
A5C21	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C22	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C23	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C24	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A5C25	0160-3875	3	2	CAPACITOR-FXD 22PF +-5% 200VDC CER 0+-30	28480	0160-3875
A5C26	0160-3875	3		CAPACITOR-FXD 22PF +-5% 200VDC CER 0+-30	28480	0160-3875
A5C27	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C28	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C29	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5CR1	1901-0179	7	6	DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A5CR2	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A5CR3	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A5CR4	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A5CR5	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A5CR6	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A5E1	9170-0029	3	2	CORE-SHIELDING BEAD	28480	9170-0029
A5E2	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A5L1	9100-2265	6	2	COIL-MLD 10UH 10% Q=60 .095DX.25LG-NOM	28480	9100-2265
A5L2	9100-2255	4	10	COIL-MLD 470NH 10% Q=35 .095DX.25LG-NOM	28480	9100-2255
A5L3	9100-2255	4		COIL-MLD 470NH 10% Q=35 .095DX.25LG-NOM	28480	9100-2255
A5L5	9100-2255	4		COIL-MLD 470NH 10% Q=35 .095DX.25LG-NOM	28480	9100-2255
A5L6	9100-2255	4		COIL-MLD 470NH 10% Q=35 .095DX.25LG-NOM	28480	9100-2255
A5L7	9100-2248	5	1	COIL-MLD 120NH 10% Q=34 .095DX.25LG-NOM	28480	9100-2248
A5L8	9100-2255	4		COIL-MLD 470NH 10% Q=35 .095DX.25LG-NOM	28480	9100-2255
A5L10	9100-2269	0	2	COIL-MLD 27UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2269
A5L11	9100-2269	0		COIL-MLD 27UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2269
A5L12	9100-2255	4		COIL-MLD 470NH 10% Q=35 .095DX.25LG-NOM	28480	9100-2255
A5L13	9100-2255	4		COIL-MLD 470NH 10% Q=35 .095DX.25LG-NOM	28480	9100-2255
A5L14	9100-2255	4		COIL-MLD 470NH 10% Q=35 .095DX.25LG-NOM	28480	9100-2255
A5L15	9100-2255	4		COIL-MLD 470NH 10% Q=35 .095DX.25LG-NOM	28480	9100-2255
A5L16	9100-2265	6		COIL-MLD 10UH 10% Q=60 .095DX.25LG-NOM	28480	9100-2265
A5L17	9100-2255	4		COIL-MLD 470NH 10% Q=35 .095DX.25LG-NOM	28480	9100-2255
A5L18	05342-80001	8	1	COIL, 5-TURNS	28480	05342-80001
A5Q1	1853-0058	8	3	TRANSISTOR PNP SI PD=300MW FT=200MHZ	07263	S32248
A5Q2	1853-0058	8		TRANSISTOR PNP SI PD=300MW FT=200MHZ	07263	S32248
A5Q3	1853-0058	8		TRANSISTOR PNP SI PD=300MW FT=200MHZ	07263	S32248
A5R1	0683-1215	9	1	RESISTOR 120 5% .25W FC TC=-400/+600	01121	CB1215
A5R2	0683-2005	7	1	RESISTOR 20 5% .25W FC TC=-400/+500	01121	CB2005
A5R3	0698-3113	1	4	RESISTOR 100 5% .125W CC TC=-270/+540	01121	BB1015
A5R4	0698-5172	6	1	RESISTOR 13 5% .125W CC TC=-270/+540	01121	BB1305
A5R5	0698-3378	0	2	RESISTOR 51 5% .125W CC TC=-270/+540	01121	BB5105
A5R6	0698-3111	9	4	RESISTOR 30 5% .125W CC TC=-270/+540	01121	BB3005
A5R7	0698-3111	9		RESISTOR 30 5% .125W CC TC=-270/+540	01121	BB3005
A5R8	0698-5170	8	2	RESISTOR 200 5% .125W CC TC=-330/+800	01121	BB2015
A5R9	0698-3380	4	2	RESISTOR 75 5% .125W CC TC=-270/+540	01121	BB7505
A5R10	0698-3113	1		RESISTOR 100 5% .125W CC TC=-270/+540	01121	BB1015
A5R11	0698-5561	7	2	RESISTOR 6.8 5% .125W CC TC=-120/+400	01121	BB6805
A5R12	0698-5998	4	1	RESISTOR 15 5% .125W CC TC=-270/+540	01121	BB1505
A5R13	0698-5564	0	1	RESISTOR 240 5% .125W CC TC=-330/+800	01121	BB2415
A5R14	0757-0398	4	1	RESISTOR 75 1% .125W F TC=0+-100	24546	C4-1/8-T0-75R0-F
A5R15	0698-5561	7		RESISTOR 6.8 5% .125W CC TC=-120/+400	01121	BB6805

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5R16	0698-3113	1		RESISTOR 100 5% .125W CC TC=-270/+540	01121	BB1015
A5R17	0698-6241	2	2	RESISTOR 750 5% .125W CC TC=-330/+800	01121	BB7515
A5R18	0698-7228	7	2	RESISTOR 464 1% .05W F TC=0+-100	24546	C3-1/8-T0-464R-G
A5R19	0698-3378	0		RESISTOR 51 5% .125W CC TC=-270/+540	01121	BB5105
A5R20	0698-3111	9		RESISTOR 30 5% .125W CC TC=-270/+540	01121	BB3005
A5R21	0698-3111	9		RESISTOR 30 5% .125W CC TC=-270/+540	01121	BB3005
A5R22	0698-5174	8		RESISTOR 200 5% .125W CC TC=-330/+800	01121	BB2015
A5R23	0698-6241	2		RESISTOR 750 5% .125W CC TC=-330/+800	01121	BB7515
A5R24	0675-1021	8	1	RESISTOR 1K 10% .125W CC TC=-330/+800	01121	BB1021
A5R25	0698-3113	1		RESISTOR 100 5% .125W CC TC=-270/+540	01121	BB1015
A5R26	0698-3376	8	1	RESISTOR 43 5% .125W CC TC=-270/+540	01121	BB4305
A5R27	0698-7228	7		RESISTOR 464 1% .05W F TC=0+-100	24546	C3-1/8-T0-464R-G
A5R28	0698-3380	4		RESISTOR 75 5% .125W CC TC=-270/+540	01121	BB7505
A5U1	1826-0372	2	2	IC 5 GHZ LIMITER/AMP	28480	1826-0372
A5U2	1858-0059	9	2	TRANSISTOR ARRAY	28480	1858-0059
A5U3	1858-0059	9		TRANSISTOR ARRAY	28480	1858-0059
A5U4	1826-0372	2		IC 5 GHZ LIMITER/AMP	28480	1826-0372
A5W1	05342-60100	6	1	CABLE ASSEMBLY, MULTIPLEXER	28480	05342-60100
				A5 MISCELLANEOUS PARTS		
	0363-0133	0	2	CONTACT-FINGER .13-WD .09-FREE-HGT BE-CU	28480	0363-0133
	0380-0970	9	1	STANDOFF-HEX .375-IN-LG 4-40THD	28480	0380-0970
	05342-20101	3	1	SCREW, GROUND	28480	05342-20101

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6	05342-60006	1	1	OFFSET LOOP AMPLIFIER ASSEMBLY (SERIES 1720)	28480	05342-60006
A6C1	0180-0228	6	2	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A6C2	0160-3879	7	6	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C3	0180-0210	6	2	CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A6C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C6	0180-0210	6		CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A6C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C8	0180-0228	6		CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A6C9	0180-1701	2	1	CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A6C10	0160-0128	3	1	CAPACITOR-FXD 2.2UF +-20% 50VDC CER	28480	0160-0128
A6C11	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C12	0160-0162	5	1	CAPACITOR-FXD .022UF +-10% 200VDC POLYE	28480	0160-0162
A6C13	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6CR1	1902-3193	3	2	DIODE-ZNR 13.3V 5% DO-7 PD=.4W TC=+.059%	28480	1902-3193
A6CR2	1902-3193	3		DIODE-ZNR 13.3V 5% DO-7 PD=.4W TC=+.059%	28480	1902-3193
A6CR3	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A6CR4	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A6Q1	1853-0020	4	3	TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
A6Q2	1854-0071	7	1	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A6Q3	1853-0020	4		TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
A6Q4	1853-0020	4		TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
A6R1	2100-2489	9	1	RESISTOR-TRMR 5K 10% C SIDE-ADJ 1-TRN	30983	ET50X502
A6R2	2100-2633	5	1	RESISTOR-TRMR 1K 10% C SIDE-ADJ 1-TRN	30983	ET50X102
A6R3	0757-0288	1	1	RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
A6R4	0757-0279	0	9	RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A6R5	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R6	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R7	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R8	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A6R9	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R10	0757-0416	7	1	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A6R11	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R12	0757-0440	7	1	RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A6R13	0757-0289	2	1	RESISTOR 13.3K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-1332-F
A6R14	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R15	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A6R16	0757-0438	3	1	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A6R17	0757-0200	7	1	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A6R18	0757-0424	7	1	RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
A6R19	0757-0407	6	1	RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A6R20	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A6R21	0698-3153	9	1	RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A6R22	0757-0199	3	1	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A6R23	0757-0427	0	2	RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A6R24	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A6R25	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A6U1	1820-1425	6	1	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A6U2	1820-0493	6	1	IC OP AMP 8-DIP-P	27014	LM307N
				A6 MISCELLANEOUS PARTS		
	1251-0600	0	1	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ 30	28480	1251-0600
	5000-9043	6	1	PIN;P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6852	3	1	EXTRACTOR, ORANGE	28480	5040-6852

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7	05342-60007	2	1	MIXER/SEARCH CONTROL ASSEMBLY (SERIES 1720)	28480	05342-60007
A7C1	0160-3879	7	9	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A7C2	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A7C3	0180-0155	8	2	CAPACITOR-FXD 2.2UF+-20% 20VDC TA	56289	150D225X0020A2
A7C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A7C5	0180-0155	8		CAPACITOR-FXD 2.2UF+-20% 20VDC TA	56289	150D225X0020A2
A7C6	0160-3878	6	10	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A7C7	0180-1701	2	4	CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A7C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A7C9	0180-1701	2		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A7C10	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A7C11	0180-1701	2		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A7C12	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A7C13	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A7C14	0180-1701	2		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A7C15	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A7C16	0160-3875	3	1	CAPACITOR-FXD 22PF +-5% 200VDC CER 0+-30	28480	0160-3875
A7C17	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A7C18	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A7C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A7C20	0160-3877	5	2	CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A7C21	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A7C22	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A7C23	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A7C24	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A7C25	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A7C26	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A7C27	0160-3877	5		CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A7C28	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A7CR1	1901-0518	8	2	DIODE-SCHOTTKY	28480	1901-0518
A7CR2	1901-0518	8		DIODE-SCHOTTKY	28480	1901-0518
A7L1	9100-2268	9	8	COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A7L2	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A7L3	9100-2247	4	3	COIL-MLD 100NH 10% Q=34 .095DX.25LG-NOM	28480	9100-2247
A7L4	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A7L5	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A7L6	9100-2247	4		COIL-MLD 100NH 10% Q=34 .095DX.25LG-NOM	28480	9100-2247
A7L7	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A7L8	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A7L9	9100-2247	4		COIL-MLD 100NH 10% Q=34 .095DX.25LG-NOM	28480	9100-2247
A7L10	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A7L11	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A7Q1	1854-0345	8	2	TRANSISTOR NPN 2N5179 SI TO-72 PD=200MW	04713	2N5179
A7Q2	1854-0092	2	2	TRANSISTOR NPN SI PD=200MW FT=600MHZ	28480	1854-0092
A7Q3	1854-0092	2		TRANSISTOR NPN SI PD=200MW FT=600MHZ	28480	1854-0092
A7Q4	1854-0071	7	2	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q5	1854-0071	7		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q6	1854-0345	8		TRANSISTOR NPN 2N5179 SI TO-72 PD=200MW	04713	2N5179
A7R1	0698-7101	5	1	RESISTOR 3K 5% .125W CC TC=-350/+857	01121	BB3025
A7R2	0698-5426	3	2	RESISTOR 10K 10% .125W CC TC=-350/+857	01121	BB1031
A7R3	0698-5426	3		RESISTOR 10K 10% .125W CC TC=-350/+857	01121	BB1031
A7R4	0698-5180	6	4	RESISTOR 2K 5% .125W CC TC=-350/+857	01121	BB2025
A7R5	0698-5181	7	1	RESISTOR 3.6K 5% .125W CC TC=-350/+857	01121	BB3625
A7R6	0698-6294	5	1	RESISTOR 47K 5% .125W CC TC=-466/+875	01121	BB4735
A7R7	0698-3378	0	2	RESISTOR 51 5% .125W CC TC=-270/+540	01121	BB5105
A7R8	0698-5075	8	2	RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A7R9	0698-3113	1	3	RESISTOR 100 5% .125W CC TC=-270/+540	01121	BB1015
A7R10	0698-5172	6	2	RESISTOR 13 5% .125W CC TC=-270/+540	01121	BB1305
A7R11	0698-5567	3	1	RESISTOR 27K 5% .125W CC TC=-466/+875	01121	BB2735
A7R12	0698-5174	8	1	RESISTOR 200 5% .125W CC TC=-330/+800	01121	BB2015
A7R13	0698-3113	1		RESISTOR 100 5% .125W CC TC=-270/+540	01121	BB1015
A7R14	0698-5565	1	1	RESISTOR 2.2K 5% .125W CC TC=-350/+857	01121	BB2225
A7R15	0698-5180	6		RESISTOR 2K 5% .125W CC TC=-350/+857	01121	BB2025
A7R16	0698-5180	6		RESISTOR 2K 5% .125W CC TC=-350/+857	01121	BB2025
A7R17	0698-5180	6		RESISTOR 2K 5% .125W CC TC=-350/+857	01121	BB2025
A7R18	0698-3378	0		RESISTOR 51 5% .125W CC TC=-270/+540	01121	BB5105
A7R19	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A7R20	0698-5172	6		RESISTOR 13 5% .125W CC TC=-270/+540	01121	BB1305
A7R21	0698-3113	1		RESISTOR 100 5% .125W CC TC=-270/+540	01121	BB1015
A7R22	0698-3379	1	1	RESISTOR 68 5% .125W CC TC=-270/+540	01121	BB6805
A7TP1	1251-0600	0	1	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SO	28480	1251-0600
A7U1	1820-0630	3	1	IC MISC TTL	04713	MC4044P
A7U2	1820-1206	1	1	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
A7U3	1826-0372	2	2	IC 5 GHZ LIMITER/AMP	28480	1826-0372
A7U4	1826-0372	2		IC 5 GHZ LIMITER/AMP	28480	1826-0372

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8	05342-60008	3	1	MAIN VCO ASSEMBLY (SERIES 1720)	28480	05342-60008
A8C1	0180-0228	6	1	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A8C2	0160-3878	6	17	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C3	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C4	0160-3877	5	4	CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A8C5	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C6	0160-3877	5		CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A8C7	0160-3872	0	1	CAPACITOR-FXD 2.2PF +-.25PF 200VDC CER	28480	0160-3872
A8C8	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C9	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C10	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C11	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C12	0160-3877	5		CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A8C13	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C14	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C15	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C16	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C17	0160-3877	5		CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A8C18	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C20	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C21	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C22	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C23	0180-0210	6	1	CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A8C24	0180-1701	2	4	CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A8C25	0180-1701	2		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A8C26	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C27	0180-1701	2		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A8C28	0180-1701	2		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A8C29	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8CR1	0122-0065	7	2	CAPACITOR1VOLTAGE VAR;29 PF/+3V	28480	0122-0065
A8CR2	0122-0065	7		CAPACITOR1VOLTAGE VAR;29 PF/+3V	28480	0122-0065
A8CR3	1902-3171	7	1	DIODE-ZNR 11V 5% DO-7 PD=.4W TC=+.062%	28480	1902-3171
A8E1	9170-0016	8	1	CORE-SHIELDING BEAD	28480	9170-0016
A8L1	9100-2268	9	9	COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L2	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L3	9100-2247	4	3	COIL-MLD 100NH 10% Q=34 .095DX.25LG-NOM	28480	9100-2247
A8L4	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L5	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L6	9100-2247	4		COIL-MLD 100NH 10% Q=34 .095DX.25LG-NOM	28480	9100-2247
A8L7	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L8	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L9	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L10	9100-2247	4		COIL-MLD 100NH 10% Q=34 .095DX.25LG-NOM	28480	9100-2247
A8L11	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8L12	9100-2268	9		COIL-MLD 22UH 10% Q=45 .095DX.25LG-NOM	28480	9100-2268
A8Q1	1854-0345	8	1	TRANSISTOR NPN 2N5179 SI TO-72 PD=200MW	04713	2N5179
A8Q2	1854-0071	7	1	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A8R1	0698-5174	8	1	RESISTOR 200 5% .125W CC TC=-330/+800	01121	BB2015
A8R2	0698-3376	8	3	RESISTOR 43 5% .125W CC TC=-270/+540	01121	BB4305
A8R3	0698-5172	6	3	RESISTOR 13 5% .125W CC TC=-270/+540	01121	BB1305
A8R4	0698-5996	2	1	RESISTOR 560 5% .125W CC TC=-330/+800	01121	BB5615
A8R5	0698-3376	8		RESISTOR 43 5% .125W CC TC=-270/+540	01121	BB4305
A8R6	0698-5075	8	3	RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A8R7	0698-3378	0	3	RESISTOR 51 5% .125W CC TC=-270/+540	01121	BB5105
A8R8	0698-3376	8		RESISTOR 43 5% .125W CC TC=-270/+540	01121	BB4305
A8R9	0698-5562	8	1	RESISTOR 120 5% .125W CC TC=-330/+800	01121	BB1215
A8R10	0698-5172	6		RESISTOR 13 5% .125W CC TC=-270/+540	01121	BB1305
A8R11	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A8R12	0698-5999	5	3	RESISTOR 4.7K 5% .125W CC TC=-350/+857	01121	BB4725
A8R13	0698-5999	5		RESISTOR 4.7K 5% .125W CC TC=-350/+857	01121	BB4725
A8R14	0698-5999	5		RESISTOR 4.7K 5% .125W CC TC=-350/+857	01121	BB4725
A8R15	0698-3378	0		RESISTOR 51 5% .125W CC TC=-270/+540	01121	BB5105
A8R16	0698-7212	9	1	RESISTOR 100 1% .05W F TC=0+-100	24546	C3-1/8-T0-100R-G
A8R17	0698-5172	6		RESISTOR 13 5% .125W CC TC=-270/+540	01121	BB1305
A8R18	0698-5075	8		RESISTOR 130 5% .125W CC TC=-330/+800	01121	BB1315
A8R19	0698-3380	4	1	RESISTOR 75 5% .125W CC TC=-270/+540	01121	BB7505
A8R20	0698-3378	0		RESISTOR 51 5% .125W CC TC=-270/+540	01121	BB5105
A8R21	0698-5426	3	1	RESISTOR 10K 10% .125W CC TC=-350/+857	01121	BB1031
A8R22	2100-2469	9	1	RESISTOR-TRMR 5K 10% C SIDE-ADJ 1-TRN	30983	ET50X502
A8R23	0698-5178	2	1	RESISTOR 1.5K 5% .125W CC TC=-350/+857	01121	BB1525
A8U1	1826-0372	2	1	IC 5 GHZ LIMITER/AMP	28480	1826-0372
				A8 MISCELLANEOUS PARTS		
	0363-0133	0	2	CONTACT-FINGER .13-WD .09-FREE-HGT BE-CU	28480	0363-0133
	0380-0970	9	1	STANDOFF-HEX .375-IN-LG 4-40THD	28480	0380-0970
	05342-20101	3	1	SCREW, GROUND	28480	05342-20101

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A9	05342-60009	4	1	MAIN LOOP AMPLIFIER ASSEMBLY (SERIES 1720)	28480	05342-60009
A9C1	0160-4084	8	2	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A9C2	0160-0165	8	1	CAPACITOR-FXD .056UF +-10% 200VDC POLYE	28480	0160-0165
A9C3	0180-0210	6	2	CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A9C4	0160-3879	7	5	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A9C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A9C6	0180-1701	2	1	CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A9C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A9C8	0160-0301	8	1	CAPACITOR-FXD .012UF +-10% 200VDC POLYE	28480	0160-0301
A9C9	0160-0153	4	2	CAPACITOR-FXD 1000PF +-10% 200VDC POLYE	28480	0160-0153
A9C10	0160-0160	3	1	CAPACITOR-FXD 8200PF +-10% 200VDC POLYE	28480	0160-0160
A9C11	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A9C12	0140-0200	0	1	CAPACITOR-FXD 390PF +-5% 300VDC MICA	72136	DM15F391J0300WV1CR
A9C13	0180-0228	6	2	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A9C14	0180-0210	6		CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A9C15	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A9C16	0160-0153	4		CAPACITOR-FXD 1000PF +-10% 200VDC POLYE	28480	0160-0153
A9C17	0180-0228	6		CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A9C18	0160-0137	8	1	CAPACITOR-FXD .33UF +-20% 25VDC CER	28480	0160-0137
A9C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A9CR1	1902-0049	2	2	DIODE-ZNR 6.19V 5% DO-7 PD=.4W TC=+.022%	28480	1902-0049
A9CR2	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A9CR3	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A9CR4	1902-0049	2		DIODE-ZNR 6.19V 5% DO-7 PD=.4W TC=+.022%	28480	1902-0049
A9L1	9140-0131	5	3	COIL-MLD 10MH 5% Q=80 .240X.74LG-NOM	28480	9140-0131
A9L2	9140-0131	5		COIL-MLD 10MH 5% Q=80 .240X.74LG-NOM	28480	9140-0131
A9L3	9140-0131	5		COIL-MLD 10MH 5% Q=80 .240X.74LG-NOM	28480	9140-0131
A9Q1	1853-0020	4	3	TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
A9Q2	1853-0020	4		TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
A9Q3	1853-0020	4		TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
A9Q4	1854-0071	7	1	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A9R1	0757-0279	0	2	RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A9R2	0698-6123	9	2	RESISTOR 20K 5% .125W CC TC=-466/+875	01121	BB2035
A9R3	0757-0280	3	3	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A9R4	0757-0199	3	3	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A9R5	0698-5184	0	2	RESISTOR 6.2K 5% .125W CC TC=-350/+857	01121	BB6225
A9R6	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A9R7	0698-6123	9		RESISTOR 20K 5% .125W CC TC=-466/+875	01121	BB2035
A9R8	0698-5184	0		RESISTOR 6.2K 5% .125W CC TC=-350/+857	01121	BB6225
A9R9	0698-3446	3	1	RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A9R10	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A9R11	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A9R12	0698-3150	6	1	RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A9R13	0757-0290	5	1	RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A9R14	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A9R15	0757-0418	9	1	RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A9R16*	0683-1065	7	1	RESISTOR 10M 5% .25W FC TC=+900/+1100	01121	CB1065
A9R17	0757-0283	6	2	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A9R18	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A9R19	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A9S1	1520-1325	5	1	IC SW CMOS BILATL QUAD	01928	CD4066AE
A9TP1	1251-0600	0	1	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A9U1	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A9U2	1820-0493	6	1	IC OP AMP 8-DIP-P	27014	LM307N
				A9 MISCELLANEOUS PARTS		
	5000-9043	6	1	PIN,P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6852	3	1	EXTRACTOR, ORANGE	28480	5040-6852

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10	05342-60010	7	1	DIVIDE-BY-N ASSEMBLY (SERIES 1720)	28480	05342-60010
A10C1	0180-1701	2	8	CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A10C2	0180-0106	9	1	CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X0006B2
A10C3	0180-1701	2		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A10C4	0160-3878	6	15	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10C5	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10C6	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10C7	0180-1701	2		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A10C8	0180-1701	2		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A10C9	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10C10	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10C11	0160-3875	3	1	CAPACITOR-FXD 22PF +-5% 200VDC CER 0+-30	28480	0160-3875
A10C12	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10C13	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10C14	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10C15	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10C16	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10C17	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10C18	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10C19	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10C20	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10C21	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A10L1	9100-2268	9	1	COIL-MLD 22UH 10% Q=45 .090DX.25LG-NOM	28480	9100-2268
A10L2	9100-1786	6	3	CHOKE-WIDE BAND ZMAX=680 OHMS 180 MHZ	02114	VK200 20/4B
A10L3	9100-1788	6		CHOKE-WIDE BAND ZMAX=680 OHMS 180 MHZ	02114	VK200 20/4B
A10L4	9100-1788	6		CHOKE-WIDE BAND ZMAX=680 OHMS 180 MHZ	02114	VK200 20/4B
A10R1	0675-1021	A	2	RESISTOR 1K 10% .125W CC TC=-330/+800	01121	BB1021
A10R2	0698-5996	2	1	RESISTOR 560 5% .125W CC TC=-330/+800	01121	BB5615
A10R3	0698-8873	2	1	RESISTOR 1.6K 5% .125W CC TC=-350/+857	01121	BB1625
A10R4	0698-3110	2	1	RESISTOR 300 5% .125W CC TC=-330/+800	01121	BB3015
A10R5	0698-6242	3	1	RESISTOR 1.2K 5% .125W CC TC=-350/+857	01121	BB1225
A10R6	0698-3360	4	1	RESISTOR 75 5% .125W CC TC=-270/+540	01121	BB7505
A10R7	0698-5177	1	1	RESISTOR 820 5% .125W CC TC=-330/+800	01121	BB8215
A10R8	0698-7101	5	1	RESISTOR 3K 5% .125W CC TC=-350/+857	01121	BB3025
A10R9	0698-5565	1	1	RESISTOR 2.2K 5% .125W CC TC=-350/+857	01121	BB2225
A10R10	0698-3376	8	1	RESISTOR 43 5% .125W CC TC=-270/+540	01121	BB4305
A10R11	0675-1021	8		RESISTOR 1K 10% .125W CC TC=-330/+800	01121	BB1021
A10TP1	1251-0600	0	1	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A10U1	1820-1251	6	1	IC CNTR TTL LS DECD ASYNCHRO	01295	SN74LS196N
A10U2	1820-0636	3	1	IC MISC TTL	04713	MC4044P
A10U3	1820-0069	2	1	IC GATE TTL NAND DUAL 4-INP	01295	SN7420N
A10U4	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A10U5	1820-1225	9	1	IC FF ECL D-M/S DUAL	04713	MC10231P
A10U6	1820-0736	0	1	IC CNTR ECL BIN DUAL	28480	1820-0736
A10U7	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A10U8	1820-1429	0	4	IC CNTR TTL LS DECD SYNCHRO	01295	SN74LS160N
A10U9	1820-1429	0		IC CNTR TTL LS DECD SYNCHRO	01295	SN74LS160N
A10U10	1820-1196	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A10U11	1820-1195	7	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
A10U12	1820-1888	5	1	IC PRESCR ECL	04713	MC12013L
A10U13	1820-1429	0		IC CNTR TTL LS DECD SYNCHRO	01295	SN74LS160N
A10U14	1820-1429	0		IC CNTR TTL LS DECD SYNCHRO	01295	SN74LS160N
A10U15	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A10U16	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
A10U17	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
				A10 MISCELLANEOUS PARTS		
	5000-9043	6	1	PIN;P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6852	3	1	EXTRACTOR, ORANGE	28480	5040-6852

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11	05342-60011	8	1	IF LIMITER ASSEMBLY (SERIES 1720)	28480	05342-60011
A11C1	0160-3879	7	5	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C2	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C3	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A11C6	0180-0490	0	2	CAPACITOR-FXD 68UF+-10% 6VDC TA	90201	TDC686K006WLF
A11C7	0180-0490	0		CAPACITOR-FXD 68UF+-10% 6VDC TA	90201	TDC686K006WLF
A11CR1	1901-0535	9	2	DIODE-SCHOTTKY	28480	1901-0535
A11CR2	1901-0535	9		DIODE-SCHOTTKY	28480	1901-0535
A11L1	9100-2247	4	1	COIL-MLD 100NH 10% Q=34 .095DX.25LG-NOM	28480	9100-2247
A11L2	9100-2265	6	2	COIL-MLD 10UH 10% Q=60 .095DX.25LG-NOM	28480	9100-2265
A11L3	9100-2265	6		COIL-MLD 10UH 10% Q=60 .095DX.25LG-NOM	28480	9100-2265
A11R1	2100-3207	1	1	RESISTOR-TRMR 5K 10% C SIDE-ADJ 1-TRN	28480	2100-3207
A11R2	0698-7102	6	1	RESISTOR 5.1K 5% .125W CC TC=-350/+857	01121	BB5125
A11R3	0698-5176	0	1	RESISTOR 510 5% .125W CC TC=-330/+800	01121	BB5115
A11R4	0698-7964	8	1	RESISTOR 100K 5% .125W CC TC=-486/+875	28480	0698-7964
A11R5	0698-3113	1	2	RESISTOR 100 5% .125W CC TC=-270/+540	01121	BB1015
A11R6	0698-5996	2	1	RESISTOR 560 5% .125W CC TC=-330/+800	01121	BB5615
A11R7	0698-3111	9	1	RESISTOR 30 5% .125W CC TC=-270/+540	01121	BB3005
A11R8	0698-7185	5	2	RESISTOR 220K 5% .125W CC TC=-600/+1137	01121	BB2245
A11R9	0698-7185	5		RESISTOR 220K 5% .125W CC TC=-600/+1137	01121	BB2245
A11R10	0698-3113	1		RESISTOR 100 5% .125W CC TC=-270/+540	01121	BB1015
A11R11	0698-7026	3	1	RESISTOR 91 5% .125W CC TC=-270/+540	01121	BB9105
A11R12	0698-1021	8	1	RESISTOR 1K 10% .125W CC TC=-330/+800	01121	BB1021
A11R13	0698-5993	9	1	RESISTOR 8.2K 5% .125W CC TC=-350/+857	01121	BB8225
A11R14	2100-3352	7	1	RESISTOR-TRMR 1K 10% C SIDE-ADJ 1-TRN	28480	2100-3352
A11TP2	1251-0600	0	3	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP3	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP7	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11U1	1826-0065	0	1	IC 311 COMPARATOR 8-DIP-P	01295	SN72311P
A11U2	1826-0372	2	1	IC 5 GHZ LIMITER/AMP	28480	1826-0372
				A11 MISCELLANEOUS PARTS		
	5000-9043	6	1	PIN;P,C, BOARD EXTRACTOR	28480	5000-9043
	5040-6852	3	1	EXTRACTOR, ORANGE	28480	5040-6852

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A12	05343-60009	5	1	IF DETECTOR (SERIES 1932)	28480	05343-60009
A12C1	0160-3872	0	1	CAPACITOR-FXD 2.2PF +-.25PF 200VDC CER	28480	0160-3872
A12C2	0160-3879	7	12	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A12C3	0160-3874	6	1	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3874
A12C4	0160-3873	1	1	CAPACITOR-FXD 4.7PF +-.5PF 200VDC CER	28480	0160-3873
A12C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A12C6	0160-3879	7				
A12C7	0160-3877	5	1	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A12C8	0160-2262	0	2	CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A12C9	0160-3879	7		CAPACITOR-FXD 16PF +-5% 500VDC CER 0+-30	28480	0160-2262
A12C10	0160-2262	0		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A12C11	0160-3879	7		CAPACITOR-FXD 16PF +-5% 500VDC CER 0+-30	28480	0160-2262
A12C12	0150-0115	7	1	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A12C13	0180-0490	4	3	CAPACITOR-FXD 27PF +-10% 500VDC CER	28480	0150-0115
A12C14	0160-4084	A	1	CAPACITOR-FXD 68UF+-10% 6VDC TA	90201	TDC686K006WLF
A12C15	0160-3879	7		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A12C16	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A12C17	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A12C18	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A12C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A12C20	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A12C21	0160-3879	7				
A12C22	0180-0491	5	2	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A12C23	0180-0491	5		CAPACITOR-FXD 10UF+-20% 25VDC TA	28480	0180-0491
A12C24	0180-0490	4		CAPACITOR-FXD 10UF+-20% 25VDC TA	28480	0180-0491
A12C25	0180-0490	4		CAPACITOR-FXD 68UF+-10% 6VDC TA	90201	TDC686K006WLF
				CAPACITOR-FXD 68UF+-10% 6VDC TA	90201	TDC686K006WLF
A12CR1	1901-0535	9	3	DIODE-SCHOTTKY	28480	1901-0535
A12CR2	1901-0535	9		DIODE-SCHOTTKY	28480	1901-0535
A12CR3	1901-0535	9		DIODE-SCHOTTKY	28480	1901-0535
A12CR4	1901-0040	1	1	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A12L1	9100-2251	0	1	COIL-MLD 220NH 10% Q=32 .095DX.25LG-NOM	28480	9100-2251
A12L2	9100-2250	9	2	COIL-MLD 180NH 10% Q=30 .095DX.25LG-NOM	28480	9100-2250
A12L3	9100-2250	9		COIL-MLD 150NH 10% Q=30 .095DX.25LG-NOM	28480	9100-2250
A12L4	9100-0346	0	1	COIL-MLD 50NH 20% Q=46 .095DX.25LG-NOM	28480	9100-0346
A12L5	9100-2265	6	3	COIL-MLD 10UH 10% Q=60 .095DX.25LG-NOM	28480	9100-2265
A12L6	9100-2265	6				
A12L7	9100-2265	6		COIL-MLD 10UH 10% Q=60 .095DX.25LG-NOM	28480	9100-2265
A12L8	9100-1788	6	2	COIL-MLD 10UH 10% Q=60 .095DX.25LG-NOM	28480	9100-2265
A12L9	9100-1788	6		CHOKE-WIDE BAND ZMAX=680 OHMS 180 MHZ	02114	VK200 20/48
				CHOKE-WIDE BAND ZMAX=640 OHMS 180 MHZ	02114	VK200 20/48
A12Q1	1854-0345	8	1	TRANSISTOR NPN 2N5179 SI TO-72 PD=200MW	04713	2N5179
A12R1	0698-7102	6	2	RESISTOR 5.1K 5% .125W CC TC=-350/+857	01121	BB5125
A12R2	2100-2489	9	2	RESISTOR-TRMR 5K 10% C SIDE-ADJ 1-TRN	30983	ET50X502
A12R3	0698-3457	6	2	RESISTOR 316K 1% .125W F TC=0+-100	28480	0698-3457
A12R4	0698-3111	9	2	RESISTOR 30 5% .125W CC TC=-270/+540	01121	BB30G5
A12R5	0757-0402	1	2	RESISTOR 110 1% .125W F TC=0+-100	28546	C4-1/8-T0-111-F
A12R6	0757-0402	1		RESISTOR 110 1% .125W F TC=0+-100	24546	C4-1/8-T0-111-F
A12R7	2100-2574	3	1	RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	30983	ET50X501
A12R8	0698-7026	3	1	RESISTOR 91 5% .125W CC TC=-270/+540	01121	BB91G5
A12R9	0698-1021	8	1	RESISTOR 1K 10% .125W CC TC=-330/+800	01121	BB1021
A12R10	0698-7964	8	1	RESISTOR 100K 5% .125W CC TC=-466/+875	28480	0698-7964
A12R11	0698-5176	0	1	RESISTOR 510 5% .125W CC TC=-330/+800	01121	BB5115
A12R12	0698-5174	8	2	RESISTOR 200 5% .125W CC TC=-330/+800	01121	BB2015
A12R13	2100-2489	9		RESISTOR-TRMR 5K 10% C SIDE-ADJ 1-TRN	30983	ET50X502
A12R14	0757-0442	9	1	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A12R15	0698-3457	6		RESISTOR 316K 1% .125W F TC=0+-100	28480	0698-3457
A12R16	0757-0397	3	1	RESISTOR 60.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-68R1-F
A12R17	0698-7102	6		RESISTOR 5.1K 5% .125W CC TC=-350/+857	01121	BB5125
A12R18	0698-3380	8	1	RESISTOR 75 5% .125W CC TC=-270/+540	01121	BB75G5
A12R19	0698-8368	8	1	RESISTOR 82 5% .125W CC TC=-270/+540	01121	BB82G5
A12R20	0757-0407	6	1	RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A12R21	0698-3381	5	1	RESISTOR 150 5% .125W CC TC=-330/+800	01121	BB1515
A12R22	0698-3111	9		RESISTOR 30 5% .125W CC TC=-270/+540	01121	BB30G5
A12R23	0698-5174	8		RESISTOR 200 5% .125W CC TC=-330/+800	01121	BB2015
A12R24	0698-3114	2	2	RESISTOR 300 5% .125W CC TC=-330/+800	01121	BB3015
A12R25	0698-3114	2		RESISTOR 300 5% .125W CC TC=-330/+800	01121	BB3015
A12TP1	1251-0600	0	11	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ SQ	28480	1251-0600
A12TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ SQ	28480	1251-0600
A12TP3	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ SQ	28480	1251-0600
A12TP4	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ SQ	28480	1251-0600
A12TP5	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ SQ	28480	1251-0600

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A12TP6	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A12TP7	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A12TP8	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A12TP9	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A12TP10	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A12TP11	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A12U1	1826-0065	0	1	IC COMPARATOR PRCN 8-DIP-P	01295	SN72311P
A12U2	1826-0372	2	2	IC 5 GHZ LIMITER/AMP	28480	1826-0372
A12U3	1820-1225	4	1	IC FF ECL D-M/S DUAL	04713	MC10231P
A12U4	1826-0372	2		IC 5 GHZ LIMITER/AMP	28480	1826-0372
A12U5	1820-0765	5	1	IC CNTR TTL BIN ASYNCHRO NEG-EDGE-TRIG	01295	SN74197N
A12U6	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A12U7	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A12U8	1820-1285	6	2	IC GATE TTL LS AND-OR-INV 4-INP	01295	SN74LS54N
A12U9	1820-1285	6		IC GATE TTL LS AND-OR-INV 4-INP	01295	SN74LS54N
A12U10	1820-1193	5	2	IC CNTR TTL LS BIN ASYNCHRO	01295	SN74LS197N
A12U11	1820-0174	0	1	IC INV TTL HEX	01295	SN7404N
A12U12	1820-1255	0	1	IC INV TTL HEX 1-INP	01295	SN74366N
A12U13	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A12U14	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A12U15	1820-1193	5		IC CNTR TTL LS BIN ASYNCHRO	01295	SN74LS197N
				A12 MISCELLANEOUS PARTS		
	5000-9043	6	1	#IN-P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6852	3	1	EXTRACTOR, ORANGE	28480	5040-6852

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A13	05342-60013	0	1	COUNTER ASSEMBLY (SERIES 1720)	28480	05342-60013
A13C1	0160-3879	7	21	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C2	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C3	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C9	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C11	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C13	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C14	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C15	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C16	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C17	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C18	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C20	0180-1746	5	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A13C21	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C22	0180-0106	9	2	CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X0006B2
A13C23	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C25	0180-0106	9		CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X0006B2
A13CR1	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A13CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A13L1	9100-1788	6	2	CHOKE-WIDE BAND ZMAX=680 OHMS 180 MHZ	02114	VK200 20/4B
A13L2	9100-1788	6		CHOKE-WIDE BAND ZMAX=680 OHMS 180 MHZ	02114	VK200 20/4B
A13Q1	1854-0071	7	2	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A13Q2	1854-0071	7		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A13R1	1810-0055	5	2	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0055
A13R2	0683-4725	2	6	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A13R3	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A13R4	0683-5115	6	4	RESISTOR 510 5% .25W FC TC=-400/+600	01121	CB5115
A13R5	1810-0055	5		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0055
A13R6	0683-2225	3	1	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A13R7	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A13R8	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A13R9	0683-1025	9	2	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A13R10	0683-1035	1	6	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A13R11	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A13R12	0683-1635	7	1	RESISTOR 16K 5% .25W FC TC=-400/+800	01121	CB1635
A13R13	0683-6825	7	4	RESISTOR 6.8K 5% .25W FC TC=-400/+700	01121	CB6825
A13R14	0683-2735	0	1	RESISTOR 27K 5% .25W FC TC=-400/+800	01121	CB2735
A13R15	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A13R16	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A13R17	0683-6825	7		RESISTOR 6.8K 5% .25W FC TC=-400/+700	01121	CB6825
A13R18	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A13R19	0683-3915	0	1	RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A13R20	0683-1215	9	1	RESISTOR 120 5% .25W FC TC=-400/+600	01121	CB1215
A13R21	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A13R22	0683-2015	9	1	RESISTOR 200 5% .25W FC TC=-400/+600	01121	CB2015
A13R23	0683-3325	6	1	RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A13R24	0683-5125	8	1	RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125
A13R25	0683-6825	7		RESISTOR 6.8K 5% .25W FC TC=-400/+700	01121	CB6825
A13R26	0683-6825	7		RESISTOR 6.8K 5% .25W FC TC=-400/+700	01121	CB6825
A13R27	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A13R28	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A13R29	0683-1315	0	1	RESISTOR 130 5% .25W FC TC=-400/+600	01121	CB1315
A13R30	0683-5115	6		RESISTOR 510 5% .25W FC TC=-400/+600	01121	CB5115
A13R31	0683-3315	4	1	RESISTOR 330 5% .25W FC TC=-400/+600	01121	CB3315
A13R32	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A13R33	0683-5115	6		RESISTOR 510 5% .25W FC TC=-400/+600	01121	CB5115
A13R34	0683-5115	6		RESISTOR 510 5% .25W FC TC=-400/+600	01121	CB5115
A13TP1	1251-0600	0	8	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SD	28480	1251-0600
A13TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SD	28480	1251-0600
A13TP3	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SD	28480	1251-0600
A13TP4	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SD	28480	1251-0600
A13TP5	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SD	28480	1251-0600

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A13TP6	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A13TP7	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A13TP8	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A13U1	1820-0634	7	2	IC CNTR MOS DECD	28480	1820-0634
A13U2	1820-0634	7		IC CNTR MOS DECD	28480	1820-0634
A13U3	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A13U4	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A13U5	1820-1238	9	4	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A13U6	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A13U7	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A13U8	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A13U9	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A13U10	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A13U11	1820-1950	2	1	IC GATE ECL OR-NOR 3-INP	04713	MC10212P
A13U12	1820-1225	4	2	IC FF ECL D-M/S DUAL	04713	MC10231P
A13U13	1820-1251	6	4	IC CNTR TTL LS DECD ASYNCHRO	01295	SN74LS196N
A13U14	1820-1251	6		IC CNTR TTL LS DECD ASYNCHRO	01295	SN74LS196N
A13U15	1820-1052	5	1	IC XLTR ECL/TTL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A13U16	1820-1225	4		IC FF ECL D-M/S DUAL	04713	MC10231P
A13U17	1820-1251	6		IC CNTR TTL LS DECD ASYNCHRO	01295	SN74LS196N
A13U18	1820-1251	6		IC CNTR TTL LS DECD ASYNCHRO	01295	SN74LS196N
				A13 MISCELLANEOUS PARTS		
	5000-9043	6	1	PIN:P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6852	3	1	EXTRACTOR, ORANGE	28480	5040-6852

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A14	05343-60006	2	1	PROCESSOR (SERIES 1932)	28480	05343-60006
A14C3	0160-3879	7	12	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A14C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A14C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A14C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A14C8	0180-2662	6	1	CAPACITOR-FXD 10UF+-10% 10VDC TA	25088	D4R7G91A10K
A14C9	0160-0570	9	2	CAPACITOR-FXD 220PF +-20% 100VDC CER	20932	5024EM100RD221M
A14C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A14C11	0160-0570	9		CAPACITOR-FXD 220PF +-20% 100VDC CER	20932	5024EM100RD221M
A14C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A14C13	0160-3877	5	1	CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A14C14	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A14C15	0180-0106	9	1	CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X0006B2
A14C16	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A14C17	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A14C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A14C20	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A14C21	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A14C22	0160-4350	1	1	CAPACITOR-FXD 68PF +-5% 200VDC CER 0+-30	28480	0160-4350
A14CR1	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A14CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A14CR3	1901-0535	9	1	DIODE-SCHOTTKY	28480	1901-0535
A14L1	9100-2268	9	1	COIL-MLD 22UH 10% Q=45 .095Dx.25LG-NOM	28480	9100-2268
A14L2	9100-1788	6	1	CHOKE-WIDE BAND ZMAX=680 OHM@ 180 MHZ	02114	VK200 20/4B
A14R1	1810-0279	5	2	NETWORK-RES 10-SIP4,7K OHM X 9	01121	210A472
A14R2	0698-7252	7	5	RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-G
A14R3	1810-0279	5		NETWORK-RES 10-SIP4,7K OHM X 9	01121	210A472
A14R4	0698-7229	8	1	RESISTOR 511 1% .05W F TC=0+-100	24546	C3-1/8-T0-511R-G
A14R5	0698-7200	5	2	RESISTOR 31.6 1% .05W F TC=0+-100	24546	C3-1/8-T00-31R6-G
A14R6	0698-7200	5		RESISTOR 31.6 1% .05W F TC=0+-100	24546	C3-1/8-T00-31R6-G
A14R7	0698-7252	7		RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-G
A14R8	0698-7252	7		RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-G
A14R9	0698-7252	7		RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-G
A14R10	0698-7252	7		RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-G
A14R11	0698-7248	7	1	RESISTOR 2.15K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2151-G
A14TP1	0360-1682	0	11	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A14TP2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A14TP3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A14TP4	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A14TP5	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A14TP6	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A14TP7	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A14TP8	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A14TP9	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A14TP10	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A14TP11	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A14U5	1820-2206	3	1	IC MISC TTL LS	01295	SN74LS640N
A14U6	1820-1917	1	2	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A14U7	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A14U10	1820-1480	3	1	IC MICPROC NMOS 8-BIT	04713	MC6800L
A14U11	1820-1216	3	3	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A14U12	1820-2036	7	1	IC DRVR NMOS CLOCK DRVR	04713	MC6875L
A14U13	1820-1202	7	2	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A14U14	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A14U15	1820-1692	7	1	IC BFR TTL LS INV HEX 1-INP	01295	SN74LS368AN
A14U16	1820-1281	2	2	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A14U17	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A14U18	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A14U19	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A14U20	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A14U21	1820-1281	2		IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A14U22	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A14U23	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A14U24	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A14U25	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A14XU10	1200-0552	4	1	SOCKET-IC 40-CONT DIP-SLDR	28480	1200-0552
A14XU12	1200-0473	8	1	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0473
A14Y1	0410-1142	4	1	CRYSTAL-QUARTZ 4.00000 MHZ	28480	0410-1142
				A14 MISCELLANEOUS PARTS		
	5000-9043	6	1	PIN(P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6852	3	1	EXTRACTOR, ORANGE	28480	5040-6852

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A16	05343-60010	8	1	MEMORY & SWEEPER CONTROL (SERIES 1932)	28480	05343-60010
A16C1	0160-3879	7	18	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C2	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C3	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C7	0160-3878	6	1	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A16C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C9	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C11	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C13	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C14	0180-0106	9	1	CAPACITOR-FXD 60UF+-20% 6VDC T4	56289	150D606X0006B2
A16C15	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C16	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C17	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C18	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16C20	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A16CR1	1901-0535	9	2	DIODE-SCHOTTKY	28480	1901-0535
A16CR2	1901-0535	9		DIODE-SCHOTTKY	28480	1901-0535
A16L1	9100-1788	6	1	CHOKE-WIDE BAND ZMAX=680 OHMS 100 MHZ	02114	VK200 20/4B
A16R1	0757-0394	0	2	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A16R2	0698-3155	1	2	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A16R3	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A16R4	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A16TP1	1251-0600	0	13	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ BU	28480	1251-0600
A16TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ BU	28480	1251-0600
A16TP3	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ BU	28480	1251-0600
A16TP4	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ BU	28480	1251-0600
A16TP5	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ BU	28480	1251-0600
A16TP6	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ BU	28480	1251-0600
A16TP7	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ BU	28480	1251-0600
A16TP8	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ BU	28480	1251-0600
A16TP9	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ BU	28480	1251-0600
A16TP10	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ BU	28480	1251-0600
A16TP11	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ BU	28480	1251-0600
A16TP12	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ BU	28480	1251-0600
A16TP13	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ BU	28480	1251-0600
A16U2	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
A16U3	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A16U5	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A16U6	1818-1038	2	1	IC NMOS 32K ROM 450-NS 3-S	28480	1818-1038
A16U7	1820-1216	3	3	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A16U8	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A16U9	1818-1039	3	1	IC NMOS 32K ROM 450-NS 3-S	28480	1818-1039
A16U10	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A16U11	1818-0197	2	2	IC NMOS 1K RAM STAT 400-NS 3-S	34335	AM91L118DC
A16U12	1820-1207	2	2	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
A16U13	1820-1207	2		IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
A16U14	1818-0197	2		IC NMOS 1K RAM STAT 400-NS 3-S	34335	AM91L118DC
A16U15	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A16U16	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A16U17	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A16U18	1820-1491	6	1	IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
A16XU6	1200-0565	9	2	SOCKET-IC 24-CONT DIP-SLDR	28480	1200-0565
A16XU9	1200-0565	9		SOCKET-IC 24-CONT DIP-SLDR	28480	1200-0565
				A16 MISCELLANEOUS PARTS		
	5000-9043	6	1	PIN:P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6843	2	1	EXTRACTOR, P.C. BOARD	28480	5040-6843

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A17	05343-60007	3	1	TIMING GENERATOR (SERIES 1932)	28480	05343-60007
A17C1	0160-3879	7	19	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C2	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C3	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C9	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C11	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C13	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C14	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C15	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C16	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C17	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C18	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A17C20	0180-0291	5	1	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A17C21	0180-0106	9	1	CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	1500606X0006B2
A17CR1	1902-3182	0	1	DIODE-ZNR 12.1V 5% DO-7 PD=.4W TC=+.064%	28480	1902-3182
A17Q1	1854-0560	9	1	TRANSISTOR NPN SI DARL PD=310MW	04713	MPS A12
A17Q2	1853-0036	2	1	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A17R1	0698-7260	7	7	RESISTOR 10K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1002-G
A17R2	0698-7260	7		RESISTOR 10K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1002-G
A17R3	0698-7260	7		RESISTOR 10K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1002-G
A17R4	0698-7219	6	1	RESISTOR 196 1% .05W F TC=0+-100	24546	C3-1/8-T0-196R-G
A17R5	0698-7236	7	3	RESISTOR 1K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1001-G
A17R6	0698-7260	7		RESISTOR 10K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1002-G
A17R7	0698-7260	7		RESISTOR 10K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1002-G
A17R8	0698-7260	7		RESISTOR 10K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1002-G
A17R9	0698-7260	7		RESISTOR 10K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1002-G
A17R10	0698-7245	8	4	RESISTOR 2.37K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2371-G
A17R11	0698-7249	2	4	RESISTOR 3.48K 1% .05W F TC=0+-100	24546	C3-1/8-T0-3481-G
A17R12	0698-7253	8	4	RESISTOR 5.11K 1% .05W F TC=0+-100	24546	C3-1/8-T0-5111-G
A17R13	0698-7236	7		RESISTOR 1K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1001-G
A17R14	0698-7236	7		RESISTOR 1K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1001-G
A17R15	0698-7253	8		RESISTOR 5.11K 1% .05W F TC=0+-100	24546	C3-1/8-T0-5111-G
A17R16	0698-7249	2		RESISTOR 3.48K 1% .05W F TC=0+-100	24546	C3-1/8-T0-3481-G
A17R17	0698-7245	8		RESISTOR 2.37K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2371-G
A17R18	0698-7253	8		RESISTOR 5.11K 1% .05W F TC=0+-100	24546	C3-1/8-T0-5111-G
A17R19	0698-7249	2		RESISTOR 3.48K 1% .05W F TC=0+-100	24546	C3-1/8-T0-3481-G
A17R20	0698-7245	8		RESISTOR 2.37K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2371-G
A17R21	0698-7253	8		RESISTOR 5.11K 1% .05W F TC=0+-100	24546	C3-1/8-T0-5111-G
A17R22	0698-7249	2		RESISTOR 3.48K 1% .05W F TC=0+-100	24546	C3-1/8-T0-3481-G
A17R23	0698-7245	8		RESISTOR 2.37K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2371-G
A17R24	0698-7097	8	1	RESISTOR 1M 5% .125W CC TC=-600/+1137	01121	BB1055
A17R25	0698-7256	1	1	RESISTOR 6.81K 1% .05W F TC=0+-100	24546	C3-1/8-T0-6811-G
A17R26	0698-7252	7	2	RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-G
A17R27	0698-7252	7		RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-G
A17TP1	0360-0535	0	9	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A17TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A17TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A17TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A17TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A17TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A17TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A17TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A17TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A17U1	1820-1430	3	2	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A17U2	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A17U3	1820-1197	9	5	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A17U4	1820-1211	8	2	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A17U5	1820-1433	6	3	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A17U6	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A17U7	1820-1202	7	2	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A17U8	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A17U9	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A17U10	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A17U11	1820-1442	7	1	IC CNTR TTL LS DECD ASYNCHRO	01295	SN74LS290N
A17U12	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A17U13	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A17U14	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A17U15	1820-1180	0	1	IC CNTR PMOS	50088	MK5009P
A17U16	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A17U17	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A17U18	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A17U19	1820-1254	9	1	IC BFR TTL NON-INV HEX 1-INP	27014	DM8095N
A17U20	1820-1196	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A17U21	1820-1225	4	1	IC FF ECL D-M/S DUAL	04713	MC10231P
A17U22	1820-1255	0	1	IC INV TTL HEX 1-INP	01295	SN74S04N
				A17 MISCELLANEOUS PARTS		
	8159-0005	0	2	WIRE 22AWG W PVC 1X22 80C	28480	8159-0005
	5000-9043	6	1	PINSP,C, BOARD EXTRACTOR	28480	5000-9043
	5040-6852	3	1	EXTRACTOR, ORANGE	28480	5040-6852

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A18	05342-60018	5	1	TIME BASE BUFFER ASSEMBLY (SERIES 1720)	28480	05342-60018
A18C1	0180-0106	9		CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X000682
A18C2	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A18C3	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A18C4	0180-0106	9		CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X000682
A18C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A18C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A18C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A18C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A18C9	0180-1714	7	2	CAPACITOR-FXD 330UF+-10% 6VDC TA	56289	150D337X900682
A18C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A18C11	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A18C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A18C13	0180-1714	7		CAPACITOR-FXD 330UF+-10% 6VDC TA	56289	150D337X900682
A18CR1	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A18CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A18L1	9140-0179	1	3	COIL-MLD 22UH 10% Q=75 .155DX.375LG-NOM	28480	9140-0179
A18L2	9140-0179	1		COIL-MLD 22UH 10% Q=75 .155DX.375LG-NOM	28480	9140-0179
A18L3	9140-0179	1		COIL-MLD 22UH 10% Q=75 .155DX.375LG-NOM	28480	9140-0179
A18R1	0698-5178	2	2	RESISTOR 1.5K 5% .125W CC TC=-350/+857	01121	BB1525
A18R2	0698-5181	7		RESISTOR 3.6K 5% .125W CC TC=-350/+857	01121	BB3625
A18R3	0698-5178	2		RESISTOR 1.5K 5% .125W CC TC=-350/+857	01121	BB1525
A18R4	0698-5181	7		RESISTOR 3.6K 5% .125W CC TC=-350/+857	01121	BB3625
A18R5	0698-3113	1	1	RESISTOR 100 5% .125W CC TC=-270/+540	01121	BB1015
A18R6	0698-5181	7		RESISTOR 3.6K 5% .125W CC TC=-350/+857	01121	BB3625
A18TP1	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A18U1	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A18U2	1820-1251	6	2	IC CNTR TTL LS DECD ASYNCHRO	01295	SN74LS196N
A18U3	1820-1251	6		IC CNTR TTL LS DECD ASYNCHRO	01295	SN74LS196N
A18U4	1820-1074	1	1	IC DRVR TTL NOR QUAD 2-INP	01295	SN74128N
A18U5	1820-1056	9	1	IC SCHMITT-TRIG TTL NAND QUAD 2-INP	01295	SN74132N
				A18 MISCELLANEOUS PARTS		
	5000-9043	6		PIN,P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6852	3		EXTRACTOR, ORANGE	28480	5040-6852

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A19	05342-60019	6	1	PRIMARY POWER ASSEMBLY (SERIES 1720)	28480	05342-60019
A19C1	0180-2802	6	2	CAPACITOR-FXD 140UF+50-10% 250VDC AL	56289	39D147F250MP4
A19C2	0180-2802	6		CAPACITOR-FXD 140UF+50-10% 250VDC AL	56289	39D147F250MP4
A19C3	0160-2216	4	1	CAPACITOR-FXD 820PF +-5% 300VDC MICA	28480	0160-2216
A19C4	0180-1975	2	2	CAPACITOR-FXD 4UF+50-10% 350VDC AL	56289	39D405F350EE4
A19C5	0180-1975	2		CAPACITOR-FXD 4UF+50-10% 350VDC AL	56289	39D405F350EE4
A19C6	0180-0106	9	2	CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X0006B2
A19C7	0180-0106	9		CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X0006B2
A19CR1	1906-0069	4	1	DIODE-FW BRDG 400V 1A	28480	1906-0069
A19CR2	1990-0543	6	1	OPTO-ISOLATOR LED-PXSTR IF=150MA-MAX	28480	1990-0543
A19DS1	2140-0018	0	2	LAMP-GLOW A9A-C 90/58VDC 700UA T-2-BULB	00466	AG4-C
A19DS2	2140-0018	0		LAMP-GLOW A9A-C 90/58VDC 700UA T-2-BULB	00466	AG4-C
A19Q1	1854-0311	8	2	TRANSISTOR NPN 2N4240 SI TO-66 PD=35W	01928	2N4240
A19Q2	1854-0311	8		TRANSISTOR NPN 2N4240 SI TO-66 PD=35W	01928	2N4240
A19R1	0686-1045	9	3	RESISTOR 100K 5% .5W CC TC=0+882	01121	EB1045
A19R2	0686-1055	1	1	RESISTOR 1M 5% .5W CC TC=0+1000	01121	EB1055
A19R3	0686-1045	9		RESISTOR 100K 5% .5W CC TC=0+882	01121	EB1045
A19R4	0686-1005	1	3	RESISTOR 10 5% .5W CC TC=0+412	01121	EB1005
A19R5	2100-0552	3	1	RESISTOR-TRMR 50 10% C SIDE-ADJ 1-TRN	28480	2100-0552
A19R6	0683-3005	9	1	RESISTOR 30 5% .25W FC TC=-400/+500	01121	CB3005
A19R7	0698-0021	4	1	RESISTOR 3.3 10% .5W CC TC=0+412	01121	EB33G1
A19R8	0813-0001	6	1	RESISTOR 1K 5% 3W PW TC=0+-20	28480	0813-0001
A19R9	0686-1045	9		RESISTOR 100K 5% .5W CC TC=0+882	01121	EB1045
A19R10	0686-1005	1		RESISTOR 10 5% .5W CC TC=0+412	01121	EB1005
A19R11	0686-1005	1		RESISTOR 10 5% .5W CC TC=0+412	01121	EB1005
A19RT1	0839-0006	5	2	THERMISTOR DISC 10-OHM TC=-3.8%/C-DEG	28480	0839-0006
A19RT2	0839-0006	5		THERMISTOR DISC 10-OHM TC=-3.8%/C-DEG	28480	0839-0006
A19RV1	0837-0106	2	2	VARISTOR 150VRMS	28480	0837-0106
A19RV2	0837-0106	2		VARISTOR 150VRMS	28480	0837-0106
A19T1	9100-3066	7	2	TRANSFORMER, POWER	28480	9100-3066
A19T2	9100-3066	7		TRANSFORMER, POWER	28480	9100-3066
A19TP4	1251-0600	0	5	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ SD	28480	1251-0600
A19TP5	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ SD	28480	1251-0600
A19TP6	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ SD	28480	1251-0600
A19TP7	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ SD	28480	1251-0600
A19TP8	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-BZ SD	28480	1251-0600
				A19 MISCELLANEOUS PARTS		
	0380-0342	9	4	STANDOFF-RVT-ON .125-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
	1205-0085	8	2	HEAT SINK TO-66-PKG	28480	1205-0085
	1400-0486	7	3	BRACKET-AFANG .312-LG X .375-LG .312-HD	28480	1400-0486
	1400-0776	8	1	CABLE TIE .01-IN-DIA .19-WD NYL	28480	1400-0776
	7120-1340	6	4	WARNING LABEL	28480	7120-1340
	5000-9043	6	1	PIN(P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6852	3	1	EXTRACTOR, ORANGE	28480	5040-6852
	05342-00019	0	1	SHIELD, PROTECTIVE	28480	05342-00019

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A20	05342-60020	9	1	SECONDARY POWER ASSEMBLY (SERIES 1720)	28480	05342-60020
A20C1	0180-1780	7	2	CAPACITOR-FXD 500UF+75-10% 10VDC AL	56289	39D507G010EJ4
A20C2	0160-0576	5	3	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A20C3	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A20C4	0180-1780	7		CAPACITOR-FXD 500UF+75-10% 10VDC AL	56289	39D507G010EJ4
A20C5	0160-0573	2	1	CAPACITOR-FXD 4700PF +-20% 100VDC CER	28480	0160-0573
A20C6	0180-1746	5	2	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X902082
A20C7	0180-0160	5	2	CAPACITOR-FXD 22UF+-20% 35VDC TA	56289	1500226X0035R2
A20C8	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X902082
A20C9	0180-0160	5		CAPACITOR-FXD 22UF+-20% 35VDC TA	56289	1500226X0035R2
A20C10	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A20C11	0180-0651	9	2	CAPACITOR-FXD 1700UF+75-10% 10VDC AL	09023	UFT-1700-10
A20C12	0180-0651	9		CAPACITOR-FXD 1700UF+75-10% 10VDC AL	09023	UFT-1700-10
A20CR1	1906-0079	6	1	DIODE-FW BRDG 100V 10A	28480	1906-0079
A20CR2	1906-0051	4	1	DIODE-FW BRDG 100V 1A	28480	1906-0051
A20CR3	1901-0784	0	2		28480	1901-0784
A20CR4	1901-0784	0			28480	1901-0784
A20CR5	1902-0522	6	1	DIODE-ZNR 1N5340B 6V 5% PD=5W IR=1UA	04713	1N5340B
A20DS1	1990-0485	5	1	LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A20L1	9100-3065	6	2		28480	9100-3065
A20L2	9140-0250	9	2	COIL 1MH Q=25 .312SDX.9LG-NOM SRF=100KHZ	28480	9140-0250
A20L3	9140-0250	9		COIL 1MH Q=25 .312SDX.9LG-NOM SRF=100KHZ	28480	9140-0250
A20L4	9100-3065	6			28480	9100-3065
A20L5	9140-0249	8	1	COIL 30UH Q=25 .4DX.875LG-NOM SRF=100KHZ	28480	9140-0249
A20Q1	1826-0214	1	1	IC V REGLTR TO-220	04713	MC79I5CT
A20Q2	1826-0106	0	1	IC 7815 V REGLTR TO-220	04713	MC7815CP
A20R1	0683-4305	4	1	RESISTOR 43 5% .25W FC TC=-400/+500	01121	CB4305
A20R2	0686-0271	7	1	RESISTOR 2.7 10% .25W FC TC=-400/+500	01121	CB27G1
A20R3	0683-1015	7	1	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A20T1	9100-3064	5	1	TRANSFORMER, POWER	28480	9100-3064
				A20 MISCELLANEOUS PARTS		
	1205-0219	0	2	HEAT SINK SGL TO-66-PKG	28480	1205-0219
	1251-0600	0	1	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ 30	28480	1251-0600
	3050-0003	3	1	WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
	3050-0082	8	2	WASHER-FL NM NO. 4 .116-IN-ID .188-IN-OD	28480	3050-0082
	5000-9043	6	1	PIN(P.C. BOARD EXTRACTOR	28480	5000-9043
	05342-00012	3	2	HEAT SINK, SOLID	28480	05342-00012
	5040-6852	3	1	EXTRACTOR, ORANGE	28480	5040-6852

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A21	05342-60021	0	1	SWITCH DRIVE ASSEMBLY (SERIES 1804)	28480	05342-60021
A21C1	0180-0229	7	8	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A21C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A21C3	0180-0159	2	2	CAPACITOR-FXD 220UF+-20% 10VDC TA	56289	150D227X0010B2
A21C4	0180-0159	2		CAPACITOR-FXD 220UF+-20% 10VDC TA	56289	150D227X0010B2
A21C5	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A21C6	0180-0210	6	4	CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A21C7	0180-0210	6		CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A21C8	0180-0210	6		CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A21C9	0180-0210	6		CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A21C10	0180-1746	5	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A21C11	0180-1701	2	1	CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A21C12	0180-0197	8	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A21C13	0160-0576	5	2	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A21C14	0180-0491	5	1	CAPACITOR-FXD 10UF+-20% 25VDC TA	28480	0180-0491
A21C15	0180-2373	6	3	CAPACITOR-FXD 580UF+150-10% 35VDC AL	28480	0180-2373
A21C16	0180-2373	6		CAPACITOR-FXD 580UF+150-10% 35VDC AL	28480	0180-2373
A21C17	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A21C18	0160-3878	6	1	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A21C19	0160-0945	2	1	CAPACITOR-FXD 910PF +-5% 100VDC MICA	28480	0160-0945
A21C20	0180-2373	6		CAPACITOR-FXD 580UF+150-10% 35VDC AL	28480	0180-2373
A21C21	0160-0161	9	1	CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
A21C22	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A21CR1	1902-0522	6	2	DIODE-ZNR 1N5340B 6V 5% PD=5W IR=1UA	04713	1N5340B
A21CR2	1906-0096	7	1	DIODE-FW BRDG 200V 2A	04713	MDA202
A21CR3	1902-0522	6		DIODE-ZNR 1N5340B 6V 5% PD=5W IR=1UA	04713	1N5340B
A21CR4	1902-0644	3	1	DIODE-ZNR 1N5363B 30V 5% PD=5W TC=+29MV	28480	1902-0644
A21CR5	1901-0040	1	1	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A21DS1	1990-0486	6	1	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4684
A21L1	9100-2276	9	1	COIL-MLD 100UH 10% Q=50 .095DX.25LG-NOM	28480	9100-2276
A21Q1	1854-0435	9	1	TRANSISTOR NPN SI PD=50W	03508	D44H5
A21Q2	1854-0634	8	1	TRANSISTOR NPN SI PD=1W FT=50MHZ	04713	MPS-U01
A21Q3	1854-0215	1	2	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A21Q4	1853-0326	3	1	TRANSISTOR PNP SI PD=1W FT=50MHZ	28480	1853-0326
A21Q5	1853-0036	2	1	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A21Q6	1853-0363	8	1	TRANSISTOR PNP SI PD=50W	03508	X45H281
A21Q7	1826-0275	4	2	IC 78L12A V RGLTR TO-92	04713	MC78L12ACP
A21Q8	1826-0275	4		IC 78L12A V RGLTR TO-92	04713	MC78L12ACP
A21Q9	1854-0246	8	2	TRANSISTOR NPN SI PD=350MW FT=250MHZ	04713	SPS 233
A21Q10	1853-0058	8	2	TRANSISTOR PNP SI PD=300MW FT=200MHZ	07263	S32248
A21Q11	1854-0246	8		TRANSISTOR NPN SI PD=350MW FT=250MHZ	04713	SPS 233
A21Q12	1853-0058	8		TRANSISTOR PNP SI PD=300MW FT=200MHZ	07263	S32248
A21Q13	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A21R1	0757-0419	0	5	RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A21R2	0757-0417	8	1	RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-562R-F
A21R3	0698-3441	8	3	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A21R4	0757-0419	0		RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A21R5	0757-0419	0		RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A21R6	0698-3155	1	5	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A21R7	0698-5808	5	1	RESISTOR 4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4001-F
A21R8	0698-3444	1	1	RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A21R9	0811-1827	2	2	RESISTOR .1 10% 3W PW TC=0+-90	28480	0811-1827
A21R10	0757-0419	0		RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A21R11	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A21R12	0811-1827	2		RESISTOR .1 10% 3W PW TC=0+-90	28480	0811-1827
A21R13	0757-0346	2	1	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A21R14	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A21R15	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A21R16	0698-0082	7	2	RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
A21R17	2100-3154	7	1	RESISTOR-TRMR 1K 10% C SIDE-ADJ 17-TRN	02111	43P102
A21R18	0757-0465	6	3	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A21R19	0698-0084	9	3	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A21R20	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A21R21	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
A21R22	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A21R23	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A21R24	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A21R25	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A21R26	0698-3150	6	2	RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A21R27	2100-3211	7	1	RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	28480	2100-3211
A21R28	0757-0419	0		RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A21R29	0698-3150	6		RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A21R30	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A21R31	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A21R33	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A21R37	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A21TP1	1251-0600	0	11	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A21TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A21TP3	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A21TP4	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A21U1	1820-0493	6	2	IC OP AMP 8-DIP-P	27014	LM307N
A21U2	1820-0493	6		IC OP AMP 8-DIP-P	27014	LM307N
A21U3	1826-0355	1	1	IC 555 8-DIP-P	28480	1826-0355
A21U4	1826-0428	9	1	IC 3524 MODULATOR 16-DIP-C	01295	SG3524J
				A21 MISCELLANEOUS PARTS		
	1205-0273	6	2	HEAT SINK SGL PLSTC-PWR-PKG	28480	1205-0273
	5000-9043	6	1	PINSP,C, BOARD EXTRACTOR	28480	5000-9043
	5040-6852	3	1	EXTRACTOR, ORANGE	28480	5040-6852

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A22	05342-60022	1	1	MOTHERBOARD ASSEMBLY (SERIES 1720)	28480	05342-60022
A22J1	1200-0785	5	2	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0785
A22J2	1200-0785	5		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0785
A22T1	9100-3067	8	1	TRANSFORMER, POWER	28480	9100-3067
A22W1	05342-60102	8	1	CABLE ASSEMBLY, 1.0 MAG	28480	05342-60102
A22W2	05342-60121	1	1	CABLE ASSEMBLY, LF MB	28480	05342-60121
A22W3	05342-60103	9	1	CABLE ASSEMBLY, IF INT	28480	05342-60103
A22W4	05342-60109	5	1	CABLE ASSEMBLY, MICRO INT	28480	05342-60109
A22W5	05342-60104	0	1	CABLE ASSEMBLY, SHIELD	28480	05342-60104
A22W6	05342-60112	0	1	CABLE ASSEMBLY, SHIELD	28480	05342-60112
A22W7	05342-60111	9	1	CABLE ASSEMBLY, POWER (INCLUDES LINE SWITCH)	28480	05342-60111
A22XA3	1251-1626	2	5	CONNECTOR-PC EDGE 12-CONT/ROW 2-ROWS	28480	1251-1626
A22XA4	1251-2034	8		CONNECTOR-PC EDGE 10-CONT/ROW 2-ROWS	28480	1251-2034
A22XA5	1251-2034	8		CONNECTOR-PC EDGE 10-CONT/ROW 2-ROWS	28480	1251-2034
A22XA6	1251-2034	8		CONNECTOR-PC EDGE 10-CONT/ROW 2-ROWS	28480	1251-2034
A22XA7	1251-1626	2		CONNECTOR-PC EDGE 12-CONT/ROW 2-ROWS	28480	1251-1626
A22XA8	1251-1626	2		CONNECTOR-PC EDGE 12-CONT/ROW 2-ROWS	28480	1251-1626
A22XA9	1251-1626	2		CONNECTOR-PC EDGE 12-CONT/ROW 2-ROWS	28480	1251-1626
A22XA10	1251-1365	6	5	CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A22XA11	1251-1626	2		CONNECTOR-PC EDGE 12-CONT/ROW 2-ROWS	28480	1251-1626
A22XA12	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A22XA13	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A22XA14A	1251-2026	8	6	CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A22XA14B	1251-2026	8		CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A22XA15A	1251-2026	8		CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A22XA15B	1251-2026	8		CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A22XA16	1251-2026	8		CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A22XA16B	1251-2034	8	6	CONNECTOR-PC EDGE 10-CONT/ROW 2-ROWS	28480	1251-2034
A22XA17	1251-2026	8		CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A22XA18	1251-2034	8		CONNECTOR-PC EDGE 10-CONT/ROW 2-ROWS	28480	1251-2034
A22XA19	1251-2582	1	1	CONNECTOR-PC EDGE 24-CONT/ROW 2-ROWS	28480	1251-2582
A22XA20	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A22XA21	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A22XA24	1251-2034	8		CONNECTOR-PC EDGE 10-CONT/ROW 2-ROWS	28480	1251-2034
	0380-0383	8	5	STANDOFF-RVT-ON .125-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
	1251-2205	5	2	POLARIZING KEY-PC EDGE CONN	28480	1251-2205
	5040-0170	6	1	GUIDE;PLUG-IN PC BOARD	28480	5040-0170
A23	0960-0444	2	1	POWER MODULE, UNFILTERED	28480	0960-0444
A24	05341-60047	9	1	10 MHZ OSCILLATOR ASSY (SERIES 1804)	28480	05341-60047
A24C1	0160-2143	6	1	CAPACITOR-FXD 2000PF +80-20% 1KVDC CER	28480	0160-2143
A24C2	0160-0552	9	1	CAPACITOR-FXD 220UF+-20% 10VDC TA	28480	0160-0552
A24L1	9100-2430	7	1	COIL-MLD 220UH 10% Q=55 .156DX.375LG-NOM	28480	9100-2430
A24Y1	0960-0394	1	1	CRYSTAL	28480	0960-0394

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2S	05343-60002	8	1	SECOND PREAMPLIFIER MOTHERBOARD (SERIES 1932)	28480	05343-60002
A2SC1	0160-3879	7	14	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2SC2	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2SC3	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2SC4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2SC5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2SJ1	1250-0257	1	3	CONNECTOR-RF BNC M PC 50-OHM	28480	1250-0257
A2SJ2	1251-2026	8	1	CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS	28480	1251-2026
A2SJ3	1250-0257	1		CONNECTOR-RF BNC M PC 50-OHM	28480	1250-0257
A2SJ4	1250-0257	1		CONNECTOR-RF BNC M PC 50-OHM	28480	1250-0257
A2STP1	0360-1682	0	8	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A2STP2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A2STP3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A2STP4	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A2STP5	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A2A1	05343-60001	7	1	SECOND PREAMPLIFIER (SERIES 1932)	28480	05343-60001
A2A1C1	0180-0418	6	4	CAPACITOR-FXD 1UF+-20% 35VDC TA	28480	0180-0418
A2A1C2	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2A1C3	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2A1C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2A1C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2A1C6	0160-0576	5	1	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A2A1C7	0160-3874	2	1	CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3874
A2A1C8	0180-0418	6		CAPACITOR-FXD 1UF+-20% 35VDC TA	28480	0180-0418
A2A1C9	0180-0418	6		CAPACITOR-FXD 1UF+-20% 35VDC TA	28480	0180-0418
A2A1C10	0180-0418	6		CAPACITOR-FXD 1UF+-20% 35VDC TA	28480	0180-0418
A2A1C11	0160-3875	3	2	CAPACITOR-FXD 22PF +-5% 200VDC CER 0+-30	28480	0160-3875
A2A1C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2A1C13	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2A1C14	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2A1C15	0160-4521	8	1	CAPACITOR-FXD 12PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-120J
A2A1C16	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2A1C17	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2A1C18	0160-3875	3		CAPACITOR-FXD 22PF +-5% 200VDC CER 0+-30	28480	0160-3875
A2A1C19	0121-0445	5	1	CAPACITOR-V TRMR-CER 4.5-20PF 160V	28480	0121-0445
A2A1C20	0160-3878	6	1	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A2A1CR1	1902-0126	6	2	DIODE-ZNR 2.61V 5% DO-7 PD=.4W TC=-.072%	28480	1902-0126
A2A1CR2	1902-0031	2	2	DIODE-ZNR 12.7V 5% DO-7 PD=.4W TC=+.061%	28480	1902-0031
A2A1CR3	1902-0031	2		DIODE-ZNR 12.7V 5% DO-7 PD=.4W TC=+.061%	28480	1902-0031
A2A1CR4	1902-0126	6		DIODE-ZNR 2.61V 5% DO-7 PD=.4W TC=-.072%	28480	1902-0126
A2A1CR5	1901-0347	1	2	DIODE-SCHOTTKY 8V	28480	1901-0347
A2A1CR6	1901-0347	1		DIODE-SCHOTTKY 8V	28480	1901-0347
A2A1D81	1990-0485	5	4	LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A2A1D82	1990-0485	5		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A2A1D83	1990-0485	5		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A2A1D84	1990-0485	5		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A2A1L1	9100-2265	6	4	COIL-MLD 10UH 10% Q=60 .095DX.25LG-NOM	28480	9100-2265
A2A1L2	9100-2247	4	3	COIL-MLD 100NH 10% Q=34 .095DX.25LG-NOM	28480	9100-2247
A2A1L3	9100-2247	4		COIL-MLD 100NH 10% Q=34 .095DX.25LG-NOM	28480	9100-2247
A2A1L4	9100-2265	6		COIL-MLD 10UH 10% Q=60 .095DX.25LG-NOM	28480	9100-2265
A2A1L5	9100-2265	6		COIL-MLD 10UH 10% Q=60 .095DX.25LG-NOM	28480	9100-2265
A2A1L6	9100-2265	6		COIL-MLD 10UH 10% Q=60 .095DX.25LG-NOM	28480	9100-2265
A2A1L7	9100-2247	4		COIL-MLD 100NH 10% Q=34 .095DX.25LG-NOM	28480	9100-2247
A2A1L8	05342-60002	9	2	COIL-3 TURNS	28480	05342-60002
A2A1L9	9100-0346	0	3	COIL-MLD 50NH 20% Q=40 .095DX.25LG-NOM	28480	9100-0346
A2A1L10	9100-0346	0		COIL-MLD 50NH 20% Q=40 .095DX.25LG-NOM	28480	9100-0346
A2A1L11	9100-0346	0		COIL-MLD 50NH 20% Q=40 .095DX.25LG-NOM	28480	9100-0346
A2A1L12	05342-60002	9		COIL-3 TURNS	28480	05342-60002
A2A1R1	0698-7212	9	6	RESISTOR 100 1% .05W F TC=0+-100	24546	C3-1/8-T0-100R-G
A2A1R2	0698-7212	9		RESISTOR 100 1% .05W F TC=0+-100	24546	C3-1/8-T0-100R-G
A2A1R3	0698-7212	9		RESISTOR 100 1% .05W F TC=0+-100	24546	C3-1/8-T0-100R-G
A2A1R4	0698-7212	9		RESISTOR 100 1% .05W F TC=0+-100	24546	C3-1/8-T0-100R-G
A2A1R5	0698-7200	5	3	RESISTOR 31.6 1% .05W F TC=0+-100	24546	C3-1/8-T00-31R6-G
A2A1R6	0698-7205	0	1	RESISTOR 51.1 1% .05W F TC=0+-100	24546	C3-1/8-T00-51R1-G
A2A1R7	2100-3207	1	1	RESISTOR-TRMR 5K 10% C SIDE-ADJ 1-TRN	28480	2100-3207
A2A1R8	0698-7210	1	2	RESISTOR 121 1% .05W F TC=0+-100	24546	C3-1/8-T0-121R-G
A2A1R9	0698-7253	8	1	RESISTOR 5.11K 1% .05W F TC=0+-100	24546	C3-1/8-T0-5111-G
A2A1R10	0698-7200	5		RESISTOR 31.6 1% .05W F TC=0+-100	24546	C3-1/8-T00-31R6-G

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A25A1R11	0698-7212	9		RESISTOR 100 1% .05W F TC=0+-100	24546	C3-1/8-T0-100R-G
A25A1R12	2100-3274	2	1	RESISTOR-TRMR 10K 10% C SIDE-ADJ 1-TRN	28480	2100-3274
A25A1R13	0698-7288	9	1	RESISTOR 147K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1473-G
A25A1R14	0698-7210	7	1	RESISTOR 82.5 1% .05W F TC=0+-100	24546	C3-1/8-T00-82R5-G
A25A1R15	0698-7200	5		RESISTOR 31.6 1% .05W F TC=0+-100	24546	C3-1/8-T00-31R6-G
A25A1R16	0698-7214	1		RESISTOR 121 1% .05W F TC=0+-100	24546	C3-1/8-T0-121R-G
A25A1R17	0698-7212	9		RESISTOR 100 1% .05W F TC=0+-100	24546	C3-1/8-T0-100R-G
A25A1R18	0698-7188	8	1	RESISTOR 10 1% .05W F TC=0+-100	24546	C3-1/8-T00-10R-G
A25A1R19	0698-7215	2	1	RESISTOR 133 1% .05W F TC=0+-100	24546	C3-1/8-T0-133R-G
A25A1R20	0698-8825	2	3	RESISTOR 681K 1% .125W F TC=0+-100	28480	0698-8825
A25A1R21	0698-8825	2		RESISTOR 681K 1% .125W F TC=0+-100	28480	0698-8825
A25A1R22	0698-8825	2		RESISTOR 681K 1% .125W F TC=0+-100	28480	0698-8825
A25A1R23	0698-7229	8	1	RESISTOR 511 1% .05W F TC=0+-100	24546	C3-1/8-T0-511R-G
A25A1TP1	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A25A1TP2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A25A1TP3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A25A1U1	1826-0372	2	2	IC 5 GHZ LIMITER/AMP	28480	1826-0372
A25A1U2	1826-0372	2		IC 5 GHZ LIMITER/AMP	28480	1826-0372
A25A1U3	1826-0065	0	1	IC COMPARATOR PRCN 8-DIP-P	01295	SN72311P
A25A1U8	1820-0054	5	1	IC GATE TTL NAND QUAD 2-INP	01295	SN7400N
				A2541 MISCELLANEOUS PARTS		
	0380-0970	9	1	STANDOFF-HEX .375-IN-LG 4-40THD	28480	0380-0970

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A26	05342-60026	5	1	SAMPLER DRIVER ASSEMBLY (SERIES 2014)	28480	05342-60026
A26C1	0160-4536	5	1	CAPACITOR-FXD 27PF +-5% 500VDC CER	28480	0160-4536
A26C2	0160-3879	7	6	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A26C3	0160-3876	4	2	CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A26C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A26C5	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A26C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A26C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A26C8	0180-1705	4	1	CAPACITOR-FXD 1.5UF+-10% 20VDC TA	56289	150D155X9020A2
A26C9	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A26C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A26C11	0160-0576	5	1	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A26C12	0160-4542	3	1	CAPACITOR-FXD 15PF +-5% 50VDC CER 0+-30	28480	0160-4542
A26C13	0160-4082	6	2	CAPACITOR-FDTHRU 1000PF 20% 200V CER	28480	0160-4082
A26C14	0160-4082	6		CAPACITOR-FDTHRU 1000PF 20% 200V CER	28480	0160-4082
A26CR1	1901-0796	0	1		28480	1901-0796
A26CR2	1901-0179	7	1	DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A26J1	05342-20109	1	1	SUPPORT, CONNECTOR OUTPUT	28480	05342-20109
A26J2	05342-20108	0	1	SUPPORT, CONNECTOR INPUT	28480	05342-20108
A26L1	9100-0346	0	1	COIL-MLD 50NH 20% Q=40 .095DX.25LG-NOM	28480	9100-0346
A26Q1	1854-0071	7	1	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A26R1	0757-0388	8	1	RESISTOR 20 1% .125W F TC=0+-100	19701	MF4C1/8-T0-20R0-F
A26R2	0698-5179	3	1	RESISTOR 1.8K 5% .125W CC TC=-350/+857	01121	BB1825
A26R3	0698-7101	5	1	RESISTOR 3K 5% .125W CC TC=-350/+857	01121	BB3025
A26R4	0757-0180	2	1	RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A26R5	0698-3111	9	1	RESISTOR 30 5% .125W CC TC=-270/+540	01121	BB3005
A26R6	0698-4132	6	1	RESISTOR 62 5% .125W CC TC=-270/+540	01121	BB6205
A26R7	0698-6648	3	1	RESISTOR 620 5% .125W CC TC=-330/+800	01121	BB6215
A26R8	0698-3437	2	1	RESISTOR 133 1% .125W F TC=0+-100	24546	C4-1/8-T0-133R-F
A26TP1	0360-1682	0	2	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A26TP2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
A26U1	1858-0060	2	1	TRANSISTOR, ARRAY	28480	1858-0060
A26W1	05342-20107	9	1	CABLE, COAX, OUTPUT	28480	05342-20107
				A26 MISCELLANEOUS PARTS		
	0380-0486	2	2	SPACER-RND .5-IN-LG .086-IN-ID	28480	0380-0486
	0520-0127	6	2	SCREW-MACH 2-56 .188-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	0570-0007	6	2	SCREW-MACH 0-80 .188-IN-LG FIL-HD-SLT	00000	ORDER BY DESCRIPTION
	0570-0024	7	1	SCREW-MACH 0-80 .25-IN-LG FIL-HD-SLT	00000	ORDER BY DESCRIPTION
	1205-0011	0	1	HEAT SINK TO-5/TO-39-PKG	28480	1205-0011
	1250-0901	2	1	CONNECTOR-RF SMB M SGL-HOLE-FR 50-OHM	28480	1250-0901
	1250-1353	0	1	CONNECTOR-RF SMA M UNMTD 50-OHM	28480	1250-1353
	05342-00009	8	1	CONTACT, DIODE	28480	05342-00009
	05342-00011	2	1	HOUSING, SAMPLER DRIVER	28480	05342-00011
	05342-00013	4	1	COVER, SAMPLER DRIVER	28480	05342-00013
	05342-00016	7	1	HEAT SINK, SILICONE	28480	05342-00016
	05342-40001	4	1	DIODE HOLDER	28480	05342-40001

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A28	05343-60003	0	1	FIRST PREAMPLIFIER (SERIES 1932)	28480	05343-60003
A28C1	0160-3879	7	8	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A28C2	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A28C3	0180-0418	6	2	CAPACITOR-FXD 1UF+-20% 35VDC TA	28480	0180-0418
A28C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A28C5	0180-0418	6		CAPACITOR-FXD 1UF+-20% 35VDC TA	28480	0180-0418
A28C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A28C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A28C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A28C9	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A28C10	0160-0576	5	1	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A28C11	0160-4494	4	1	CAPACITOR-FXD 39PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-390J
A28C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A28C13	0160-4082	6	2	CAPACITOR-FDTHRU 1000PF 20% 200V CER	28480	0160-4082
A28C14	0160-4082	6		CAPACITOR-FDTHRU 1000PF 20% 200V CER	28480	0160-4082
A28CR1	1902-3082	9	1	DIODE-ZNR 4.64V 5% DO-7 PD=.4W TC=-.023%	28480	1902-3082
A28J1	1200-0847	8	1	SOCKET-XSTR 3-CONT TO-18 DIP-SLDR	28480	1200-0847
A28J2	1250-0901	2	1	CONNECTOR-RF SMB M SGL-HOLE-FR 50-OHM	28480	1250-0901
A28L1	9100-0346	0	1	COIL-MLD 50NH 20% Q=40 .095D%.25LG-NOM	28480	9100-0346
A28Q1	1854-0591	6	2	TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-90
A28Q2	1854-0591	6		TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-90
A28R1	0698-7229	8	1	RESISTOR 511 1% .05W F TC=0+-100	24546	C3-1/8-T0-511R-G
A28R2	0698-7188	8	1	RESISTOR 10 1% .05W F TC=0+-100	24546	C3-1/8-T00-10R-G
A28R3	0698-7236	7	1	RESISTOR 1K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1001-G
A28R4	0698-7212	9	1	RESISTOR 100 1% .05W F TC=0+-100	24546	C3-1/8-T0-100R-G
A28R5	0698-7230	1	2	RESISTOR 562 1% .05W F TC=0+-100	24546	C3-1/8-T0-562R-G
A28R6	0698-7224	3	2	RESISTOR 316 1% .05W F TC=0+-100	24546	C3-1/8-T0-316R-G
A28R7	0698-7241	4	1	RESISTOR 1.62K 1% .05W F TC=0+-100	28480	0698-7241
A28R8	0698-7223	2	1	RESISTOR 287 1% .05W F TC=0+-100	24546	C3-1/8-T0-287R-G
A28R9	05342-60004	1	4	RESISTOR-MODIFIED	28480	05342-60004
A28R10	05342-60004	1		RESISTOR-MODIFIED	28480	05342-60004
A28R11	0698-7246	9	1	RESISTOR 2.61K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2611-G
A28R12	05342-60004	1		RESISTOR-MODIFIED	28480	05342-60004
A28R13	05342-60004	1		RESISTOR-MODIFIED	28480	05342-60004
A28R14	0698-7244	7	1	RESISTOR 2.15K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2151-G
A28R15	0698-7224	3		RESISTOR 316 1% .05W F TC=0+-100	24546	C3-1/8-T0-316R-G
A28R16	0698-7230	1		RESISTOR 562 1% .05W F TC=0+-100	24546	C3-1/8-T0-562R-G
A28R17	0698-7234	9	1	RESISTOR 825 1% .05W F TC=0+-100	24546	C3-1/8-T0-825R-G
				A28 MISCELLANEOUS PARTS		
	0380-0486	2	2	SPACER-RND .5-IN-LG .086-IN-ID	28480	0380-0486
	05342-20109	1	1	SUPPORT-CONNECTOR INPUT	28480	05342-20109
	05343-00002	2	1	HOUSING-PREAMPLIFIER	28480	05343-00002
	05343-00005	5	1	PANEL-FRONT	28480	05343-00005
	05343-20205	9	1	SHELL-CONNECTOR	28480	05343-20205

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS		
B1	3160-0209	4	1	FAN-TBAX 32-CFM 105-125V 50/60-HZ	23936	8500C
F1	2110-0360	2	1	FUSE .75A 250V 1.25X.25 UL	75915	313.750
F1	2110-0421	6	1	FUSE .375A 250V 1.25X.25 UL	75915	313.375
F2	2110-0301	1	1	FUSE .125A 125V .281X.093	28480	2110-0301
FL1	9135-0042	6	1	FILTER-LINE WIRE LEAD-TERMS	28480	9135-0042
J1	05305-60205	7	1	CONNECTOR ASSEMBLY-BNC	28480	05305-60205
J2	1250-0083	1	4	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
J3	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
J4	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
J5	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
J6	1250-0829	3	2	CONNECTOR-RF SMC M SGL-HOLE-FR 50-OHM	28480	1250-0829
J7	1250-0829	3		CONNECTOR-RF SMC M SGL-HOLE-FR 50-OHM	28480	1250-0829
MP1	05343-20206	0	1	FRAME-FRONT	28480	05343-20206
MP2	5020-8816	1	1	CASTING, REAR FRAME	28480	5020-8816
MP3	5020-8837	6	2	STRUT-CORNER	28480	5020-8837
MP4	5001-0423	0	1	TOP COVER	28480	50001-0423
MP5	5061-1940	4	1	COVER-BOTTOM	28480	5061-1940
MP6	05343-00004	4	1	PANEL-REAR	28480	05343-00004
MP7	4040-1610	0	1	FRONT PANEL	28480	4040-1610
MP8	05342-20105	7	1	HOUSING-MAIN	28480	05342-20105
MP9	5001-0439	8	1	TRIM-STRIP, SIDE	28480	5001-0439
MP11	5000-7201	8	4	FOOT(STANDARD)	28480	5040-7201
MP12	5040-7203	0	1	TRIM-TOP 1/2	28480	5040-7203
MP13	05343-00003	3	1	PANEL-SUB	28480	05343-00003
MP14	05342-00001	2	1	COVER-CASTING	28480	05342-00001
MP16	05342-00004	3	1	SHIELD-PROTECTIVE	28480	05342-00004
MP17	05342-00005	4	1	SHIELD-RFI	28480	05342-00005
MP18	05342-00008	7	2	BRACKET-MOTHER BOARD	28480	05342-00008
MP19	05342-00010	1	1	PLATE-PATCH	28480	05342-00010
P1	1251-4735	0	1	CONNECTOR 42-PIN PRESSURE TYPE	28480	1251-4735
S2	3103-0056	9	1	SWITCH-THRM FXD +167F 15A OPN-ON-RISE	28480	3103-0056
S3	3101-1327	5	1	SWITCH-SL DPST MINTR .5A 125VAC/DC	28480	3101-1327
S4	3101-2306	2	1	SWITCH-SL DPDT STD .5A 125VAC/DC	28480	3101-2306
U1	5088-7045	8	1	SAMPLER	28480	5088-7045
W1	8120-1378	1	1	CABLE ASSY 18AWG 3-CNDCT JGK-JKT	28480	8120-1378
W2	8120-0664	6	1	CABLE ASSEMBLY	28480	8120-0664
W3	05342-60105	1	1	CABLE ASSEMBLY-IF EXTERNAL	28480	05342-60105
				MISCELLANEOUS PARTS		
	0360-0053	7	2	TERMINAL-SLDR LUG LK-MTG FOR-#10-SCR	28480	0360-0053
	0370-1005	2	1	KNOB-BASE-PTR 3/8 JGK .125-IN-ID	28480	0370-1005
	0510-0592	8	3	RETAINER-PUSH ON TUB EXT .14-IN-DIA	28480	0510-0592
	0520-0139	0	2	SCREW-MACH 2-56 .875-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	0624-0078	6	2	SCREW-TPG 6-32 .375-IN-LG PAN-HD-POZI	28480	[illegible]-0078
	1400-0015	8	3	CLAMP-CABLE .25-DIA .375-WD STL	28480	1400-[illegible]
	1400-0053	4	1	CLAMP-CABLE .172-DIA .375-WD NYL	28480	1400-0053
	1400-0985	1	1	CLAMP-CABLE POLYP	06383	FCM2-A-20
	1460-1345	5	2	TILT STAND SST	28480	1460-1345
	2680-0172	1	2	SCREW-MACH 10-32 .375-IN-LG 100 DEG	28480	2680-0172
	3050-0050	0	1	WASHER-FL MTLC 7/16 IN .5-IN-ID	28480	3050-0050
	5040-7219	8	1	STRAP, HANDLE, CAP-FRONT	28480	5040-7219
	5040-7220	1	1	STRAP, HANDLE, CAP-REAR	28480	5040-7220
	5060-9804	3	1	STRAP, HANDLE, ASSY	28480	5060-9804
	05343-00001	1	1	PLATE-MOUNTING	28480	05343-00001
	05343-20202	6	1	SUPPORT-MTG PLATE	28480	05343-20202
	05343-20203	7	1	SPACER-THREADED	28480	05343-20203
	05343-20204	8	1	COLLAR-CONNECTOR	28480	05343-20204
	05343-20211	7	1	NUT-BODY	28480	05343-20211

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-4. Option 001 Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A24	10544-60011	3	1	CRYSTAL OSCILLATOR ASSEMBLY	28480	10544-60011

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-5. Option 004 Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	05343-60008	4	1	OPTION 004 = (OAC) DISPLAY DRIVER (SERIES 1932)	28480	05343-60008
A2C1	0180-0106	9	1	CAPACITOR-FXD 600UF+-20% 6VDC TA	56289	150D606X0006B2
A2C2	0180-0230	0	4	CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A2C3	0160-3879	7	13	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C5	0180-1743	2	1	CAPACITOR-FXD .1UF+-10% 35VDC TA	56289	150D104X9035A2
A2C6	0160-3878	6	2	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A2C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C9	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C10	0160-0570	9	1	CAPACITOR-FXD 220PF +-20% 100VDC CER	20932	5024EM100RD221M
A2C11	0160-0571	0	1	CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A2C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C13	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C14	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C15	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C16	0180-1714	7	1	CAPACITOR-FXD 330UF+-10% 6VDC TA	56289	150D337X9006B2
A2C17	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C18	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C19	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A2C20	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A2C21	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C22	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C23	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A2C24	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A2J3	1250-0835	1	1	CONNECTOR-RF SMC M PC 50-OHM	28480	1250-0835
A2Q1	1854-0560	9	1	TRANSISTOR NPN SI DARL PD=310MW	04713	MPS A12
A2R1	0757-0420	3	1	RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A2R3	0683-4725	2	10	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R4	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R5	1810-0279	5	2	NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
A2R6	0757-0390	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A2R7	0698-3430	5	8	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R8	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R9	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R10	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R11	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R12	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R13	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R14	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A2R15	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R16	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
A2R17	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R18	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R19	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A2R20	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R21	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R22	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R23	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R24	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R25	2100-2655	1	2	RESISTOR-TRMR 100K 10% C TOP-ADJ 1-TRN	73138	82PR100K
A2R26	2100-2655	1		RESISTOR-TRMR 100K 10% C TOP-ADJ 1-TRN	73138	82PR100K
A2R27	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R28	0757-0442	9	1	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R29	0698-3243	8	2	RESISTOR 178K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1783-F
A2R30	0698-3243	8		RESISTOR 178K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1783-F
A2R31	0698-3455	4	2	RESISTOR 261K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2613-F
A2R32	0698-3455	4		RESISTOR 261K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2613-F
A2R33	0698-3153	9	1	RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A2R34	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A2TP1	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-85C-BZ BQ	28480	1251-0600
A2TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-85C-BZ BQ	28480	1251-0600
A2TP3	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-85C-BZ BQ	28480	1251-0600
A2TP4	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-85C-BZ BQ	28480	1251-0600
A2TP5	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-85C-BZ BQ	28480	1251-0600
A2TP6	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-85C-BZ BQ	28480	1251-0600
A2TP15*	1251-0600	0	8	CONNECTOR-SGL CONT PIN 1.14-MM-85C-BZ BQ	28480	1251-0600
A2TP15-	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-85C-BZ BQ	28480	1251-0600
A2U1	1820-0539	1	2	IC GFR TTL NAND QUAD 2-INP	01295	SN7437N
A2U2	1820-0468	5	2	IC DCDR TTL BCD-TO-DEC 4-TO-10-LINE	01295	SN7445N

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-5. Option 004 Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2U3	1820-1443	8	1	IC CNTR TTL LS BIN ASYNCHRO	01295	SN74LS293N
A2U4	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A2U5	1820-1049	0	1	IC BFR TTL NON-INV HEX	01295	SN74367N
A2U6	1820-0539	1		IC BFR TTL NAND QUAD 2-INP	01295	SN7437N
A2U7	1820-0628	9	2	IC TTL 64-BIT RAM 60-NS 0-C	01295	SN7489N
A2U8	1820-0468	5		IC DCDR TTL BCD-TO-DEC 4-TO-10-LINE	01295	SN7445N
A2U9	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A2U10	1820-1200	5	1	IC INV TTL LS HEX	01295	SN74LS05N
A2U11	1820-0515	3	1	IC MV TTL MONOSTBL RETRIG/RESET DUAL	04713	MC6602P
A2U12	1820-0628	9		IC TTL 64-BIT RAM 60-NS 0-C	01295	SN7489N
A2U13	1820-1254	9	2	IC BFR TTL NON-INV HEX 1-INP	27014	DM8095N
A2U14	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A2U15	1820-1194	6	3	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
A2U16	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A2U17	1820-1254	9		IC BFR TTL NON-INV HEX 1-INP	27014	DM8095N
A2U18	1820-1428	9	1	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
A2U19	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A2U20	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A2U21	1820-1194	6		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
A2U22	1820-1194	6		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
A2U23	1820-1865	2	1	IC RGTR TTL LS D-TYPE QUAD	27014	DM74LS173N
A2U24	1813-0092	6	1	IC CONV 12-B-D/A 24-DIP-C	8E175	DAC80-CCD-V
A2W1	8159-0005	0	1	WIRE 22AWG W PVC 1X22 80C	28480	8159-0005
A2XU1	1200-0565	9	2	SOCKET-IC 24-CONT DIP-SLDR	28480	1200-0565
A2XU24	1200-0565	9		SOCKET-IC 24-CONT DIP-SLDR	28480	1200-0565

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-6. Option 011 Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A15	05342-60015	2	1	HP-IB ASSEMBLY (SERIES 1720)	28480	05342-60015
A15C1	0160-3879	7	11	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A15C2	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A15C3	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A15C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A15C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A15C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A15C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A15C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A15C9	0160-0106	9	1	CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X0006B2
A15C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A15C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A15C13	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A15L1	9100-1788	6	1	CHOKE-WIDE BAND ZMAX=680 OHM@ 180 MHZ	02114	VK200 20/4B
A15R1	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A15R2	1810-0164	7	3	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0164
A15R3	1810-0164	7		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0164
A15R4	1810-0164	7		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0164
	0360-0124	3	2	CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
	0360-0124	3		CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
A15U1	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A15U2	1820-1144	6	4	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A15U3	1820-1112	8	8	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A15U4	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A15U5	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A15U6	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A15U7	1820-1211	8	1	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A15U8	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A15U9	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A15U10	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A15U11	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A15U12	1820-1206	1	1	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
A15U13	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A15U14	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A15U15	1820-0578	4	1	IC RGTR TTL D-TYPE 4-BIT	01295	SN74173N
A15U16	1820-1196	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A15U17	1820-1198	0	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
A15U18	1820-1368	6	2	IC DRVR TTL BUS DRVR HEX 1-INP	01295	SN74366N
A15U19	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A15U20	1820-1262	3	2	IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109N
A15U21	1820-1997	7	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	34335	SN74LS374PC
A15U22	1820-1689	4	4	IC MISC QUAD	04713	MC3446P
A15U23	1816-1154	9	1	ROM 32 X 8 OC	01295	SN74S188N PROGRAMMED
	1200-0473	6	2	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0473
A15U24	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	34335	SN74LS374PC
A15U25	1820-1689	4		IC MISC QUAD	04713	MC3446P
A15U26	1816-1155	0	1	ROM 32 X 8 OC	01295	SN74S188N PROGRAMMED
	1200-0473	6		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0473
A15U27	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	34335	SN74LS374PC
A15U28	1820-1689	4		IC MISC QUAD	04713	MC3446P
A15U29	1820-1262	3		IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109N
A15U30	1820-1368	6		IC DRVR TTL BUS DRVR HEX 1-INP	01295	SN74366N
A15U31	1820-1689	4		IC MISC QUAD	04713	MC3446P
A15U32	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A15U33	1820-0908	4	1	IC COMPTR TTL L MAGTD 5-BIT	07263	93L24PC
A15U34	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A15U35	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A15U36	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
	5000-9043	6	1	PIN:P.C. BOARD EXTRACTOR	28480	5000-9043
	5040-6852	3	1	EXTRACTOR, ORANGE	28480	5040-6852
A29	05342-60029	8	1	HP-IB INPUT ASSEMBLY (SERIES 1720)	28480	05342-60029
A29J1	1251-3283	1	1	CONNECTOR 24-PIN F MICRORIBBON	28480	1251-3283
A29J2	1200-0485	2	1	SKT-IC,14 PIN; PC MTG; RT ANGL; CONT	28480	1200-0485
A29S1	3101-1973	7	1	SWITCH-SL 7-14-NS DIP-SLIDE-ASSY .14	28480	3101-1973
A29W5	8120-1966	3	1	CABLE ASSY 26AWG 24-CNDCT	28480	8120-1966
				A29 MISCELLANEOUS PARTS		
	0380-0644	4	2	STANDOFF-METRIC SHORT STUD MOUNT; FOR	28480	0380-0644
	1530-1098	4	2	CLEVIS 0.070-IN W SLT; 0.456-IN PIN CTR	00000	ORDER BY DESCRIPTION
	2190-0034	5	2	WASHER-LK HLCL NO. 10 .194-IN-ID	28480	2190-0034
	05342-00017	8	1	PLATE, PATCH	28480	05342-00017

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-7. Manufacturers Code List

MFR. NO.	MANUFACTURER NAME AND ADDRESS	ZIP CODE
00000	Any Satisfactory Supplier	
01121	Allen-Bradley Company, Milwaukee, WI	53204
01295	Texas Instrument Inc., Semiconductor Component Division, Dallas, TX	75222
02114	Ferroxcube Corporation, Saugerties, NY	12477
03888	KDI Pyrofilm Corporation, Whippany, NJ	07981
04713	Motorola Semiconductor Products, Phoenix, AZ	85062
06383	Panduit Corporation, Tinley Park, IL	60477
16546	U. S. Capacitor Corporation, Burbank, CA	91504
20932	EMCON Division ITW, San Diego, CA	92129
23936	Pamotor Division, William J. Purdy, Burlingame, CA	94010
24546	Corning Glass Works (Bradford Division), Bradford, PA	16701
25088	Siemens Corporation, Iselin, NJ	08830
25403	Amperex Elek Corporation, Semicon. & MC Division, Slatersville, RI	02876
27014	National Semiconductor Corporation, Santa Clara, CA	95051
28480	Hewlett-Packard Company Corporate Headquarters, Palo Alto, CA	94304
30983	Mepco/Electra Corporation, San Diego, CA	92121
34335	Advanced Micro Devices, Incorporated, Sunnyvale, CA	94086
50088	Mostek Corporation, Carrollton, TX	75006
51642	Centre Engineering Incorporated, State College, PA	16801
56289	Sprague Electric Company, North Adams, MA	01247
73138	Beckman Instruments Incorporated, Helipot Division, Fullerton, CA	92634
75915	Littelfuse, Incorporated, Del Plaines, IL	60016
8E175	Burr Brown Company, Huntsville, AL	35801
90201	Mallory Capacitor Company, Indianapolis, IN	46206

SECTION VII
MANUAL CHANGES

7-1. INTRODUCTION

7-2. This section contains information necessary to adapt this manual to apply to newer instruments.

7-3. MANUAL CHANGES

7-4. This manual applies directly to Model 5343A Microwave Frequency Counters with serial number prefix 2014A and below.

7-5. As engineering changes are made, newer instruments may have serial prefix numbers higher than those listed on the title page of this manual. The manuals for these instruments will be supplied with MANUAL CHANGES sheets containing the required information. Replace affected pages or modify existing manual information as directed in the MANUAL CHANGES pages. Contact the nearest Hewlett-Packard Sales and Service Office if the change information is missing.

SECTION VIII
SERVICE

8-1. INTRODUCTION

8-2. This section provides service information and symbol descriptions, theory of operation, troubleshooting procedures, and schematic diagrams. The arrangement of content of this section is described in detail below. Refer to the Table of Contents for specific page and paragraph numbers.

a. **Schematic Diagram Symbols and Reference Designations.** Describes the symbols used on schematic diagrams and reference designators used for parts, subassemblies and assemblies.

b. **Identification Markings.** Describes the method used by Hewlett-Packard for identifying printed-circuit boards and assemblies.

c. **Safety Considerations.** Describes the safety considerations applicable during maintenance, adjustments, and repair.

d. **Signal Names.** Lists signal mnemonics, names, source, destination, and function for 5343A signals.

e. **Disassembly and Reassembly Procedures.** Describes removal of covers, front frame, assemblies to gain access to parts.

f. **Factory Selected Components.** Lists procedures for replacement of parts whose values are selected at time of manufacture for optimum performance.

g. **Service Accessory Kit 10842A.** Describes the use and function of kit (extender boards) used for testing pc boards.

h. **Logic Symbols.** Description of logic symbols used on schematics.

i. **Theory of Operation.** Includes block diagram description of overall operation, special function descriptions, and detailed circuit operation explanations.

j. **Assembly Locations.** Describes and illustrates location of assemblies, adjustments, front and rear panel components by reference designators.

k. **Troubleshooting Procedures.** Provides troubleshooting techniques, recommended test equipment, and troubleshooting tables arranged to isolate trouble to an assembly and then to the component level.

l. **Schematic Diagrams.** A diagram for each assembly is included, arranged in order of assembly number. A component locator photo is included adjacent to each diagram. The schematic diagrams contain tables of reference designations, tables of active elements (by part number), voltage measurements and signature analyzer signatures, where applicable.

8-3. SCHEMATIC DIAGRAM SYMBOLS AND REFERENCE DESIGNATORS

8-4. *Figure 8-1* shows the symbols used on the schematic diagrams. At the bottom of *Figure 8-1*, the system for reference designators, assemblies, and subassemblies is shown.

8-5. Reference Designations

8-6. Assemblies such as printed-circuits are assigned numbers in sequence, A1, A2, etc. As shown in *Figure 8-1*, subassemblies within an assembly are given a subordinate A number. For example, rectifier subassembly A1 has the complete designator of A25A1. For individual components, the complete designator is determined by adding the assembly number and subassembly number if any. For example, CR1 on the rectifier assembly is designated A25A1CR1.

8-7. IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS

8-8. HP printed-circuit boards (see *Figure 8-1*) have four identification numbers: an assembly part number, a series number, a revision letter, and a production code.

8-9. The assembly part number has 10 digits (such as 05343–60001) and is the primary identification. All assemblies with the same part number are interchangeable. When a production change is made on an assembly that makes it incompatible with previous assemblies, a change in part number is required. The series number (such as 1936A) is used to document minor electrical changes. As changes are made, the series number is incremented. When replacement boards are ordered, you may receive a replacement with a different series number. If there is a difference between the series number marked on the board and the schematic in this manual, a minor electrical difference exists. If the number on the printed-circuit board is lower than that on the schematic, refer to Section VII for backdating information. If it is higher, refer to the looseleaf manual change sheets for this manual. If the manual change sheets are missing, contact your local Hewlett-Packard Sales and Service Office. See the listing on the back cover of this manual.

8-10. Revision letters (A, B, etc.) denote changes in printed-circuit layout. For example, if a capacitor type is changed (electrical value may remain the same) and requires different spacing for its leads, the printed-circuit board layout is changed and the revision letter is incremented to the next letter. When a revision letter changes the series number is also usually changed. The production code is the four-digit seven-segment number used for production purposes.

SYMBOLS

DANGEROUS VOLTAGE, EXCEEDS 1000 VOLTS

FRONT PANEL LABEL

REAR PANEL LABEL

INTERIOR AND PC BOARDS LABEL

WIPER MOVES TOWARD "CW" WHEN CONTROL IS ROTATED CLOCKWISE

OR PROTECTIVE CONDUCTOR TERMINAL

CIRCUIT COMMON

IDENTIFIED COMMON

OR CHASSIS TERMINAL

KNOB CONTROL

SCREWDRIVER ADJUST

MAIN SIGNAL PATH

FEEDBACK PATH

OR OR TEST POINT

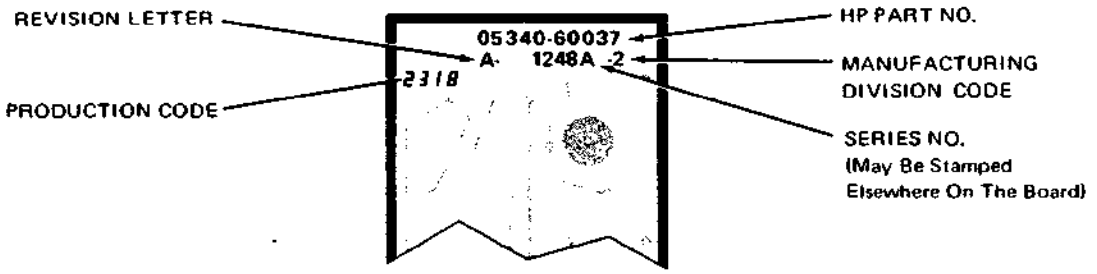
INSTRUCTION MANUAL REFERENCE

ALTERNATING CURRENT

DIRECT CURRENT

ALTERNATING OR DIRECT CURRENT

PRINTED CIRCUIT BOARD IDENTIFICATION



REFERENCE DESIGNATIONS

REFERENCE DESIGNATIONS WITHIN ASSEMBLIES ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION. JACKS ARE THE STATIONARY CONNECTORS AND PLUGS ARE THE MORE MOVEABLE OF TWO CONNECTORS.

ASSEMBLY	ABBREVIATION	COMPLETE DESCRIPTION
A25	C1	A25C1
A25A1	CR1	A25A1CR1
NO PREFIX	J3	J3

EXAMPLE ONLY

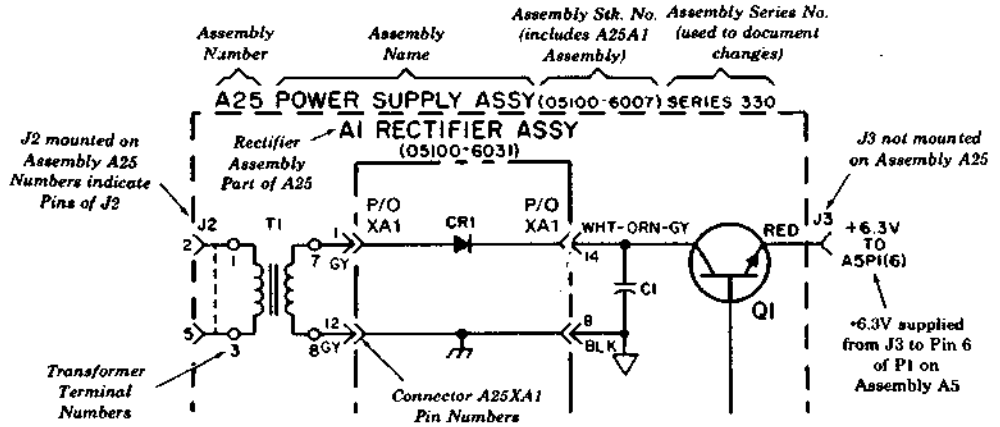


Figure 8-1. Schematic Diagram Notes

8-11. Assembly Identification

8-12. The assembly number, name and Hewlett-Packard part number of 5343A assemblies are listed in *Table 8-1*.

NOTE

Some assemblies in the 5343A are identical with those in the 5342A. Pay particular attention to the HP Part Number listed below, i.e., 05342- or 05343-.

Table 8-1. Assembly Identification

ASSEMBLY	NAME	HP PART NO.
A1	Keyboard Display	05343-60004
A2	Display Driver	05343-60005
A2	Option 004 (DAC) Display Driver	05343-60008
A3	Direct Count Amplifier	05342-60003
A4	Offset VCO	05342-60004
A5	RF Multiplexer	05342-60005
A6	Offset Loop Amplifier	05342-60006
A7	Mixer/Search Control	05342-60007
A8	Main VCO	05342-60008
A9	Main Loop Amplifier	05342-60009
A10	Divide-by-N	05342-60010
A11	IF Limiter	05342-60011
A12	IF Detector	05343-60009
A13	Counter	05342-60013
A14	Processor	05343-60006
A15	Option 011 HP-IB	05342-60015
A16	Memory and Sweeper Control	05343-60010
A17	Timing Generator	05343-60007
A18	Time Base Buffer	05342-60018
A19	Primary Power	05342-60019
A20	Secondary Power	05342-60020
A21	Switch Drive	05342-60021
A22	Motherboard	05342-60022
A23	Power Module	05342-60023
A24	Oscillator	05341-60047
A24	Option 001 Oscillator	10544-60011
A25	2nd Preamplifier Motherboard	05343-60002
A25A1	2nd Preamplifier	05343-60001
A26	Sampler Driver	05342-60026
U1	Sampler	5088-7022
A27	NOT USED	
A28	1st Preamplifier	05343-60003
A29	Option 011 HP-IB Interconnection	05342-60029

8-13. SAFETY CONSIDERATIONS

8-14. Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition. Service and adjustments should be performed only by service-trained personnel.

WARNING

ANY INTERRUPTION OF THE PROTECTIVE (GROUNDING) CONDUCTOR (INSIDE OR OUTSIDE THE INSTRUMENT) OR DISCONNECTION OF THE PROTECTIVE EARTH TERMINAL IS LIKELY TO MAKE THE INSTRUMENT DANGEROUS. INTENTIONAL INTERRUPTION IS PROHIBITED.

8-15. Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

8-16. Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

8-17. Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuseholders must be avoided.

WARNING

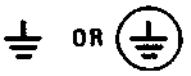
PRIOR TO MAKING ANY VOLTAGE TESTS ON THE A19 PRIMARY POWER ASSEMBLY, THE VOLTMETER TO BE USED OR THE 5343A MUST BE ISOLATED FROM THE POWER MAINS BY USE OF AN ISOLATION TRANSFORMER. A TRANSFORMER SUCH AS AN ALLIED ELECTRONICS, 705-0165 (120V AC) MAY BE USED FOR THIS PURPOSE. CONNECT THE TRANSFORMER BETWEEN THE AC POWER SOURCE AND THE POWER INPUT TO THE 5343A.

8-18. Safety Symbols

8-19. The following safety symbols are used on equipment and in manuals:

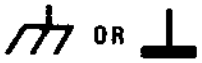
Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with the symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.



Frame and chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).

Direct current (power line).

Alternating or direct current (power line).

WARNING

The WARNING signal denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which is not correctly performed or adhered to, could result in damage to or destruction of part all of the product.

8-20. SIGNAL NAMES

8-21. *Table 8-2* is a list of signal names used in the 5343A. The list is in alphabetical order and includes the mnemonics for cross-reference with the schematic diagram signal names. A description of the function of each signal and the source and destination is included in the table.

Table 8-2. Signal Names

MNEMONIC	NAME	FROM	TO	FUNCTION
A0	Address 0	XA14A($\overline{3}$)	XA13($\overline{1}$), XA15A($\overline{3}$), XA16A($\overline{3}$), A22W4(5), A22J1(24)	Address Lines
A1	Address 1	XA14A($\overline{4}$)	XA13($\overline{2}$), XA15A($\overline{4}$), XA16A($\overline{4}$), A22W4(6), A22J1(23)	
A2	Address 2	XA14A($\overline{5}$)	XA13($\overline{3}$), XA15A($\overline{5}$), XA16A($\overline{5}$), A22W4(9), A22J1(22)	
A3	Address 3	XA14A($\overline{6}$)	XA13A($\overline{4}$), XA15A($\overline{6}$), XA16A($\overline{6}$), A22W4(10), A22J1(10)	
A4	Address 4	XA14A($\overline{7}$)	XA13($\overline{5}$), XA15A($\overline{7}$), XA16A($\overline{7}$), A22W4($\overline{17}$)	
A5	Address 5	XA14A($\overline{8}$)	XA13($\overline{6}$), XA15A($\overline{8}$), XA16A($\overline{8}$), A22W4($\overline{18}$)	
A6	Address 6	XA14A($\overline{9}$)	XA15A($\overline{9}$), XA16A($\overline{9}$), A22W4(19)	
A7	Address 7	XA14A($\overline{10}$)	XA15A($\overline{10}$), XA16A($\overline{10}$), A22W4(20)	
A8	Address 8	XA14A($\overline{11}$)	XA15A($\overline{11}$), XA16A($\overline{11}$), A22W4(33)	
A9	Address 9	XA14A($\overline{12}$)	XA15A($\overline{12}$), XA16A($\overline{12}$), A22W4(34)	
A10	Address 10	XA14A($\overline{13}$)	XA15A($\overline{13}$), XA16A($\overline{13}$), A22W4(35)	
A11	Address 11	XA14A($\overline{14}$)	XA15A($\overline{14}$), XA16A($\overline{14}$), A22W4(36)	
A12	Address 12	XA14A($\overline{15}$)	XA15A($\overline{15}$), XA16A($\overline{15}$), A22W4(37)	
A13	Address 13	XA14A($\overline{16}$)	XA15A($\overline{16}$), XA16A($\overline{16}$), A22W4(38)	
A14	Address 14	XA14A($\overline{17}$)	XA15A($\overline{17}$), XA16A($\overline{17}$), A22W4(39)	
A15	Address 15	XA14A($\overline{18}$)	XA15A($\overline{18}$), XA16A($\overline{18}$) A22W4(40)	
CHECK	Check Output	XA10($\overline{11}$)	XA11(7, $\overline{7}$)	75 MHz signal sent from A10 Divide-by-N to A11 IF Limiter when 5343A is in CHECK mode.
DIRECT A	Direct Count A Output	XA3(2)	XA13($\overline{7}$)	Divide-by-two output of Direct Count Amplifier Assembly to A13 Counter Assembly.
DIRECT B	Direct Count B Output	XA3($\overline{1}$)	XA13(14)	Divide-by-four output of Direct Count Amplifier Assembly to A13 Counter Assembly.

Table 8-2. Signal Names (Continued)

MNEMONIC	NAME	FROM	TO	FUNCTION
DIV N	Divide-by-N	XA8($\overline{5}$)	XA10(8)	Signal from A8 Main VCO to A10 Divide-by-N.
DØ	Data Ø	XA14A(3)	XA9($\overline{9}$), XA10(15), XA13(1), XA14A(3), XA15A(3), XA16A(3), XA17(10), A22J1(20), X22W4(11)	Data Lines
D1	Data 1	XA14A(4)	XA10(16), XA13(2), XA17(11), A22J1(19), A22W4(12)	
D2	Data 2	XA14A(5)	XA10(17), XA13(3), XA15A($\overline{5}$), XA16A(5), XA17(12), A22J1(18), A22W4(13)	
D3	Data 3	XA14A(6)	XA10(18), XA13(4), XA15A(6), XA16A(6), XA17(13), A22J1(17), A22W4(14)	
D4	Data 4	XA14A(7)	XA10($\overline{15}$), XA12(15, $\overline{15}$), XA15A(7), XA16A(7), XA17(11), A22J1(5), A22W4(15)	
D5	Data 5	XA14A(8)	XA10($\overline{16}$), XA12(16, $\overline{16}$), XA15A(8), XA16A(8), XA17(10), A22J1(6), A22W4(16)	
D6	Data 6	XA14A(9)	XA10($\overline{17}$), XA12(17, $\overline{17}$) XA15A(9), XA16A(9), XA17(9), A22J1(7), A22W4(23)	
D7	Data 7	XA14A(10)	XA10($\overline{18}$), XA12(18, $\overline{18}$), XA15A(10), XA16A(10), XA17($\overline{8}$), A22J1(8), A22W4(24)	
EXT IN	External Input	J2 (rear panel)	XA18($\overline{10}$)	Signal from an external source via J2 on rear panel to A18 Time Base Buffer Assembly
HECL RST (HECLR)	High ECL Reset	XA13($\overline{10}$)	XA3(4)	High signal from A13 Counter Assembly that resets the main gate on A3 Direct Count Amplifier Assembly.
HDSP WRT (HDSP)	High Display Write	XA14B(10)	XA2(3)	High signal from A14 Microprocessor causes data from bus to be written into RAM on A2 Display Driver. When signal goes low, contents of RAM are displayed.
HSRCH EN	High Search Enable	XA7(2)	XA6(8)	High signal from 500 kHz detector on A7 sent to Search Generator on A6 if the offset VCO frequency is not 500 kHz less than the main VCO frequency.

Table 8-2. Signal Names (Continued)

MNEMONIC	NAME	FROM	TO	FUNCTION
IF	Intermediate Frequency	A25J3	XA11($\overline{1}$), via A22W3	A25 Preamplifier output to A11 IF Limiter Assembly.
IF COUNT	Intermediate Frequency to Counter	XA12(8)	XA13(7)	A12 IF Detector output to A13 Counter Assembly
IF LIM	Intermediate Frequency Limiter Output	XA11($\overline{12}$)	XA12($\overline{1}$)	A11 IF Limiter output to A12 IF Detector Assembly.
IF OUT	Intermediate Frequency Output	A25J4	J4 (rear panel) via W3	A25 Preamplifier intermediate frequency output to rear panel connector.
ISOLATOR	Optical Isolator	XA19(18, $\overline{18}$)	XA20(15, $\overline{15}$), XA21(17, $\overline{17}$)	Signals excessive current load to the U3 Timer Overcurrent shutdown circuit.
LCTR RD	Low Counter Read	XA14B(2)	XA13(6)	Signal from A14 Microprocessor to A13 Counter Multiplexer circut to read contents of A or B counter to the data bus (depending upon the state of the A5 line).
LCTR WRT	Low Counter Write	XA14B(3)	XA13(7)	Signal from A14 Microprocessor to A13 Counter FF circuit that selects either IF or Direct B to be counted.
LDA	Low Digital-to-Analog	XA14B($\overline{3}$)	XA2U15(4, 5)	Signal from A14 Microprocessor that loads data into U15 Buffer register on A2 board (Option 004) for conversion to analog.
LDIR Gate	Low Direct Gate	XA17($\overline{4}$)	XA3(5)	Low signal from A17 Timing Generator that enables the direct count main gate on A3 Direct Count Amplifier Assembly.
LDVRST	Low Device Reset	XA14B(4)	XA2J1(9)	Temporary low signal from A14 Microprocessor to A2 Display that blanks the display during power up.
LEXT	Low External	S4 (rear panel)	XA18(9)	Low signal from rear panel switch (EXT/INT) in EXT position that selects external oscillator input to A18 Time Base Buffer instead of internal oscillator.
LHP-IB	Low HP Interface Bus	XA14B($\overline{14}$)	XA15B(6)	Low signal from decoder on A14 Microprocessor to enable reading from and writing to A15 HP-IB (Option 011).
LIF Gate	Low Intermediate Frequency Gate	XA17($\overline{5}$)	XA13(16)	Low signal from A17 Timing Generator that enables counter A or B on A13 Counter Assembly (depending upon the state of the LO switch signal).

Table 8-2. Signal Names (Continued)

MNEMONIC	NAME	FROM	TO	FUNCTION
LIRQ	Low Interrupt Request	XA2J1(1)	XA14A(13)	Low signal from A2 Display Driver or HP-IB Option 011 that interrupts A14 Microprocessor.
LKBRD (LKBR)	Low Keyboard	XA14B(9)	XA2(4)	Low signal enables A2 Display Driver to send keyboard information to A14 Microprocessor.
LO FREQ	Local Oscillator Frequency	A4W1	A26J2	A5 Multiplexer Local Oscillator output to A26 Sampler Driver.
LO Switch	Local Oscillator Switch	XA17($\overline{1}$)	XA5($\overline{5}$), XA13($\overline{8}$)	Low signal from A17 Timing Generator that switches A5 Multiplexer between Main VCO and Offset VCO synchronously with switching between Counter A and B on A13 Counter Assembly.
LOVL (OL)	Low Overload	A25A1($\overline{18}$)	XA12(14)	Not used.
LPD READ (LPDRD)	Low Power Detect Read	XA14B($\overline{9}$)	XA12($\overline{13}$)	Low signal from A14 Microprocessor to A12 IF Detector that causes A12 to output data to the bus.
LPD WRT	Low Power Detect Write	XA14B($\overline{10}$)	XA12($\overline{14}$), XA9(9)	Low signal from A14 Mircoprocessor to A12 IF Detector that causes A12 to detect input signal power level. When high, selects narrow or wide filter on A9 Main Loop Amplifier, depending upon the state of data bit DØ.
LPOS SLOPE (LPOS SL)	Low Positive Slope	XA6($\overline{8}$)	XA7($\overline{2}$)	Low signal from A6 Search Generator to A7 Mixer/ Search Control prevents loop from locking on upper sideband when offset VCO is 500 kHz greater than main VCO.
LPWR	Low Power	XA14B($\overline{13}$)	XA16B(2)	Low signal from A14 Microprocessor to A16 Trigger circuit that enables decoder U17.
LTIM RD (LTMRD)	Low Timing Read	XA14B($\overline{6}$)	XA17(8)	Low signal from A14 Microprocessor that results in data transfer from A17 Timing Generator to A14 via the data bus.
LTIM WRT (LTMWRT)	Low Timing Write	XA14B($\overline{7}$)	XA17(9)	Low signal from A14 Microprocessor that clocks data into the Input Register on A17 Timing Generator.
LSYNHI (LSYH)	Low Synch High	XA14B($\overline{11}$)	XA10($\overline{14}$)	Low to high transition from A14 Microprocessor decoder that loads the high order bits into the N register on the A10 Divide-by-N Assembly.

Table 8-2. Signal Names (Continued)

MNEMONIC	NAME	FROM	TO	FUNCTION
LSYNLO (LSYL)	Low Synch Low	XA14B($\overline{12}$)	XA10(14)	Low to high transition from A14 Microprocessor decoder that loads low order bits into N register.
LXROM	Low External ROM	XA15A(16), XA16A(16)	XA14A(16)	Not used.
MAIN $\Delta\phi$1	Main Phase Error 1	XA10(1)	XA9(12)	Phase error signals from A10 Divide-by-N assembly to A9 Main Loop Amplifier that control the A8 Main VCO.
MAIN $\Delta\phi$2	Main Phase Error 2	XA10($\overline{1}$)	XA9($\overline{12}$)	
MAIN CTRL	Main Control	XA9(6)	XA8(1)	Control voltage signal from A9 Main Loop Amplifier that controls the frequency of the A8 Main VCO.
MAIN OSC	Main Oscillator	XA8(7)	XA5(10)	A8 Main VCO output to A5 RF Multiplexer Assembly.
MAIN VCO	Main Voltage Controlled Oscillator	XA8(3)	XA7(12)	A8 Main VCO output to A7 Mixer/Search Control Assembly that is mixed with the signal from A4 Offset VCO.
OFFSET $\Delta\phi$1	Offset Phase 1	XA7(1)	XA6(10)	A7 Mixer/Search Control outputs that are processed by A6 Offset Loop Amplifier to develop OFFSET CONTROL signal.
OFFSET $\Delta\phi$2	Offset Phase 2	XA7($\overline{1}$)	XA6($\overline{10}$)	
OFS CNTRL	Offset Control	XA6(6)	XA4(5)	A dc control voltage signal from A6 Offset Loop Amplifier to A4 Offset VCO Assembly.
OFS OSC	Offset Oscillator	XA4(10)	XA5(1)	A4 Offset VCO output to A5 RF Multiplexer Assembly.
OFS VCO	Offset Voltage Controlled Oscillator	XA4($\overline{7}$)	XA7(9)	A7 Offset VCO output to A7 Mixer/Search Control Assembly.
500 kHz	500 kilohertz	XA18(3)	XA7($\overline{7}$), XA10(5, $\overline{5}$)	500 kHz signal from A18 Time Base to the phase detector on A7 and to ÷10 circuit on A10 Divide-by-N Assembly.
1 MHz	1 Megahertz	XA18(1)	XA12($\overline{10}$), XA17(6)	1 MHz signal from A18 Time Base to A12 IF Detector and to the prs generator on A17 Timing Generator.
10 MHz OUT	10 Megahertz Out	XA18(5)	J3 (rear panel)	10 MHz signal from A18 Time Base to FREQ STD OUT connector on rear panel.

8-22. DISASSEMBLY AND REASSEMBLY

8-23. Before performing any of the following disassembly or reassembly procedures, the following steps must be performed.

a. Set LINE ON-STBY switch to STBY position.

b. Remove line power cable from Input Power Module (A23).

8-24. Top Cover Removal

8-25. To remove the top cover proceed as follows:

a. Place 5343A with top cover facing up.

b. At top rear of instrument remove pozidrive screw from rear cap retainer and remove retainer.

c. Slide top cover back until free from frame and lift off.

d. To gain access to pc assemblies remove screws from top plate and remove plate.

8-26. Bottom Cover Removal

8-27. To remove the bottom cover proceed as follows:

a. Place 5343A with bottom cover facing up.

CAUTION

In the following step, the two front plastic feet must be removed from the bottom panel to avoid damage to internal wiring.

b. Remove two front plastic feet from bottom cover. Lift up on back edge of plastic foot and push back on front edge of plastic foot to free foot from bottom cover.

c. Loosen captive pozidrive screw at rear edge of bottom cover.

d. Slide bottom cover back until it clears the frame. Reverse the procedure to replace the cover.

8-28. FRONT FRAME REMOVAL

8-29. To remove front frame from main housing of the instrument, proceed as follows:

a. Remove top and bottom covers as described in preceding paragraphs.

b. Remove two screws from front of each side strut attaching front panel frame. See *Figure 8-2*. Pull front out slightly to allow access to wiring.

c. From bottom front of instrument, remove coax cable by pulling off connectors from A1J1 and A1J3. Remove cable strap connector from A2 Display Driver board. Note orientation of connector pins for reference during reassembly. If DAC Option 004 is installed, remove coax cable at A2J3 and RED and VIOLET wires near ribbon cable connector. Also, remove single GRAY/WHITE wire at "LDA" point.

d. Remove coax cables from A28J2 (First If Preamp) and A26J2 (Sampler Driver).

e. Remove two screws from side of front frame that attach U1 Sampler, A26 Sampler Driver and A28 Preamplifier mounting plate. Loosen and separate coax fitting at input to sampler.

CAUTION

In the following step, note the cable attached to the power LINE switch and avoid stress on cable connections during removal of front panel frame.

f. The front panel frame (containing assemblies A1 and A2) can now be moved freely within limits of the power cable, as shown in *Figure 8-2*.

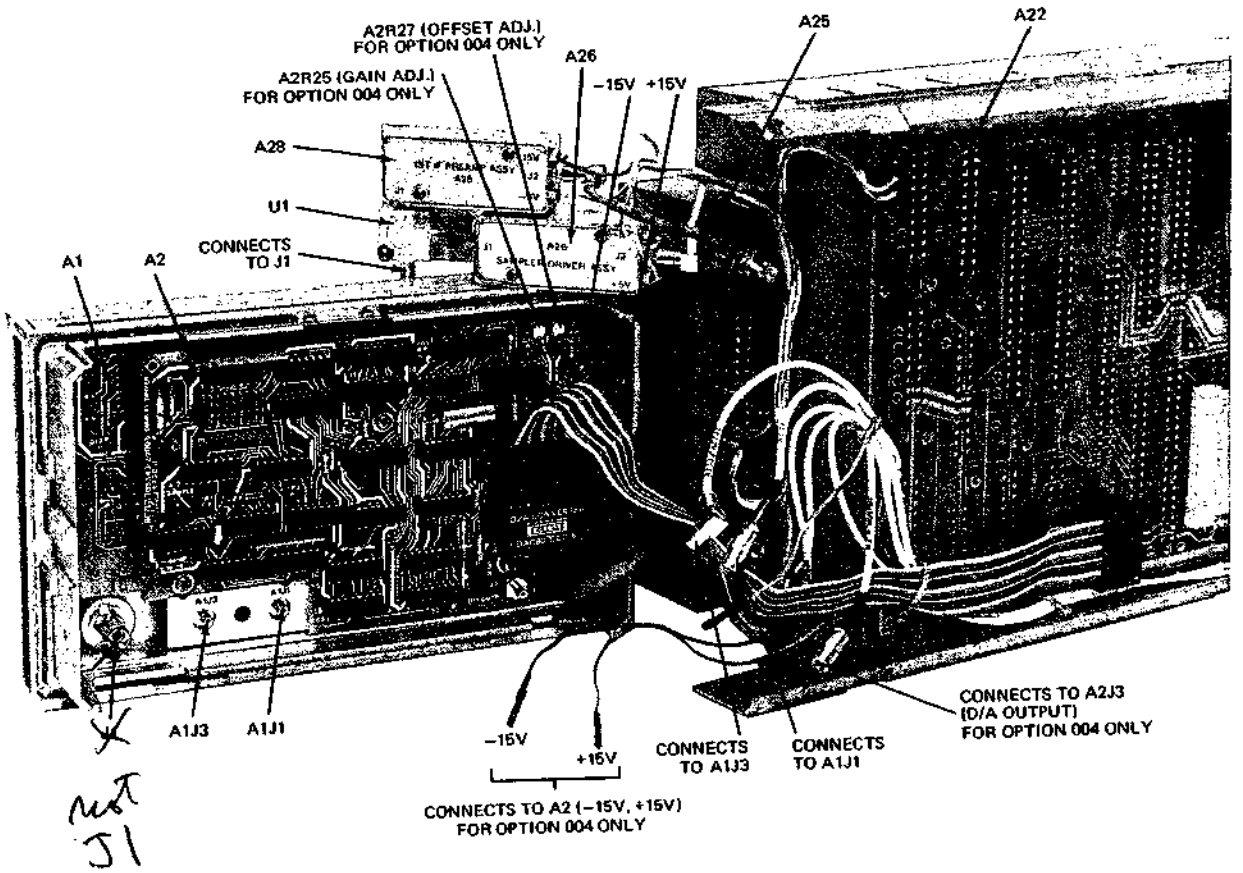


Figure 8-2. Front Frame, A26, A28, and U1 Removal

8-30. Removal of A1 Display Assembly and A2 Display Drive Assembly from Front Panel Frame

8-31. To remove A1 and A2 assemblies, remove frame as described in above paragraph and proceed as follows:

a. Remove the A1-A2 assemblies (combined) from front panel frame by removing the nut from the front panel BNC connector and removing the 5 large attaching screws from A2 Display Driver board.

b. Separate the A1 and A2 assemblies by removing the two nuts attaching plug P1 on the A1 Display assembly. Do not remove the attached screws from A2 Display Driver assembly.

c. Reassembly procedures are essentially the reverse of the disassembly procedures.

8-32. Replacement of LED's in Front Panel Switches

8-33. To replace a defective LED in a front panel pushbutton switch, remove and separate the A1 and A2 boards as described in the preceding paragraphs, and proceed as follows:

a. Pull off the switch cap that covers the defective LED. Use needle nose pliers under edge of cap and gently pry up to avoid marring cap.

b. Use a short length (approximately 2 inches) of heat-shrink tubing that will fit over the replacement LED. Apply heat to the tubing to make a tight fit.

c. Unsolder the connections to the defective LED on the A1 board. Slide the heat-shrink tubing over the defective LED and withdraw.

d. Place the replacement LED into the heat-shrink tubing and insert into the switch. Solder the leads to the board. Replace key cap.

8-34. Removal of U1 Sampler, A28 1st Preamplifier, and A26 Sampler Driver

8-35. Remove U1, A28 and A26 as follows:

a. Remove front frame as described in paragraph 8-28.

b. Unsolder the wires connected to the feedthru capacitors on A26 and A28.

c. Remove each assembly by removing the screws attaching to the mounting plate.

CAUTION

In the following step, use extreme care in separating the units. Carefully pull straight apart to avoid damage to components.

d. Separate U1 from A26 by loosening the joining connector.

8-36. FACTORY SELECTED COMPONENTS

8-37. Some component values are selected at the time of final checkout at the factory. These values are selected to provide optimum compatibility with associated components and are identified on schematics and parts lists by an asterisk (*). The recommended procedure for replacing a factory-selected part is as follows:

a. Refer to paragraphs 8-38 through 8-43 for test procedures required for selection of critical value parts.

b. For factory selected components that are not listed in paragraphs 8-38 through 8-43, use the original value.

c. After replacing parts, perform the test specified for the circuit in the performance and adjustment sections of this manual to verify correct operation.

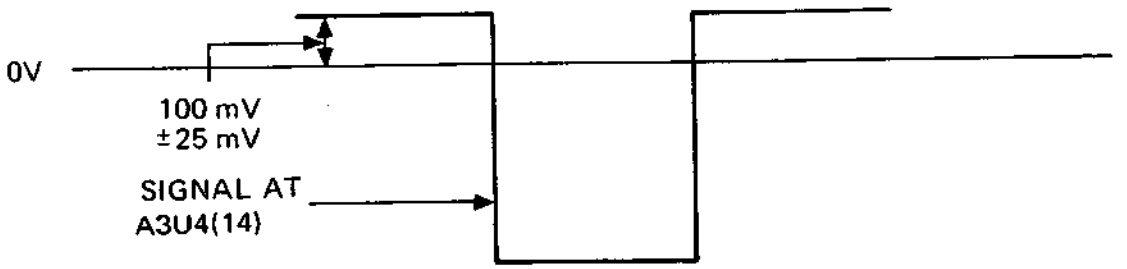
8-38. Procedure for Selecting Resistor R15 on Direct Count Amplifier A3

8-39. If resistor A3R15 is not properly selected for value (average value 42.2 ohms), the 5343A may exhibit a miscount at the low frequency direct count input for frequencies near 500 MHz. To properly select A3R15, perform the following:

a. Set the 5343A to the 10 Hz—500 MHz RANGE and select 1 kHz RESOLUTION.

b. With assembly A3 on an extender board, monitor A3U4(14) with an oscilloscope.

c. The signal at A3U4(14) must go positive by 100 mV (±25 mV).



d. To determine the value of A3R15, first decide how much the actual upper voltage level at A3U4(14) must change in order to fall between +75 mV to +125 mV. For every 5 mV increase required, the value of A3R15 must be increased by 1 ohm and for every 5 mV decrease, the value of A3R15 must be decreased by 1 ohm. For example, if the actual voltage only goes positive by 25 mV, then a 75 mV increase is required. Increase A3R15 by 15Ω.

e. Use a 1%, 0.125W resistor for A3R15. The following are HP part numbers for resistors which may be used.

Value	Part No.
61.9Ω	0757-0276
56.2Ω	0757-0395
51.1Ω	0757-0394
46.4Ω	0698-4037
42.2Ω	0757-0316
38.3Ω	0698-3435
34.8Ω	0698-3434
31.6Ω	0757-0180
28.7Ω	0698-3433

8-40. Procedure for Selecting Resistor R16 and Capacitor C10 on Direct Count Amplifier A3

8-41. If resistor A3R16 and capacitor A3C10 are not the proper value, the 5343A will exhibit miscount at low levels for frequencies near 10 Hz at the high impedance direct count input. This miscount is caused by leakage of the 300 MHz synthesizer frequency into the low frequency input. To select A3R16 and A3C10, perform the following:

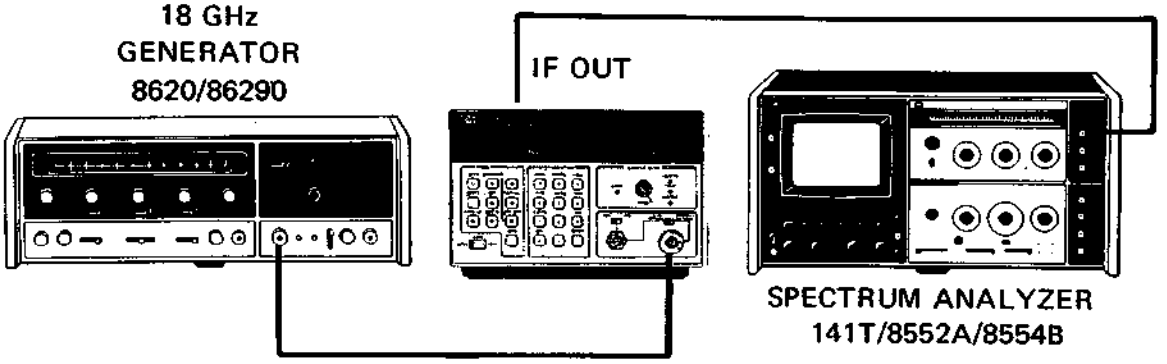
a. With the 5343A set to the 10 Hz—500 MHz, impedance select set to 1 MΩ, 1 Hz resolution, apply a 10 Hz signal at a level of 50 mV rms. If the counter properly counts 10.Hz, leave A3R16 at 51Ω (0698-3378) and A3C10 at 2.2 pF (0160-3872).

b. If the counter miscounts, change A3R16 to 510Ω (0698-5176) and change A3C10 to 10 pF (0160-3874).

8-42. Procedures for Selecting Resistor R16 on Main Loop Amplifier A9

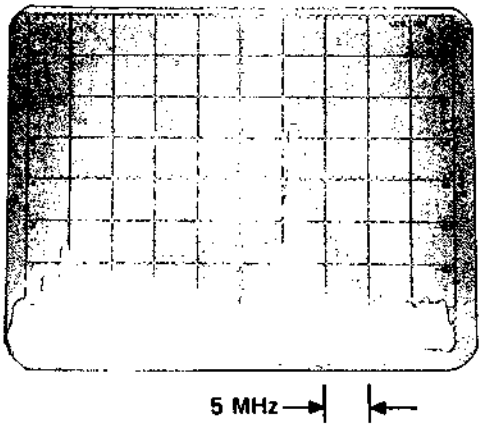
8-43. Whenever a repair is made in the main synthesizer loop consisting of assemblies A9, A8, and A10, it may be necessary to change the value of resistor A9R16. If A9R16 is not the proper value, the counter will miscount at high frequencies. This miscount will be independent of input signal level. Start with A9R16 equal to 10 MΩ (HP P/N 0683-1565) and test as follows:

a. Test setup:

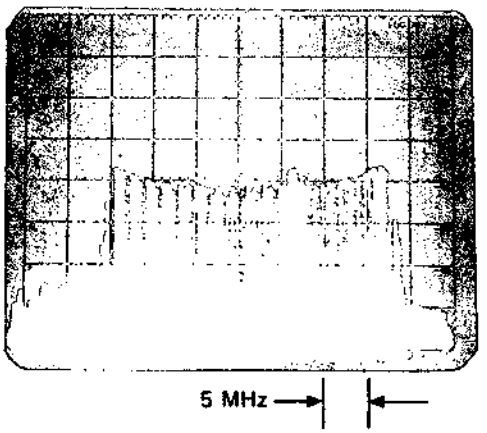


b. Set the signal generator to 18 GHz and approximately -10 dBm. Place the 5343A to AUTO and observe 18 GHz count.

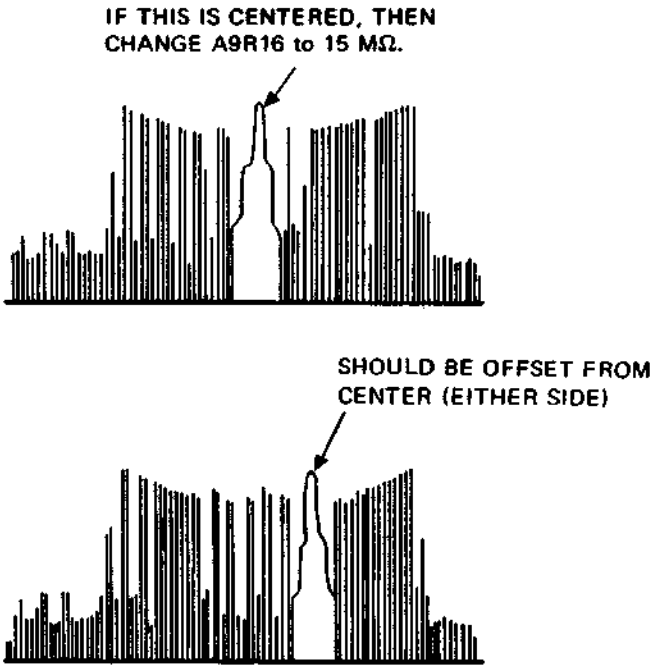
c. Set 5343A to MANUAL and observe the 5343A rear panel IF OUT on the spectrum analyzer. Set spectrum analyzer SCAN WIDTH to 5 MHz and observe the following:



d. Reduce input signal level until counter no longer counts 18 GHz but displays all zeros. The IF OUT on the spectrum analyzer should appear as:



e. If the spectrum analyzer display remains as in the first photo, or if the IF is centered as shown below, then change A9R16 to 15 MΩ (0683-1565).



8-44. After replacement of factory selected parts, conduct the performance tests required in Section IV.

8-45. Refer to Section V for adjustments if the performance tests are not passed.

8-46. SERVICE ACCESSORY KIT 10842A

8-47. The 10842A Service Accessory Kit contains 10 special extender boards (*Figure 8-3*) designed to aid in troubleshooting the 5343A. The following paragraphs describe equipment supplied, replaceable parts and operation.

8-48. Equipment Supplied

8-49. *Table 8-3* lists the boards contained in the 10842A Service Accessory Kit with their general description and usage. The kit is shown in *Figure 8-3*.

Table 8-3. 10842A Kit Contents

HP PART NO.	QTY.	DESCRIPTION FOR USE
05342-60030	1	10 pin X2 Extender Boards for A4, A5, A6, and A18 assemblies.
05342-60031	1	12 pin X2 Extender Boards for A3, A7, A8, A9, and A11 assemblies.
05342-60032	1	15 pin X2 Extender Boards for the A24 assembly.
05342-60033	2	18 pin X2 Extender Boards for the A17 assembly.
05342-60034	2	22 pin X2 Extender Boards for A10, A12, A13, A20, A21 assemblies.
05342-60035	1	24 pin X2 Extender Boards for the A19 assembly.
05342-60036	1	Double 18 pin X2 Extender Boards for the A14 assembly.
05342-60039	1	Keyed double 18 pin X2 Extender Boards for the A15 HP-IB assembly.

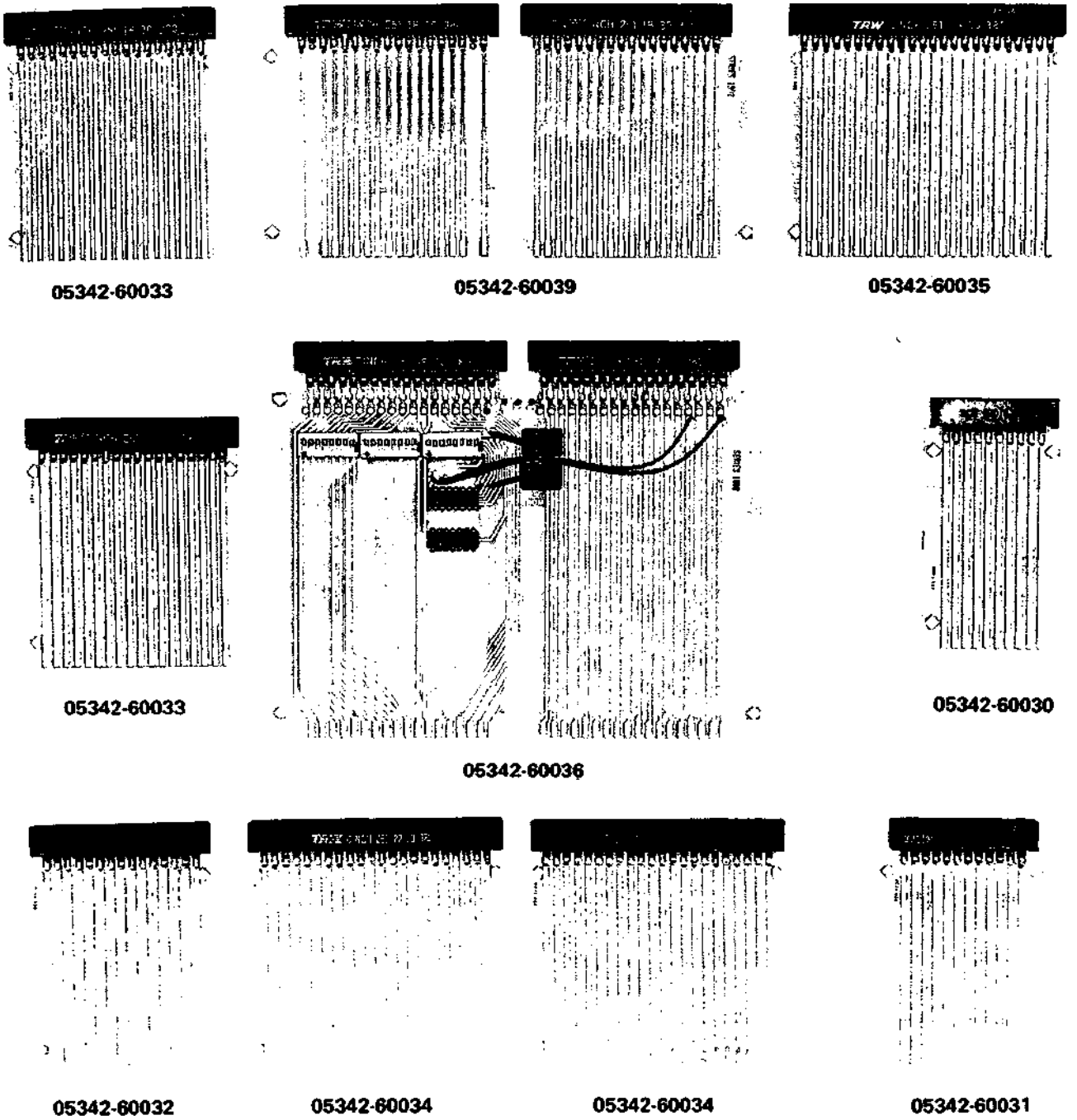


Figure 8-3. 10842A Service Accessory Kit

8-50. Replaceable Parts

8-51. The only replaceable parts in the 10842A kit are the two integrated circuits and five switches on the 05342-60036 extender board. *Table 8-4* lists the HP part number and description of those parts. Refer to Section VI for ordering information.

Table 8-4. Replaceable Parts for Extender Board 05342-60036

REF. DESIG.	HP PART NUMBER	QTY.	DESCRIPTION	MFR. CODE	MFR. PART NUMBER
U1	1820-1197	1	IC GATE TTL LS NAND QUAD 2-INPUT	01698	SN74LS00N
U2	1820-1281	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INPUT	01698	SN74LS139N
S1	3101-1856	1	SWITCH-SL-8-1A-NS DIP-SLIDE-ASSY .1A	28480	3101-1856
S2	3101-1856	1	SWITCH-SL-8-1A-NS DIP-SLIDE-ASSY .1A	28480	3101-1856
S3	3101-1856	1	SWITCH-SL 8-1A-NS DIP-SLIDE-ASSY .1A	28480	3101-1856
S4	3101-1213	1	SWITCH-TGL SUBMIN DPST .5A 120VAC PC	28480	3101-1213
S5	3101-1675	1	SWITCH-TGL SUBMIN DPST .5A 120VAC/ DC PC	28480	3101-1675

8-52. Using Extender Board 05342-60036

8-53. The following paragraphs describe the general operation of the extender board (05342-60036). Included is a description of the 3 DIP switches (S1, S2, and S3) the two toggle switches (S4 and S5) and test points R6K and R7K on A14. *Figure 8-4* shows the signals present at R6K and R7K. *Figure 8-5* is the schematic diagram of the extender board.

8-54. The 05342-60036 extender board is used for troubleshooting the A14 Microprocessor Assembly in the 5343A. This extender board not only allows operation of A14 outside the instrument casting but it also permits:

a. Isolation of the 16-line address bus and the 8-line data bus from the rest of the instrument.
b. Generation of START/STOP signals for performing signature analysis on individual ROM's on A14.
c. Manual control of the microprocessor reset.

8-55. The S1 switch (leftmost switch) opens the data bus. With all switches up, the switches are in the closed position. The S2 and S3 switches open the 16 lines of the address bus.

8-56. Test points R1, R2, and R3 on the extender board are used in taking signatures of the 5342A and do not apply to the 5343A.

8-57. If the A14 Microprocessor is put into freerun as described in *Table 8-11*, the signals shown in *Figure 8-4* should be observed at test points R6K and R7K on the A14 board.

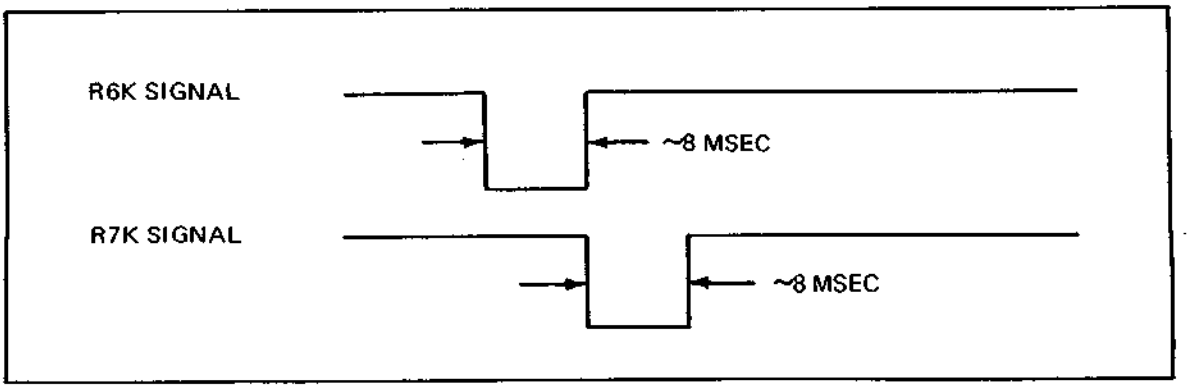


Figure 8-4. A14 Board (05343-60006) Test Points R6K, R7K

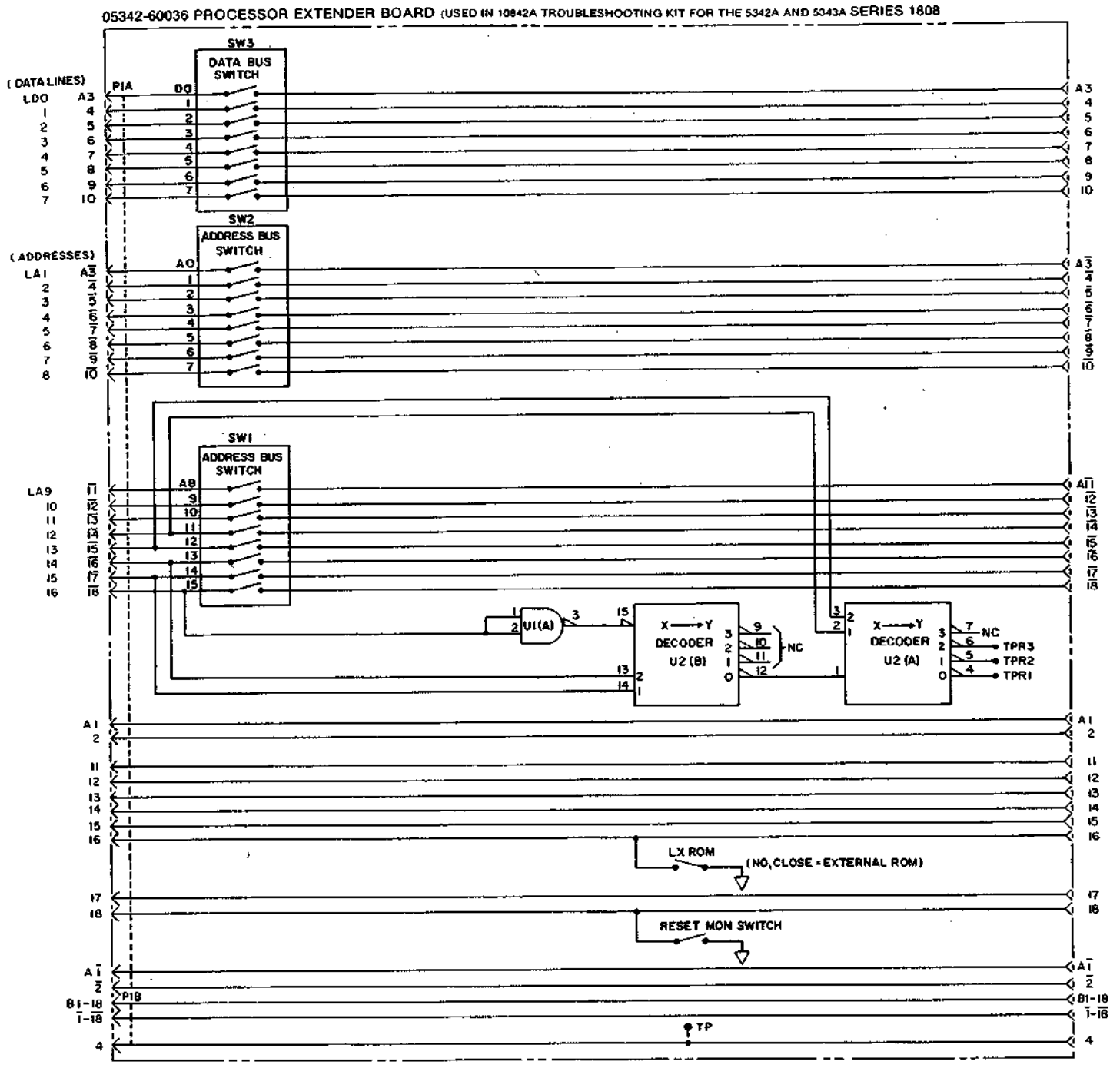


Figure 8-5. Extender Board (05342-60036) Schematic Diagram

8-58. LOGIC SYMBOLS

8-59. Logic symbols used in this manual conform to the American National Standard ANSI Y32.14-1973 (IEEE Std. 91-1973). This standard supersedes MIL-STD-806B. In the following paragraphs logic symbols are described. For further descriptions refer to HP Logic Symbology manual, part number 5951-6116.

8-60. Logic Concepts

8-61. The binary numbers 1 and Ø are used in pure logic where 1 represents true, yes, or active and Ø represents false, no, inactive. These terms should not be confused with the physical quantity (e.g., voltage) that may be used to implement the logic, nor should the term "active" be confused with a level that turns a device on or off. A truth table for a relationship in logic shows (implicitly or explicitly) all the combinations of true and false input conditions and the result (output). There are only two basic logic relationships, AND and OR. The following illustrations assume two inputs (A and B), but these can be generalized to apply to more than two inputs.

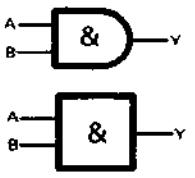
AND Y is true if and only if A is true and B is true (or more generally, if all inputs are true).
Y=1 if and only if A=1 **and** B=1
Y=A•B

OR Y is true if and only if A is true or B is true (or more generally, if one or more input(s) is (are) true).
Y=1 if and only if A=1 **or** B=1
Y=A+B

TRUTH TABLE

A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

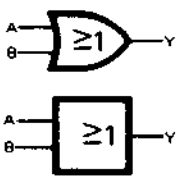
EQUIVALENT SYMBOLS



TRUTH TABLE

A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

EQUIVALENT SYMBOLS



8-62. Negation

8-63. In logic symbology, the presence of the negation indication symbol O provides for the presentation of logic function inputs and outputs in terms *independent* of their physical values, the Ø-state of the input or output being the 1-state of the symbol referred to the symbol description.

EXAMPLE 1

TRUTH TABLE

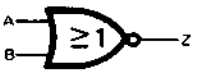
A	B	Z
1	1	0
1	0	1
0	1	1
0	0	1

EXAMPLE 2

TRUTH TABLE

A	B	Z
1	1	0
1	0	1
0	1	1
0	0	1

EXAMPLE 3



TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

EXAMPLE 4

TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

EXAMPLE 1 says that Z is *not* true if A is true *and* B is true or that Z is true if A *and* B are *not* both true. $\overline{Z}=AB$ or $Z=\overline{AB}$. This is frequently referred to as NAND (for NOT AND).

EXAMPLE 2 says that Z is true if A is *not* true *or* if B is *not* true. $Z=\overline{A}+\overline{B}$. Note that this truth table is identical to that of Example 1. The logic equation is merely a DeMorgan's transformation of the equations in Example 1. The symbols are equivalent.

EXAMPLE 3 $\overline{Z}=A+B$ or $Z=\overline{A}+\overline{B}$ and,

EXAMPLE 4 $Z=\overline{A \bullet B}$, also share common truth table and are equivalent transformations of each other. The NOT OR form (Example 3) is frequently referred to as NOR.

NOTE

In this manual the logic negation symbol is NOT used.

8-64. Logic Implementation and Polarity Indication

8-65. Devices that can perform the basic logic functions, AND and OR, are called gates. Any device that can perform one of these functions can also be used to perform the other if the relationship of the input and output voltage levels to the logic variables 1 and Ø is redefined suitably.

8-66. In describing the operation of electronic logic devices, the symbol H is used to represent a "high level", which is a voltage within the more-positive (less-negative) of the two ranges of voltages used to represent the binary variables. L is used to represent a "low level", which is a voltage within the less-positive (more-negative) range.

8-67. A function table for a device shows (implicitly or explicitly) all the combinations of input conditions and the resulting output conditions.

8-68. In graphic symbols, inputs or outputs that are active when at the high level are shown without polarity indication. The polarity indicator symbol ◺ denotes that the active (one) state of an input or output *with respect to the symbol to which it is attached* is the low level.

NOTE

The polarity indicator symbol " ◺ " is used in this manual.

EXAMPLE 5 assume two devices having the following function tables.

DEVICE #1
FUNCTION TABLE

A	B	Y
H	H	H
H	L	L
L	H	L
L	L	L

DEVICE #2
FUNCTION TABLE

A	B	Y
H	H	H
H	L	H
L	H	H
L	L	L

POSITIVE LOGIC by assigning the relationship H=1, L=Ø at both input and output, Device #1 can perform the AND function and Device #2 can perform the OR function. Such a consistent assignment is referred to as positive logic. The corresponding logic symbols would be:

DEVICE #1

DEVICE #2

NEGATIVE LOGIC

alternatively, by assigning the relationship H=Ø, L=1 at both input and output, Device #1 can perform the OR function and Device #2 can perform the AND function. Such a consistent assignment is referred to as negative logic. The corresponding logic symbols would be:

DEVICE #1

DEVICE #2

8-69. MIXED LOGIC. The use of the polarity indicator symbol (◺) automatically invokes a mixed-logic convention. That is, positive logic is used at the inputs and outputs that do not have polarity indicators, negative logic is used at the inputs and outputs that have polarity indicators.

EXAMPLE 6
FUNCTION TABLE

A	B	Z
H	H	L
H	L	H
L	H	H
L	L	H

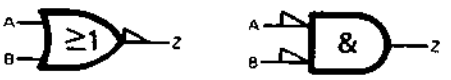
This may be shown either of two ways:

Note the equivalence of these symbols to examples 1 and 2 and the fact that the function table is a positive-logic translation (H=1, L=Ø) of the NAND truth table, and also note that the function table is the negative-logic translation (H=Ø, L=1) of the NOR truth table, given in Example 3.

EXAMPLE 7
FUNCTION TABLE

A	B	Z
H	H	L
H	L	L
L	H	L
L	L	H

This may be shown either of two ways:



Note the equivalence of these symbols to examples 3 and 4 and the fact that the function table is a positive-logic translation (H=1, L=Ø) of the NOR truth table, and also note that the function table is the negative-logic translation (H=Ø, L=1) of the the NAND truth table, given in Example 1.

8-70. It should be noted that one can easily convert from the symbology of positive-logic merely by substituting a polarity indicator (◺) for each negative indicator (o) while leaving the distinctive shape alone. To convert from the symbology of negative-logic, a polarity indication (◺) is substituted for each negation indicator (o) and the OR shape is substituted for the AND shape or vice versa.

8-71. It was shown that any device that can perform OR logic can also perform AND logic and vice versa. DeMorgan's transformation is illustrated in Example 1 through 7. The rules of the transformation are:

1. At each input or output having a negation (o) or polarity (◺) indicator, delete the indicator.
2. At each input or output not having an indicator, add a negation (o) or polarity (◺) indicator.
3. Substitute the AND symbol ⊐ for the OR symbol ⊃ or vice versa.

These steps do not alter the assumed convention; positive-logic stays positive, negative-logic stays negative, and mixed-logic stays mixed.

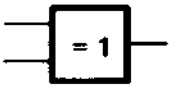
8-72. The choice of symbol may be influenced by these considerations: (1) The operation being performed may best be understood as AND or OR. (2) In a function more complex than a basic gate, the inputs will usually be considered as inherently active high or active low (e.g., the J and K inputs of a J-K flip-flop are active high and active low, respectively). (3) In a chain of logic, understanding and the writing of logic equations are often facilitated if active low or negated outputs feed into active low or negated inputs.

8-73. Other Symbols

8-74. Additional symbols are required to depict complex logic diagrams, as follows:

Dynamic input activated by transition from a low level to a high level. The opposite transition has no effect at the output.

Dynamic input activated by transition from a high level to a low level. The opposite transition has no effect at the output.



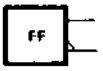
Exclusive OR function. The output will assume its indicated active level if and only if one and only one of the two inputs assumes its indicated active level.

Inverting function. The output is low if the input is high and it is high if the input is low. The two symbols shown are equivalent.

Noninverting function. The output is high if the input is high and it is low if the input is low. The two symbols shown are equivalent.

OUTPUT DELAY. The output signal is effective when the input signal returns to its opposite state.

EXTENDER. Indicates when a logic function increases (extends) the number of inputs to another logic function.



FLIP-FLOP. A binary sequential element with two stable states: a set (1) state and a reset (Ø) state. Outputs are shown in the 1 state when the flip-flop is set. In the reset state the outputs will be opposite to the set state.

RESET. A 1 input will reset the flip-flop. A return to Ø will cause no further effect.

SET. A 1 input will set the flip-flop. A return to Ø will cause no further action.

TOGGLE. A 1 input will cause the flip-flop to change state. A return to 0 will cause no further action.

J INPUT. Similar to the S input except if both J and K (see below) are at 1, the flip-flop changes state.

K INPUT. Similar to the R input (see above).

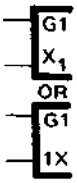
D INPUT (Data). Always dependent on another input (usually C). When the C and D inputs are at 1, the flip-flop will be set. When the C is 1 and the D is Ø, the flip-flop will reset.

Address symbol has multiplexing relationship at inputs and demultiplexing relationship at outputs.

8-75. Dependency Notation "C" "G" "V" "F"

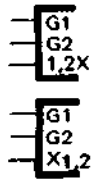
8-76. Dependency notation is a way to simplify symbols for complex IC elements by defining the existence of an AND relationship between inputs, or by the AND conditioning of an output by an input without actually showing all the elements and interconnections involved. The following examples use the letter "C" for control and "G" for gate. The dependent input is labeled with a number that is either prefixed (e.g., 1X) or subscripted (e.g., X_1). They both mean the same thing. The letter "V" is used to indicate an OR relationship between inputs or between inputs and outputs with this letter (V). The letter "F" indicates a connect-disconnect relationship. If the "F" (free dependency) inputs or outputs are active (1) the other usual normal conditions apply. If one or more of the "F" inputs are inactive (Ø), the related "F" output is disconnected from its normal output condition (it floats).

The input that controls or gates other inputs is labeled with a "C" or a "G", followed by an identifying number. The controlled or gated input or output is labeled with the same number. In this example, "1" is controlled by "G1."



When the controlled or gated input or output already has a functional lable (X is used here), that label will be prefixed or subscripted by the identifying number.

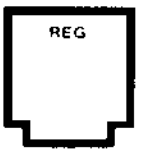
If a particular device has only one gating or control input then the identifying number may be eliminated and the relationship shown with a subscript.



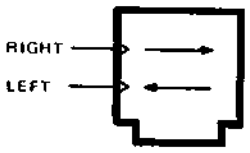
If the input or output is affected by more than one gate or control input, then the identifying numbers of each gate or control input will appear in the prefix or subscript, separated by commas. In this example "X" is controlled by "G1" and "G2."

8-77. Control Blocks

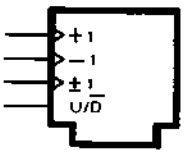
8-78. A class of symbols for complex logic are called control blocks. Control blocks are used to show where common control signals are applied to a group of functionally separate units. Examples of types of control blocks follow.



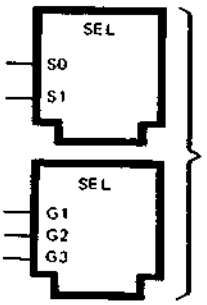
Register control block. This symbol is used with an associated array of flip-flop symbols to provide a point of placement for common function lines, such as a common clear.



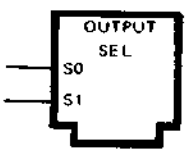
Shift register control block. These symbols are used with any array of flip-flop symbols to form a shift register. An active transition at the inputs causes left or right shifting as indicated.



Counter control block. The symbol is used with an array of flip-flops or other circuits serving as a binary or decade counter. An active transition at the +1 or −1 input causes the counter to increment one count upward or downward, respectively. An active transition at the ±1 input causes the counter to increment one count upward or downward depending on the input at an up/down control.



Selector control block. These symbols are used with an array of OR symbols to provide a point of placement for selection (S) or gating (G) lines. The selection lines enable the input designated 0, 1, ...n of each OR function by means of a binary code where S0 is the least-significant digit. If the 1 level of these lines is low, polarity indicators (◺) will be used. The gating lines have an AND relation with the respective input of each OR function: G1 with the inputs numbered 1, G2 with the input numbered 2, and so forth. If the enabling levels of these lines is low, polarity indicators (◺) will be used.

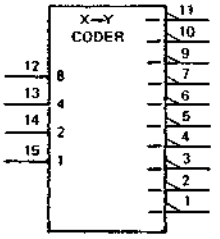


Output selector control block. This symbol is used with a block symbol having multiple outputs to form a decoder. The selection lines enable the output designated 0, 1, ...n of each block by means of a binary code where S0 is the least-significant digit. If the 1 level of these lines is low, polarity indicators (◺) will be used.

8-79. Complex Logic Devices

8-80. Logic elements can be combined to produce very complex devices that can perform more difficult functions. A control block symbol can be used to simplify understanding of many complex devices. Several examples of complex devices are given here. These examples are typical of the symbols used in schematic diagrams in this manual.

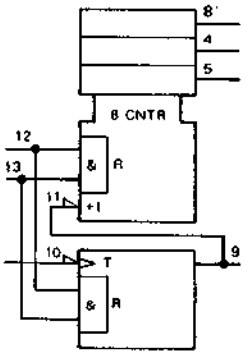
Reference Designation
A2U2, A2U8
Part Number
1820-0468
SN7445N



Description
BCD TO DECIMAL
DECODER/DRIVER

The output which is low will correspond to the binary weighted input. The minus signs at the output indicate that the element is capable of supplying LOW's only.

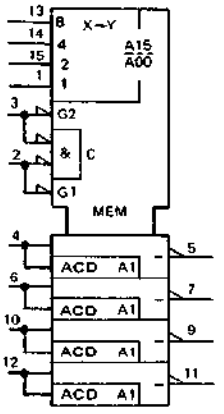
Reference Designation
A2U3
Part Number
1820-1443
SN74LS293N



Description
4-BIT BINARY COUNTER

This binary counter has four master-slave flip-flops and gating for which the count cycle length is divide-by-eight. The counter has a gated zero reset. To use the maximum count length, the pin 11 input is connected to the pin 9 output. The input count pulses are applied to the pin 10 input.

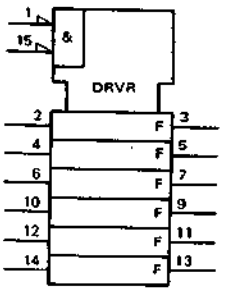
Reference Designation
A2U7, A2U12
Part Number
1820-0628
SN7489



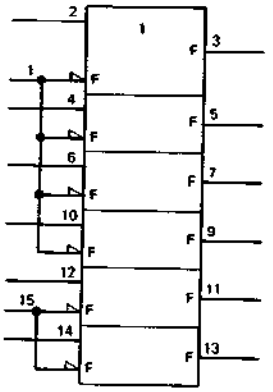
Description
64-BIT READ/WRITE MEMORY

This memory has an array of 64 flip-flop memory cells in a matrix to provide 16 words of 4 bits each. Information present at the data inputs (pins 4, 6, 10, 12) is written into memory by holding both the memory enable (pin 2) and write enable (pin 3) LOW while addressing the desired word at the BCD weighted inputs (pins 1, 13, 14, 15). The complement of the information written into memory is read out at the four outputs by holding memory enable (pin 2) LOW, write enable (pin 3) HIGH and selecting the desired address.

Reference Designation
A2U13, U17
Part Number
1820-1254
DM8095N



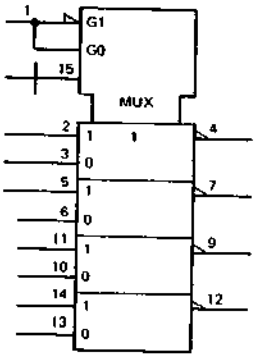
Reference Designation
A2U5
Part Number
1820-1049
DM8097N



Description
HEX BUFFERS - HEX INVERTERS

The buffers (8095-8097) and inverters (8096-8098) convent standard TTL or DTL outputs to TRI-STATE outputs. The 8095 and 8096 control all six devices from common inputs (pins 1 and 15 LOW). The 8097 and 8098 control four devices from one input (pin 1 LOW) and two devices from another input (pin 15 LOW).

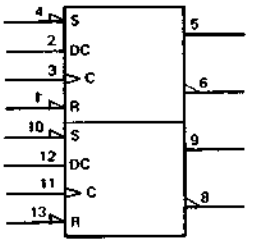
Reference Designation
A2U18
Part Number
1820-1428
74LS158



Description
2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

This quad two input multiplexer selects one of two word inputs and outputs the data the data when enabled. The level at pin 1 selects the input word. The outputs are LOW when pin 15 is LOW.

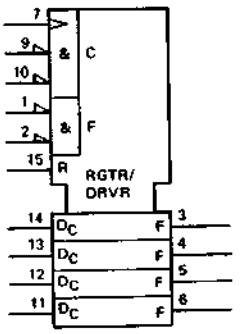
Reference Designation
A2U19, A2U20
A9U1, A10U4, A12U13
A13U4, A14U22, A15U3
A15U4, U9, U10, U14
A15U19, U34, U35
A17U9, U17
Part Number
1820-1112
SN74LS74N



Description
DUAL D-TYPE FLIP-FLOP

The dual D-type flip-flop consists of two indepentent D-type flip-flops. The information present at the data (D_C) input is transferred to the active-high and active-low outputs on a low-to-high transition of the clock (C) input. The data input is then locked out and the outputs do not change again until the next low-to-high transition of the clock input. The set (S) and reset (R) inputs override all other input conditions: when (S) is low, the active-high output is forced high; when reset (R) is low, the active-high output is forced low. Although normally the active-low output is the complement of the active-high output, simultaneous low inputs at the set and reset will force both the active-low and active-high outputs to go high at the same time on some D-type flip-flops. This condition will exist only for the length of time that both set and reset inputs are held low. The flip-flop will return to some indeterminate state when both the set and reset inputs are returned to the high state.

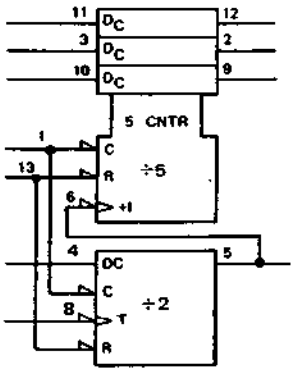
Reference Designation
A2U23
Part Number
1820-0574
DM8551N



Description
4-BIT D-TYPE REGISTERS

When both data-enable inputs (9 and 10) are LOW, data at the D_C inputs is loaded into the flip-flops on the next positive transition of the clock (pin 7). When both outputs control inputs (pins 1 and 2) are LOW, data is available at the outputs. The outputs are disabled by a HIGH at either output control input. The outputs then represent a high impedance.

Reference Designation
A10U1, A13U13,
A13U14,U17,U18
Part Number
1820-1251
SN74LS196N

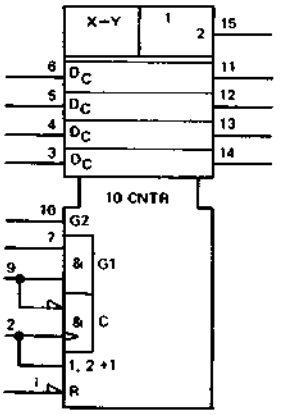


Description
50/30 MHz PRESETTABLE
DECADE COUNTER/LATCH

The Decade Counter consists of a divide-by-two and a divide-by-five counter formed by connecting pin 5 to pin 6 and taking the output from pin 12.

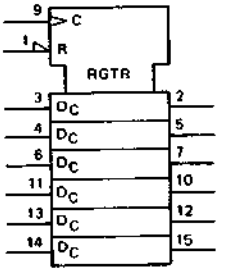
The outputs may be preset to any state by making "C" active low and entering the desired data at the "D_C" inputs. The outputs at pins 5, 9, 2, and 12 will then correspond to the data inputs independent of the state of the count-up clocks at pins 6 and 8. An active high signal at pin 1 then enables the counter by latching the parallel data into the counter. The count-up clock at pin 8 clocks the ÷2 counter and pin 6 clocks the ÷5 counter. When the counter is clocked at pins 8 or 6, the outputs will change on the negative-going edge of the signal. An active low at the "R" (reset) input (pin 13) causes all the outputs to go low independent of the counting state.

Reference Designation
A10U8,U9,U13,U14
Part Number
1820-1429
74LS160

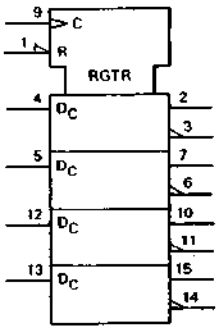


Description
SYNCHRONOUS DECADE COUNTER

This synchronous presettable decade counter has four master slave flip-flops that are triggered on the positive-going edge of the clock pulse (pin 2). A LOW at the load input (pin 9) disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels at the enable inputs (pins 7 and 10). The clear function (pin 1) is asynchronous and a low level clear input sets all outputs low regardless of the levels of the clock, load or enable inputs. Both count enable inputs (pins 7 and 10) must be HIGH to count and the pin 10 input is fed forward to enable the carry output (pin 15).



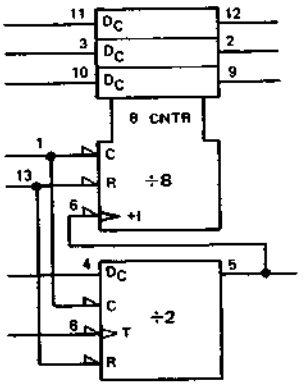
Reference Designation
A10U10, U15, U17
Part Number
1820-1196
SN74LS174N



Reference Designation
A10U11, U16
Part Number
1820-1195
SN74LS175N

Description
HEX/QUAD D-TYPE FLIP-FLOPS

Information at the D inputs is transferred to the outputs on the positive-edge of the clock pulse (pin 9). Clock triggering occurs at a particular voltage level. The hex FFs have single outputs, the quad FFs have complementary outputs.



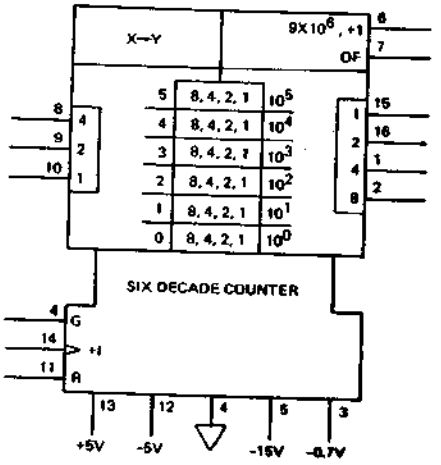
Reference Designation
A12U10, U15
Part Number
1820-1193
SN74LS197N

Description
30 MHz PRESETTABLE
BINARY COUNTERS/ LATCHES

This counter consists of four master-slave flip-flops that form a divide-by-two and a divide-by-eight counter. The outputs may be preset to any state by placing a low on pin 1 and entering the desired data. The outputs will change to agree with the inputs regardless of the state of the clocks. When used as a high-speed 4-bit ripple-through counter, the output of pin 5 must be externaly connected to the clock 2 input (pin 6). The input count pulses are applied to the clock 1 input (pin 8). Simultaneous divisions by 2, 4, 8, and 16 are performed at output pins 12, 2, 9, and 5, respectively.

When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock 2 input (pin 6). Simultaneous frequency divisions by 2, 4, and 8 are available at pin 12, 2 and 9, respectively. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

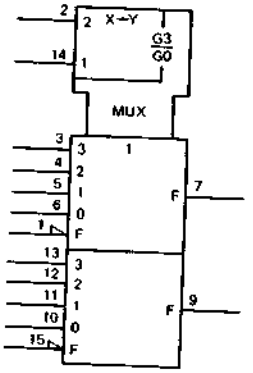
Reference Designation
A13U1, U2
Part Number
1820-0634



Description
SIX DECADE COUNTER

The six decade counter is an MOS, 6 digit, 10 MHz ripple-through counter with buffer storage for each of the 6 decades. The circuit has one set of BCD (positive logic (8421) outputs that may be switched from digit-to-digit by means of a 3-to-6 line decoder. An overflow output (pin 7) and a fifth decade carry output (pin 6) is also available. When the transfer input (pin 4) is held LOW, the decimal count of a selected decade can be transmitted through its own decade storage buffer to the BCD outputs by means of the 3-to-6 line decoder which is controlled by the BCD inputs.

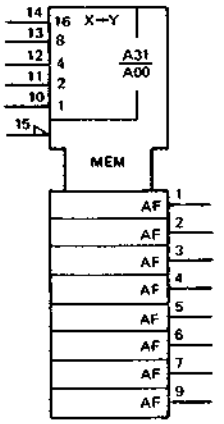
Reference Designation
A13U5,U6,U9,U10
Part Number
1820-1238
SN74LS253N



Description
DUAL 4-INPUT MULTIPLEXER

Input states on pins 2 and 14 are decoded according to their weighting modifiers to form AND gates (G0 through G3) in the common control block. The data inputs have numeric modifiers to indicate the specific gate which must be active for that input to be selected. The output on pin 7 will be HIGH IFF the selected input is HIGH and the inhibit input on pin 1 is LOW. Similarly, the ouptut on pin 9 will be HIGH IFF the selected input is HIGH and the inhibit input on pin 15 is LOW. If an inhibit input (pin 1 or 15) is HIGH the corresponding output (pin 7 or 9) will be LOW regardless of the state of the selected input.

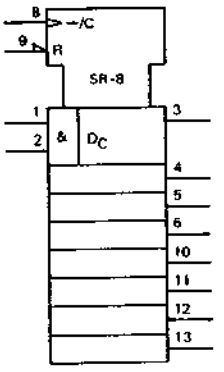
Reference Designation
A15U23
Part Number
1816-1154
Reference Designation
A15U26
Part Number
1816-1155



Description
READ ONLY MEMORY (ROM) WITH 32 ADDRESSES

Address selection is determined by the five upper inputs which are decoded into 32 possible addresses (A00 through A31) corresponding to the weighing modifiers at the inputs. Input modifier F (pin 15) gates the outputs. Stored data will be read from the selected memory address if F is active (LOW). The output data (pins 1-7 and 9) are active HIGH.

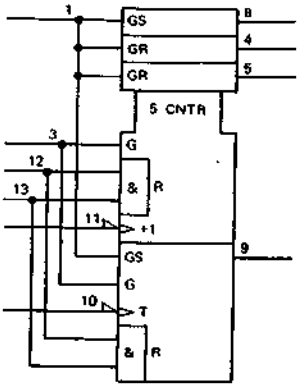
Reference Designation
A17U13, U5, U10
Part Number
1820-1433
SN74LS164N



Description
8-BIT PARALLEL OUT SERIAL SHIFT REGISTER

This 8-bit shift register has gated serial inputs and an asynchronous clear. A LOW at one or both gated serial inputs (pins 1, 2) inhibits entry of data and resets the first FF to the low level at the next clock pulse (pin 8). A high-level input (pin 1 or 2) enables the other input which will then determine the state of the first FF. Data is serially shifted in and out of the 8-bit register during the positive-going transition of the clock pulse. Clear is independent of the clock and occurs when pin 9 is LOW.

Reference Designation
A17U11
Part Number
1820-1442
SN74LS290N



Description
DECADE COUNTER

The decade counter has four master-slave flip-flops and gating for which the count cycle length is divided by five. This counter has a gated zero reset and a gated set-to-nine input. To use the maximum count length, the pin 11 input is connected to the pin 9 output. The input count pulses are applied to the T input at pin 10. A symmetrical divide-by-ten count can be obtained by connecting the pin 8 ouptut to the pin 10 input and applying the input count to the pin 11 input to obtain a divide-by-ten square wave at the pin 9 output.

8-81. THEORY OF OPERATION

8-82. The following theory of operation is introduced with a description of the unique harmonic heterodyne technique used in the 5343A. Then the overall operation is described with a simplified block diagram, followed by discussions of FM tolerance, automatic amplitude discrimination, and sensitivity. The function and relationships of the major assemblies are described next (to a complete block diagram), followed by a detailed description of the circuits on each assembly with reference to the schematic diagrams.

8-83. HARMONIC HETERODYNE TECHNIQUE

8-84. The HP 5343A Frequency Counter uses a harmonic heterodyne down-conversion technique to down convert the microwave input frequency into the range of its internal, low-frequency counter. This technique combines the best performance characteristics of heterodyne converters and transfer oscillators to achieve high sensitivity, high FM tolerance, and automatic amplitude discrimination.

8-85. All microwave counters must down convert the unknown microwave frequency to a low frequency signal which is within the counting range of an internal low frequency counter (typically 200 to 500 MHz). Heterodyne converters down convert the unknown signal, f_x, by mixing it with an accurately known local oscillator frequency, f_{LO}, such that the difference frequency, f_{IF} ($= f_x - f_{LO}$ if $f_x > f_{LO}$ and $= f_{LO} - f_x$ if $f_x < f_{LO}$) is within the counting range of the low frequency counter. The counted frequency, f_{IF}, is then added (or subtracted if $f_x < f_{LO}$) to/from the local oscillator frequency to determine the unknown frequency.

8-86. Like heterodyne converters, transfer oscillators also mix the unknown signal with harmonics of an internally generated signal, f_{VCO}. When one of the harmonics of the VCO signal, $N \cdot f_{VCO}$, mixes with the unknown to produce zero beat, then the VCO frequency is measured by the low frequency counter. After determining which harmonic produced zero beat, the measured VCO frequency is multiplied by N ($f_x = N \cdot f_{VCO}$). One of the major differences between the heterodyne technique and the transfer oscillator technique is the fact that the heterodyne converter employs a filter to select only one harmonic of the internal oscillator to mix with the unknown whereas the transfer oscillator mixes the unknown simultaneously with all harmonics of the internal frequency.

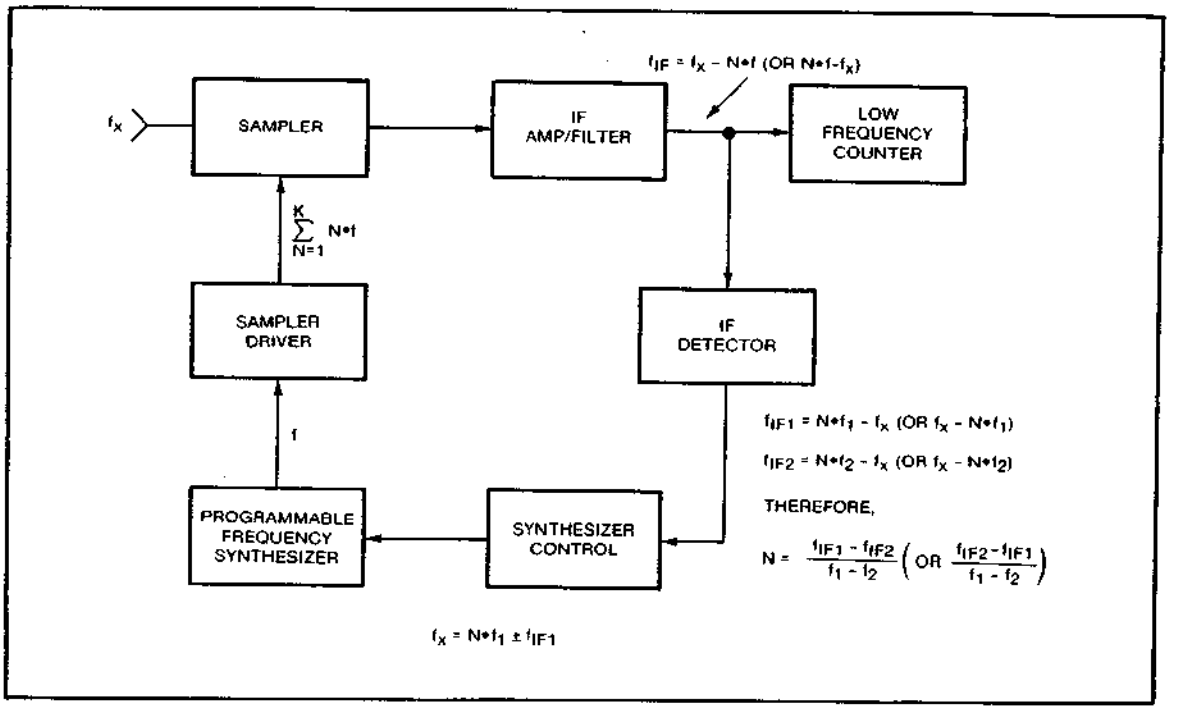


Figure 8-6. Harmonic Heterodyne Technique

8-87. *Figure 8-6* is a simplified block diagram of the harmonic heterodyne technique. In this technique, all of the harmonics of an internal oscillator (a programmable frequency synthesizer locked to the counter's time base) are simultaneously mixed with the unknown signal by the sampler and sampler driver (samplers are like harmonic mixers except that the conduction angle is much narrower — the sampling diodes in the HP 5343A sampler, for example, conduct for only a few picoseconds during each period of the sampling signal). The output of the sampler consists of sum and difference frequencies produced by each harmonic of the internal oscillator mixing with the unknown. The programmable frequency synthesizer is incremented in frequency until one of the outputs of the sampler is in the counting range of the low frequency counter. The IF detector detects when the IF is in the range of the low frequency counter and sends a signal which causes the synthesizer control to stop incrementing the frequency of the frequency synthesizer. The IF is then counted by the low frequency counter. The unknown frequency can be determined from the relation: $f_x = N \cdot f_1 \pm f_{IF1}$

where f_x = unknown frequency

N = harmonic of frequency synthesizer which mixed with unknown to produce countable IF

f_1 = programmed frequency of synthesizer

f_{IF1} = IF produced by $N \cdot f_1$ mixing with f_x

8-88. The frequency, f_1, of the programmable synthesizer is known since it is known where indexing of the synthesizer was stopped. The IF, f_{IF1}, is known since it is counted by the low frequency counter. Still to be determined are the N number and the sign (±) of the IF (the sign of f_{IF1} will be (+) if $N \cdot f_1$ is *less* than f_x; the sign of f_{IF1} is (—) if $N \cdot f_x$ is *greater* than f_x).

8-89. To determine N and the sign of f_{IF1}, one more measurement must be taken with the synthesizer offset from its previous value by a known frequency, $f_2 = f_1 - \Delta f$. This produces an IF,

f_{IF2}, which is counted by the low frequency counter. N is determined by the following:

$$f_{IF1} = N \cdot f_1 - f_x \text{ (if } Nf_1 > f_x)$$

$$f_{IF2} = N \cdot f_2 - f_x \text{ (if } Nf_2 > f_x)$$

$$\text{therefore } N = \frac{f_{IF1} - f_{IF2}}{f_1 - f_2}$$

or, if f_x is greater than Nf_1:

$$f_{IF1} = f_x - N \cdot f_1 \text{ (if } Nf_1 < f_x)$$

$$f_{IF2} = f_x - N \cdot f_2 \text{ (if } Nf_2 < f_x)$$

$$\text{therefore } N = \frac{f_{IF2} - f_{IF1}}{f_1 - f_2}$$

8-90. Referring to *Figure 8-7*, it is seen that if f_x is *greater* than $N \cdot f_1$, then f_{IF1}, produced by mixing $N \cdot f_1$ with f_x, will be *less* than f_{IF2}, produced by mixing $N \cdot f_2$ with f_x, since f_2 is *less* than f_1, by Δf. However, if f_x is *less* than $N \cdot f_1$, then f_{IF1} will be *greater* than f_{IF2}.

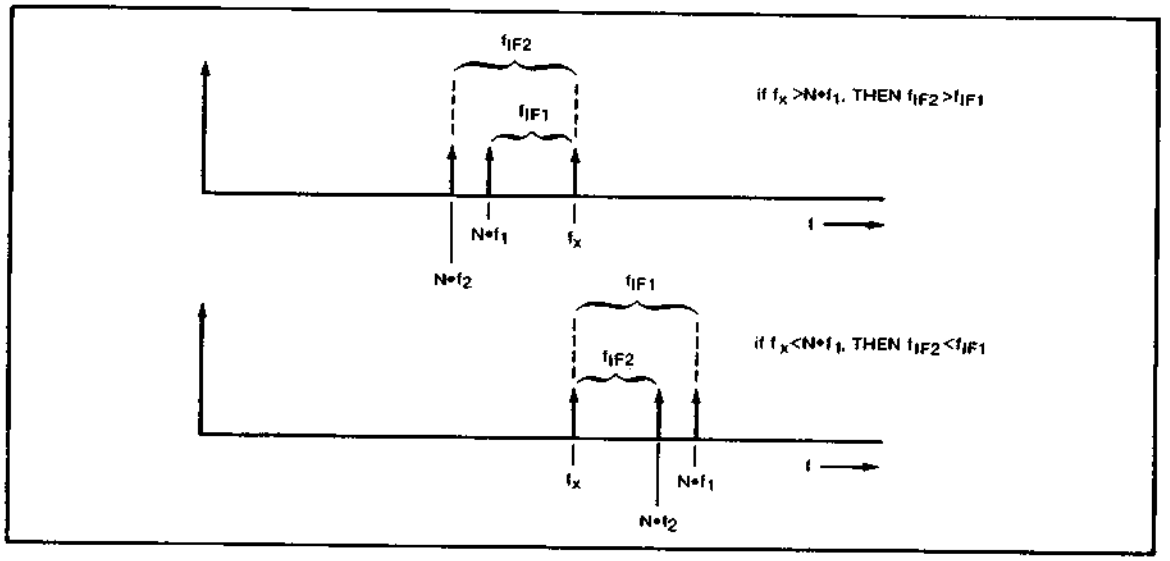


Figure 8-7. Frequency Relationships

8-91. If f_{IF2} is *less* than f_{IF2}, then N is computed from

$$N = \frac{f_{IF1} - f_{IF2}}{f_1 - f_2}$$

If f_{IF2} is *greater* than f_{IF1}, then N is computed from

$$N = \frac{f_{IF2} - f_{IF1}}{f_1 - f_2}$$

8-92. The unknown frequency is then computed from the following:

$$f_x = N \cdot f_1 - f_{IF1} \text{ } (f_{IF2} < f_{IF1})$$

$$f_x = N \cdot f_1 + f_{IF1} \text{ } (f_{IF1} < f_{IF2})$$

8-93. Since the frequency of the synthesizer is known to the accuracy of the counter's time base and the IF is measured to the accuracy of the counter's time base, the accuracy of the microwave measurement is limited only by the time base error and ±1 count error.

8-94. HP 5343A OVERALL OPERATION

8-95. If all signals into the counter could be guaranteed to have little or no FM, then the counter could operate quite simply as described previously. However, many signals in the microwave region, such as those originating from microwave radios, have significant amounts of frequency modulation. To prevent FM on the signal from causing an incorrect computation of N, the harmonic heterodyne technique is implemented as shown in *Figure 8-8* which is a simplified block diagram of the HP 5343A. The differences between *Figure 8-8* and the block diagram of *Figure 8-6* are:

a. Two synthesizers which are offset by precisely 500 kHz.

b. Two counters.

c. A multiplexer which multiplexes between the two synthesizer frequencies — when f_1 is driving the sampler driver, the IF_1 produced is measured by counter A and when f_1 drives the sampler driver, the IF_2 produced is measured by counter B.

d. A pseudorandom sequence generator which controls the multiplexer during N determination.

8-96. The overall operating algorithm for the block diagram of *Figure 8-8* is as follows: With the multiplexer having selected the main oscillator output, the main oscillator frequency, f_1, is swept from 350 MHz to 300 MHz in 100 kHz steps (the offset oscillator frequency, f_2, is maintained at f_1 - 500 kHz by a phase-locked loop) until the IF detector indicates the presence of an IF signal in the range of 50 MHz to 100 MHz. At this point, the synthesizer stops its sweep and the counter starts the harmonic number (N) determination. A pseudorandom sequence (prs) output by the prs generator switches between the main oscillator and offset oscillator as well as counter A and B so that counter A accumulates f_{IF1} (produced by $N \cdot f_1$ mixing with f_x) and counter B accumulates f_{IF2} (produced by $N \cdot f_2$ mixing with f_x). The pseudorandom switching prevents coherence between

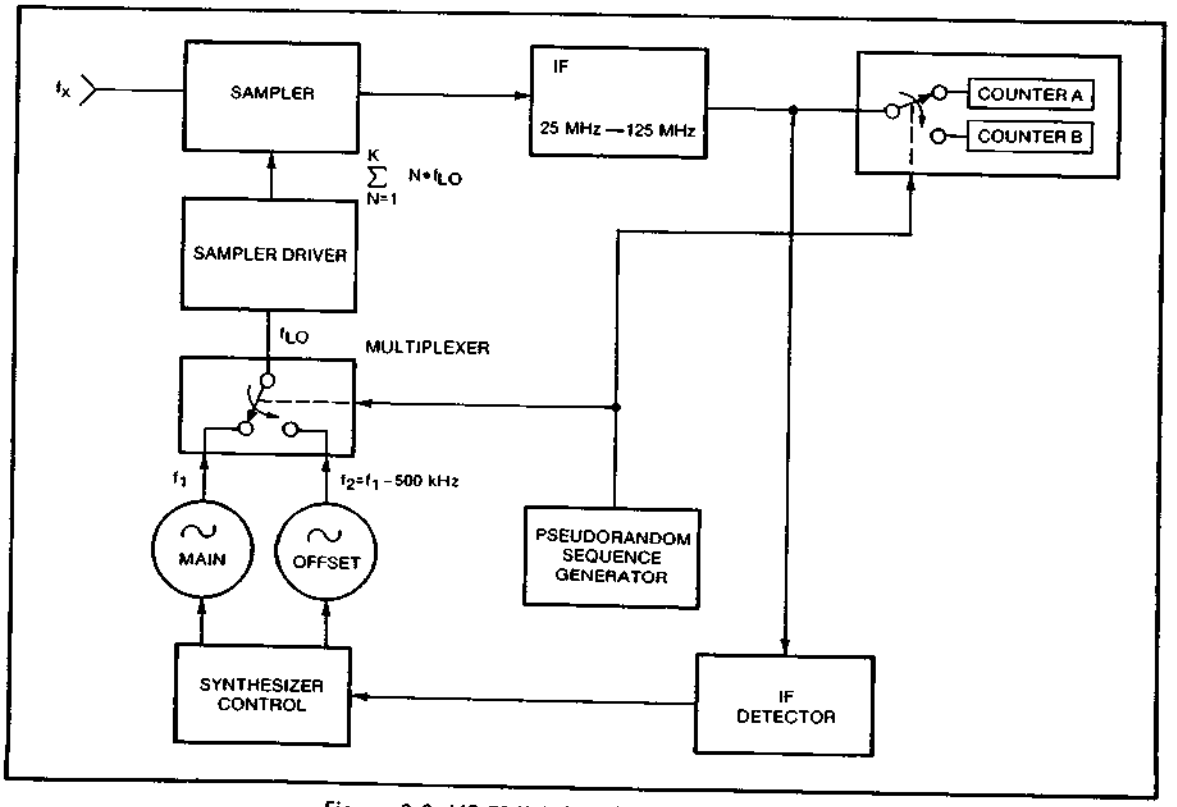


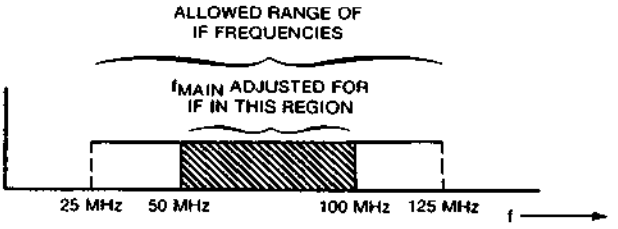
Figure 8-8. HP 5343A Simplified Block Diagram

the switching rate of the multiplexer and the modulation rate of the FM from producing an incorrect computation of N. Of course, during the sequence, each counter is enabled for exactly the same total amount of time. The N number and sign of the IF are computed as previously described since counter A accumulates f_{IF1}, and counter B accumulates f_{IF2}. The prs (pseudo-random sequence) is then disabled, the main oscillator is selected, and the frequency of f_{IF1} is measured in counter A to the selected resolution.

8-97. The total measurement time, then, consists of these three components: sweep time, N determination time, and gate time. The period of the sweep is 150 ms which is the worst case time to detect a countable IF. The normal prs for N determination lasts for 360.4 ms (a rear panel switch selects a longer prs for higher FM tolerance). The gate time required depends on the resolution. For 1 Hz resolution, the gate is 1 second. For gate times from 10 Hz to 100 kHz, the gate time is 4 s/Hz so that 1 kHz resolution is achieved in 4 ms. 1 MHz resolution takes a 10-microsecond gate time.

8-99. FM TOLERANCE

8-99. The worst case normal mode FM tolerance is 20 MHz p-p and occurs when the period of the modulation is near the period of the pseudorandom sequence which is 360.4 milliseconds. When the FM exceeds 20 MHz p-p, the computation of N may be in error by ±1 (round off error). For FM is excess of 20 MHz p-p, a wide range FM mode with a long prs is selectable (via a rear panel switch) which provides a worst case FM tolerance of 50 MHz p-p. In this case, however, the limiting factor is not round off in the computation of N but the allowable range of frequencies in the IF.



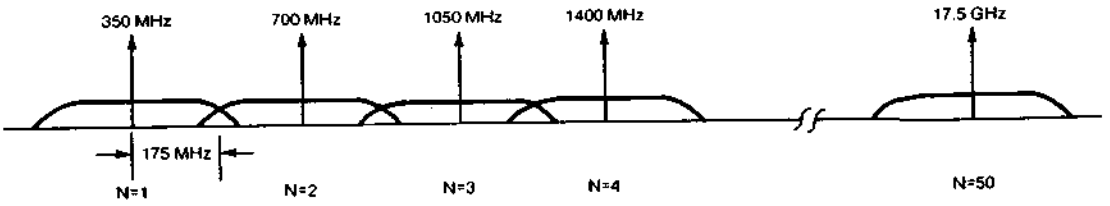
8-100. During the sweep, the frequency of the main oscillator is adjusted until f_{IF1} and f_{IF2} both fall within the range of 50 MHz to 100 MHz. In the worst case, when the IF occurs at 100 MHz or 50 MHz, the signal may deviate by a maximum of 25 MHz before crossing the band-edge of allowable IF frequencies. This gives a worst case FM tolerance of 50 MHz peak-to-peak. For the wide range FM, the period of the long pseudorandom sequence is 2.096 seconds which means that acquisition time is significantly longer for the wide range FM mode. The period of the short pseudorandom sequence (22.52 ms) provides shorter acquisition time and an FM tolerance of 6 MHz peak-to-peak.

8-101. AUTOMATIC AMPLITUDE DISCRIMINATION

8-102. The HP 5343A has the ability to automatically discriminate against lower amplitude signals in its range of 0.5—26.5 GHz in favor of the highest amplitude signal in the range. Thus, if there is 20 dB separation (typically better than 10 dB) between the highest amplitude signal and any other signal in the 0.5—26.5 GHz range, the counter automatically measures the highest amplitude signal.

8-103. Amplitude discrimination is a feature of the HP 5343A because of two design features: the bandwidth of the preamplifier, which is 175 MHz, means that there are no gaps between the power spectrums produced by mixing harmonics of the oscillator with the input; and limiting of all IF signals produced by inputs greater than the counter's sensitivity means that the IF is at the

frequency of the largest amplitude signal in the input spectrum and is frequency modulated by the lower amplitude signals. (This is the AM to PM conversion characteristic of limiters. The bandwidth and roll off of the preamp are chosen so that the PM does not introduce errors into the count.)



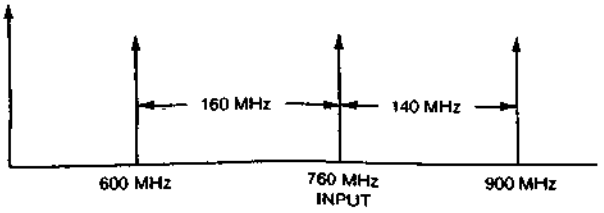
8-104. If there were gaps, then there could be a signal in the 0.5—26.5 GHz range which would not appear in the down converted IF. Thus, this signal, even if it were the largest, could not be measured.

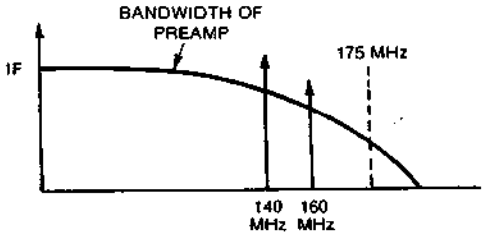
8-105. SENSITIVITY

8-106. The limiting factor in determining the sensitivity of the HP 5343A is the effective noise bandwidth of the IF. Since the IF signal to noise ratio must be kept at a value which insures that there are no noise induced errors in counting the IF signal, the noise bandwidth of the IF determines the noise power; and, therefore, sets the minimum input signal level.

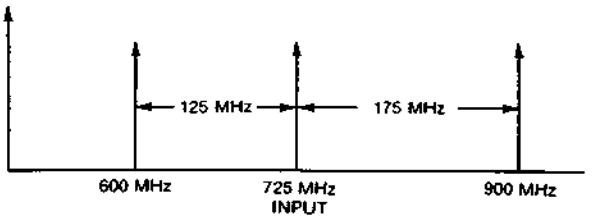
8-107. The IF Detector detects two parameters: one output is true if the IF signal is in the range of 50 MHz to 100 MHz and the input power level is greater than approximately -30 dBm; the other output is true if the IF signal is in the range of 25 MHz to 125 MHz and the input power level is greater than approximately -30 dBm. The detector thus insures that the input signal is sufficiently large to produce an IF with an acceptable signal to noise ratio. The 50 to 100 MHz IF output is used when sweeping since, to achieve the specified FM tolerance, the counter must center the IF somewhere in the range of 50 to 100 MHz. The 25 to 125 MHz output is used to ensure that the IF signal does not exceed those limits and that the input does not drop below -30 dBm. Either of these events occurring could cause a wrong computation for N.

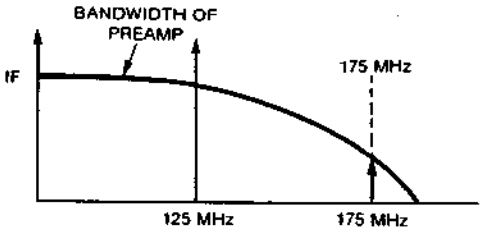
8-108. The reason the IF is restricted to a 25 to 125 MHz bandwidth is examined in the following: the actual bandwidth of the IF is approximately 175 MHz which is required for automatic amplitude discrimination. However, the counter restricts the countable IF to frequencies less than 125 MHz so as to prevent generating two IF signals — one generated by "N" times the main oscillator frequency and the other generated by "N±1" times the main oscillator frequency. If two IF signals are generated, then incorrect counting may result. By restricting the IF signal to be less than 125 MHz, the upper tone is of a high enough frequency as to be sufficiently attenuated by the 175 MHz bandwidth of the preamplifier so that no errors are introduced. Consider what would happen if IF frequencies to 175 MHz were allowed. Take the example of a 760 MHz input signal. By mixing with the second harmonic of 300 MHz, an IF of 160 MHz is produced. The input also mixes with the third harmonic of 300 MHz to produce another IF signal at 140 MHz. Neither signal is greatly attenuated by the 175 MHz bandwidth of the preamp as shown below and miscounting results because of interference between the two tones.





8-109. By limiting the IF to frequencies less than 125 MHz, the problem described in paragraph 8-108 does not occur. For the case of a 725 MHz input, the second harmonic of 300 MHz produces an IF of 125 MHz (the maximum allowable IF) and the third harmonic produces an IF of 175 MHz. But the IF signal at 175 MHz is attenuated by the 175 MHz bandwidth of the preamplifier as shown below so as to prevent errors in counting.





8-110. HP 5343A BLOCK DIAGRAM DESCRIPTION

8-111. *Figure 8-9* is a block diagram of the HP 5343A showing the major assemblies of the instrument. There are five major sections: The direct count section, the synthesizer section, the IF section, the time base section, and the control section. Each of these are discussed in the following paragraphs.

8-112. Direct Count Section

8-113. The direct count section consists of the A3 Direct Count Amplifier assembly and the A13 Counter assembly. Frequencies less than 500 MHz may be measured directly by the direct count input. The input signal, which is applied to the front panel BNC connector, is amplified and conditioned by the input amplfier on A3. The direct count main gate, also on A3, is enabled for a specific period of time (determined by the resolution selected) by the LDIR GATE signal from A17. During the time that the A3 main gate is enabled, counts pass through the main gate to Counter A on the A13 Counter assembly where they are totalized. At the conclusion of the gate time, the A14 Microprocessor assembly reads the contents of Counter A and sends the result to A1 Display along with the correct annunciators and decimal point. The microprocessor continually reads the status of a hardware flag on A17 which indicates the end of the sample rate delay. At the end of the delay, the measurement process begins again.

8-114. Synthesizer Section

8-115. The synthesizer section consists of a main oscillator and an offset oscillator to provide two output frequencies to A5 RF Multiplexer in the range of 300 MHz to 350 MHz which are locked to the counter's 10 MHz time base. The frequency is selected with 100 kHz resolution by the A14 Microprocessor. The main oscillator is formed by the A8 Main VCO assembly, the A9 Main Loop Amplifier assembly, and the A10 Divide-by-N assembly. The microprocessor controls the division factor N in A10 which determines the main oscillator frequency. The offset oscillator consists of the A4 Offset VCO assembly, the A7 Mixer/Search Control assembly, and the A6 Offset Loop Amplifier assembly. The offset loop is phase locked at a frequency 500 kHz below the main VCO frequency. *Figure 8-10* is a block diagram of the synthesizer section which is described in the following paragraphs.

8-116. Main Loop Operation

8-117. A buffered signal from the A8 Main VCO is fed back to the A10 Divide-by-N assembly. The division factor, N, is programmed by the A14 Control assembly and is chosen by the relation N= programmed frequency/50 kHz. For example, if the program requests a frequency of 346.7 MHz, then N would be equal to 6934 (=346.7/0.05). When the main loop is locked, the output of the divide-by-N circuitry on A10 is 50 kHz. This is compared to a 50 kHz signal which is derived from the time base and the phase error is sent to the A9 Main Loop Amplifier. The phase error signals, available at XA10(1) and $\overline{(1)}$, are used by the main loop to drive the VCO frequency to the programmed frequency.

8-118. The A9 Main Loop Amplifier sums and integrates the two phase detector outputs of A10. The error signal is then passed through one of two lowpass filters. When the HP 5343A is searching for an input signal in the range of 500 MHz to 26.5 GHz, the main loop VCO is programmed to step from 350 MHz to 300 MHz in 100 kHz steps in approximately 90 milliseconds. To achieve this fast search rate, a wideband lowpass filter of approximately 2 kHz bandwidth is selected. When the counter is actually making a measurement by opening the main gate and counting the IF frequency, a narrowband lowpass filter of approximately 100 Hz bandwidth is selected to achieve high spectral purity in the VCO output.

8-119. The error signal at the output of A9 drives the A8 Main VCO to a frequency which minimizes the error signal. Three buffered outputs are provided: one output is fed back to the A10 Divide-by N; another goes to the A5 RF Multiplexer; the third goes to the A7 Mixer/Search Control assembly and is used by the OFFSET LOOP to set the offset VCO to a frequency which is exactly 500 kHz below the Main VCO frequency.

8-120. Offset Loop Operation

8-121. The frequency of the main VCO and the frequency of the offset VCO are fed to a mixer on the A7 Mixer/Search Control asembly. The difference frequency at the output of the mixer is fed to a phase detector and a 500 kHz detector. The 500 kHz detector sends a search enable (HRSC EN) signal to the search generator on the A6 Offset Loop Amplifier if the offset VCO frequency is not 500 kHz less than the main VCO frequency. The search signal on A6 is a ramp waveform which drives the offset VCO to a frequency which is 500 kHz less than the main VCO frequency. When the 500 kHz detector on A7 detects the presence of 500 kHz, the search is stopped. The phase detector on A7 compares the difference frequency out of the mixer with a 500 kHz reference derived from the time base. The phase error signal is sent to A6.

8-122. The A6 Offset Loop Amplifier sums and integrates the two outputs of the phase detector on A7. This error signal keeps the offset VCO on a frequency which is 500 kHz below the main VCO frequency. To get the difference frequency out of the mixer on A7 into the capture range of the phase-locked loop formed by A7, A6, and A4, a search generator on A6 is turned on in the absence of a 500 kHz difference frequency. The generator sweeps the offset VCO over its range until the VCO is 500 kHz less than the main VCO (the LPOS Slope signal generated on A6, prevents the loop from locking on the upper sideband where the offset VCO is 500 kHz greater than the main VCO). At this point the search generator is disabled and the output of the phase detector on A7 keeps the loop locked.

8-123. The offset VCO has two buffered outputs: one goes to the A5 RF Multiplexer and the other is fed back to the A7 Mixer/Search Control assembly.

8-124. IF Section

8-125. The IF section amplifies the output of the U1 sampler and routes this IF to A13 for counting. It also provides digital outputs which indicate that the IF signal is of sufficient amplitude to be counted and that it is in the proper frequency range. The 1st and 2nd Preamplifier assemblies provide high gain amplification for the output of the sampler (the sampler has a –48 dB conversion efficiency which means that an input signal at a level of Ø dBm will yield an IF at approximately –48 dBm). The A11 IF Limiter assembly limits the amplitude of the IF signal. The A12 IF Detector assembly detects both the amplitude of the IF as well as the frequency of the IF. During the sweep, the microprocessor monitors the state of the 50 MHz—100 MHz detector output of A12 and stops sweeping when that detector output is true. At the conclusion of the N determination the latched 25 MHz—125 MHz detector output is checked. If this detector output is true, then the IF signal never varied beyond the 25—125 MHz range nor did it drop too low in amplitude. If the detector output is false, then the computation of N may be incorrect and the algorithm specifies that the sweep start at a frequency 100 kHz lower than where it previously stopped sweeping.

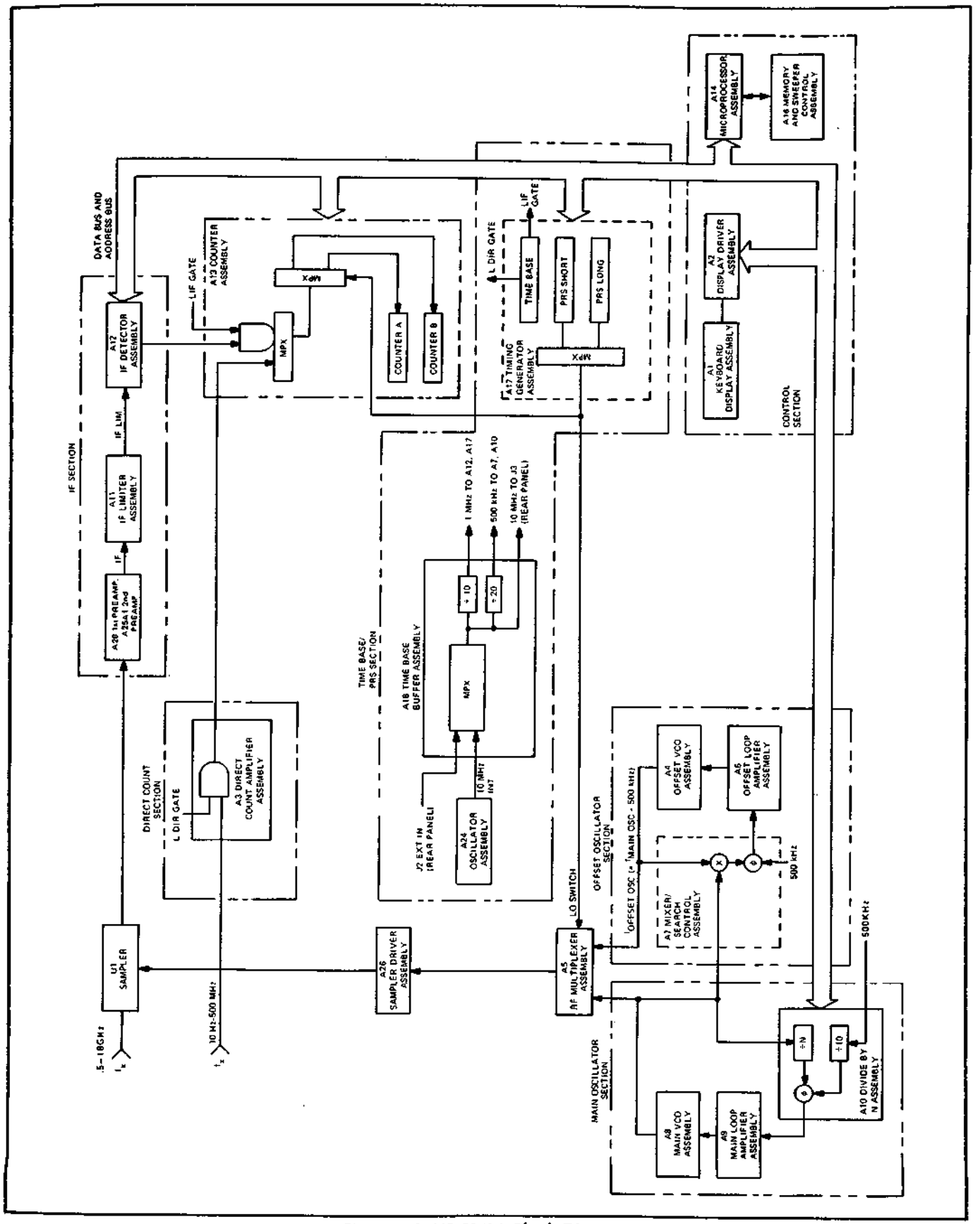


Figure 8-9. HP 5343A Block Diagram

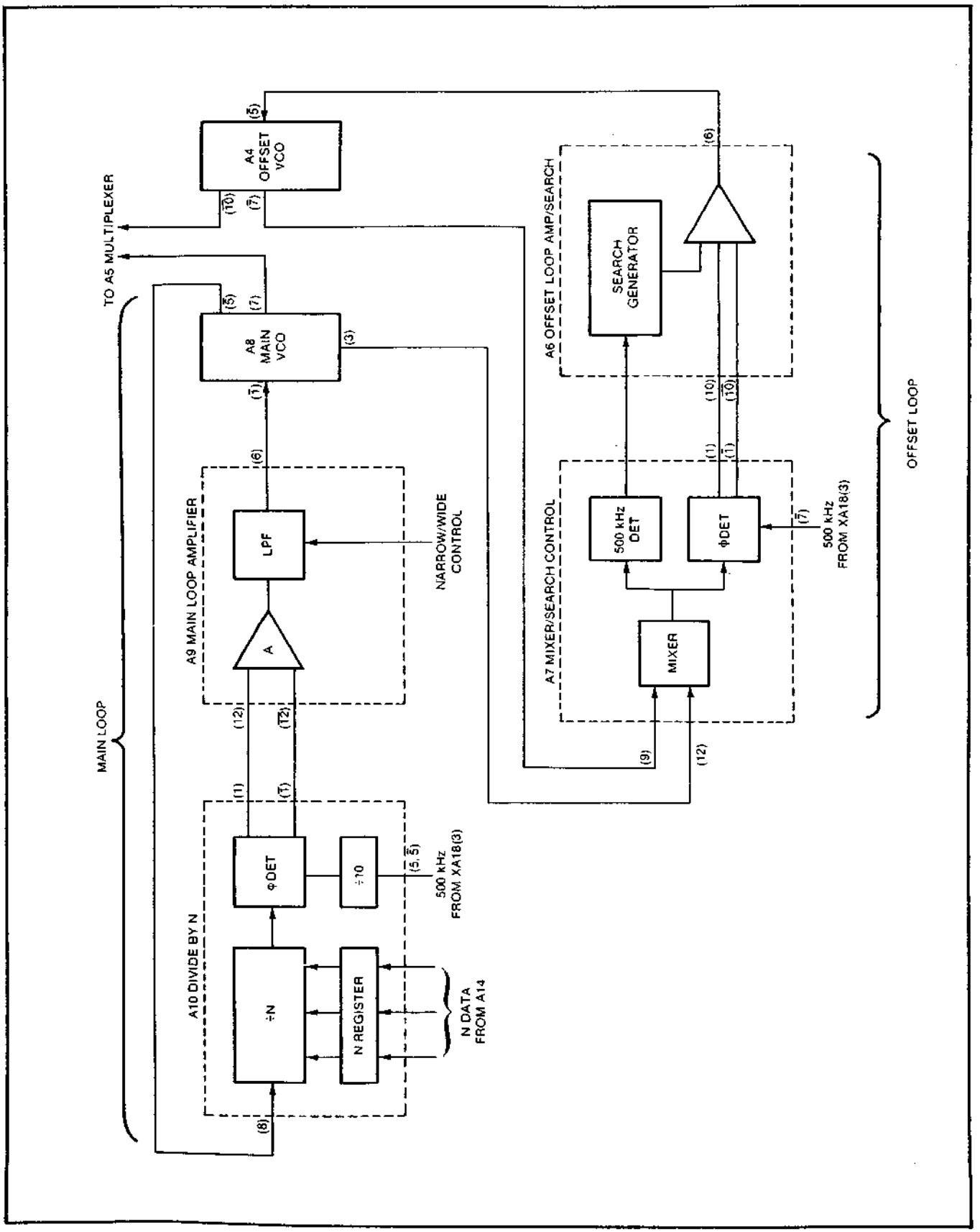


Figure 8-10. Block Diagram of Synthesizer Section

8-126. Time Base/PSR Section

8-127. The time base section consists of the A24 Oscillator assembly which provides a 10 MHz sine wave to the A18 Time Base Buffer assembly. A18 provides TTL compatible 10 MHz, 1 MHz, and 500 kHz outputs to the rest of the counter. The A17 Timing Generator assembly uses the 1 MHz signal to provide gate times from 1 microsecond to 1 second in decade steps as well as generate a pseudorandom sequence during the N determination portion of the algorithm. Based on the position of the rear panel FM switch, the microprocessor selects a normal prs (360.4 ms long) for 20 MHz p-p FM tolerance or a long prs (2.096 seconds long) for 50 MHz p-p FM tolerance or a short prs (22.56 ms long) for 6 MHz p-p FM tolerance.

8-128. Control Section

8-129. The control section is made up of the A14 Microprocessor assembly, the A2 Display Driver assembly, and the A1 Display assembly. The program stored in ROM on the A14 assembly controls the operating algorithm of the instrument. The A1 assembly is used by the operator to interface with the stored program. Via the A1 keyboard, the operator selects operating modes (AUTO, MANUAL, CHECK), resolution and offsets. The A1 assembly also displays measurement results. The A2 Display Driver assembly controls A1 and provides the interface with the A14 Microprocessor.

8-130. DETAILED THEORY OF OPERATION

8-131. The detailed theory of operation is provided in the following paragraphs in numerical order of the assemblies.

8-132. A1 DISPLAY ASSEMBLY AND A2 DISPLAY DRIVER ASSEMBLY

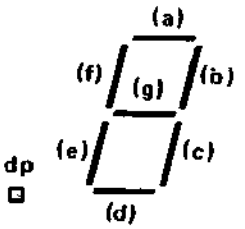
8-133. The A1 Display assembly and A2 Display Driver assembly shown in *Figure 8-24* operate together to provide the user interface with the microprocessor. For a description of microprocessor operation, refer to paragraph 8-228. The keyboard on the A1 Display permits the operator to input commands to the microprocessor. The display on the A1 Display is used by the microprocessor to display measurement results, error codes, and other information to the operator. As an example, consider what occurs when the SET key is pressed by the operator. Pressing the key generates an interrupt to the microprocessor. The program stops executing the current program and jumps to a subroutine to find out which device caused the interrupt and why. The subroutine determines that the keyboard generated the interrupt. Circuitry on A2 tells the microprocessor that the SET key was pressed. The program then sends commands to A2 to cause the light in the SET key to blink as well as the $\overline{\overline{\ \ }}$ code to be displayed, both of which act as prompters to the user. All of this occurs very quickly and is virtually transparent to the user.

8-134. The A2 Display Driver assembly is driven by a 6 kHz clock (scan clock) formed by Schmitt trigger U4E, feedback resistor R15, and capacitor C5. This clock is continuously running and outputs a TTL signal with a positive pulse width of approximately 40 μs. The output of the scan clock goes through a jumper (which may be removed to allow testing with a logic pulser to simulate the clock) and drives decade counter U3. The outputs of U3 are decoded by U14C and U5 to reset the U3 outputs to all TTL low after 13 clocks have been counted. These 13 states correspond to the 11 digits and 2 annunciator lines which need to be driven in the display.

8-135. The output of the U3 counter passes through 3-state driver U5. The purpose of U5 is to force invalid states into column scanner U2 and U8 so that on power-up, (when LDVRST goes low) the display is blank. On reset, the input to U10D goes low and the control to U5(1) goes high, which forces U5 to the high Z state. Pull up resistors R16(A,B,C,G) put state 16 into U8 and put state 7 into U2. Since these states are out of the normally operating range of the scanners, all display digits and annunciators are blanked.

8-136. In normal operation, U5(1) is low and the output of the 13 state counter drives BCD-to-decimal decoders U2 and U8. These two devices form a column scanner whose low output turns on, one at a time, A1 driver transistors Q13, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q1, Q2, Q11, Q12 for a period of approximately 166 μs (⅙ kHz). For example, when the 13 state counter reaches 0 1 1 1 (7), then U8(9) goes low, turning on transistor A1Q4 and applying +5.0V to the LED digit. Whatever segment inputs are low will thus be momentarily lighted. The correct code to be input to the LED digit is stored in TTL RAM A2U12 and U7. U7 and U12 each can store sixteen 4-bit words. When the 13 state counter is in state 0 1 1 1, then the inputs to RAM U12 and U7 are at 0 1 1 1 and the desired digits code is output, through A2U1 and U6, to the selected digit. Limiter resistors R1-R13, R16 limit the current through the LED segments when the NAND gate output (U6 and U1) goes low. When the 13 state counter reaches 1 0 0 0, then the input to U2 looks like Ø Ø Ø Ø and U2(1) goes low which applies +5.0 volts to Q1 and lights DS13. When the 13 state counter reaches 1 1 0 0 (12, 13th state since started at Ø), then the input to U2 is 0 0 1 0 and U2(5) goes low and one or more annunciator lights are turned on according to the code stored in RAM U12, U7.

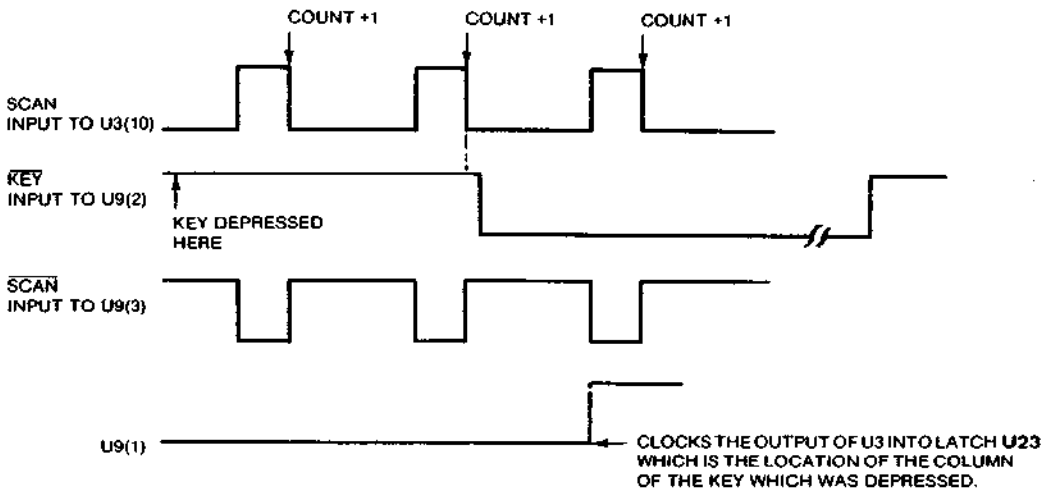
8-137. HDSPWRT comes in at A2J1(3). When this signal is high, data is written into RAM U7, U12 from the microprocessor for display. When HDSPWRT goes low, the output of U14C is low and quad multiplexer U18 selects its "1" inputs. Thus, the output of the 13 state counter increments through 13 locations in RAM and causes the contents of RAM to be displayed. When HDSPWRT is high, U18 selects its "Ø" inputs. The write enable inputs to U12 and U7 pin 3 are enabled and data appearing on the DØ through D7 data lines is stored at the addresses appearing on the AØ through A3 address lines. Segments are labeled as shown below. DØ lines sends (a) segment information; D1 sends (b), D2 sends (c), D3 sends (d). Segments (a), (b), (c), and (d) are stored in U12. The D4 data lines sends (e) segment information, D5 sends (f), D6 sends (g), D7 sends decimal point. Segments (e), (f), (g), (dp) are stored in U7. For example, if it were desired to display 2 in the DS21 or least significant digit, then segments (a), (b), (g), (e), and (d) must be lighted.



To light these segments the following action occurs. In address location 1 1 1 1 (the output of U18 is inverted in U12, 1 (=D1) 1 (=D2) Ø (=D3) 1 (=D4) are stored. In address location 1 1 1 1 in U7, 1 (=D1) Ø (=D2) 1 (=D3) Ø (=D4) are stored. When the 13 state counters puts out Ø Ø Ø Ø, then the output of U12 will be 1 1 Ø 1 (5, 7, 9, 11) and the output of U7 will be 1 Ø 1 Ø (5, 7, 9, 11). The column scanner has output U8(1) low and all other outputs high (U2(10) is also low but it is not connected to any digit). Thus +5.0 volts is applied to DS21 and the correct segment inputs to DS21 are grounded to turn on segments (a), (b), (g), (e), and (d) which forms a digit 2. The DØ—D3 data lines and AØ, A1 address lines are also connected from driver U18 to the Option 004 (DAC) circuit on A2 assembly, *Figure 8-25*. Refer to paragraph 8-306 for Option 004 circuit description.

8-138. Keyboard Operation

8-139. When a key (pushbutton switch) is depressed, it is not immediately recognized but must wait until the column scanner reaches that particular key. However, since the scan rate is 6 kHz, this is much faster than the operator can depress and withdraw his finger. When the column scanner places a low on the line connected to the key which has been depressed, a low pulse is generated on the output of A2U4(4). This pulse is called $\overline{\text{KEY}}$ and when low, indicates that a key has been depressed.



8-140. With $\overline{\text{KEY}}$ low and $\overline{\text{SCAN}}$ low, U9(1) goes high which clocks latch U23 and causes it to store the address (0000 to 1100) of the column of the key which was pushed. Since there are two keys per column, another line is used to indicate top or bottom row. The output of U9(1), which clocks U23, also clocks U20A. U20A(5) will be low if a top row key is pushed and will be high if a bottom row key is pushed. In this manner, the microprocessor determines exactly which key has been depressed.

8-141. Flip-flop U19A is also clocked by the output of U9(1). Its output at U19A(5) will be high anytime that a key is pushed. It is reset to low when the 13 state counter reaches the end of the scan at state 1100. The low signal at U2(5) causes the output of U9(10) to go momentarily low and reset U19A. The End of Scan signal at the output of U9(13) clocks U20B and, if U19A(5) is high, will clock a high into U20B(9). This output is the Key Down signal. Key Down high goes to U23(9, 10) and inhibits other addresses from being latched. U20B(9) is also used as part of the Recall subroutine. To recall a value, the recalled value will be displayed as long as its associated key is depressed. The program examines the output of U20B(9) and if it remains high, continues to display the recalled value. When the key is released, U20B(9) will be reset by End of Scan and the program, upon detecting this, stops displaying the recalled value and displays the original display (e.g., frequency).

8-142. Flip-flop U19B stores the interrupt. U20B(9) going high at the end of the scan clocks a high into U19B(9). This is inverted by U10 and becomes LIRQ which interrupts the microprocessor. The program jumps to a service routine which, upon determining that the keyboard has requested service, issues a low keyboard read command LKBRD. This signal enables three-state latch U23 which puts out its contents onto the bus. LKBRD also enables the three-state buffer U13 which puts out the contents of U20A, U19B, and the position of the front panel RANGE switch. The program determines which key was pressed and acts accordingly. The LKBRD also resets the interrupt flip-flop U19B.

8-143. The processor monitors J1(15) [input impedance select] to check if operation is in direct mode (10 Hz—500 MHz) or 500 MHz—26.5 GHz mode.

8-144. HDSP WRT is sent from U4(8) via single-shot U11 to provide the write pulse to U7(3) and U12(3). Capacitor C6 prevents noise triggering of U11.

8-145. A3 DIRECT COUNT AMPLIFIER ASSEMBLY

8-146. The input signal is applied to the BNC connector and switch S23 on the A1 Display assembly as shown in *Figure 8-24* (upper left of A1 schematic). Switch S23 routes the signal

through either a 1 MΩ path or a 50Ω path to A3. As shown in *Figure 8-26*, the Z switch transistors Q7 and Q6 bias the 1 MΩ input at pin 8 of U7 and the 50Ω input at pin 7 of U7 to turn balanced amplifier U7 either on or off, depending upon which signal path has been selected by switch S23. The impedance select line biases pin 7 or 8 approximately −2 volts (50Ω) or −3.3 volts (1 MΩ).

8-147. The 50Ω signal path consists of clamping diodes CR8, CR5, and the limiting diode bridge formed by CR3, CR4, CR6, CR7 which limit the output to 1 volt peak-to-peak.

8-148. The 1 MΩ path consists of ac coupling capacitor A1C1, resistor A1R13 (on A1 Display assembly) to A3 compensation network C8, R13, clamping diodes CR1, CR2, source follower Q3, and emitter follower Q1. Field effect transistor Q2 is biased as a current source for Q3.

8-149. Balanced amplifier U7 provides complementary outputs of the input signal increased in amplitude by times 2. These complementary outputs drive differential amplifier U6 which provides amplification of times 10 so that the overall gain from U7 input to U6 output is approximately times 20. A portion of the output of U6 is integrated by U3, C17 to provide a dc voltage proportional to amplitude. This voltage provides AGC to U7 so that the input to Schmitt trigger U5 remains relatively constant. The output of U5 is a 0V to −650 mV signal which is divided-by-2 in U4 and divided-by-2 in U1. The main gate on U4 passes the output of U5 on to the dividers only when it is enabled by the LDIR GATE signal from A17 going low.

8-150. The DIRECT A output passes through EECL to TTL converter formed by Q8, Q9 to A13 where it is ready by the microprocessor. The DIRECT B output passes through EECL to ECL converter U2 to A13 where it is counted by the A counter.

8-151. HECL RSET high clears U4, U1 before LDIR GATE opens the main gate for counting.

8-152. A4 OFFSET VCO

8-153. The A4 OFFSET VCO (*Figure 8-27*) is essentially identical to the A8 MAIN VCO assembly described in paragraph 8-172, with the exception that A4 has one less buffer amplifier. The OFS OSC amplitude at XA4($\overline{10}$) should be approximately 600 mV rms and OFS OSC at XA4($\overline{7}$) should be approximately 300 mV rms. Measure with a high impedance RF millivoltmeter, such as the HP 411A.

8-154. A5 RF MULTIPLEXER ASSEMBLY

8-155. The A5 RF Multiplexer assembly shown in *Figure 8-28*, receives two input signals: MAIN OSC from the A8 Main VCO assembly at XA5($\overline{10}$) and OFFSET OSC from the A4 Offset VCO assembly at XA5($\overline{1}$). Upon command by the LO SWITCH signal from the A17 Timing Generator assembly, MAIN OSC (if LO SWITCH is TTL high) or OFFSET OSC (if LO SWITCH is TTL low) is gated to the output of A5 and becomes the LO FREQ signal which drives the A26 Sampler Driver.

8-156. The oscillator signals enter A5 at a level of approximately +4 dBm at XA5($\overline{1}$) for the OFFSET OSC and XA5($\overline{10}$) for the MAIN OSC. After passing through 6 dB matching pads formed by R8, R7, R6, and R22, R21, R20, both signals are amplified by differential amplifiers; U1 amplifies OFFSET OSC and U4 amplifies MAIN OSC. The amplified outputs pass through ac coupling capacitors C6 and C20, respectively, and then are either blocked or passed by diode switches. The offset channel switch is composed of CR3, CR1, CR2, and the main channel switch is composed of CR5, CR6, CR4. With the LO SWITCH signal TTL high, the base of Q3 increases to approximately 3.8 volts which decreases the current through the Q3 emitter. Since the differential amplifier formed by Q2, Q3 is driven by constant current source Q1, the current through the Q2 emitter increases since the total current must remain constant. This causes the voltage dropped across R27 to decrease (because the current decreased) so that the collector of Q3 is at −0.8 volts. Since the

voltage dropped across R18 increases, the collector of Q2 goes to +0.8 volts. The -0.8 volts at the Q3 collector is passed through the decoupling network L1, L2, C2 which prevents the 300—350 MHz signal in one channel from passing through the switching network over to the other channel. A -0.8 volt at the cathode of CR1 causes CR1 to be foreward biased and CR2, CR3 to be reversed biased, thereby blocking the OFFSET OSC signal. The +0.8 volt at the cathode of CR6 reverse-biases CR6 and forward-biases CR5 and CR4, thus permitting the MAIN OSC signal to pass in to the differential amplifier U2. With LO SWITCH TTL low, the current through Q3 increases and the operation is reversed.

8-157. The output of the U2 differential pair drives common emitter amplifier U3 which uses one-half of a differential transistor pair. The output, at a level of approximately +15 dBm, is ac coupled through C25 and sent to the A26 Sampler Driver.

8-158. A6 OFFSET LOOP AMP/SEARCH GENERATOR ASSEMBLY

8-159. The A6 Offset Loop Amplifier/Search Generator assembly (*Figure 8-29*) consists of:

a. A filter and amplifier which condition the phase error signal from A7 for locking the offset loop.

b. A search signal generator which drives the offset VCO such that the difference frequency between the offset VCO and the main VCO is within the capture range of the offset phase-locked loop. A signal, called LPOS Slope, is generated on A6 which prevents the loop from locking up when the offset VCO is 500 kHz above the main VCO; this insures that the offset VCO is always 500 kHz *below* the main VCO.

8-160. The search generator consists of transistor Q4, Schmitt trigger NAND gates U1A, U1B, U1D, diodes CR3, CR4, and the integrator formed by operational amplifier U2 and integrating capacitor C10. This integrator is also used by the error signals from A7 and is part of the compensation for the phase-locked loop.

8-161. Variable resistors R1 (SWEEP CENTER FREQ) and R2 (SWEEP RANGE) are adjusted to provide a triangular waveform at test point TP1 of -4 to +4 volts which corresponds to a VCO search frequency range of approximately 380 MHz to 270 MHz.

8-162. With HSRCH EN low, both diodes CR3 and CR4 are reversed-biased and the search generator is effectively isolated from the integrator U2. With HSRCH EN low, the loop is maintained in a locked condition by the phase error signals at XA6(10) and XA6($\overline{10}$). These signals are summed and integrated by U2 and then filtered by the low pass filter formed by R21, C12, and R20. The error signal drives the offset VCO to maintain a constant 500 kHz offset.

8-163. Two voltage regulators convert the +15 and -15 volt inputs to +12 and -12 volts, respectively. The +12 volt regulator consists of transistor Q2, diode CR1, resistors R4, R6, and capacitors C1 and C3. The -12 volt regulator consists of transistor Q3, diode CR2, resistors R8 and R11, and capacitors C8 and C6.

8-164. When the 500 kHz detector on A7 detects that there is not a 500 kHz difference frequency present, the HSRCH EN at XA6(8) goes TTL high and enables U1A and U1B. Since U1D(13) is tied to +5V, it is already enabled. The threshold voltages for U1D(12) are 0.8 volts and 1.6 volts which means that a logic 1 condition is not recognized until the input to U1D(12) moves from below 0.8 volts up through 1.6 volts. A logic 0 condition does not occur until the signal moves from above 1.6 volts down through 0.8 volts. Assuming a 0.8 volt level at U1D(12) to start with, the operation is as follows: U1D(11) is high, which drives U1B(6) low and U1A(3) high. With U1A(3) high, Q4 is *turned off and* CR4 is reversed-biased since the voltage at U2 inputs is at +1.5 volts. Since U1B(6) is low, CR3 is forward-biased and sinks current from the integrating capacitor C10. This causes the voltage at the output of operational amplifier U2(6) to increase linearly until the voltage at U1A(2)

crosses above 1.6 volts. With the output of U1A(3) high, the LPOS Slope signal is high and prevents the loop from locking up on an offset VCO signal which is 500 kHz higher than the main VCO. This is so because with LPOS Slope high, the offset VCO is changing from its high frequencies to lower frequencies. A 500 kHz difference frequency resulting from this sweep would be on the upper sideband. With LPOS Slope low, the offset VCO is changing from low frequencies to higher frequencies. A 500 kHz difference resulting from this sweep only occurs if the offset VCO frequency is 500 kHz less than the main VCO frequency.

8-165. When the sweep ramp present at U1D(12) crosses above the upper threshold of 1.6 volts, the output of U1D(11) goes low, U1B(6) goes high and U1A(3) goes low. This causes Q4 to conduct which forward-biases CR4. Since U1B(6) is high, CR3 is reversed-biased. Current is now supplied through CR4 to the intergrating capacitor C10. This causes the output of U2(6) to decrease linearly. Since U1A(3) is low, LPOS Slope is TTL low and the loop is allowed to lock once a 500 kHz difference frequency is detected on A7. When lock is achieved, HSRCH EN goes TTL low which causes U1B(6) and U1A(3) to both go TTL high, thereby reverse-biasing both CR4 and CR3. The voltage at the output of U2(6) is therefore maintained at that level which achieved lock. The timing diagram for this operation is shown in *Figure 8-11*.

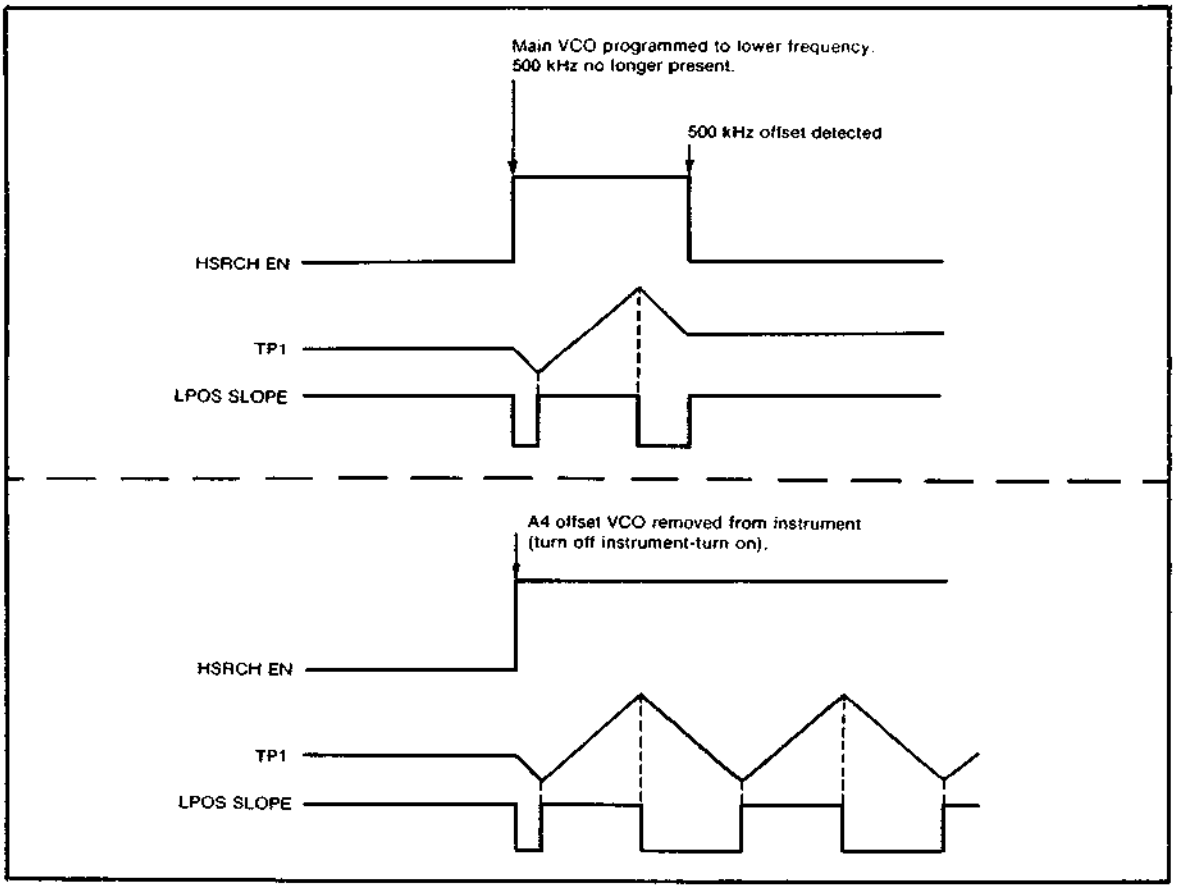


Figure 8-11. Timing Diagram of A6 Search Generator Operation

8-166. A7 MIXER/SEARCH CONTROL ASSEMBLY

8-167. The output of the main loop VCO, which comes in at XA7(12), *Figure 8-30*, is amplified by differential pair U4 to a level of approximately +5 dBm and is half-wave rectified by transistor Q6 whose base-emitter junction is used as the rectifying diode. The output of the offset VCO, which comes in at XA7(9), is amplified by U3 to a level of approximately 0 dBm and is applied to the base of Q1. Since Q1 is being alternately turned on and off by the Main VCO signal appearing at the Q1 emitter, the output appearing across R15 contains the sum and difference frequencies $f_{MAIN} \pm f_{OFFSET}$ (if $f_{MAIN} > f_{OFFSET}$) or $f_{OFFSET} \pm f_{MAIN}$ (if $f_{OFFSET} > f_{MAIN}$). Since Q2 is a low frequency

transistor, the sum frequency is attenuated and only the difference frequency is amplified. At test point TP1, the difference frequency at an amplitude of Ø to 5V is available.

8-168. To insure that the offset phase-locked loop locks up only when a 500 kHz difference frequency is produced by the Main VCO being 500 kHz greater (not less) than the offset VCO frequency, three control signals are produced which control the search enable flip-flop U2. When the HSRCH EN output at XA7(2) is TTL high, the triangle search waveform on A6 is enabled. HSRCH EN goes low when the U2(3,4,5) inputs are all low. This occurs when the following conditions are met:

a. The output of the 500 kHz detector is low.
b. The U1(2) equal frequency output is low.
c. The LPOS Slope signal from A6 is low.

8-169. The 500 kHz detector consists of the low-pass filter formed by resistors R5, R6, and capacitor C16, a full-wave rectifier formed by diodes CR1, CR2, and capacitor C22, and emitter follower Q3. For signal less than approximately 1 MHz, the full-wave rectifier produces a level at the base of transistor Q4 sufficient to turn Q4 on. This developes a voltage across resistor R3 which turns transistor Q5 on. The collector of Q5 then drops from a TTL high to a TTL low.

8-170. U1 is a phase detector which produces fixed amplitude variable duty cycle pulse trains at its two outputs. The duty cycle of the pulse train is proportional to the phase difference between the signals at its inputs. The OFFSET $\Delta\phi 1$ and OFFSET $\Delta\phi 2$ outputs are summed, integrated, and amplified by A6 to provide a dc control voltage to the A4 OFFSET VCO. When the frequency at U1(1) is less than or equal to the 500 kHz reference frequency at U1(3), U1(2) goes TTL low. A TTL low at U2(4) is necessary but not sufficient to disable the search waveform on A6.

8-171. The third input to the NOR gate on U2 is the LPOS Slope signal from A6. This signal is TTL low when the search signal from A6 is sweeping the A4 VCO from low frequencies to high frequencies. Consequently, if a 500 kHz difference frequency is obtained and LPOS Slope is low, then the offset VCO must be 500 kHz less than the main VCO.

8-172. A8 MAIN VCO ASSEMBLY

8-173. The synthesizer uses two voltage controlled oscillators which are essentially identical in operation (A8 and A4). The oscillator circuit shown in *Figure 8-31* consists of transistor Q1, feedback capacitor C7, and varactor diodes CR1 and CR2. Resistors R14 and R13 provide dc bias for Q1. Capacitor C11 resonates with the inductance of ferrite bead E1 to provide a low impedance path to ground for frequencies in the range of the VCO, thus eliminating parasitic oscillations. Transistor Q1, which is operating a common base mode for the VCO frequency range, has a portion of the output signal at its emitter fed back to its collector via capacitor C7. This positive feedback sets up oscillations at a frequency equal to the parallel resonant frequency of the tank circuit formed by varactor diodes CR1 and CR2 and the inductance of a metal trace on the A8 board. By changing the MAIN VCO CONTROL voltage at A8($\overline{1}$), the capacitance of the varactors change which changes the resonant frequency of the tank circuit and hence the frequency of oscillation. The modulation sensitivity of the VCO is approximately –12.5 MHz/volt. For a MAIN VCO CONTROL voltage at A8($\overline{1}$) of +2 volts, the VCO frequency should be approximately 300 MHz while a control voltage of –2 volts results in an output frequency of approximately 350 MHz.

8-174. A voltage regulator, consisting of 11-volt Zener diode CR3, transistor Q2, resistors R21, R22, R23, and capacitor C1, is used to provide low noise dc power to the oscillator circuit since any noise on the power supply of the oscillator will degrade the oscillator's spectral purity. Potentiometer R22 is used to adjust the output voltage of the voltage regulator circuit so that the free-run frequency of the VCO (i.e., the frequency with Ø volts at the MAIN VCO CONTROL A8($\overline{1}$) input) is 325 MHz ±2 MHz. The nominal voltage which achieves this free-run frequency is 8.5 volts and is measured at the junction of C20 and CR2. Inductor L8, capacitors C23 and C16, and resistor R19 provide further filtering for the dc power to the VCO.

8-175. The output of the VCO is sent to three buffer amplifier U1, U2, and U3. Capacitor C4 is a dc blocking capacitor. The differential transistor pairs contained in U1, U2, and U3 provide +6 dB, +8 dB, and +6 dB gain, respectively. The gain is determined by the dc current flowing through the emitters of the transistors. This current is set by the networks connected to pin 3 of the IC. Decoupling networks L7 and C15, L1 and C3, L4 and C8, L11, C22, C24, C25, C26 isolate the -5.2 volt power from the RF signal. Decoupling networks L5 and C10, L2 and C5, L9 and C14, and L12, C18, C27, C28, C29 isolate the +5 volt power from the RF signal. The output of each buffer amplifier, after removal of the dc component by dc blocking capacitor C17, C6, or C12, is transmitted to other parts of the instrument over a 50Ω microstrip transmission line. The ground plane of the microstrip board is connected to the ground plane of the motherboard. The output at XA8($\overline{5}$) and XA8(3) should be approximately 250 mV rms while the output of XA8(7) should be approximately 500 mV rms.

8-176. A9 MAIN LOOP AMPLIFIER ASSEMBLY

8-177. The two variable duty cycle pulse outputs from the phase detector on A10, Main $\Delta\phi 1$ and Main $\Delta\phi 2$, are summed and integrated by U2 on the A9 Main Loop Amplifier assembly, shown in *Figure 8-32*. Bidirectional switch U3(B, C, and D) controlled by D flip-flop U1B, selects the compensation for the phase-locked loop by selecting one of two feedback paths around operational amplifier U2 and by selecting one of two low pass filters in the output. When the HP 5343A is searching for an input signal, the wideband filter is selected. When the HP 5343A is making an actual measurement, the narrowband filter is selected.

8-178. When the least significant bit of the data bus from A14(DØ), is a logic 1 and the LPD Write address is decoded on A14 so that LPD Write goes high, then U1(8) goes low which selects the wideband filter consisting of inductors L1, L2, capacitors C2, C12, C16, C11, and C1. With U1(8) low and U1(9) high, transistor Q3 is turned on and provides +5.6 volts to control pins U3(6) to turn on the switch; transistor Q2 is turned off, thus providing a -5.6 volt level to control pins U3(5) and U3(12) to turn off the switch.

8-179. When DØ is a logic Ø and LPD Write goes high, U1(9) goes low and U1(8) goes high. This selects the narrowband filter consisting of L3, C8, C9, and C10 and also selects the R15 feedback resistor connected to U2. With U1(9) low, Q2 is turned on so that +5.6 volts is applied to control pins U3(5) and U3(12) to turn on the switch. With U1(8) high, Q3 is off and -5.6 volts is applied to control U3(6) to turn off the switch.

8-180. The voltage regulator consisting of transistor Q4, diode CR4, resistors R10, R11, and capacitor C17 converts +15 volts to +5.6 volts and the voltage regulator consisting of transistor Q1, diode CR1, resistors R1, R3, and capacitor C3 converts -15 volts to -5.6 volts.

8-181. A10 DIVIDE-BY-N ASSEMBLY

8-182. The A10 Divide-by-N assembly is essentially a programmable frequency divider and phase detector. As shown in *Figure 8-33* the output of the A8 Main VCO enters at DIV N XA10(8), and is initially divided by two by the ECL D flip-flop U6. The divider chain formed by U12, U9, U13, U14, and U8 divides the output of U6(4) by N. The division factor N is programmed from the A14 Microprocessor assembly via the data bus lines. The output of the divider chain goes from U8 through U3B to the U2 phase comparator where it is compared to a 50 kHz reference frequency. The phase error outputs of the U2 phase comparator, MAIN $\Delta\phi 1$ and MAIN $\Delta\phi 2$, are conditioned by the A9 Main Loop Amplifier and cause the A8 MAIN VCO to go to that frequency which, when divided by N in the divider chain on A10, produces a 50 kHz output.

8-183. Registers U10, U15, and U7A provide storage for the BCD encoded N data sent from A14 and registers U16, U11, and U17 provided buffer storage for the N data. Decade divider U1 outputs a 50 kHz reference frequency to U2 against which the N divided VCO frequency is compared.

8-184. The N divider chain formed by U12, U9, U13, U14, and U8 is programmed by the A14 Microprocessor assembly with a 4-digit positive-true BCD encoded number which is the 9's complement of the desired main VCO frequency. The main VCO frequency may be programmed with 100 kHz resolution. To program the main VCO to a frequency of 342.6 MHz, for example, the program would want N to be 6573 (9's complement of 3426). The actual overall division factor is

$$\frac{342.6}{0.050} = 6852$$

8-185. Since the data bus is only 8-bits wide, the 4-bit BCD encoded N number is divided into two 2-bit bytes. The two more significant bits form the upper byte and the two lower significant bits form the lower byte. The upper byte is first loaded into U17 when LSYH, decoded on A14, goes high. Since the range of VCO is 270 to 380 MHz, the most significant digit of the N number will be either a 6 or 7 (9's complement of 3 and 2, respectively). In BCD, this means that only the least significant bit of the BCD encoded most significant digit of the N number need be sent. If the most significant digit of N is 6, then the D4 input will be a low. If MSD of N is 7, then D4 will be high. U7A stores the D4 bit and presents it to U8 which represents the most significant digit of the N number.

8-186 The lower byte is loaded into U16 and U11 when LSYL, decoded on A14, goes high. The data, which has been temporarily stored in U16, U11, and U17, is next transferred to U10, U15, and U7A by the operation of U4A and U4B. When LSYL goes high, a high is clocked into U4A(5) and is presented to U4B(12). The next positive transition at U4B(11) causes U4B(8) to go low, which clears U4A(5). The following positive transition at U4B(11) then clocks U4B(8) high. The low to high transition of U4B(8) loads the data into U10, U15, and U7A. *Figure 8-12* shows the timing of this operation.

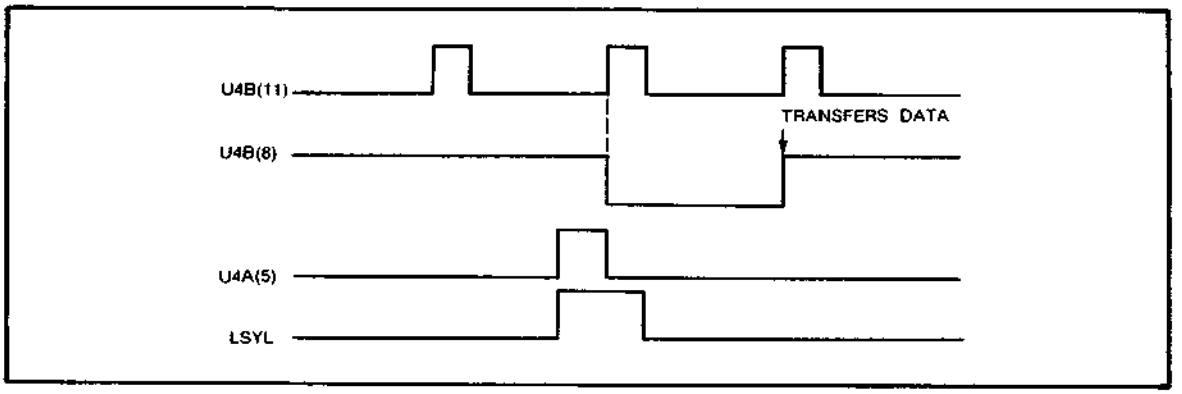


Figure 8-12. Data Transfer Timing in A10 Circuit

8-187. For example, if the program wants to set the main VCO to 342.6 MHz, the following data would be sent:

D7	D6	D5	D4	D3	D2	D1	D0	CONTROL SIGNAL
1†	d*	d*	1	0	1	0	1	LSYH
results in 6 in U8 (9's complement of 3)				5 (9's complement of 4)				

*don't care digits
†not check if 1 (check if = 0)

This would be followed by:

D7	D6	D5	D4	D3	D2	D1	D0	
0	1	1	1	0	0	1	1	LSYL
7 (9's complement of 2)				3 (9's complement of 6)				

8-188. The most significant bit in the upper byte is used to indicate the CHECK condition. If U17(12) is low, the D flip-flop U5 is enabled and the output of U6 is again divided by two. In CHECK mode, the main VCO is programmed to 300 MHz. The CHECK signal at XA10($\overline{11}$) is 300 MHz divided by four so that the 5343A displays 75 MHz in CHECK. In CHECK, the following outputs should be present:

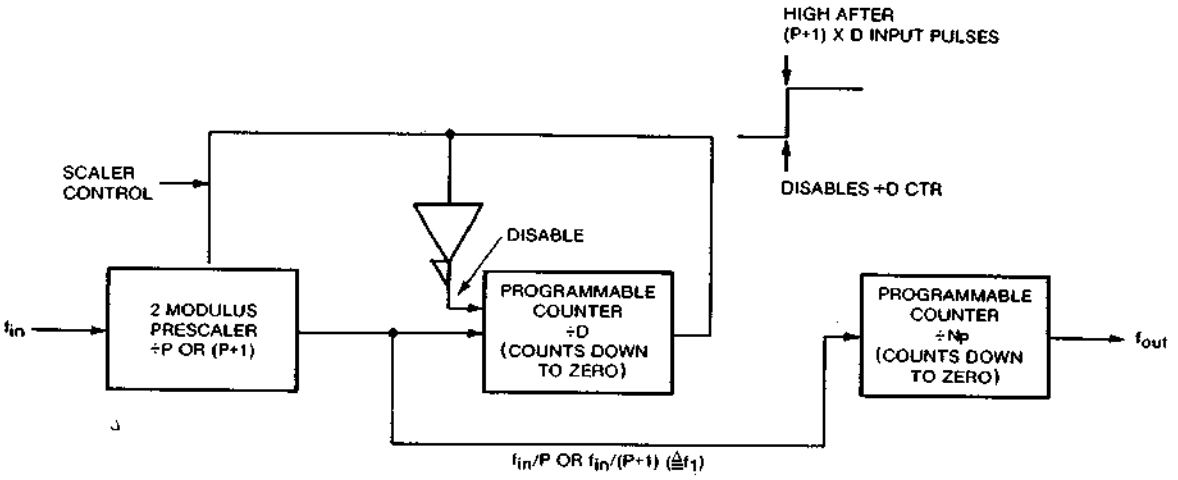
U16(15)	1	LSB	Least significant BCD digit (9's complement of Ø)
U16(10)	Ø		
U16(2)	Ø		
U16(7)	1	MSB	
U11(7)	1	LSB	Digit 2 (9's complement of Ø)
U11(2)	Ø		
U11(15)	Ø		
U11(10)	1	MSB	
U17(2)	1	LSB	Digit 3 (9's complement of Ø)
U17(5)	Ø		
U17(7)	Ø		
U17(10)	1	MSB	
U17(15)	Ø	—	Most significant digit
U17(12)	Ø	—	CHECK

8-189. Before the divider chain formed by U12, U9, U13, U14, and U8 can be explained, the two following divide-by-N techniques must be discussed:

a. Two modulus prescaler technique.
b. A counter (divider) chain utilizing 9's complement.

8-190. Two Modulus Prescaler Technique

8-191. The two modulus prescaler technique is illustrated below.



8-192. At first, the scaler control line is set to a low level so that the two modulus prescaler can operate as a ÷ (P+1) prescaler. Therefore, it generates a pulse every P+1 input pulses. After (P+1) × D input pulses occur, the second counter (÷D) reaches zero since it was preprogrammed to D at first. When the content of the second counter (÷D) gets to zero, it generates a pulse which changes the level of the scaler control line high and disables the ÷D counter (itself) at the same time. So, actually, the output of ÷D is not a pulse but a level change. Therefore, after this change occurs, the ÷D counter stops counting and keeps the new state which lets the two modulus prescaler operate as a ÷P prescaler.

8-193. When the level change occurs, the content of the ÷Np counter (which was preprogrammed to Np) is Np-D since D pulses have passed by so far. So, the ÷Np counter will reach zero after receiving (Np-D)•P input pulses (f_{in}). As soon as the ÷Np counter gets to zero, it generates a pulse at f_{out} terminal.

8-194. Therefore, the total input pulses (f_{in}) necessary to get one output pulse is:

$$(P+1)\bullet D+p\bullet(Np-D) \quad (1)$$

8-195. For example, if we choose 10 as P and 100A + 10B + C as Np, equation (1) becomes as follows:

$$11D+10(100A+10B+C)-D$$
$$=1000A+100B+10C+D \quad (2)$$

NOTE

The output is also used as a loading pulse to initiate the next dividing cycle.

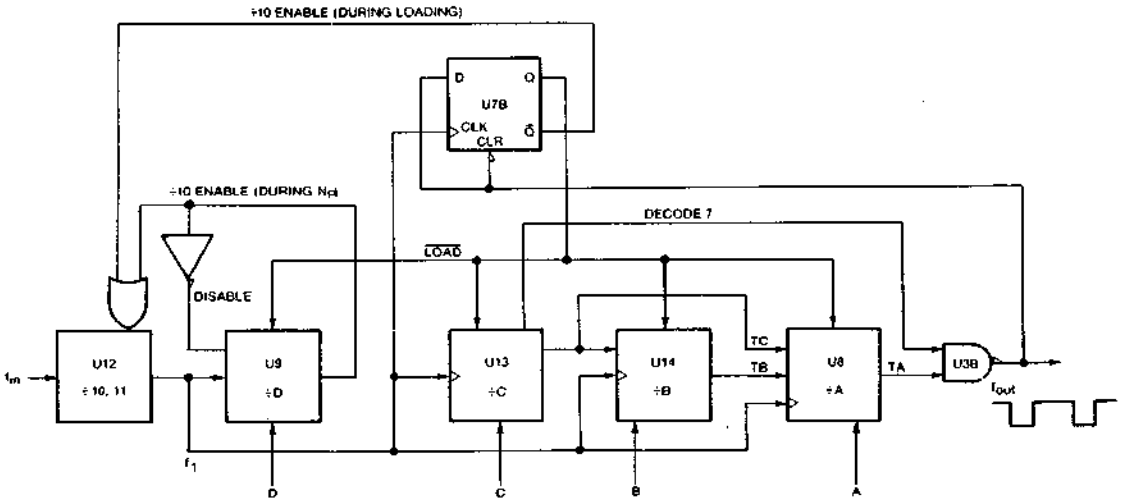
8-196. Now, we have a complete programmable divider chain which can be programmed to any dividing ratio expressed by equation (2). The only limitation on this technique is as follows:

$$Np \geq D \quad (3)$$

8-197. This limitation doesn't matter for our application because $NP \geq 299 \geq 9 \geq D$.

8-198. Counter (Divider) Chain Utilizing 9's Complement

8-199. A counter chain utilizing 9's complement numbers is illustrated below. In the explanation above, we used down counters to achieve ÷D and ÷Np. In the actual circuit, however, up counters (74LS160) are used for that purpose. The up counter generates a positive pulse when used for that purpose. The up counter generates a positive pulse when it reaches a state 9. Therefore, a divide-by-D can be realized if it is preprogrammed to 9-D at first. Then, it generates a pulse after getting D input pulses. One comment to note is that after generating an output pulse (after getting D pulses), it will operate as a divide-by-10 divider unless it is present (loaded to D again).



Remarks:
1. TA, TB, and TC are outputs of ÷A, ÷B, and ÷C.
2. TC for ÷A is look forward connection.
3. ÷B and ÷C operate as divide-by-10 after their first dividing cycle.
4. A, B, C, and D are numbers to be loaded.
5. U9 is preset to 9 in check. Output is high so it is always disabled and always ÷10.

8-200. A two-pulse period of f_1 is used to load the divider chain since one pulse period is not long enough to load the divider chain. The load pulse is provided by U7B. As soon as the f_{out} pulse (negative pulse) appears, LOAD goes low because of CLR input and stays low when the next f_1 pulse comes in because of the low input to D input. LOAD goes high when the second f_1 comes in because of a high input to D input. As long as LOAD is low, the counter chain is inhibited and the state of each divider agrees with the number to be loaded. Since we use a two-pulse period for loading, we have to decode 997 (999-2) for the ÷Np chain to get a correct dividing ratio as a whole. The BCD output of U13 is decoded to detect 7 for this purpose. The output of U8 which corresponds to 99X (X = don't care) is AND'ed with the decoded 7 to get the f_{out} pulse. Since a NAND gate is used, the output pulse is a negative pulse.

8-201. When CHECK mode is selected, the MPU writes to the A10 Divide-by-N assembly to enable D flip-flop U5 and to select a 300 MHz main oscillator frequency. With LSYNHI going low, bit D7 low at U17(13) is clocked in to cause U17(12) to go low, thus enabling U5(÷2). When CHECK is not selected, U17(12) is high so that U5 is disabled and the CHECK output at XA10(11) is inhibited.

8-202. A11 IF LIMITER ASSEMBLY

8-203. The A11 IF Limiter assembly, shown in *Figure 8-34*, provides an additional 14 dB gain to the IF signal over a bandwidth of 0.1 to 175 MHz. For high amplitude signals, the output of A11 is amplitude limited. The 14 dB amplification is provided by differential pair U2. Potentiometer R1, "AMP", is used to maximize the gain through U2 by balancing the currents through the differential pair. The 75 MHz CHECK signal from A10 enters the IF circuitry at XA11(7, $\overline{7}$). CHECK should not be selected when a signal at the APC-3.5 input connector is present.

8-204. The A11 assembly also generates a LPWR RST signal which is not used in the 5343A.

8-205. As shown in *Figure 8-34*, detecting diode CR1 and capacitor C2 detect the negative half-cycle of the IF signal. This dc level is sent to voltage comparator U1 which compares the detected level with a reference level set by the "DET" potentiometer, R14. For input signals greater than approximately -15 dBm, the detected IF appearing at U1(3) will be more negative than the reference voltage at U1(2) and the output at U1(7) will be TTL high. When the input level to the counter drops below about -15 dBm, U1(7) will go TTL low which means that LPWR RST is low. The LPWR RST signal is provided for possible use in future applications.

8-206. A12 IF DETECTOR ASSEMBLY

8-207. The A12 IF Detector assembly shown in *Figure 8-35*, further amplitude limits the IF signal by amplifying it an additional 28 dB before sending it to the A13 Counter assembly to be counted. A level-detecting diode detects if the input signal level is of sufficient amplitude to be counted. A digital filter provides two outputs which indicate: 1) the IF is in the range of 32 MHz to 126 MHz, and 2) the IF is in the range of 22 MHz to 128 MHz. The program reads these filter outputs and stops the sweep when the IF is in the range of 32 MHz to 126 MHz. The 22 MHz to 128 MHz output is latched and is reset if the input power to counter drops below a preset level or if the IF leaves the range of 22 MHz to 128 MHz. This output is examined at the conclusion of the N determination routine to insure that the count during the prs was not invalidated by a power drop-out or excessive FM deviation.

8-208. The IF signal enters differential pair U2 and is amplified by approximately 14 dB. The output at U2(5) passes through a 125 MHz low pass filter formed by C5, L1, C10, L2, C7, and is detected by CR1 and C1. The voltage across C1 is presented to the inverting input of voltage comparator U1, which, due to the positive feedback provided by resistor R9, exhibits approximately 5 mV hysteresis. The OFFSET potentiometer R7 is adjusted so that the output of U1(7) goes low when the input signal to the counter drops below -32 dBm (for a 1 GHz input).

8-209. The other IF output of U2, (pin 8), is ac coupled through C11 to differential pair U4 where it is amplified by another 14 dB. Potentiometer R12, (B2) is used to equalize (balance) the currents through the two emitters of the transistor pair. This is done by adjusting R5 for maximum gain through the stage. Potentiometer R2, (B1) is adjusted in a similar manner. U4 has two outputs: U4(5) and U4(8). The output at U4(5), IF COUNT, appears at XA12($\overline{8}$) and is sent to the A13 counter to be counted. The output at U4(8) is ac coupled by capacitor C16 to a digital filter.

8-210. The digital filter consists of U6, U5, U10, U8, U9, U11, U14, and U15. The filter counts the IF signal for a period of 4 microseconds and, based on the number of counts totalized during the 4 microseconds, sets two qualifiers which indicate if the IF is within the necessary frequency range. The counters are reset every 8 microseconds and the counting of the IF begins again. This process of counting the IF for 4 microseconds, setting the qualifiers, and resetting the counters after 8 microseconds occurs continuously.

8-211. The IF signal output is prescaled by 4 in U3A (÷2) and U3B (÷2). The ECL output of U3(15) is translated to TTL levels by transistor Q1. This signal is then counted for 4 microseconds. The NOR gate U6A is enabled for a period of 4 microseconds by U6(2) going low for 4 microseconds. This 4-microsecond gate is generated by divider U15 which divides a 1 MHz input by 8. The input is from the A18 Time Base Buffer. During the 4-microseconds gate time; the count is totalized by binary counters U5 and U10. The contents of the counters are decoded by U8, U9 such that if the IF frequency is in the range of 32 MHz to 126 MHz (the U5 and U10 counters count 32 to 126 counts during the 4-microsecond gate), U6(13) [TP5] will be high. If the IF is in the range of 22 MHz to 128 MHz, U6(10) [TP6] will be high. Dual flip-flop U13 is loaded with this qualifier information every 8 microseconds by a clock signal from U11(12) [TP4]. After a 1-microsecond delay, the U5, U10 counters are reset by a low level from U14(6). *Figure 8-13* shows the timing for the filter.

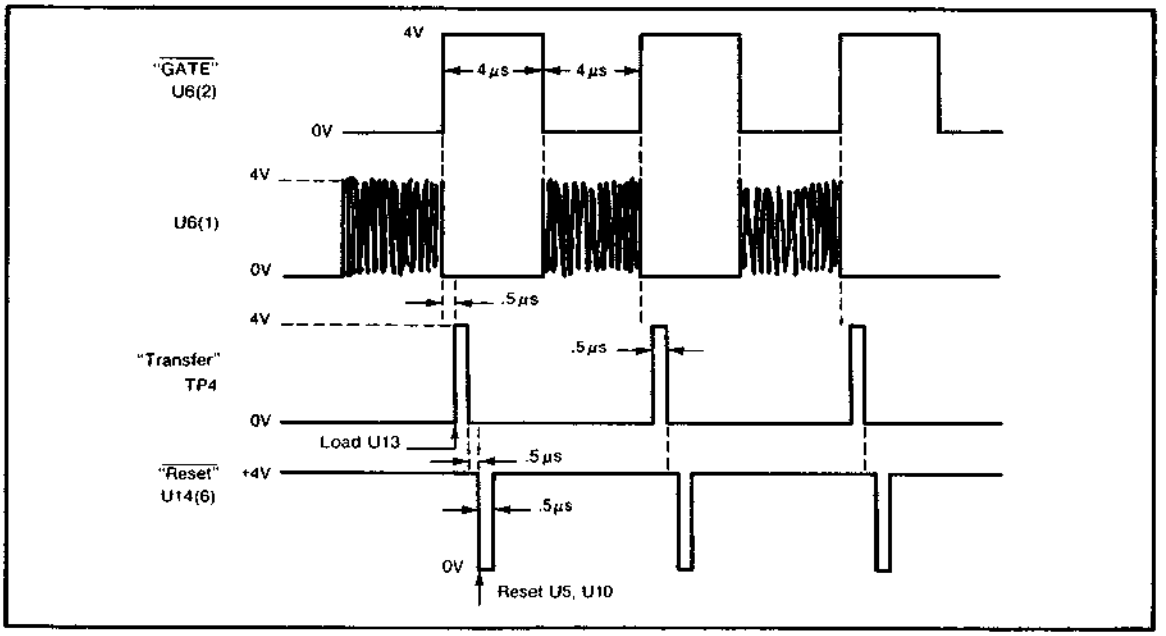


Figure 8-13. Filter Timing on A12 IF Detector

8-212. When the instrument is sweeping, the A14 Microprocessor issues LPDREAD which enables the three-state buffer/driver U12, and data from A12 is placed onto the data bus. The 32—126 MHz detector output (D6) is examined and when D6 is low (TP8 high), the microprocessor stops sweeping the main oscillator. After the sweep has stopped, the microprocessor issues LPDWRT which sets the U7(11) output of the latch formed by U7C and U7D to the low state. U7(11) [TP10] goes low when LPDWRT goes low since U13(5) is high (since U6(13) is high, then U6(10) must also be high).

8-213. The program then begins the N determination. At the conclusion of the N determination, the microprocessor sends LPDREAD and examines the latched 22—128 MHz detector D7. If the input power has dropped below -32 dBm or if the IF has exceed the range of 22 MHz to 128 MHz, then U13(5) will have been low at some time and the U7(11) output of latch U7C, U7D will have been reset to a high. If the D7 bit read by the microprocessor is low, then the N determination is considered invalid and the sweep routine is re-entered at a point 100 kHz lower in frequency than when it previously stopped searching.

8-214. The D4 bit output of U12(7) to the MPU to indicate an overload input signal is not used in the 5343A.

8-215. A13 COUNTER ASSEMBLY

8-216. The IF Count signal enters the A13 Counter Assembly shown in *Figure 8-36* at XA13(17) and is capacitively coupled via C10 into the main gate of the counter, U11C. U11 is a high-speed ECL AND gate. When U11(9) and U11(10) are both low (–0.8V = high; -1.5V = low), the gate is enabled and the IF Count signal is passed through the gate to be counted. Flip-flop U4B selects either the IF Count signal at XA13(17) or the Direct B signal from the direct count amplifier at XA13(14) to be counted. If in direct count mode, the microprocessor sets the D1 bit to logic Ø and writes to the counter so that LCTRWRT (low counter write) will clock a logic Ø into U4(9). When operating in the 500 MHz—26.5 GHz range, D1 will be logic 1 and the U4(9) output will be a logic 1. This enables U11B and disables U11C.

8-217. There are two operating modes, one during and one after acquisition. During acquisition the A5 multiplexer is switched between the two LO's. In synchronism with the A5 multiplexer switching, the IF signal on the A13 Counter assembly is switched between counter A (U17, U13, and U1) and counter B (U18, U14, and U2). Thus, counter A accumulates counts only during the time that the main VCO is producing the IF and counter B accumulates counts only during the time that the offset VCO is producing the IF. After acquisition, the pseudorandom switching between VCO's stops and the multiplexer selects the main VCO. The IF is then measured by counter A with a gate time determined by the desired resolution.

8-218. The LO Switch signal comes in at XA13($\overline{8}$) and, after passing through TTL to ECL converters, drives U12A and U12B to switch the IF between counter A and counter B. When LO Switch is high, counter A is selected and when LO Switch is low, counter B is selected.

8-219. The 8-decade channel A counter consists of decade counter U17 (the least significant decade), decade counter U13, and 6-decade counter U1. The 8-decade channel B counter consists of decade counter U18 (least significant decade), decade counter U14, and 6-decade counter U2.

8-220. To output the contents of the 8 decades to the microprocessor, each counter has outputs which pass through multiplexers. The counter A multiplexer consists of 4-line-to-1-line data selectors U5A, U5B, U9A, U9B. The counter B multiplexer consists of U6A, U6B, U10A, and U10B. If the LCTRRD (low counter read) signal goes low and if A5 = logic 1, then the A counter multiplexer is enabled (otherwise the three-state outputs are in the high Z state) and the contents of the A counters are output on the data lines to the microprocessor. With LCTRRD low and the A5 = logic Ø, then B counter multiplexer is enabled and its contents are output on the data lines.

8-221. After passing through main gate U11, the signal is switched to either the A counter or the B counter by gates associated with ÷2 flip-flop U12A and U12B. If the A counter is selected, the IF signal is divided by 2 by U12B and divided by 2 again by U16B. The output of U16B(14) passes through ECL to TTL level converter U15. The outputs of these first two binaries are connected to the "Ø" data inputs of the multiplexer and are read first by the microprocessor.

8-222. For example, the output of the first binary in the A counter chain [U12B(14)] is connected, via an ECL to TTL converter, to U9A(6). Consequently, the state of the A counter's two least significant binaries is read by the microprocessor by sending LCTRRD low, A5 = logic 1, and A3 = A4 = logic 1 (the inverter U7 causes the "Ø" data inputs of the multiplexer to be connected to the multiplexer outputs). The outputs of the first decade counter following the binaries are read in a similar fashion. These outputs are connected to the "1" data input of the multiplexers. For example, to read the first decade of the A counter, LCTRRD goes low with A5 = logic 1, A3 is set to logic Ø and A4 is set to logic 1 (because of the inversion, the "1" data inputs to the multiplexers are selected). To read the last six decades, the "3" data inputs of the multiplexers are selected by setting A3 = A4 = logic Ø. The AØ, A1, and A2 address lines used to address the decades in U2 (if A5 = logic Ø) or U1 (A5 = logic 1). To address the least significant decade in U1, for example, the logic state of the address lines would be:

LCTRRD	A5	A4	A3	A2	A1	AØ
Ø	1	Ø	Ø	1	1	1

8-223. The Direct A input at XA13($\overline{7}$) is the output of the first high-speed binary located on the A3 Direct Count Amplifier. The Direct B input is the output of the second high-speed binary on A3 and it drives the A counter when making direct count measurments. The state of the first and second binaries on A3 are connected to the "Ø" data inputs of U5A and U5B on A13 and are read first for direct count measurement. The state of the ÷4 output from A3, which causes the output of A13U11C(4), passes through an ECL to TTL converter formed by Q2 and Q3 before going to U5B(10). Therefore, in direct count, the signal is divided by 4 on A3 and then divided by 4 in U12A, U16A on A17, before passing to the decade counters U17, U13, and U1.

8-224. After counting, the decades are reset by writing to A13 counter board with DØ = logic Ø. This causes U4(5) to go low to reset U18, U17, and U13. U4(6) goes high to reset U2 and U1 as well as U12 and U16.

8-225. A14 MICROPROCESSOR ASSEMBLY

8-226. The A14 Microprocessor (MPU) assembly shown in *Figure 8-37* contains the microprocessor, address bus and data bus drivers and decoder circuits. This assembly controls the measurement cycle, performs numerical computations for frequency measurements, and interfaces with many of the other assemblies.

8-227. The A14 MPU assembly uses the Motorola 6800 MPU (U10). The application in the HP 5343A is described in the following paragraphs. The memory circuits (ROM and RAM) for the MPU are contained on A16 Memory and Sweeper Control assembly.

8-228. Microprocessor Operation

8-229. The HP 5343A uses U10 for control and computation purposes. An expanded block diagram of U10 is shown in *Figure 8-14*. The 16-bit address bus allows the MPU to address up to 64K memory locations. The data bus is 8 bits wide and is bidirectional. Data on the bus is read into the internal MPU registers when the Read/Write control line is low. All operations are synchronized to a two-phase nonoverlapping 1 MHz clock, $\phi 1$ and $\phi 2$. Each instruction requires at least two-clock cyles for execution. The HP 5343A utilizes the following additional 6800 control lines:

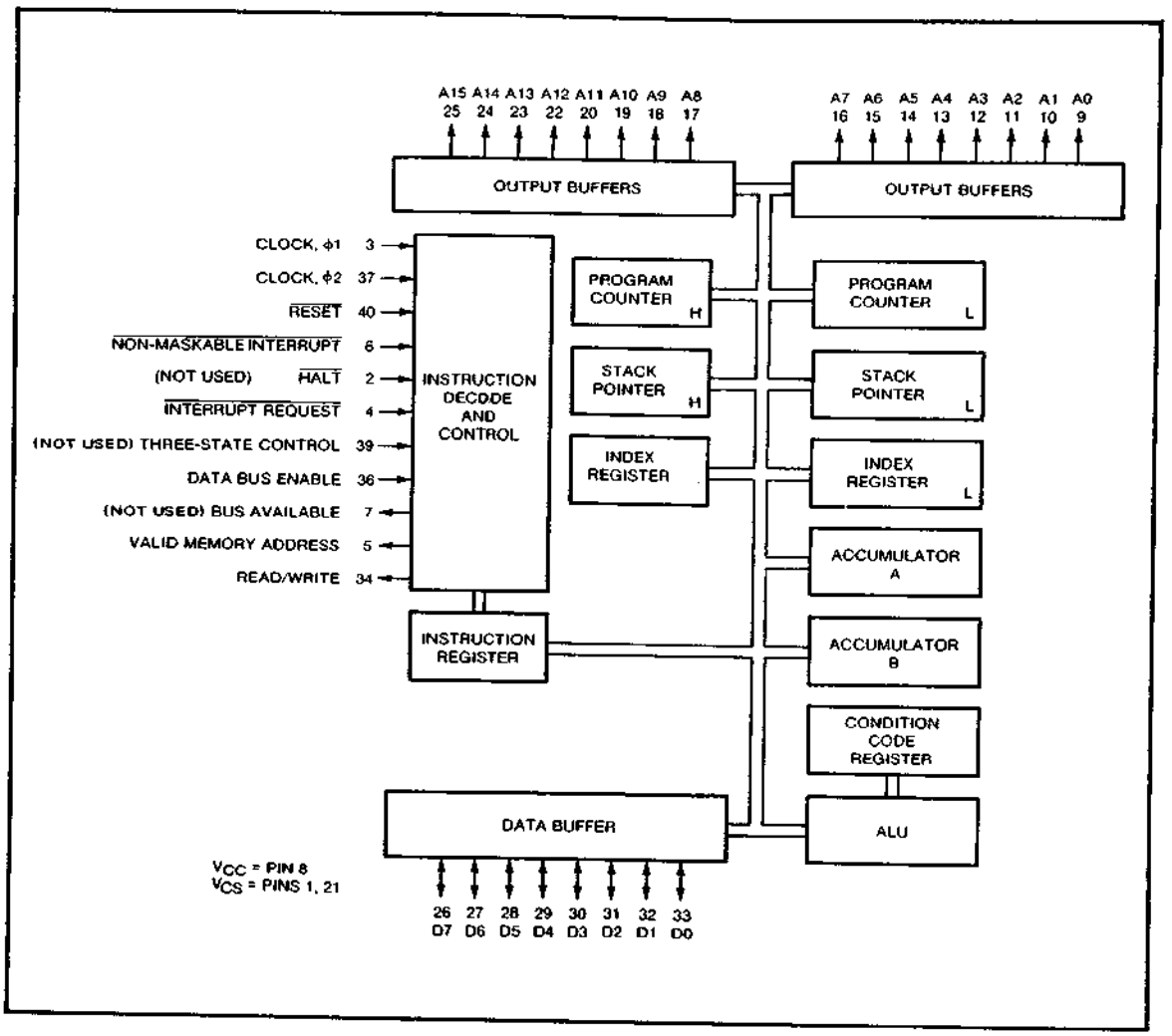


Figure 8-14. A14U10 Expanded Block Diagram

a. $\overline{\text{RESET}}$ — This input is used to reset and start the MPU from a power-down condition, resulting from a power failure or an initial start-up of the processor. If a positive edge is detected on the input, this will signal the MPU to begin the reset sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$.

b. $\overline{\text{NONMASKABLE INTERRUPT}}$ ($\overline{\text{NMI}}$) — A low-going edge on this input request that a nonmask-interrupt sequence be generated within the processor. As with the $\overline{\text{INTERRUPT REQUEST}}$ signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask-bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a nonmaskable interrupt routine in memory. $\overline{\text{NMI}}$ has a high impedance pullup internal resistor, however, a 3 KΩ external resistor to Vcc should be used for wire-OR and optimum control in interrupts. Inputs IRQ and $\overline{\text{NMI}}$ are hardware interrupt lines that are sampled during $\phi 2$ and will start the interrupt routine on $\phi 1$ following the completion of an instruction.

c. Data Bus Enable (DBE) — This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it would be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.

d. $\overline{\text{INTERRUPT REQUEST}}$ ($\overline{\text{IRQ}}$) — This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory. The $\overline{\text{HALT}}$ line must be in the high state for interrupts to be recognized. The $\overline{\text{IRQ}}$ has a high impedance internal pullup; however, a 3 KΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

e. Valid Memory Address (VMA) — This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces. This signal is not three-state. One standard TTL load and 30 pF may be directly driven by this active high signal.

f. Read/Write (R/W) — This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-state Control going high will turn Read/Write to the off (high impedance) state. Also, when the processor is halted, it will be in the off state. The output is capable of driving one standard TTL load and 130 pF.

8-230. The MPU (U10) is driven by a two-phase clock, $\phi 1$ at U10(3) and $\phi 2$ at U10(37). As shown in *Figure 8-37*, the two-phase clock is derived from the 4 MHz input at U12(1 and 2).

8-231. The address outputs of U10 pass through three-state inverting line drivers U6 and U7. Since the Bus Available control line, U10(7), is low, the three-state drivers are always enabled. (In direct memory access (DMA) applications, which are not implemented in the HP 5343A, Bus Available goes high indicating that the MPU has stopped and that the address bus is available.) The address lines drive ROMs U6 and U9 and RAMs U11 and U14 on the A16 Memory and Sweeper Control assembly. The RAM occupies 256 memory locations from 0080 to 00FF. To see how this is implemented, consider what happens when the address 0080 is output by the MPU:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0				0				8				0			

After going through the inverting line drivers U6 and U7, the address lines become:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
F				F				7				F			

The address lines go to the memory circuits on A16 Memory and Sweeper Control assembly.

8-232. The address lines are decoded by device decoding circuitry on A14. In some instances, further decoding occurs at a particular device (for example, on the A13 Counter assembly). The MPU treats an external device just like a memory location. To pass information between the registers of the MPU and the registers of an external device (such as the count registers on the A13 Counter assembly), the program writes or reads data from (or to) the location associated with the device. Address decoding circuitry decodes the address output from the MPU and generates a strobe which enables the register on the device. For example, to read data from the A1 keyboard, LKBRD goes low which enables the three-state bus driver A1U23 to drive the data bus and send keyboard information back to the MPU. The address location assigned to reading the keyboard is ØØ1Ø. When ØØ1Ø is output by the MPU, address decoding causes U17(7) to go low. Since only one device can drive the data bus at a time, all other device code outputs are high (so that the device buffers on these devices are in the high Z state). To see how ØØ1Ø causes U17(7) to go low, consider that the inverted address lines at the output of inverter buffers U6 and U7.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	AØ
1	1	1	1	1	1	1	1	1	1	1	Ø	1	1	1	1

Since AØ, A1, and A2 are all high, these inputs to U17 will cause 7 to be decoded and U17(7) to go low provided that the control inputs U17(4) and U17(5) are both low. U17(5) is low (ground) and U17(4) is low when U16 decodes the address output by the MPU and the address in the range of ØØ1Ø to ØØ17. U16(11) is low when U16(14) is high and U16(13) is low, provided that the control input U16(15) is low. Since inverted A3 is high and inverted A4 is low, the U16(11) output will be low provided that U16(15) is low. U16(15) is low since U20A is enabled by A5, VMA·ϕ2 and U14(7) output. Inverted A15, A14, A13, A12, A11, A10 all high is decoded by U13A and U13B. A9 is also high. Thus U14 is enabled. Since inverted A8, A7, A6 are all high, the decoded 7 output U14(7) goes low. In summary, U14(7) goes low only when inverted A15, A14, A13, A12, A11, A10, A9, A8, A7, A6 are all high. Inverted A5 high, A4 low, A3 high is decoded by U21. Inverted A2, A1, and AØ all high is decoded by U17.

8-233. The eight bidirectional data bus lines coming out of U10 pass through octal transceiver U5 which allows each line in the data bus to be isolated for troubleshooting purposes. Two U10 data lines are connected to ground via CR1 and CR2 (these lines connected to ground only when LFRERUN (TP4) is grounded), to cause a CLB (clear accumulator B) instruction to be presented to the MPU. This causes the MPU to continuously increment the addresses on the address bus from the least significant address (ØØØØ) to the most significant address (FFFF) for diagnostic purposes when using the 5004A Signature Analyzer. With U5 isolated, feedback is broken between the ROM outputs and the MPU inputs which is a necessary condition for taking signatures with the HP 5004A Signature Analyzer. If LXROM (Low External ROM) is grounded, the ROM's will be disabled and the address lines can now be used to drive external memory residing in the upper 32K of the memory map.

8-234. The power-up reset circuitry formed by Clock Driver U12 provides a low reset pulse to the MPU reset input U10(40) and a LDVRST output to the A2 Display Driver to blank the display during power-up.

8-235. The eight data lines pass through bidirectional inverting octal transceiver U5. When data is being written out to the external devices (or to RAM), U5(34) goes low which causes U15(7) and U5(1) to go high thereby enabling the drivers which write to external devices. When data is being read from external devices (or RAM), U5(34) goes high and U5(1, 19) go low. This enables the drivers in U5 which read data from external devices.

8-236. A15 OPTION 011 HP-IB ASSEMBLY

8-237. The A15 Option 011 HP-IB assembly is described under OPTIONS in paragraph 8-312.

8-238. A16 MEMORY AND SWEEPER CONTROL ASSEMBLY

8-239. The A16 Memory and Sweeper Control assembly as shown in *Figure 8-39*, contains two separate groups of circuits. One group is the memory circuit for A14 MPU and the other group is the trigger circuit for control of an external, compatible sweeper.

8-240. Memory Circuits

8-241. The memory consists of ROMs U6 and U9, each containing 4K bytes. RAMs U11 and U14 provide 256 4-bit bytes each, for a total of 256 8-bit bytes, of which 128 are used.

8-242. The memory circuits are connected to the bidirectional data bus via transceiver U2, which controls the direction of data flow. Pin 19 of U2 must be low (enable) and pin 1 is high or low (HR/LW for High Read/Low Write) to determine direction of data flow. Pin 19 is low when the proper conditions are met at AND gate U15B. This gate requires a timing signal input (VMA·ϕ2) and an input from ROM/RAM decoder OR gate U13.

8-243. The ROM/RAM decoder OR gate U13 is enabled by the RAM enabled output, U15(8), which is decoded from the address lines LA8—LA15 via U12, U15A, C and U3D. OR gate U13 is also enabled by the ROM enable output, which is decoded from address lines LA12—LA14 via U7 and U10. Either the RAM or ROM enable output results in a low signal to enable transceiver U2 on the data bus. The decoded output of U8 is not used in the 5343A and U8 is disabled at U8(4).

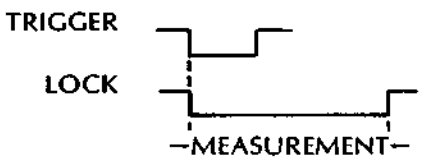
8-244. Trigger Circuits

8-245. The trigger circuits, provided for use with an external, compatible sweep oscillator, consist of multiplexer U17, flip-flop U16 and driver U18.

8-246. Multiplexer U17 decodes address lines LA0, LA1, and LA2 to output the signals labeled 0028 (pin 7) and 0029 (pin 9). The $\overline{\text{VMA}\cdot\phi 2}$ signal and LPWR signal from the MPU are used to enabled U17.

8-247. Driver U18 is connected by wires to rear panel connectors to provide a control interface to an external compatible sweep oscillator. Pin 14 of U18 receives a trigger from the sweep oscillator, labeled SWPA(T) on the A16 board. Pin 3 outputs a sweeper lock signal labeled SWPB(L) on the board. (These signals may be monitored at test points at the top of the board.) The sweeper output is connected to the 5343A front panel input connector.

8-248. When the SWP M button on the 5343A front panel is pressed, the LPWR and $\overline{\text{VMA}\cdot\phi 2}$ signals enable U17 to output 0028 to enable the driver U18. This results in signals to the data bus that cause the MPU to look for a trigger from the sweeper. The SWP M key LED flashes to indicate the mode is operating. When a trigger occurs, the 5343A takes a measurement during which time the lock signal is sent to the sweeper to lock the sweep signal, as shown below.



Trigger signal from sweeper goes TTL low, then Lock signal to sweeper goes TTL low during the measurement.

8-249. The Lock signal to the sweeper is generated by the 0029 output of U17 which clocks the U16 FF. The output of U16 to pin 2 of U18 provides the low SWPB (L) Lock signal. When the measurement is completed, FF U16 is reset and the Lock signal is released (high).

8-250. A17 TIMING GENERATOR ASSEMBLY

8-251. The A17 Timing Generator shown in *Figure 8-40*, has the following functions: during acquisition, it generates the pseudorandom sequence used to switch the A5 Multiplexer and the A13 counters for N determination; after acquisition, it generates gate times for the measurement of the IF on A13; between measurements, its sample rate circuitry determines when to begin a new measurement.

8-252. The DØ through D5 data lines from the microprocessor data bus transmit data from the microprocessor to the hex D-type register U20 when the LTIM WRT signal (decoded on A14) goes low. LTIM WRT returning high clocks the data into the register. The data lines also transmit data back to the microprocessor from hex three-state driver U19 which drives the data bus when LTIMRD (decoded on A14) goes low.

8-253. Pseudorandom Sequence Generation

8-254. During acquisition, after a countable signal has been detected and the sweep stopped, the N number must be computed. By measuring the IF_1 frequency which occurs when the Nth harmonic of the main VCO mixes with the unknown frequency and then measuring the IF_2 that occurs when the Nth harmonic of the offset VCO mixes with the unknown, the harmonic number N can be determined. N equals $(IF_1—IF_2)/500$ kHz where 500 kHz is the precise frequency difference between the main VCO and the offset VCO. To speed the process of determining N, two counters (on A13) are used, counter A and counter B. To prevent coherence between FM on the unknown signal and the switching rate between counters from causing an incorrect computation of N, the switching between counter A and B (which is synchronous with the switching in A5 between the main VCO and the offset VCO) is done in a pseudorandom fashion. Three different sequence lengths are possible (selected by a rear panel switch). 1) the normal or pseudorandom sequence (prs) which lasts for a total time of 360.4 milliseconds (counter A and counter B are open for 163.83 ms each — there's ≈32.8 ms of "dead" time). This normal prs gives a worst case FM tolerance of 20 MHz peak-to-peak; or 2) the slow prs, which lasts for a total time of 2.096 seconds (counter A and counter B are open for 524 ms each in addition to 1.048 seconds of "dead" time). This slow prs gives FM tolerance of 50 MHz peak-to-peak; or 3) the fast prs, which lasts for 22.52 ms (Counter A and Counter B are open for 10.24 ms each in addition to 2.04 ms of dead time). The fast prs gives FM tolerance of 6 MHz peak-to-peak. (The acquisition times listed in *Table 1-1* are longer than those listed here due to inclusion of sweep time in *Table 1-1*.)

8-255. The medium and the slow prs modes of operation are indicated by # (medium) and * (slow) indicators on the front panel. When the indicators are not lit, the fast prs mode is in operation.

8-256. To begin the pseudorandom sequence, the microprocessor writes to A17 and sets U20(15) high (prs enable), U20(12) low (gate time disable), U20(7) high (for 1 MHz prs clock), and U20(5) high for the slow prs or sets U20(2) high for the medium prs. Both U20(5) and U20(2) are set low for the fast prs. For the medium prs, a 100 kHz prs clock is used and U20(7) is low. Decade divider U11 divides down the 1 MHz input to 100 kHz which appears at U16(8). For the slow prs, a 1 MHz prs clock is used and U20 (7) is high. Since U11(1, 3) are both high, the counter is preset to 9 so that U11(9, 8) are both high which enables U16. Thus the 1 MHz input appears at U16(8) and becomes the prs clock.

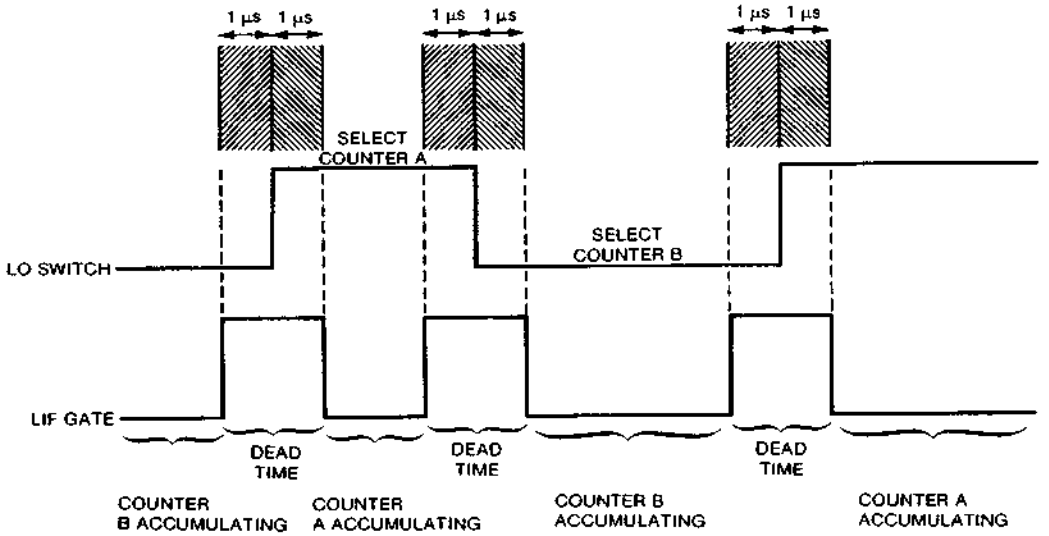
8-257. The prs generator consists of shift registers U13, U10, U5, 4-bit counters U2, U1, and logic gates U6, U3. When U20(15) (prs enable) goes high, the output of U18(6) goes high which releases the reset signal from all the components of the prs generator and starts the sequence. To generate the sequence, data is shifted through the shift register formed by U5, U10, and U13. Feedback taps exclusively "OR" two of the shift register outputs to generate the

next input. This feedback generates the prs. For the fast pres, U3B(4) is high and U6A is used to perform the exclusive "OR" function (the output of U13(6) is not used for the fast prs). For the slow prs, U3A(1) is high and U6B performs the exclusive "OR". The data is then fed back to the input of the shift register at U5(1, 2) via inverter U3D.

8-258. The medium prs is 15 bits long and stops after 14 consecutive highs in the sequence are detected. The slow prs is 20 bits long and stops after 19 consecutive highs in the sequence are detected. The fast prs is 11 bits long and stops after 10 consecutive highs in the sequence are detected. The detection of the number of consecutive highs in the sequence is performed by presettable counters U2 and U1. For the medium prs, "1" is preset into U2 (lest significant counter) and "15" is preset into U1 (most significant counter) by a low level on U2(9) and U1(9). When a high appears in the sequence, the U2 counter is incremented by the prs clock at U2(2). When a low appears in the sequence, U2 and U1 are reset to the initial preset conditions and counting up begins again. After 14 consecutive high in the prs, U2 has counted to "15" and the carry output U2(15) has enabled U1 so that the 14th clock causes the carrry output U2(15) to go high. This causes U8A(3) to go low which resets the latch formed by U18C and U18D so that U18B(6) goes low to reset U13, U10, U5, U2, and U1.

8-259. For the slow prs, operation is similar: this time "12" is preset in U2 and "14" is preset into U1 so that after 19 consecutive highs in the prs, the carry out of U2 sets U18D(11) low so that U18B(6) is low and clears the prs generator. For the fast prs, "5" is preset in U2 and "15" is preset in U1 so that after 10 consecutive highs, the prs generator is cleared.

8-260. To allow sufficient settling time for the multiplexer on A5 after switching, 2 microseconds of dead time are added to each transition in the sequence which means that the transistions of the LIF GATE signal (which enables counter A or counter B on A13) are delayed with respect to the LO Switch signal which switches the A5 multiplexer and switches between counter A and counter B on A13 as shown below:



8-261. The dead time in the LIF GATE signal is generated by D flip-flops U9A, U9B, exclusive "OR" U6D, and D flip-flop U17A. The dead time is generated when U6D(11) goes high for two periods of the 1 MHz clock. With U6D(11), high, U16B is disabled and the prs clock at U16C(8) remains high. The reset input to U17A(1) is low during the prs generation so that U17A(5) is low. When the preset input U17A(4) goes low also, the output goes high for the time that the preset signal is high (both Q and $\overline{Q}$ output go high when preset and clear inputs are both low). When U6D(11) goes high to disable the prs clock for 1 µs, U17A(5) goes low for 2 µs. The low is presented to U21A(7) and on the next clock at U21A(6), the low at U21A(7) is clocked into the output so that LIF GATE goes low to enable counting on A13.

8-262. The timing diagram in *Figure 8-15* for the slow prs generation (prs clock = 1 MHz) will help clarify the operation:

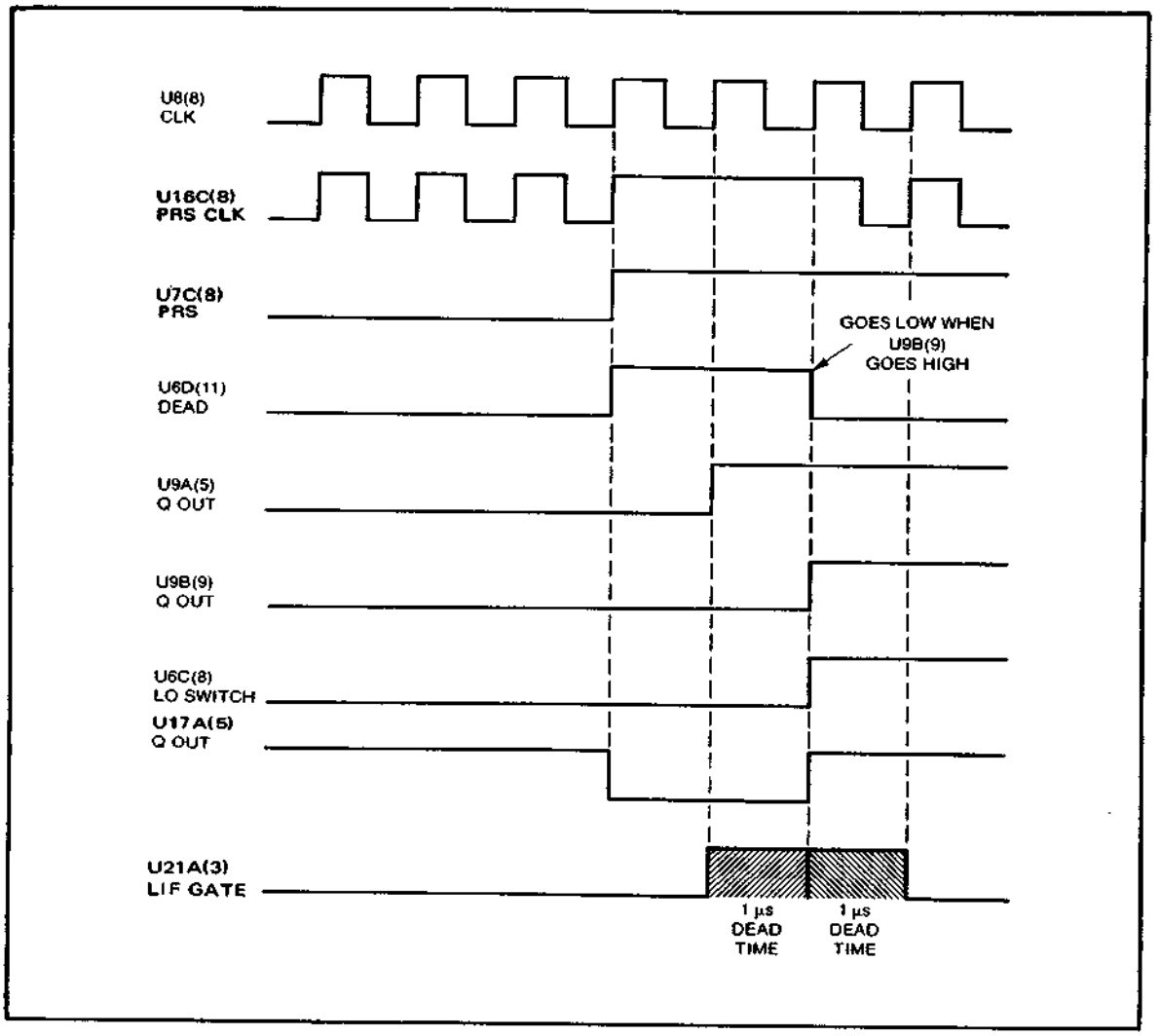


Figure 8-15. PRS Timing Diagram

8-263. When the prs is over, U18B(6) goes low. When the A17 board is read by the microprocessor, LTIM RD goes low and three-state drivers U19 are enabled. If the prs is over, U20(5) is low and the program detects this, causing the next program segment to be executed.

8-264. Gate Time Generation

8-265. Gate times for measuring the IF signal after acquisition and N determination are generated by time base generator U15, D flip-flops U17 and U21. To generate gate times from 10 µs to 1-second, the microprocessor writes to A17 to set U20(21) (gate time enable) high, U20(10) (sets LOW SWITCH to high which selects counter A and the main loop VCO) high, U20(15) low (prs disabled), and a 3-bit resolution code on U20(7, 5, 2) which selects the division factor of the decade dividers in U15.

8-266. For gate time generation, divider U11 divides the 1 MHz clock input to 100 kHz. Since U18(3) is high, the 100 kHz from U11(9) passes through gate U12D to U15(3). The 100 kHz signal at U15(3) will be divided by a factor of 10^0 to 10^5, depending upon the resolution code at U15(14, 13, 12) and will appear at the output of U15(1):

U15(14)	U15(13)	U15(12)	U15(1)
1	Ø	1	1 Hz
Ø	Ø	1	10 Hz
Ø	1	1	100 Hz
Ø	1	Ø	1 kHz
1	Ø	Ø	10 kHz
Ø	Ø	Ø	100 kHz

8-267. Since U17B(8) is high, the low to high transition at U17(3) clocks a high into U17A(5). U17A(6) low then presets U17B(8) low so that after one period of the divided U15 output, a low is clocked into U17A(5). After passing through a TTL to ECL level shifter, the gate signal is clocked into the high-speed ECL D flip-flop U21A and U21B. U21A and U21B act as the main gate flip-flop for the counter. U21A is used for measurements in the 0.5—18 GHz range and U21B for direct measurements below 500 MHz.

8-268. U17A(6) goes low when the gate time has expired and this is sent to three-state driver U19D(6). When LTIM RD goes low, U19B(3) low indicates to the microprocessor that the gate time is over and that the program may advance to the next operation.

8-269. Sample Rate Generation

8-270. The sample rate rundown is initiated by writing a low into U20(2) followed by writing a high into U20(2). During the time that U20(2) is low, C17 is charged toward +5 volts through the saturated transistor Q2. The voltage at the base of Q1 is sufficient to turn on Q1, which generates a TTL high at U19B(4). With U20(2) high, the charge on C17 is discharged through R9 and the 1 MΩ SAMPLE RATE pot R2 (on A2) until the voltage at the base of Q1 turns off the transistor, thus producing a TTL low at U19C(4). The microprocessor reads this data and upon detecting the low, advances to the beginning of the measurement algorithm. For infinite sample rate the SAMPLE RATE pot is adjusted to 1 MΩ position so that the leakage through R9 and the SAMPLE RATE pot is less than the charging current flowing through R24.

8-271. U19E, U19F, and U22 are not currently used but are reserved for future use.

8-272. A18 TIME BASE BUFFER ASSEMBLY

8-273. The A18 Time Base Buffer assembly shown in *Figure 8-41*, provides logic to select a 10 MHz signal from either the internal 10 MHz standard (A24) or from a 10 MHz external standard applied to the 5343A rear panel. A rear panel switch generates an LEXT signal which, when TTL low, disables gate U5C (and hence the internal 10 MHz) and enables gate U5A which allows the external standard to pass through gate U5B.

8-274. The 10 MHz output of U5B is divided by 10 in U3 to provide a 1 MHz ouptut to A12 IF Detector and to the prs generator on A17 Timing Generator. Dividers U2 and U1 divide-by-20 to provide a 500 kHz output to the phase detector on A7 Mixer/Search Control assembly and to the divide-by-10 circuit on A10 Divide-by-N assembly.

8-275. A19, A20, A21 POWER SUPPLY

8-276. The power supply used in the 5343A is a high efficiency switching regulator which is made up of the A19 Primary Power Assembly, the A20 Secondary Power Assembly, and the A21 Switch Drive Assembly. The ac line voltage is directly rectified on A19. Consequently, A19 is isolated from the rest of the instrument and care must be exercised when voltage measurements are made on A19. A19 measurements should be made by supplying power to the 5343A via an isolation transformer.

8-277. SIMPLIFIED BLOCK DIAGRAM. *Figure 8-16* is a simplified block diagram of the 5343A power supply. As shown in the diagram, the supply consists of six major elements: an input rectifier-filter, a pair of push-pull switching transistors (A19Q1, Q2), an RF transformer (A20T1), output rectifiers and associated linear voltage regulators, a pulse width control feedback network, and current limiting circuitry.

8-278. VOLTAGE REGULATION LOOP. Regulation is accomplished primarily by switching transistors Q1 and Q2 under control of a feedback network consisting of the A21U4 20 kHz oscillator/pulse width modulator, and the switch drive transformers on A19. The schematic diagram is shown in *Figure 8-42*. If the 5V (D) output (digital supply) voltage attempts to decrease, the +5V sense signal drops which causes an error signal (difference between +5V sense and +5V reference set by A21R17) to drive a pulse width modulator (part of U4) and increase the pulse width of the 20 kHz outputs of A21U4. Conversely, for an increase in the voltage of +5V (D), the pulse width of the A21U4 outputs decrease. The net result of controlling the pulse width of the 20 kHz output is to control the duty cycle of the output waveforms of Q1, Q2, and hence the duty cycle of the rectangular waveform delivered to the LC filter in the +5V (D) output. The LC filter averages this rectangular waveform to produce a dc output level which is proportional to the duty cycle of the input waveform.

8-279. The feedback provided by the +5V (D) sense signal establishes a controlled input to the primary of A20T1. Other taps on the secondary of A20T1 are rectified, filtered, and delivered to individual linear voltage regulators to provide +5V (A) output (analog supply), -5.2V, +15V, -15V, and +12V.

8-280. The oven transformer output is rectified and filtered to provide power to the control circuits U3, U4 on A21 and oven power when the Option 001 oven oscillator is installed. These oven transformer voltages are available whenever the 5343A is plugged into the line voltage, regardless of the position of front panel power switch.

8-281. CURRENT LIMITING. Total current load is sensed by resistor A19R5 and a signal is sent, via optical isolator CR2, to the A21U3 Timer which acts as an overcurrent shutdown circuit. When excessive current is drawn, the output of U3 turns off the 20 kHz oscillator on U4 for approximately 2 seconds.

8-282. For output voltages other than the +5V (D) output, excessive current may or may not cause A21U4 to turn off since the current limiting circuitry built into the individual linear regulator may shutdown the output before the U3 Timer has time to shutdown the 20 kHz oscillator in U4.

8-283. When the hold-off output of U3 is TTL high, the 20 kHz oscillator on U4 is disabled. This high level causes a red LED to light which indicates overcurrent shutdown. When this occurs, the green LED on A20 turns off, indicating the absence of +5V (D).

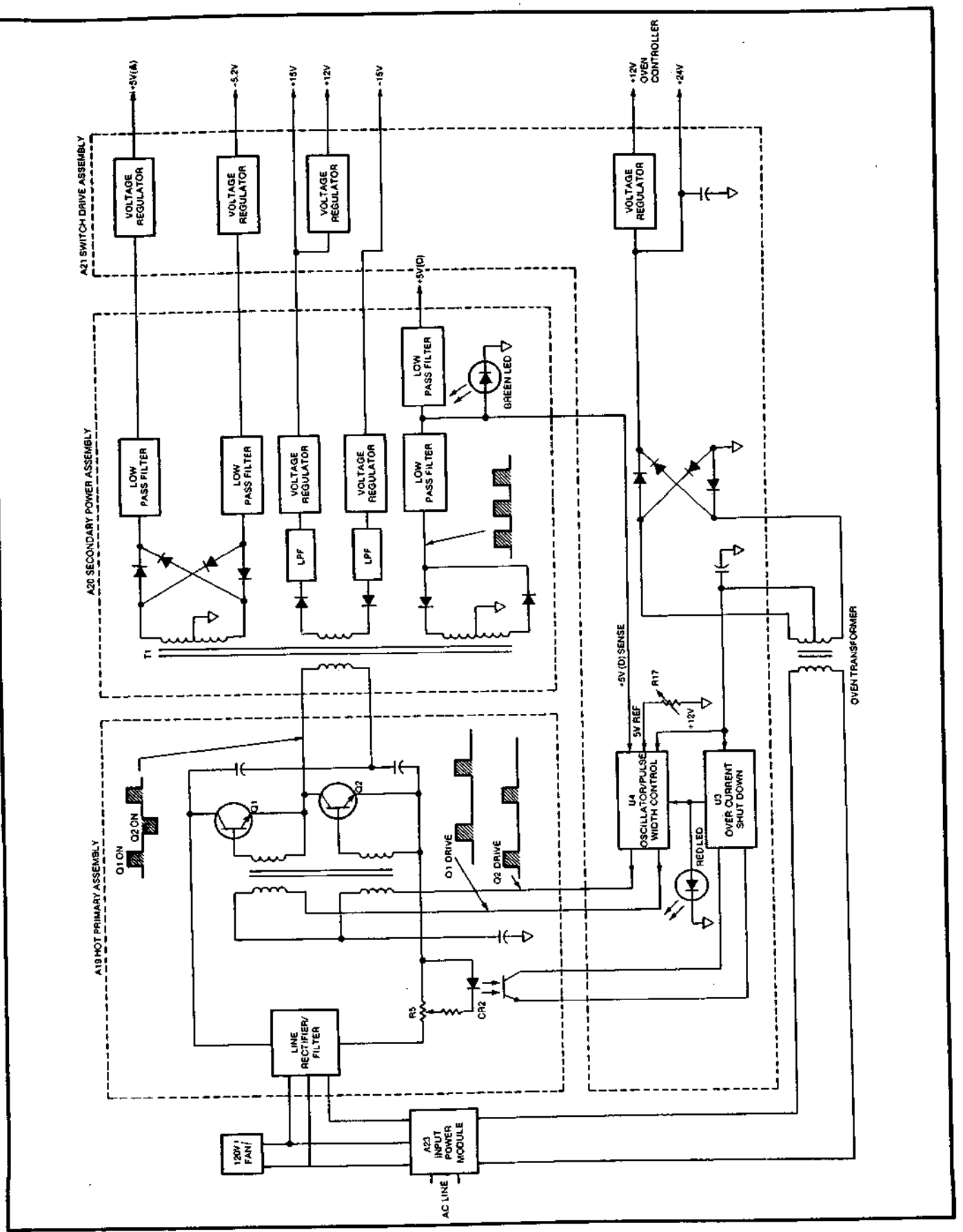


Figure 8-16. A19, A20, and A21 Power Supply Block Diagram

8-284. A22 MOTHERBOARD

8-285. The A22 Motherboard contains the XA (Assembly No.) connectors for the plug-in printed circuit assemblies (cards) and provides interconnections between the cards. The motherboard also contains terminals and connectors for interconnection of assemblies to the front and rear panels. See *Figure 8-22.*

8-286. A23 POWER MODULE

8-287. The A23 Power Module is mounted on the rear panel of the 5343A and contains a connector for a power cable, a fuse and a pc card. The pc card can be inserted in any one of four positions to select 100-, 120-, 200-, or 240-volt ac operation. The schematic diagram of the power module is shown in *Figure 8-42* and a detailed description is contained in paragraph 2-6.

8-288. A24 OSCILLATOR ASSEMBLY

8-289. The A24 oscillator board contains a 10 MHz crystal oscillator that supplies the internal signal to the A18 Time Base Buffer Assembly. An Option 001 A24 board contains an oven-controlled crystal oscillator (10544A) that results in higher accuracy and longer time periods between calibration. Refer to the specification listed in *Table 1-1.* The schematic diagrams for both oscillators is shown in *Figure 8-43.*

8-290. A25 IF MOTHERBOARD

8-291. As shown in *Figure 8-44,* A25 IF Motherboard provides connections for A25A1 2nd IF Preamplifier. A25 provides the dc operating voltages and connects the input/output circuits of A25A1 to other circuits in the instruments. Five filtering capacitors are mounted on this board, one for each voltage line and one for the overload line. Coaxial connectors are provided for the IF OUT INT (J3), IF OUT EXT (J4), and IF INPUT (J1). See *Figure 8-23* for interconnections.

8-292. 2nd Preamplifier A25A1

8-293. The 2nd Preamplifier receives the 1st Preamplifier output signal at PI($\overline{16}$), as shown in *Figure 8-44.* The signal passes through an elliptical filter consisting of coils L11, L9, L8, L10, and L12, capacitors C18, C19, and resistor R17. This filter reduces the IF bandwidth from 500 MHz to less than 175 MHz. Variable capacitor C19 is adjusted to provide the required roll-off at 175 MHz. Differential pair U2 provides approximately 14 dB gain.

8-294. The output of U2 passes through a 200 MHz low-pass filter whose main function is to filter out the fundamental sampling frequencies of the main oscillator and offset oscillator which appear in the output of the sampler. Differential pair U1 provides 14 dB gain and the output is coupled through capacitor C3 to A11 IF Limiter.

8-295. OVERLOAD CIRCUIT. Voltage comparator U3 and associated circuitry provide an overload signal proportional to the amplitude of the RF input. This circuit is not used in the 5343A.

8-296. Each of the operating voltages used in the instrument, +5, -5, +15, and -15 volts, dc is connected to an indicator (LED) on this assembly. These indicators are used during troubleshooting to supply a visual indication that the instrument operating voltages are at the required level. Each voltage is connected through a resistor and zener diode to an LED which is labeled with the appropriate value.

8-297. A26 SAMPLER DRIVER ASSEMBLY

8-298. The A26 Sampler Driver shown in *Figure 8-45* converts the LO FREQ sine wave signal into a negative spike waveform at the same frequency as the LO FREQ signal input. The spike goes from +0.7V dc to about -8V dc with a slew rate of approximately 8 picoseconds/volt. This fast transition is used to turn on the sampling diodes in the sampler for a few picoseconds and is necessary in order to produce useable harmonics of the VCO frequency up beyond 18 GHz.

8-299. The input frequency, in the range of 300 to 350 MHz, is applied to a common collector amplifier formed by one-half of transistor pair U1 (ac coupling for the LO FREQ signal is provided on the A5 RF Multiplexer). The otuput is taken off the emitter of the 1st transistor, through R5, and is applied to the common emitter formed by the other half of U1. Matching network R1, L1, C3, L3, L2, C1 is used to match the output impedance of U1 to the step recovery diode CR1.

8-300. AGC is provided by coupling part of the U1 output through CR5 to detecting diode CR2. The detected dc voltage which appears across C10 is used to cause transistor Q1 to conduct more or less current, thereby changing the gain through the first transistor in U1. The gain is changed in such a fashion as to cause the A26 output at the SMA connector A26J1 to have little change in amplitude for variations in input signal amplitude. The output is sent to U1 Sampler.

8-301. A28 FIRST PREAMPLIFIER

8-302. The First Preamplifier receives the output of U1 Sampler and provides approximately 20 dB gain, which is flat up to 175 MHz.

8-303. As shown in *Figure 8-46*, the first stage of amplification (transistor Q2 and associated components) provides approximately 10 dB gain. Resistors R8 and R11 provide negative feedback to stabilize Q2's operating point. Emitter resistors R12 and R13 are low inductance strip resistors and also provide negative feedback for gain stabilization. The amplified output of Q2 is coupled through dc blocking capacitor C6 to a similar stage of amplification built around Q1. The output of this second stage is approximately 20 dB greater than the U1 output and is coupled through capacitor C4 to the IF output. This signal is sent to the 2nd IF Amplifier A25A1.

8-304. OPTIONS THEORY (OPTIONS 004 AND 011)

8-305. The following paragraphs contain the theory of operation for the 5343A options as follows:

a. Option 004 Digital-to-Analog Conversion (DAC).

b. Option 011 Hewlett-Packard Interface Bus (HP-IB).

8-306. OPTION 004 DIGITAL-TO-ANALOG CONVERSION (DAC)

8-307. The digital-to-analog (DAC) conversion option (004) provides an analog output at the rear panel DAC OUT connector. Any group of three consecutive digits on the front panel display may be selected to produce an analog output of from 0 to 10 volts, dc as described in *Figure 3-4*. This conversion is performed by the circuit shown in *Figure 8-25*. The components of this circuit are added to the A2 Display Driver Assembly to provide Option 004.

NOTE

The following description assumes a knowledge of the theory of operation of A1 Display, A2 Display Driver (paragraph 8-132) and A14 Microprocessor (paragraph 8-225).

8-308. The four data lines, D0-D3, and two address lines A_0, A_1 are connected to the input of the DAC circuit as shown in *Figure 8-25*. These lines from A14 Microporocessor are connected via U16 on A2 assembly as shown in *Figure 8-24*. The only other signal input to the DAC circuit is the Load Digital Analog (LDA) signal from Decoder U17 on A14 Microprocessor.

8-309. Data lines D0-D3 are connected to counters U15, U21 and U22 which act as buffer registers (control lines connected to +5V). When LDA is low, the A_0 and A_1 lines are decoded by U16 to provide a clock signal to the buffer registers. Each of the buffer registers provides a 4-bit output to the 12-bit digital-to-analog converter U24. Register U15, U21 and U22 provide the least-, next- and most-significant digit, respectively, to U24 for conversion to analog voltage which is output at pin 15 to the DAC OUT connector.

8-310. The GAIN ADJ variable resistor R25 and OFFSET variable resistor R26 are internal service adjustments to set the high and low limits of the DAC output voltage. Refer to paragraph 5-32 for adjustment procedures.

8-311. To keep incremental changes in the DAC output as small as possible, the 5343A should be operated in the manual mode with minimum required resolution and as fast a sample rate as possible. If operating with a low sample rate or high resolution (1 Hz is highest) and a rapidly changing counted input, the DAC output will change in large increments. The AUTO operating mode may also have a similar effect with a resultant loss of smoothness in the DAC output.

8-312. OPTION 011 HEWLETT-PACKARD INTERFACE BUS (HP-IB)

8-313. Introduction

8-314. The A15 HP-IB Assembly serves as an interface between the microprocessor on A14 and the device controlling the lines of the HP interface bus as shown in *Figure 8-38*. The A15 HP-IB consists of seven interface registers (which are used by the microprocessor for interpreting commands and data, sending status, sending data, interpreting interrupts, etc.), two command decoding ROM's, source handshake circuitry, and acceptor handshake circuitry.

8-315. Interface Registers

8-316. There are seven interface registers on A15 which are used by the A14 microprocessor to communicate with the device controlling the HP interface bus. A register is selected by the microprocessor when the microprocessor sends that particular register's address. This address is decoded by 1-of-8 decoder U11. Decoder U11 is enabled by the LHPIB signal (decoded from address lines on A14) and the phase 2 clock, $\phi 2$, also from A14. A particular register is selected by decoding the two-least-significant address lines of the microprocessor, LAØ and LA1, in addition to the read/write line, LR/HW also from A14. The following table shows which register is selected for each combination of the three inputs to U11, provided U11 is enabled by LHPIB and $\phi 2$.

U11(3) (LR/HW)	U11(2) (LA1)	U11(1) (LAØ)	U11 OUTPUT GOES LOW	ENABLES REGISTER
0	0	0	U11(15)	U30 STATE IN
0	0	1	U11(14)	U15 COMMAND IN
0	1	0	U11(13)	U18 INTERRUPT IN
0	1	1	U11(12)	U27 DATA IN
1	0	0	U11(11)	— —
1	0	1	U11(10)	U16 CONTROL OUT
1	1	0	U11(9)	U24 STATUS OUT
1	1	1	U11(8)	U21 DATA OUT

8-317. State In buffer U30 is read by the microprocessor when the microprocessor wants to determine the state of the interface. Listen flip-flop U20B, talk flip-flop U20A, serial poll mode flip-flop U29B, remote flip-flop U29A, and service request flip-flop U9A are all buffered by U30. Buffer U30 is enabled by U11(15) going low.

8-318. Command In register U15 is read by the microprocessor whenever an addressed command is sent by the controller.

8-319. Interrupt In buffer U18 is read by the microprocessor in response to an interrupt. The output of the interrupt buffer indicates why the A15 assembly generated the interrupt (LIRQ low).

8-320. Data In register U27 stores programming codes which have been sent over the HP-IB by the controller. Data In register U27 is clocked by decoding ROM U23(5) which sets Data flip-flop U19A. After one byte of ASCII program data has been clocked into U27, an interrupt is generated by A15 and the microprocessor reads the U18 Interrupt In buffer to find out why the interrupt was generated. Since U18(2) is high, the microprocessor knows that program data is ready to be read from U27. The microprocessor then reads U27. If the byte completes a code (for example, the "5" of the code "SR5"), the microprocessor executes the code and then continues executing the operating program. If the byte does not complete a code, the microprocessor waits until the completed code has been sent.

8-321. Control Out register U16 is used by the microprocessor to control the HP-IB board. For example, in response to a front panel reset, the microprocessor returns A15 to local control by setting U16(10) low then high, which resets the remote flip-flop U29B. On power up, U16(2) is set low then high which resets Serial Poll FF U29B, Talk FF U20A, and Listen FF U20B. When measurement data is sent to the HP-IB, the microprocessor sets U16(12) low which sets the EOI control line of the HP-IB low after the final byte of the data message is sent (i.e., after CR, LF).

8-322. Status Out register U24 is used by the microprocessor to send a status byte when the serial poll mode is ordered by the system controller. The microprocessor sends octal 120 (01010000) to indicate that it has pulled on SRQ (bit 7) and that a measurement has been completed (bit 5).

8-323. Data Out register U21 is used by the microprocessor to output measurement data, one byte at a time, to the HP-IB. U21 is clocked by the Address Decoder U11 and is enabled by Serial Poll FF U29B being set low (not serial poll mode).

8-324. Command Decoding ROM's

8-325. Decoding ROM's U23 and U26 decode bytes sent over the data lines of the HP-IB. The acceptor handshake operates when LATN is low (address information is being sent) or when the Listen flip-flop has been set. Decoding ROM U23 is enabled only during the acceptor handshake cycle. The outputs of the ROM's generate interrupts, set or reset various control flags, and are read by the microprocessor via Command in register U15.

8-326. During the acceptor handshake; U1C(8) goes low for one period of the $\phi 2$ clock just prior to the HDAC signal going high, thus enabling U23 (U26 is always enabled). The byte on the data lines of the HP-IB appears at the inputs to U23 and U26. The ROM outputs change accordingly.

8-327. If the Unlisten command is given, U26(1) goes low and U23(2) goes high to clock Unlisten FF U20B, causing it to be reset. If a talk address other than the 5343A's talk address is sent, U23(1) goes high to clock into the U20A Talk FF the output of Address Comparator U33. Since the 5343A's talk address was not sent, U33(14) is low and the U20A Talk FF is set low. If the 5343A's listen address is sent, U23(2) goes high to clock a high from U33(14) into Listen flip-flop U20B.

8-328. Now that the 5343A is addressed to listen, consider what occurs when program data is sent. When program data appears at the inputs to ROM's U23 and U26, output U23(5) goes low to set the Data flip-flop, U19A. When U23(5) returns high, Data In register U27 is clocked and the data byte is stored in U27. At the same time that U23(5) goes low, U23(6) goes low which resets Interrupt flip-flop U14A and causes LIRQ (the output of U17B) to go low and interrupt the microprocessor. The microprocessor reads Interrupt In buffer U18 (which clears interrupt FF U14A), determines that program data is in U27, and reads U27. When U27 is read (U27(1) goes low), the U19A Data flip-flop is reset in preparation for the next byte.

8-329. Consider what occurs when an addressed command or universal command is sent by the controller. If a command is sent, U23(4) goes low which sets Command flip-flop U14B. When U23(4) returns high, it clocks into Command In register U15 the decoded outputs from U26 as follows:

Command	U26(4)	U26(5)	U26(6)	U20(9)	
LLO (Local lockout)	0	0	0	1	Universal
DCL (device clear)	1	0	0	1	Commands
GTL (go to local)	0	0	1	0	
SDC (selected device clear)	1	0	1	0	Addressed
GET (group execute trigger)	0	1	1	0	Commands

8-330. At the same time that U23(4) goes low, U23(6) goes low. This sets Interrupt flip-flop U14A and causes LIRQ to go low, whch interrupts the microprocessor. The microprocessor reads Interrupt In buffer U18, determines that a command code is in U15, and reads U15. The microprocessor determines which command was sent according to the table and acts accordingly.

8-331. When the serial poll enable signal is sent, U26(2) goes high and U23(3) goes high to clock Serial poll flip-flop U29B to the high state. When the serial poll disable signal is sent, U26(3) goes low and U23(3) goes high to clock U29B to the low state.

8-332. Acceptor Handshake

8-333. The acceptor handshake is enabled by U1B(4) low (LATN control line of bus is low, indicating address information is being sent) or U1B(5) low (the 5343A has been addressed to listen). When the talking device puts data on the HP-IB data bus and pulls LDAV low indicating data valid, the acceptor handshake causes HDAC to go high (indicating that the data has been read into U27). After the data in U27 has been read by the microprocessor, the acceptor handshake causes HRFD to go high, indicating that U27 has been read by the MPU and that the MPU is ready to receive the next data byte.

8-334. A timing diagram of a typical acceptor handshake is shown in *Figure 8-17*. The talker places a data byte on the eight data lines and, after allowing for settling, pulls LDAV low to indicate to the listener (5343A in this case) that there is valid data on the data bus. The first positive transition of the $\phi 2$ clock after LDAV goes low, clocks a high into flip-flop U3B(9). This causes the input to U3A(2) to go high. On the next clock, U3A(5) goes high and U3A(6) goes low. U3A(5) high and U3B(9) high cause U1C(8) to go low which enables ROM U23. When ROM U23 is enabled, Data flip-flop U19A(5) is set high which causes U32(12) to go high (HRFD goes low) and also clocks the data into U27. Simultaneously, LIRQ goes low to interrupt the microprocessor. The next $\phi 2$ clock causes U3B(9) to return low, thus disabling U23. Since U3B(9) is low and U3A(6) is low, HDAC goes high, indicating to the talking device that the data has been accepted (read into U27) and may be removed from the data lines. The talker then removes the data from the bus and takes LDAV high to indicate that there is not valid data on the bus. U3A(2) goes low when LDAV goes high. On the next positive transition of $\phi 2$, the low at the input to U3A is clocked into the output, causing U3A(5) to go low and U3A(6) to go high. This causes HDAC to return low. After the

microprocessor reads the Interrupt In register U18 and determines that data is stored in U27, the U27 Data In register is read by the MPU. This causes the U19A data flag to be reset and also causes HRFD to go high, indicating that the Data In register has been read and is ready for another data byte. The handshake process then repeats as described.

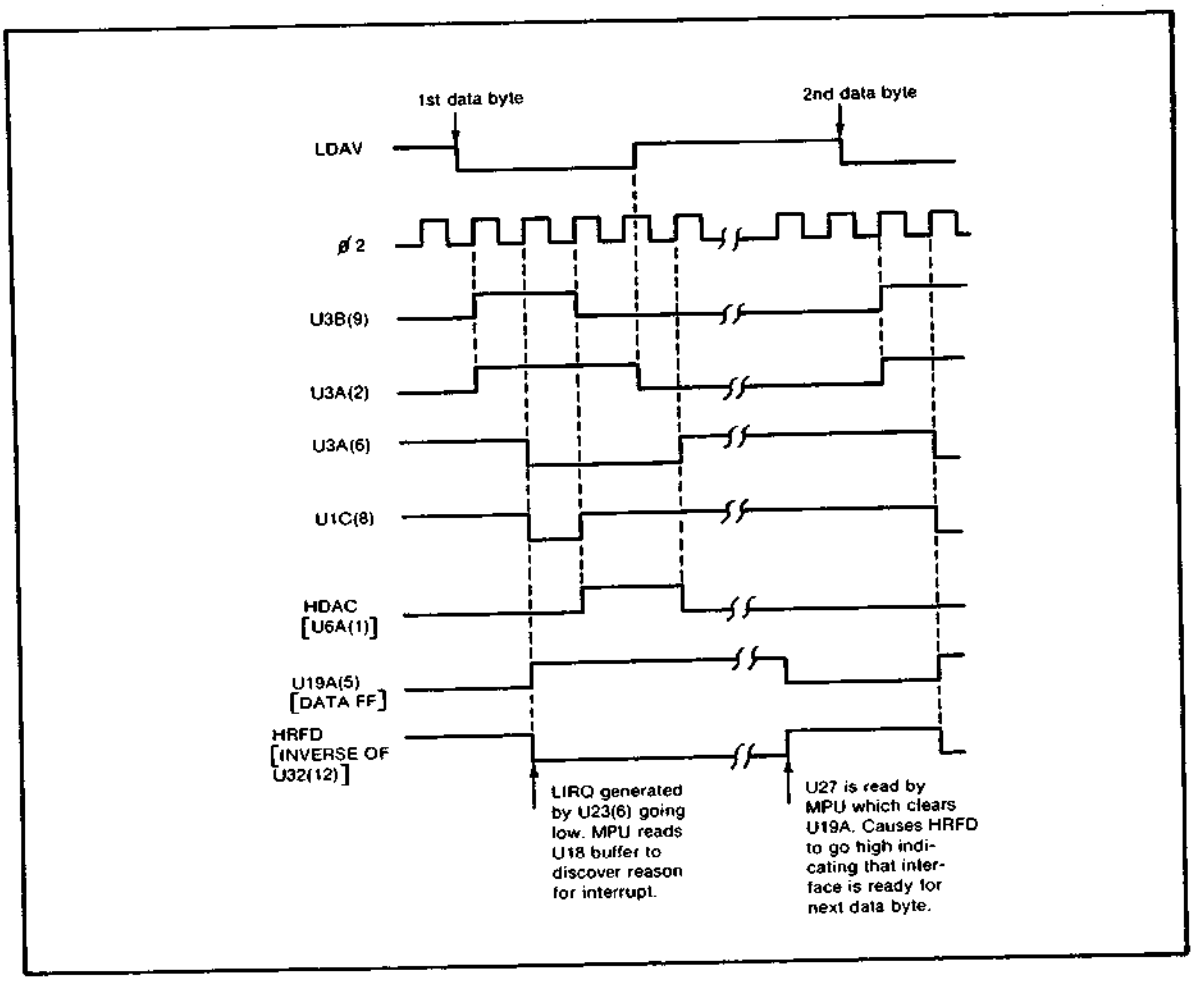


Figure 8-17. Acceptor Handshake Timing Diagram

8-335. Source Handshake

8-336. The source handshake controls the LDAV control line of the HP-IB in response to the state of the HDAC and HRFD control lines which are controlled by the acceptor handshake circuitry in the listening device. When the 5343A operating program finishes a measurement, the microprocessor reads State In buffer U30 to see if the counter has been addressed to talk. If the counter has been addressed to talk, the microprocessor reads Interrupt In buffer U18 to determine the state of Data Out flip-flop U9B. If U9B(9) is high, then the previous data byte has been accepted by the listener and a new data byte may be written into Data Out register U21. When a data byte is written into U21, U9B(9) is reset low and the source handshake logic sets LDAV low, two $\phi 2$ periods later. When the listener sets HDAC high, U9B(9) goes high on the next positive transition of the $\phi 2$ clock. Since the listener has accepted the data, a new data byte is written into U21. However, LDAV will not go low again until the listener sets HRFD high to indicate that it is ready for more data. Data Out register U21 is always enabled if the Serial Poll FF U29 is set low. The output data bus drivers, U22, U25, U31, and the source handshake circuits however, are only enabled in talk mode and LATN set high.

8-337. A timing diagram of a typical source handshake is shown in *Figure 8-18*. Since U9B(9) is high, the microprocessor clocks data into U21. This clock also resets U9B(9) low. U9B(9) going low causes the input to flip-flop U4B to go low, and U4B's output goes low on the next $\phi 2$ clock positive transition. Since U4(9) is low and HRFD is high, the input to flip-flop U4A(2) goes high and the U4(5) output goes high on the next clock. When U4(5) goes high, LDAV at U36(3) goes low. Sometimes later the listener set HDAC high to indicate that the data has been accepted. HDAC going high causes the U4(12) flip-flop input to go high and the U4(9) output goes high on the next clock pulse. Since U4(9) is high and U4(5) is high, U12(6) goes high and sets the Data Ready flip-flop U9(9) to high. When U9B(9) goes high, U4(2) input goes low and causes the U4(5) flip-flop output to go low on the next clock. This causes LDAV to return high. After LDAV goes high, the listener reset HDAC low in preparation for the next handshake cycle. Since U9B(9) is high, the microprocessor writes the second data byte into U21. U21(11) going high resets U9B(9) to a low which sets the U4B(9) flip-flop output low. However, the source handshake logic can not indicate the presence of the second data byte (by pulling LDAV low) until the listener sets HRFD high. When HRFD finally does go high, the output of flip-flop U4(5) goes high on the first clock after HRFD goes high. U4(5) going high sets LDAV low. When the listener senses LDAV low, it sets HRFD low and the process continues as previously described.

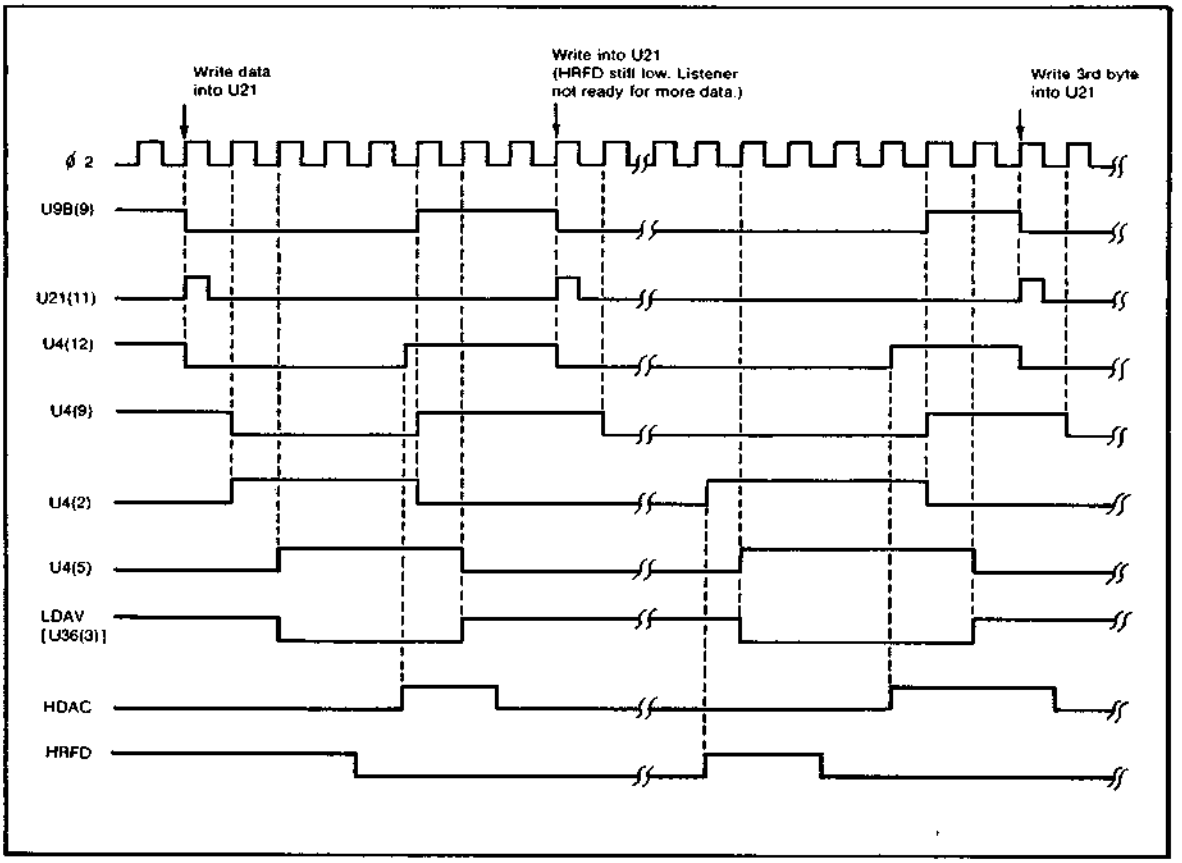


Figure 8-18. Source Handshake Timing Diagram

8-338. ASSEMBLY LOCATIONS

8-339. *Figures 8-19, 8-20, 8-21* and *8-22* shows the front (A1 Display Assembly) rear, top and bottom views, respectively, of the 5343A. The front and rear views show reference designators of the front and rear panel controls, connectors, and indicators. The top view shows assembly locations and adjustments.

8-340. TROUBLESHOOTING TO THE ASSEMBLY LEVEL (STANDARD INSTRUMENT)

8-341. Troubleshooting Technique

8-342. In the troubleshooting procedure outlined in *Table 8-5*, the 5343A is exercised through a series of operating modes which are arranged in an increasing order of complexity. As can be seen in *Table 8-6*, an increasing number of assemblies is exercised as the operating modes progress from the first mode (power-up diagnostic) to the last mode (HP-IB). By noting the first mode in the sequence that fails, it is possible to isolate the defective assembly to a specific group of assemblies by noting those assemblies common to the current (failed) test and all previous tests (which passed). These common assemblies can be eliminated as being the source of the failure and only those assemblies which are not common to previous operating modes are examined. *Table 8-7* is a list of the noncommon assemblies for each of the operating modes and it is the basis for the troubleshooting procedure presented in *Table 8-5*.

8-343. *Tables 8-9* through *8-22* are individual troubleshooting procedures for various assemblies and assembly groups and are referenced in the overall troubleshooting of *Table 8-5*. By using the diagnostic modes of the 5343A, explained in *Table 8-6*, and the test equipment listed in *Table 1-4*, the troubleshooting procedure outlined in *Table 8-5* and *Tables 8-9* through *8-22* allows isolation of a failed assembly. By reading the detailed theory of operation of the assembly and referencing the dc voltages and 5004A signatures provided on the individual schematics, it should be possible to find the failed components.

8-344. *Figure 8-23* is a detailed description block diagram of the 5343A and is valuable in troubleshooting. *Figure 8-9* shows the relationship of the assemblies listed in *Table 8-6*.

8-345. RECOMMENDED TEST EQUIPMENT

8-346. Test equipment recommended for troubleshooting, adjustments, operational verification, and full performance testing is listed in *Table 1-4*. Equipment other than that listed may be used if it meets the required characteristics.

Table 8-5. Overall Troubleshooting

1. POWER UP DIAGNOSTIC — Apply power to the 5343A and press front panel power switch to ON. The power-up diagnostic routine progressively lights all LED segments in the 5343A display, from left to right. Finally, the following should be displayed briefly:

   a. If the 5343A powered up properly, go to step 2. If not:

      (1) Check the -15V, +15V, -5V, and +5V power supply indicator LEDs at the top of the A25A1 board. If any of the indicators are not lit, refer to *Table 8-9* for power supply troubleshooting.

      (2) If E's fill the display, then RAMs A16U11 or A16U14 failed the check sum routine exercised on power up. The RAMs may be faulty if none of the address lines AØ—A15 or data lines DØ—D7 are stuck low or high. Check address lines and data lines on A16 for stuck nodes (use current tracer such as 547A to find faulty device). Stuck data lines may be caused by stuck ROM outputs or stuck buffer inputs. If 1 is displayed, then ROM A16U6 failed the check sum routine exercised on power up. Since the RAMs proved good (E's were not displayed), the data lines and address lines be OK. Replace A16U6.

      (3) If 2 is displayed, then ROMs A16U11 or A16U14 failed the check sum routine exercised on power up. Replace ROM.

   b. Go to *Table 8-10* for A14 testing, *Table 8-11* for A16 Memory and Sweeper Control testing.

   c. Go to *Table 8-12* for A1, A2 Keyboard/Display testing.

2. DIAGNOSTIC MODE 8 — Put the 5343A in diagnostic mode 8 (see *Table 8-8* for a description of diagnostic modes and how to set them). Perform the keyboard check, paragraph 3-52. If the 5343A operates properly, go to step 3. If not:

   a. Go to *Table 8-12* for A1, A2 testing. If the 5343A passed the power-up diagnostic test but failed the diagnostic mode 8 test, then likely problems on A1, A2 are failed A1 keyboard or failed A2 keyboard decoding circuitry such as A1U23, U13, U19, U20, etc.

   b. Go to *Table 8-10* for A14 testing. The difference between this test and the previous test is that the LKBRD device select is sent by A14.

3. DIRECT COUNT MODE — Apply the 10 MHz FREQ STD OUT from the rear panel of the 5343A to the direct count input (front panel BNC). Place the impedance select switch in 50Ω position and place the range switch in the 10 Hz—500 MHz position. If the counter counts 10 MHz ±1 count for all resolution settings, go to step 4. If not:

   a. Check the A3 Direct Count Amplifier (*Table 8-14*).

   b. Check the A14 Microprocessor as described in *Table 8-10*. A difference between this test and previous tests is that LCTRRD, LCTRWRT, TMRD, LTMWRT device select codes are used.

   c. Check the A13 counter (*Table 8-15*). Only the A counter is used in this mode.

   d. Check the A17 timing generator (*Table 8-13*). Only the gate time generation circuitry is used in this mode.

4. CHECK MODE — Place the 5343A in CHECK (place range switch in 500 MHz—26.5 GHz posititon) and verify that the counter displays 75 MHz ±1 count for all resolution settings. If the counter operates properly, go to step 5. If not:

   a. Go to *Table 8-10* for A14 Microprocessor testing. A difference between this test and previous test is that LSYNHI, LSYNLO, LPDREAD, LPDWRT device select codes are used.

   b. Check that the 500 kHz output of A18, available at XA18(3), is present.

   c. Go to *Table 8-16* for A8, A9, A10 Main Loop Synthesizer troubleshooting.

   d. Go to *Table 8-17* for IF troubleshooting. Since the check signal enters the IF chain at A11($7,\overline{7}$) the 1st and 2nd Preamplifiers and the U1 Sampler can be eliminated as possible failed modules.

Table 8-5. Overall Troubleshooting (Continued)

5. AUTO/50 MHz MODE — Place the 5343A in AUTO mode, with the range switch in the 500 MHz—26.5 GHz position and apply a 50 MHz signal at –10 dBm to the high frequency input. Verify that the counter counts 50 MHz ±1 count for all resolution settings. If the 5343A operates properly, go to step 6. If not:

   a. Place the 5343A in diagnostic mode Ø. If the counter displays SP or SP2 only (instead of SP23 followed by Hd), then the failure is likely in the U1 Sampler or the Preamplifiiers since A11 and A12 are used in the CHECK mode. Go to IF troubleshooting in *Table 8-17*.

   b. If the counter (still in diagnostic mode Ø) displays SP23 but does not display Hd, suspect A17 PRS generation circuitry. Go to *Table 8-13* for A17 troubleshooting.

   c. If the counter displays an incorrect answer, go to diagnostic mode 4 to verify that the IF measured is 50 MHz. If it is not, check the A counter on A13 (*Table 8-15*). Also go to diagnostic mode 1 to check the N number computed. If N is not Ø, check the B counter on A13 (*Table 8-15*).

6. AUTO/1 GHz MODE — Place the 5343A in AUTO mode, with the range switch in the 500 MHz—26.5 GHz position and apply a 1 GHz signal at –20 dBm to the high frequency input. Verify that the counter counts 1 GHz ±1 count for all resolution settings.

   a. Place the 5343A in diagnostic mode Ø. If the counter displays SP (instead of SP23 followed by Hd), then the failure may be A26 Sampler Driver, A5 RF Multiplexer, or the MAIN and OFFSET Loop Synthesizers. Go to *Table 8-20* for A26 Sampler Driver troubleshooting and *Table 8-19* for A5 Multiplexer troubleshooting.

   b. Check U1 Sampler per *Table 8-17*, step 2.b.

7. SWEEP MODE — Place 5343A in SWEEP mode by pressing SWP M button on front panel key board. Observe slow blinking lamp in key, and blank display.

   a. With a short jumper wire, connect SWP INTFC A jack on rear panel to ground. 5343A should trigger, and take a measurement if an input signal is applied.

   b. Using an oscilloscope, observe a negative true TTL level at SWP INTFC B jack on rear panel when step a. above is executed.

   If problems with the SWEEP mode are evident, go to *Table 8-11* for troubleshooting information.

8. TOTALIZE MODE — Place 5343A in TOTALIZE mode (press SET, SET, 9) with a signal connected to the low frequency input (10 Hz—500 MHz). Observe accumulative counting on display and steady illumination of GATE LAMP.

   a. All of the circuit assemblies used in TOTALIZE mode have been checked in the preceding mode tests. TOTALIZE mode is a software function programmed into the 5343A ROMs.

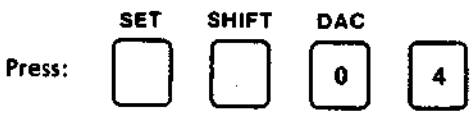
   b. If TOTALIZE mode fails to function, recheck the A14 and A16 assemblies. In particular, the ROM signatures on A16 may be incorrect.

9. DAC MODE — Place the 5343A in the Option 004 DAC mode as follows:

   a. Apply the input frequency of 1000.00 MHz to the 5343A.

   b. Connect a DVM to the DAC output jack on the rear of the 5343A. Set DVM to 0—200 range.

   c. Set up digits for conversion as follows:



   d. Observe on the DVM A reading of .001 (±.005)V.

   e. Adjust the input frequency to 999.9XXX MHz. Observe on the DVM a reading of 10.000 (±.005)V.

   If these indications are not obtained, refer to *Table 8-22*, DAC Option 004, Troubleshooting Procedures.

Table 8-6. Assemblies Tested by Test Mode

ASSEMBLIES	TEST MODES								TROUBLESHOOTING TABLE NO.
	POWER-UP DIAG.	SET 8 DIAG.	DIRECT COUNT	CHECK	AUTO 50 MHz	AUTO 1 GHz	SWEEP MODE	HP-IB	
A1 Keyboard Display	√(1)	√	√	√	√	√			Table 8-12
A2 Display Driver	√(2)	√	√	√	√	√			Table 8-12
A2 DAC (Option 004)	√(2)	√	√	√	√	√			Table 8-22
A3 Direct Count Amp			√						Table 8-14
A4 Offset VCO						√			Table 8-18
A5 RF Multiplexer						√			Table 8-19
A6 Offset Loop Amp						√			Table 8-18
A7 Mixer/Search Control						√			Table 8-18
A8 Main VCO				√(12)		√		√	Table 8-16
A9 Main Loop Amp				√		√		√	Table 8-16
A10 Divide-by-N				√		√		√	Table 8-16
A11 IF Limiter				√	√	√		√	Table 8-17
A12 IF Detector				√	√	√		√	Table 8-17
A13 Counter			√(7)	√(7)	√	√		√(7)	Table 8-15
A14 Processor	√(3)	√(6)	√(8)	√	√	√		√	Table 8-10
A15 HP-IB (Option 011)								√	Table 8-21
A16 Memory/Sweeper	√(11)	√(11)	√(11)	√(11)	√(11)	√(11)	√		Table 8-11
A17 Time Base Generator	√(4)	√(4)	√(9)	√(9)	√	√		√(9)	Table 8-13
A18 Time Base Buffer	√(5)	√(5)	√(5)	√	√	√		√	Table 8-13
A19 Primary Power	√	√	√	√	√	√		√	Table 8-9
A20 Secondary Power	√	√	√	√	√	√		√	Table 8-9
A21 Switch Drive	√	√	√	√	√	√		√	Table 8-9
A24 Oscillator	√	√	√	√	√	√		√	Table 8-13
A25 A1 Second IF					√	√			Table 8-17
A26 Sampler Driver						√			Table 8-20
A28 First IF					√	√			Table 8-17
U1 Sampler					√(10)	√			Table 8-17

NOTES: (1) Keyboard not exercised.
(2) Keyboard decoding circuitry such as A2U23, U13, U19, U20 not exercised.
(3) HDSPWRT select code is only device select code exercised.
(4) A17U8 only is exercised; sends 1 MHz clock to A14.
(5) 1 MHz output only is used.
(6) HDSPWRT, LKBRD select codes are only device select codes excerised.
(7) B counter not exercised.
(8) LPDREAD, LPDWRT, LSYNHL, LSYNLO device select codes not exercised.
(9) PRS generation circuitry not exercised.
(10) Tests only that at least one of the two diodes is not open.
(11) ROM and RAM only are exercised.
(12) Only "÷N" output is checked.

Table 8-7. Probable Failed Assemblies by Test Mode

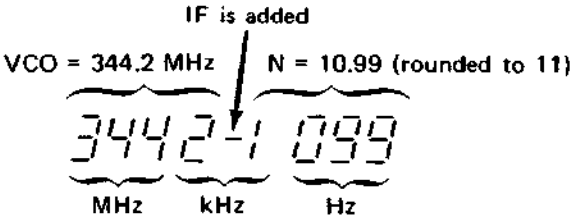
TEST MODES					
POWER-UP DIAG.	SET 8 DIAG.	DIRECT COUNT	CHECK	AUTO 50 MHz	AUTO 1 GHz
A1	A1(1)	A3	A8	A17(9)	A4
A2	A2(2)	A13(4)	A9	A25A1,A28	A5
A14	A14(3)	A14(5)	A10	U1	A6
A17		A17(6)	A11	A13(10)	A7
A18			A12		A8
A19			A14(7)		A26
A20			A18(8)		U1
A21					
A24					

NOTES:

(1) A1 keyboard.
(2) A2 keyboard decoding circuitry such as A2U23, U13, U19, U20.
(3) A14 LKBRD device select code.
(4) A counter.
(5) A14 LCTRRD, LCTRWRT, LTIMRD, LTIMWRT device select codes.
(6) A17 gate time generation.
(7) A14 LSYNHI, LSYNLO, LPDREAD, LPDWRT device select codes.
(8) A18 500 kHz output.
(9) A17 prs generation.
(10) A13 B counter exercised.

Table 8-8. Diagnostic Modes of the 5343A

To go to a diagnostic mode, press front panel SET key twice (SET, SET) and then the number corresponding to the desired mode. For example, pressing SET SET 8 goes into diagnostic mode 8, the keyboard check. To leave a diagnostic mode, press RESET . The following describes the available diagnostic modes:

DIAGNOSTIC MODE	FUNCTION
0	Displays mnemonics SP 23 followed by Hd. SP indicates that the VCO's are sweeping. 2 indicates an IF of sufficient amplitude and in the range of 50—100 MHz. 3 indicates that there is a proper IF for both the Main VCO and OFFSET VCO. 3 is displayed after the VCO's have stopped sweeping. Hd indicates harmonic determination has been complete. It is displayed at the end of the prs.
1	Counter displays Main OSC in MHz to 100 kHz, sign of IF (+ for subtract and - for add) and the harmonic number N. For example:  This is displayed at the end of the harmonic determination. (The (-) sign of the IF indicates that the Nth harmonic of the VCO is **less** than the unknown so that the IF must be added; the (+) sign of the IF indicates that the Nth harmonic of the VCO is **greater** than the unknown so that the IF must be subtracted.)
2	Counter continuously displays the contents of the A counter during harmonic determination.
3	Counter continuously displays the contents of the B counter during the harmonic determination.
4	Counter continously displays the measured IF frequency. Resolution determined by resolution selected before going to diagnostic mode 4.
5	Not used.
6	Not used.
7	Sweeps Main VCO from 350 MHz to 300 MHz in 100 kHz steps. Time between updates in VCO frequency determined by SAMPLE RATE setting. To stay at a particular frequency, put SAMPLE RATE to HOLD. (Remove input signal to counter, place counter in 500 MHz—26.5 GHz range and AUTO mode.)
8	Keyboard check. Refer to paragraph 3-52 for complete list of what should be displayed when each key is pressed.

To return to normal operation, press RESET .

TABLE 8-8 DIAGNOSTIC MODES

Table 8-9. A19, A20, A21 Power Supply Troubleshooting

CAUTION

It is extremely dangerous to troubleshoot the A19 assembly of the power supply if an isolation transformer is not used. A19 is connected directly to the power main. Use an isolation transformer such as Allied Electronics P/N 705-0165 (115/120V ac) to isolate the instrument from the power main. The measurements in this troubleshooting procedure may be made only if an isolation transformer is used.

1. Connect 5343A power cord to isolation transformer.
2. The first step in power supply troubleshooting is to check the state of the green LED on A20 and the red LED on A21. If the green LED is on and the red LED is off, then the +5V(D) supply is working properly. If the red LED is on and the green LED is off, then one or more of the voltage outputs of A20, A21 may be drawing excessive current. Even if the green LED is on, one of the regulated outputs of A21 may be shut down due to excessive current. Check the following voltage levels:

SUPPLY	LOCATION	VALUE
-5.2V	XA15B(3)	-5.2 (-0.1, +0.05)V*
+5V(D)	XA15B(4)	+5 (±0.1)V
+15V	XA15B(2)	+15 (±0.5)V
-15V	XA15B(1)	-15 (±0.5)V
+5V(A)	XA5(7)	+5 (±0.1)V
+12V oven	XA21(14)	+12 (±0.5)V
+12V	XA21(16, 16)	+12 (±0.5)V

*If this voltage is not correct, adjust A21R17 before making other voltage measurements.

NOTE

If one or more of the voltage outputs is at ground, then a problable cause is that one of the assemblies in the instrument connected to that voltage output has a short to ground. Remove assemblies connected to that voltage output, one at a time, until the short is removed. After removing an assembly, replace it in the instrument if that assembly is not the problem. This must be done because the power supply looses regulation if not run at approximately 75% of full load. The following table shows which assemblies are connected to the various supply voltages:

SUPPLY	FROM	TO
+5V(D)	XA20(18, 18)	A1, A2, A12, A13, A14, A15, A16, A17, A19
-5.2V	XA21(5, 5)	A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A15, A16, A17 A25, A26
+15V	XA21(14)	A4, A6, A7, A8, A9, A10, A11, A12, A13, A15, A16, A17, A25
-15V	XA21(13)	A6, A7, A9, A10, A11, A12, A13, A15, A16, A17, A25
+5V(A)	XA21(1, 1)	A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A16, A18, A25, A26
+12V oven	XA21(14)	A24(8, 8)
+12V	XA21(16, 16)	A24(3)
+24V	XA21(11, 11)	A24(8, 8)

CAUTION

The waveforms in the following paragraphs require using an isolation transformer as described in the CAUTION preceding step 1.

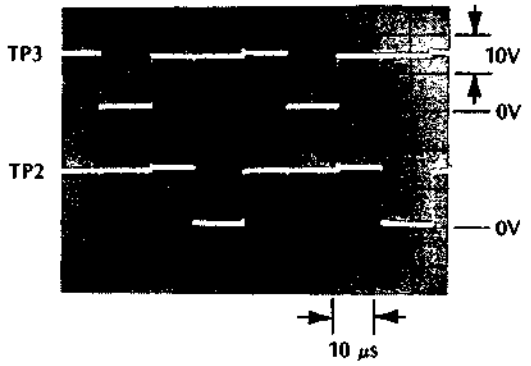
TABLE 8-9
A19, A20, A21

Table 8-9. A19, A20, A21 Power Supply Troubleshooting (Continued)

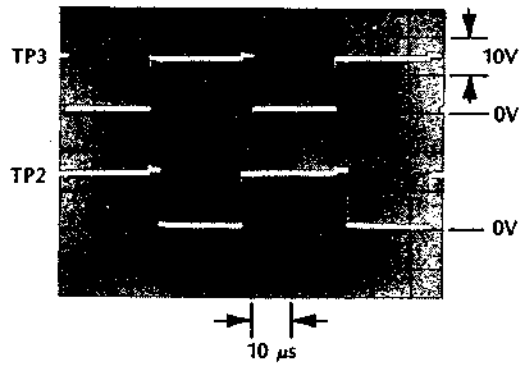
3. A21 Troubleshooting

   a. Pull A19 and A20 from the instrument and put A21 on an extender board. Plug the 5343A to the line but leave the ON/STBY switch in STBY. Measure the voltage at test lead TLS (labeled TLS 13.5V), which is the positive side of A21C20, and verify that this voltage is approximately 13.5 volts. If not, suspect rectifier A21CR2 or oven transformer T4.

   b. With the 5343A still in STBY, monitor test points TP2 and TP3 on A21 with an oscilloscope. Short TPJ and TPG (lower right corner TP on A21) together. Observe the following waveforms:



   Now remove the short from TPJ to TPG and observe:

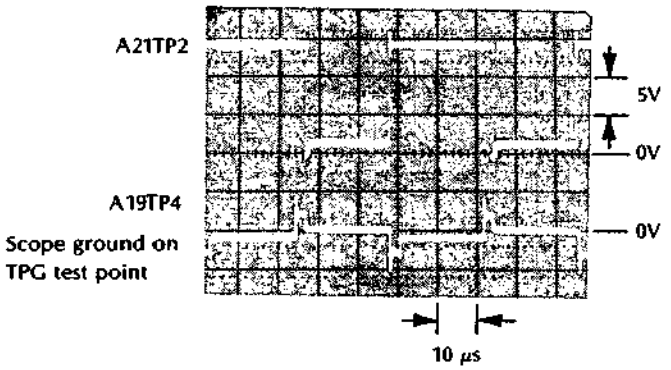


   c. Connect a clip lead to A21TP4 and momentarily ground the other end to the chassis. Observe red LED turn on for approximately 1–2 seconds and waveforms at TP2, TP3 go to a constant +13 volts for same duration. If not, suspect A21U3.

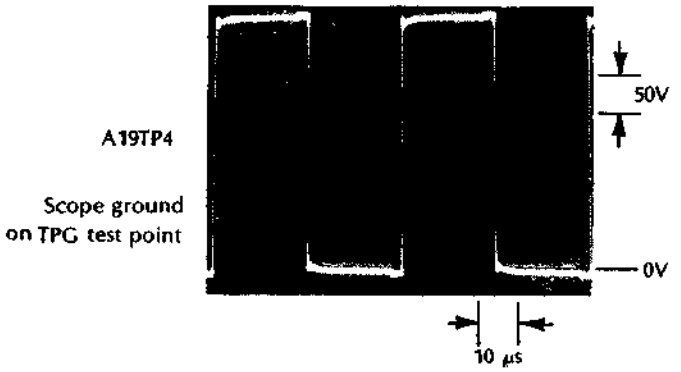
TABLE 8-9
A19, A20, A21

Table 8-9. A19, A20, A21 Power Supply Troubleshooting (Continued)

4. With A21 still on extender board (remove short from TPJ to TPG), insert A19 on an extender board into the instrument (A20 is still out of the instrument). Leave the 5343A line switch in STBY. The waveform at A19TP4 indicates that A19 transformers T1 and T2 are operating properly.



Now set front panel line switch to ON and observe:



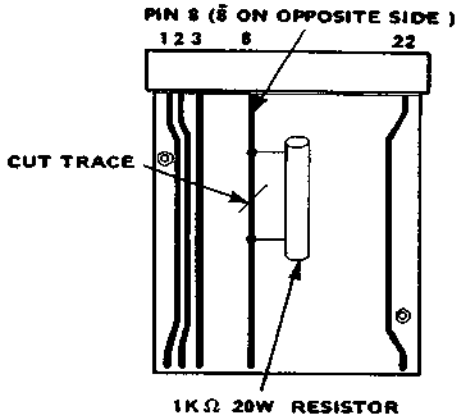
If the above waveform is not present, check the collector of A19Q1 for 300V (with respect to the test point TPG). If 300V dc is not present, suspect input rectifier A19CR1 and associated circuitry. If 300V dc is present, suspect open transistors Q1 and Q2.

Table 8-9. A19, A20, A21 Power Supply Troubleshooting (Continued)

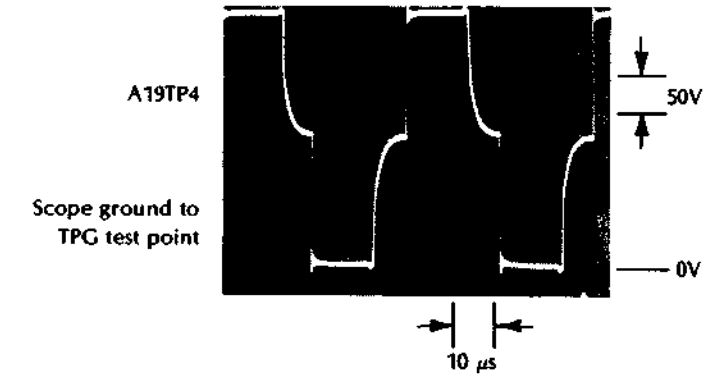
5. Fabricate the following special test extender board shown below. This board is useful because, by placing a 1 KΩ load in series with the A20T1 transformer, the current drawn from transistors A19Q1, Q2 is limited. If A19Q1, Q2 have failed because of excessive current (due to a failure in the A21 overcurrent protection circuitry), then replacing A19Q1, Q2 and using the 1 KΩ load allows the power supply to be checked out without danger to blowing A19Q1, Q2 again.

   a. Take a 22-pin extender board (such as HP P/N 05342-60034) and cut the traces on pin 8 and $\overline{8}$ as shown below.

   b. Solder a 1 KΩ, 20W resistor (HP P/N 0819-0006) above and below the cut as shown:



   c. Insert A20 (in the above extender board) into the instrument. Insert A21 (on standard HP P/N 05342-60034 extender board) into the instrument. Short A21TPJ to TPG (low right test point). Insert A19 on extender into instrument. Monitor A19TP4 with the scope probe ground on A19TPG test point (emitter of Q2). If an isolation transformer is not used, do NOT make this measurement.



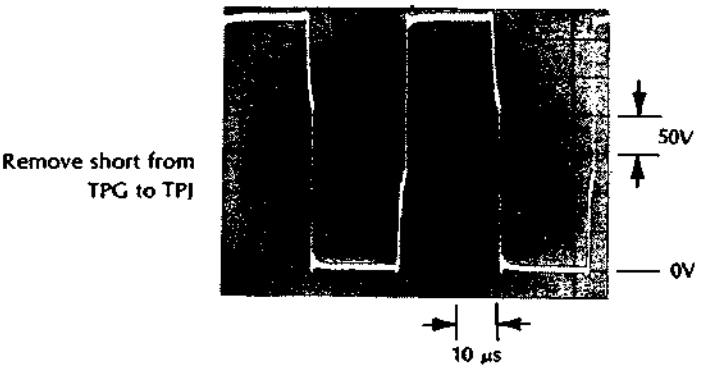
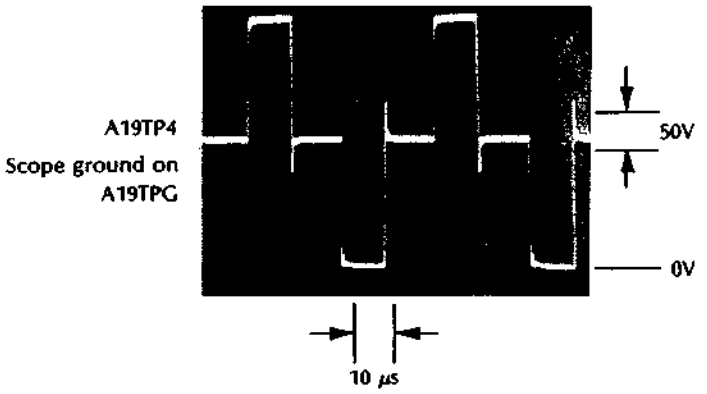


Table 8-9. A19, A20, A21 Power Supply Troubleshooting (Continued)

d. Remove special extender board and remove the short between A21TPJ and TPG. Insert A20 into XA20.



Green LED on A20 should be lit.

e. Now monitor A19TP5 and observe (adjust A19R1 for –1V on trailing edge):

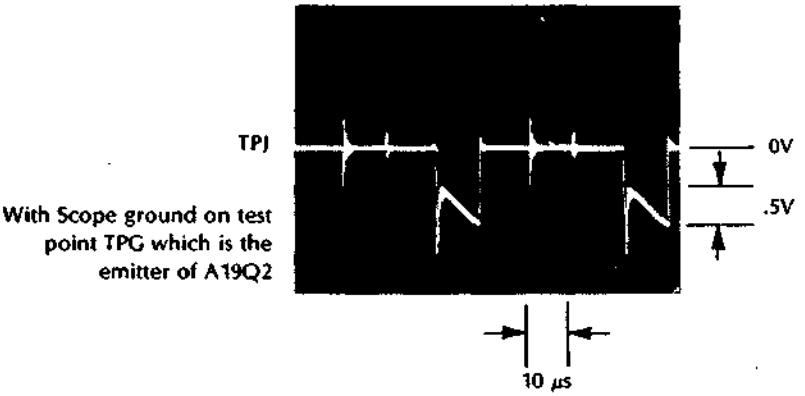
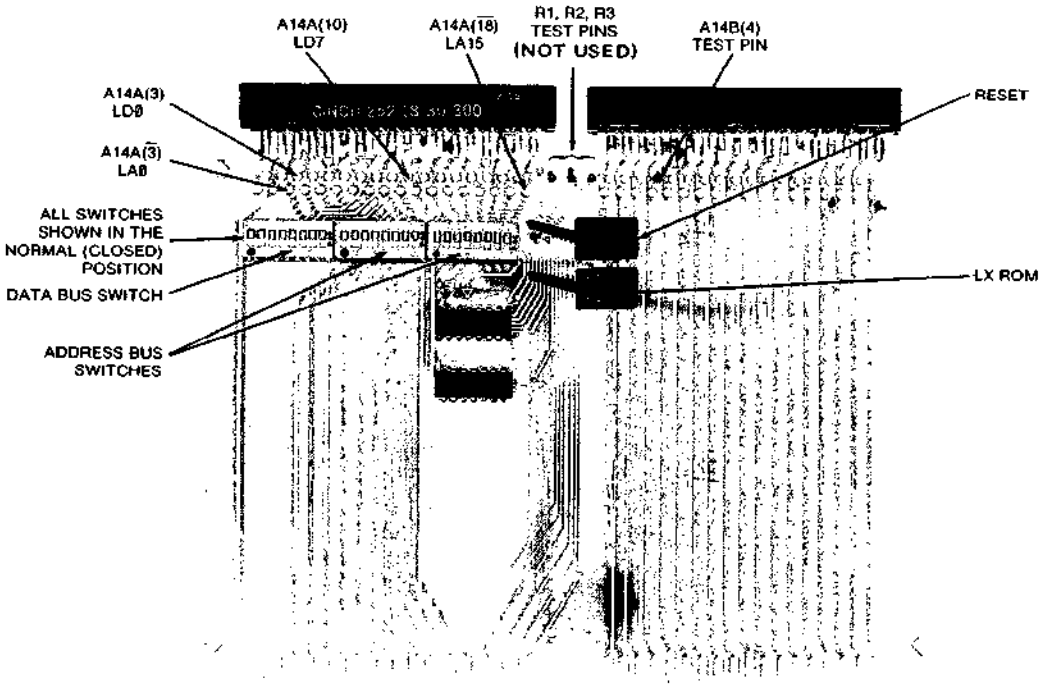


Table 8-10. A14 Microprocessor Troubleshooting

1. Place the A14 Microprocessor Assembly on the extender board (P/N 05342-60036) shown below. Place the 5004A START and STOP probes on the B(4) test pin of the A14 extender board. (Or, place AP clip on U7 of A14 and place the START probe and the STOP probe of a 5004A Signature Analyzer on A14U7(6), which is the most significant address line out of the U10 Microprocessor (A15). Place the CLOCK probe of the 5004A on the $\overline{VMA \bullet \phi 2}$ test point located in the upper lefthand corner of A14. Place the GROUND probe on the 5004A on the ground test point of A14.



2. Set the 5004A for positive slope on START, STOP, and CLOCK (all pushbuttons of the 5004A should be out). Apply power to the 5343A.
3. Place the 5343A in freerun mode by connecting a jumper from ground to "LFR" test point on A14. Set all data bus switches down (opens up data bus lines back into MPU U10). Ensure that the LX ROM switch on the A14 extender board is in the up position. Press the RESET switch on the A14 extender board. The display will be blank when A14 is in freerun mode.

EXTENDER BOARD DATA BUS SWITCH

TABLE 8-10
A14

Table 8-10. A14 Microprocessor Troubleshooting (Continued)

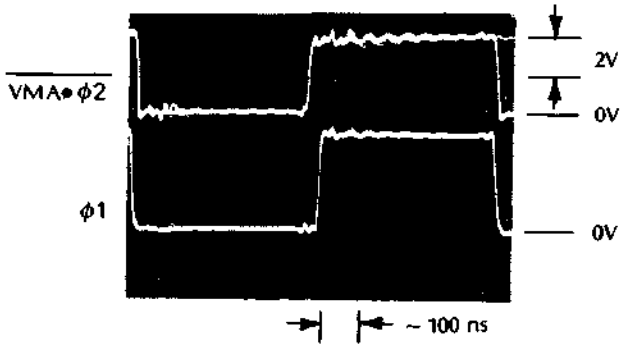
4. Place the 5004A data probe on +5V and verify that the characteristic "1's" signature displayed on the 5004A is 0003. If 003 is not displayed, then the U10 Microprocessor is not freerunning. If 0003 is displayed when the 5004A data probe is placed on +5V, go to step 5.

   a. Check the clock inputs to the microprocessor by looking at the $\phi 2$ (phase 2) clock test point on A14 and the $\overline{VMA \bullet \phi 2}$ test point. These signals should be as in the following oscilloscope photos. If these signals are not present, troubleshoot the clock generation circuitry U12, U15, U18, U19, U23, etc., on A14.

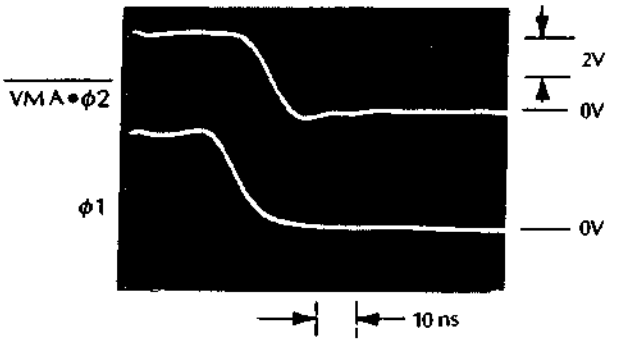
   b. If these signals are present, check diodes CR1 and CR2. If these parts are good, then the U10 is suspect.

   c. With the jumper connected for freerun, check for correct inputs, as listed below:

$\overline{RESET}$ U10(40) — High, $\overline{NMI}$ U10(6) — High, $\overline{HALT}$ U10(2) — High, $\overline{IRQ}$ U10(4) — High, 3-State Control U10(39) — Low



*Time base of scope out of CAL in order to get one complete period in photo.



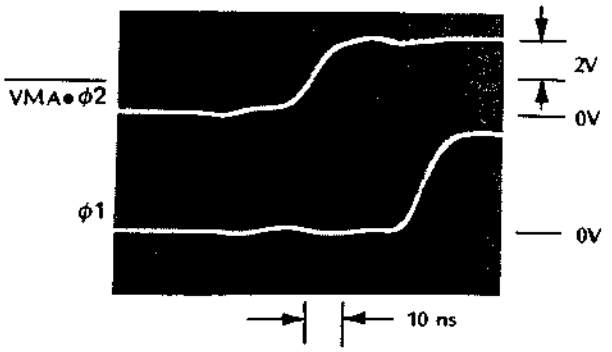


TABLE 8-10
A14

Table 8-10. A14 Microprocessor Troubleshooting (Continued)

5. Place the 5004A data probe on the following address signal points (available on the A14 extender board) and check that the proper freerun signatures are obtained as follows:

NOTE

In addition to using the 5004A Signature Analyzer, the address lines may be checked using an oscilloscope. SA is preferred, but the scope may provide useful backup. The freerun SA routine sequentially addresses the address lines in a binary format. Thus, the address line A15 is the divide-by-2 result of A14, and A14 is the divide-by-2 result of A13, etc. In other words, AØ will be toggling twice as fast as A1, A1 will be toggling twice as fast as A2, etc. The scope will verify address bus activity and quickly show a stuck line.

XA14($\overline{3}$)	UUUF	XA14A($\overline{11}$)	7792
XA14A($\overline{4}$)	FFFU	XA14A($\overline{12}$)	6322
XA14A($\overline{5}$)	8487	XA14A($\overline{13}$)	37C6
XA14A($\overline{6}$)	P760	XA14A($\overline{14}$)	6U2C
XA14A($\overline{7}$)	1U5H	XA14A($\overline{15}$)	4FC9
XA14A($\overline{8}$)	0355	XA14A($\overline{16}$)	486C
XA14A($\overline{9}$)	U75A	XA14A($\overline{17}$)	9UP2
XA14A($\overline{10}$)	6F99	XA14A($\overline{18}$)	0001

If the above signatures are obtained, go to step 6.

a. Check the signatures on the MPU side of buffer/drivers U6 and U7 as listed below. Correct or incorrect signatures should isolate the problem to either U10 or one or more of the buffer/divers U6 or U7.

ADDRESS LINE	IC PINS	(SAME AS)	SIGNATURE
AØ	U6(2)	Same as U10(9)	UUUU
A1	U7(2)	U10(10)	FFFF
A2	U6(17)	U10(11)	8484
A3	U7(17)	U10(12)	P763
A4	U7(4)	U10(13)	1U5P
A5	U6(4)	U10(14)	0356
A6	U7(15)	U10(15)	U759
A7	U6(6)	U10(16)	6F9A
A8	U7(8)	U10(17)	7791
A9	U6(15)	U10(18)	6321
A10	U6(13)	U10(19)	37C5
A11	U6(11)	U10(20)	6U28
A12	U7(11)	U19(22)	4FCA
A13	U6(8)	U10(23)	4868
A14	U7(13)	U10(24)	9UP1
A15	U7(6)	Same as U10(25)	0002

b. A signature may be incorrect because that particular address line is being held low or high by another assembly which is connected to the address bus. To check this possibility, isolate the A14 address bus from the other assemblies by setting the address bus switches on the A14 extender board all open (Low).

TABLE 8-10 A14

Table 8-10. A14 Microprocessor Troubleshooting (Continued)

6. Place the 5004A data probe on the following device select codes and check that the proper freerun signatures are obtained:

DEVICE SELECT CODE	LOCATION IC	P1	SIGNATURE
HDSPWRT	U23(3)	B(10)	U05H
LKBRD	U17(7)	B(9)	FF48
LTIMRD	U17(9)	B($\overline{6}$)	7311
LTIMWRT	U17(10)	B($\overline{7}$)	9FF7
LCTRWRT	U17(11)	B(3)	A732
LPDRD	U17(12)	B($\overline{9}$)	A9FU
LPDWRT	U17(13)	B($\overline{10}$)	6A70
LSYNHI	U17(14)	B($\overline{11}$)	1A9U
LSYNLO	U17(15)	B($\overline{12}$)	46A4
LCTRRD	U25(8)	B(2)	94F1
LHPIB	U21(7)	B($\overline{14}$)	CC1A
LSWP	U21(6)	B($\overline{13}$)	1P2A

If these signatures are correct, go to step 7.

a. If the signatures are not correct, check the inputs to the IC's with the incorrect signatures. If the inputs are not correct, troubleshoot backwards along the signal flow, from output to input, until a device is found where the input exhibits a correct signature but the output is incorrect. The correct signatures are shown adjacent to the A14 schematic diagram. Change that IC.

b. If the inputs to U23, U25, U17, or U21 have good signatures, then either the IC is bad or the output line is being held high or low by some other assembly connected to that signal. To check this possibility, A14 must be isolated from the rest of the instrument. Perform as follows:

(1) Remove A14 assembly and place it near lefthand side of instrument.

(2) Connect a clip lead from the +5V test pin on A17 to the +5V test pin on A14.

(3) Connect a clip lead from the ground test pin on A17 to ground test pin on A14.

(4) Connect an AP clip to A14U7. Place the 5004A START and STOP inputs on A14U7(6). 5004A pushbuttoms are left in the out position.

(5) Connect the 5004A CLOCK to $\overline{VMA \cdot \phi 2}$ test pin on A14 and connect GROUND to A14 ground test pin.

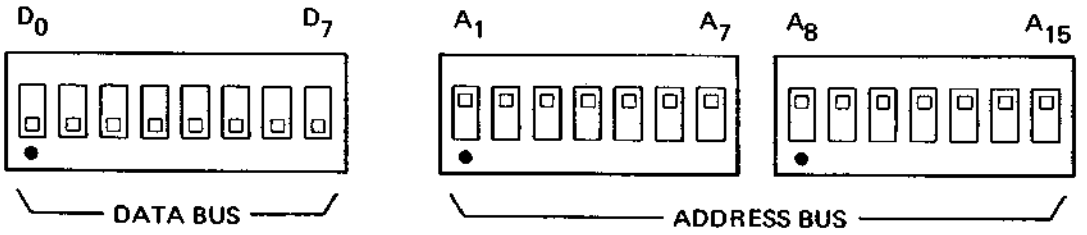
(6) Place the A14 board in freerun as in step 3. (Jumper from ground to "LFR" test point.)

(7) Measure the signatures again. If the A14 signatures are now good, then there is an assembly common to that signal which has a faulty input/output buffer. To detect which assembly that is, put A14 back in the instrument and pull assemblies which are connected to the failed A14 signal output, one at a time, until a good signature is obtained.

Table 8-10. A14 Microprocessor Troubleshooting (Continued)

7. To check the Data Bus Transceiver U5, perform the following steps:

   a. Disconnect the data bus from the A14 board by setting the extender board data bus DIP switches in the down position as shown below:



   b. Remove U10 from its socket. U5 is now isolated from the instrument and from the A14 board.

   c. Connect an AP clip to U5. Attach a clip lead from U5(19) to ground. This will enable U5.

   d. When U5(1) is TTL Low, it will pass data from the instrument data bus to the A14 board. When U5(1) is TTL High. it will pass data from the A14 board to the instrument data bus. With the 10526T Logic Pulser and 10525T Logic Probe, test U5 in each direction, as follows:

      (1) Connect the logic probe and pulser's BNC leads together with a BNC tee. Using a BNC-to-alligator clip adapter, apply 5V to the probes using the 5 volt test point on the A14 board. Connect the ground lead to the chassis.

      (2) With no other clip leads attached (except the chip enable lead at U5(19) to ground), U5(1) is held Low by buffer U15(7). Buffer input U15(6) is floating high because microprocessor U10 is removed from its socket. With this set-up, U5 may be checked in the direction data bus to A14.

PULSED PIN	OBSERVED OUTPUT PIN
U5(15)	U5(5)
U5(16)	U5(4)
U5(17)	U5(3)
U5(18)	U5(2)
U5(11)	U5(9)
U5(12)	U5(8)
U5(13)	U5(7)
U5(14)	U5(6)

      (3) To test the opposite direction, apply another AP clip to U15. Connect a clip lead from U15(6) to ground. Leave all other leads in place. Now, U5 is set up to read data from A14 to data bus.

PULSED PIN	OBSERVED OUTPUT PIN
U5(5)	U5(15)
U5(4)	U5(16)
U5(3)	U5(17)
U5(2)	U5(18)
U5(9)	U5(11)
U5(8)	U5(12)
U5(7)	U5(13)
U5(6)	U5(14)

      If the trouble still persists, replace U10. U10 may freerun and still not operate properly.

TABLE 8-10 A14

Table 8-11. A16 Memory and Sweeper Control Troubleshooting

ROM CHECK

1. To check the ROMs on this board, perform the following steps:
   a. Place A14 board on extender board, 05342-60036. All DIP switches should be in the "on", or up position.
   b. Place A14 board in freerun mode by connecting a jumper from LFR test point to ground.
   c. Connect and set 5004A as follows:
      (1) Clock to "Ø2" point.
      (2) START and STOP leads to R6K test point for first ROM U6; to R7K test point for second ROM U9.
      (3) Ground lead to ground test point.
      (4) Set START pushbutton for negative going edge (IN on 5004A).
      (5) Set STOP pushbutton for positive going edge (OUT on 5004A).
      (6) Set CLOCK pushbutton for negative going edge (IN on 5004A).
   d. Probe the points shown in the following table and observe the signature shown. If observed signatures don't match those shown in the tables, replace the faulty ROM on the A16 board.

FOR R6K ROM: U6		FOR R7K ROM: U9	
PROBE A14 LINES	SIGNATURE	PROBE A14 LINES	SIGNATURE
A3	768A	A3	418H
A4	4815	A4	1778
A5	3C40	A5	8F17
A6	0679	A6	4UUA
A7	3P62	A7	C7U9
A8	3F93	A8	P4A0
A9	H4H1	A9	A78H
A10	HP3F	A10	80HP

NOTE
The address lines are probed on the A14 board due to easier access.

   e. RAMs U11 and U14 are tested at power-up. If display is filled with "E's" (for error), either RAM U11 or U14 is faulty. Replacement of both IC's is the approved procedure in this case.
   f. In summary, if the microprocessor will freerun and if the microprocessor and ROM signatures are correct then the microprocessor and memory is ok.

SWEEP INTERFACE CHECK

1. Signature analysis can be used to troubleshoot the majority of the sweeper interface circuitry (U7, U10, U5, U17, U3, U8, U12, U13, and U15) as follows:
   a. Place A16 board on extender cards.
   b. Put A14 Microprocessor board in freerun by connecting a jumper between LRF test point and ground. Display should blank.
   c. Connect 5004A as follows:
      (1) Put AP clip on U12 of A16 board. Connect START and STOP leads to pin 6 of this IC. Set 5004A for negative slope on both START and STOP.
      (2) Connect CLOCK lead to "Ø2" test point on A14 board. Set 5004A for negative slope.
      (3) Signature 0003.
   d. Signature trace through the circuitry, verifying the signatures shown in the following table. Replace the faulty IC(s).

Table 8-11. A16 Memory and Sweeper Control Troubleshooting (Continued)

PIN	U7	U10	U12	U13	U17
1	4FC9*	26UU*	6U2C*	0003	UUUF*
2	486C*	0003	3716*	0003	FFFU*
3	9UP2*	26UU*	4FC9*	26UU*	8487*
4	0000	1ACA*	486C*	147P*	1P2A*
5	0000	0003	9UP2*	1ACA*	0000*
6	0003	1ACA*	0001*	C7HA*	0003
7	H21U*	0000	0000	0000	5F0C*
8	0000	C7HA*	72HA*	UC6H*	0000
9	3714*	0003	0003*	0003	H701*
10	3H02*	C7HA*	0003*	0003	C5F3*
11	47PC*	147P*	6322*	648U*	AH73*
12	C7HA*	0003	7792*	0003	AC5U*
13	1ACA*	147P*	0003*	0003	6AH4*
14	147P*	0003	0003	0003	5AC6*
15	26UU*				16AP*
16	0003				0003

PIN	U15	U5	U3	U8
1	72HA*	9UP1*	0003*	6U2C*
2	72HA*	9UP2*	0003	4FC9*
3	72HA*	0003	0000*	486C*
4	0003*	0000	0003	0003
5	UC6H*	0000	0000	0000
6	UC6P*	0003	0003	9UP1*
7	0000	0000	0000	0003
8	648U*	0000	0000	0000
9	6F9A*	0003	0003	0003
10	72H9*	9UP1	0003	0003
11	0003	9UP2	6F9A	0003
12	0003	0003	6F99	0003
13	0000	0000	6F99	0003
14	0003	0003	0003	0003
15				0003
16				0003

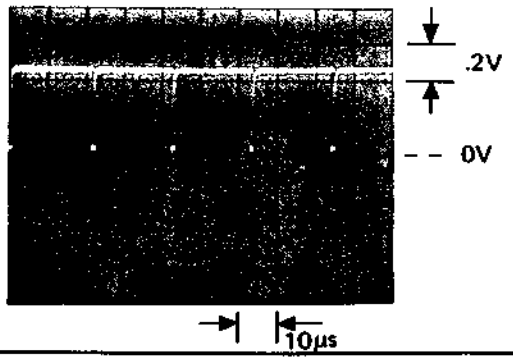
NOTE: *Indicates probe blinks

2. The remainder of the sweep interface circuits (U16 and U18) can be troubleshot in the conventional manner using an oscilloscope and/or the logic pulser and logic probe. Proceed as follows:

   a. Remove all jumpers and SA leads from all boards.

   b. Place 5343A in sweep mode. Observe slow blinking SWP M indicator.

   c. Check U17(7) for a negative true TTL level pulse train as shown below: This signal is the 3-state enable signal for U18.



U17, Pin 7

TABLE 8-11 A16

Table 8-11. A16 Memory and Sweeper Control Troubleshooting (Continued)

d. Place jumper between SWPA (T) test point and adjacent ground point. SWPM lamp should light steadily and counter should gate. This jumper simulates the Sweep Trigger signal.

e. Check the outputs of U17, U16, and U18 with an oscilloscope as follows:

(1) U17(7) waveform as in step 2c above.

(2) U16(9) for TTL Low with jumper in place, TTL High with jumper removed. This is the Sweep Lock signal that the 5343A outputs.

f. These ICs may also be checked by first removing the A14 board from the instrument. This disables the bus. Then, use the logic pulser and probe to test U16 and U18 input-to-output.

g. To test U2, proceed as follows:

(1) Remove A14 from the instrument to disable the bus. When this is done, the read/write line will be low.

(2) Attach AP clip to U15. Using jumper, connect U15(6) to ground.

(3) Using the logic pulser and probe, check the following:

PULSE	PROBE	
11	9	(This is the Write direction,
12	8	or instrument-to-A16 board.)
13	7	
14	6	
15	5	
16	4	
17	3	
18	2	

h. To check the read direction, or A16 board-to-instrument direction, proceed as follows:

(1) In addition to same setup as above, attach jumper from U15(12) to ground. This will put U2 in the Read direction.

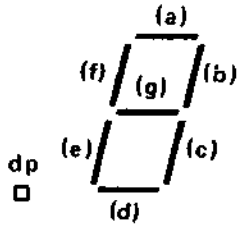
(2) Using the logic pulser and probe, check the following:

PULSE	PROBE
9	11
8	12
7	13
6	14
5	15
4	16
3	17
2	18

Table 8-12. A1, A2 Keyboard/Display Troubleshooting

1. First verify that HDSPWRT at XA14B(10) pulses high when power is applied to the 5343A by using a logic probe such as the 545A. If not, troubleshoot A14 to obtain an HDSPWRT signal.
2. If HDSPWRT is present on the power-up and pulses consistently thereafter but the display/keyboard still does not operate properly, remove the A1, A2, and front panel assembly as follows:
   a. Remove front panel SAMPLE RATE knob using Allen wrench.
   b. Remove BNC connector nut.
   c. Unplug coax cables and other leads going to A1 and A2 assemblies.
   d. At right side of front panel, loosen two screws holding U1 Sampler, A26 Sampler Driver, and A28 Preamp.
   e. Remove 4 screws (two each side) holding front panel to side rails. Pull front frame out to gain access to parts.
   f. Loosen SMA fitting at input to Sampler U1.
   g. If DAC option is installed, pull + and –15V leads at top left corner of A2. (RED is +15V, VIOLET is –15V.) Temporarily pull ribbon cable loose at A2J1.
   h. Lay front frame on its face. Remove 4 screws holding A1/A2 to front frame. Pull out the A1/A2 assemblies.
   i. Replace ribbon cable into A2 for troubleshooting.
3. Remove A14 from the 5343A chassis. With a clip lead, ground the following pins and observe the display for the following lighted LED segments:
   a.
A2U1(3)	all (b) segments and # indicator should light
A2U1(6)	all decimal points, blue key, and TALK indicator should light
A2U1(8)	all (d) segments, REM light, and MAN (MHz) key should light
A2U1(11)	all (c) segments, GATE light, and OFS MHz key should light

   b.
A1U6(3)	all (g) segments, RECALL key, and LISTEN indicator should light
A1U6(6)	all (a) segments, # indicator, and KYBD LK key should light
A2U6(8)	all (e) segments, AUTO key, and SIGN indicator should light
A2U6(11)	all (f) segments, SET key, and SWP M key should light



   c. If all segments light as specified, then the LED's A1DS11 through DS21 and the associated transistor drivers on A1 are operating properly. In addition, the scan clock comprised of A2U4, U3, U12, U5, and the the column scanners A2U2, U8 are operating properly.
   d. If only one segment in the display lights, troubleshoot the scan clock and column scanners on A2.

TABLE 8-12
A1, A2

Table 8-12. A1, A2 Keyboard/Display Troubleshooting (Continued)

4. If the 5343A does not perform the power-up diagnostic but A1, A2 properly perform the test described in step 3, the probable cause of the failure is A2U12, U7 (TTL RAM memory), A2U17 (data bus buffer), A2U4, U14 (write enable generation), or U18 (multiplexer).

5. If the 5343A performs the power-up diagnostic but does not perform the diagnostic mode 8 keyboard check, the probable cause of the problem is the key decoding circuitry on A2 consisting of U14A, U4C, U19, and U13. To test this circuitry, perform the following tests with A14 still removed from instrument:

   a. Monitor U10(8) with a logic probe and verify that each time a key is pressed, U10(8) goes low. To cause U10(8) to return to high, ground U23(1) momentarily. This verifies that pushing a key generates an interrupt request (LIRQ) and that reading the keyboard (LKBRD) clears the interrupt request.

   b. Place AP clip on U23 and monitor the outputs of latch U23 by grounding U23(1) and verify that when a key is pressed, the latch stores the following data:

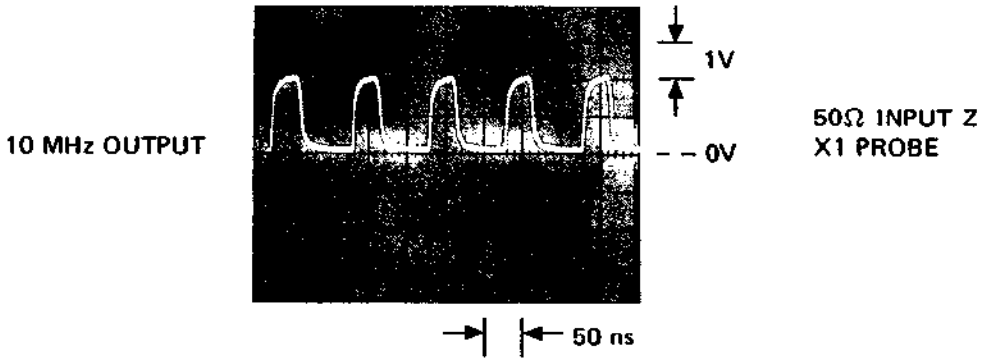
KEY	U23(3)	(4)	(5)	(6)
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
•	0	1	0	1
ENTER	1	1	0	1

   c. Monitor U13(2) and verify that when any of the leftmost grouping of keys (AUTO, MAN, RESET, etc.) is pressed, U13(2) is high and that when any of the rightmost grouping of keys (0, 1, 2, etc.) is pressed, U13(2) is low. This verifies that the top/bottom row decoder U20 is operating properly.

   d. If the A2 assembly passes all the above, then the most probably cause of the problem is the A2U13 bus driver. Another possible cause is that the A14 MPU does not respond to the LIRQ signal.

Table 8-13. A17, A18, A24 Timing Troubleshooting

1. The A24 oscillator is the source of most timing signals within the 5343A. The overall condition of this assembly and the multiplex section of A18 Time Base Buffer may be observed at J3 rear panel jack FREQ STD OUT, 10 MHz. To observe this signal, the INT-EXT switch must be in INT (internal) position. See photo below for oscilloscope view of 10 MHz output.



2. If no output is obtained from J3, check INPUT to A18 at pin $\overline{8}$. No signal here indicates failure of A24. The standard A24 assembly may be repaired if the oscillator module itself is ok. Option 001 A24 is not field repairable — it must be replaced. Option 001 A24 is available on a blue stripe replacement basis. See Section VI for information.

3. If A24 output is valid, check outputs of A18 assembly (double check INT-EXT switch position). A18 provides 3 outputs:

   a. 1 MHz to drive A17 Timing Generator (pin 1)

   b. 500 kHz to drive A7 Mixer/Search Control and A10 Divide-by-N assembly (pin 3).

   c. 10 MHz to rear panel (pin $\overline{5}$).

   The above three signals are TTL level square waves. If these signals are present, proceed to A17 Timing Generator. If these signals are not valid, troubleshoot A18 to find the stoppage in the signal path.

4. The A17 Timing Generator has a number of outputs:

   a. LO SWITCH at XA17($\overline{1}$) which switches the A5 multiplexer and A13 counters in a pseudorandom sequence after acquisition.

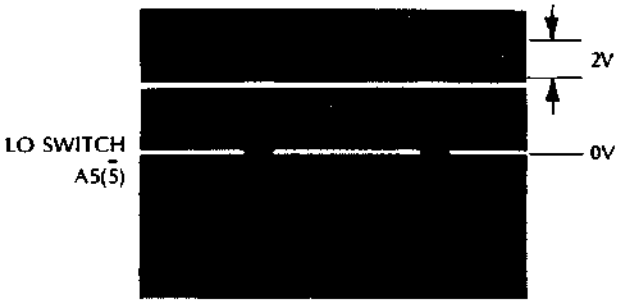
   b. LDIR GATE at XA17($\overline{4}$) which gates the main gate on A3 for direct count measurements.

   c. LIF GATE at XA17($\overline{5}$) which gates counter A on A13 for measuring the IF.

   d. When A17 is read by the microprocessor, the D4 line is examined to see if the gate time is over. The D1 line indicates the end of the prs.The D2 line indicates the end of the sample rate run down.

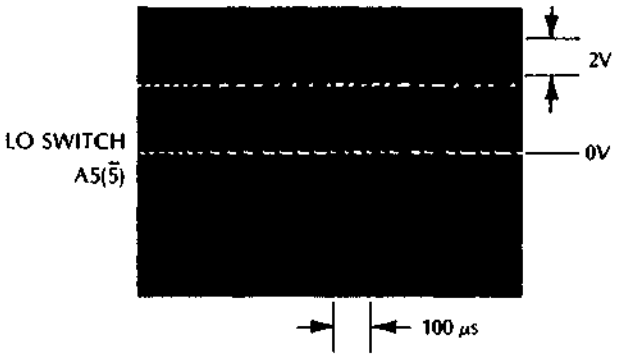
Table 8-13. A17, A18, A24 Timing Troubleshooting (Continued)

5. LO SWITCH signal verification. To verify that the LO SWITCH signal is operating properly, the 5343A must be able to acquire so that the counter can be forced into its harmonic determination routine. This means that A25A1, A28, U1, A11, and A12 must be working properly. To check LO SWITCH, apply a 50 MHz signal, -10 dBm, to the high frequency connector and put the 5343A in the 500 MHz—26.5 GHz range. The LO SWITCH signal at XA5($\overline{5}$) should appear:



The time during which the signal switches between high and low levels in a pseudorandom fashion should be 360 ms (ACQ TIME switch on rear panel in MED position). The time where the signal is high and not switching is controlled by the front panel sample rate control and resolution of counter. If the rear panel switch is placed in the SLOW position, then the time during which the signal is switching should extend to 2.1 seconds (actually 2.096). In FAST position the time should be 22.52 ms.

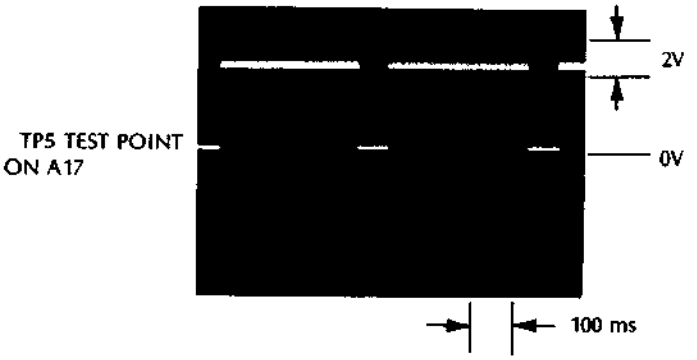
A sample of what the sequence looks like is shown below where the sweep speed of the scope has been increased to 100 μs.

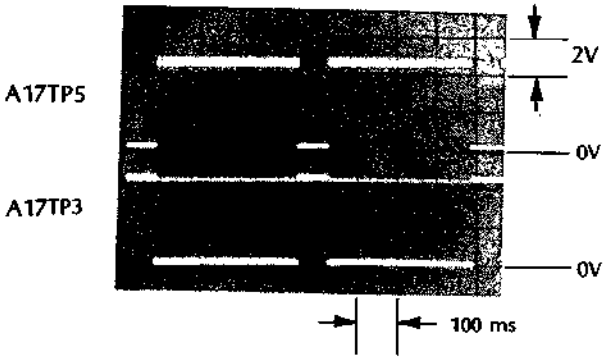


If LO SWITCH is stuck low, then the 5343A will not acquire even if all the IF circuitry is working properly. This is due to the fact that during acquisition, a 1 μs measurement is made on the IF and this requires that LO SWITCH go high to select the A counter on A13. This measurement is made to insure that the IF is in the proper frequency range. The above troubleshooting procedure will not work in this case since diagnostic mode 3 can not be entered. This condition would be evidenced by the counter displaying SP2 in diagnostic mode 0.

Table 8-13. A17, A18, A24 Timing Troubleshooting (Continued)

IF LO SWITCH is not present, check the TP5 test point on A17 to see if the prs generator is working. Put the counter in diagnostic mode 2 for continual prs generation. TP5 is high during the prs and should remain high for 360 ms (MED mode on rear panel) or for 2.096 seconds (SLOW mode) or for 22.52 ms (FAST mode).





6. Troubleshooting the A17 prs generator.

   To troubleshoot the prs generator on A17 (consisting of A17U13, U10, U5, U2, U1, and various gates), pull the A18 Time Base Buffer board from the instrument to disable the 1 MHz clock into A17. Put A17 on an extender board, connect logic probe and logic pulser power leads to A17 +5V and ground, and perform as follows:

   a. U13, U10, U5 SHIFT REGISTER CHECK

      (1) Put AP clip on U3 and connect clip lead from U3(9) to ground. Verify that U5(1) is high. Clear U13, U10, U5 by applying 1 pulse with logic pulser to TP5 test point. Monitor U5(9) with logic probe to see that the clear input pulses low (if clear input powers up low, then apply a pulse to U20(9) then to U18(2) to cause the cler input to go high).

      (2) Apply logic pulser to TP4 test point and monitor the shift register outputs:

      After 1 pulse at TP4, U5(3) should go from low to high.
      Apply 2 more pulses at TP4, U5(5) should go from low to high.
      Apply 12 more pulses at TP4, U10(12) should go from low to high.
      Apply 5 more pulses at TP4, U13(6) should go from low to high.

Table 8-13. A17, A18, A24 Timing Troubleshooting (Continued)

b. U2, U1 Counters Check

(1) Connect AP clip to U3. Connect clip lead from U3(1) to ground.

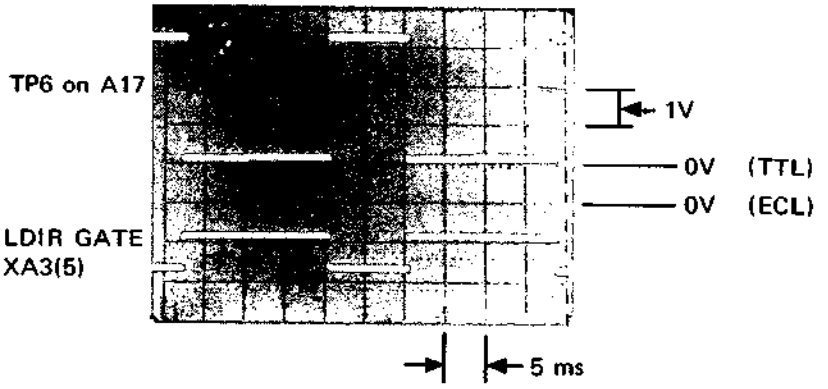
(2) Verify that U1(1) is high. If not, pulse U20(9), then U18(2) with logic pulser. Verify that U2(3) is high and U2(5) is low. If not pulse U20(9).

(3) Connect another clip lead from U3(5) to ground. Verify that U1(9) is low. Move clip lead from U3(5) to U3(6) so that U3(6) is grounded. Verify that U1(9) is high. This loads data into U1 and U2 counters.

(4) Monitor U1(5) with logic probe and pulse TP4 test point with pulser 14 times. ON 14th clock, U1(5) should pulse high.

7. A17 LDIR GATE and LIF GATE troubleshooting.

a. Set the 5343A to 10 Hz—500 MHz range, sample rate full ccw, no input signal, and 100 Hz resolution. With an oscilloscope, monitor LDIR GATE at XA3(5) and TP6 on A17 as shown below:



b. As the resolution is changed, the width of the gate signal (TP6 high) should vary as follows:

Resolution	Width
1 MHz	1 μs
100 kHz	10 μs
10 kHz	100 μs
1 kHz	1 ms
100 Hz	10 ms
10 Hz	100 ms
1 Hz	1 s

c. Change the range of the 5343A to the 500 MHz—26.5 GHz range and place the counter in MAN mode and observe:

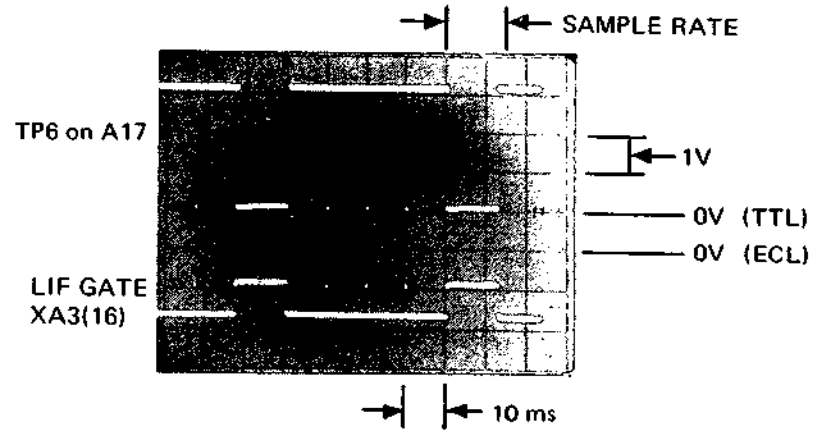


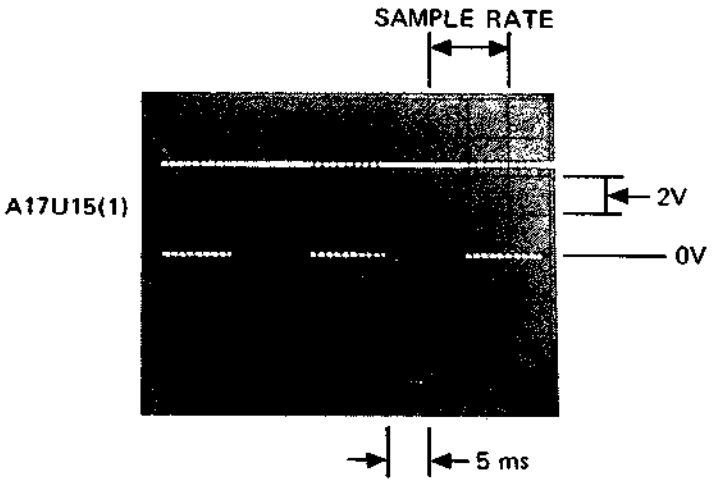
Table 8-13. A17, A18, A24 Timing Troubleshooting (Continued)

d. As the resolution is changed, the width of the gate signal should vary as follows:

RESOLUTION	WIDTH
1 MHz	10 μs
100 kHz	Four 10 μs width pulses, 100 μs between each
10 kHz	Four 100 μs width pulses, 100 μs between each
1 kHz	Four 1 ms width pulses, 100 μs between each
100 Hz	Four 10 ms width pules, 100 μs between each
10 Hz	Four 100 ms width pulses, 100 μs between each
1 Hz	1 s

Four resolutions from 100 kHz to 10 Hz, each gate time consists of four gate signals separated by 100 μs dead time.

8. IF LDIR GATE or LIF GATE signals are not present, place A17 on an extender board and monitor A17U15(1), the output of the U15 time base generator. Place the 5343A in 10 Hz—500 MHz range, sample rate full ccw, and 1 kHz resolution and observe:



Only the first period of the U15(1) output is used to generate the LDIR GATE signal as shown below:

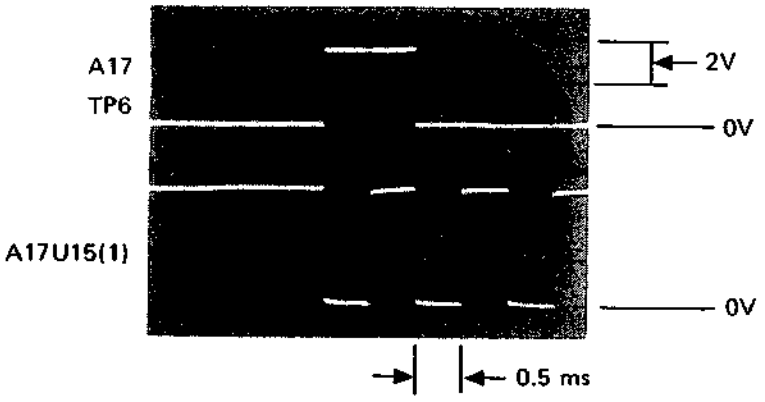


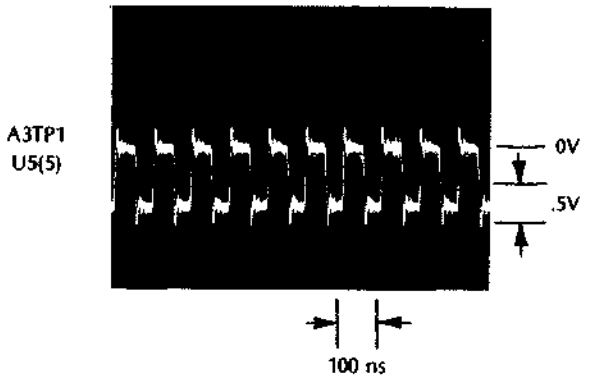
TABLE 8-13
A17, A18, A24

Table 8-14. A3 Direct Count Amplifier Troubleshooting

NOTE

The Direct Count (10 Hz—520 MHz) input is protected by a fuse installed in front panel BNC connector (see *Figure* 6-7). Check this fuse if A3 is suspected as faulty. Remove the BNC (and fuse) by using a BNC Tee and turning counterclockwise.

To check that the direct count amplifier is working, connect the 10 MHz FREQ STD rear panel output to the direct count input (front panel BNC). Place the range switch in the 10 Hz—500 MHz range and the impedance select to 50Ω. Monitor TP1 of A3 for the following waveform (TP1 is the output of Schmitt Trigger U5).



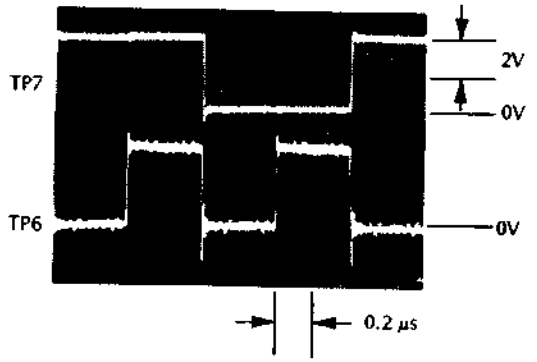
NOTE

Check that the output of A3, DIRECT B available at XA3($\overline{1}$), is divided by four and that DIRECT A available at XA3(2) is divided by two.

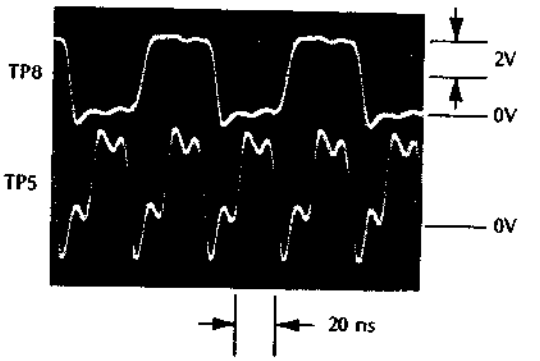
Table 8-15. A13 Counter Troubleshooting

1. Apply a 50 MHz signal at -10 dBm to the high frequency input of the 5343A. Put the counter in diagnostic mode 2 (press SET, SET, 2) to read the contents of the A counter. The A counter should read approximately 8,200,000. Put the 5343A in diagnostic mode 3 to read the B counter. It should be the **same** reading as A, ±1 count (provided the stability of the 50 MHz source is that good). If this is true, then A13 is good. If it is not true, A13 may be a fault (as well as A17 for the prs generation and gate time generation).

2. Check the inputs to the A counter as follows: Apply 10 MHz FREQ STD OUT on rear panel to the direct count input (front panel BNC) with 50Ω position selected. Check the following A counter test points (since 10 MHz is divided by four on A3, TP6 which divides A3 output by 2, should have a period of 8×100 ns = 800 ns and TP7, which divides A3 output by four should have a period of 16×100 ns = 1.6 μs):

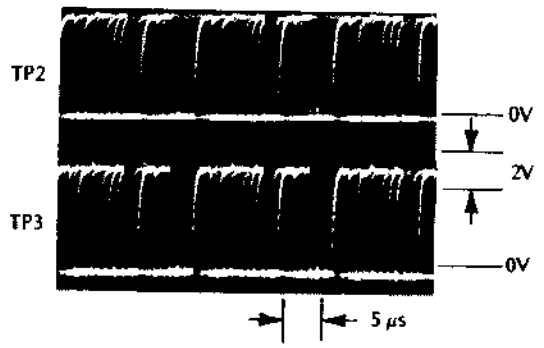


3. Check the inputs to the B counter as follows: Apply a 50 MHz, -10 dBm signal to the high frequency input and select the 500 MHz—26.5 GHz range. Put the 5343A into AUTO and push RESET to cause the counter to go to the prs generation, thus enabling the B counter. Place the rear panel FM switch to the FM position so that the B counter is enabled for 2.1 seconds.

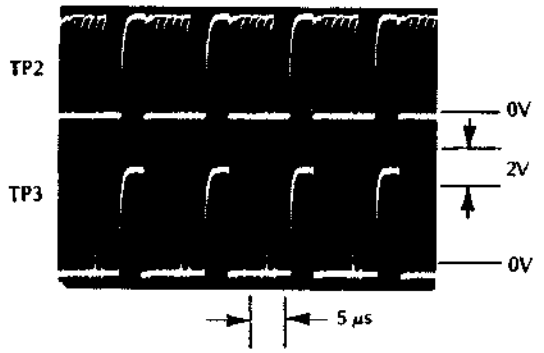


4. Test the outputs of U1 and U2 for activity by applying a 50 MHz, -10 dBm signal to the high frequency input. Place the counter in AUTO, 500 MHz—26.5 GHz range, and diagnostic mode 2 so that the prs is continually generated. Monitor TP2 and TP3 with an oscilloscope. If the signals appear much different than the waveform shown below, one or more of the U3 buffers have probably failed. Use a logic pulser and logic probe to check out the U3, U7 buffers. An HP 1607A Logic State Analyzer may be used to check out the actual data going back to the microprocessor as shown in step 5.

Table 8-15. A13 Counter Troubleshooting (Continued)



When the counter is not in diagnostic mode 2 but is just measuring the 50 MHz signal, the waveform below shows activity at the A counter (counting the IF) but none at the B counter.



5. 1607A check out of A13:

   a. Put A13 on extender board and put AP clips on A13U3, U5, U8, and U10. Connect the following 1607 data lines as follows:

1607A DATA INPUTS	A13 CONNECTIONS	DESCRIPTION
Data bit 0	U3(8)	AØ line
Data bit 1	U3(10)	A1 line
Data bit 2	U3(12)	A2 line
Data bit 3	U5(14)	A3 line
Data bit 4	U5(2)	A4 line
Data bit 5	U8(1)	A5 line
•GND	U3(7)	GND
Data bit 6	U8(12)	LCTR RD
Data bit 7	U5(7)	DØ
DAta bit 8	U5(9)	D1
DAta bit 9	U10(7)	D2
Data bit 10	U19(9)	D3
Data bit 11	NOT USED	
•GND	U5(8)	GND
CLOCK	$\overline{VMA}$•$\phi 2$ TP on A14	
•GND	U10(8)	GND

   b. Set 1607A to repetitive, Table A, word trigger, delay off and start display. Put bits 15-7 in the OFF (don't care) position. Place the 5343A in CHECK mode and 1 MHz resolution. Select each of the following trigger words (EXAMPLES 1, 2, and 3) and verify the proper 1607A display in the don't care bits of the trigger word.

TABLE 8-15 A13

Table 8-15. A13 Counter Troubleshooting (Continued)

Example 1. CHECK Mode — 1 MHz Resolution

COMMENTS	OFF DATA BITS SHOULD BE:				TRIGGER (DATA BITS)						
	10	9	8	7	6	5	4	3	2	1	0
*These two bits ignored in CHECK since they represent state of dividers on A3. This reads out least significant counts. In this case we're reading state of divider U12B (bit 9) and divider U16B (bit 10). Count equals 3 in this case.	1	1	*	*	0	1	0	0	0	0	0
Bit 7 = U17(5) output Bit 8 = U17(9) output Bit 9 = U17(2) Bit 10 = U17(12) Count = 8 in this case.	1	0	0	0	0	1	0	1	0	0	0
Bit 7 = U13(5) output Bit 8 = U13(9) output Bit 9 = U13(2) output Bit 10 = U13(12) Count = 1 in this case.	0	0	0	1	0	1	1	0	0	0	0
Bit 7 = U1(15) 10^0 decade Bit 8 = U1(16) 10^0 decade Bit 9 = U1(1) 10^0 decade Bit 10 = U1(2) 10^0 decade Count = 0	0	0	0	0	0	1	1	1	0	0	0
Bit 7 = U1(15) 10^1 decade Bit 8 = U1(16) 10^1 decade Bit 9 = U1(1) 10^1 decade Bit 10 = U1(2) Count = 0	0	0	0	0	0	1	1	1	0	0	1
Bit 7 = U1(15) 10^2 decade Bit 8 = U1(16) 10^2 decade Bit 9 = U1(1) 10^2 decade Bit 10 = U1(2) 10^2 decade Count = 0	0	0	0	0	0	1	1	1	0	1	0
Bit 7 = U1(15) 10^3 decade Bit 8 = U1(16) 10^3 decade Bit 9 = U1(1) 10^3 decade Bit 10 = U1(2) 10^3 decade Count = 0	0	0	0	0	0	1	1	1	0	1	1
Bit 7 = U1(15) 10^4 decade Bit 8 = U1(16) 10^4 decade Bit 9 = U1(1) 10^4 decade Bit 10 = U1(2) 10^4 decade Count = 0	0	0	0	0	0	1	1	1	1	0	0
Bit 7 = U1(15) 10^5 decade Bit 8 = U1(16) 10^5 decade Bit 9 = U1(1) 10^5 decade Bit 10 = U1(2) 10^5 decade Count = 0	0	0	0	0	0	1	1	1	1	0	1

Total Count = 3+4(8+10) = 75 counts
(Count display 75 MHz)

Multiply all the counts after the 1st by 4 since the input to the decade counters has essentially been prescaled by 4.

Table 8-15. A13 Counter Troubleshooting (Continued)
Example 2. CHECK Mode — 100 Hz Resolution

COMMENTS	OFF DATA BITS SHOULD BE:				TRIGGER WORD (DATA BITS)						
	10	9	8	7	6	5	4	3	2	1	0
Count = 0	0	0	*	*	0	1	0	0	0	0	0
Count = 0	0	0	0	0	0	1	0	1	0	0	0
Count = 0	0	0	0	0	0	1	1	0	0	0	0
Count = 5	0	1	0	1	0	1	1	1	0	0	0
Count = 7	0	1	1	1	0	1	1	1	0	0	1
Count = 8	1	0	0	0	0	1	1	1	0	1	0
Count = 1	0	0	0	1	0	1	1	1	0	1	1
Count = 0	0	0	0	0	0	1	1	1	1	0	0
Count = 0	0	0	0	0	0	1	1	1	1	0	1

Total Count = 4(187500) +0 = 750,000 = Display of 75.0000 MHz

Example 3. Apply 10 MHz from EXT FREQ STD OUT to 10 Hz—500 MHz Input and Select the Direct Count Range with 1 Hz Resolution

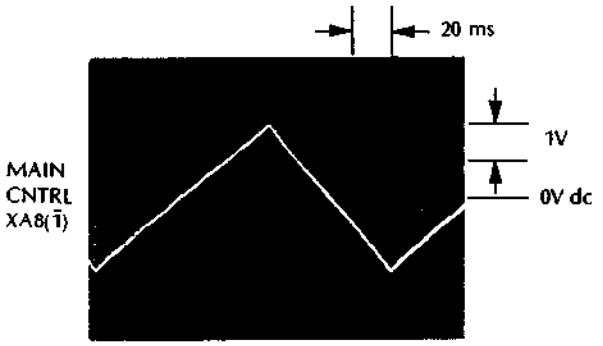
COMMENTS	OFF DATA BITS SHOULD BE:				TRIGGER WORD (DATA BITS)						
	10	9	8	7	6	5	4	3	2	1	0
Count = 0	0	0	0	0	0	1	0	0	0	0	0
Count = 0	0	0	0	0	0	1	0	1	0	0	0
Count = 0	0	0	0	0	0	1	1	0	0	0	0
Count = 0	0	0	0	0	0	1	1	1	0	0	0
Count = 5	0	1	0	1	0	1	1	1	0	0	1
Count = 2	0	0	1	0	0	1	1	1	0	1	0
Count = 6	0	1	1	0	0	1	1	1	0	1	1
Count = 0	0	0	0	0	0	1	1	1	1	0	0
Count = 0	0	0	0	0	0	1	1	1	1	0	1

In the direct count mode, because of the divide-by-4 on A3, the output of the decade dividers must be multiplied by 16 instead of 4. So total count is 16(625,000) +0 = 10,000,000 and is displayed as 10.000000 MHz.

To check the B counter, the same set-up may be used but Bit 5 in the Trigger word must be a zero. Put the counter in diagnostic mode 3 with a 50 MHz, -10 dBm signal applied to the high frequency input. Observe that a reading of around 8,200,000 is output for 1 Hz resolution.

Table 8-16. A8, A9, A10 Main Loop Synthesizer Troubleshooting

1. To test if the A9 Main Loop Amplifier and A10 Divide-by-N are operating properly, put the 5343A in AUTO and select the 500 MHz—26.5 GHz range. Disconnect any input signal. In diagnostic mode 0 (press SET, SET, 0), the counter should display SP, indicating that it is sweeping the synthesizers. The MAIN CNTRL signal, measured at XA9($\overline{1}$), should look like:



The sweep up time is approximately 90 ms while the sweep down time is 60 ms. If this signal is present, then A9, A10, and part of A8 as well as the ROM program on A14, are operating properly.

2. To test if the A8 Main VCO is operating properly, put the 5343A in MANUAL mode, 500 MHz—26.5 GHz range and set the MANUAL center frequency to the values in the following table. Connect a coax cable, with BNC connector on one end and alligator clips on the other, from XA5($\overline{10}$) to the 50Ω Channel A input of the 5345A Electronic Counter. The 5345A counter will measure the MAIN OSC signal at XA5($\overline{10}$). Verify the 5345A measurement indicates the correct MAIN OSC frequency for each of the MANUAL center frequencies selected.

MAN CENTER FREQ	MAIN OSC FREQ
500 MHz	300.0 MHz
550 MHz	312.5 MHz
600 MHz	337.5 MHz
650 MHz	350.0 MHz

Also test the output level of the A8 outputs. Using an RF Millivoltmeter with a high Z probe, the following A8 output levels should be measured (±100 mV):

XA8(7)	MAIN OSC	500 mV rms
XA8(3)	MAIN VCO	250 mV rms
XA8($\overline{5}$)	DIV N	250 mV rms

These levels are essentially independent of frequency.

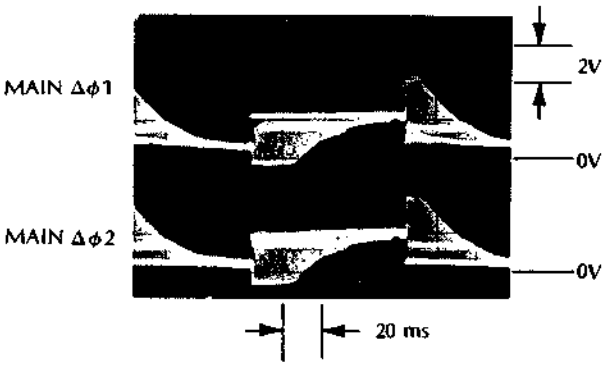
If steps 1 and 2 pass the test, then the Main Loop Synthesizer is working properly. If not, proceed to step 3.

3. A8 FREERUN FREQUENCY CHECK. Connect XA5($\overline{10}$), the MAIN OSC signal, to the direct count input (front panel BNC), of the 5343A. Use a coax cable, BNC on one end and alligator clips on the other. With a jumper, short MAIN CNTRL, A9TP1, to ground. The 5343A should read approximately 325 MHz (±2 MHz). If not, adjust A8R22. If no signal is present, repair A8. (Test all of the A8 outputs for a signal.)

Table 8-16. A8, A9, A10 Main Loop Synthesizer Troubleshooting (Continued)

4. Troubleshooting A9 and A10.

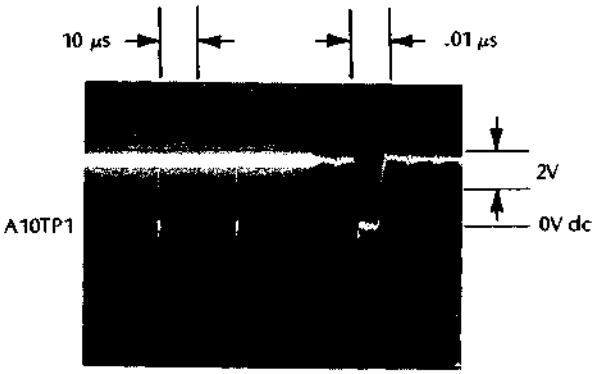
   Put A10 on an extender board and put an AP clip on A10U2. Connect scopes probes to U2(5) which is MAIN $\Delta\phi_1$ and U2(10) which is MAIN $\Delta\phi_2$. Ground TP1 on A9 with a clip lead. This causes the A8 VCO to go to its freerun frequency of 325 MHz. Put the 5343A in AUTO, 500 MHz—26.5 GHz range, and no input. This causes the 5343A to sweep the synthesizers. Verify that the U2 phase detector outputs appear as follows:



   If these signals are not present, then either the divide-by-N or the phase detector on A10 is faulty. If this signal is present but there is no MAIN CNTRL sweep signal at XA8($\overline{1}$) as in step 1, then A9 is faulty.

5. The following test determines if the divide-by-N is faulty:

   With the Main Synthesizer Loop working properly, the signal at A10TP1 is a 50 kHz signal as shown:



MIXED SCOPE DISPLAY

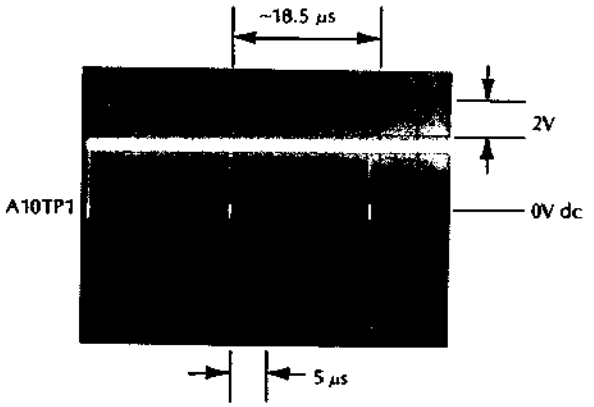
Table 8-16. A8, A9, A10 Main Loop Synthesizer Troubleshooting (Continued)

TABLE 8-16
A8, A9, A10

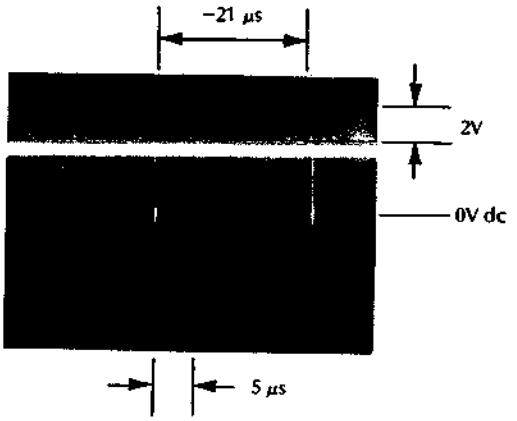
Ground A9TP1 so that A8 will go to its freerun frequency of 325 MHz. Put the 5343A in MANUAL mode and set the following center frequencies. Monitor A10TP1 and check the period of this signal. It should vary per the table below since the 325 MHz freerun frequency is divided by the programmed N.

MAN CNTRL FREQ	DESIRED VCO FREQ (frequency A8 would go to if A9TP1 not grounded)	DIVISION FACTOR N	A10TP1 PERIOD (if freerun = 325.0 MHz)
500 MHz	300.0 MHz	6000	18.46 μs
550 MHz	312.5 MHz	6250	19.23 μs
600 MHz	337.5 MHz	6750	20.77 μs
650 MHz	350.0 MHz	7000	21.54 μs

For example:



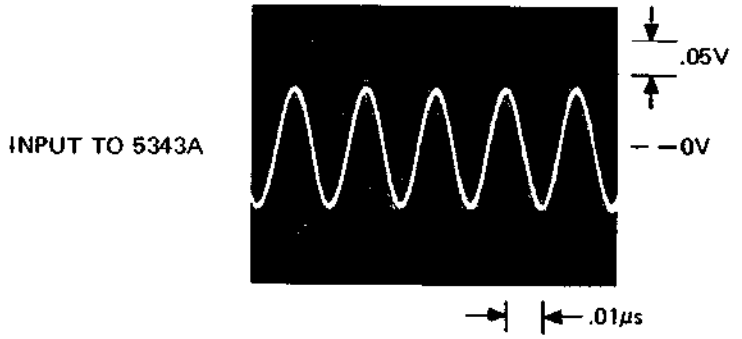
If the MAN CNTRL FREQ is changed to 600 MHz, then the period of A10TP1 changes:



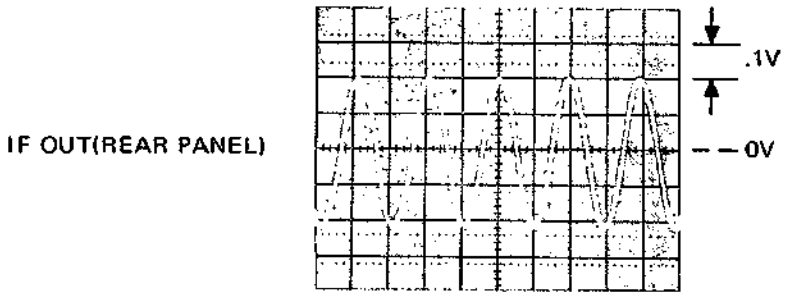
If this doesn't occur, then the divide-by-N circuitry on A10 is faulty.

Table 8-17. A11, A12, A25, A28 U1 IF Troubleshooting

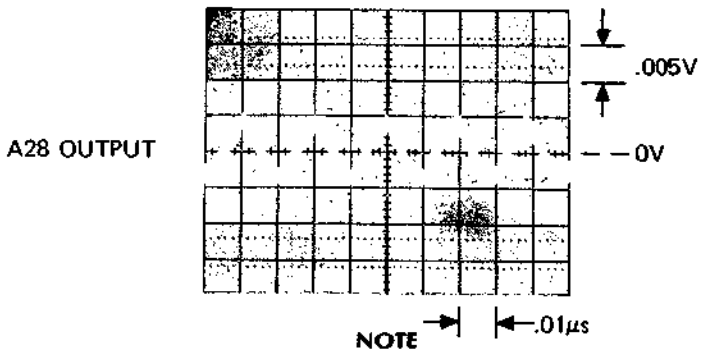
1. Set-up signal generator at 50 MHz to deliver -10 dBm (70 mV rms, 170 mV p-p) into 50Ω measured on an oscilloscope with 100 MHz bandwidth.



2. Apply the 50 MHz signal generator output to the 500 MHz—26.5 GHz input of the 5343A. Place the 5343A in AUTO and the range switch in the 500 MHz—26.5 GHz position.
   The IF OUT on the rear panel of the 5343A should appear as follows:



3. If this output is as shown above, go to step 7.
   a. If this output is not present, then either the U1 Sampler, the A28, or the A25A1 amplifier has failed. To determine which has failed, proceed as follows:
      (1) Disconnect the A28 assembly from the A25 IF Amp motherboard by removing the coax cable between the two assemblies.
      (2) Using a scope probe (scope set for 50Ω input impedance), check for presence of a signal a A28 output jack.



NOTE

Do not be concerned that the signal level shown above is less than that shown as the test signal input in step 1. Sampler U1 has about 40 dB of conversion loss while preamplifier A28 has about 22dB gain. The sampler conversion loss accounts for the signal level loss.

(a) If a signal is present as shown, A28 and Sampler U1 are probably good. Proceed to A25A1checks.

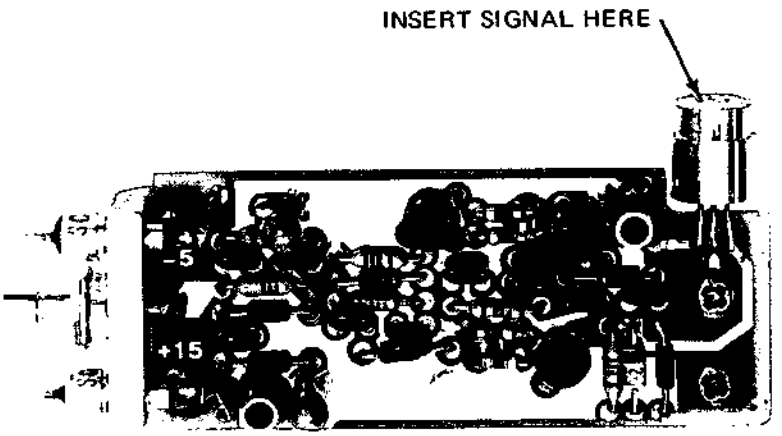
(b) If no signal is present at this point, check A28, then Sampler U1.

Table 8-17. A11, A12, A25, A28 U1 IF Troubleshooting (Continued)

4. A28 Checks:

   a. To gain access to A28, remove the two screws that go through the assembly to remove the cover. Separate A28 from Sampler U1 by *CAREFULLY* pulling the two apart.

   Inject a 50 MHz signal into A28, using a coupling capacitor of 20 to 50 pF. Apply a signal level of –20 dBm (22 mV into 50Ω) to the pin shown below. (A coupling capacitor is necessary because this pin is at –5V; some sources cannot withstand any dc on the output.)



NOTE

Insure that the A28 assembly stays grounded to the chassis for power supply return. HINT! Without the cover in place, put one screw back into the circuit board and through the bottom housing. Retain with a nut. The bottom housing will protect A28 and prevent short circuits. If proper grounding is not observed, A28 may oscillate giving faulty troubleshooting information.

   c. Using a 100 MHz bandwidth oscilloscope, check the output of A28 for a signal per photo in step 2 (IF OUT). If no signal is present, signal trace A28 to find the faulty component(s).

   d. If a signal is present, proceed to check the A26 Sampler Driver, *Table 8-20.*

5. A25A1 Checks:

   a. Place A25A1 on an extender board.

   b. Inject a test signal into A18 as described in step 4b above.

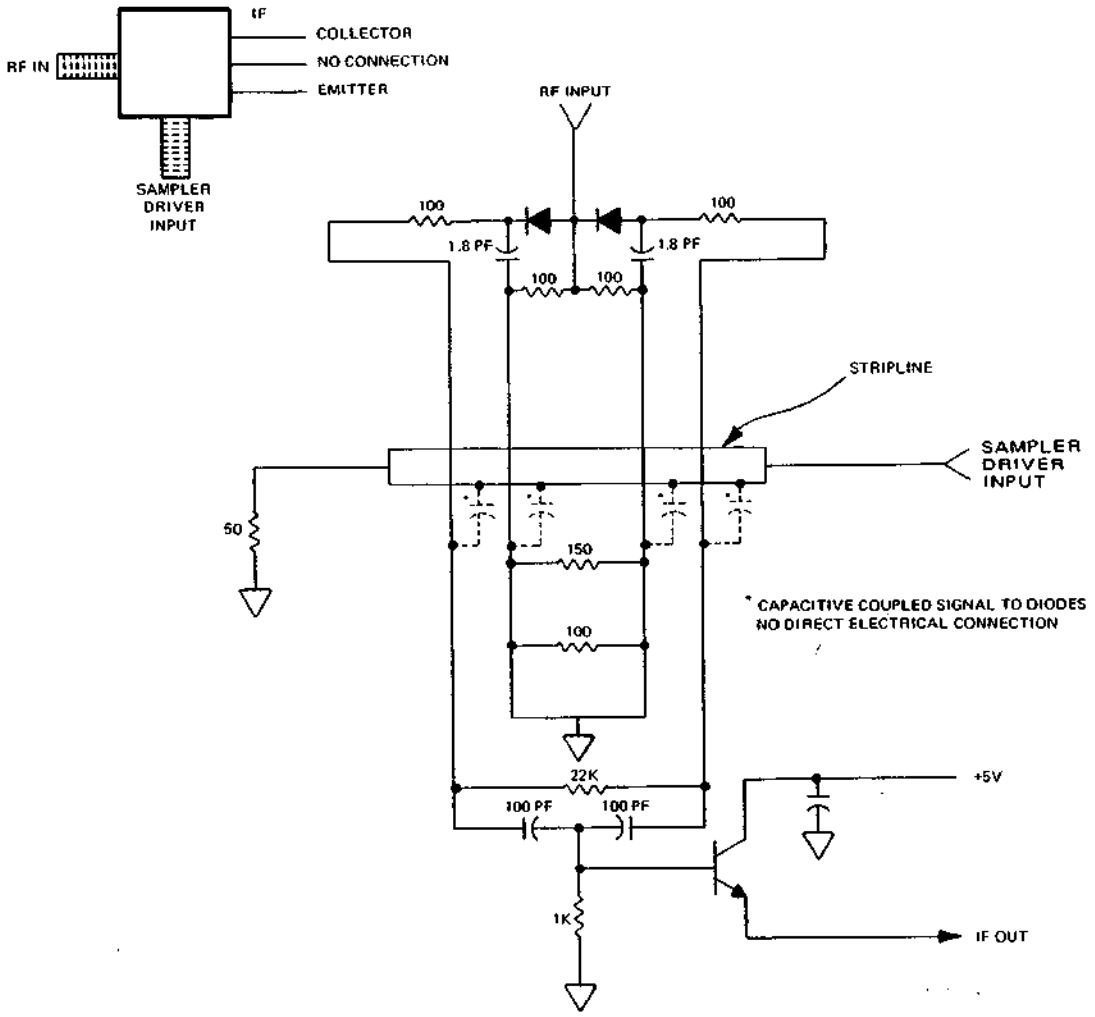
   c. With a scope probe, reach down inside casting to probe input to A25A1 for check of interconnecting cable.

   d. Signal trace through A25A1 to locate faulty component. DC levels are shown on apron of schematic.

TABLE 8-17
A11, A12, A25, A28

Table 8-17. A11, A12, A25, A28 U1 IF Troubleshooting (Continued)

e. The U1 Sampler contains an NPN one-transistor amplifier. The output leads are actually the emitter and collector of this transistor as shown:



f. As can be seen in the above drawing, ohmmeter checks can quickly determine if the transistor is good. Check for the following readings:

Ohmmeter Lead		
–	+	**Model 3465 Ohmmeter Range**
E	B*	1.79K (2K range)
B*	E	1.483 Meg (2 meg range)
E	C	∞ (2 meg range)
C	E	1.65 meg (2 meg range)
C	B*	555K (2 meg range)
B*	C	1.78K (2K range)

*Base is Sampler case

Even though the transistor checks ok, the sampler diodes or other components may be damaged. This is especially true if the 5343A has been overloaded by inputs in excess of the damage level (+25 dBm).

Table 8-17. A11, A12, A25, A28 U1 IF Troubleshooting (Continued)

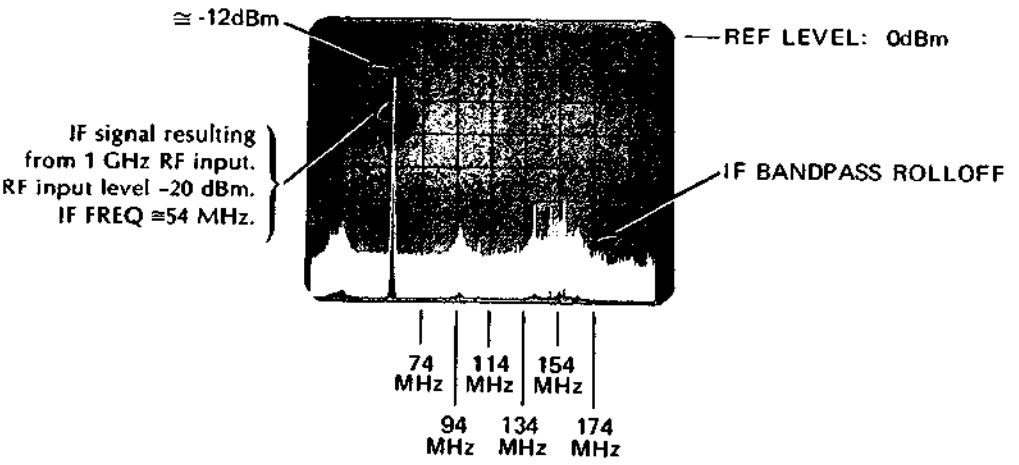
6. IF Troubleshooting Using Spectrum Analyzer

a. As an additional means of troubleshooting the IF section, the spectrum analyzer may be used. A study of the display below shows some features that indicate proper IF operation. The IF signal amplitude is a big clue to proper gain in the IF section.

b. Observe:

Input	-20 dBm
Sampler Conv. Loss	-40 dBm
Gain A28	+22 dB
Gain A25A1	+26 dBm
	≅-12 dBm

c. Close inspection of display shows the IF signal to be at ≅ -12 dBm level. Another point of interest is the IF bandpass rolloff at 175 MHz, as indicated on display. Note also the action of this spectrum picture as the input frequency is shifted. The IF signal will be seen to move across the screen.



IF OUT — Spectrum Analyzer

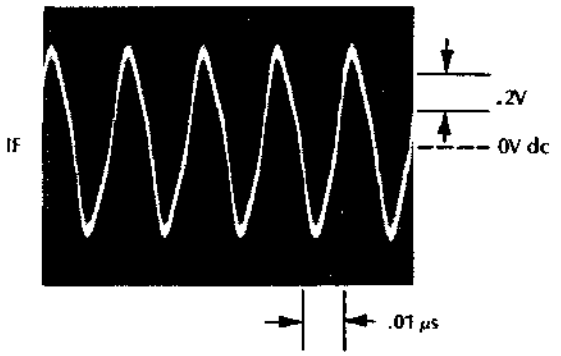
8565 Settings:

RES BW	300 kHz
REF LEVEL	0 dBm
INPUT ATTEN	10 dB
SCALE	10 dB/div
CENTER FREQ	114 MHz
FREQ/DIV	20 MHz

TABLE 8-17
A11, A12, A25, A28

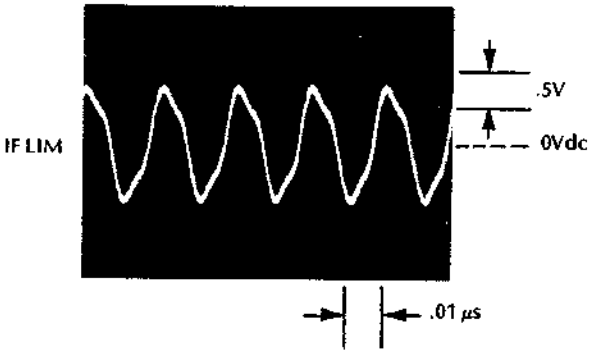
Table 8-17. A11, A12, A25, A28 U1 IF Troubleshooting (Continued)

7. Check the IF signal at XA11($\overline{1}$) using a 10 MΩ/10 pF oscilloscope probe. Signal should appear as follows:



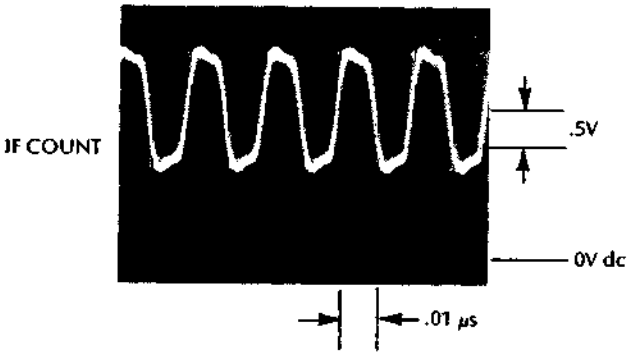
If this signal is not present, suspect the second stage of A25A1 or the interconnecting cable between A25 and the motherboard.

8. Check the IF LIM signal at XA11($\overline{12}$) with 10 MΩ/10 pF oscilloscope probe. Signal should appear as shown:



If this signal is not present, suspect A11.

9. Check the IF COUNT signal at XA12($\overline{8}$) with 10 MΩ/10 pF scope probe. Signal should appear as shown:



If this signal is not present, suspect amplifiers U2 and/or U4 on A12.

TABLE 8-17
A11, A12, A25, A28

Table 8-17. A11, A12, A25, A28 U1 IF Troubleshooting (Continued)

10. Testing A12 IF Detectors

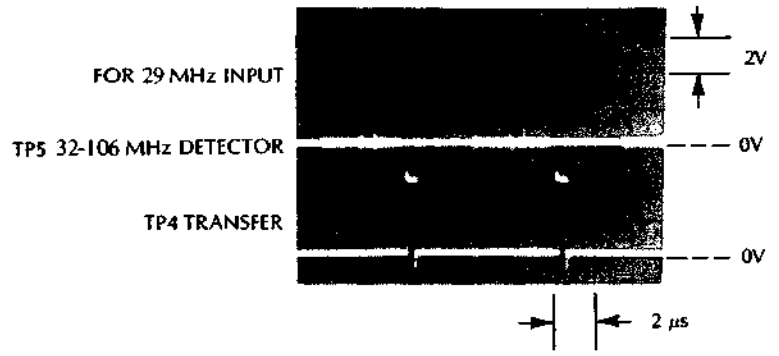
    a. Put the A12 IF detector on an extender board. Monitor TP8 (32—106 MHz detector) and TP9 (22—128 MHz detector) with a logic probe. Put the 5343A in AUTO and the 500 MHz—26.5 GHz range. Apply a 20 MHz 0 dBm signal to the high frequency input. Note that both TP8 and TP9 are low. Increase the input frequency to 22 MHz and notice that the logic probe indicates a high at TP9 (near the limits of the detectors, the logic probe will blink high). Increase the input frequency to 32 MHz and check that TP8 goes high. As the frequency is increased to 106 MHz, both TP8 and TP9 should be high. As the frequency is increased beyond 106 MHz, TP8 should go low and TP9 should remain high until 128 MHz is reached, at which TP9 also goes low. If these test points are correct the detectors operate properly. If the detectors do not operate, go to step 7.

    b. If the detectors operate as above but if the counter is in AUTO with a 50 MHz signal applied to its high frequency input and if, after placing the counter in diagnostic mode 0, the counter displays SP or SP2 only, the most probable cause is that the U12 output gates which drive the data bus are bad or else LPDRD is not being sent by the MPU. Use a logic pulser to pulse LPDRD and check the bus driver outputs with a logic probe. Also use a pulser to pulse LPDWRT to see if that sets the U7 latch to the low state (monitor TP10).

11. Troubleshooting 32—106 MHz Detector on A12:

    With a dual trace oscilloscope, monitor TP5 (32—106 MHz detector) and TP4 (transfer signal) on A12 under the following conditions. Check that the correct display is obtained. (Put A12 on extender board 05342-60034).

    a. Apply a 29 MHz signal at 0.6V p-p to the 500 MHz—26.5 GHz input of the 5343A.



    b. Increase the frequency to 32 MHz. The following display should be observed:

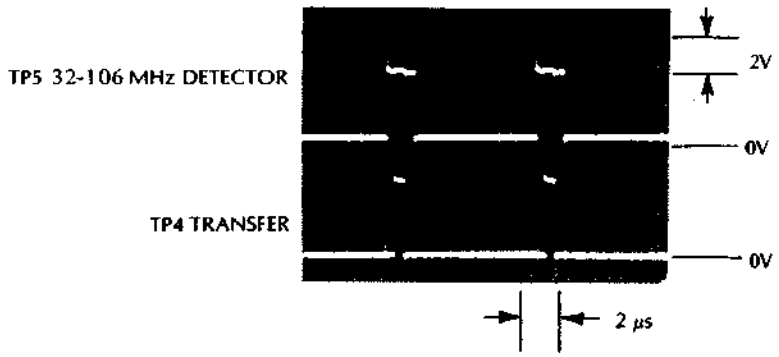
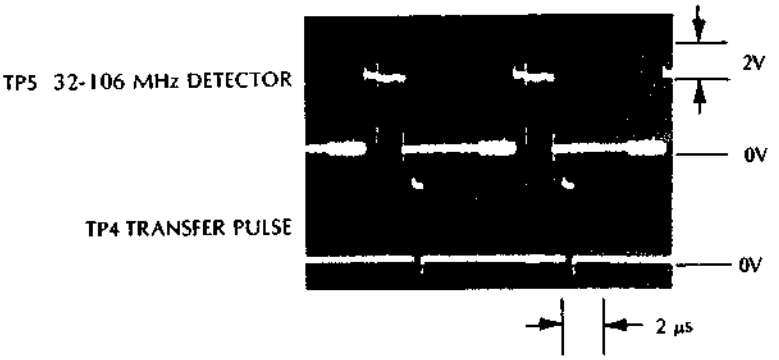


TABLE 8-17
A11, A12, A25, A28

Table 8-17. A11, A12, A25, A28 U1 IF Troubleshooting (Continued)

c. Increase the frequency from 32 to 106 MHz. Over the entire frequency range, the transfer pulse (TP4) should occur inside the detector pulse (TP5). The transfer pulse clocks the state of the detectors into U13 on A12.

d. Increase the frequency beyond 106 MHz to obtain the following display:



Transfer pulse occurs outside the detector pulse so that a low is transferred into U13.

e. Similar waveforms occur for the 22—128 MHz detector with different frequency limits.

f. Using the 5004A Signature Analyzer, troubleshoot the frequency detectors on A12, as follows:

g. Put A12 on an extender board and an AP clip on A12U15. Place the START probe and STOP probe of the 5004A Signature Analyzer on U15(12). Place the CLOCK probe of the 5004A on U15(8) which is the 1 MHz input to A12. Place the GROUND probe on U15(7).

h. Place the CLOCK, START, and STOP switches on the 5004A to positive slope (buttons out).

i. Connect the 10 MHz FREQ STD output on the rear panel of the 5343A to the high frequency input of the 5343A.

j. Place the data probe on +5V to see if characteristic 1's signature of UP73 is obtained. If not, replace U15. CHECK the signature at U6(3) to see if the 10 MHz signal is entering the digital filter properly. This signature should be 55H1. Check U6 signature and work back along the incorrect signature signal path.

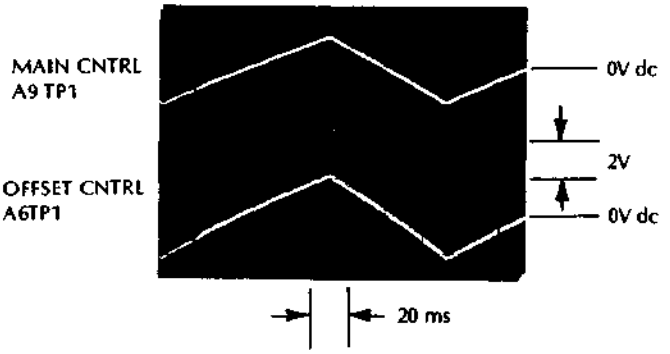
U6(1) A1C9	U5(1) UP73	U8(1) 0000	U9(1) 0000
U6(2) 0U16	U5(2) 6097	U8(2) 0000	U9(2) 1F2C
U6(3) 55H1	U5(3) NA	U8(3) HP01	U9(3) 0000
U6(4) P258	U5(4) NA	U8(4) P258	U9(4) 6097
U6(5) 1F2C	U5(5) 9HP0	U8(5) 0000	U9(5) 2F60
U6(6) 0000	U5(6) 9HP0	U8(6) UP73	U9(6) UP73
U6(7) 0000	U5(7) 0000	U8(7) 0000	U9(7) 0000
U6(8) 0000	U5(8) A1C9	U8(8) UP73*	U9(8) 0000*
U6(9) UP73	U5(9) 2F60	U8(9) UP73	U9(9) UP73
U6(10) 0000	U5(10) NA	U8(10) 0000	U9(10) UP73
U6(11) 0000	U5(11) NA	U8(11) 0000	U9(11) 0000
U6(12) UP73	U5(12) 1F2C	U8(12) UP73	U9(12) 0000
U6(13) 0000	U5(13) UP73*	U8(13) 0000	U9(13) UP73
U6(14) UP73	U5(14) UP73	U8(14) UP73	U9(14) UP73

U10(1) UP73	U11(1) UP73	U7(1) 6097	U14(1) 0U16
U10(2) 0000	U11(2) 0000	U7(2) 2F60	U14(2) 55H1
U10(3) NA	U11(3) 0000	U7(3) HP01	U14(3) 0000*
U10(4) NA	U11(4) UP73		U14(4) FH3F
U10(5) 0000	U11(5) 0000		U14(5) 0000*
U10(6) 0000	U11(6) UP73		U14(6) UP73*
U10(7) 0000	U11(7) 0000		U14(7) 0000
U10(8) 1F2C	U11(8) ACA2		U14(8) UP73*
U10(9) 0000	U11(9) 55H1		U14(9) 0000*
U10(10) NA	U11(10) FH3F		U14(10) FH3F
U10(11) NA	U11(11) 334U		U14(11) NA
U10(12) 0000	U11(12) 0000*		U14(12) ACA2
U10(13) UP73*	U11(13) UP73*		U14(13) 0U16
U10(14) UP73	U11(14) UP73		U14(14) UP73

***Probe blinks**

Table 8-18. A4, A6, A7 Offset Loop Synthesizer Troubleshooting

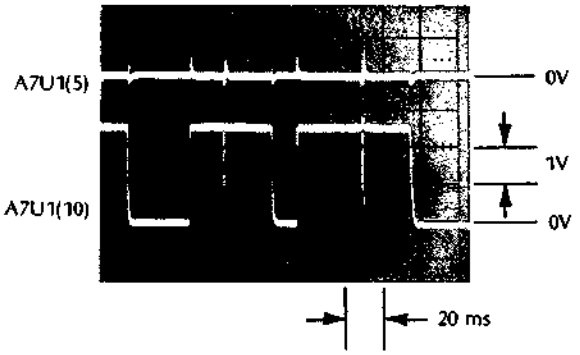
1. To test if the Offset Loop Synthesizer is working, put the 5343A in AUTO, 500 MHz—26.5 GHz range, and no input signal. Monitor the OFFSET CNTRL signal at A6TP1 and the MAIN CNTRL signal at A9TP1:

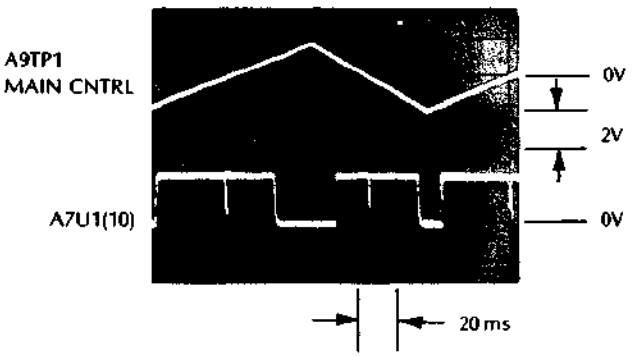


   Also measure the A4 output signal levels with an RF millivoltmeter with a high impedance probe. XA4($\overline{10}$) should be around 600 mV rms and XA4($\overline{7}$) around 300 mV rms. Both levels are ±100 mV and essentially independent of frequency.

2. To determine if A4 has failed, use a clip lead to ground A6TP1. This forces the A4 VCO to its freerun frequency of 325 MHz (±2 MHz). Connect XA4($\overline{10}$), the OFFSET OSC signal, to the direct count input of the 5343A using a coax cable with BNC connector on one end and alligator clips on the other. Adjust A4R1 for the proper frequency if necessary. Check that the level is approximately 600 mV rms.

3. If A4 is good, then either A6 or A7 has failed. Pull the A6 OFFSET LOOP AMP from the instrument, put A7 on an extender board and monitor A7U1(5) and A7U1(10), the phase detector outputs, with an oscilloscope. Put the 5343A in AUTO, 500 MHz—26.5 GHz range, and no signal input. Ground XA4($\overline{5}$), the OFFSET CNTRL signal, with a clip lead to cause A4 to go to 325 MHz. It may be necessary to push MAN, then AUTO, in order to get the characteristic display of all zeros and start the instrument sweeping. The display should be as follows:

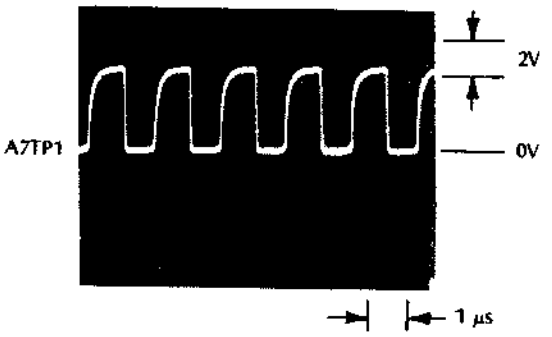




   If these signals are present, then A7 is OK.

TABLE 8-18
A4, A6, A7

4. If these signals are not present, then the mixer portion of A7 should be checked. With A6 out of the instrument, ground XA4($\overline{5}$) so that the A4 VCO goes the 325 MHz. Put the 5343A in manual mode and program the MAN center frequency (to check that the VCO frequency is that desired, put the 5343A in diagnostic mode 1 so that the main VCO frequency is displayed). For example, program the MAN center frequency to 576 MHz: the diagnostic mode 1 displays 325.5 MHz as the main VCO frequency. Monitor A7TP1, the output of the mixer and check for the presence of the difference frequency between the main VCO programmed frequency and the freerun frequency of A4.



With A6 removed, HSRCH EN, XA7(2) should be TTL high.

5. To check A6, install A6 and remove A7 from the instrument. Remove the short to ground on XA4($\overline{5}$). The search generator on A6 should begin search and driving the OFFSET CNTRL signal in a search ramp. LPOS SLOPE should go low to indicate when the frequency of the VCO is being swept ROM higher to lower values.

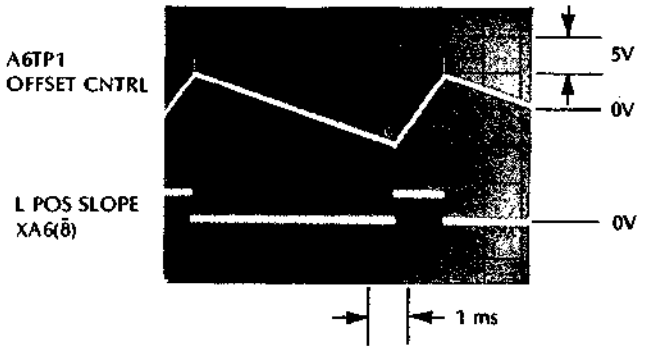
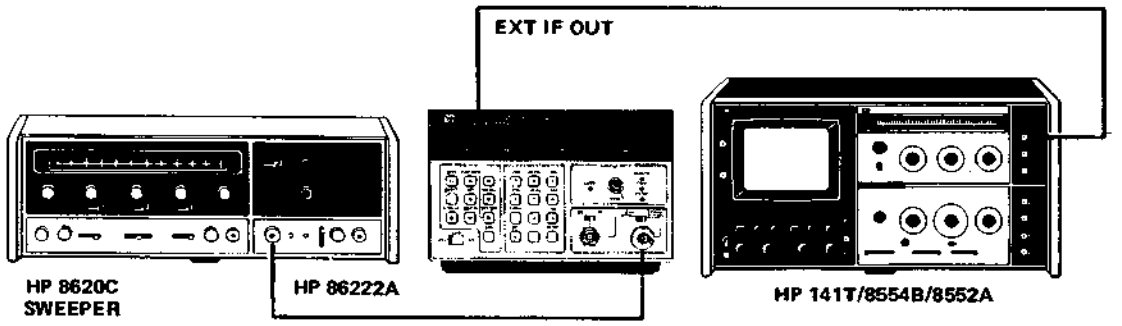


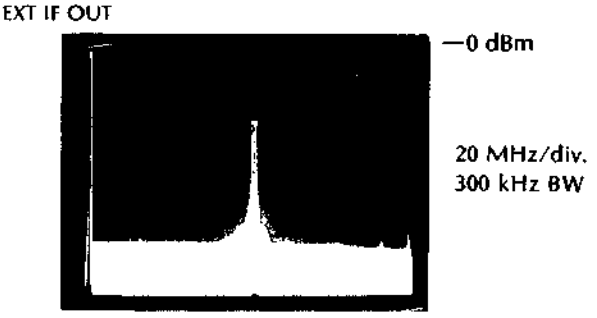
Table 8-19. A5 RF Multiplexer Troubleshooting

Set up the test equipment as shown:



Set the 8620C to 1.2 GHz at approximately –20 dBm. Place the 5343A in AUTO, 500 MHz—26.5 GHz range, and in diagnostic mode 2 (press SET, SET, 2) so that the counter continuously displays the A counter contents as it remains in the harmonic determination routine. The trace on the spectrum analyzer should show two IF's, indicating that the A5 Multiplexer is switching between the main synthesizer and the offset synthesizer.

The wideband filter on A9 is switched in as can be determined by the wider noise skirts about the signal.



1.2 GHz @ –20 dBm input to CNTR.

If the scale is expanded to 1 MHz/div., it is seen that the separation between the IF's is 2 MHz (=4 × 500 kHz) where 4 is the N number. Go to diagnostic mode 1 to verify N=4.

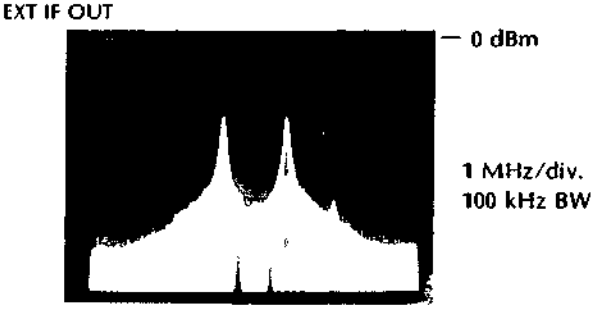
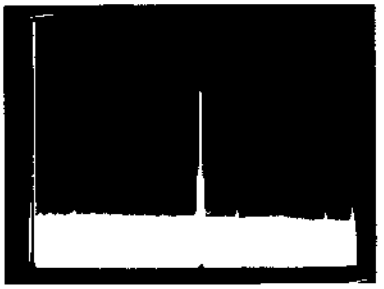


TABLE 8-19
A5

Table 8-19. A5 RF Multiplexer Troubleshooting (Continued)

Put counter in diagnostic mode 4 which continuously measures the IF. The narrow band filter on A9 is switched in and noise skirt about IF reduced.

EXT IF OUT



—0 dBm

20 MHz/div.
300 KHz BW

1.2 GHz @ -20 dBm input

TABLE 8-19
A5

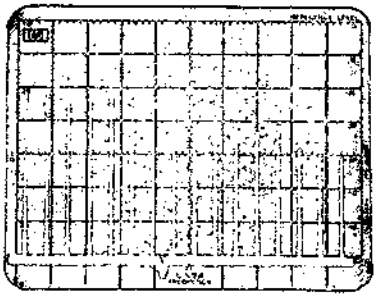
Table 8-20. A26 Sampler Driver Troubleshooting

1. Remove U1 Sampler, A26 Sampler Driver, and A28 IF Preamplifier as described in paragraph 8-35.
2. Two approaches exist for checking A26. The first method, and the preferred one, is a spectrum analyzer check of the Sampler Driver output. The second method is an output power level check.
   a. Spectrum Analyzer check:
      (1) Carefully remove the Sampler U1 from the A26 assembly. Use particular caution in not twisting or jerking on the A26 coax connector.
      (2) Using appropriate adapters and coax cable, connect A26J1 to the Spectrum Analyzer input.

CAUTION

Total output power of A26 is ≅+17 dBm. Provide spectrum analyzer input attenuation if necessary.

      (3) Set the 5343A to check mode. Observe a spectrum analyzer presentation similar to that shown below. Note that the amplitude level in the analyzer display does not approach +17 dBm. This is normal. The power meter response is broadband and will present a readout of ALL signals recorded at its input. The spectrum analyzers narrower response will give a lower level display.



REF LEVEL: 20dBm
RESOLUTION BW: 3 MHz
INPUT ATTEN: 20dB
SCALE: 10dB/div.

NOTE

Depending on the test setup, cable quality and length, etc., A26 output may be observable up to 26 GHz. However, if a display similar to above is obtained, A26 can be considered OK, unless the specific complaint is lack of performance at the upper end of the 5343A's input range (>18 GHz). A new step recovery diode CR1 may cure the problem.

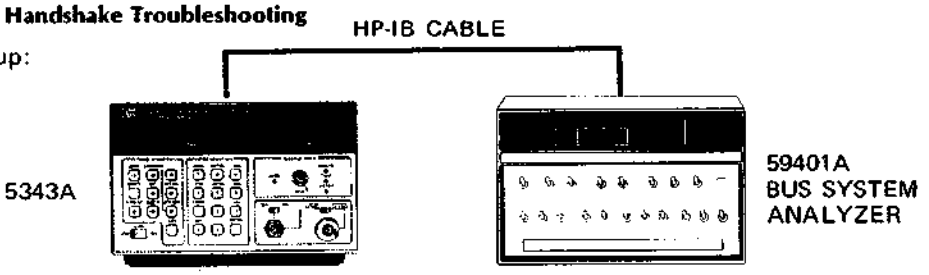
   b. Power Meter check:
      (1) Set 5343A to CHECK mode and measure the sampler driver output with a power meter. The output should be greater than +16 dBm (if the output of A5, which is driving A26, is at a level of approximately +15 dBm).
      (2) If the A26 output level is good, then A26U1 and associated circuitry are probably functioning properly. However, a good level does **not** indicate that the step recovery diode CR1 is working. CR1 could be open. To check the diode with an ohmmeter, connect the positive lead of the ohmmeter (such as the HP 3465A in OHMS function) to the center conductor of the A26 Sampler Driver output and the common leads to the A26 case. Place the ohmmeter in the 2K range (1 mA current source) and measure a forward resistance of approximately 800 ohms. Measure a reverse resistance of infinity.
      (3) To replace CR1, simply unscrew the plastic holder and remove CR1 with tweezers. Reverse the process for assembly.

      If A26 is producing an output comparable to display above, and the 5343A still will not count a microwave input, check Sampler U1, *Table 8-17*.

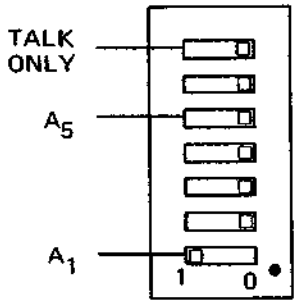
Table 8-21. Option 011 HP-IB Troubleshooting

1. Acceptor Handshake Troubleshooting

a. Setup:



Set 5343A rear panel address switch to:



59401A settings:
MEMORY . . . . OFF
COMP . . . . . OFF
TALK Mode
HALT
ATN = 1, SRQ = 0, EOI = 0
REN true (REN light on)
DIO switches to 5343A listen address:

8	7	6	5	4	3	2	1
0	0	1	0	0	0	0	1

b. Remove the A14 Microprocessor assembly from the 5343A. Perform the actions listed in *Table 8-21A* to verify the acceptor handshake. Use a 546A Logic Pulser to apply a clock pulse to a particular circuit node. Use a 545A Logic Probe to check the state of circuit nodes.

Table 8-21A. Acceptor Handshake (HP-IB)

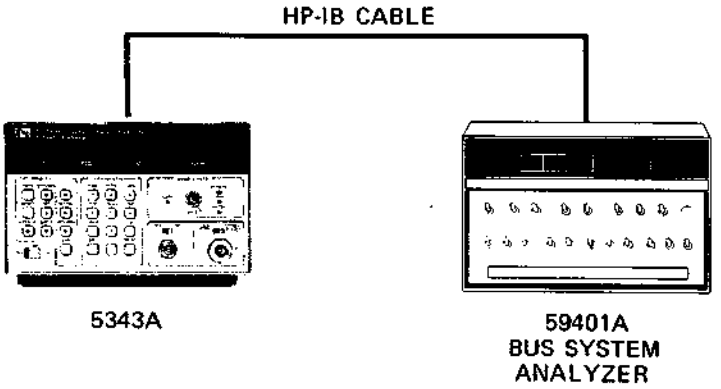
STEP	ACTION	59401A*			U6(13)	U3(9)	U6(10)	U6(4)	U3(5)	U6(1)	U32(6)	COMMENTS
		DAV Light	NRFD Light	NDAC Light								
0	Apply power to 5342A	OFF	ON	ON	Low	High	Low	Low	High	Low	High	Since the 5342A's listen address is on the data lines, U33(14) should be high. If not, check inputs. U33(4,5,6,7, 9,10,11,12) should all be TTL high. U33(3,13) should be TTL low.
1	Clock U3(11) once	OFF	OFF	ON	Low	Low	High	Low	Low	Low	Low	U20(10) and U29(6) should go high. U23(2) should go high. U1(8) should go high. Interrupt flag U10(5) should go high
2	Press EXECUTE on 59401A	ON	OFF	ON	High	Low	High	Low	Low	Low	Low	
3	Clock U3(11) once	ON	OFF	ON	High	High	Low	High	Low	Low	Low	
4	Clock U3(11) once	ON	ON	ON	Low	High	Low	High	High	Low	High	
5	Clock U3(11)	OFF	ON	OFF	Low	Low	Low	Low	High	High	High	
6	Go to Step 1 and Handshake sequence Repeats											

NOTES:
*DAV "ON" means that LDAV at A15U31(6) is TTL Low.
NRFD "ON" means that HRFD at A15U22(14) is TTL Low.
NDAC "ON" means that HDAC at A15U25(14) is TTL Low.

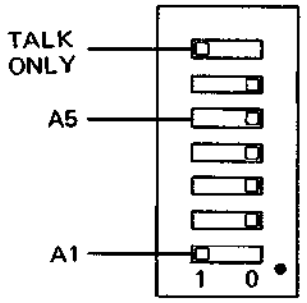
Table 8-21. Option 011 HP-IB Troubleshooting (Continued)

2. Source Handshake Troubleshooting

a. Setup:



Set rear panel address switch to Talk only:



59401A settings:
- REN true (REN light ON)
- HALT
- LISTEN mode

b. Remove the A14 Microprocessor assembly. Perform the actions listed in *Table 8-21B* to verify the source handshake. Use a 546A Logic Pulser to clock circuit nodes and a 545A Logic Probe to check the state of circuit nodes.

Table 8-21B. Source Handshake (HP-IB)

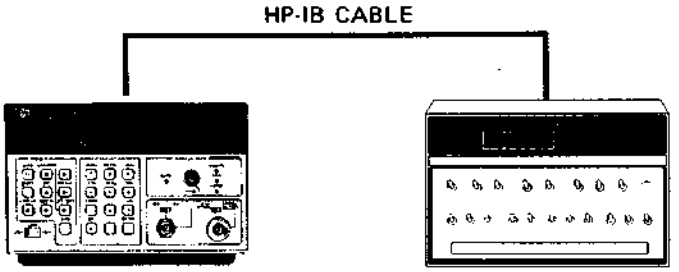
STEP	ACTION	59401A			U5(4)	U9(9)	U2(4)	U2(13)	U4(9)	U5(13)	U4(5)	U36(3)
		DAV Light	NRFD Light	NDAC Light								
0	Apply power to 5342A	OFF	OFF	ON	High	High	Low	Low	High	Low	Low	High
1	Clock U9(11) once	OFF	OFF	ON	High	Low	High	Low	High	Low	Low	High
2	Clock U4(11) once	OFF	OFF	ON	High	Low	High	High	Low	Low	Low	High
3	Clock U4(11) once	ON	OFF	ON	High	Low	Low	High	Low	Low	High	Low
4	Press EXECUTE on 59401A	ON	ON	OFF	High	Low	Low	Low	Low	Low	High	Low
5	Clock U4(11) once	OFF	OFF	ON	Low	High	Low	Low	High	Low	High	High
6	Clock U4(11) once	OFF	OFF	ON	High	High	Low	Low	High	Low	Low	High
7	Go to Step 1 and the Handshake Sequence Repeats											

TABLE 8-21
OPTION 011

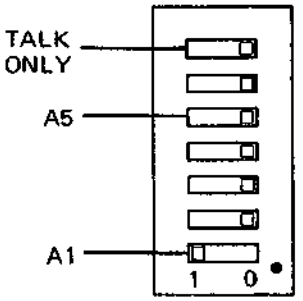
Table 8-21. Option 011 HP-IB Troubleshooting (Continued)

3. U23, U26 ROM Troubleshooting

a. Setup:



Set rear panel address switch to:



59401A settings:

MEMORY . . . . OFF
COMP . . . . . OFF
TALK Mode
HALT
SRQ = 0, EOI = 0
REN True

b. Remove the A14 Microprocessor assembly from the 5343A. Place A15 HP-IB assembly on an extender. Place an AP clip on U1 and ground U1(8). Set ATN and the DIO switches on the 59401A as listed in *Table 8-21C* and check with a 545A Logic Probe for the correct outputs.

Table 8-21C. U23, U26 ROM Table (HP-IB)

COMMENTS	**59401A SETTINGS DIO LINES								*U23 PINS							*U26 PINS							
	ATN	8	7	6	5	4	3	2	1	1	2	3	4	5	6	7	1	2	3	4	5	6	7	9
Listen Address	1	0	0	1	0	0	0	0	0	1	0	1	1	1	1	1	1	0	1	0	0	0	0	0
Talk Address	1	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0
Data (M)	0	0	1	0	0	1	1	0	1	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0
Go to Local	1	0	0	0	0	0	0	0	1	1	1	0	0	1	0	1	1	0	1	1	1	0	1	0
Serial Poll Enable	1	0	0	0	1	1	0	0	0	1	1	0	1	1	1	1	1	1	1	0	0	0	0	0
Serial Poll Disable	1	0	0	0	1	1	0	0	1	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0
Group Execute Trigger	1	0	0	0	0	1	0	0	0	1	1	0	0	1	0	1	1	0	1	1	0	0	1	0
Local Lock-Out	1	0	0	0	1	0	0	0	1	1	1	0	0	1	0	1	1	0	1	1	1	1	1	0
Device Clear	1	0	0	0	1	0	1	0	0	1	1	0	0	1	0	1	1	0	1	0	1	1	1	0
Selected Device Clear	1	0	0	0	0	0	1	0	0	1	1	0	0	1	0	1	1	0	1	0	1	0	1	0
Unlisten	1	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	0	0	1	0	0	0	0	0
Untalk	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	0	0	1	0	0	0	0	0

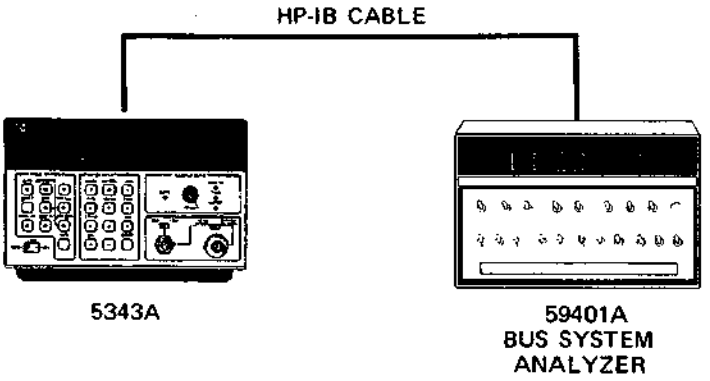
NOTES:
*Ground U1(8) to enable ROM U23
*1 = TTL High for U23, U26
**(1 = TTL Low for 59401A outputs, e.g., if DIO7 set to 1, then LDIO7 at A15U31(10) is TTL Low)

TABLE 8-21
OPTION 011

Table 8-21. Option 011 HP-IB Troubleshooting (Continued)

4. Troubleshooting Registers U27, U24, U21, U16, U18, U30, U15

a. Setup:



b. Remove A14 Microprocessor assembly from the 5343A and place the A15 HP-IB assembly on extender boards.

c. Place an AP clip on U11 and connect a clip lead from U11(12) to ground. This enables the U27 Data In register.

d. U27 CHECK:

Set the 59401A to TALK, HALT, and the 8 DIO switches to Ø (all switches down). Check the inputs to U27(3, 4, 7, 8, 13, 14, 17, 18) for all TTL high. If these inputs are not all TTL high, troubleshoot the input data buffers U22, U25, U31. With the 546A Logic Pulser, pulse U27(11). Check the outputs of U27(2, 5, 6, 9, 12, 15, 16, 19) for all TTL high. Change the DIO switch of the 59401A to all 1 (all switches up). Pulse U27(11) once. Check the U27 outputs for all TTL low.

e. U21 CHECK:

If U27 is working, it is possible to control the state of the microprocessor data bus and thereby check out U21, U24, and U16. To check out U21, gound U12(5) with another clip lead (U12(12) is still grounded). This enables U21. With the 59401A DIO switches all set to 1 (all switches up), clock U27(11) with the Logic Pulser. Now check U21(11). Check the outputs of U21(2, 5, 6, 9, 12, 15, 16, 19) for all TTL low. Now change all the 59401A DIO switches to Ø (all switches down). Clock U27(11) with the Logic Pulser. Verify that the U21 outputs are still TTL low. Now clock U21(11). Verify that the U21 ouptuts are all high.

f. U24 CHECK:

Check the clip lead on U12 from pin 5 to pin 13 so that U12(13) is grounded. Check that U21(1) is TTL high. If U21(1) remains low after the clip lead is removed, the serial poll FF U29 must be set high. To do this, ground U29(14) and clock U29(12). Verify that U29(10) is TTL high. U12(13) grounded enables U24. U27 should still be enabled by the ground on U11(12). With the 59401A DIO switch all set to Ø (switches down), clock U27(11) and clock U24(11). Verify that that outputs of U24(2, 5, 6, 9, 12, 15, 16, 19) are all TTL high. Change the 59401A DIO switches to 1 (all switches up). Clock U27(11) with the Logic Pulser. Verify that all the U24 outputs are still TTL high. Now clock U24(11) and verify that the U24 outputs are all TTL high.

g. U16 CHECK:

Remove the clip lead from U12(13). U27 should still be enabled by the ground on U11(12). With the DIO switches of the 59401A all set to 1 (all switches up), clock U27(11) with the 546A Logic Pulser. Next clock U16(9) and verify that the outputs of U16(2, 5, 7, 10, 12, 15) are all TTL low. Change the DIO switches on the 59401A to Ø (all switches down) and clock U27(11). Verify that U16 outputs remain TTL low. Now clock U16(9) and verify that the U16 outputs are all TTL high.

Table 8-21. Option 011 HP-IB Troubleshooting (Continued)

h. U18 CHECK:

Change the clip lead on U11 from pin 12 to pin 13 so that U11(13) is now grounded. This action will disable the U27 Data In register and will enable the U18 Interrupt Out register. Clock each of the inputs to U18(2, 4, 6, 10, 12) with a 546A Logic Pulser, and simultaneously check the corresponding output, U18(3, 5, 7, 9, 11) with the 545A Logic Probe. Remove the ground from U11(13) and verify that clocking an input has no effect upon an output (all the outputs should be in the high Z state).

i. U30 CHECK:

Change the ground to U11(15) with the clip lead. This enables the State In register U30. Clock each of the inputs to U30(2, 6, 10, 12, 14) and simultaneously check the corresponding outputs of U30(3, 7, 9, 11, 13). Remove the ground from U11(15) and verify that clocking an input has no effect upon an output.

j. U15 CHECK:

Change the ground to U11(14) which enables the Command In register U15. Set the DIO switches and ATN to the following:

ATN	8	7	6	5	4	3	2	1
1	0	0	1	0	0	0	0	0

(5343A rear panel HP-IB address switches set to 00001)

This should cause the U26 ROM outputs to present a TTL low to U15(12, 13, 14). Verify this with a logic probe. U15(11) will be TTL high since the A15 assembly powers up with the U20 Listen FF reset.

Clock U15(7) with the Logic Pulse and verify that U15(3, 4, 5) are TTL low and U15(6) is TTL high.

Set the DIO switches to the following:

ATN	8	7	6	5	4	3	2	1
1	0	0	1	0	0	0	0	1

Clock U20(12) to set the U20 Listen FF. This causes U15(11) to go TTL low.

Now set the DIO switches to the following:

ATN	8	7	6	5	4	3	2	1
1	0	0	0	1	0	0	0	1

This causes the U26 ROM outputs to present a TTL high to U15(12,13, 14). Verify this with the logic probe. U15(11) should be TTL low. Clock U15(7) and verify that U15(3, 4, 5) are TTL high and U15(6) is TTL low.

Table 8-22. Option 004 Digital-to-Analog (DAC) Troubleshooting

NOTE

The DAC option components are located on the A2 Display Driver board. To gain access to this board, the front panel must be disassembled. Refer to paragraph 8-28 for disassembly instructions.

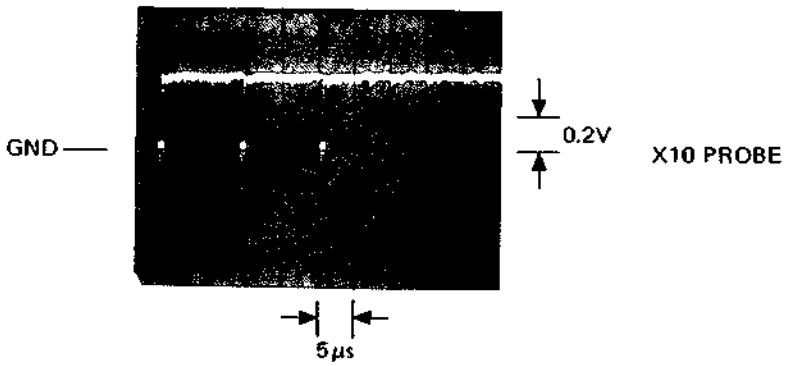
The troubleshooting procedure is based on the following assumptions regarding normal operation:

a. The 5343A measures applied signals properly.

b. The +15V and -15V power supplies are functioning. Check these voltages at the +15V and -15V input points on A2 assembly.

c. The 5343A has no software problems. The algorithm needed to perform the DAC function is contained in ROM firmware. If after the following checks, the DAC option still will not perform properly, suspect a ROM failure. Refer to *Table 8-10* and *Table 8-11* for information on the microprocessor and memory troubleshooting.

d. The LDA signal is present. See photo below for a view of this signal.

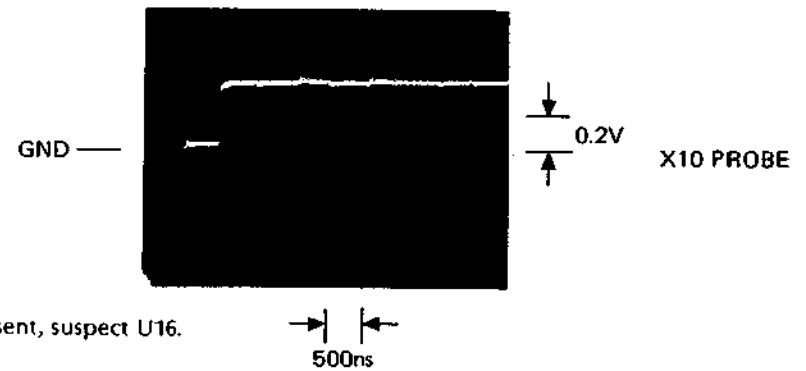


The LDA signal is used by the DAC option to load the selected digits (BCD word) into three registers on A2 (see *Figure 8-25*). U16 decodes address bit A0 and A1, and with LDA, loads BCD data (D0, D1, D2, D3) into U22 (MSD), U21 and U15 (LSD).

The stored BCD data in U22, U21, and U15 is then presented to D/A converter U24. The data on D0, D1, D2, and D3 will be changing as the input frequency changes, or different sets of 3 digits are chosen for D/A conversion.

Since the data and address information used for conversion are taken from the instruments buses, those signals can be assumed as present since the remainder of the instrument is working properly. With the LDA signal checked and found OK, all inputs to the option are accounted for. To check the remainder of the option circuitry, proceed as follows:

1. Check the outputs of decoder U16 pins 7, 9, and 10 for the signal used to clock the registers U22, U21, and U15 (shown below).



If this signal is not present, suspect U16.

TABLE 8-22 OPTION 004

Table 8-22 Option 004 Digital-to-Analog (DAC) Troubleshooting (Continued)

2. Apply an input frequency of 1000.00XX MHz. (X = Don't care).
3. Set up the DAC conversion, thus: SET [ ] SHIFT [ ] DAC [0] [4]

   This will convert the digits underlined: 0 1 0 0 0 0 X X X X X
4. Observing the DVM connected to the DAC output jack on the rear panel of the 5343A, note that it should read 0.001 (±.005)V.
5. If the above reading is not obtained, check the outpus of U22, U21, and U15 registers (pins 7, 6, 2, and 3). They shoud all be TTL high. If an output of a register is stuck low, check for short to ground using the current tracer (HP 547A). Since the 5343A is displaying its frequency properly, it may be assumed that the data lines (D0—D3) inputs to the register are valid. The register itself may have failed also.
6. Apply an input frequency of 777.7 MHz. Leave the DAC conversion set up as in step 2.
7. On each register (U22, U21, U15) output, check pins 6, 2, and 3 for a TTL low signal. If an output is stuck high, look for shorts to V_{cc} using the current tracer. The register itself may have failed also. (Pin 7 of each register should be TTL high at this time.)
8. To check that pin 7 of each register will indeed go low, apply an input frequency of 888.8 MHz.
9. Check pin 7 of each register (U22, U21, and U15) for a TTL low signal. If any of these lines are stuck high, check for shorts to V_{cc}. The register itself may have failed also.
10. After all of these register outputs are verified, the only circuit element remaining is the D/A converter U24. Before replacing U24, verify that the power supply voltages are correct (+ and −15V), and that "gain" and "offset" adjustments function (paragraph 5-33). After the replacement of U24, perform the adjustments as prescribed in paragraph 5-33.

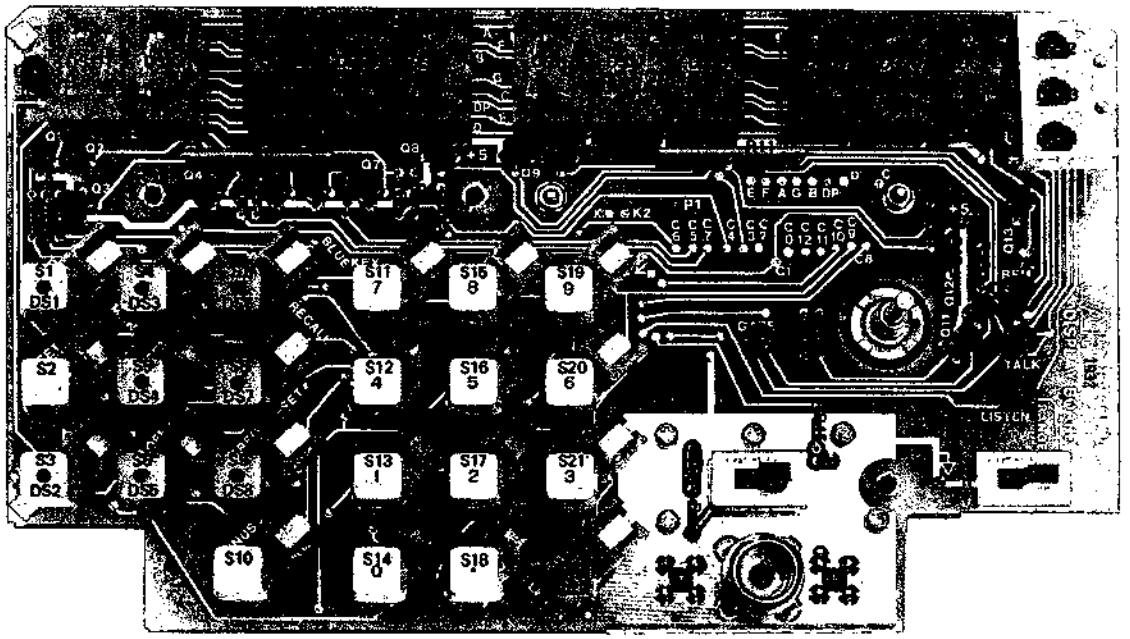


Figure 8-19. 5343A Front (A1 Display) View

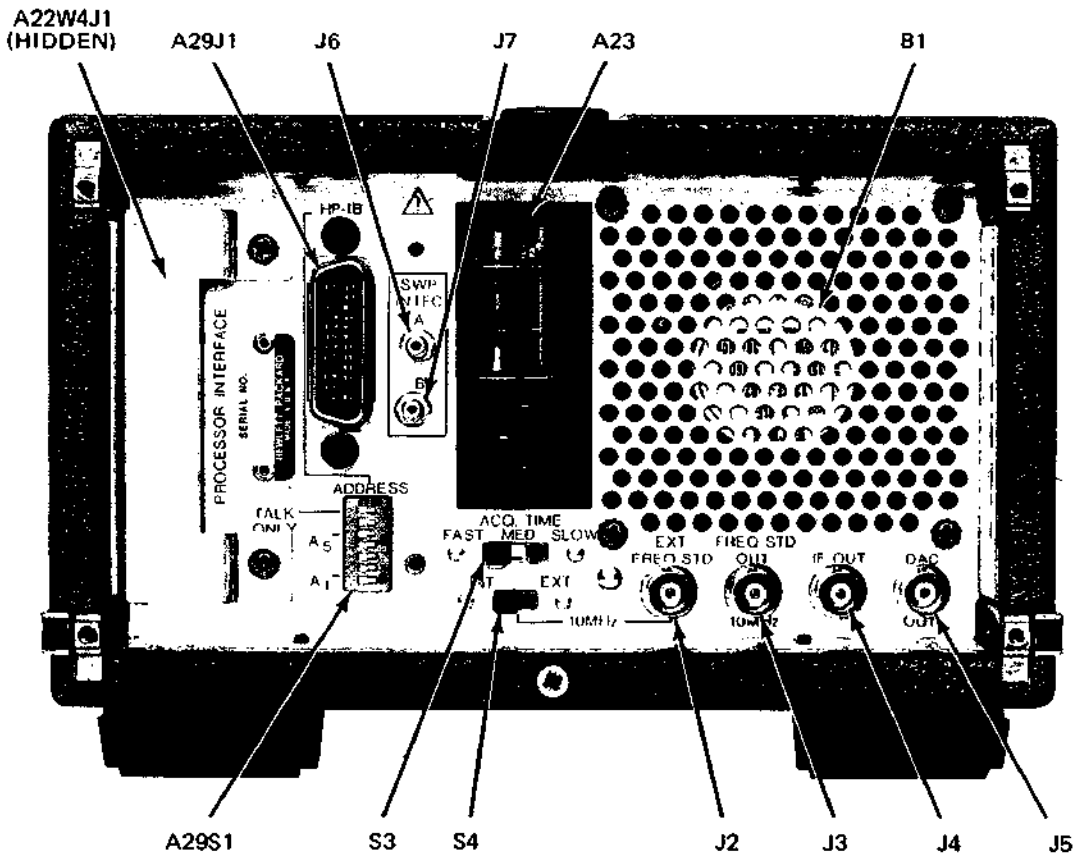


Figure 8-20. 5343A Rear View

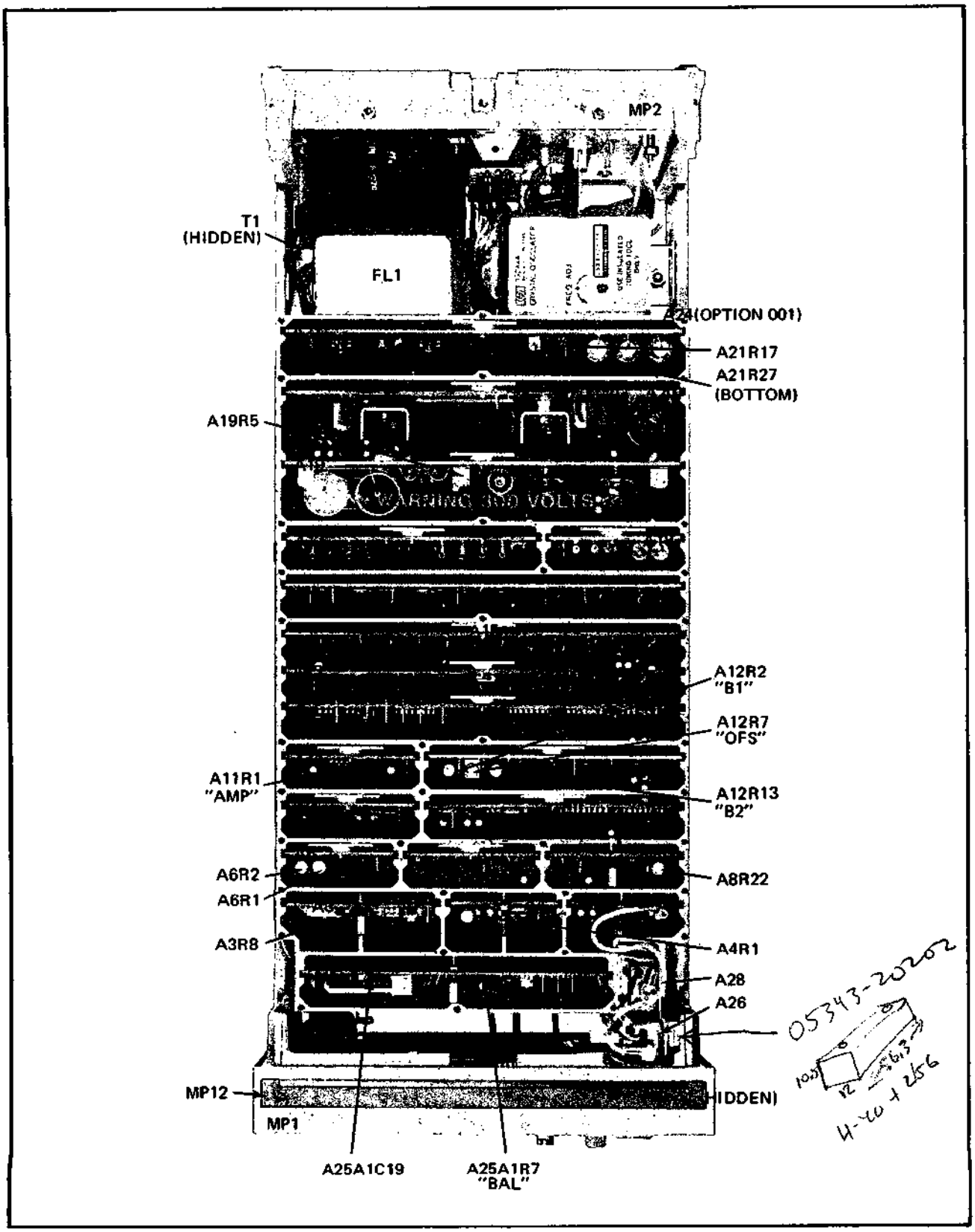


Figure 8-21. 5343A Top View (Assembly Location and Adjustments)

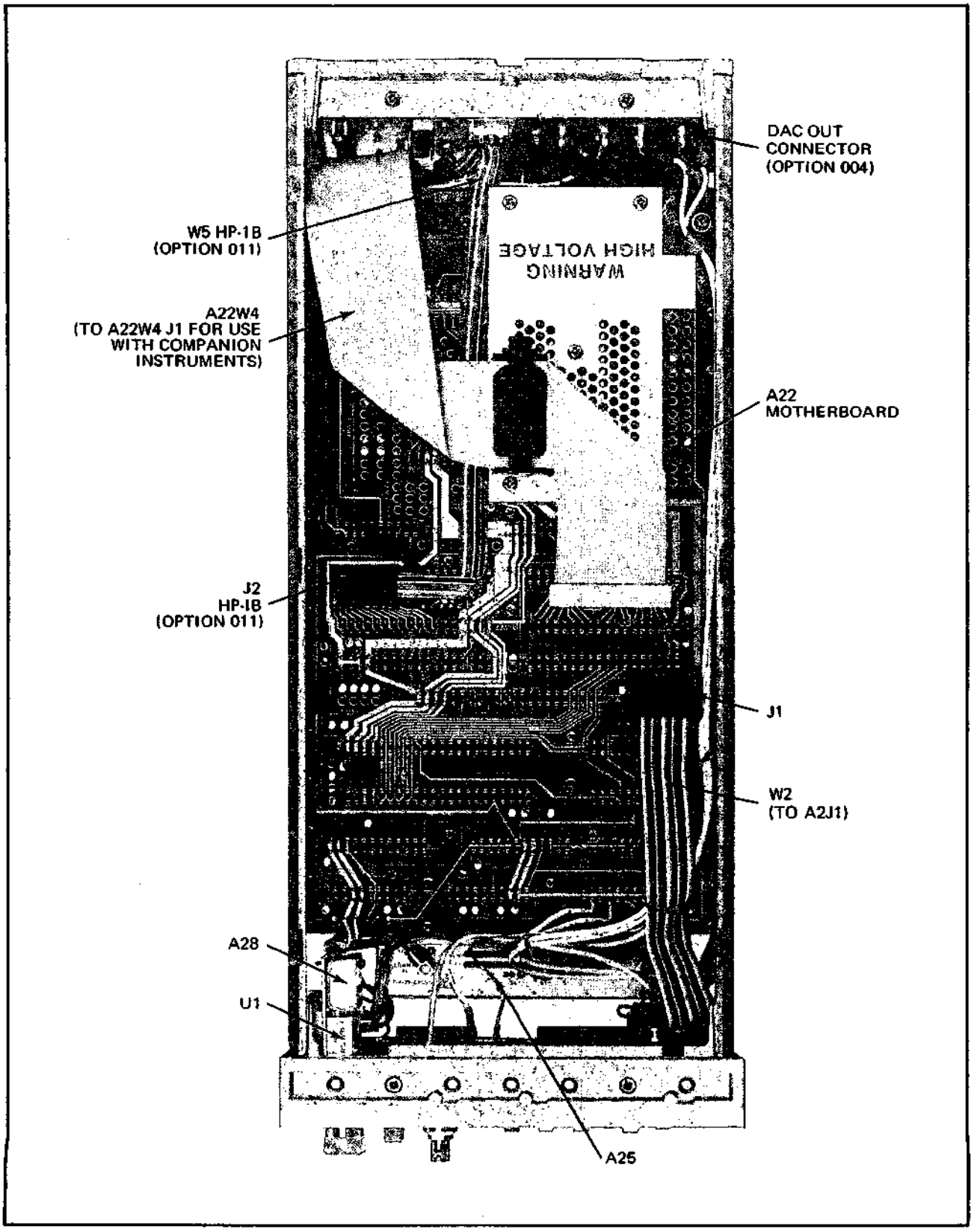


Figure 8-22. 5343A Bottom View, Options Installed

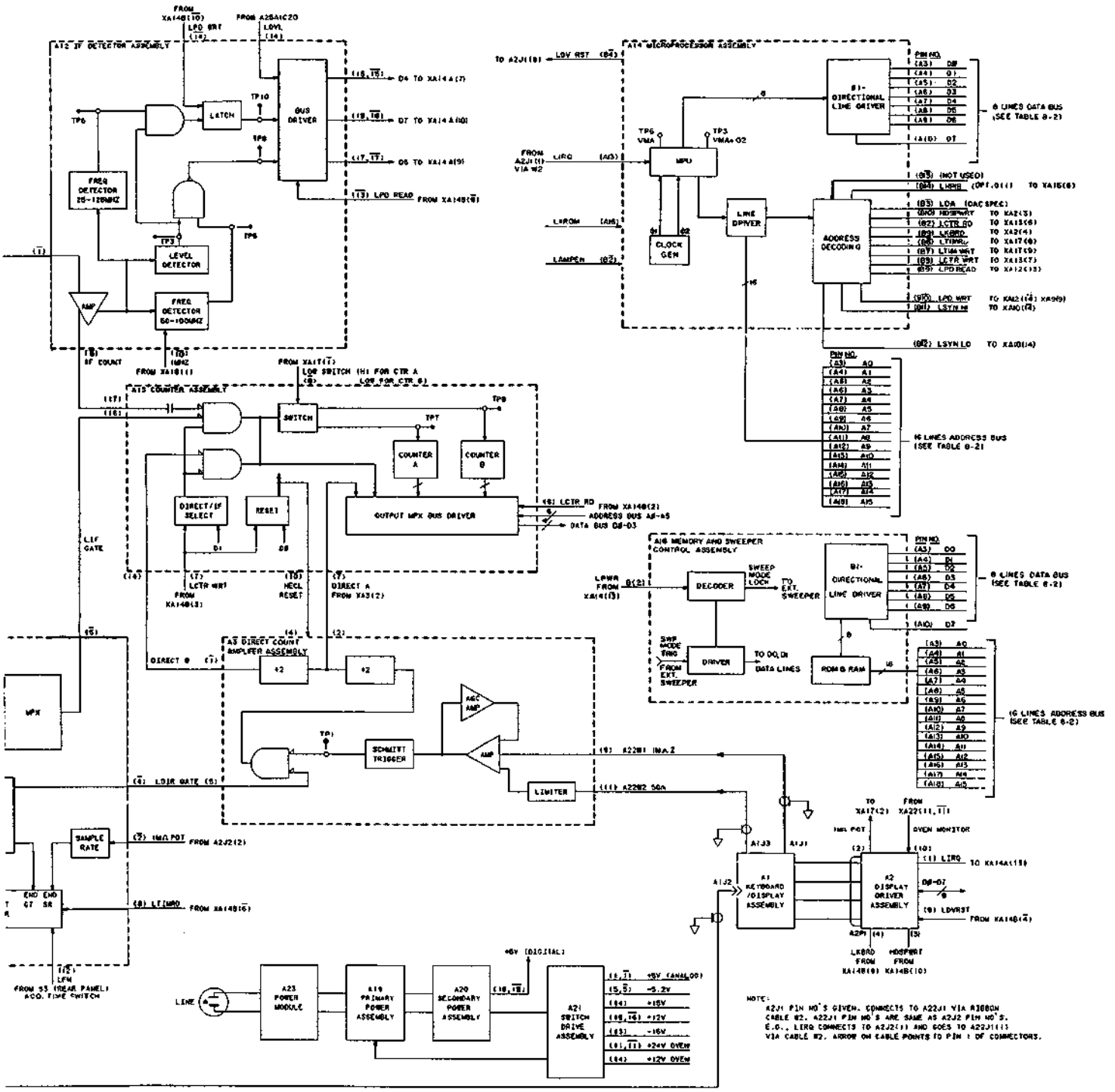
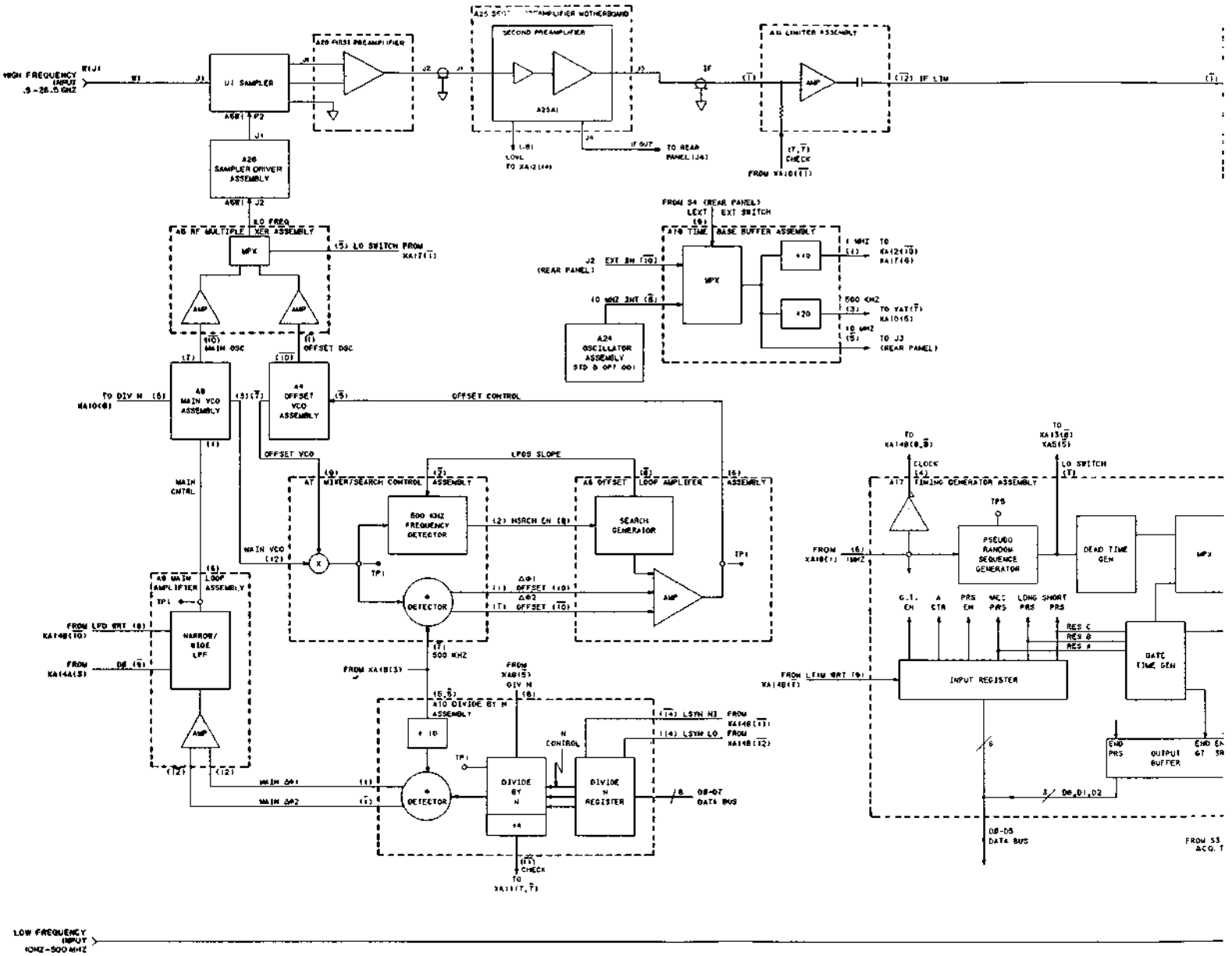
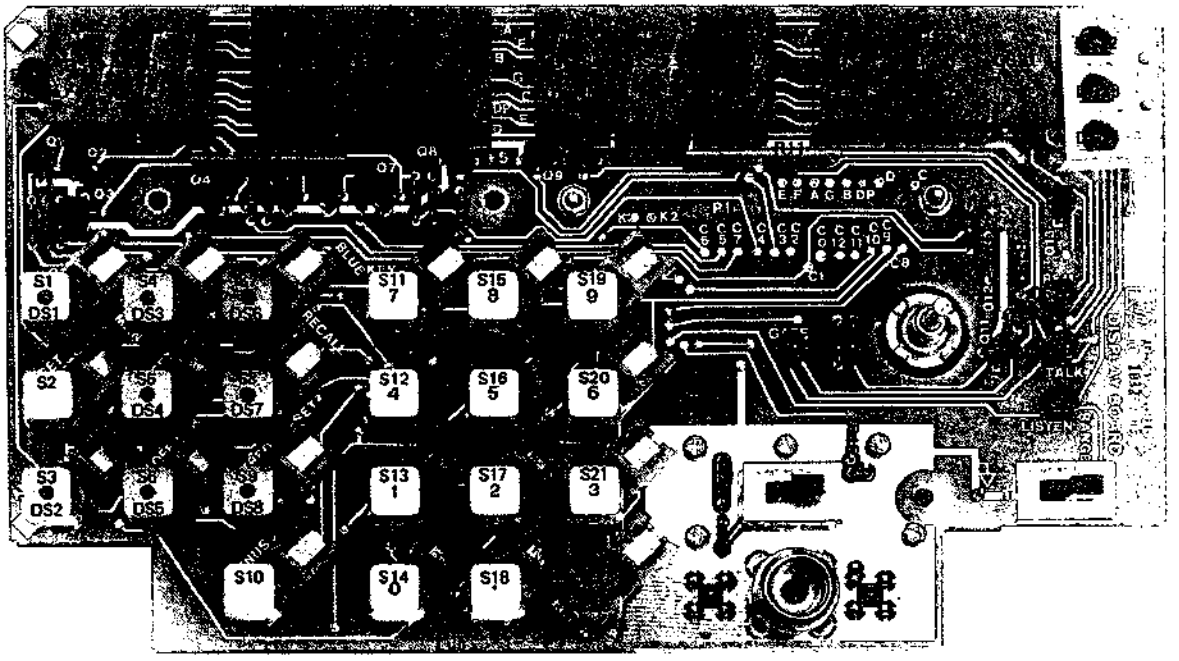


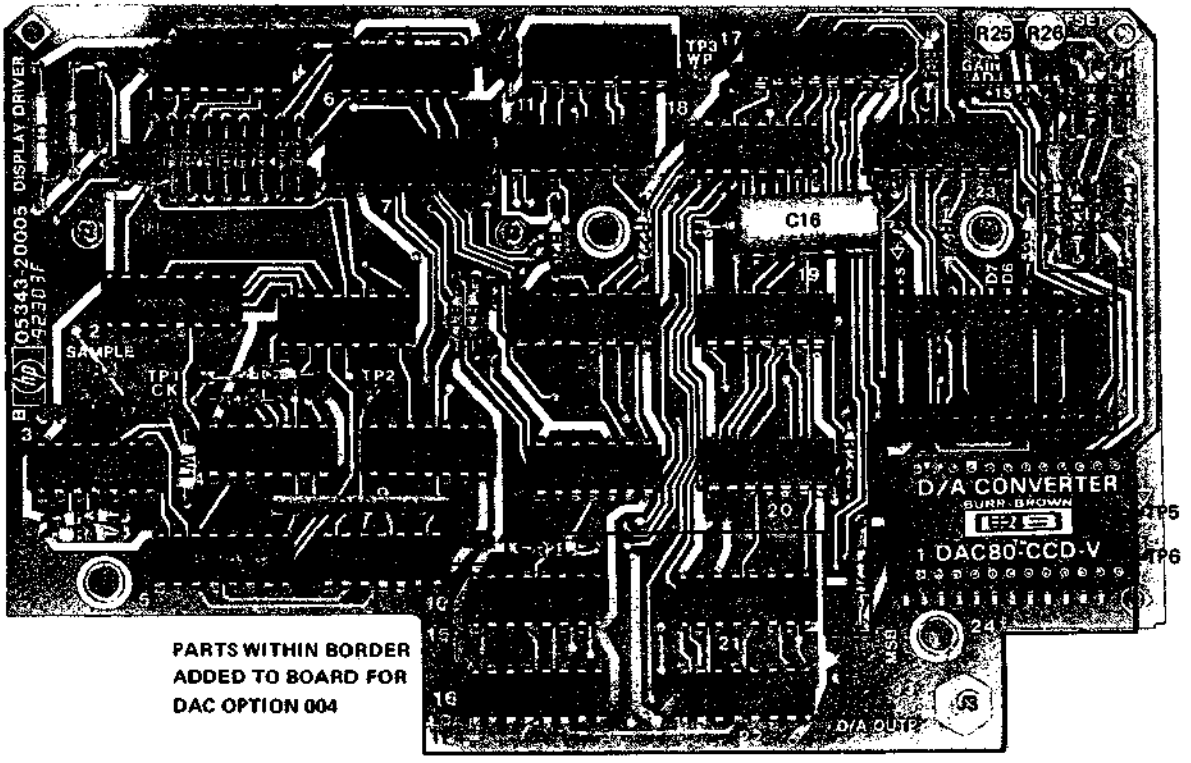
Figure 8-23. 5343A Detailed Block Diagram

5343A DETAILED BLOCK DIAGRAM





A1



A2

Part of Figure 8-24. A1 Display Assembly and A2 Display Drive Assembly

SERVICE NOTE

Supersedes:
None

HP 5343A MICROWAVE FREQUENCY COUNTER

ALL SERIAL PREFIXES

IMPROVED IF ADJUSTMENT PROCEDURES

This service note contains IF adjustment procedures which utilizes a spectrum analyzer instead of an RF voltmeter. These improved procedures are intended to be a substitute for the information contained on pages 5-5 through 5-7 in the Operating and Service Manual. Either procedure will give valid results, and the procedure to use will be dependent upon available equipment.

Perform the tests below in the order they are given. Do not skip any test to perform a later one.

5-21. IF Adjustment

Maintain the following counter settings and connections unless otherwise specified:

Impedance	50 ohm
Frequency Range	500 MHz - 26.5GHz
Sample Rate	full ccw
Connect rear FREQ STD OUT	signal generator EXT REF
Connect Input 1 (500MHz-26.5GHz)	signal generator output

Set spectrum analyzer to the following settings:

Center frequency	100MHz
Frequency span/div	20MHz
Bandwidth	300KHz
Sweep time	20ms
Input attenuation	0dB
Reference level	0dBm

I/PM/WN

05/88-02/FEP

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Printed in U.S.A.

5-22. A25A1R7 (balance) adjustment

a. Enter a center frequency of 500MHz by keying in SET, MAN, 500, ENTER.

b. Apply a 530MHz, 0dBm signal to the 5343A.

c. Connect the 5343A rear IF OUT to the spectrum analyzer input.

d. Adjust A25A1R7 to minimize the second harmonic signal seen on the spectrum analyzer. The second harmonic will be located at about 140MHz (see *Figure 1*).

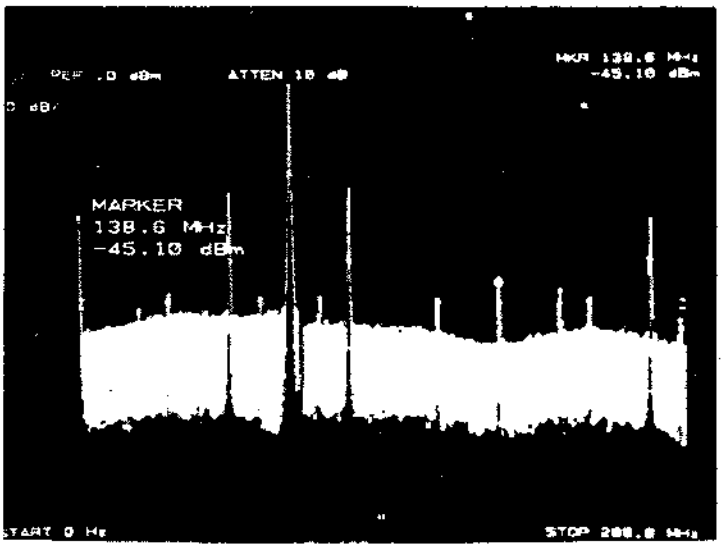

Figure 1

5-23. A25A1C19 (175 MHz rolloff) adjustment

a. Set frequency mode to AUTO.

b. Set sample rate to HOLD (full cw).

c. Set diagnostic mode 7 by keying in SET, SET, 7. The counter should display 350.5MHz indicating that the MAIN VCO is at 350.5MHz.

d. Set signal generator to –15dBm. Sweep from 10MHz to 200MHz in 5MHz steps.

e. Increase the sweep time of the spectrum analyzer to get an IF response similar to *Figure 2*. Note the amplitude of the flat portion of the band. This portion is usually located at about 60MHz - 100MHz.

f. Set the signal generator's output to 175MHz.

g. Turn the 5343A sample rate ccw and observe the displayed frequency count down. When the display shows 330MHz, turn the sample rate fully cw to the HOLD position. (The reason for adjusting the VCO frequncy from 350MHz to 330MHz in this test is to move the second frequency line on the spectrum analyzer away from the 175MHz signal. The signal that doesn't move is the 175MHz signal that is used to make the adjustment.)

h. Adjust A25A1C19 so that the response signal at 175MHz is 10(±1)dB below the amplitude noted in e. See *Figure 2.*

i. Press RESET.

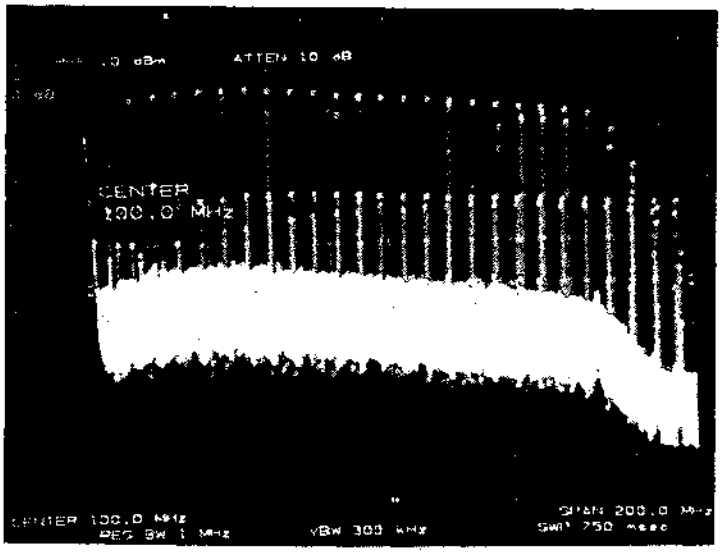

Figure 2

5-24. A11R1 ("Amp" gain) adjustment

a. Place A12 on a 22-pin extender board (HP P/N 05342-60034).

b. Set sample rate fully ccw.

c. Enter a center frequency of 500MHz by keying in SET, MAN, 500, ENTER.

d. Apply a 530MHz, –15dBm signal to the 5343A.

e. Probe A12U2 pin 1 with a spectrum analyzer.

f. Adjust A11R1 to minimize the second harmonic signal (at about 140MHz) seen on the spectrum analyzer.

5-25. A12R2 and A12R13 (gain) adjustments

a. Apply a 530MHz, –25dBm signal to the 5343A.

b. Probe A12U2 pin 5 with a spectrum analyzer.

c. Adjust A12R2 to minimize the second harmonic signal (at about 140MHz) seen on the spectrum analyzer.

d. Apply a 530MHz, –35dBm signal to the 5343A.

e. Probe A12U4 pin 8 with a spectrum analyzer.

f. Adjust A12R13 to minimize the second harmonic signal (at about 140MHz) seen on the spectrum analyzer.

g. Remove extender board from A12 slot and insert A12 board.

5-26. A12R7 (threshold detect) adjustment

a. Set 5343A to AUTO.

b. Pre-set A12R7 maximum cw. Observe that the 5343A is not counting.

c. Depending on the installed options in your counter, apply the following signal to the 500MHz - 26.5GHz input of the 5343A:

500MHz, –36dBm . . . . . STD

500MHz, –33dBm . . . . . Option 6

d. Adjust A12R7 ccw until the counter correctly reads 500 MHz.

e. Sweep up to 1GHz to assure proper count.

f. Set synthesizer to –20dBm power level and sweep from 1GHz to 26.5GHz to assure proper count.

Continue with Section 5-27 as stated in the Operating and Service Manual.

S E R V I C E N O T E

SUPERSEDES NONE

HP 5343A Microwave Frequency Counter

Serial Numbers: 2826A02787/2826A02798
See text for excluded serial numbers.

A1 Display Assembly P/N 05342-60004 Revision E
HP-IB LED Indicators May Give Erroneous Indications

To Be Performed By: HP-qualified personnel

Parts Required: None

Situation:

Some Revision E A1 Display Assemblies have been constructed with improperly connected HP-IB LED indicators. These indicators will light after certain combinations of key presses. This problem only affects the front-panel display of the actual state of the instrument. It indicates activity on the HP-IB bus when none is actually present. Excluded serial numbers are 2826A02791, 2826A02793, and 2826A02795

Solution/Action:

If the A1 Display Assembly has the two jumpers shown in Figure 1, this is the working version of the revision E boards. If the board does NOT have these jumpers, it needs to be repaired.

DATE 16 JUNE 1989

ADMINISTRATIVE INFORMATION

SERVICE NOTE CLASSIFICATION:

MODIFICATION RECOMMENDED

ACTION CATEGORY:	☐ IMMEDIATELY ■ ON SPECIFIED FAILURE ☐ AGREEABLE TIME	STANDARDS: LABOR 1.0 HOURS		
LOCATION CATEGORY:	☐ CUSTOMER INSTALLABLE ☐ ON-SITE ■ HP LOCATION	SERVICE INVENTORY:	☐ RETURN ☐ SCRAP ■ SEE TEXT	USED PARTS: ☐ RETURN ☐ SCRAP ■ SEE TEXT
AVAILABILITY:	PRODUCT'S SUPPORT LIFE	RESPONSIBLE ENTITY: 0200		UNTIL: 16 June 1991
AUTHOR: BOB KELLEY	ENTITY: 0200	ADDITIONAL INFORMATION:		

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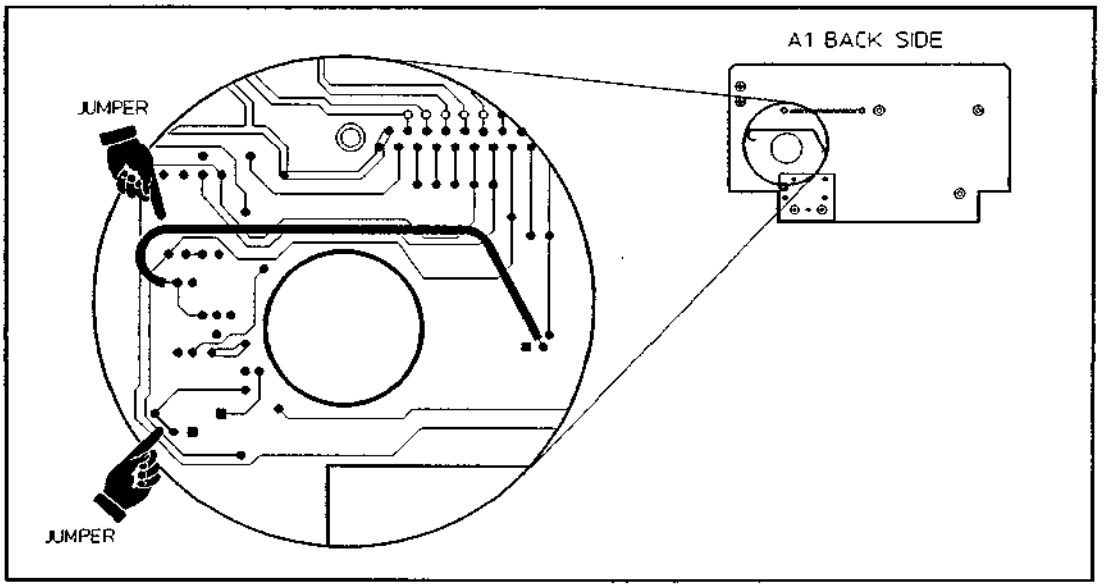

Figure 1. Good Revision E A1 Display Assembly (Back Side)

Repair Procedure:

1. You must solder two jumpers on the back side of the A1. The jumpers are shown on *Figure 1*.

2. You must cut two traces on the front side of the A1. The location of the two cuts are circled on *Figure 2*. The first is to the left of the LISTEN LED, between the cathode of a diode and the words "LISTEN". The second is between the words "TALK" and "REM".

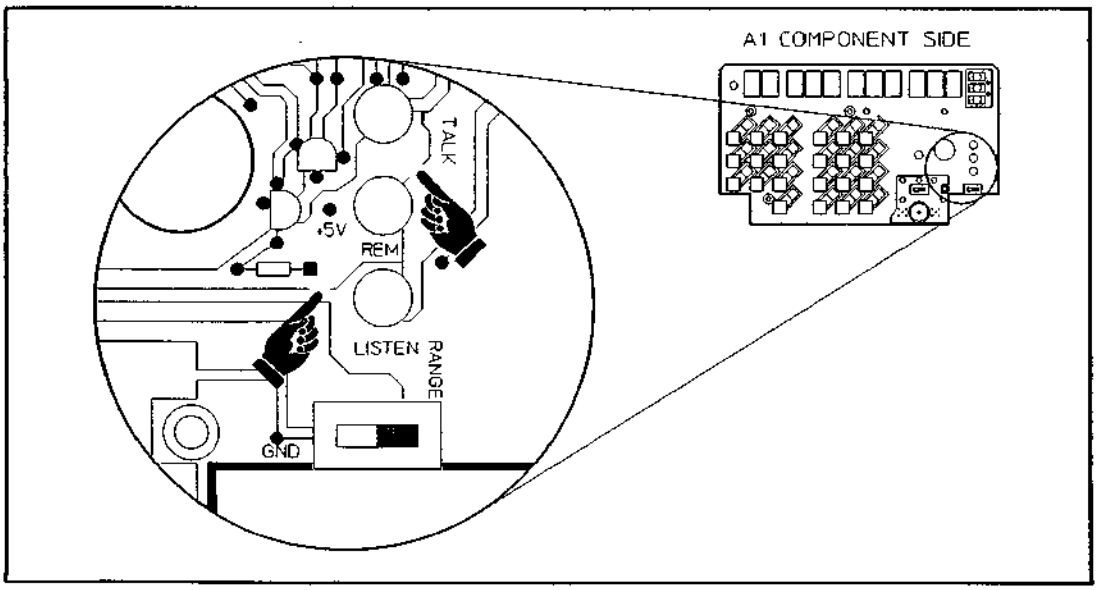

Figure 2. Location of Trace Cuts on Revision E A1 (Front Side)

Table 1. HP 5342A Service Notes Addressing 350 MHz Miscount Failures

SERIAL NUMBERS/PREFIXES	SERVICE NOTE	TITLE
2317A07386/2317A07905	5342A-41B	High Frequency Miscount
0000A00000/2440A09236	5342A-42A	High Frequency Miscount
0000A00000/9999A99999	5342A-59	Troubleshooting 350 MHz Miscount Problems

Table 2. HP 5343A Service Notes Addressing 350 MHz Miscount Failures

SERIAL NUMBERS/PREFIXES	SERVICE NOTE	TITLE
2014A and Below	5343A-7	Procedure to Correct Miscounts Between 24 - 26.5 GHz
Prior to 2026A	5343A-8	Procedure to Correct Miscounting Between 18 and 26.5 GHz
2317A01026/2317A01155	5343A-19A	High Frequency Miscount
0000A00000/2424A01674	5343A-20A	High Frequency Miscount
0000A00000/9999A99999	5343A-30A	Troubleshooting 350 MHz Miscount Problems

SERVICE NOTE

Supersedes:
None

HP 5343A MICROWAVE FREQUENCY COUNTER

Series Prefix 2542

A3 BOARD MISCOUNT PROBLEM SOLUTION
P/N 05342-60042

Some 5343A's between the serial numbers of 2510A02316 and 2510A02375 were shipped with a potential problem that exhibits itself as follows: input applied to low frequency input (10 Hz to 500 MHz) will be seen as a miscount or a count may be seen with no input that may clear up after warm up of an hour or more. Sensitivity is not an issue, as the miscount may occur at levels well above the minimum sensitivity.

The steps to fix this problem are as follows:

1. Replace *R31, *R40 and *R52 with 21.5 ohm resistors (P/N 0698-7196)

2. Place a ferrite bead (P/N 9170-0029) on the negative lead of electrolytic capacitor C21.

   Note: It may necessary to replace C21 (0180-3084) due to the increased lead length needed to install a ferrite bead on the negative lead.

3. Electrically test the A3 board as usual. If the instrument miscounts, *R31 and *R40 can be lowered to as low as 8 ohms to reduce the gain of the amplifier and eliminate the miscount. If the instrument does not pass sensitivity specs INCREASE *R31 and *R40.

   Note: *R31 and *R40 should be changed as a pair (*R31=*R40)

See other side for list of resistors.

D/OF/WO

07/86-02/AJ

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RESISTOR	P/N
10.0 ohm	0698-7188
12.1 ohm	0698-7190
13.3 ohm	0698-7191
15.0 ohm	0698-7690
16.2 ohm	0698-7193
16.7 ohm	0698-8651
27.4 ohm	0757-0387
34.8 ohm	0698-7201
38.3 ohm	0698-7202

MARIO TALBOT

5343A-30A

S E R V I C E N O T E

SUPERSEDES 5343A-30

HP 5343A Microwave Frequency Counter 350 MHz Miscount Problems

SERIAL NUMBERS: 0000A00000/9999A99999

DUPLICATE NOTES: 5342A-59

TO BE PERFORMED BY: HP/Qualified Personnel

Situation:

A common failure mode of the HP 5342A and HP 5343A is to miscount by ±350 MHz when measuring high frequencies (typically 18 GHz and above). Troubleshooting this failure can be difficult because it is usually intermittent and related to an open ground loop somewhere in the instrument. This problem typically occurs in older units.

This service note concentrates on possible remedies as opposed to identification of this failure mode.

Solution:

Here are some possible fixes to this failure mode that have proved successful. Suggestions 1 through 4 mention service notes that have been written in the past about the 350 MHz miscount problem. Even though they apply to specific serial numbers, all units should be checked for compliance. *Tables 1* and *2* at the end of this service note provide a consolidated listing with affected serial numbers of these service notes.

1. Duplicate service notes 5342A-41B and 5343A-19A address a 350 MHz miscount problem due to plastic extractors on the A4, A5 and A8 assemblies. The plastic extractors should be replaced with ground screws in order to complete the ground loop. (Refer to *Table 1* and *Table 2* for the applicable serial numbers.)

DATE 17 APRIL 1991

ADMINISTRATIVE INFORMATION

SERVICE NOTE CLASSIFICATION:

INFORMATION ONLY

AUTHOR:	ENTITY:	ADDITIONAL INFORMATION:
MARA DUMOND	0200	

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2. Duplicate service notes 5342A-42A and 5343A-20A address a 350 MHz miscount problem due to insufficient RF sheilding on the A26 and A28 assemblies. (Refer to *Table 1* and *Table 2* for the applicable serial numbers.)

3. Service note 5343A-7 addresses a 350 MHz miscount problem that really applies to HP 5343As prior to series prefix 2026A, even though the service note indicates all serials. A terminal ground lug is required between the HP 5343A main casting and the A26 Sampler Driver to complete an open ground loop.

4. Service note 5343A-8 addresses a 350 MHz miscount problem between 18 GHz and 26.5 GHz for serial prefixes prior to 2026A. In this case, the miscounts are caused by unequal levels between the Main and Offset VCOs.

If the 350 MHz miscount still persists, then try each suggestion below. They are listed by ease of performance. Each suggestion is known to correct 350 MHz miscounts, so it is worth taking the time to check each one.

5. Verify that the input signal is making a good and proper connection at Input 1.

6. Verify that cable A5W1 is not crimped or scratched by the RF Cavity cover. This cable connects from the A5 assembly, which is covered, to the A26 Sampler Driver, which is not.

7. With the RF Cavity cover removed, verify that the grounding screws on the A3, A4, A5, A8 and A25 assemblies make good contact with the main casting and are not loose. These grounding screws are located at the top of each assembly.

8. Verify that the ground fingers on the A4, A5 and A8 assemblies have not broken off. These fingers are located on the sides of the assemblies. Service note 5342A-11B describes procedures on how to replace them as well as an illustration of their location. This service note also applies to the HP 5343A.

9. For the HP 5343A, verify that the terminal ground lug is securely attached between the main casting and the A26 Sampler Driver assembly. Service note 5343A-7 provides a clear picture of this location. (It is critical that this ground lug be securely attached.)

10. Check for a loose cover or any missing screws on the A26 Sampler Driver, the A28 1st IF Preamp Assembly and the U1 Sampler.

11. Check for loose connections, bent pins and metal flakes at the following connections:

    a. between Input 1 and U1 Sampler.

    b. between Input 1 and U2 Sampler, if option 002 is installed.

    c. between U2 Sampler and U1 Sampler, if option 002 is installed.

    d. between U1 Sampler and A28 and A26 assemblies.

12. As a last resort, try replacing the A26 Sampler Driver and/or the A8 Main VCO.

SERVICE NOTE

Supersedes:
None

HP 5343A MICROWAVE FREQUENCY COUNTER

A29 REVISION C, HP-IB INTERCONNECTION BOARD LAYOUT ERROR

Certain 5343A Microwave Frequency Counters do not operate properly when used in either of the following situations: (1) "TALK ONLY" mode or (2) counter is set to an address greater than or equal to 16. This is due to a board layout error on the A29 HP-IB connector assembly which cause address switch no. 5 and TALK ONLY switch to be interchanged.

A29 assemblies (05342-60029) of Revision C vintage will cause the counter not to work properly unless a modification was made to the board prior to shipment. Some assemblies escaped unmodified. All subsequent A29 assemblies (Rev. D and later) were manufactured correctly.

Please notify the Santa Clara Division support engineer for microwave products when the counter indicates the above problem. The approved repair method is to replace the A29 Rev C board with the current production A29 board. It should take no longer than one hour to complete this repair.

D/OF/WA

04/88-02/FEP

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REFERENCE DESIGNATIONS

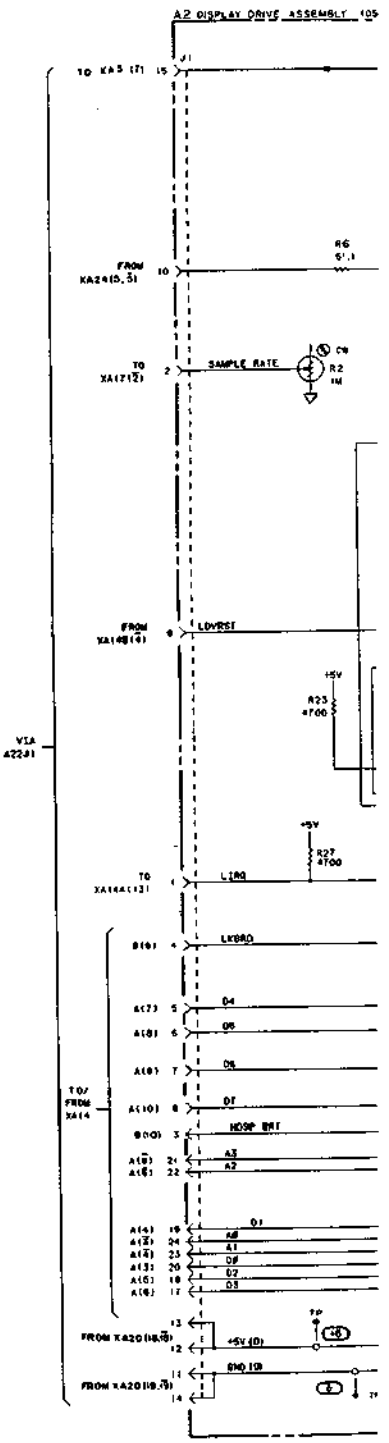
A1
C1, C2
DS1-DS28
J1-J3
Q1-Q13
R1-R18
S1-S24
TP1, TP2

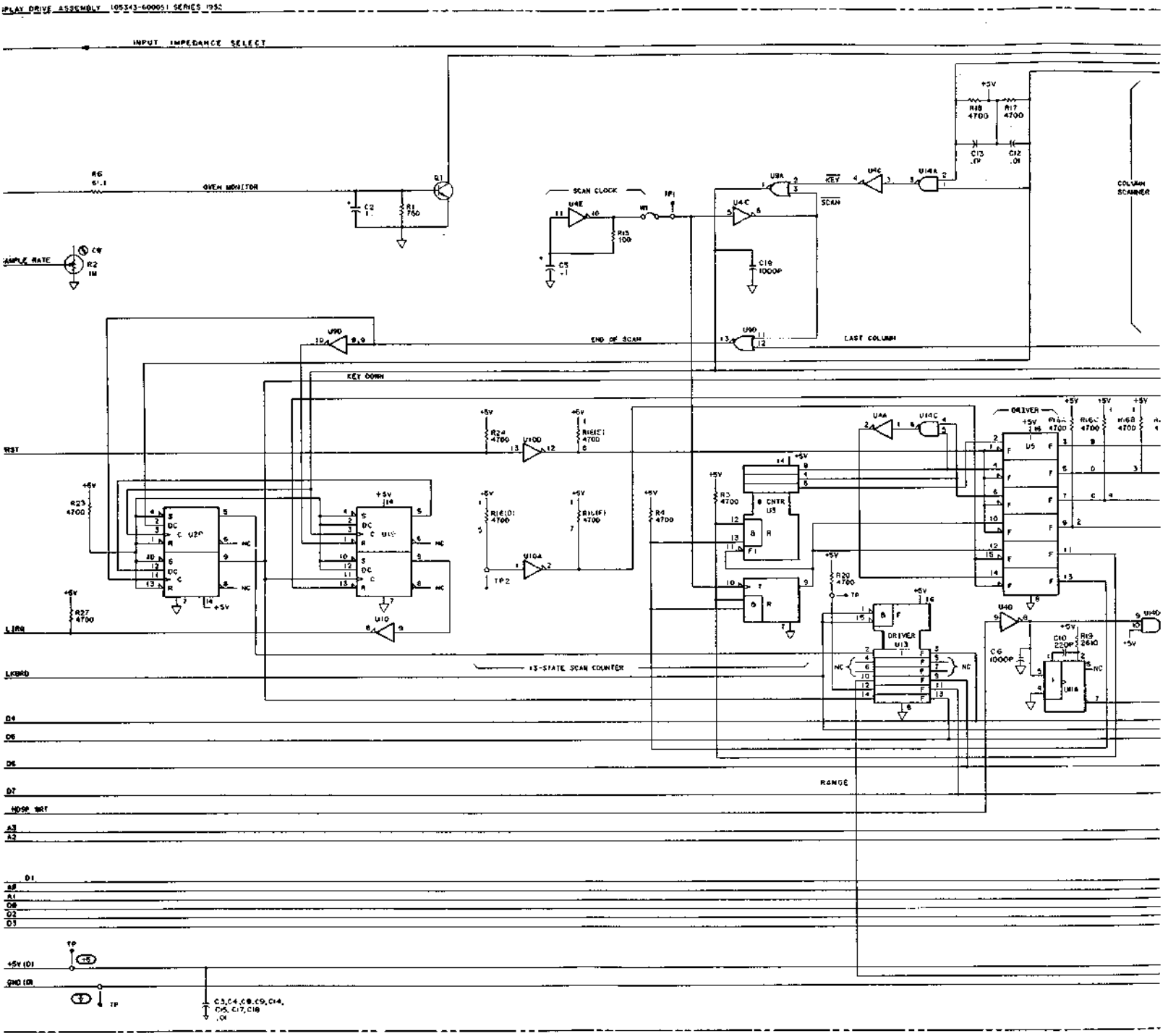
A2
C1-C24
Q1
R1-R34
TP1
U1-U24

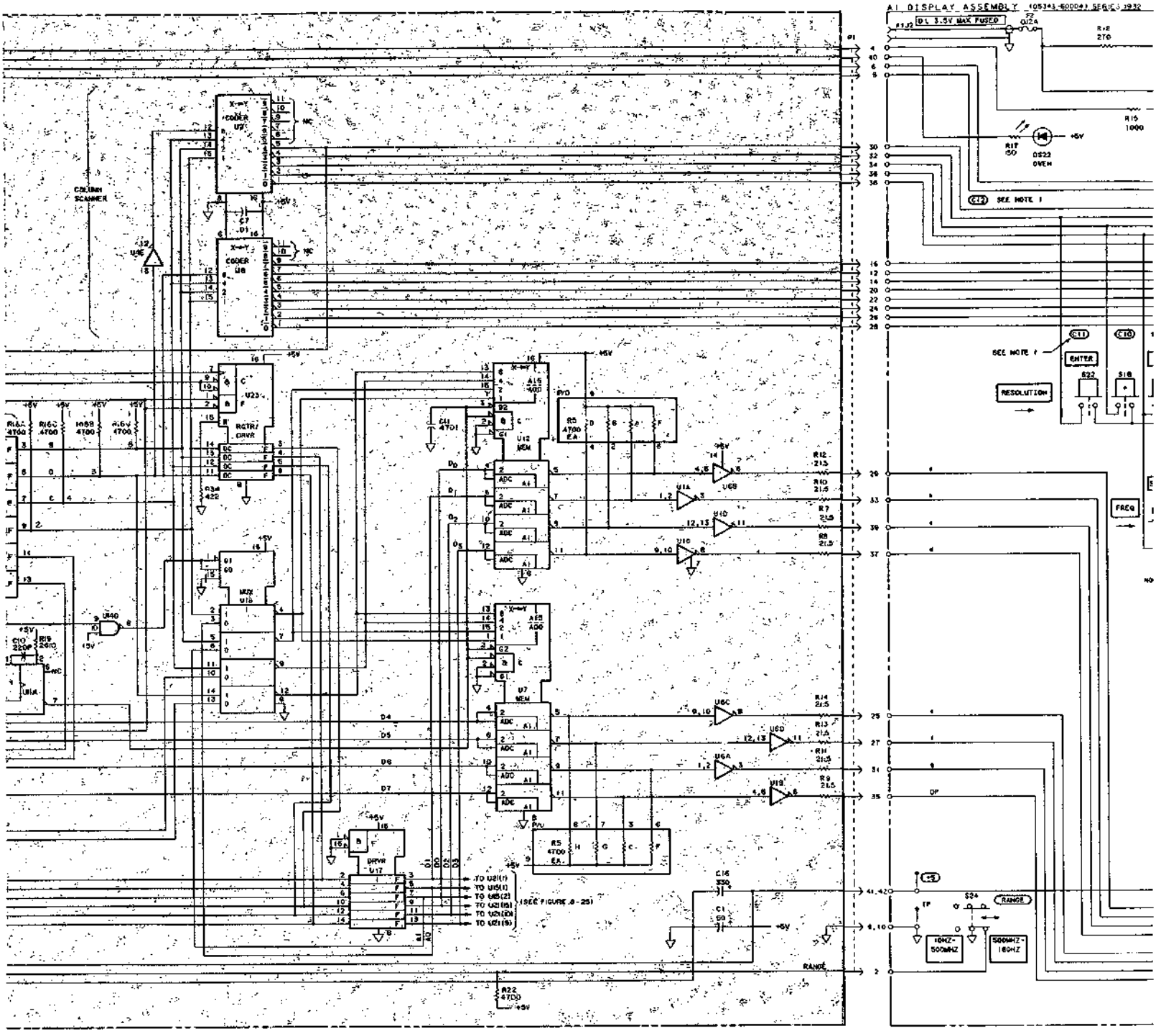
Deleted: DS9

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
A1Q1-Q13	1853-0318	MPS6562
A2		
U1, U6	1820-0539	SN7437N
U2, U8	1820-0468	SN7445N
U3	1820-1443	SN74LS293N
U4	1820-1416	SN74LS14N
U5	1820-1049	DM8097N
U7, U12	1820-0628	DM7489N
U9	1820-1144	9L302PC
U10	1820-1200	SN74LS05N
U11	1820-0515	9602PC
U13, U17	1820-1254	DM8095N
U14	1820-1197	SN74LS00N
U18	1820-1428	SN74LS158N
U19, U20	1820-1112	SN74LS74N
U23	1820-1885	DM74LS173N
A2 Option 004		
U15, U21, U22	1820-1194	SN74LS193N
U16	1820-1216	SN74LS128N
U24	1813-0092	DAC80-CCD-V







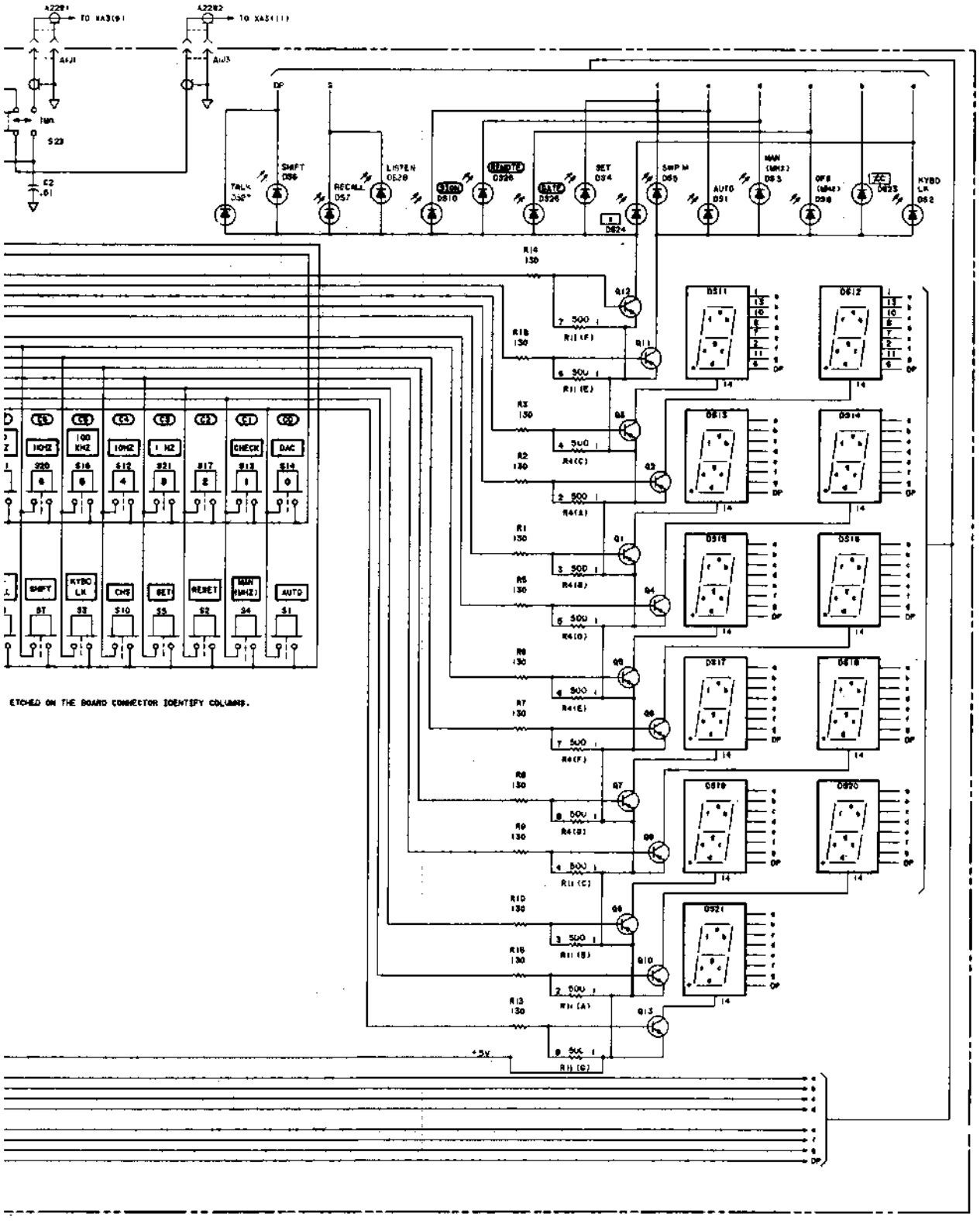


Figure 8-24. A1 Display Assembly and A2 Display Drive Assembly

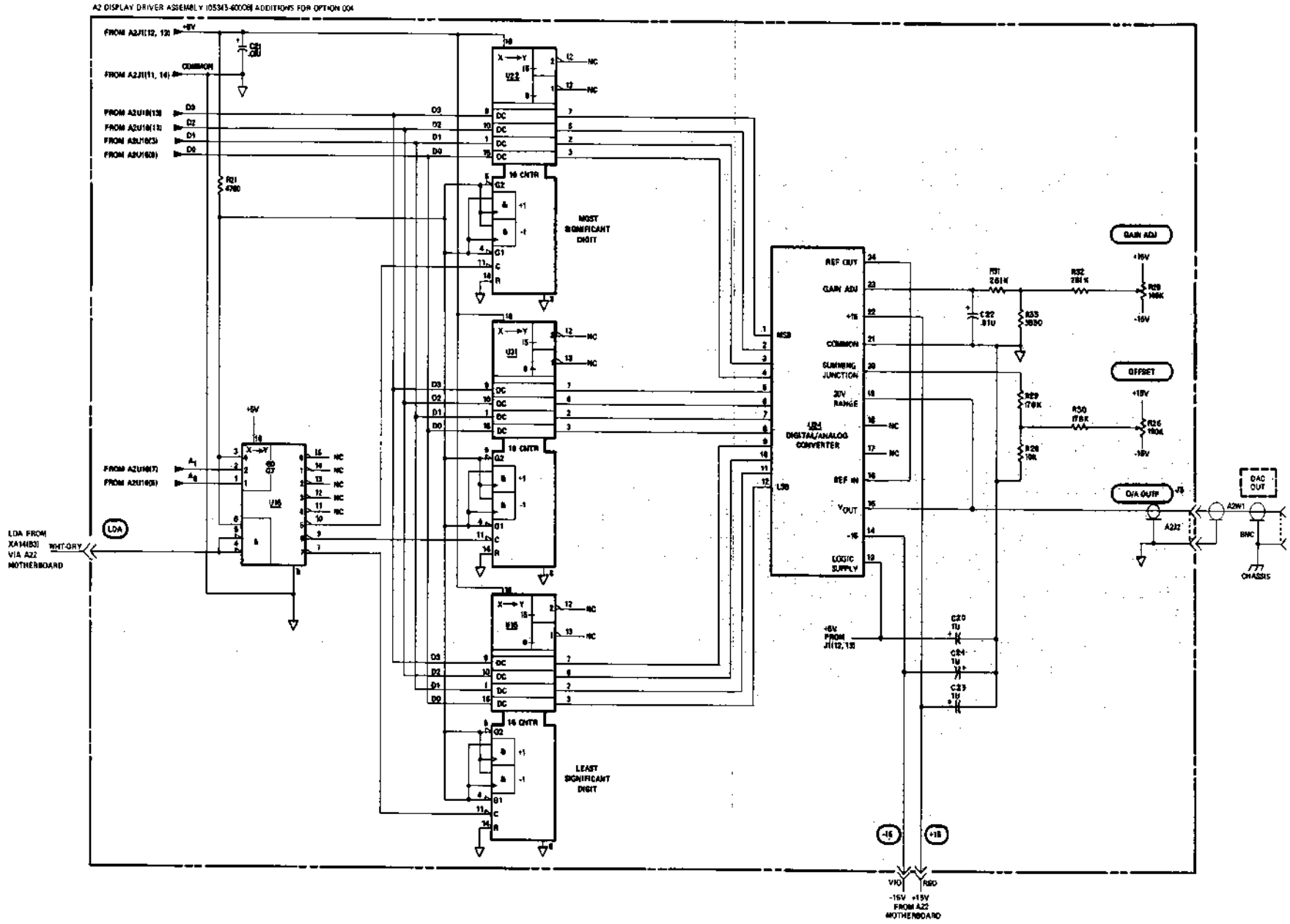
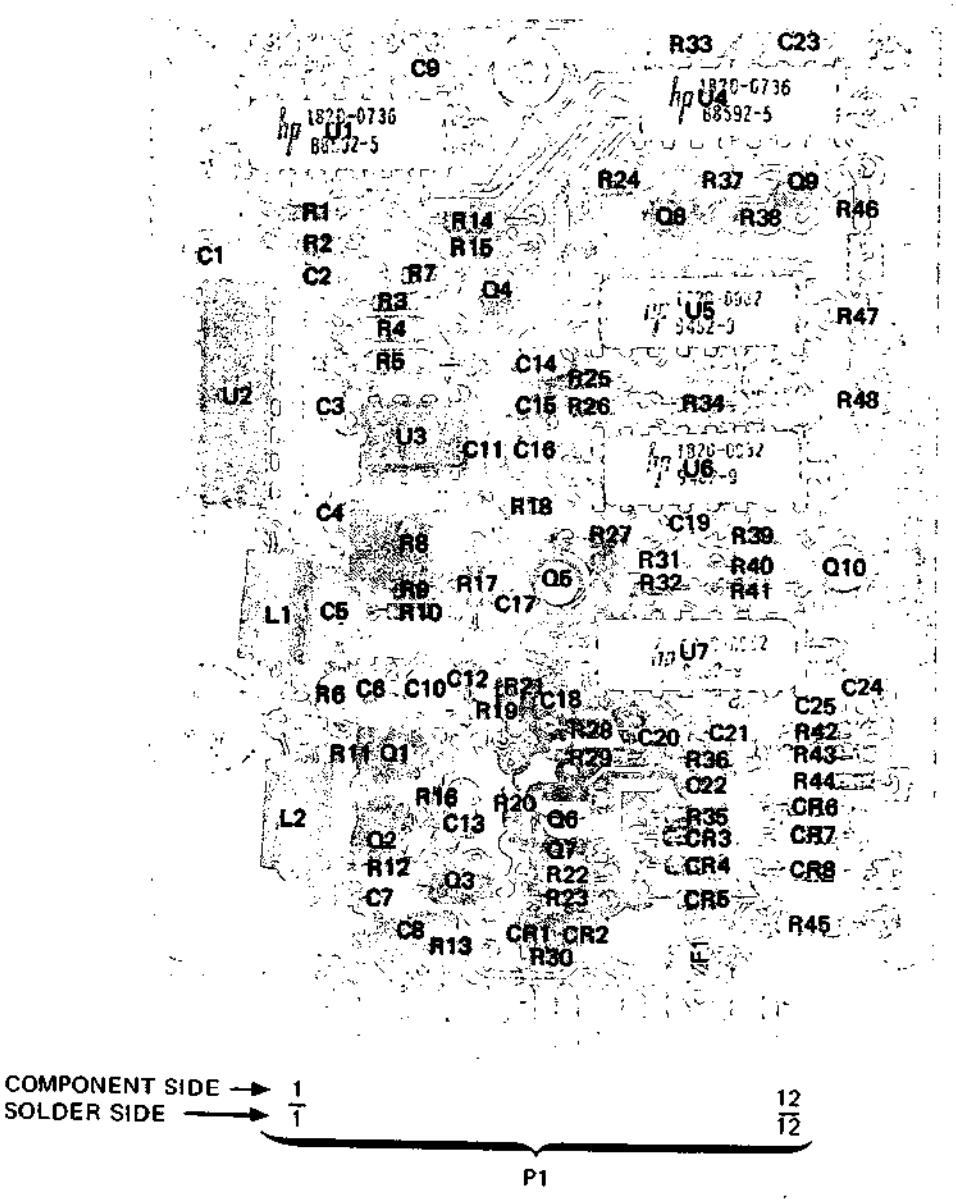


Figure 8-25. Option 004 Display Driver Additions on A2 Assembly



Part of Figure 8-26. A3 Direct Count Amplifier Assembly

A3 DIRECT COUNT AMPLIFIER

CONDITIONS: No signal input and A17 removed from instrument.

Q1		Q2		Q3		Q4		Q4		Q6	
E	-0.8	D	-0.09	D	+5	E	-1.2	E	-1.0	E	-5.15
B	-0.1	S	-5.0	S	-0.09	B	-1.9	B	-0.3	B	-4.4 (50Ω); -5.1 (1 MΩ)
C	+5	G	-5.15	G	+0.0	C	-5.15	C	+0.0	C	-5.1 (50Ω); -2.9 (1 MΩ)

Q7		Q8		Q9		Q10	
E	-5.15	E	-0.7	E	-0.7	E	-1.7
B	-5.1 (50Ω);-4.5 (1 MΩ)	B	-0.72	B	-0.04	B	-1.0
C	-2.9 (50Ω); -5.1 (1 MΩ)	C	-0.0	C	-0.54	C	-0.3

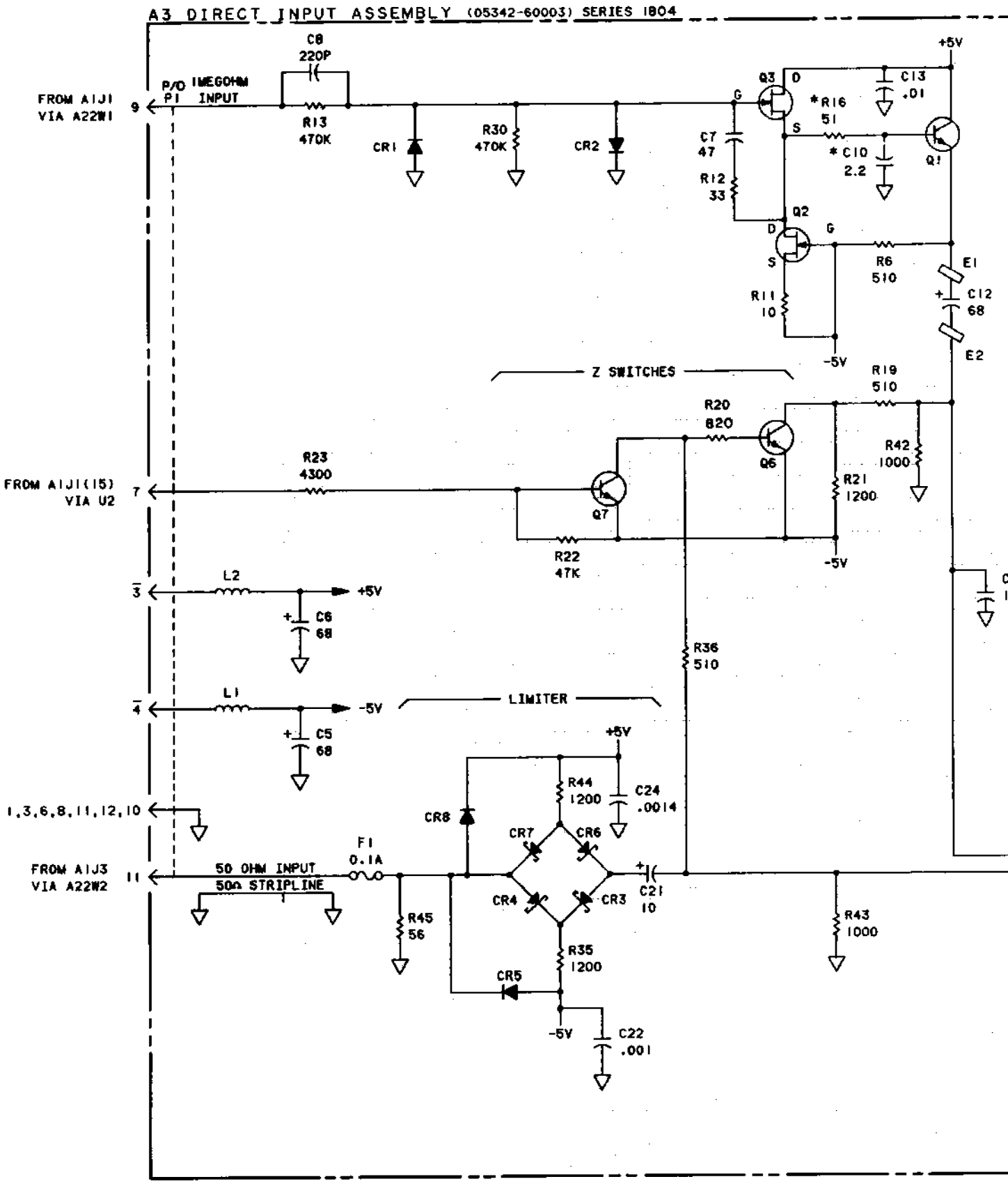
U3		U5		U6		U7	
1	+0.27 (50Ω); +1.23 (1 MΩ)	1	-5.15	1	-5.15	1	5.15
2	-0.37	2	-0.64	2	-0.33	2	-1.93 (50E); -1.88 (1 MΩ)
3	-0.37	3	-0.64	4	-0.37	3	-0.00
4	-5.15	4	-0.64	7	-5.11	4	-1.74
5	-1.4	5	0.0	8	-0.34	5	-1.74
6	-1.3	6	0.0			5	-1.75
7	+4.5	7	-1.8			6	-0.00
8	+5.0	8	0.37			7	-1.9 (50Ω); -3.3 (1 MΩ)
						8	-3.3 (50Ω); -1.9 (1 MΩ)

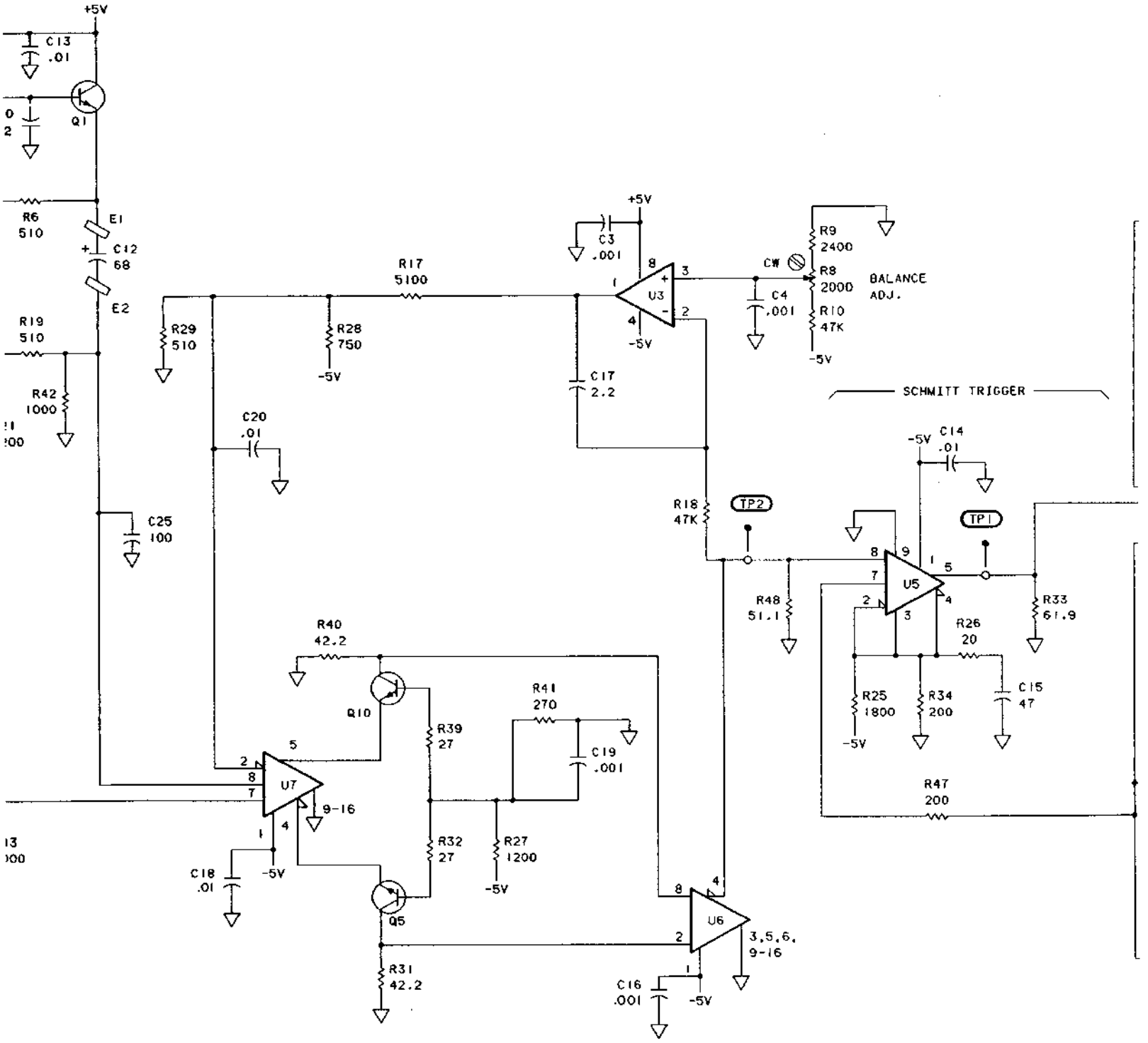
REFERENCE DESIGNATIONS

A3
C1-C25
CR1-CR8
E1, E2
F1
L1, L2
Q1-Q10
R1-R48
U1-U7

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFG OR INDUSTRY PART NUMBER
CR1, CR2	1901-0040	Same
CR6, CR7	1901-0535	Same
CR5, CR8	1901-0050	Same
Q1	1854-0215	SPS3411
Q2, Q3	1855-0081	2N5245
Q4	1853-0015	Same
Q5, Q10	1854-0546	Same
Q6, Q7, Q8, Q9	1854-0071	Same
U1, U4	1820-0736	Same
U2	1820-1224	MC10214P
U3	1826-0139	MC1458P1
U5, U6, U7	1820-0982	Same





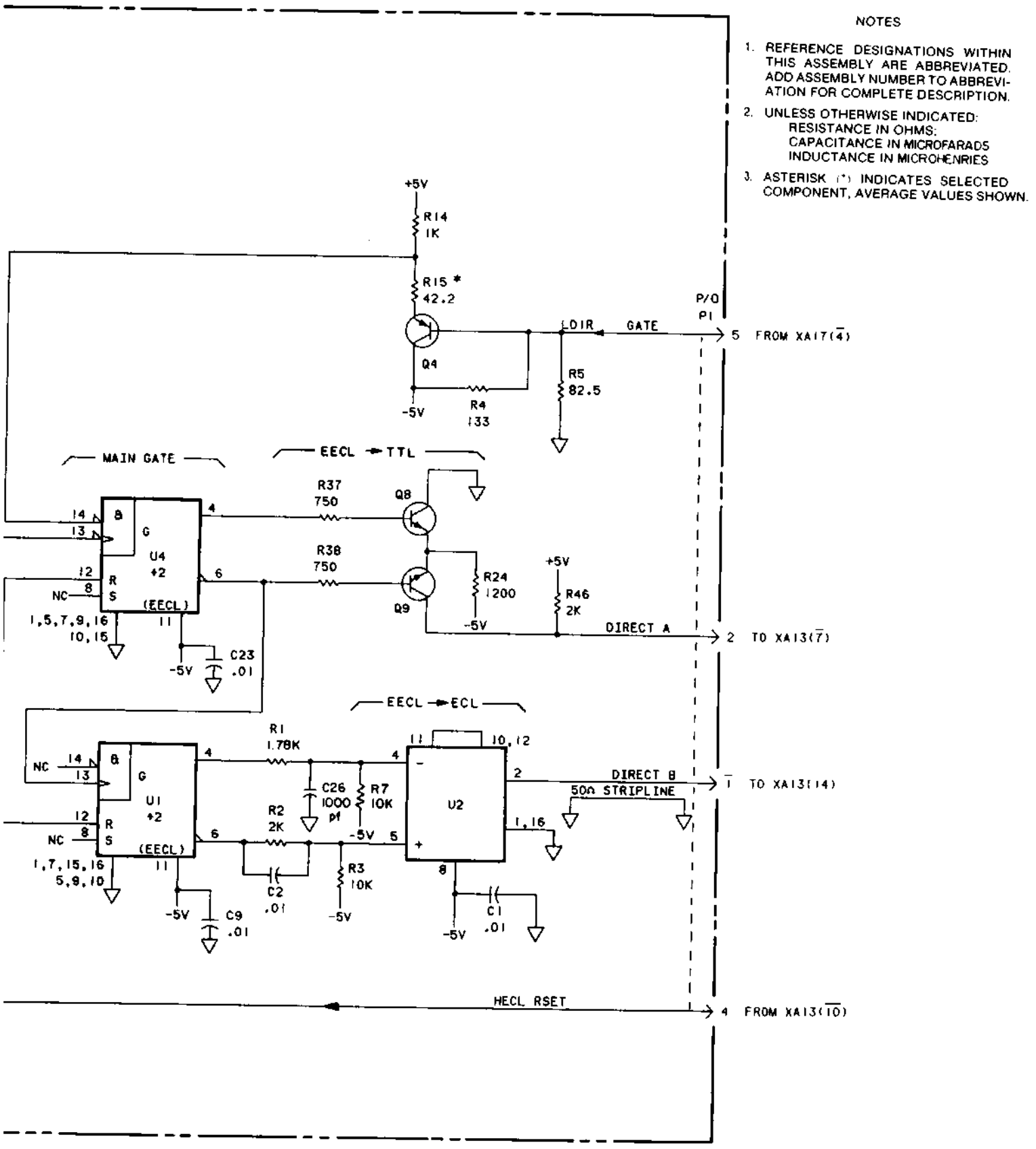
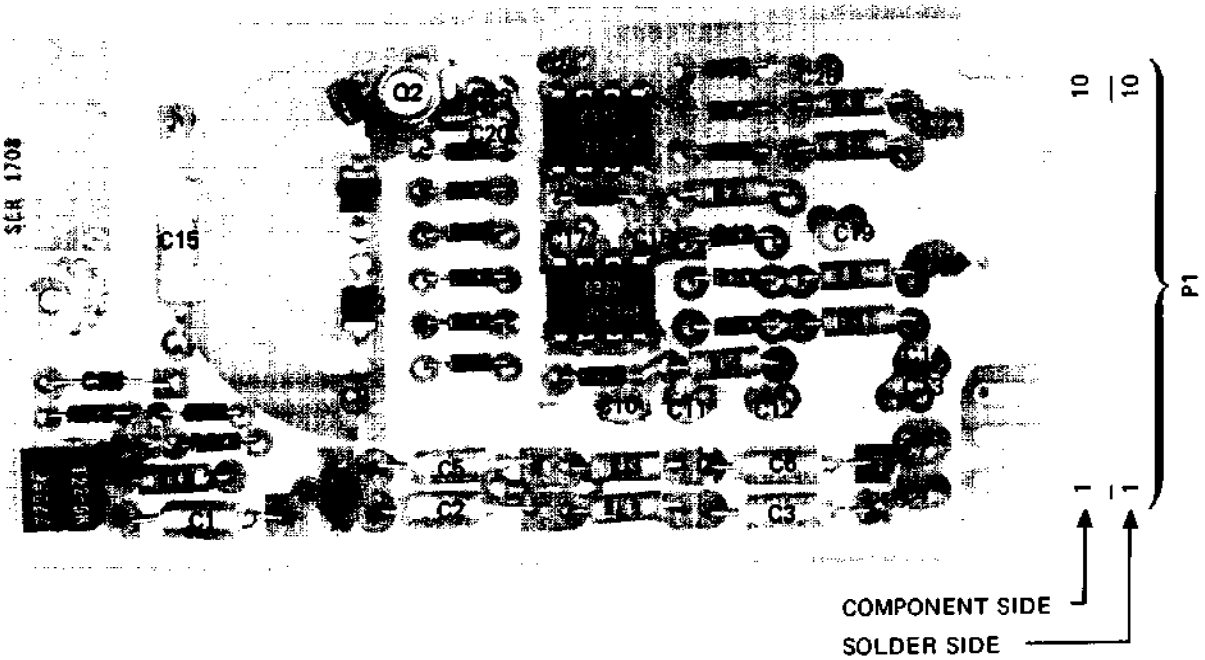


Figure 8-26. A3 Direct Count Amplifier Assembly



Part of Figure 8-27. A4 Offset VCO Assembly

A4 OFFSET VCO ASSEMBLY

CONDITIONS: No signal input, 5343A in CHECK mode.
Junction of varactors CR2 to CR3, V = +1.4 in CHECK mode.

Q1		Q2		U1		U2	
E	+8.0	E	+3.0	1	-0.02	1	-0.03
B	+8.6	B	+3.5	3	-2.27	3	-3.02
C	+15.1	C	+7.5	5	+4.0	5	+3.55
				7	+4.83	7	+4.78
				8	+4.02	8	+3.67

REFERENCE DESIGNATIONS

A4
C1-C25
CR1-CR3
E1
L1-L9
Q1, Q2
R1-R18
U1, U2

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1	1902-3171	FZ7264
CR2, CR3	0122-0065	Same
Q1	1854-0071	Same
Q2	1854-0345	2N5179
U1, U2	1826-0732	Same

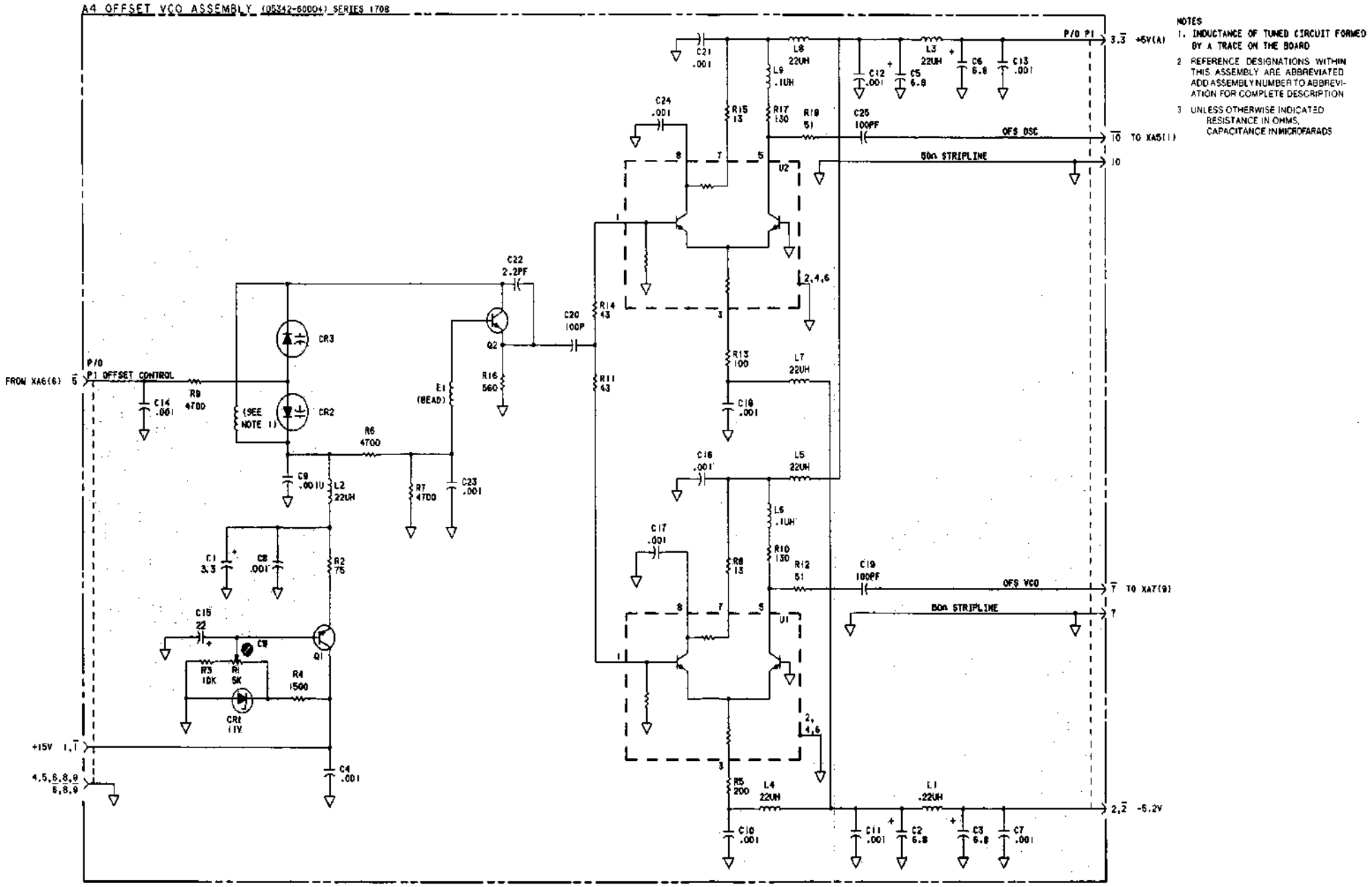
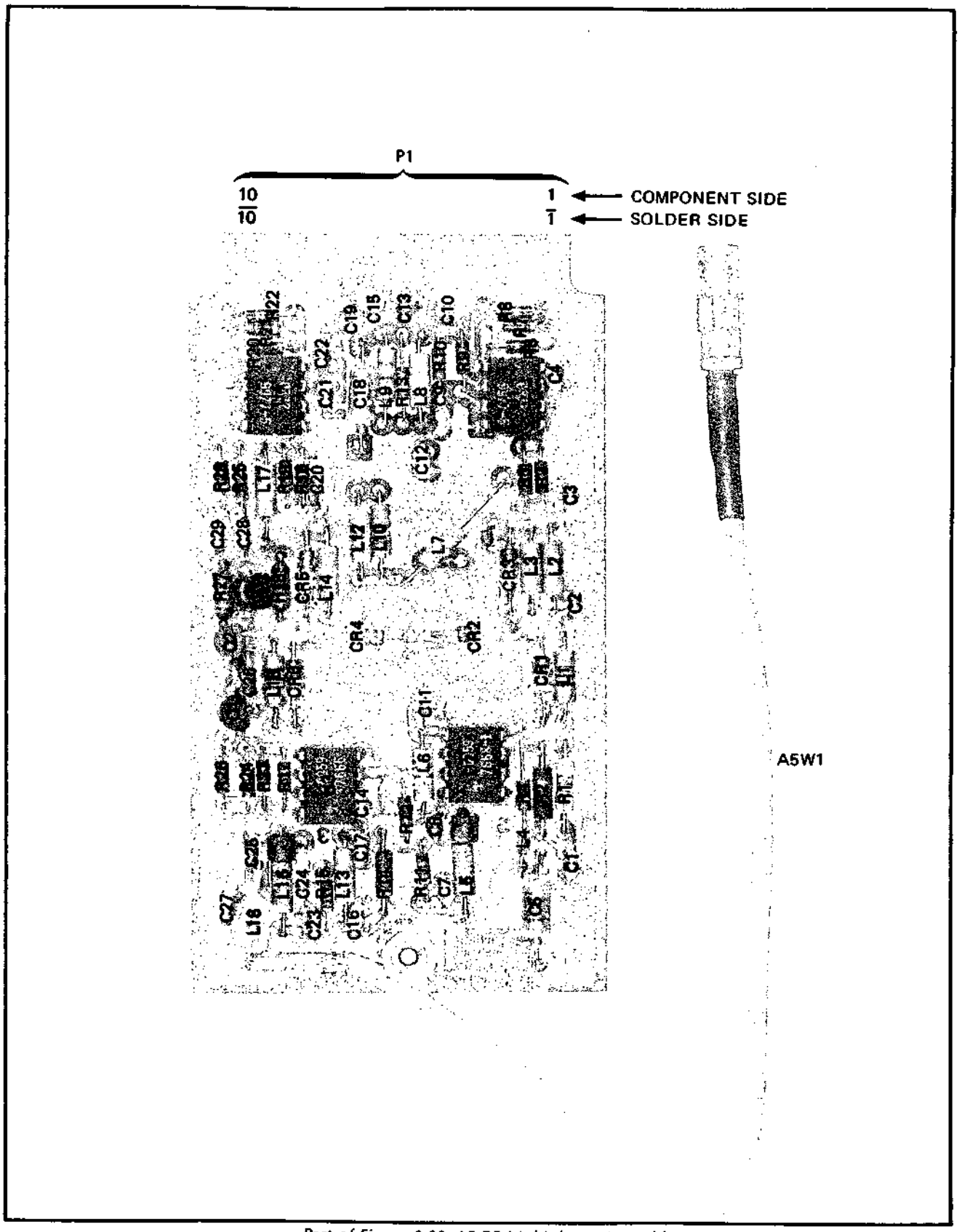


Figure 8-27. A4 Offset VCO Assembly



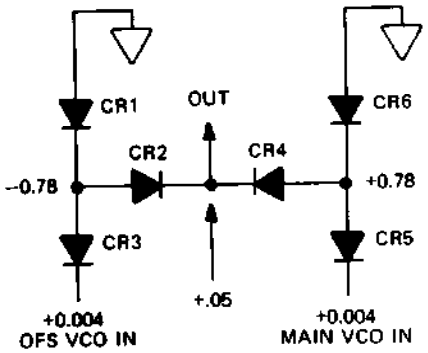
Part of Figure 8-28. A5 RF Multiplexer Assembly

A5 RF MULTIPLEXER ASSEMBLY

CONDITIONS: 5343A in CHECK mode. Disconnect A5W1 from A26J2.

U1		U2		U3		U4		Q1		Q2		Q3	
1	0.0	1	0.0	1	-0.74	1	0.0	E	+3.56	E	+2.2	E	+2.2
3	-2.36	2	-0.68	2	-0.74	3	-2.36	B	+2.85	B	+1.50	B	+3.6
5	+3.91	3	-0.68	3	-0.74	5	+3.91	C	+2.2	C	+0.82	C	-0.8
7	+4.58	3	-0.68	3	-0.74	7	+4.58						
8	+3.85	4	+0.05	4	0.0	8	+3.84						
		5	+4.38	5	+4.2								
		8	+4.38										

DIODE SWITCH SIMPLIFIED DRAWING



REFERENCE DESIGNATIONS

A5
C1-C29
CR1-CR6
E1, E2
L1-L18
Q1-Q3
R1-R28
U1-U4
W1

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1-CR6	1901-0179	Same
Q1-Q3	1853-0058	832248
U1, U4	1826-0372	Same
U2, U3	1858-0059	Same

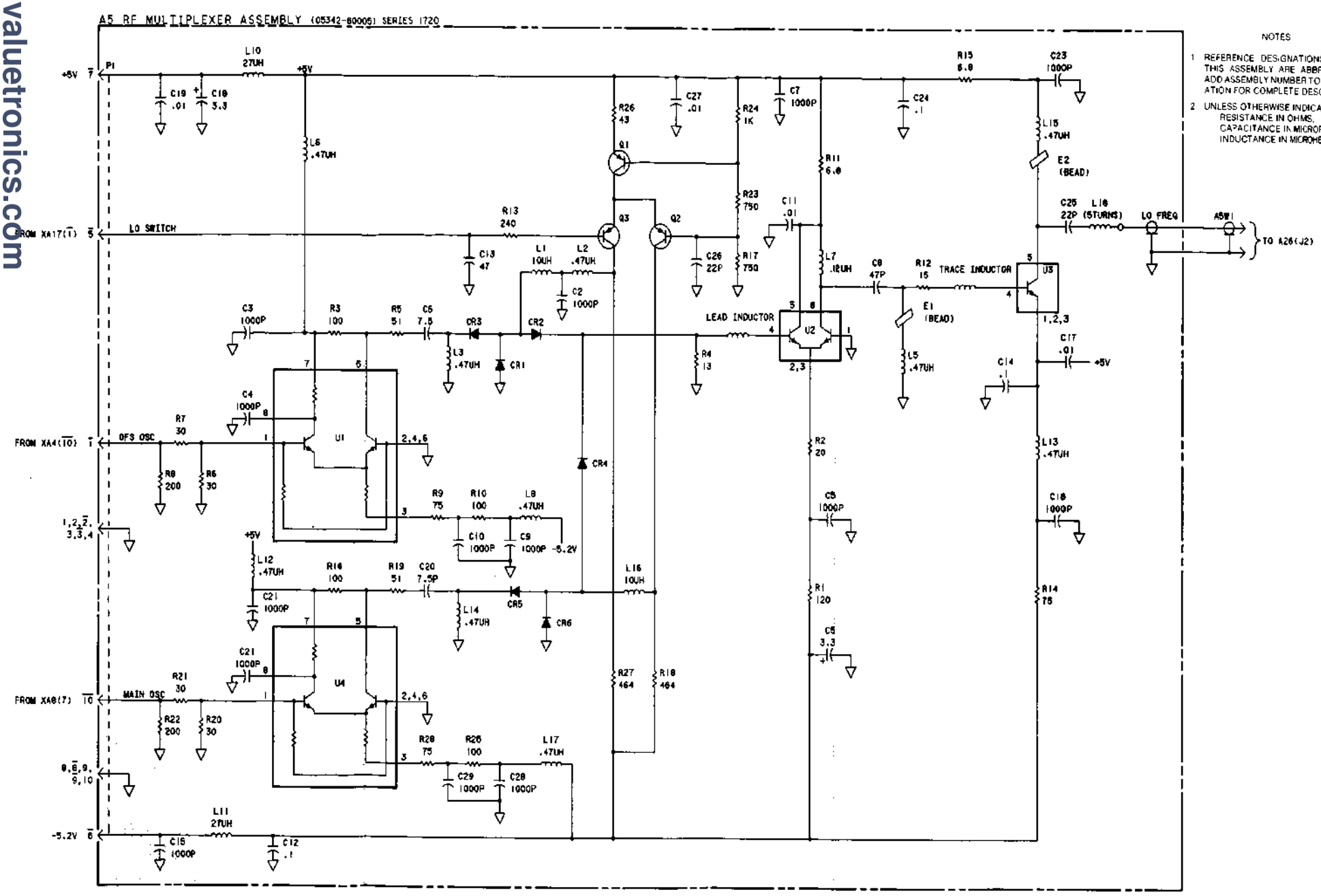
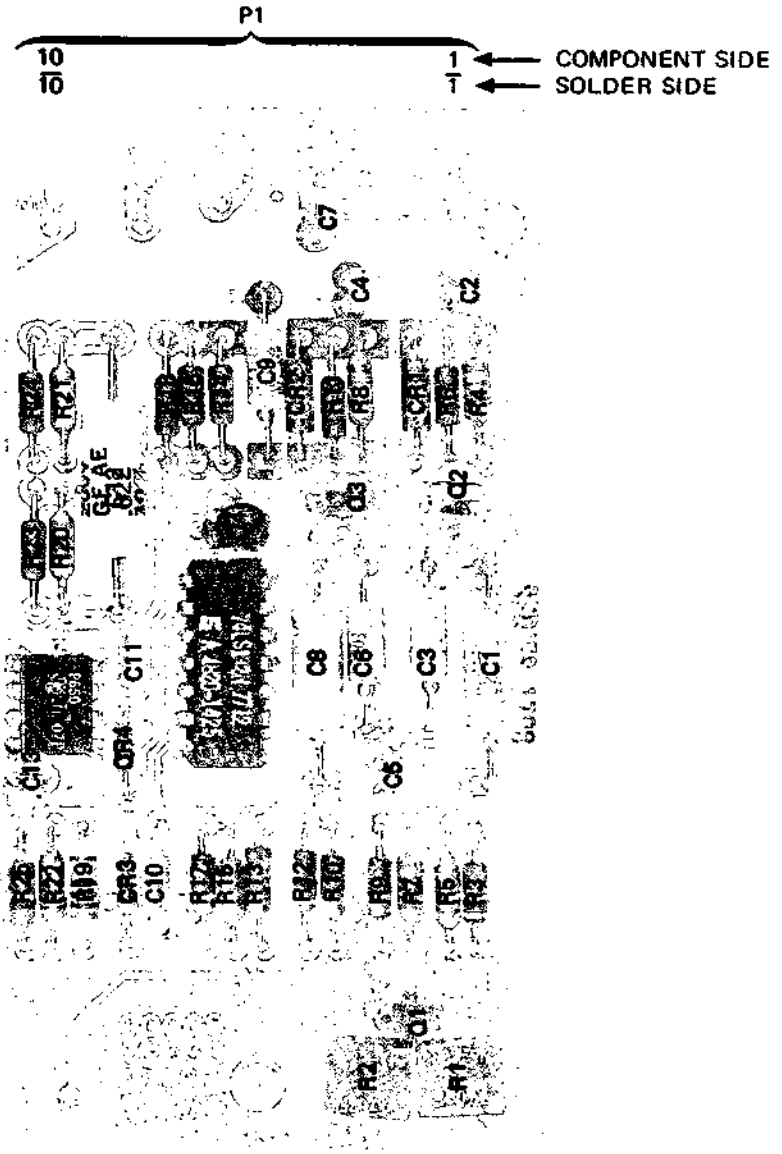


Figure 8-28. A5 RF Multiplexer Assembly



Part of Figure 8-29. A6 Offset Loop Amp/Search Generator Assembly

A6 OFFSET LOOP AMPLIFIER ASSEMBLY

CONDITIONS: No signal input, 5343A in CHECK mode.

Q1		Q2		Q3		Q4		U2	
E	+1.3	E	+12.4	E	-12.1	E	+5.05	2	+1.6
B	+0.7	B	+13.0	B	-12.8	B	+5.3	3	+1.6
C	-11.0	C	+15.1	C	-14.7	C	0.0	4	-12.1
								6	+1.9
								7	+12.4

NOTE
Junction of CR4, CR3:+1.58V

CONDITIONS: A7 Assembly removed; 5343A in CHECK mode.

Q4		U2	
E	+5.05	2	+1.54
B	+4.42	3	+1.58
C	+4.37	4	-12.1
		6	+0.15
		7	+12.4

NOTE
Junction of CR4, CR3: +1.54

REFERENCE DESIGNATIONS

A6
C1-C13
CR1-CR4
Q1-Q4
R1-R25
U1, U2

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1, CR2	1902-3193	F27272
CR3, CR4	1901-0040	Same
Q1, Q3, Q4	1853-0020	Same
Q2	1854-0071	Same
U1	1820-1425	SN74LS132N
U2	1820-0493	LM307N

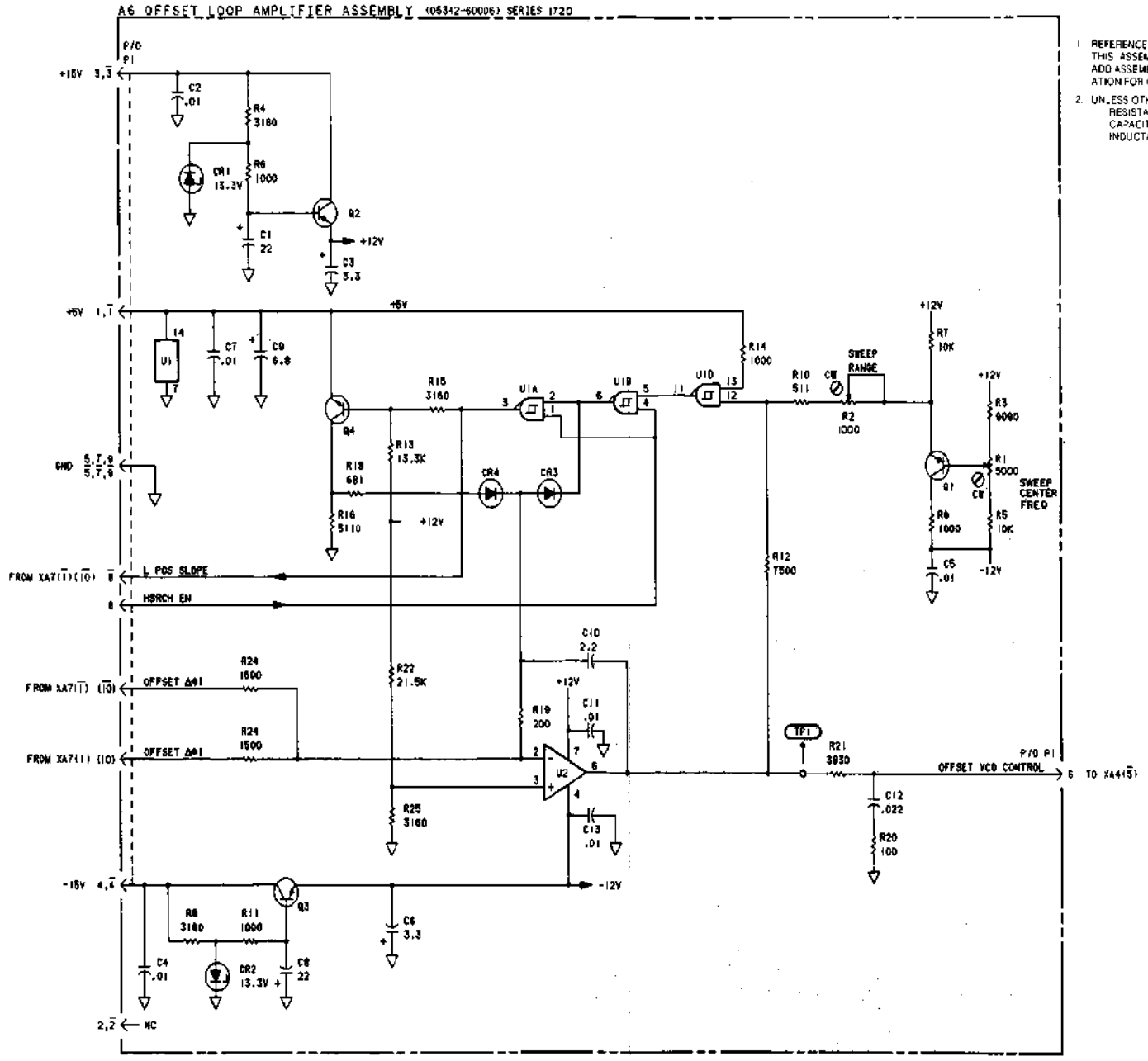
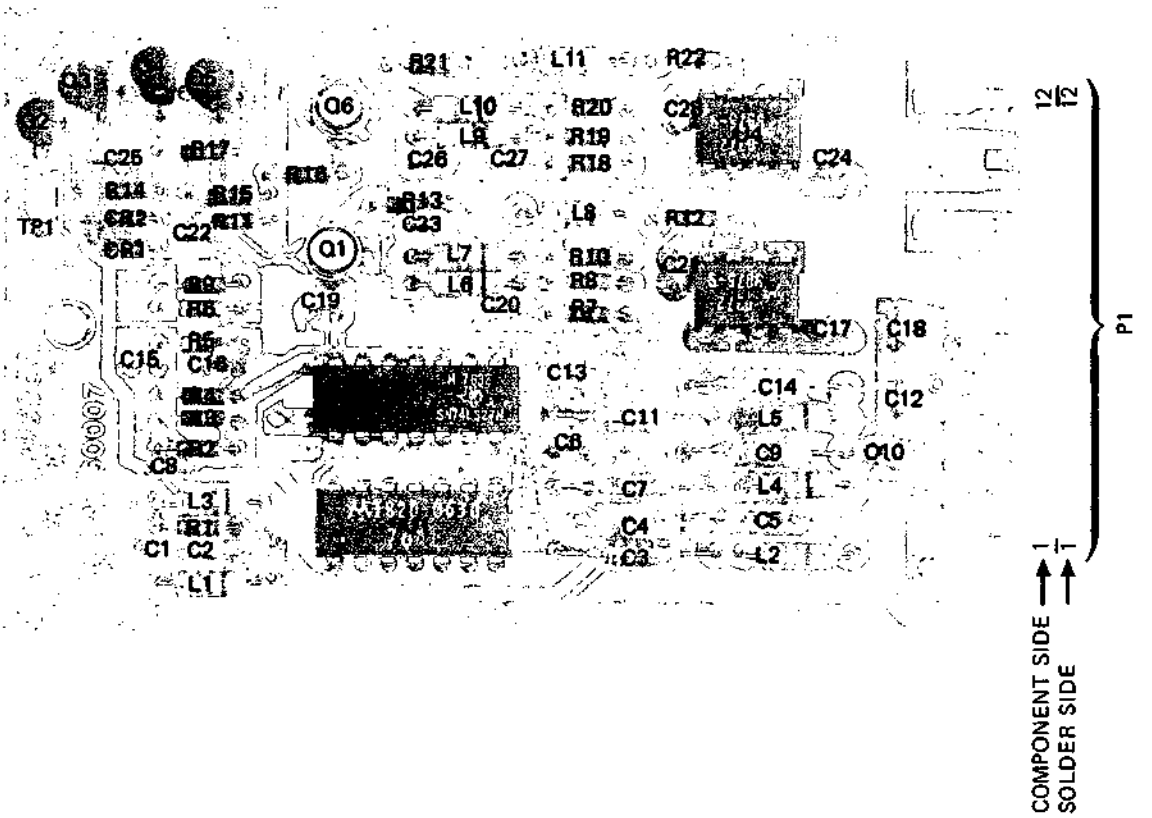


Figure 8-29. A6 Offset Loop Amp/Search Generator Assembly



Part of Figure 8-30. A7 Mixer/Search Control Assembly

A7 MIXER/SEARCH CONTROL ASSEMBLY

CONDITIONS: A4 and A8 VCO assemblies removed from instrument.

U3		U4		Q1		Q2		Q3		Q4		Q5		Q6	
1	-0.01	1	-0.01	E	-0.75	E	0.0	E	-1.3	E	-0.7	E	0.0	E	-0.7
3	-2.4	3	-.35	B	-0.00	B	-0.5	B	-0.6	B	-0.1	B	-0.6	B	0.0
5	+3.8	5	+3.1	C	-0.5	C	+4.8	C	+4.8	C	+4.8	C	4.8	C	0.0
7	+4.7	7	+4.6												
8	+4.1	8	+3.5												

CONDITIONS: 5343A in CHECK mode

NOTE — U3 and U4 voltages approximately the same as with VCO's removed.

Q1		Q2		Q3		Q4		Q5		Q6	
E	-0.5	E	0.0	E	-1.3	E	+2.8	E	0.0	E	-0.5
B	-0.0	B	+0.36	B	-0.6	B	+3.4	B	+0.7	B	-0.01
C	+0.7	C	+1.7	C	+4.8	C	-4.8	C	+0.02	C	0.0

REFERENCE DESIGNATIONS

A7
C1-C28
CR1, CR2
L1-L11
Q1-Q6
R1-R22
TP1
U1-U14

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1, CR2	1901-0518	Same
Q1, Q6	1854-0345	2N5179
Q2, Q3	1854-0092	Same
Q4, Q5	1854-0071	Same

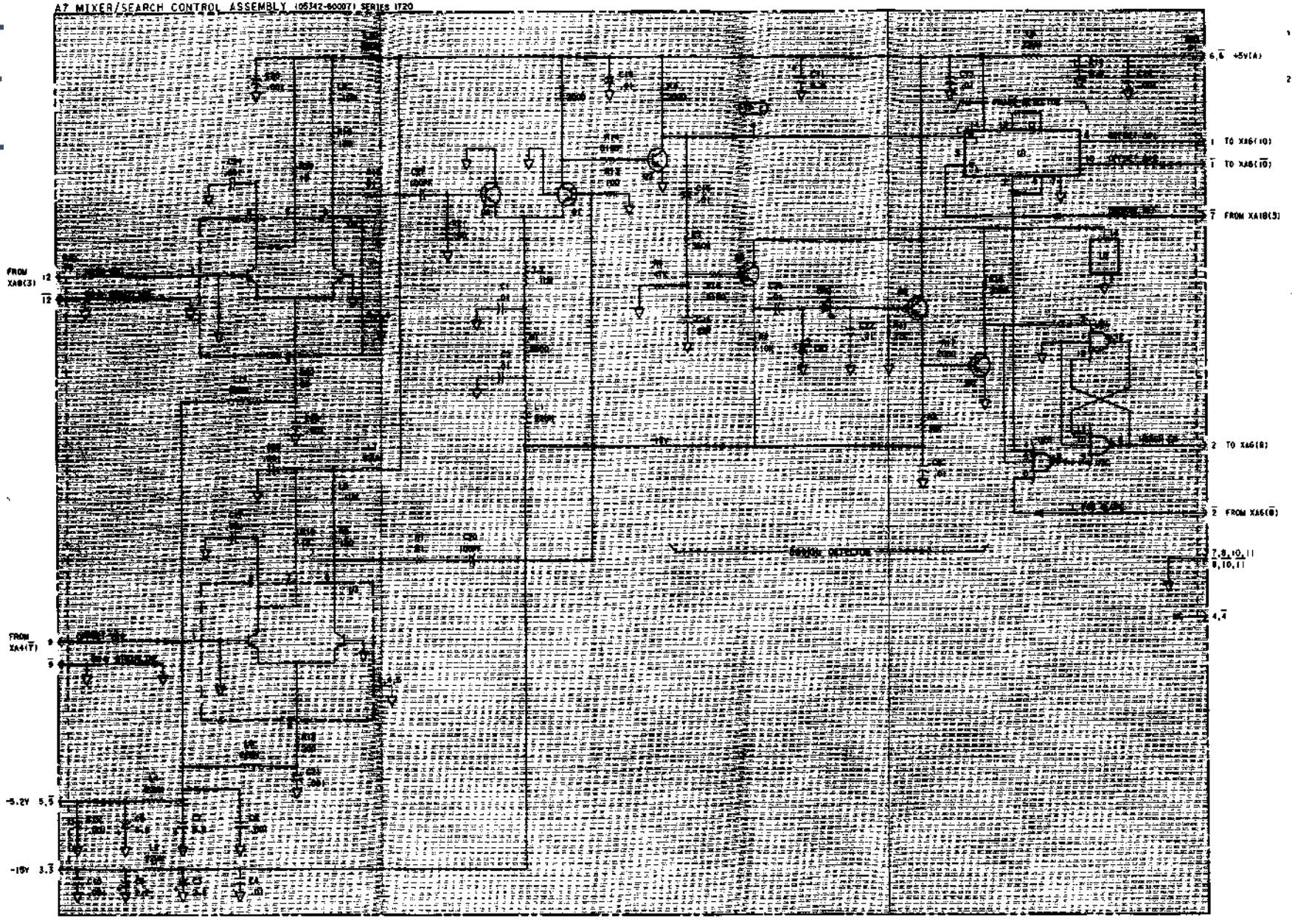
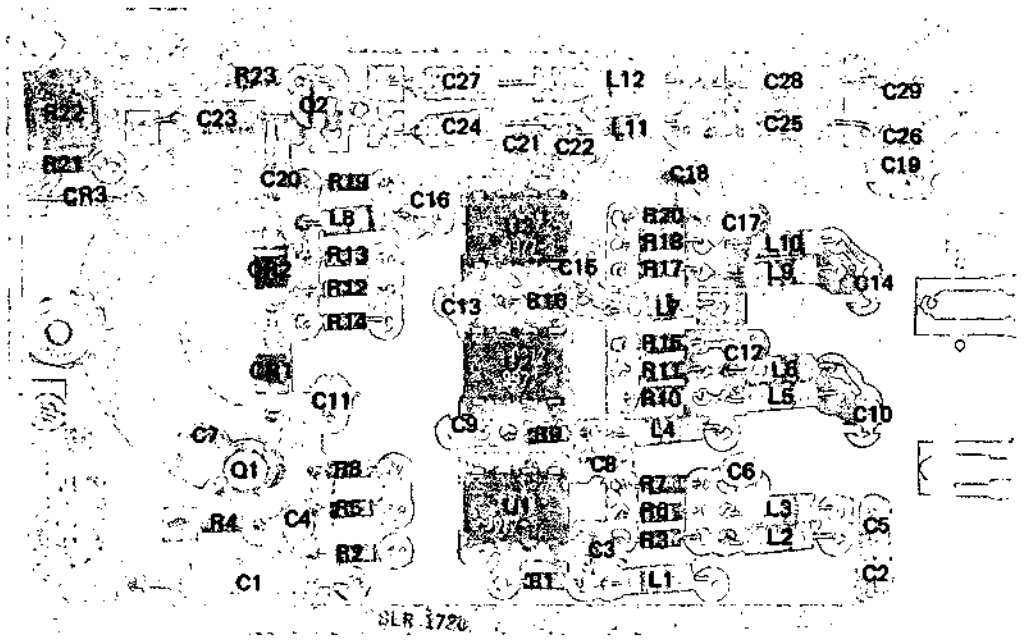


Figure 8-30. A7 Mixer/Search Control Assembly



Part of Figure 8-31. A8 Main VCO Assembly

A8 MAIN VCO ASSEMBLY

CONDITIONS: 5343A in CHECK mode.

Q1		Q2		U1		U2		U3	
E	+2.8	E	+7.5	1	-0.01	1	-0.02	1	-0.02
B	+3.4	B	+8.2	3	-2.3	3	-2.8	3	-3.0
C	+7.1	C	+15.1	5	+4.0	5	+3.7	5	+3.5
				7	+4.8	7	+4.7	7	+4.7
				8	+4.0	8	+3.7	8	+3.6

REFERENCE DESIGNATIONS

A8
C1-C29
CR1-CR3
E1
L1-L2
Q1, Q2
R1-R23
U1

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1, CR2	0122-0065	Same
CR3	1902-3171	F27264
Q1	1854-0071	Same
Q2	1854-0071	Same
U1	1826-0372	Same

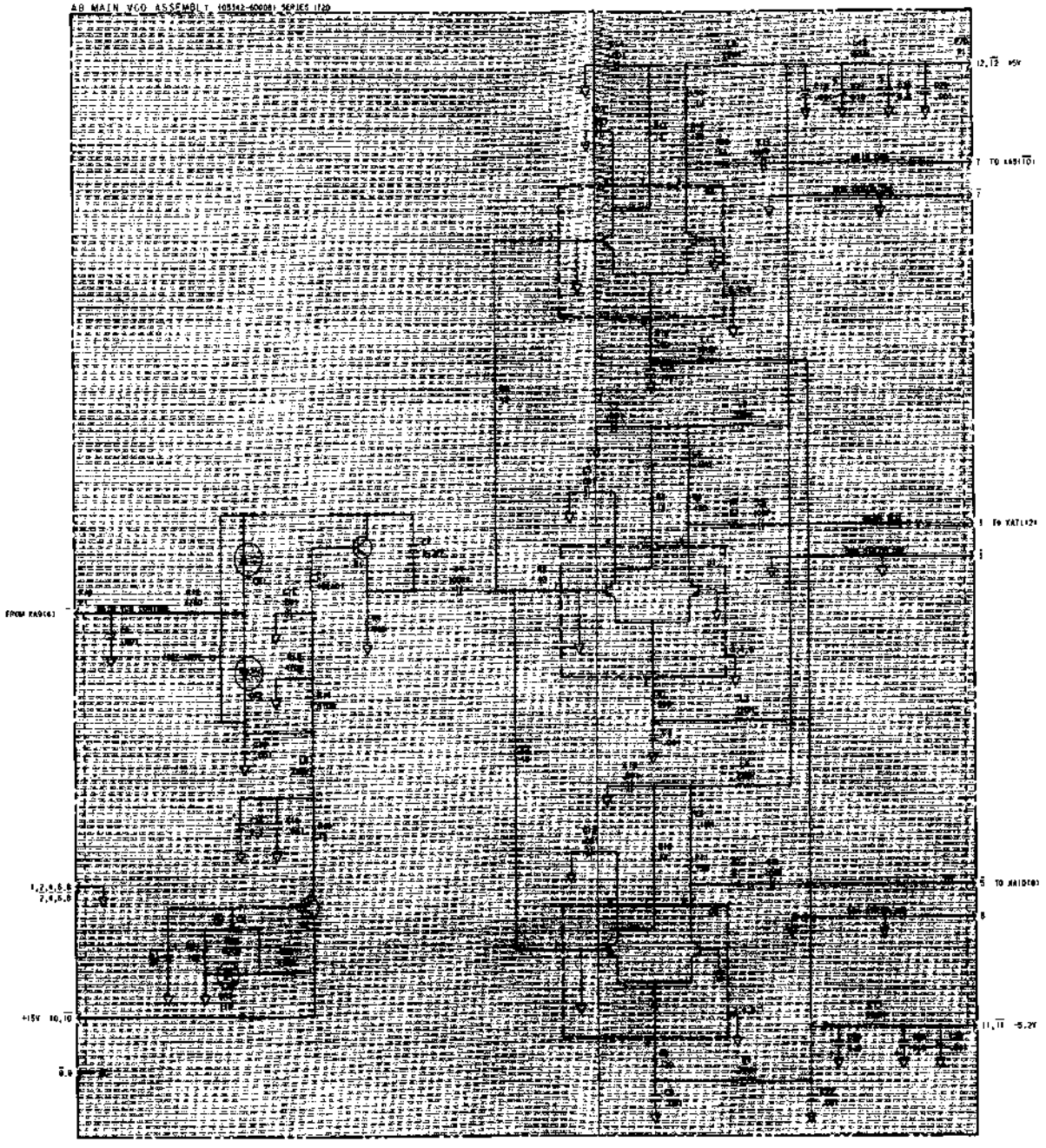
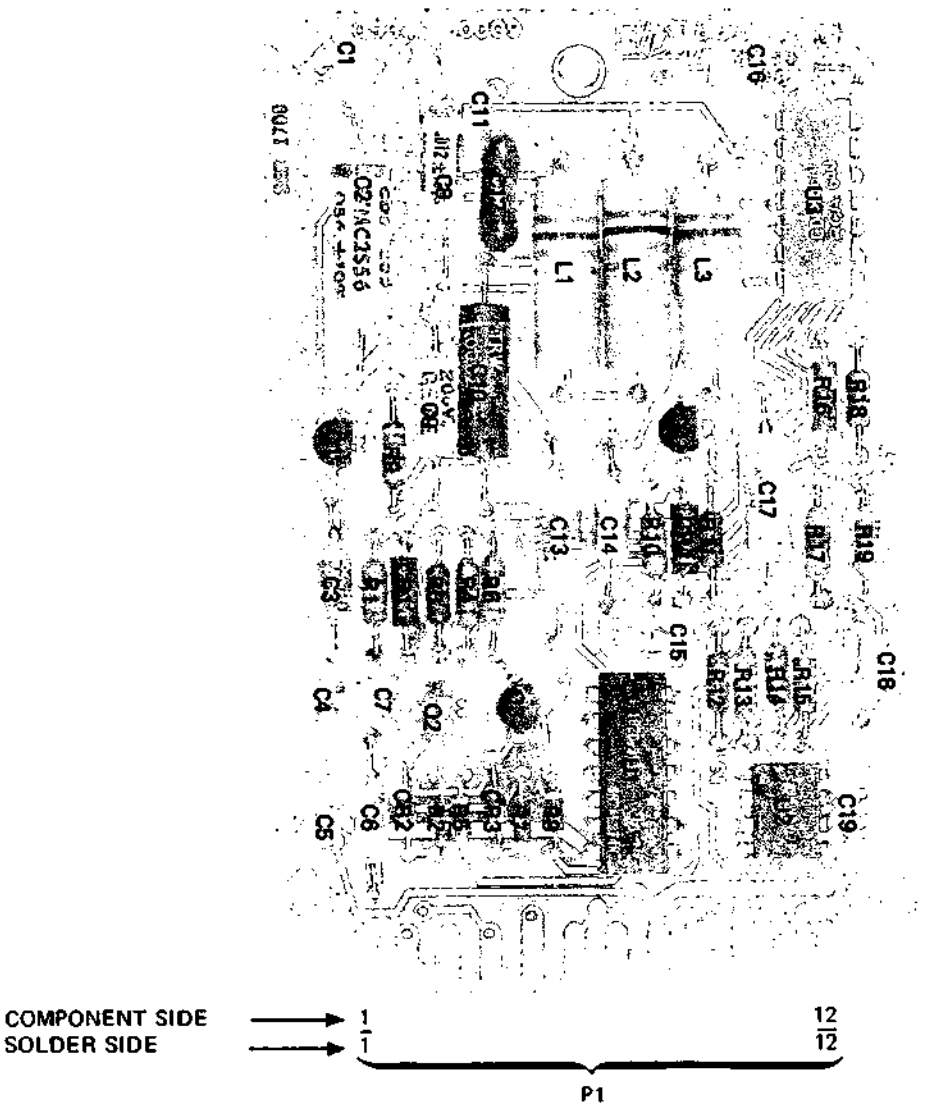


Figure 8-31. A8 Main VCO Assembly



Part of Figure 8-32. A9 Main Loop Amplifier Assembly

A9 MAIN LOOP AMPLIFIER ASSEMBLY

CONDITIONS: 5343A in CHECK mode.

Q1		Q2		Q3		Q4		U2	
E	-5.3	E	+5.7	E	+5.7	E	+5.7	2	+1.57
B	-5.9	B	+5.0	B	+6.2	B	+6.3	3	+1.58
C	-14.7	C	+5.7	C	-5.3	C	+15.1	6	+1.79

CONDITIONS: 5343A NOT in CHECK mode.

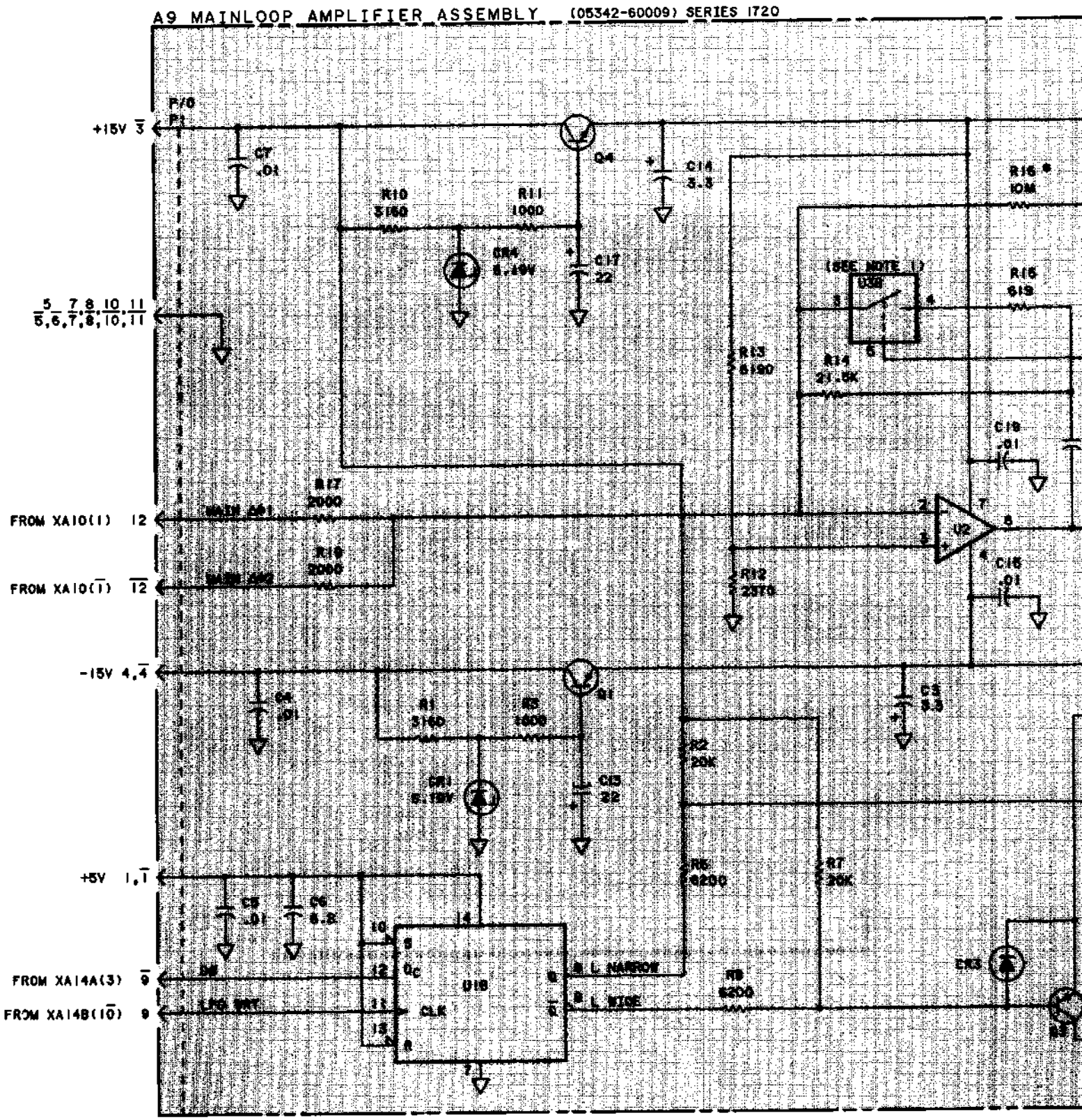
Q2		Q3	
E	+5.7	E	+5.7
B	+6.2	B	+5.0
C	-5.3	C	+5.7

REFERENCE DESIGNATIONS

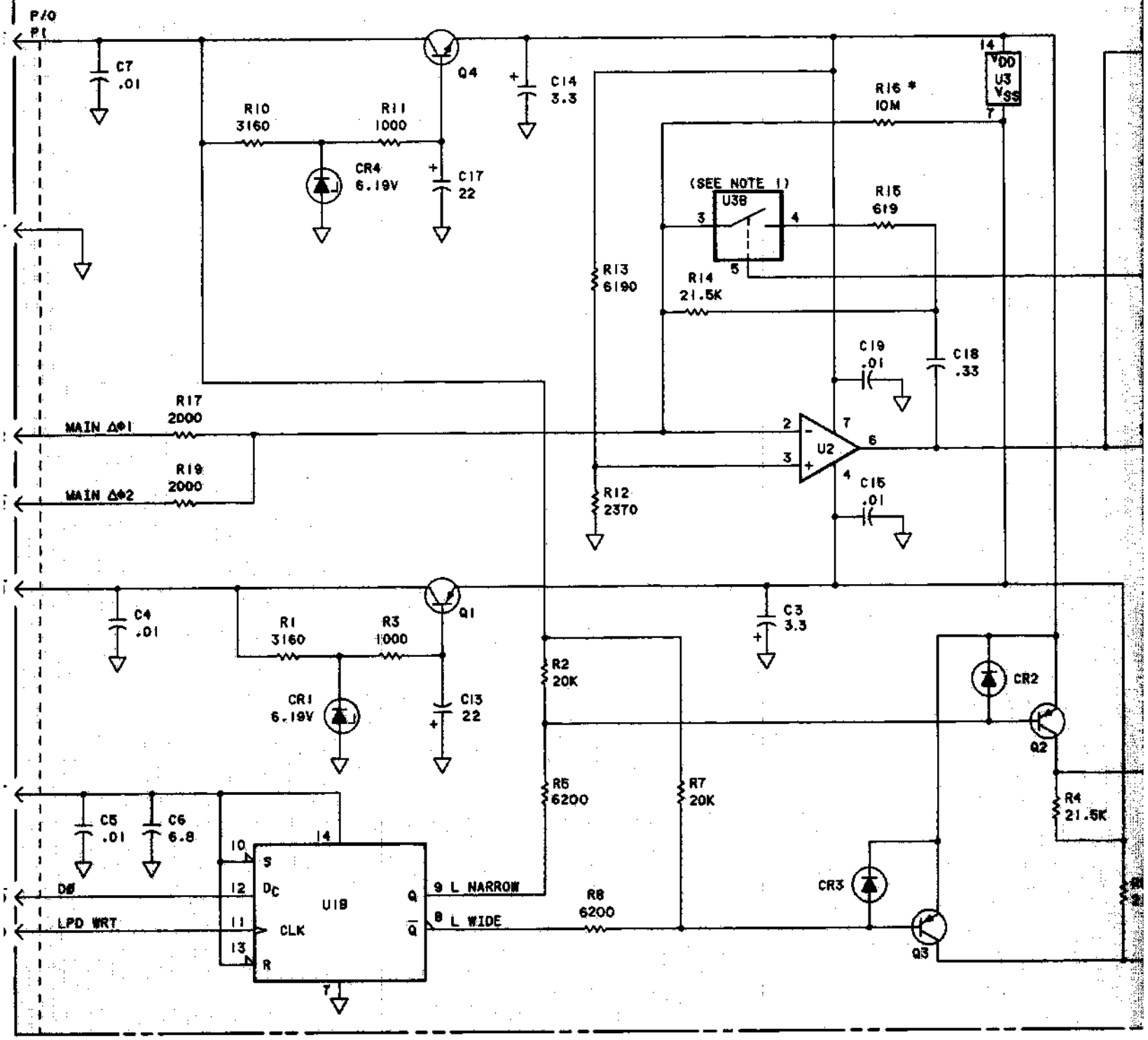
A9
C1-C19
CR1-CR4
L1-L3
Q1-Q4
R1-R19
TP1
U1-U3

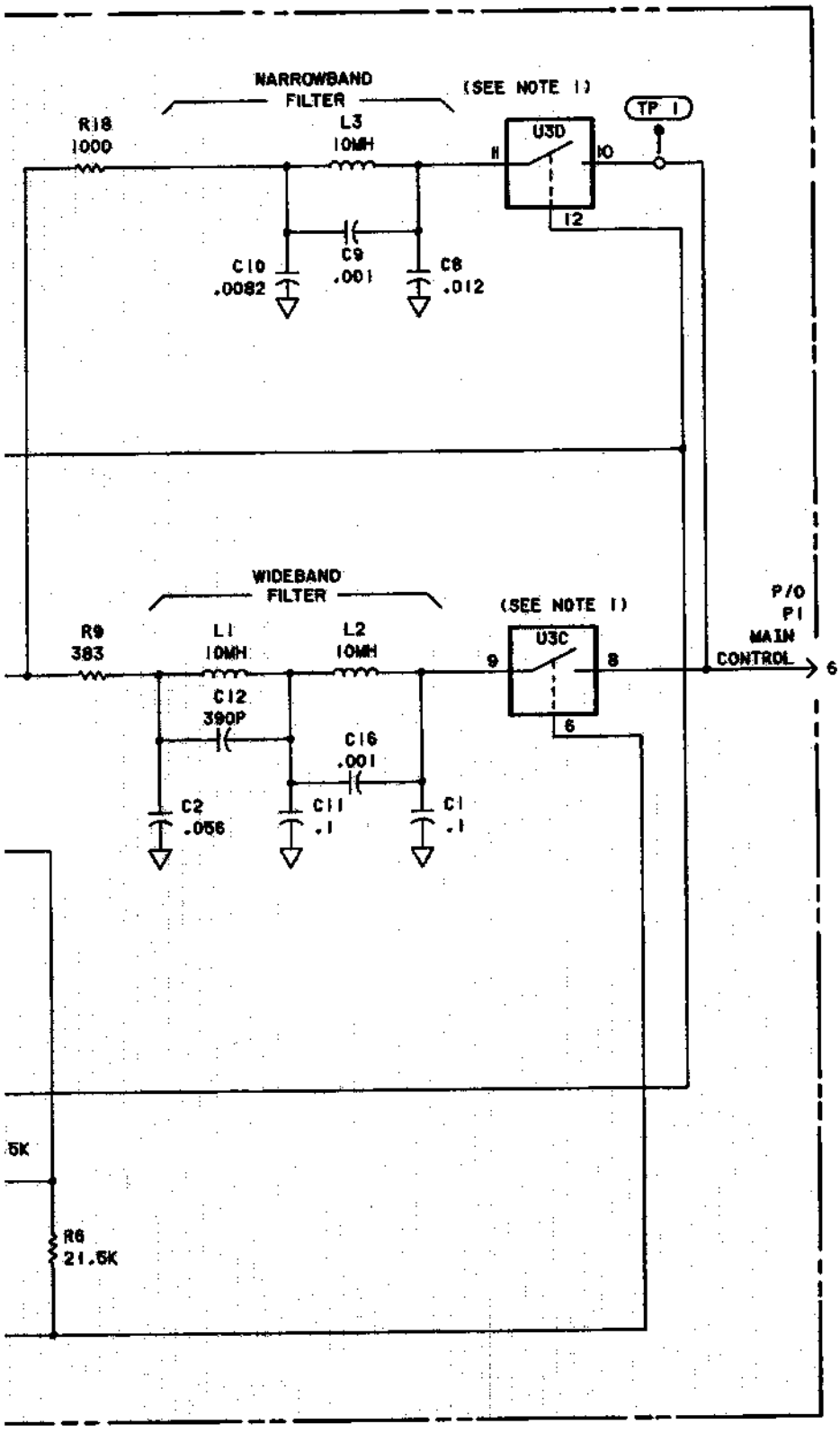
TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1, CR4	1902-0049	FZ7240
CR2, CR3	1901-0040	Same
Q1-Q3	1853-0020	Same
Q4	1854-0071	Same
U1	1820-1112	SN74LS74N
U2	1820-0493	LM307N
U3	1820-1325	CD4066AF



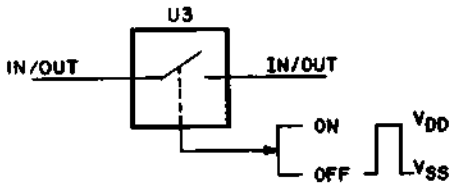
A9 MAINLOOP AMPLIFIER ASSEMBLY (05342-60009) SERIES 1720





NOTES

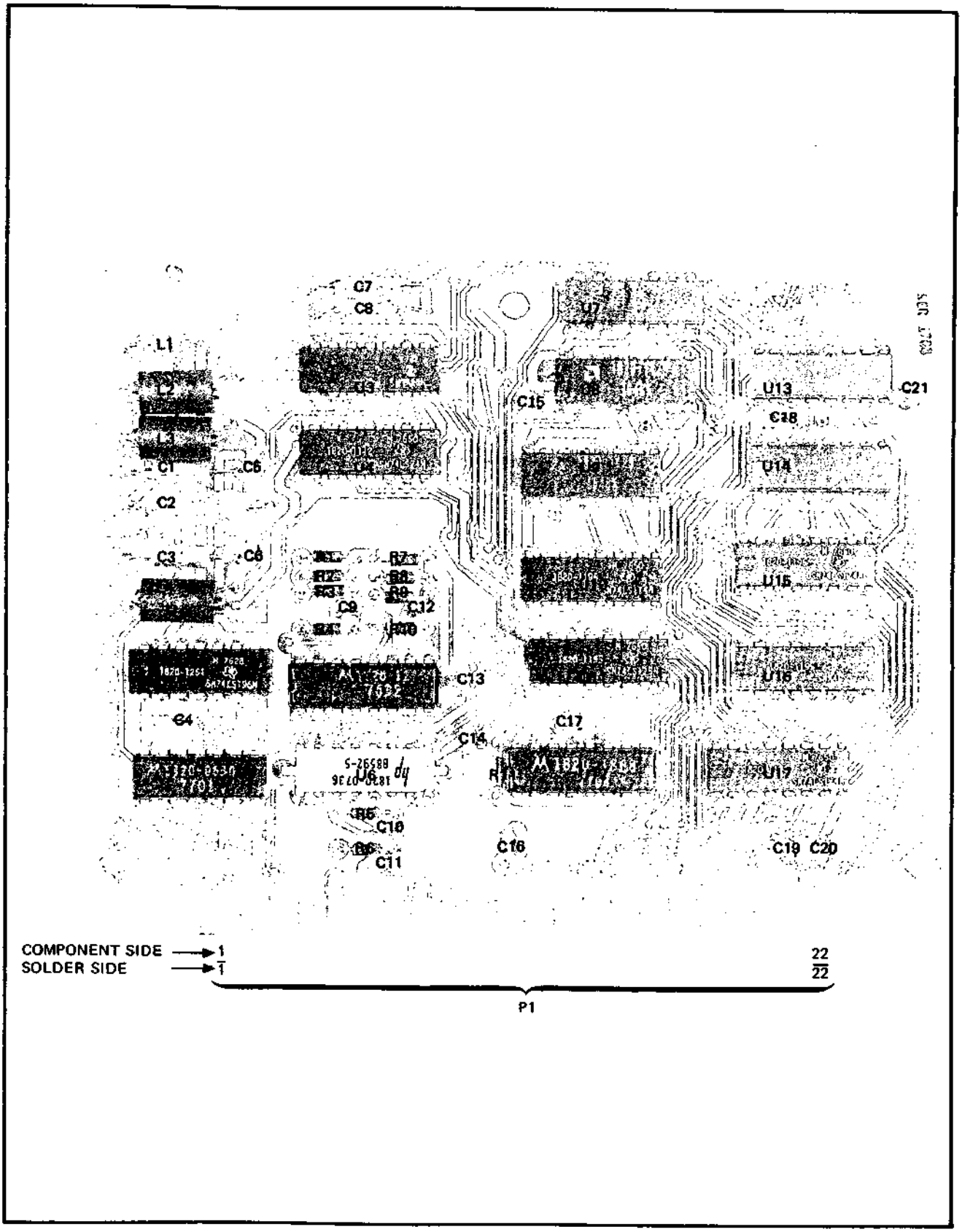
1. U3 BILATERAL SWITCH SYMBOL:



PINS 1 AND 2 OF U3A ARE JUMPERED CLOSED PERMANENTLY.

2. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
3. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN MICROFARADS
   INDUCTANCE IN MICROHENRIES
4. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN.

Figure 8-32. A9 Main Loop Amplifier Assembly



Part of Figure 8-33. A10 Divide-by-N Assembly

REFERENCE DESIGNATIONS

A10
C1-C21 L1-L4 R1-R11 TP1 U1-U17

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
U1	1820-1251	SN74LS196N
U2	1820-0630	MC4044P
U3	1820-0069	7420PC
U4	1820-1112	SN74LS74N
U5	1820-1225	MC10231P
U6	1820-0736	Same
U7	1820-0693	74S74PC
U8, U9, U13, U14	1820-1429	AM74LS160N
U10, U15, U17	1820-1196	AM74LS174N
U11, U16	1820-1195	AM74LS175N
U12	1820-1888	MC12013L

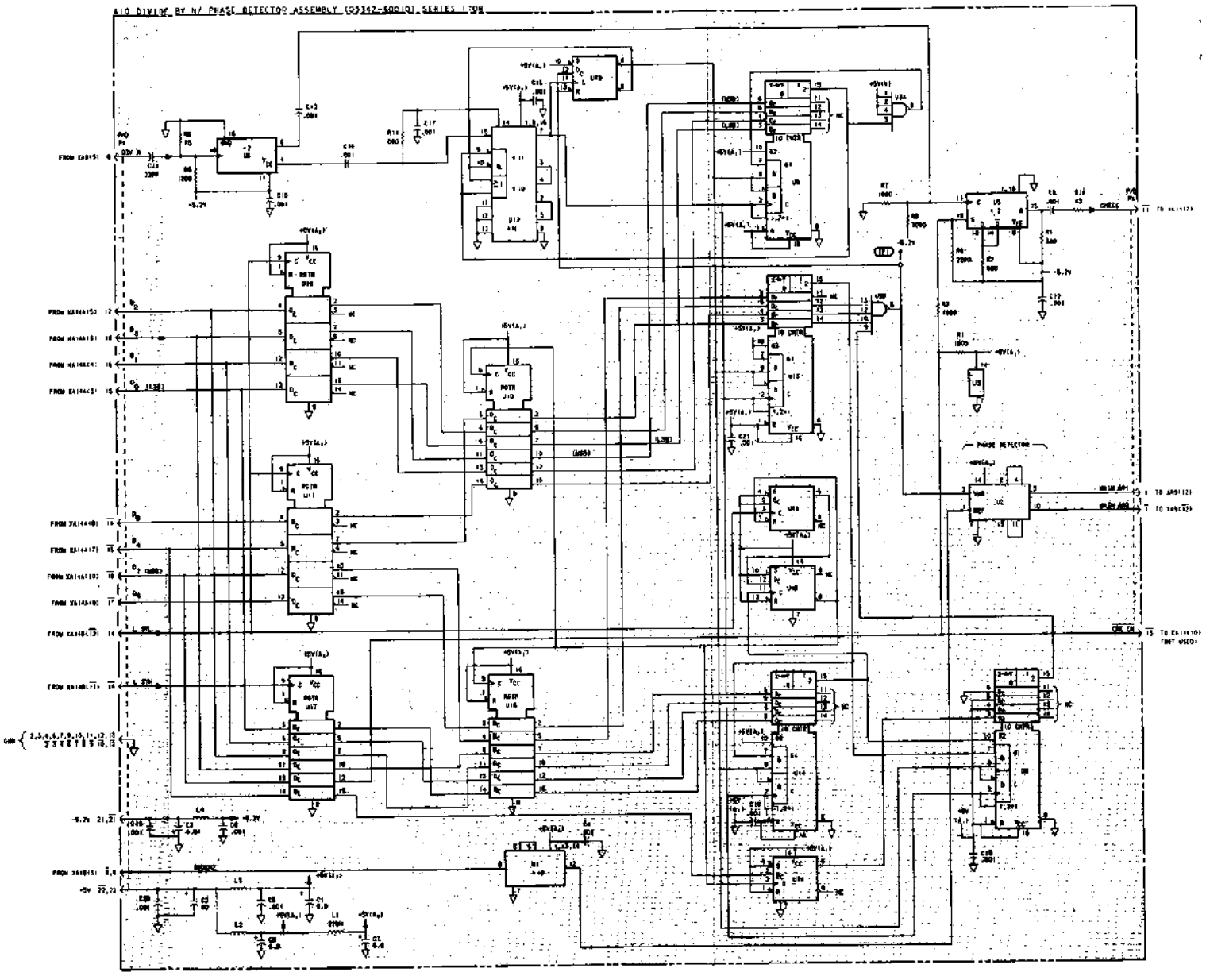
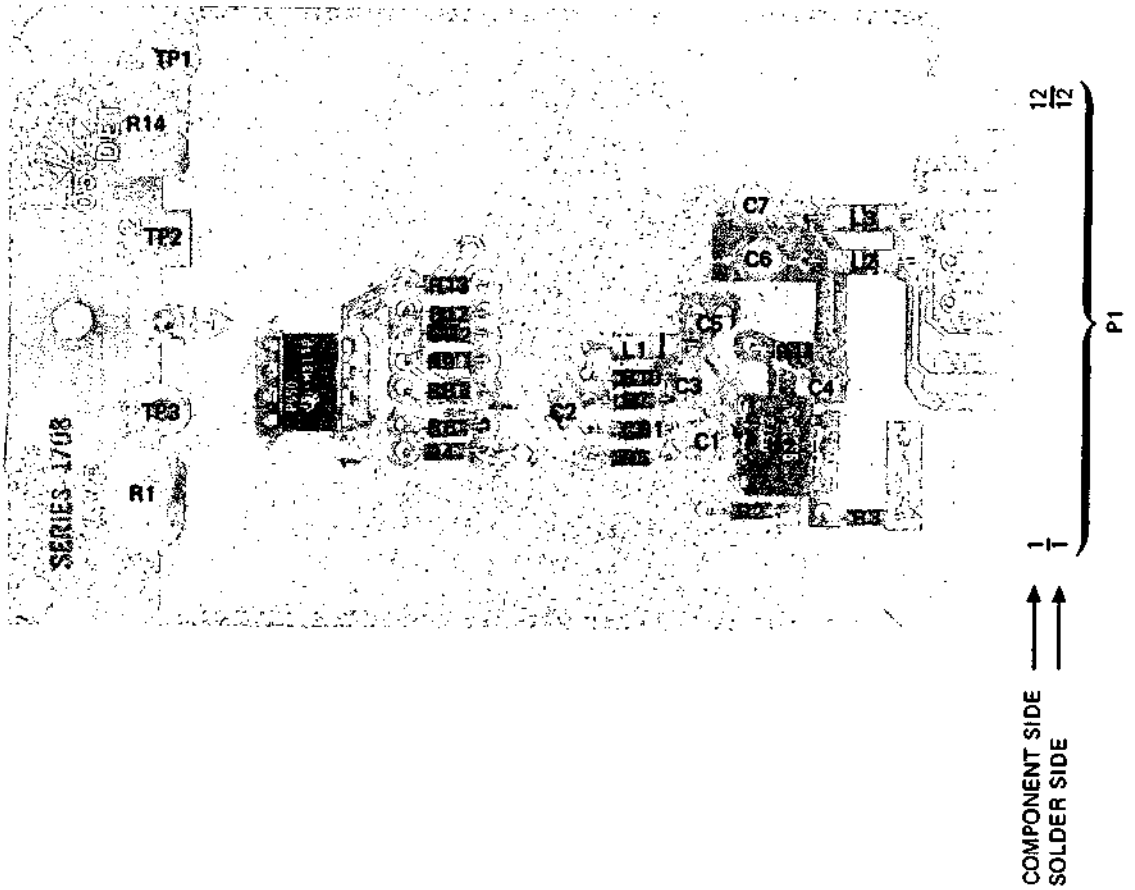


Figure 8-33. A10 Divide-by-N Assembly



Part of Figure 8-34. A11 IF Limiter Assembly

A11 IF LIMITER ASSEMBLY

CONDITIONS: No input signal, NOT in CHECK mode

U1		U2	
2	+0.18	1	0.0
3	+0.25	3	-3.25
4	-5.1	5	+3.3
5	+4.8	7	+4.3
7	+0.19	8	+3.2
8	+5.0		

U1 (with 5343A in CHECK mode)

2	+0.24
3	+0.05
7	+4.9

REFERENCE DESIGNATIONS

A11
C1-C7
CR1, CR2
L1-L3
R1-R14
TP1-TP4
U1, U2

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1, CR2	1901-0535	Same
U1	1826-0065	5000-9043
U2	1826-0372	Same

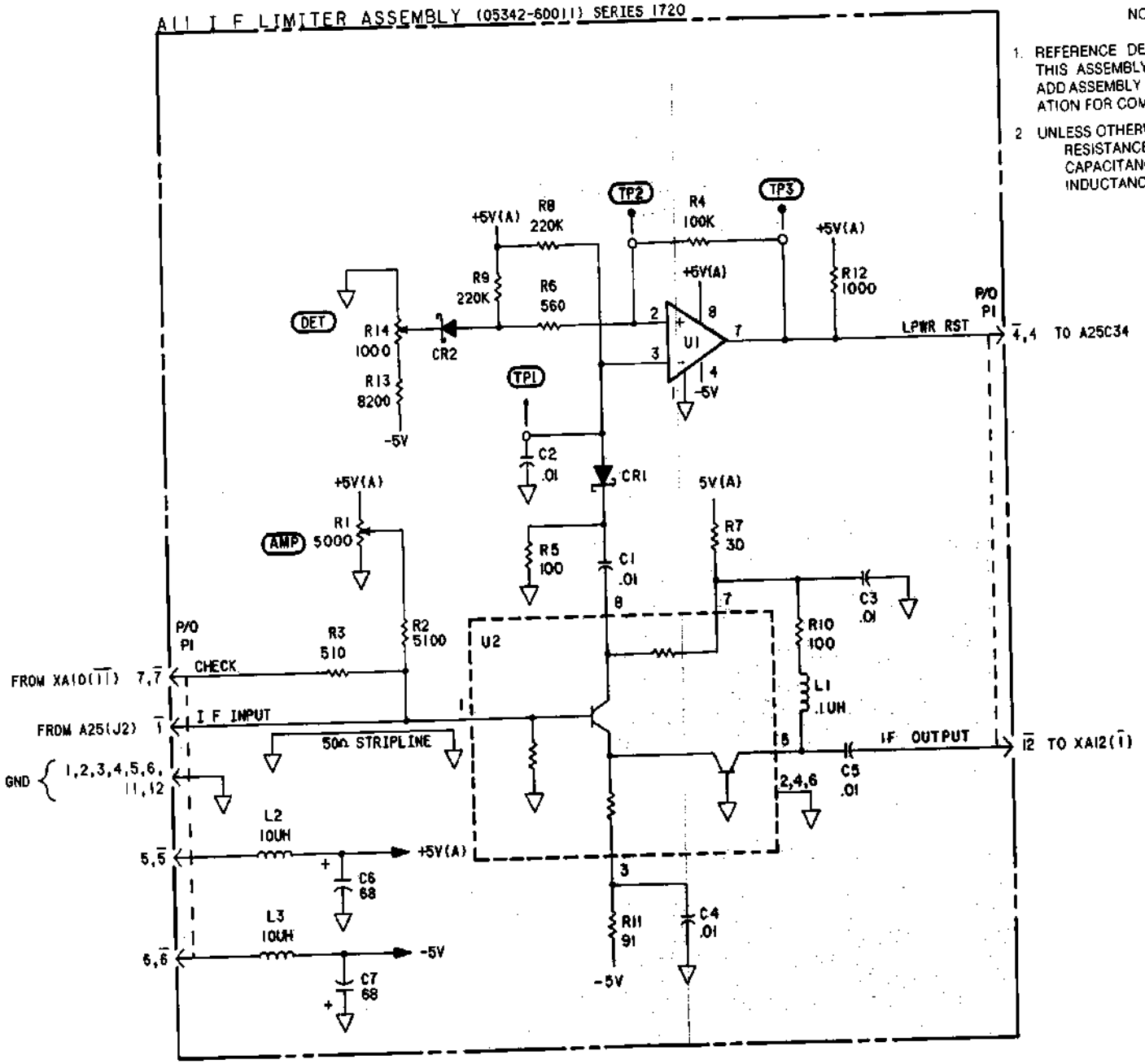
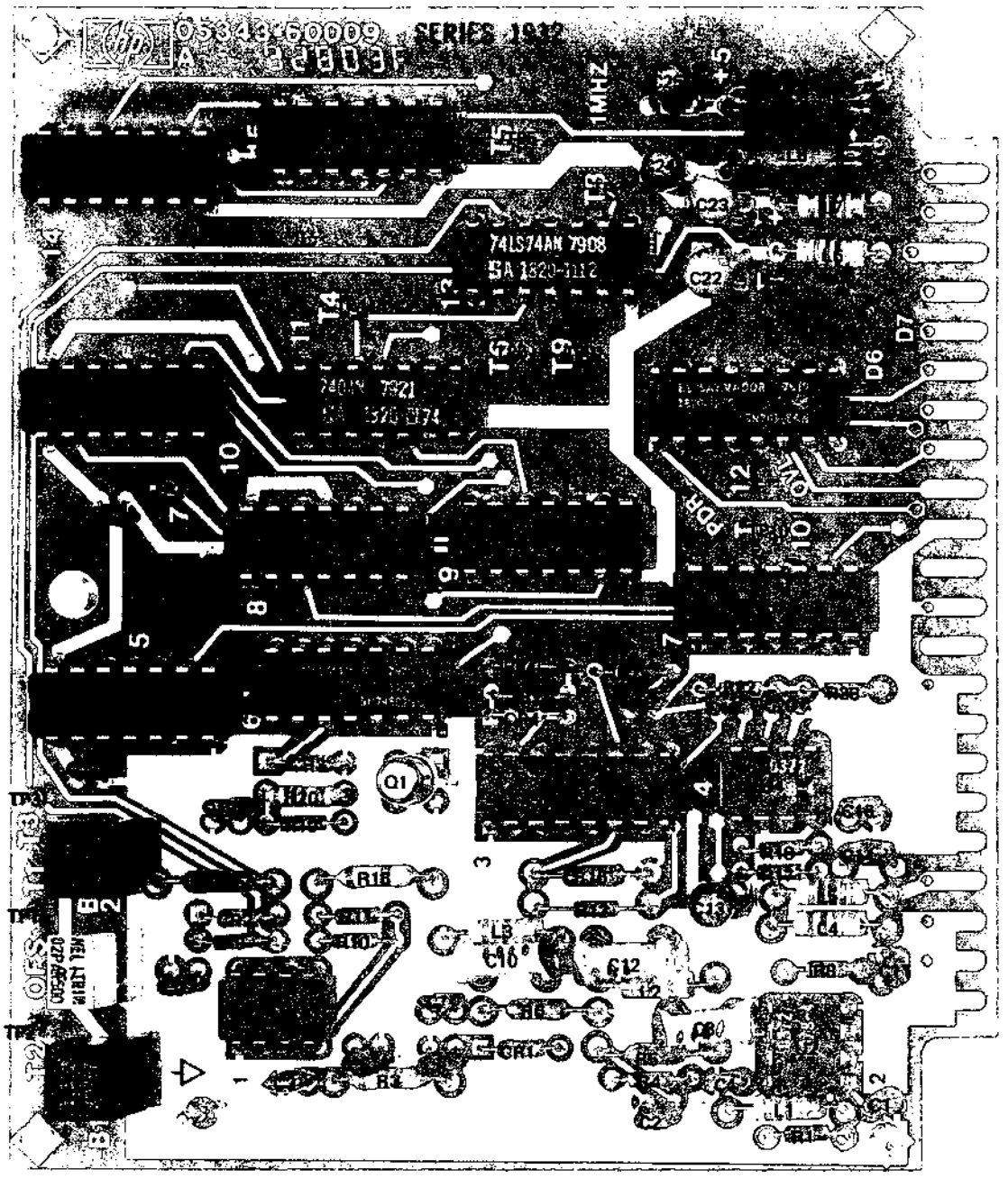


Figure 8-34. A11 IF Limiter Assembly



Part of Figure 8-35. A12 IF Detector Assembly

A12 IF DETECTOR ASSEMBLY

CONDITIONS: No input signal, NOT in CHECK mode.

U2		U4		Q1		NO INPUT SIGNAL	CHECK MODE
1	0.0	1	0.0	E	-1.6		
3	-3.3	3	-3.5	B	-1.3		
5	+3.0	5	+2.1	C	+1.6		
7	+4.2	7	+4.2				
8	+3.1	8	+2.8	grounded case			
					TP1	+0.27	-0.25
					TP2	+0.05	+0.10
					TP3	+0.18	+4.8

REFERENCE DESIGNATIONS

A12
C1-C25
CR1-CR4
L1-L7
Q1
R1-R25
TP1-TP11
U1-U15

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1-CR3	1901-0535	Same
CR4	1901-0040	Same
Q1	1854-0345	2N5179
U1	1826-0065	LM311N
U2, U4	1826-0372	Same
U3	1820-1225	MC10231P
U5	1820-0765	SN74197N
U6	1820-1322	SN74S02N
U7	1820-1197	SN74LS00N
U8, U9	1820-1285	SN74LS54N
U10, U15	1820-1193	SN74LS197N
U11	1820-0174	7404PC
U12	1820-1255	DM8098N
U13	1820-1112	SN74LS74N
U14	1820-1204	SN74LS20N

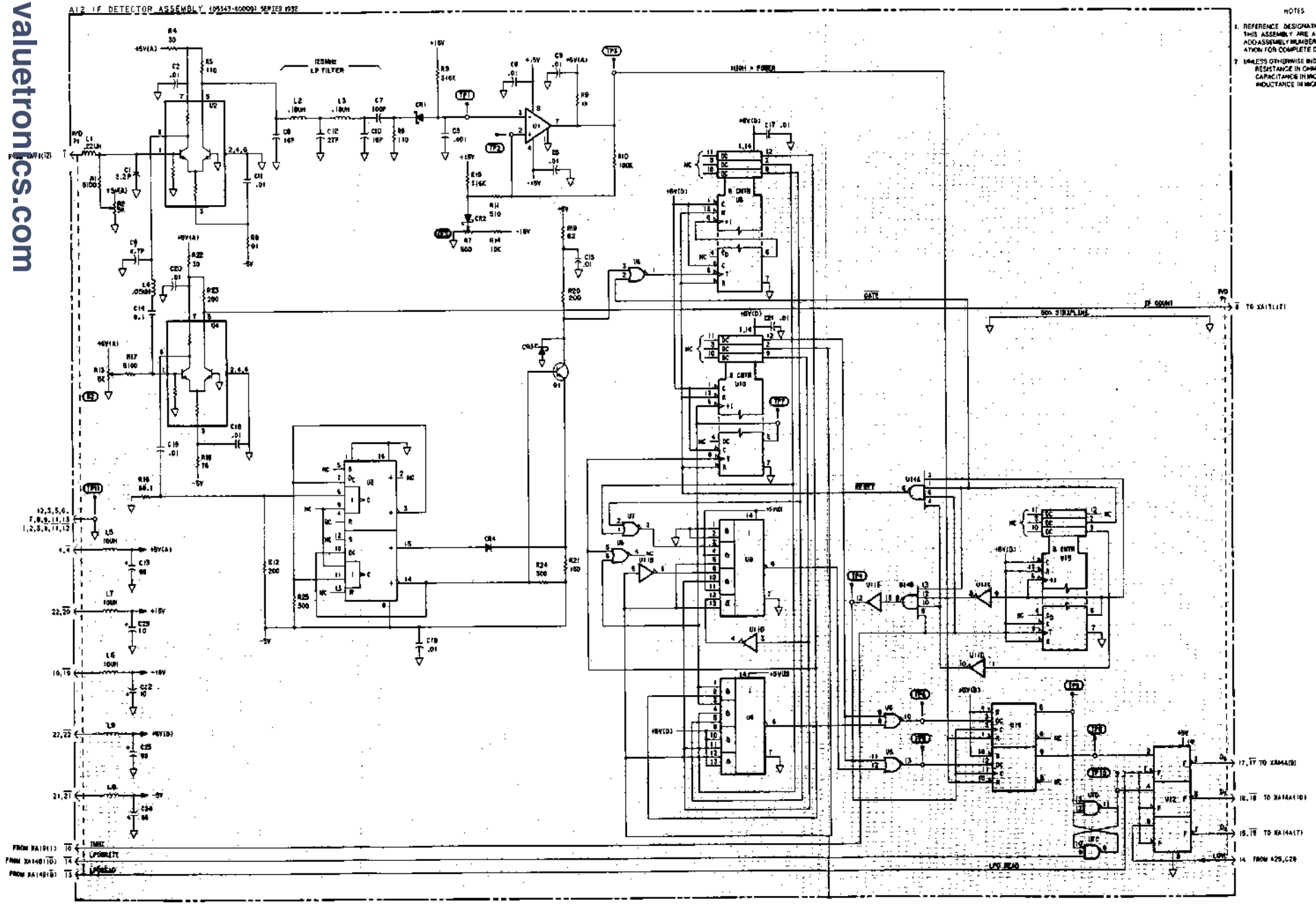
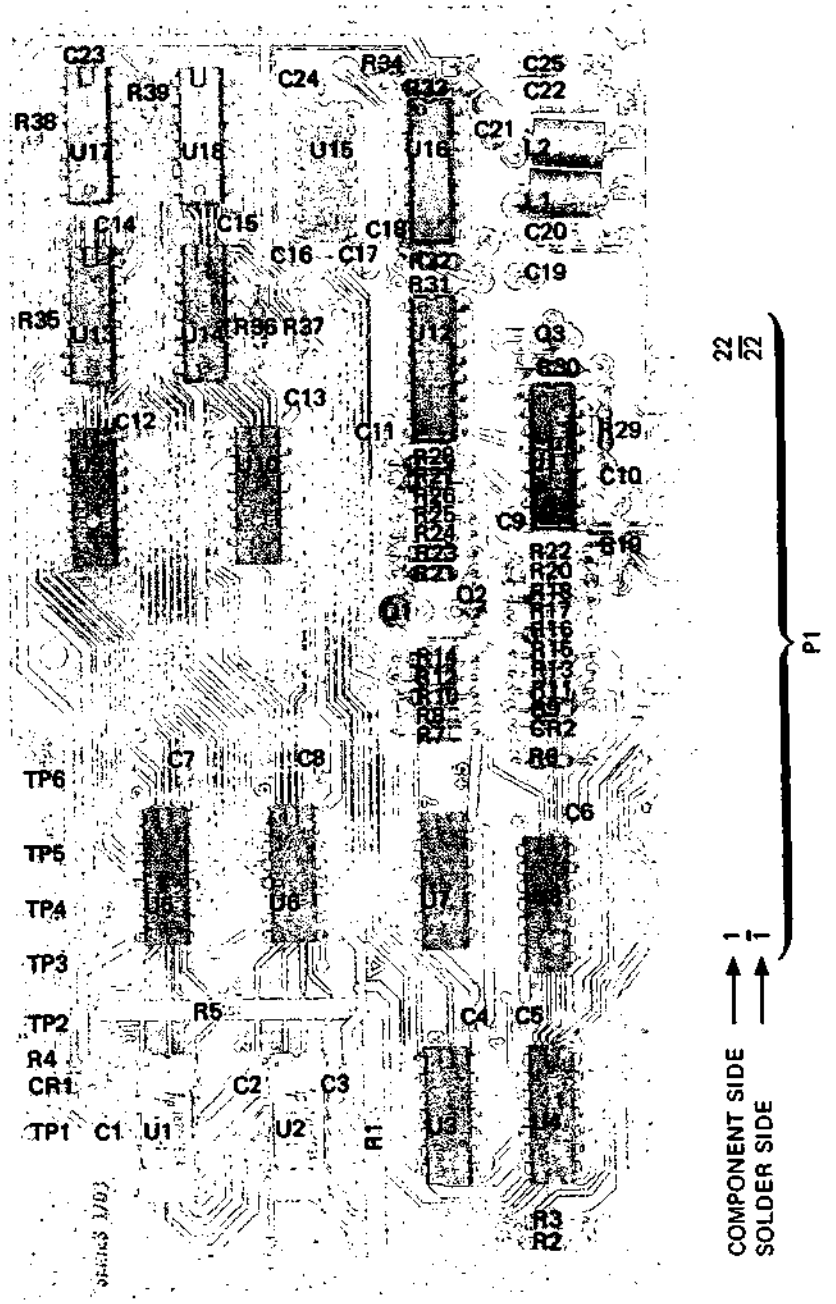


Figure 8-35. A12 IF Detector Assembly



Part of Figure 8-36. A13 Counter Assembly

A13 COUNTER ASSEMBLY

CONDITIONS: No input signal; SAMPLE RATE to HOLD

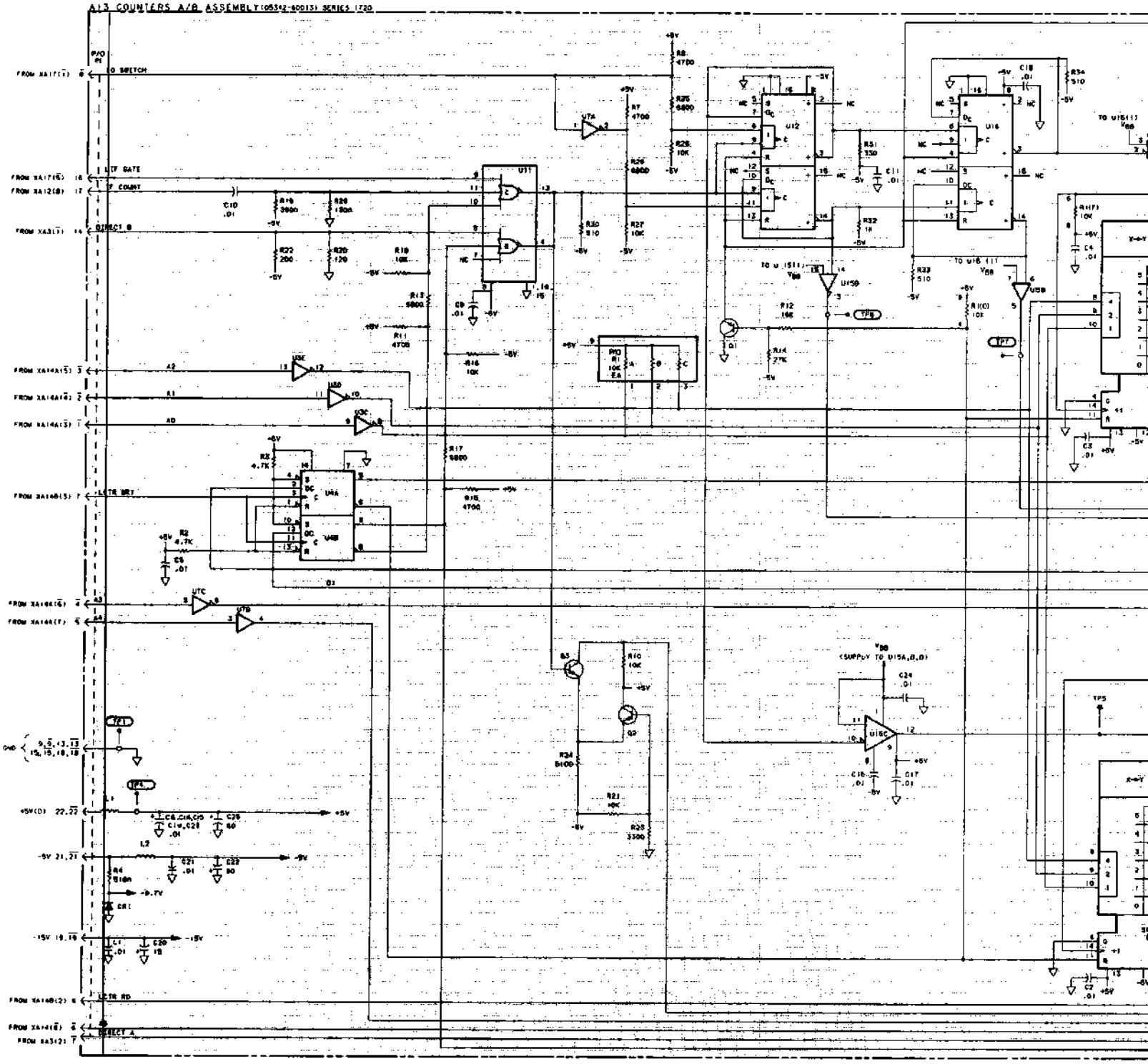
Q1		Q2		Q3	
E	-2.4	E	-1.9	E	-1.9
B	-1.8	B	-1.3	B	-1.7
C	-0.0	C	+5.0	C	+5.0

REFERENCE DESIGNATIONS

A13
C1-C25 CR1, CR2 L1, L2 Q1, Q2 R1-R34 TP1-TP8 U1-U18

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1, CR2	1901-0040	Same
Q1, Q2	1854-0071	Same
U1, U2	1820-0634	Same
U3, U7	1820-1199	SN74LS04N
U4	1820-1112	SN74LS74N
U5, U6, U9, U10		SN74LS253N
U8	1820-1197	SN74LS00N
U11	1820-1950	MC10212P
U12, U16	1820-1225	MC10231P
U13, U14	1820-1251	SN74LS196N
U17, U18	1820-1251	SN74LS196N
U15	1820-1052	MC10125L



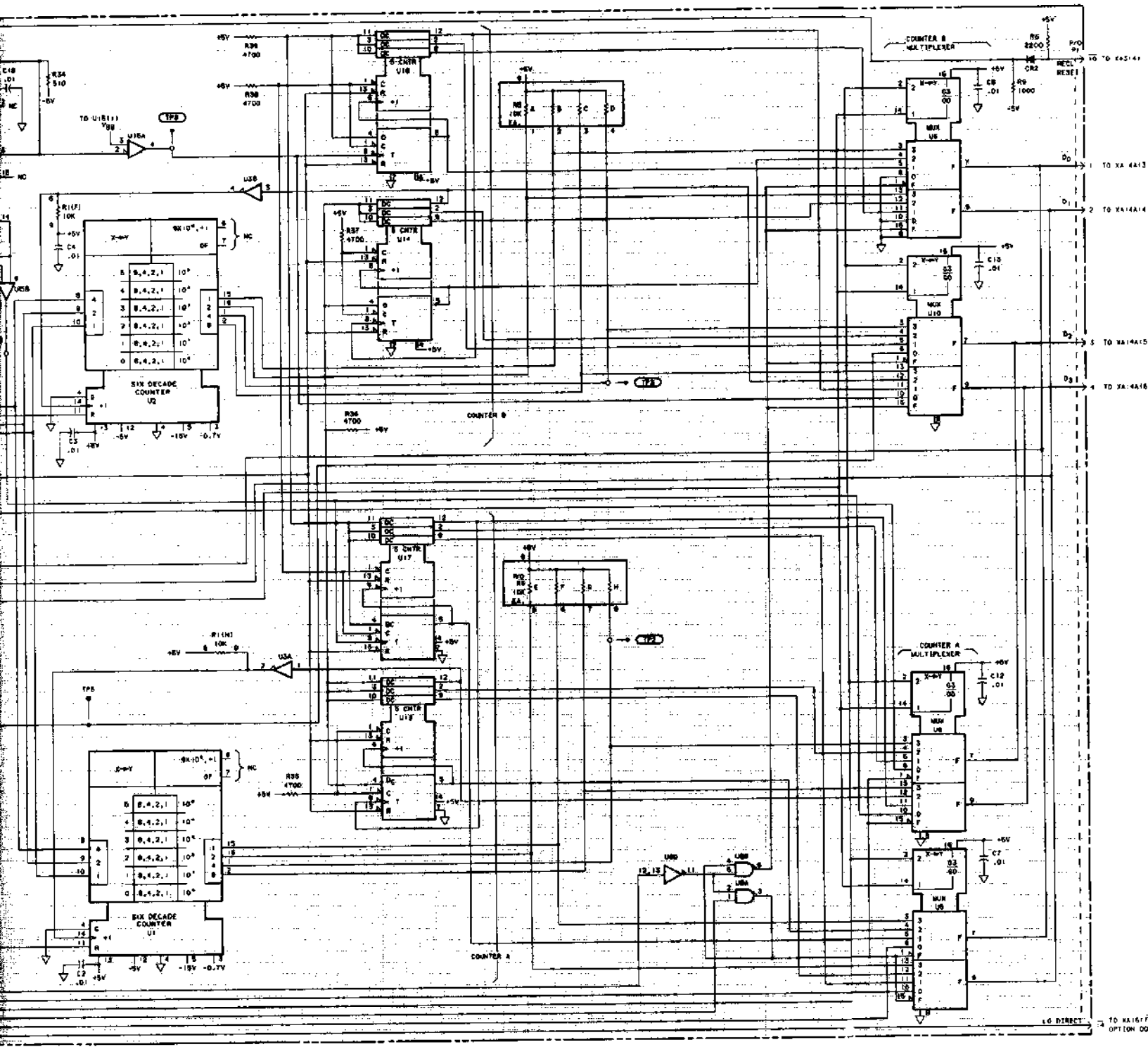


Figure 8-36. A13

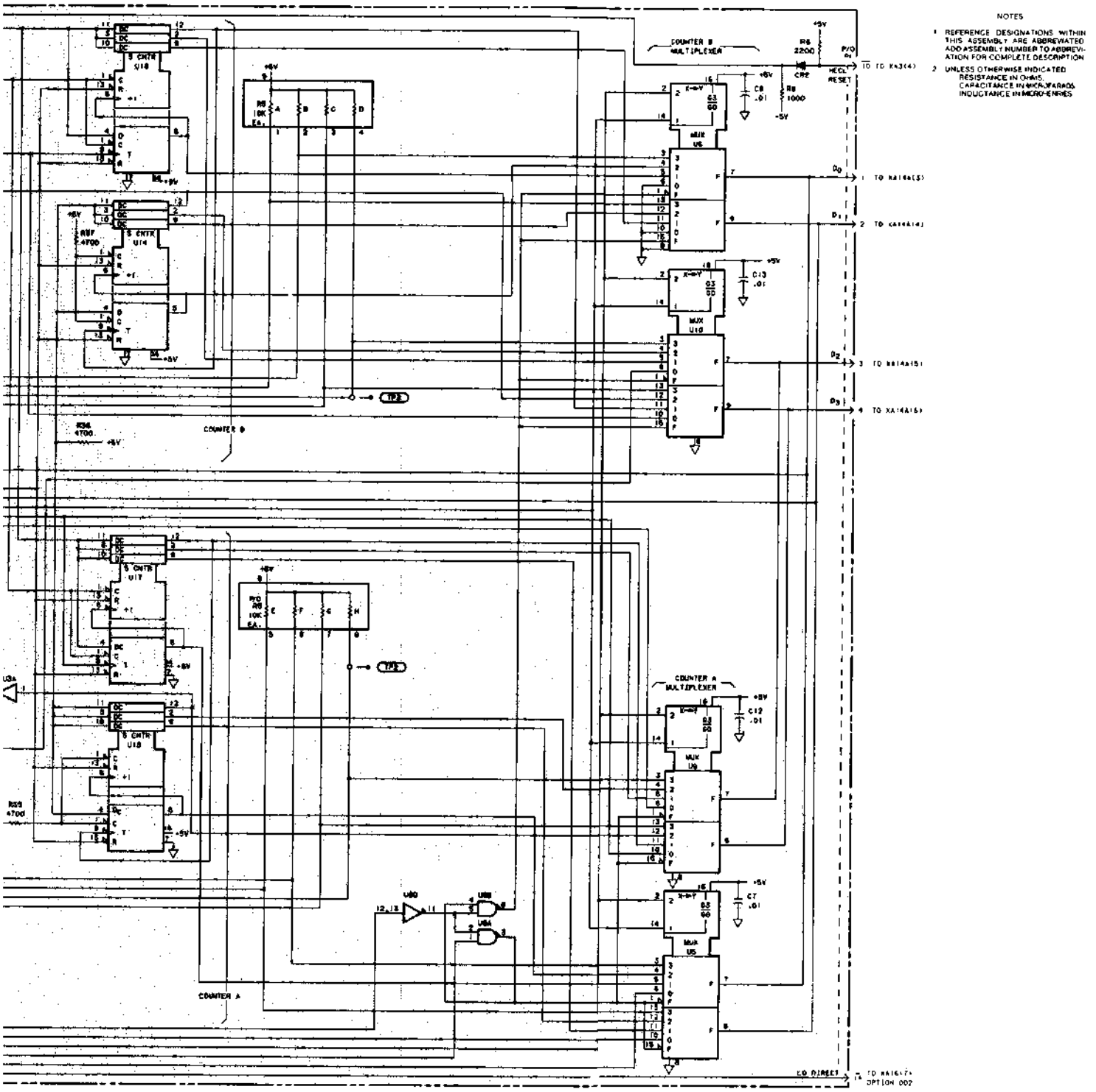
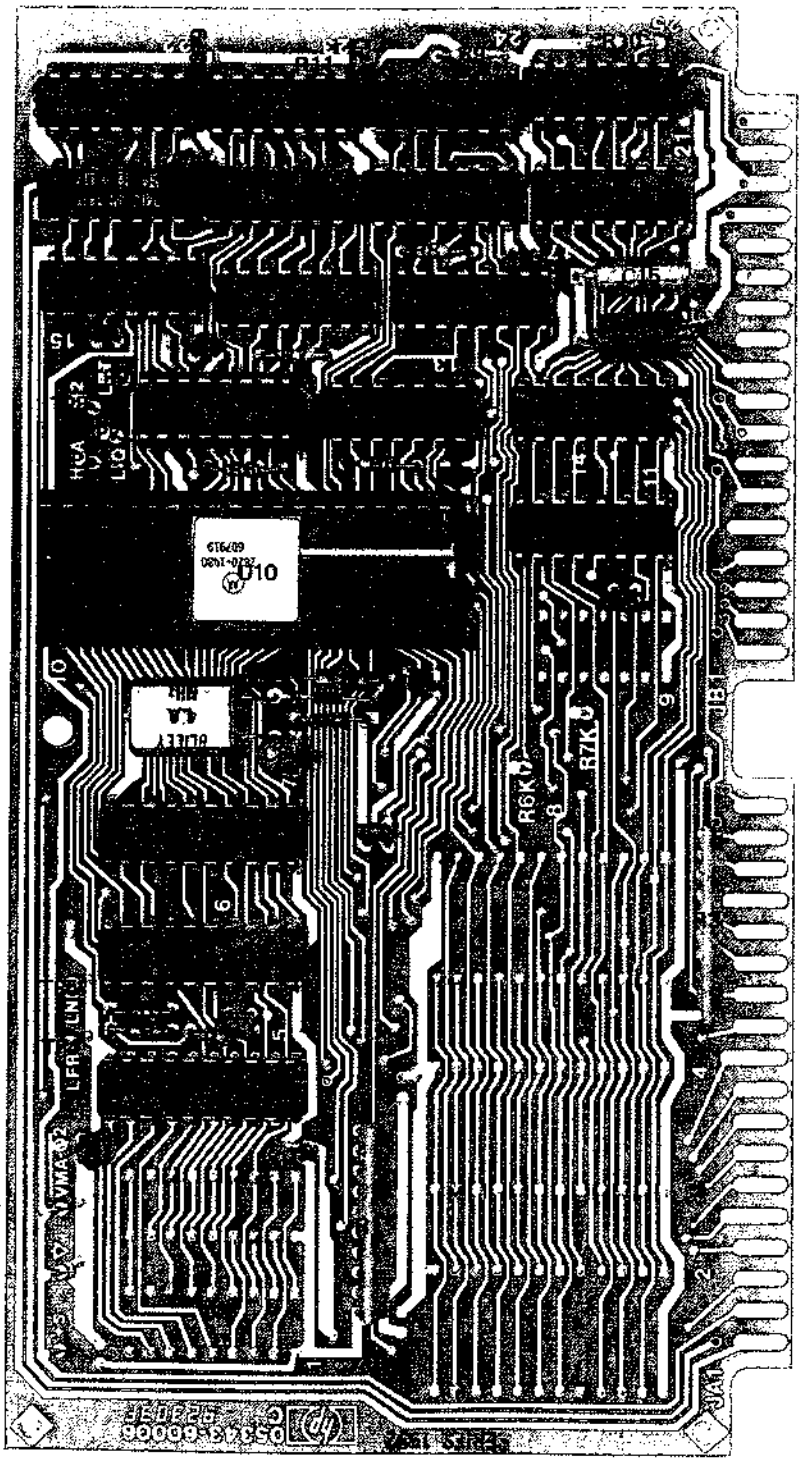


Figure 8-36. A13 Counter Assembly



Part of Figure 8-37. A14 Microprocessor Assembly

REFERENCE DESIGNATIONS

A14
C1-C22
CR1-CR3
L1, L2
TP1-TP11
U5-U7, U10-U14
U16-U25

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR. OR INDUSTRY PART NUMBER
CR1, CR2	1901-0040	Same
CR3	1901-0535	Same
U5	1820-2206	SN74LS640N
U6, U7	1820-1917	SN74LS240N
U10	1820-1480	MC6800L
U11, U14, U17	1820-1216	SN74LS138N
U12	1820-2036	6875
U13, U20	1820-1202	SN74LS10N
U16, U21	1820-1281	SN74LS139N
U18	1820-1144	SN74LS02N
U19, U24	1820-1199	SN74LS04N
U15	1820-1492	SN74LS368N
U22	1820-1112	SN74LS74N
U23, U25	1820-1197	SN74LS00N

With the test setup described in *Table 8-10*, steps 1, 2, and 3, the signatures shown below are correct.

*** = PROBE BLINKS**

PIN	U5	U6	U7	U11	U12	U13
1	0000	0000	0000	4FCA*	0003	4FC9*
2	0003*	UUUU*	FFFF*	4868*	0003	642C*
3	0000	8487*	P760*	9UP1*	0000	0001*
4	0000*	0356*	1U5P*	0000	0000*	9UP2*
5	0000	6322*	U75A*	0000	0000*	486C
6	0000	6F9A*	0002*	0003	0003	5FUA*
7	0000	37C6*	9UP2*	26UU*	0003*	0000
8	0000	4868*	7791*	0000	0000	6UP5*
9	0000	6U2C*	4FC9*	147P*	0003*	84UA*
10	0000	0000	0000	1ACA*	0003	P076*
11	0003	6U28*	4FCA*	C7HA*	0000	0C6A*
12	0003	486C*	7792*	47PC*	0003	32U8*
13	0003	37C5*	9UP1*	3H02*	0003*	37C6*
14	0003	6F99*	0001*	3714*	0003	0003
15	AH9F*	6321*	U759*	H21U*	0000*	
16	AH9F*	0355*	1U5H*	0003	0003	
17	0003	8484*	P763*			
18	0003	UUUF*	FFFU*			
19	0003	0000	0000			
20	0003	0003	0003			

PIN	U14	U15	U16	U17	U18	U19
1	U75A*	0000*	0003	UUUF*	0000	C531*
2	6F99*	18AH*	0003	FFFU*	0000	C532*
3	7792*	18AP*	0003	8487*	0003	0003
4	32U8*	0003	0003	1C2C*	0000*	0000
5	5FUA*	0000	0003	0000	0003*	0000
6	6322*	0003	0003	0003	0000*	0003
7	1H3U*	0000	0000	FF48	0000	0000
8	0000	0000	0000	0000	0000	0003
9	0C6A*	0003	9H1F*	7311*	0000	0000
10	P076*	0000	6H41*	9FF7*	0000	0000
11	84UA*	AH9F*	1C2C*	A732*	C531*	0000
12	9569*	0003	C531*	A9FU*	8487*	0000
13	94F1*	AH9F	1U5H*	6A70*	18AH*	0003
14	CCUC*	0003	P760*	1A9U*	0003	0003
15	9945*	AH9F	5P44*	46A4*		
16	0003	0003	0003	0003		

PIN	U20	U21	U22	U23	U24	U25
1	0003*	4378*	0003	6H41*	6UP5*	0003*
2	1H3F*	P760*	0003*	9H1F*	6UP6*	0003*
3	1H3F*	1U5H*	0003	U05H*	0003	0000
4	0003*	F963*	0003	0003	0000	0000
5	0356*	2U28*	0003	0000	0000	0000
6	4378*	1P2A*	0000	0003	0003	0000
7	0000	CC1A*	0000	0000	0000	0000
8	0000	0000	0003*	0000	0003	94F1*
9	0000	0003	0000*	0003	0000	94F2*
10	0000	0003	0003*	0003*	1H3F	0003*
11	0000	0003	0003*	AH9F*	1H3U	0000
12	5P44*	0003	0000*	8487*	94F2	0003
13	0355*	0003	0003	C532*	94F1	0003
14	0003	0003	0003	0003	0003	0003
15		0003				
16		0003				

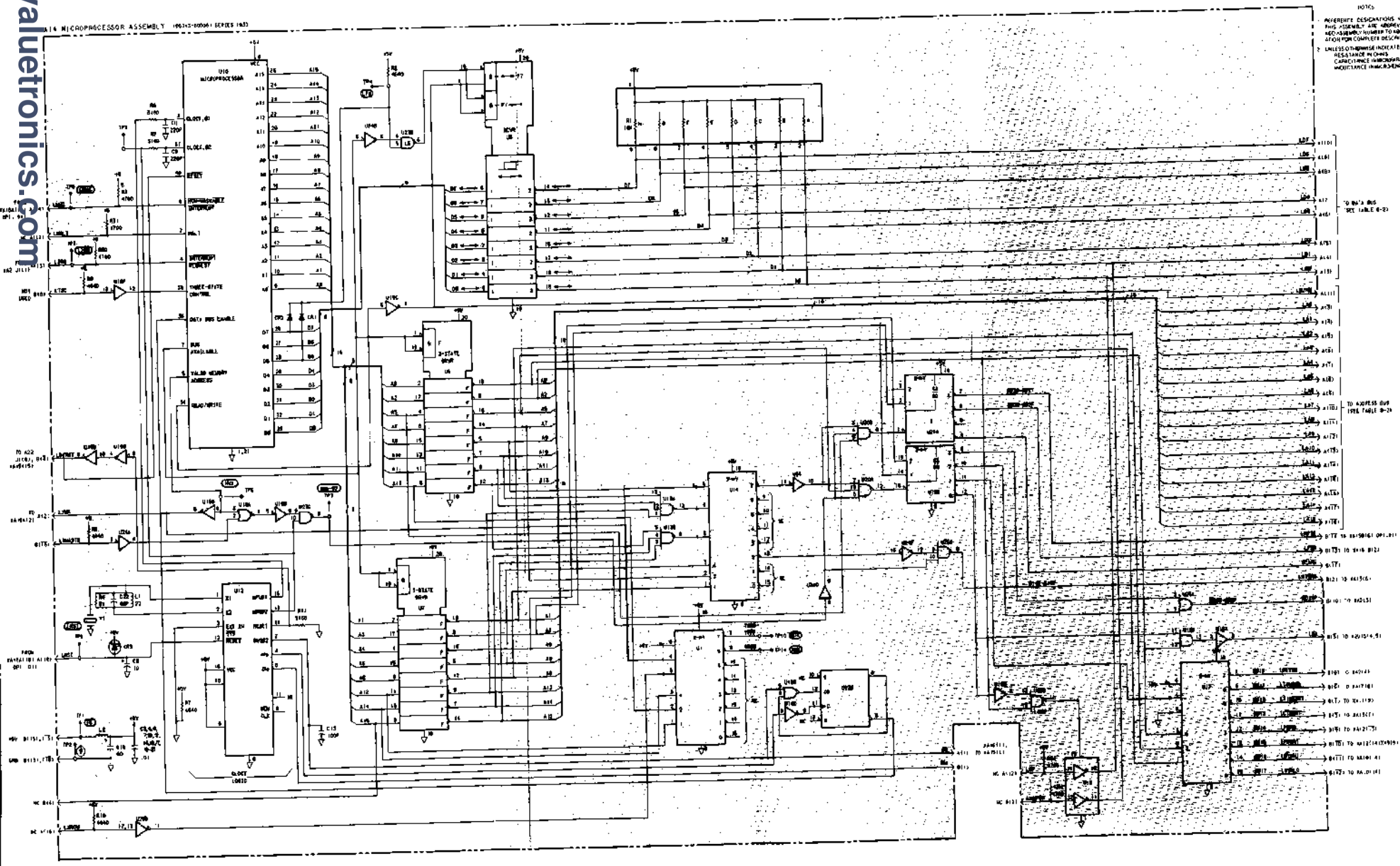
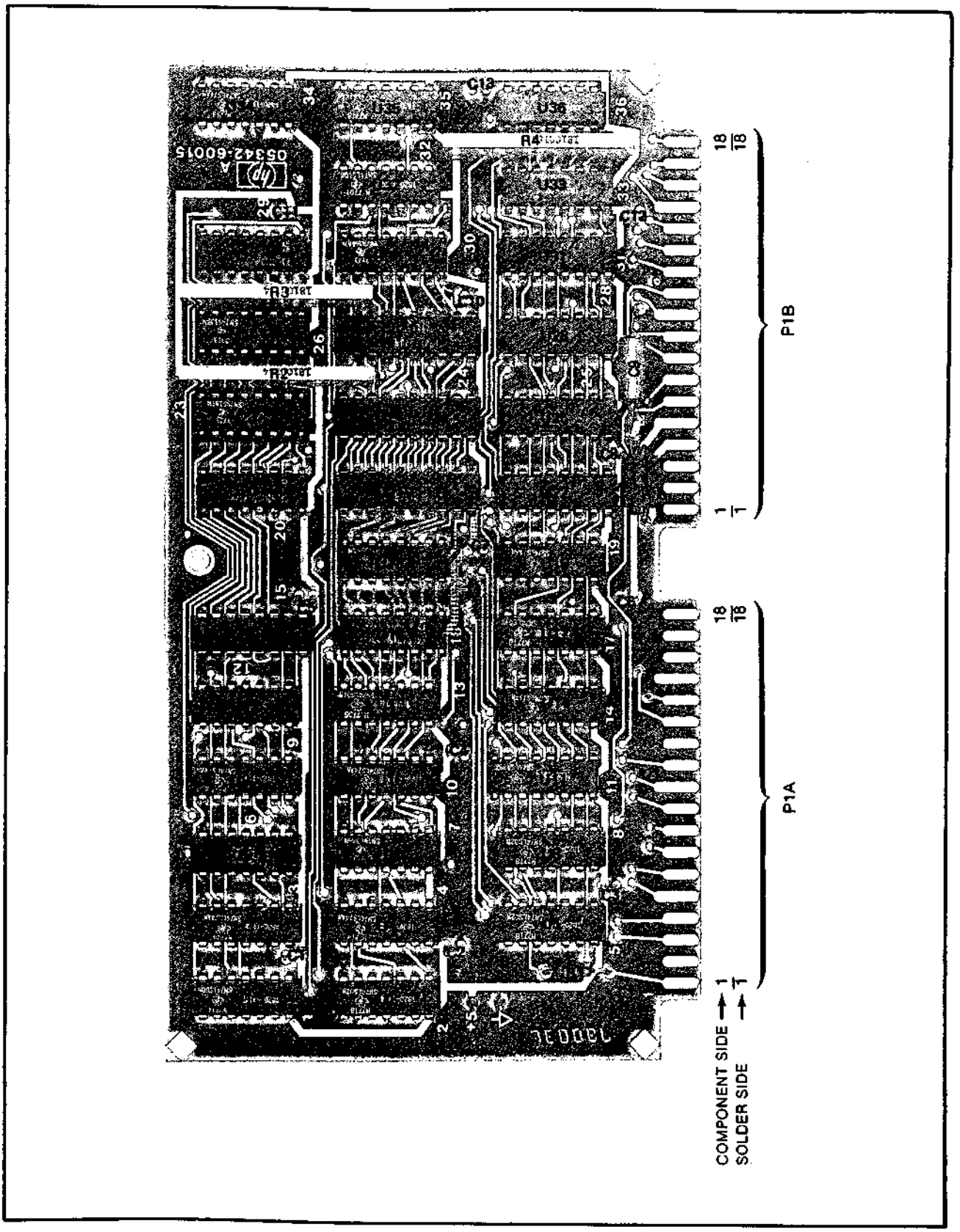


Figure 8-37. A14 Microprocessor Assembly



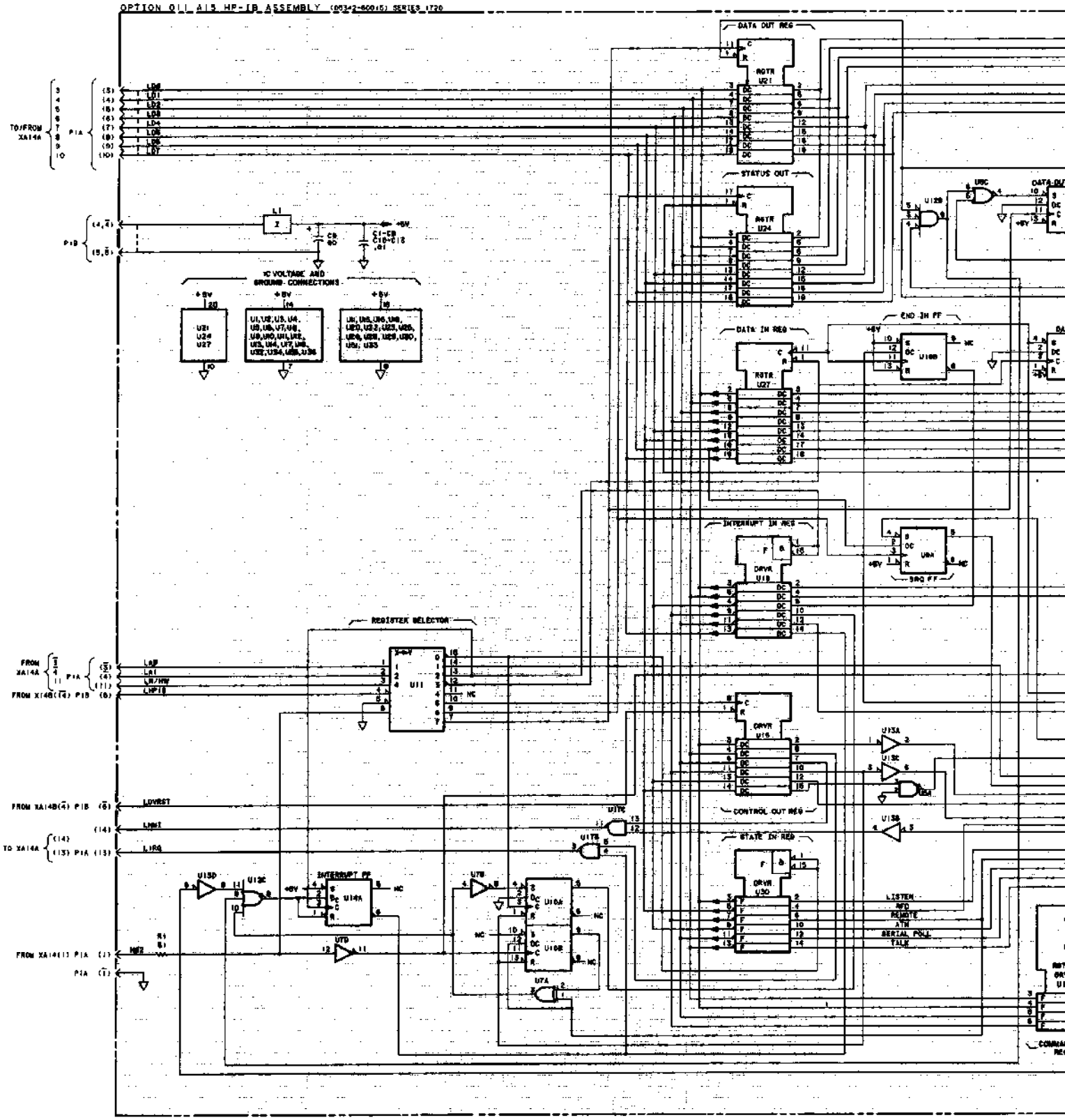
Part of Figure 8-38. Option 011 A15 HP-IB Assembly

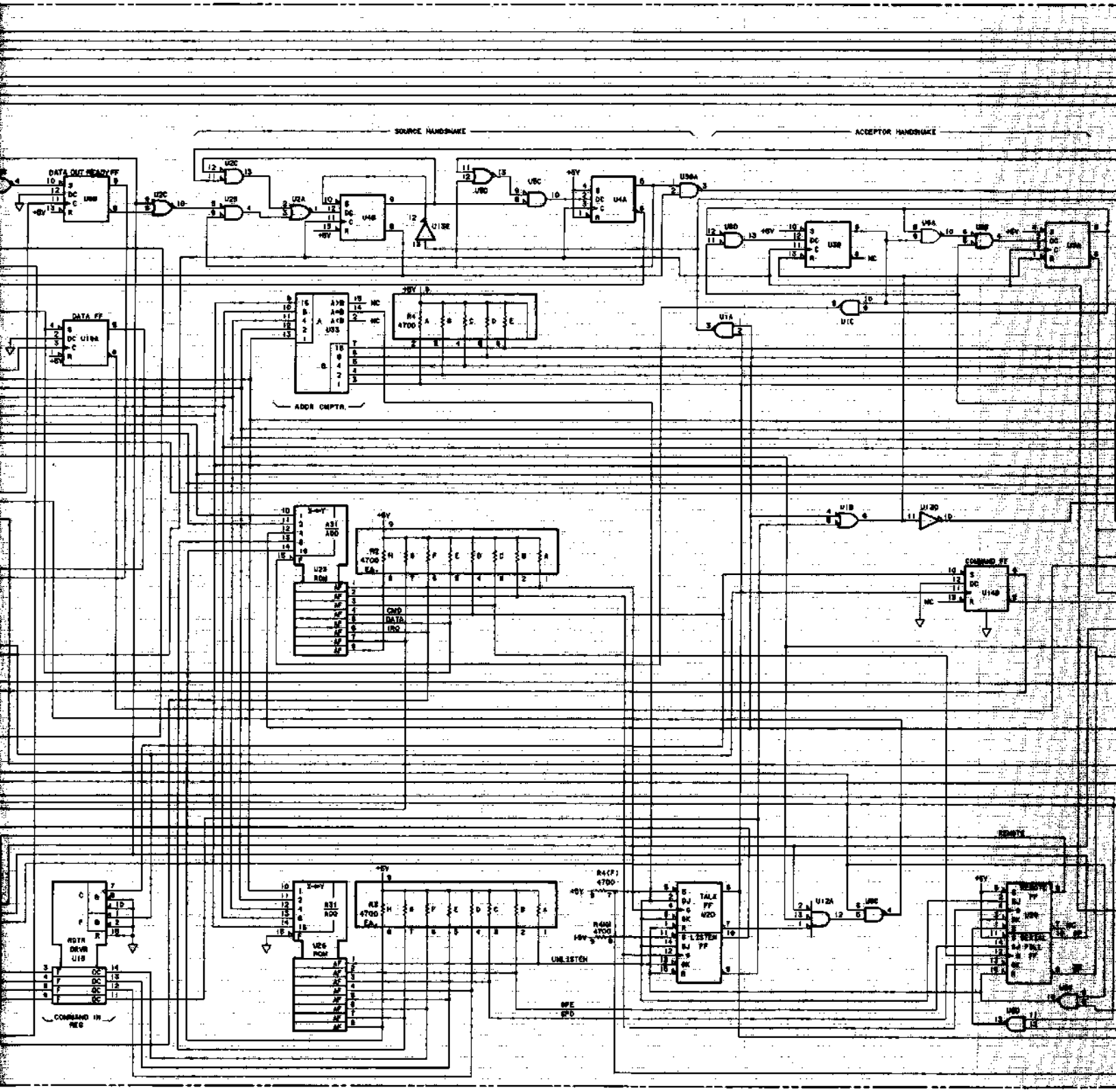
REFERENCE DESIGNATIONS

A15
C1-C3 L1 R1-R4 U1-U36

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFG OR INDUSTRY PART NUMBER
U1, U36	1820-1197	SN74LS00N
U2, U5, U6, U8	1820-1144	9LS02PC
U3, U4, U9 U10, U14, U19, U34, U35	1820-1112	SN74LS74N
U7	1820-1211	SN74LS86N
U11	1820-1216	SN74LS138N
U12	1820-1206	SN74LS27N
U13	1820-1199	SN74LS04N
U15	1820-1885	DM74LS173N
U16	1820-1196	AM74LS174N
U17	1820-1198	SN74LS03N
U18, U30	1820-1368	DM8096N
U20, U29	1820-1282	SN74LS109N
U21, U24, U27	1820-1997	SN74LS374PC
U22, U25, U28, U31	1820-1689	MC3446P
U23	1816-1154	Same
U26	1816-1155	Same
U32	1820-1202	9LS10PC
U33	1820-0904	93L24PC





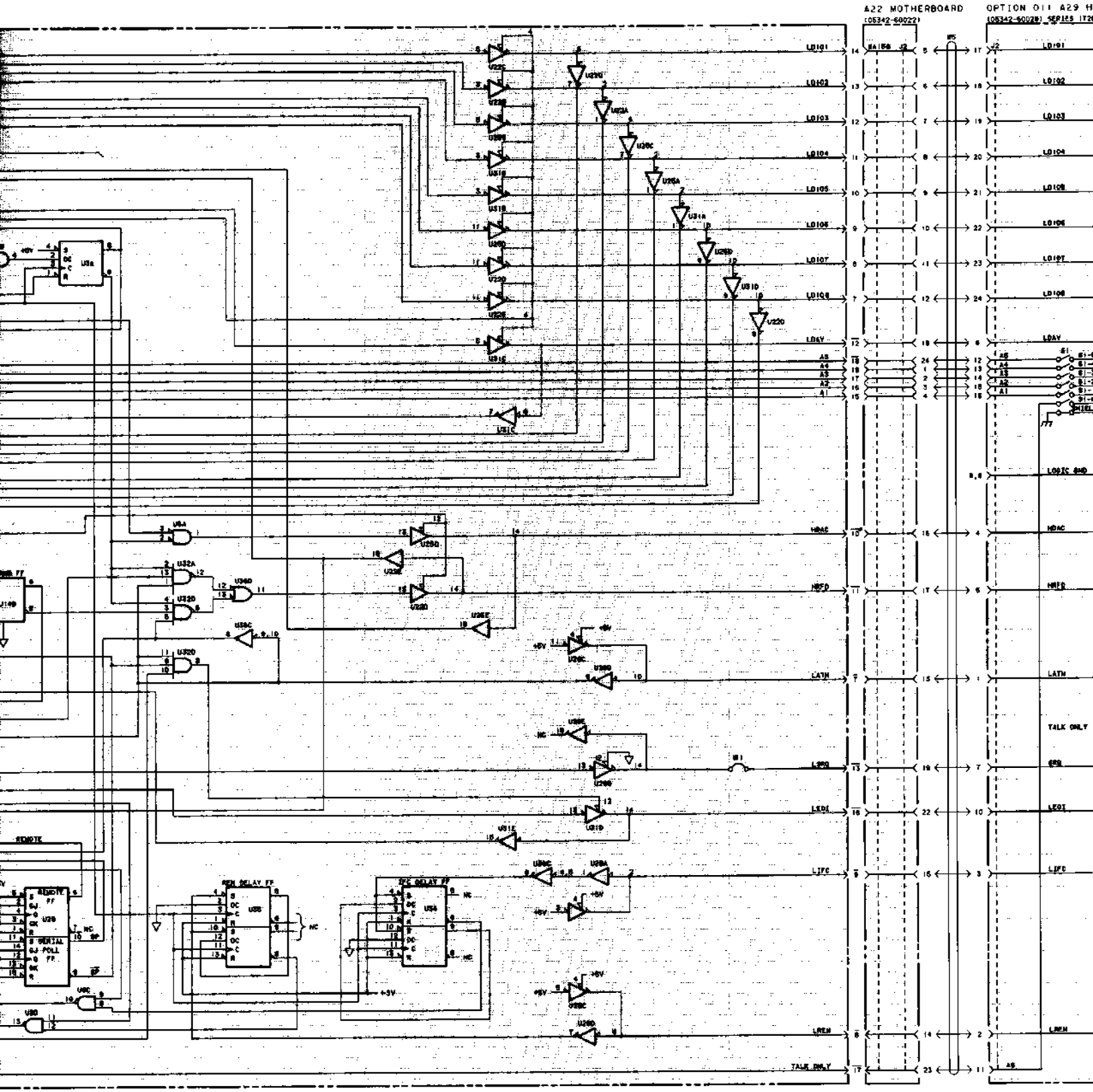


Figure 8-38. Opti

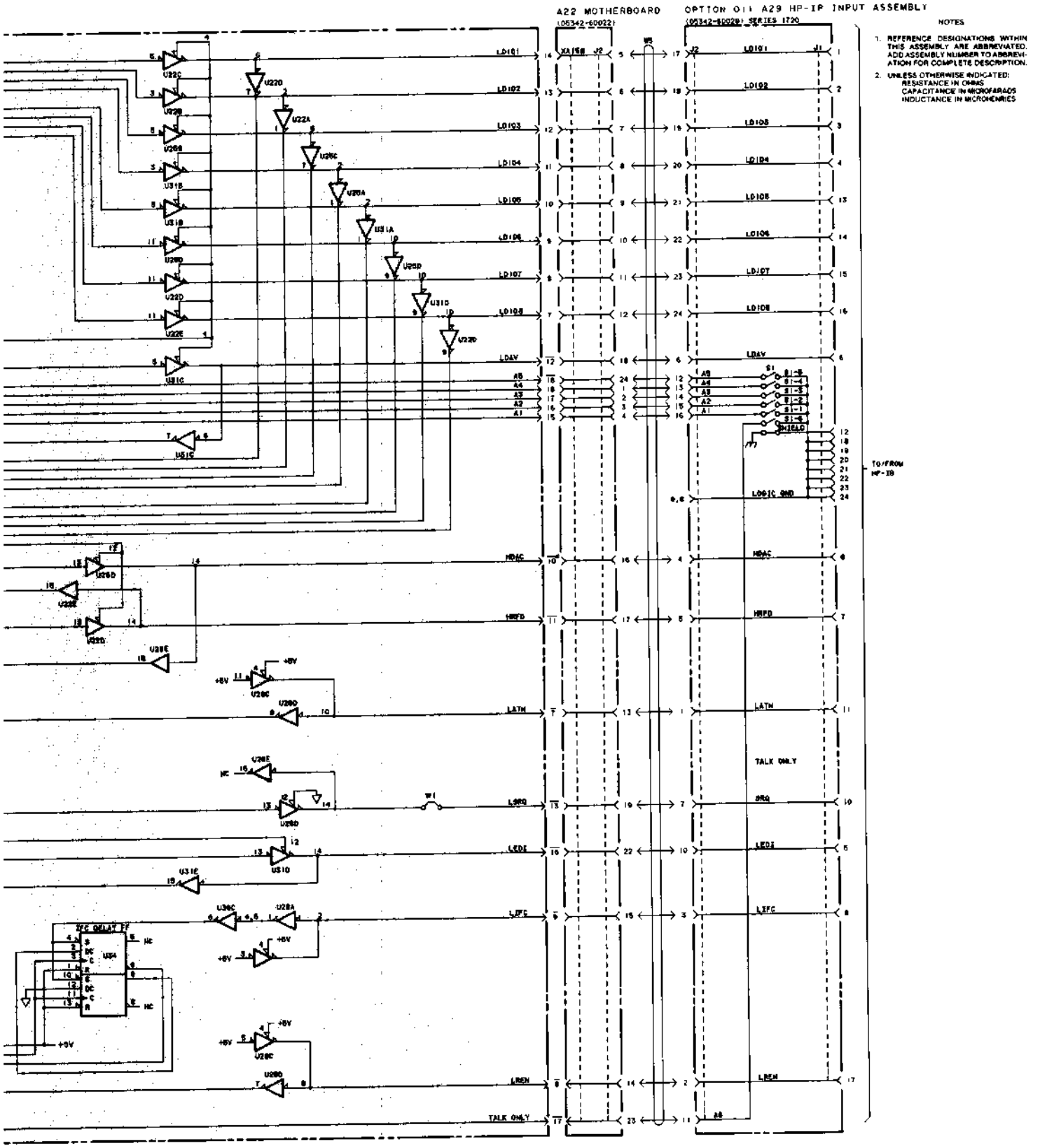
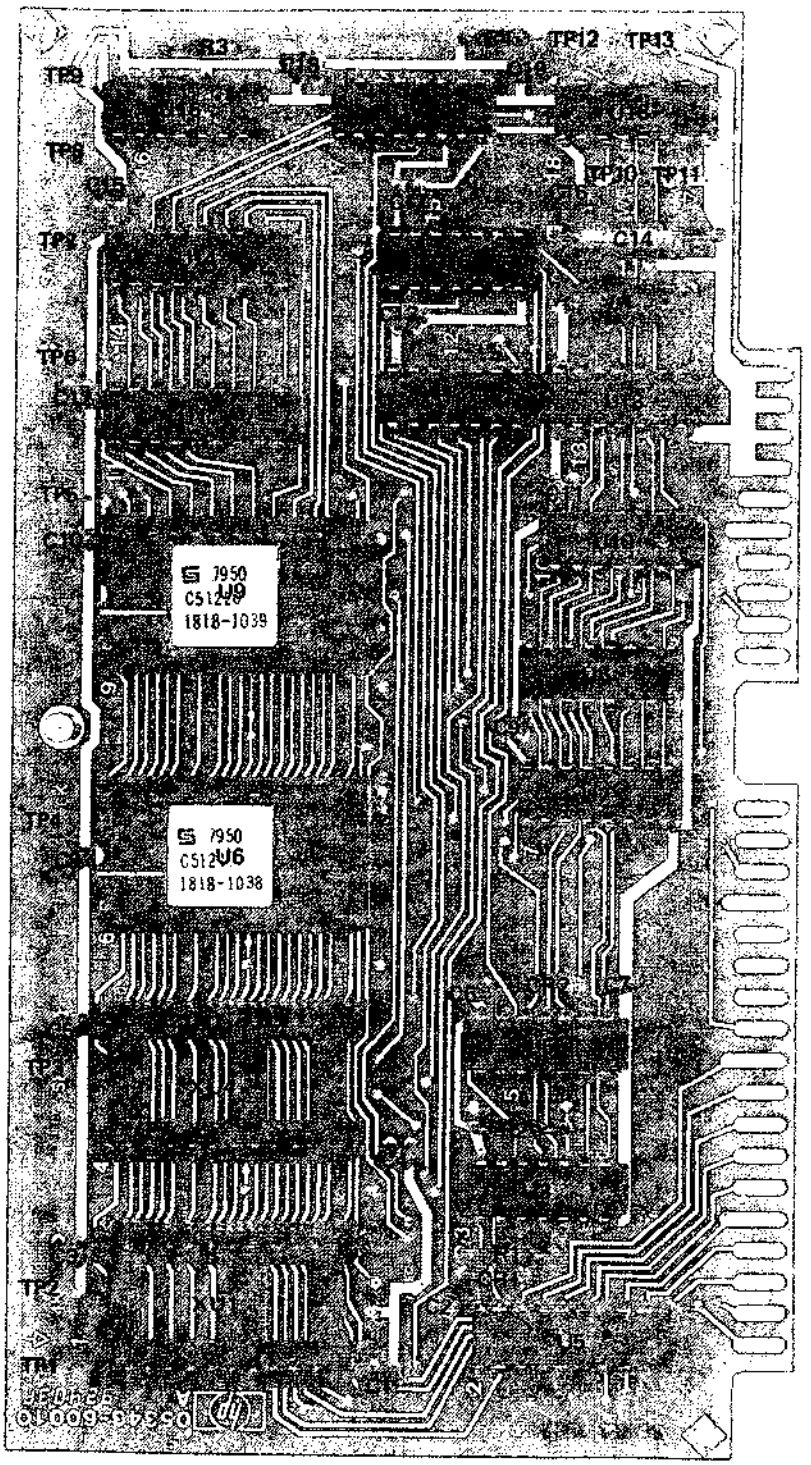


Figure 8-38. Option 011 A15 HP-IB Assembly



Part of Figure 8-39. A16 Memory and Sweeper Control Assembly

REFERENCE DESIGNATIONS

A16
C1-C20
CR1, CR2
L1
R1-R4
TP1-TP13
U2, U3, U5-U18

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATIONS	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1, CR2	1901-0535	Same
U2	1820-2075	SN74LS245N
U3, U15	1820-1197	SN74LS00N
U5	1820-1199	SN74LS04N
U6	1818-1038	Same
U7, U8, U17	1820-1216	SN74LS138N
U9	1818-1039	Same
U10	1820-1201	SN74LS08N
U11, U14	1818-0197	Same
U12, U13	1820-1207	SN74LS30N
U16	1820-1112	SN74LS74N
U18	1820-1491	SN74LS367N

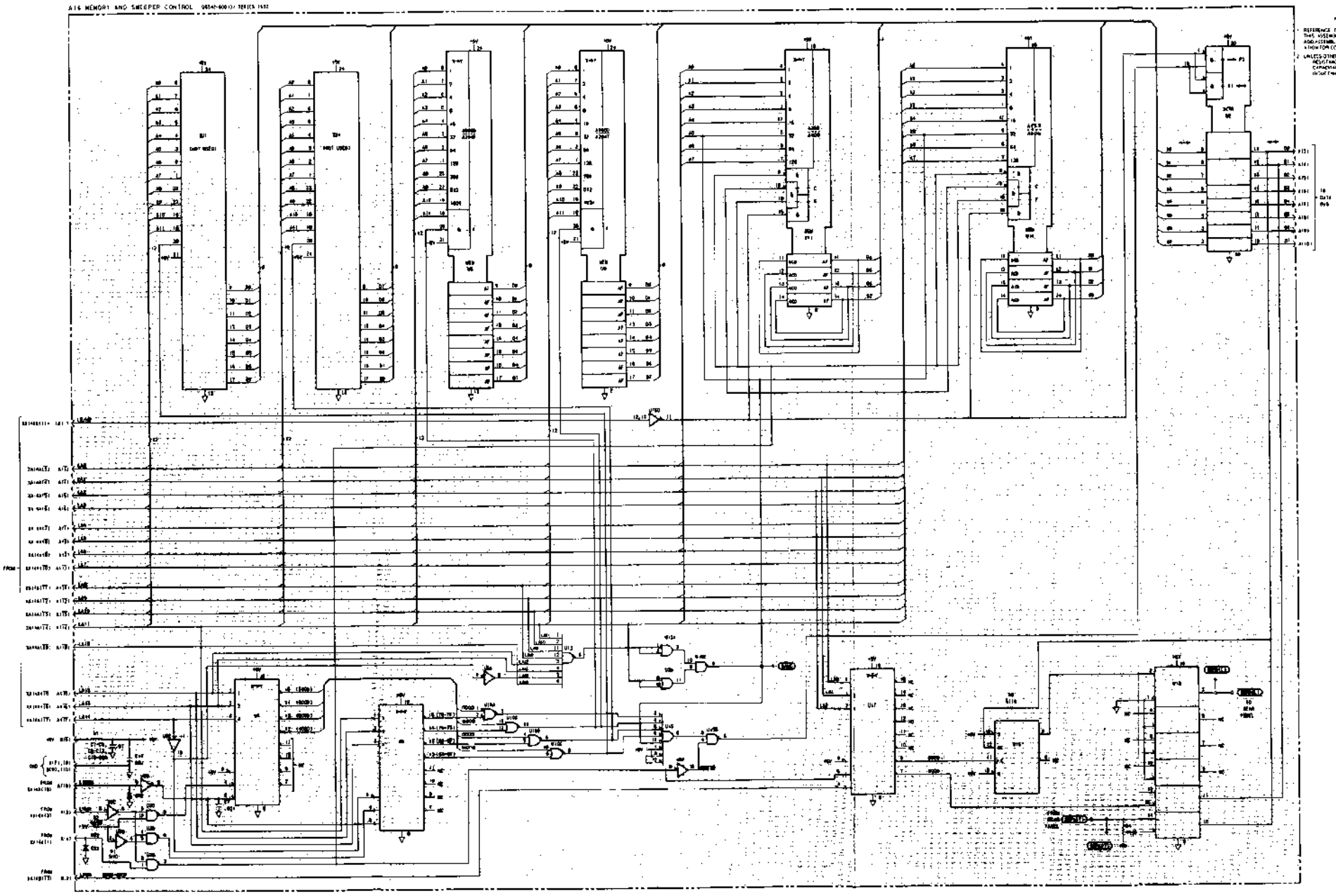
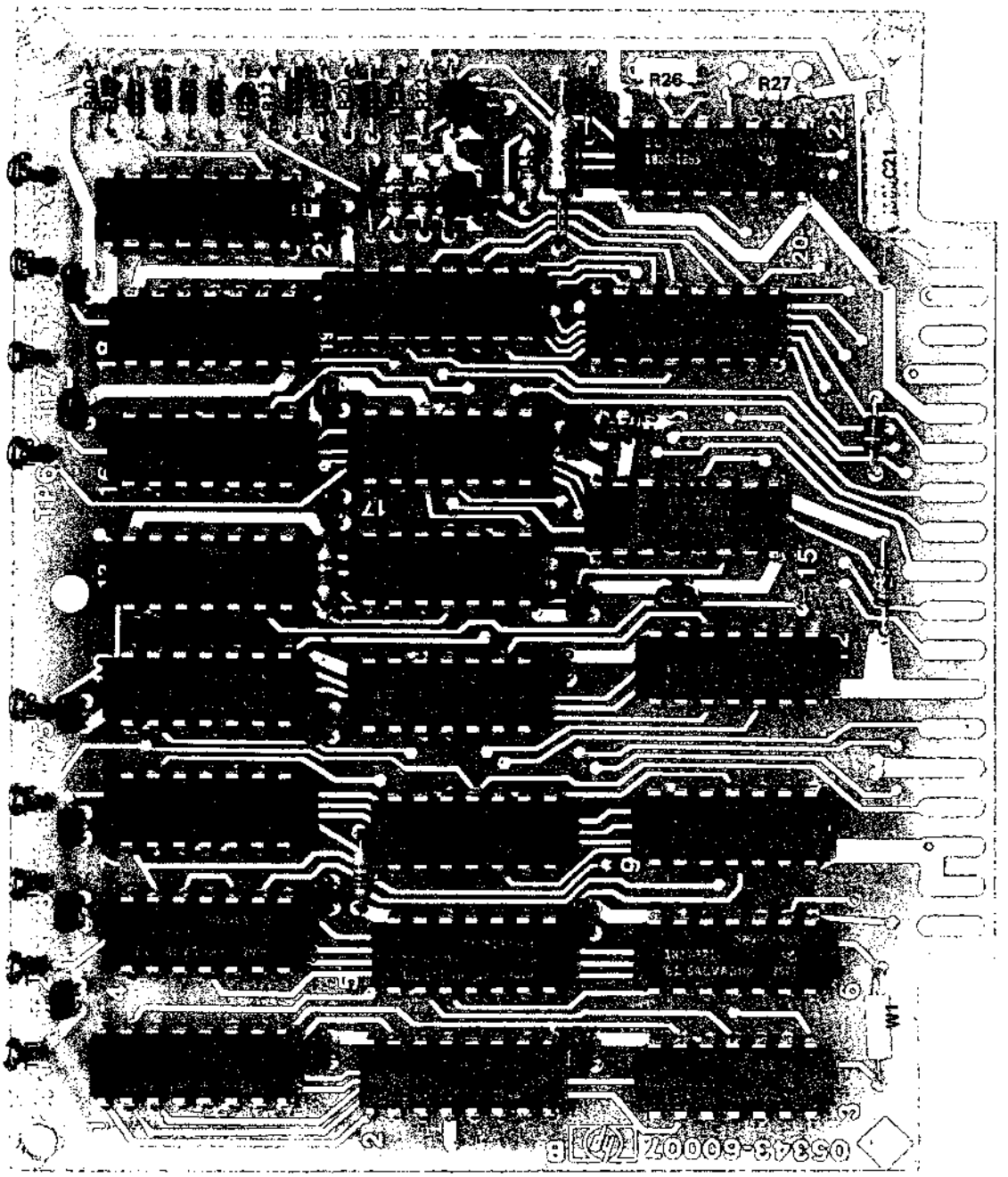


Figure 8-39. A16 Memory and Sweeper Control Assembly



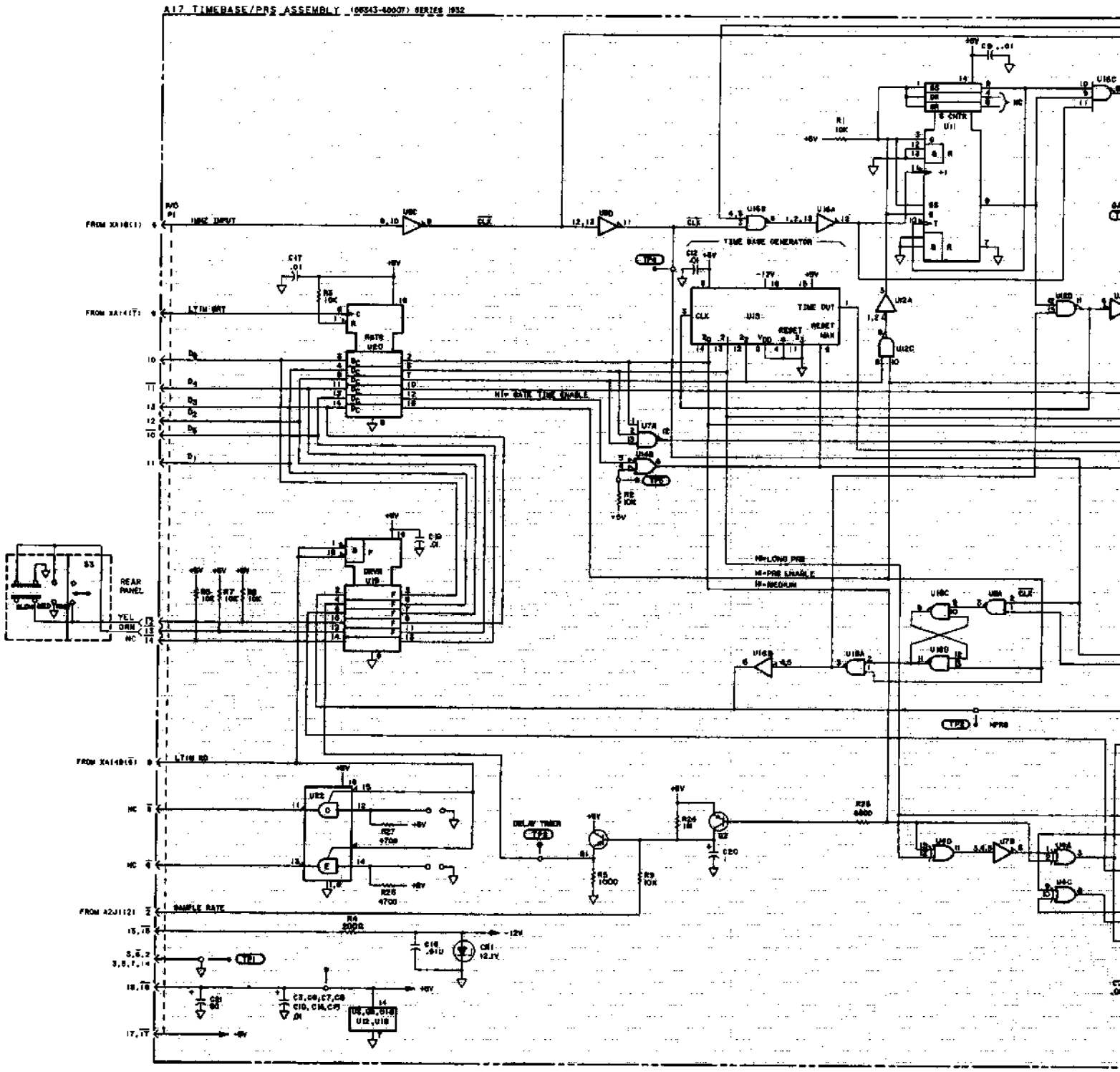
Part of Figure 8-40. A17 Timing Generator Assembly

REFERENCE DESIGNATIONS

A17
C1, C21
CR1
Q1, Q2
R1-R27
TP1-TP9
U1-U22

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1	1902-3182	FZ7268
Q1	1854-0560	SP36740
Q2	1853-0036	2N3906
U1, U2	1820-1430	AM74LS161N
U3,U8,U12,U14,U18	1820-1197	SN74LS00N
U5, U10, U13	1820-1433	SN74LS164N
U4, U6	1820-1211	SN74LS86N
U9, U17	1820-1112	SN74LS74N
U7, U16	1820-1202	9LS10PC
U11	1820-1442	SN74LS290N
U15	1820-1180	MK5009P
U21	1820-1225	MC10231P
U19	1820-1254	DM8095N
U20	1820-1196	AM74LS174N
U22	1820-1255	DM8098N



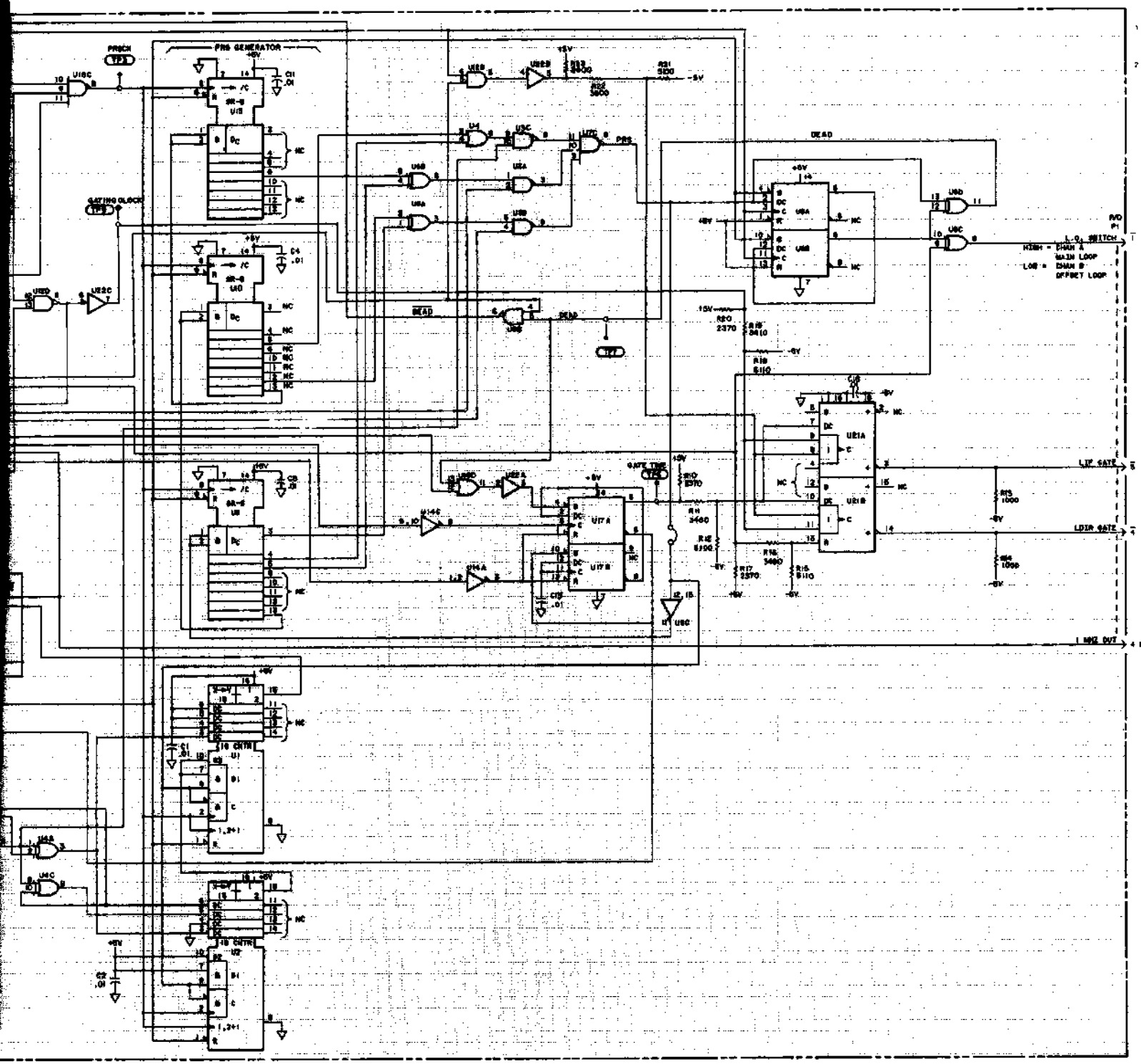


Figure 8-40. A17 Timing Gener

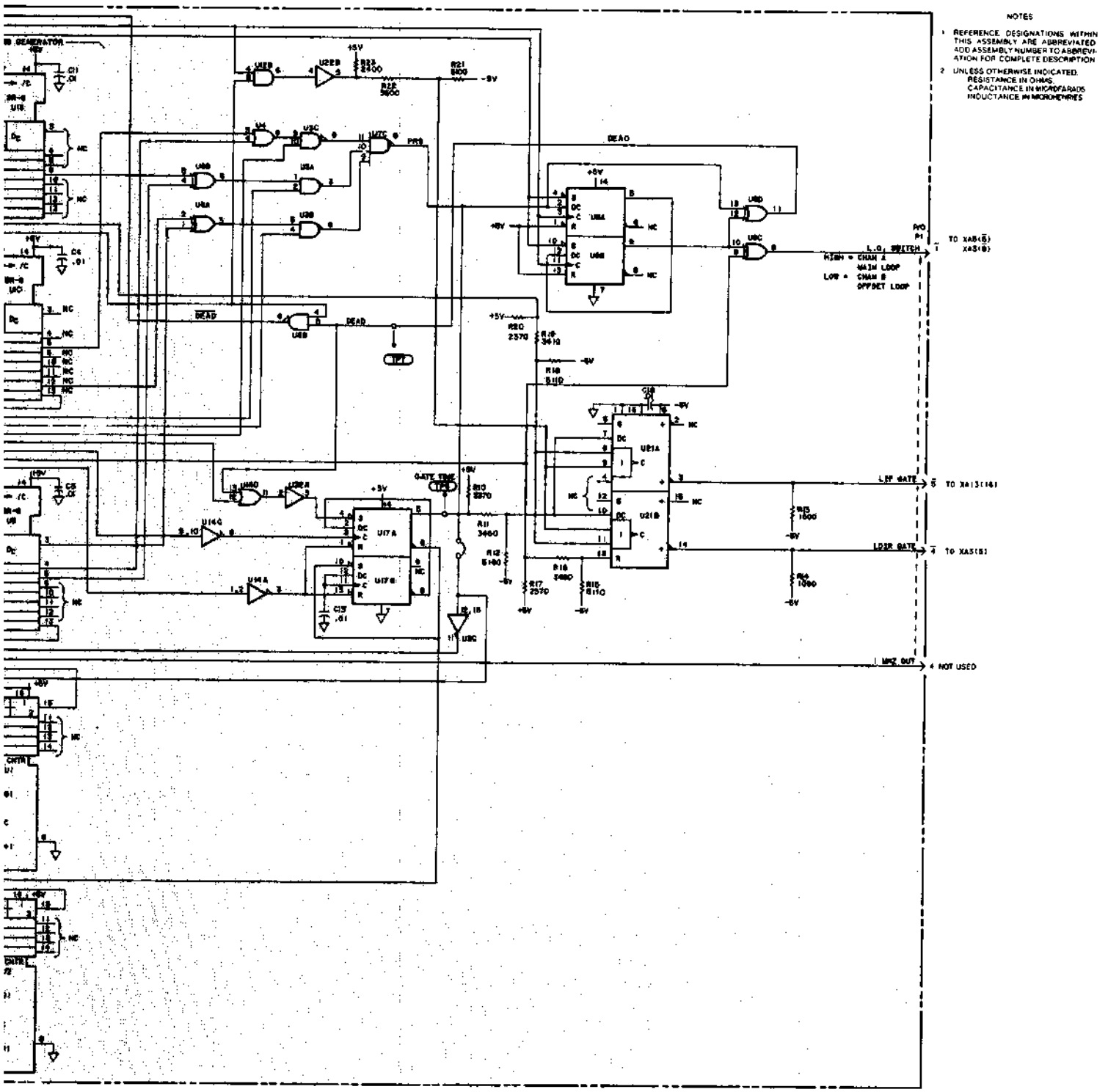
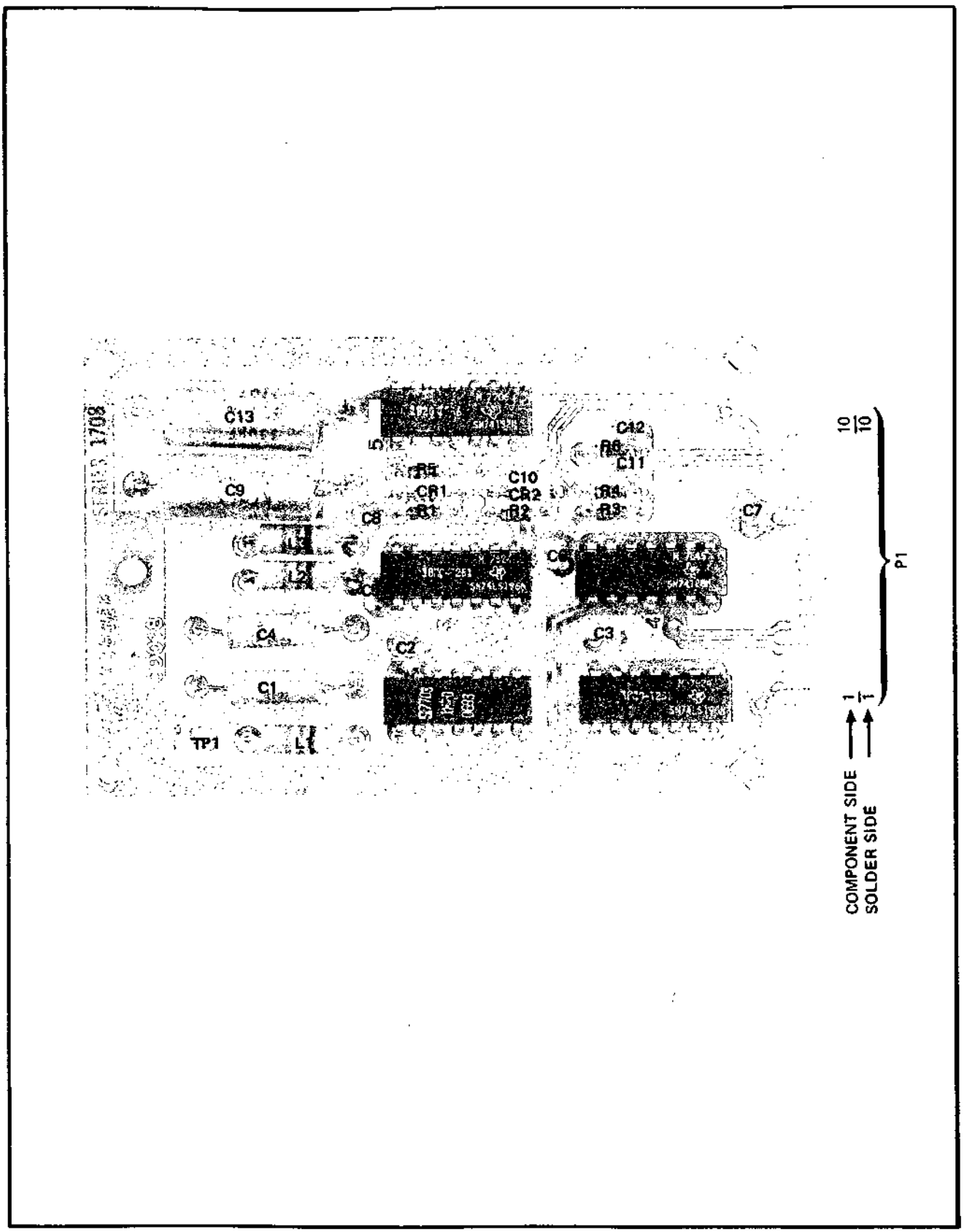


Figure 8-40. A17 Timing Generator Assembly



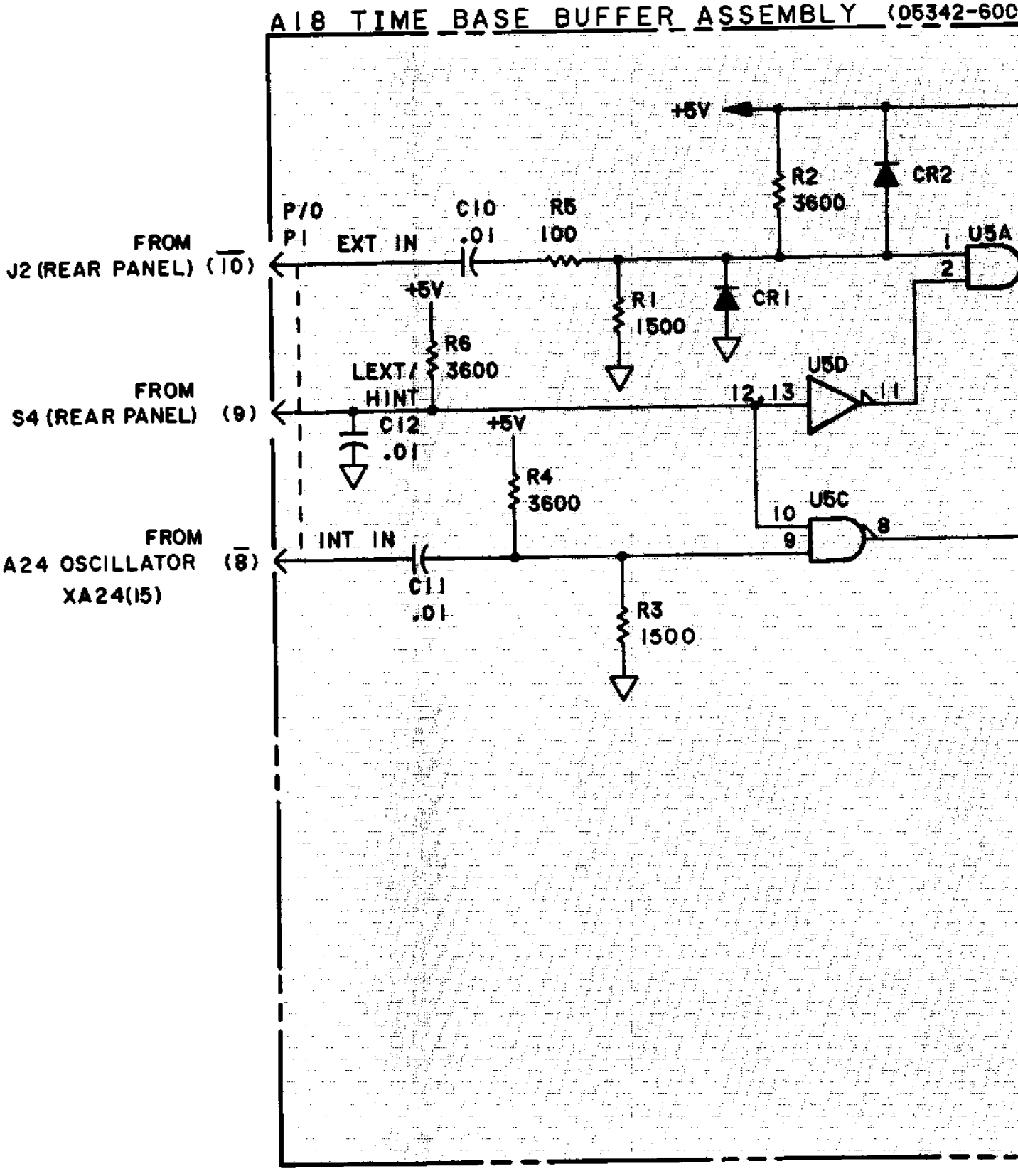
Part of Figure 8-41. A18 Time Base Buffer Assembly

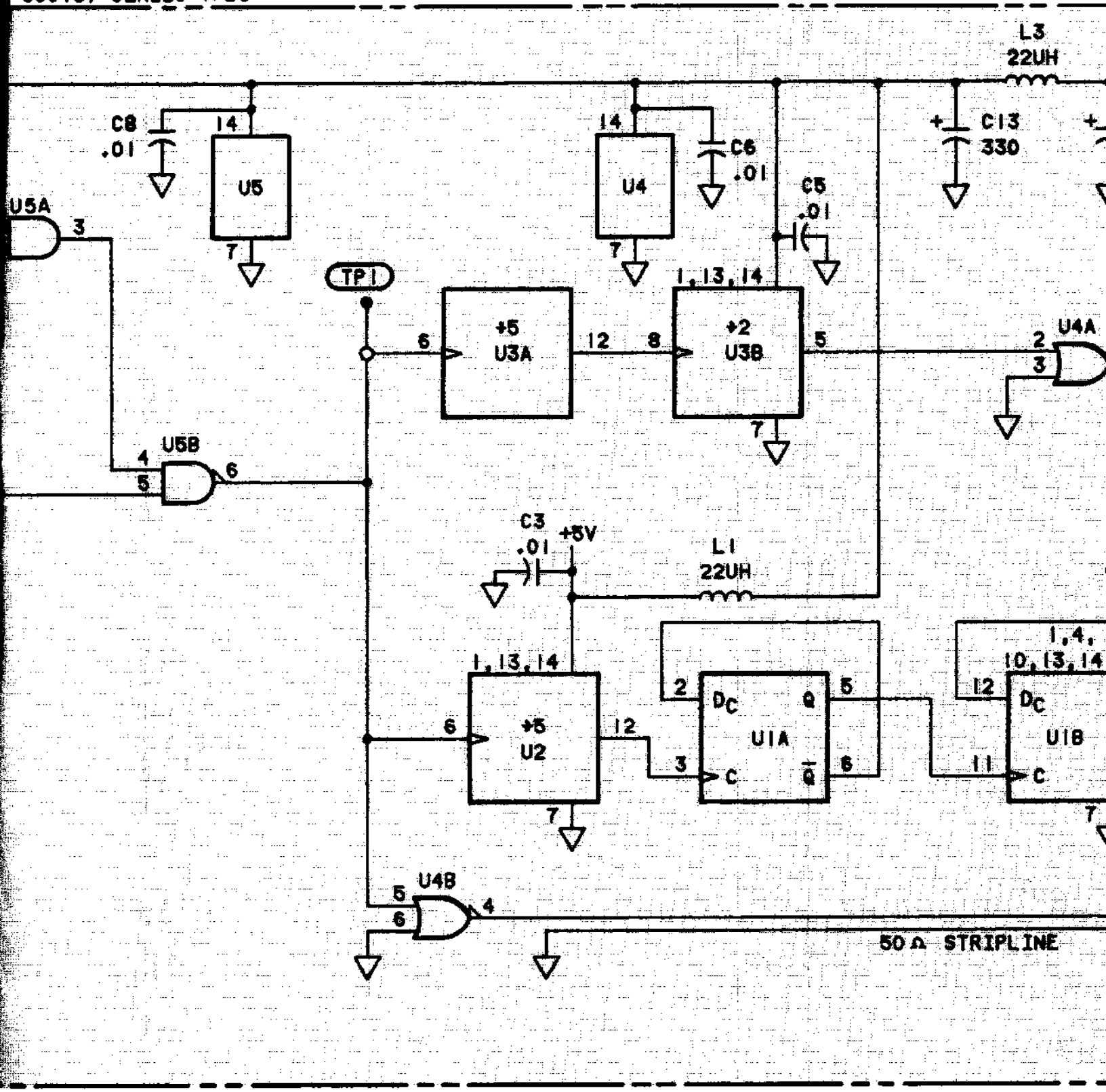
REFERENCE DESIGNATIONS

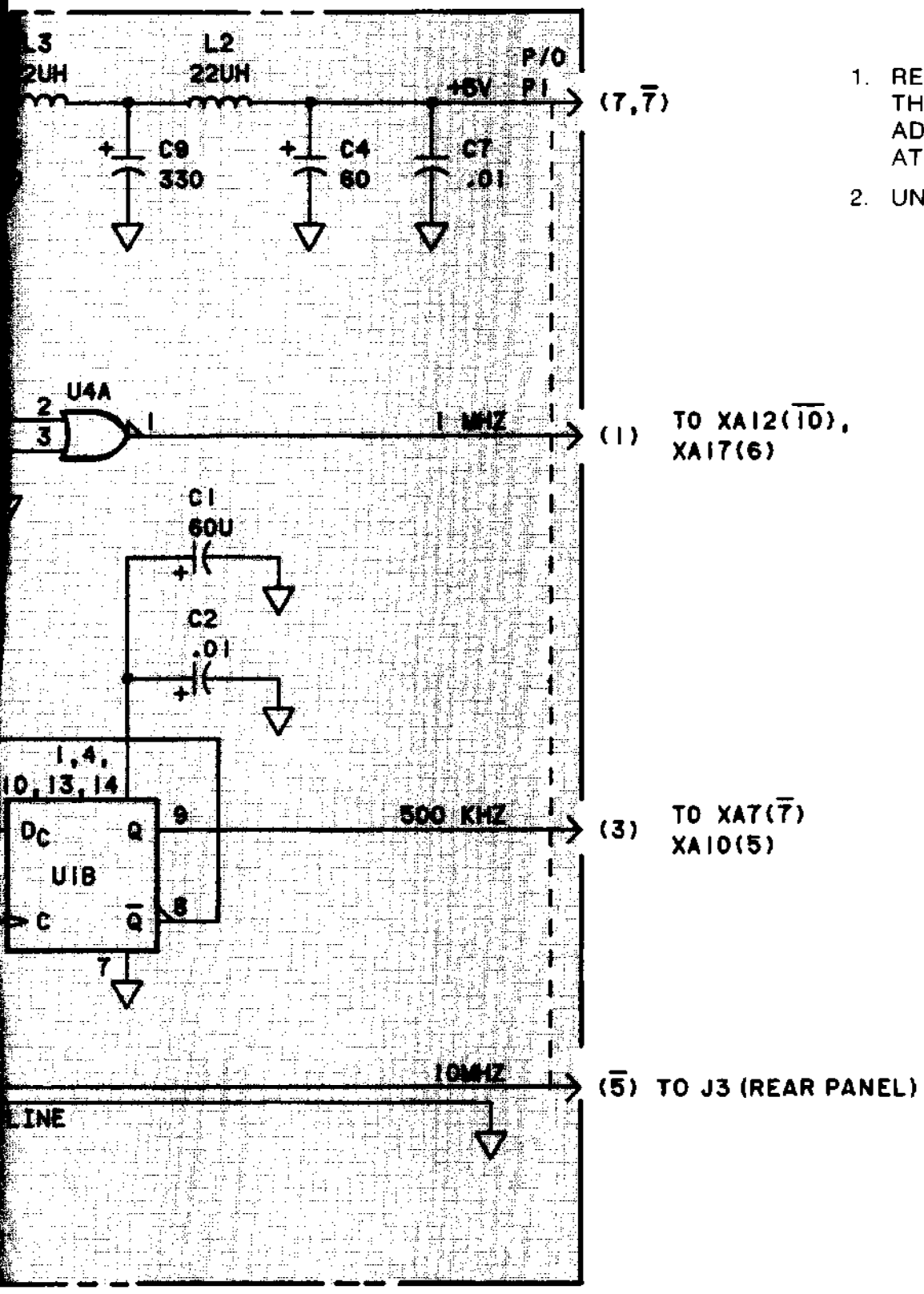
A18
C1-C13 CR1, CR2 L1-L3 R1-R6 TP1 U1-U5

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1, CR2	1901-0040	Same
U1	1820-0693	74S74PC
U2, U3	1820-1251	SN74LS196N
U4	1820-1074	SN74128N
U5	1820-1056	SN74132N



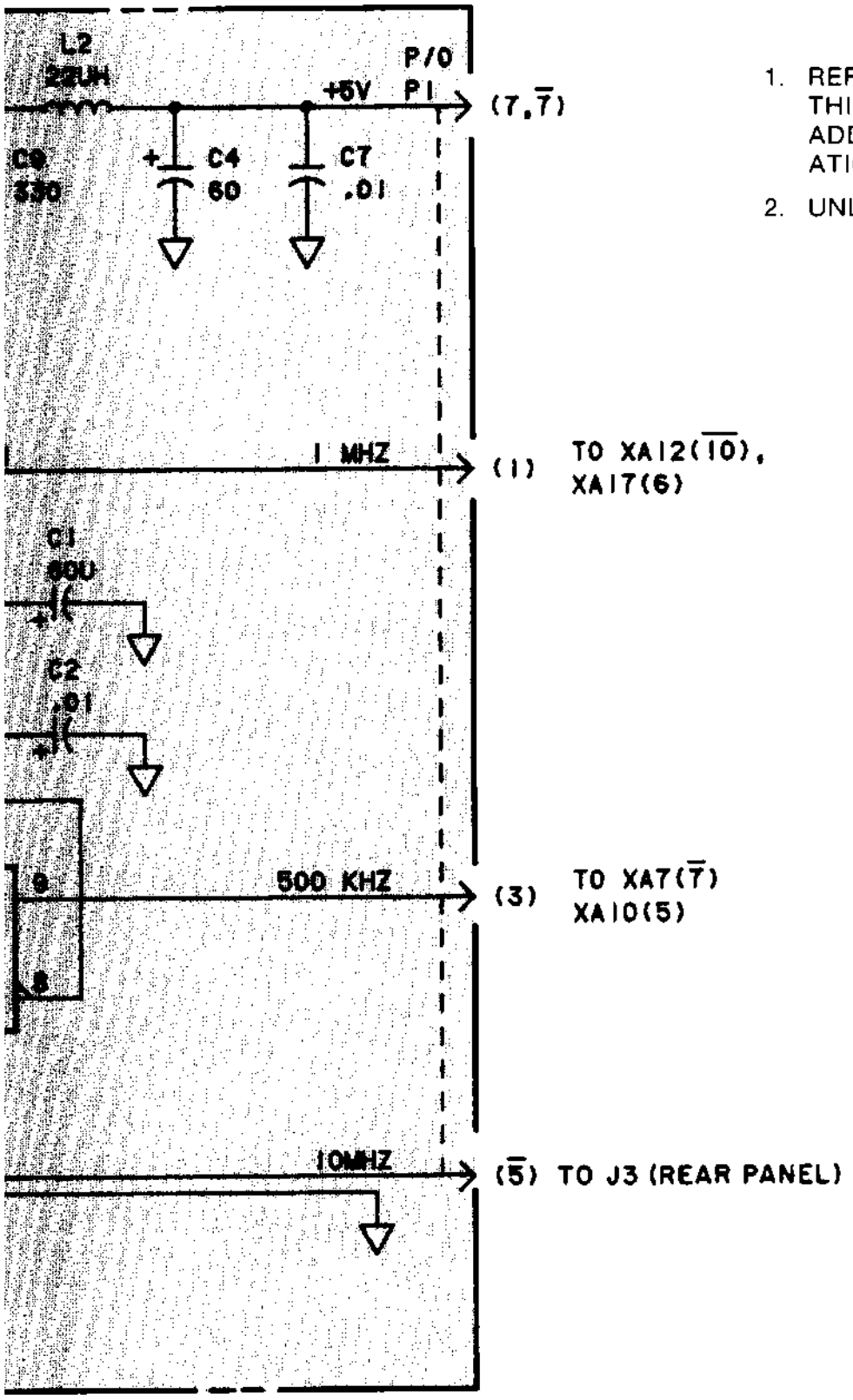




NOTES

1. REFERENCE DESIGNATIONS WIT
THIS ASSEMBLY ARE ABBREVIAT
ADD ASSEMBLY NUMBER TO ABBRI
ATION FOR COMPLETE DESCRIPTI
2. UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS;
CAPACITANCE IN MICROFARADS
INDUCTANCE IN MICROHENRIES

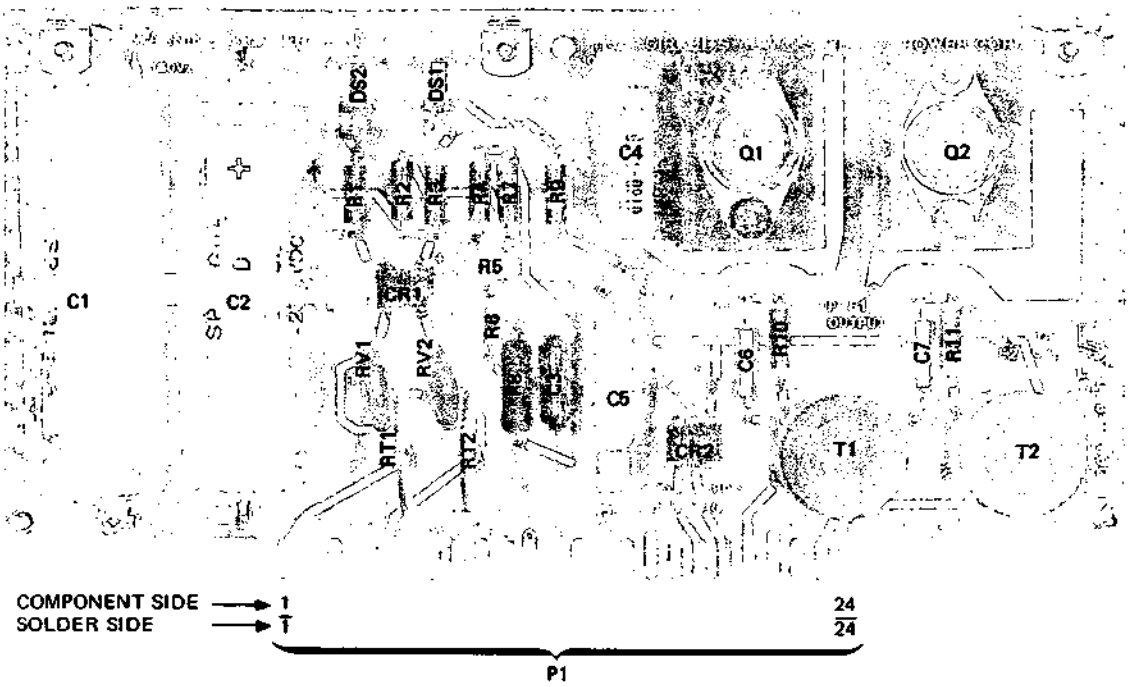
Figure 8-41. A18 Time Base Buffer Asser



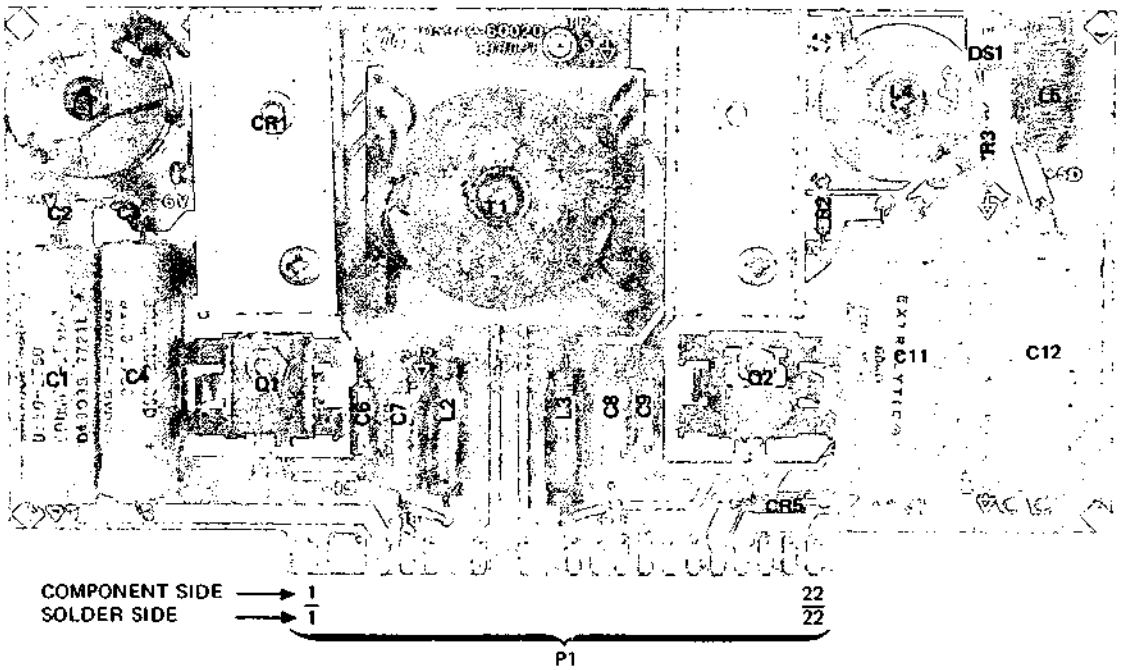
NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN MICROFARADS
   INDUCTANCE IN MICROHENRIES

Figure 8-41. A18 Time Base Buffer Assembly

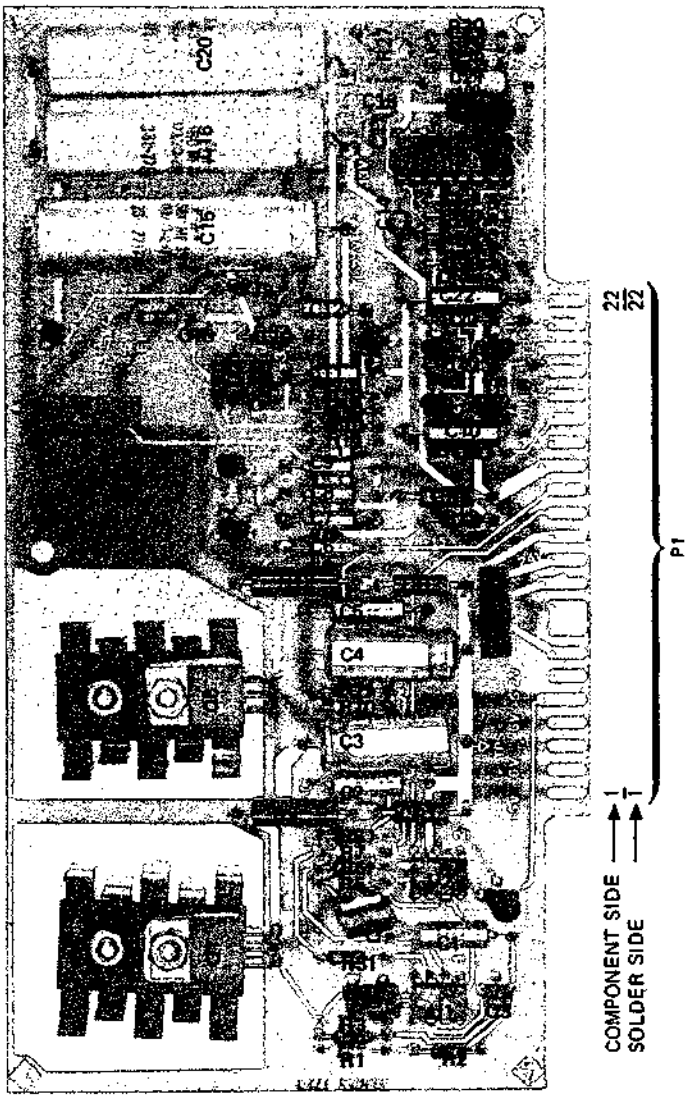


A19



A20

Part of Figure 8-42. A19, A20, A21, and A23 Power Supply



A21

REFERENCE DESIGNATIONS

A19
C1-C7
CR1, CR2
DS1, DS2
Q1, Q2
R1-R11
RT1, RT2
RV1, RV2
T1, T2
TP1-TP6

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1	1906-0069	Same
CR2	1990-0543	Same
DS1, DS2	2140-0018	A9A-C

REFERENCE DESIGNATIONS

A20
C1-C12
CR1-CR5
DS1
L1-L5
R1-R3
T1
U1, U2

TABLE OF ACTIVE ELEMENTS

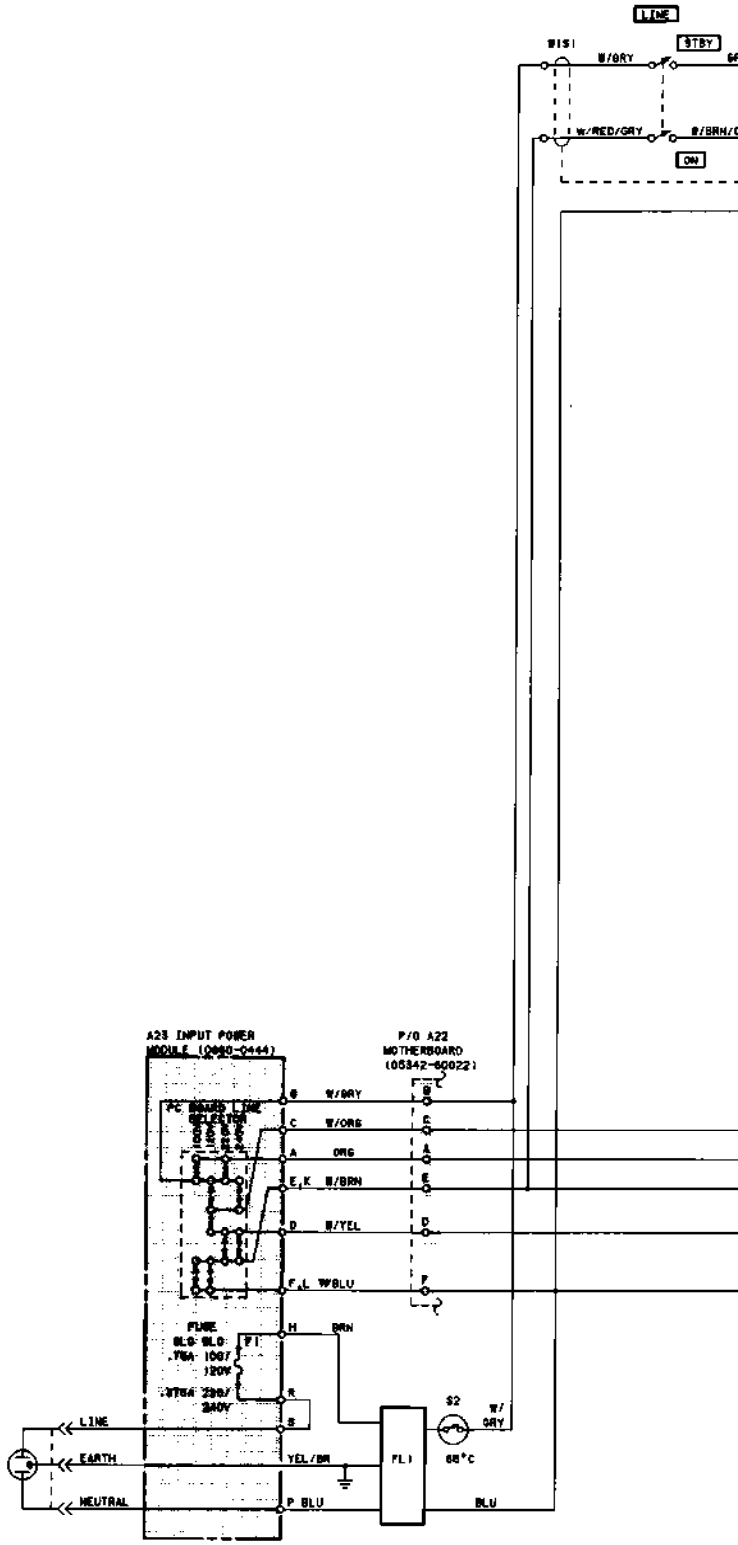
REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1	1906-0079	Same
CR2	1906-0051	Same
CR3, CR4	1901-0784	Same
CR5	1902-0522	IN5340B
DS1	1990-0485	Same
U1	1826-0214	MC7915CT
U2	1826-0106	7815UC

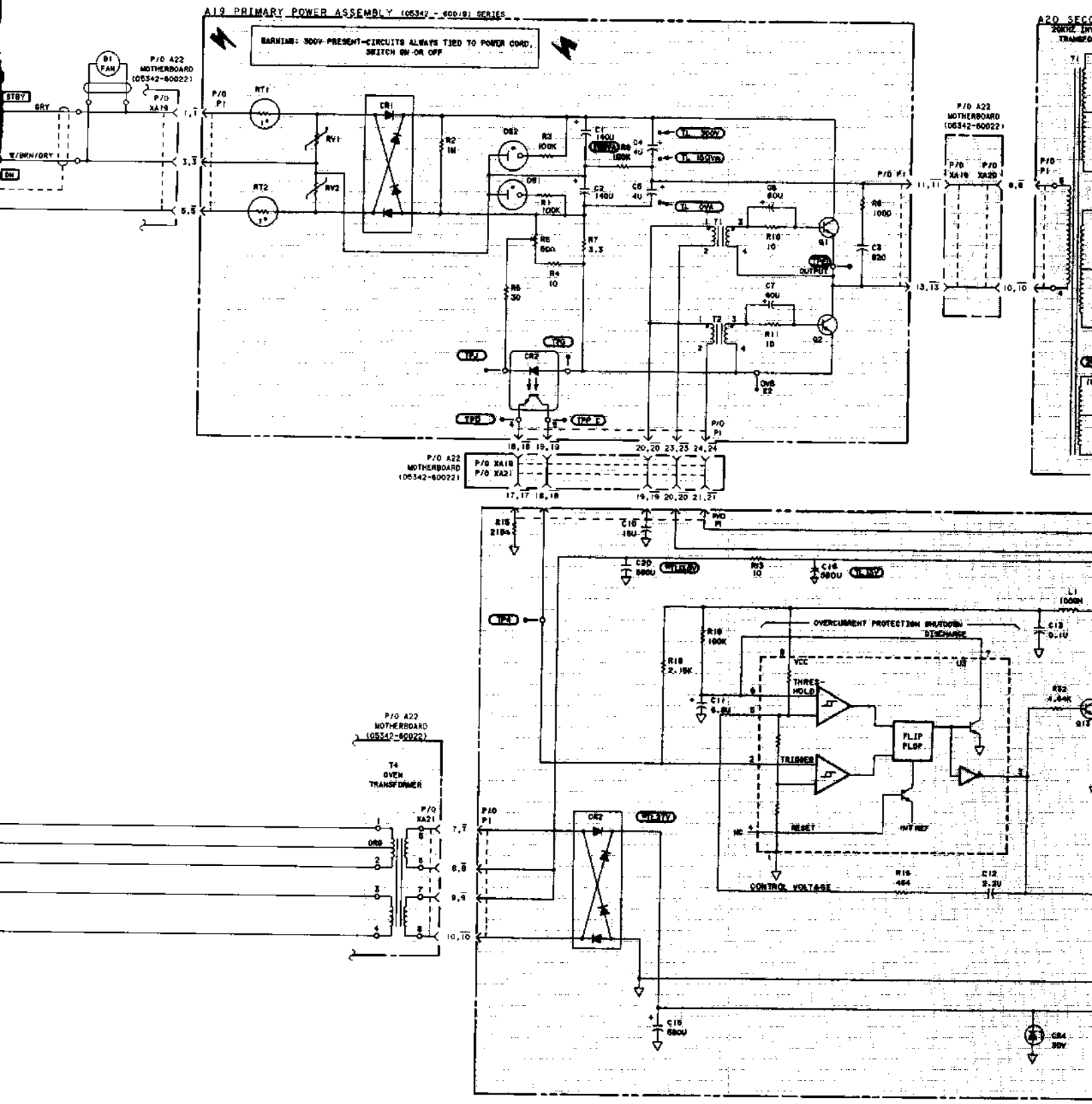
REFERENCE DESIGNATIONS

A21
C1-C22
CR1-CR5
DS1
L1
Q1-Q13
R1-R33
TP1-TP8
U1-U4

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1, CR3	1902-0522	IN5340B
CR2	1906-0096	MDA202
CR4	1902-0644	Same
CR5	1901-0040	Same
DS1	1990-0486	Same
Q1	1854-0635	D44H5
Q2	1854-0634	MPS-U01
Q3	1854-0215	SPS3611
Q4	1853-0326	Same
Q5	1853-0036	Same
Q6	1853-0363	D45H5
Q7, Q8	1826-0275	78L12AC
Q9, Q11	1854-0246	2N3643
Q10, Q12	1853-0058	S32248
Q13	1854-0215	SPS3611
U1, U2	1820-0493	LM307N
U3	1826-0160	NE555V
U4	1826-0428	SG3524





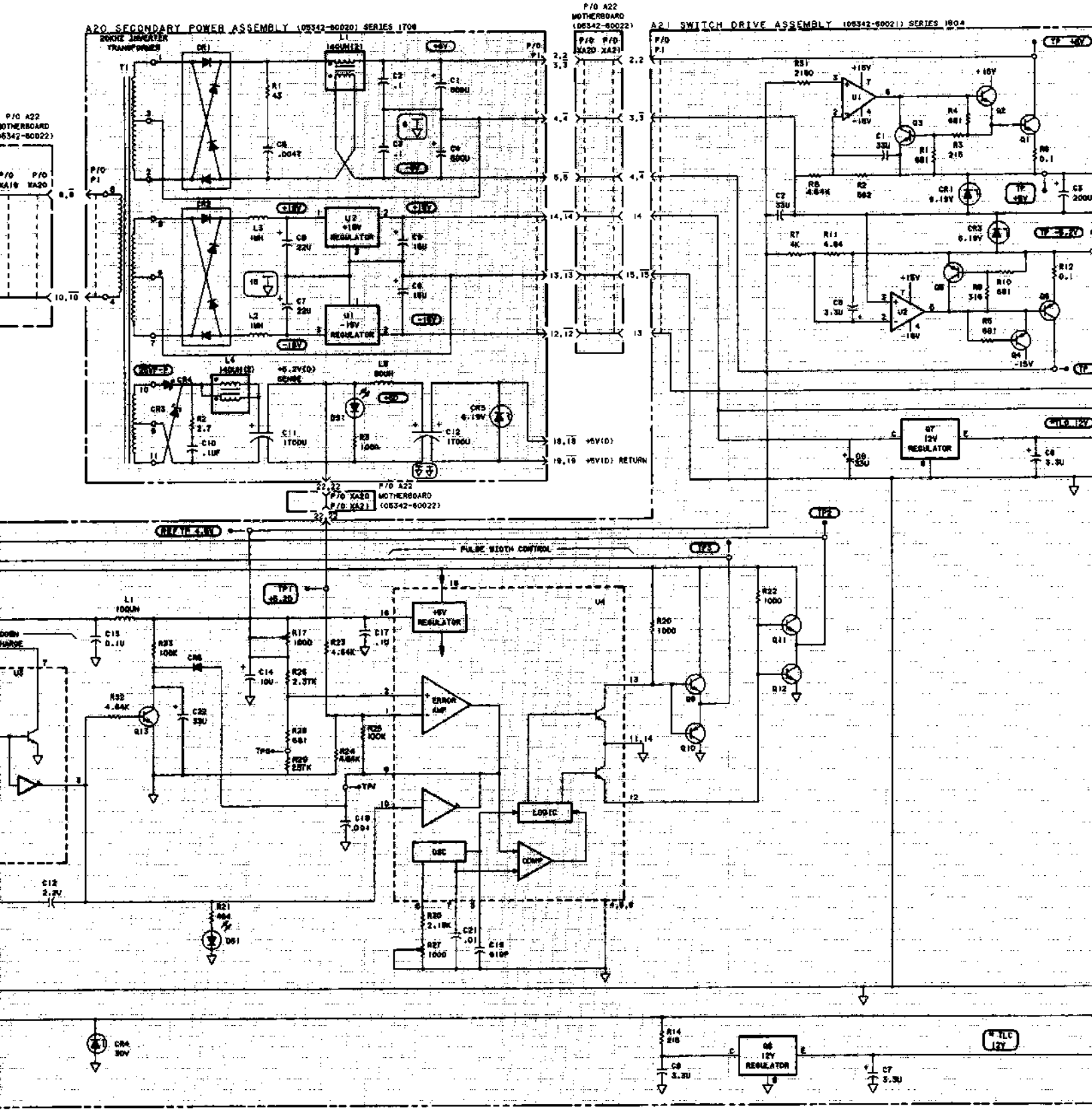


Figure 8-42. A19, A20, A21, and A2

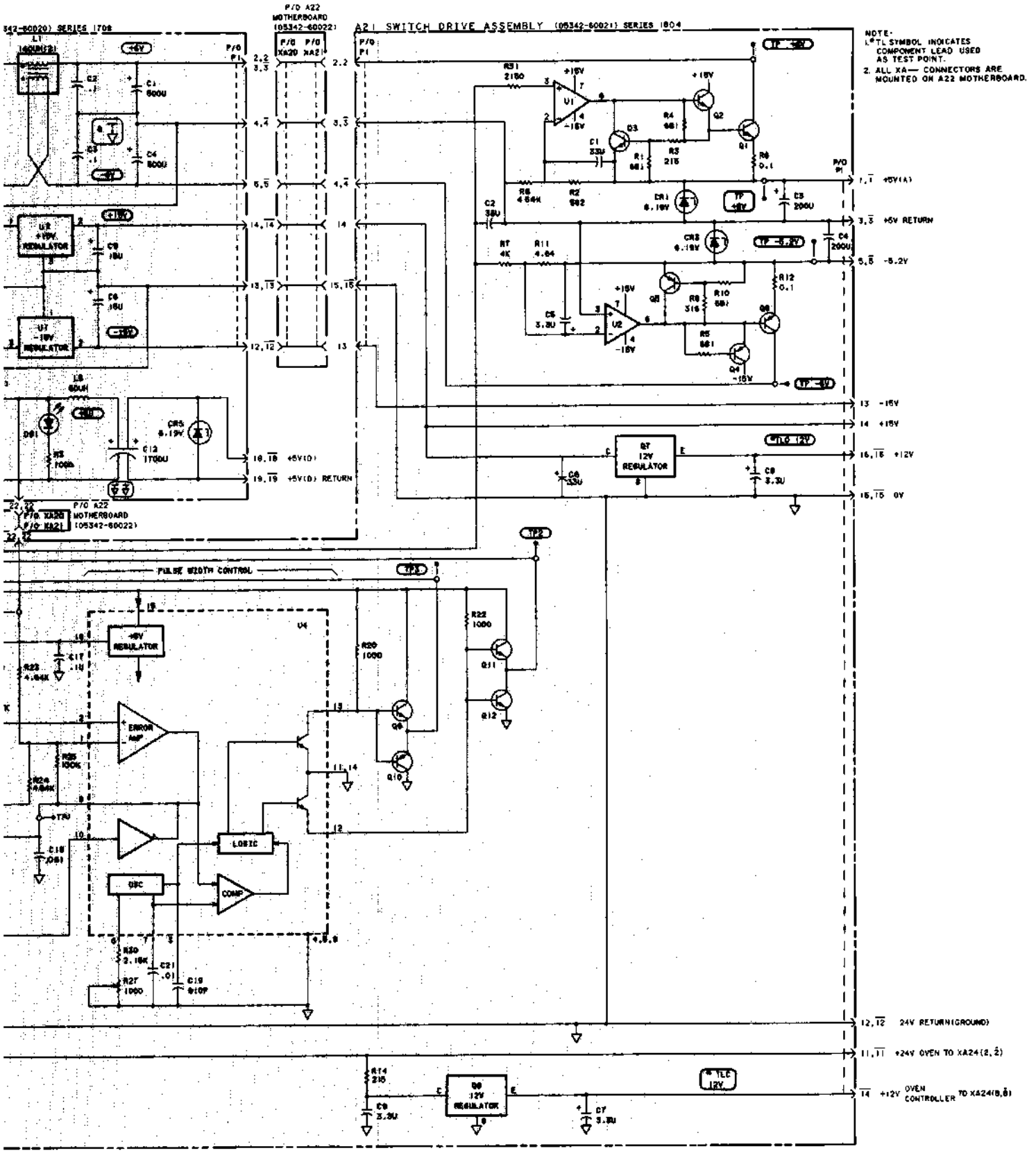
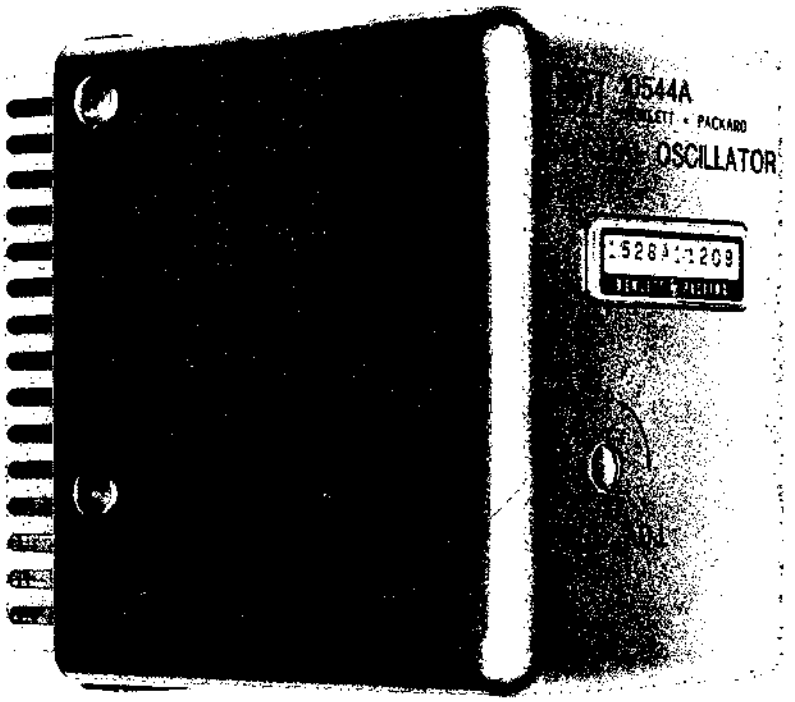
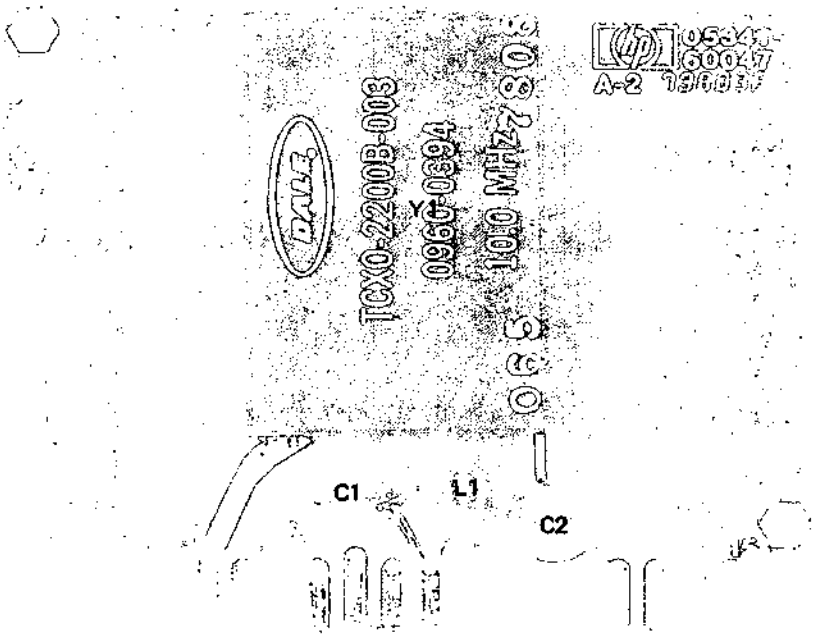


Figure 8-42. A19, A20, A21, and A23 Power Supply Assemblies

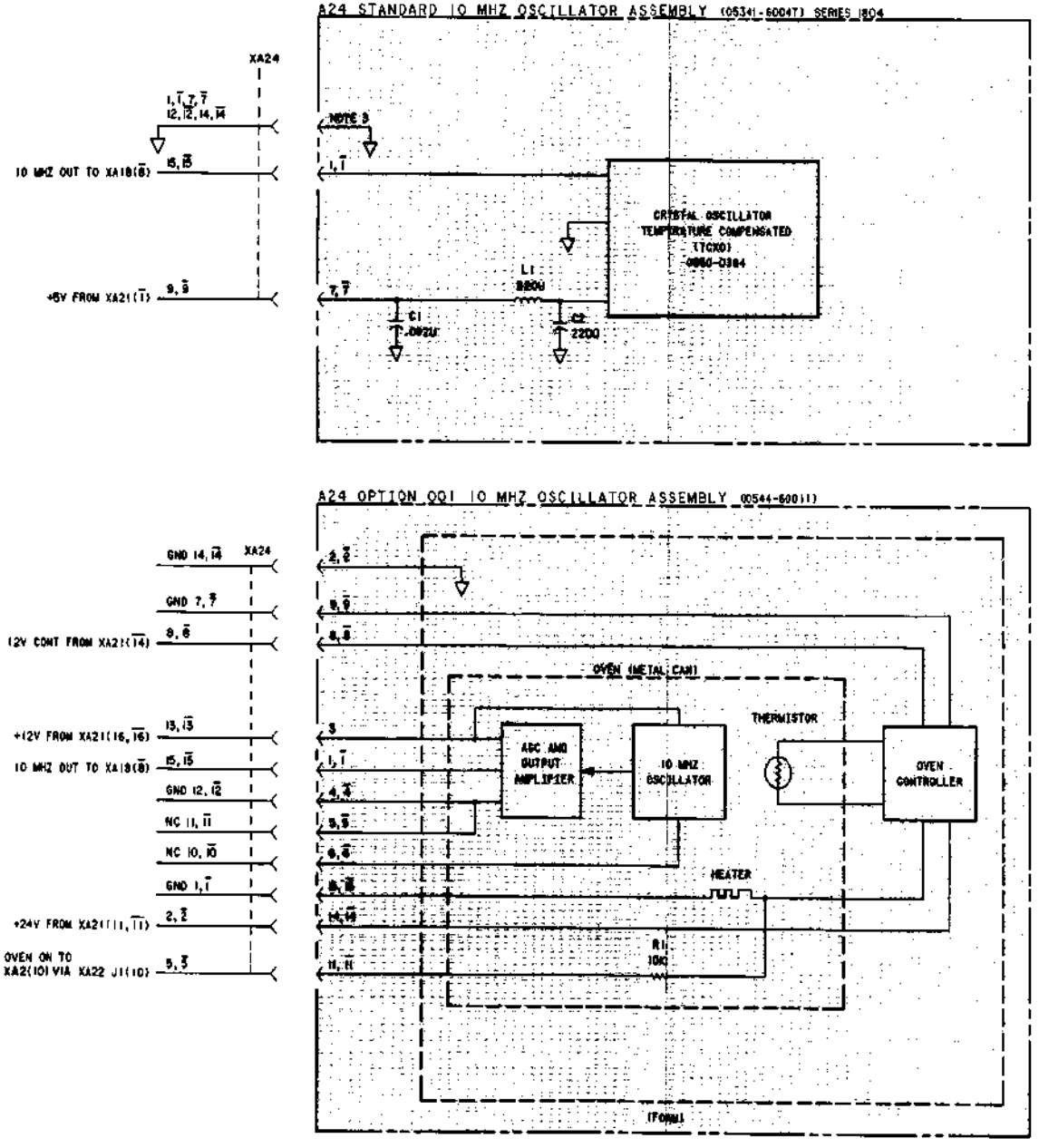


A24 OPTION 001



A24 STANDARD

Part of Figure 8-43. A24 Oscillator Assemblies



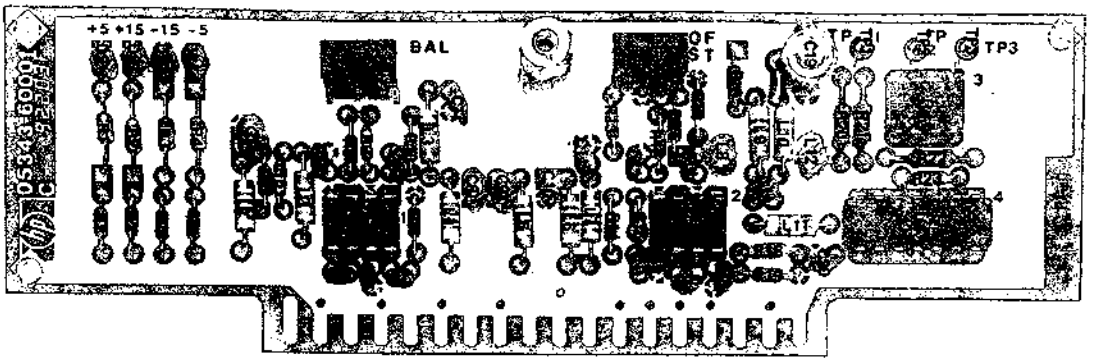
NOTES:

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

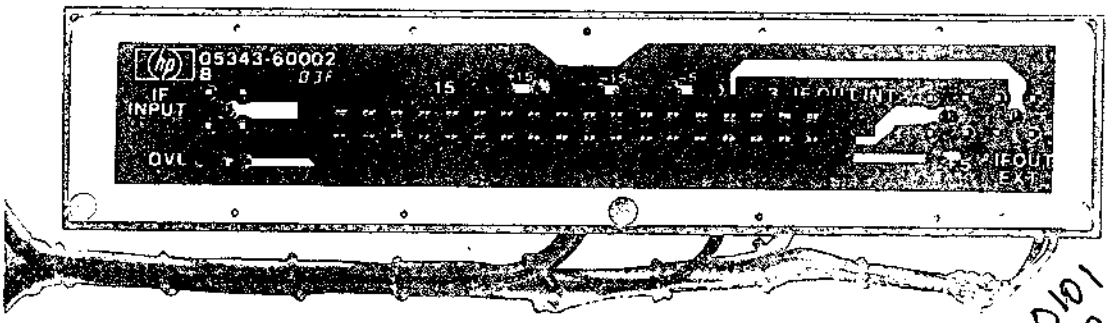
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES

3. THE FOLLOWING ASSEMBLIES ARE NOT FIELD REPAIRABLE
   a. CRYSTAL OSCILLATOR 0960-0384
   b. A24 OPTION 001 10MHZ OSCILLATOR 10544-60011

Figure 8-43. A24 Oscillator Assembly

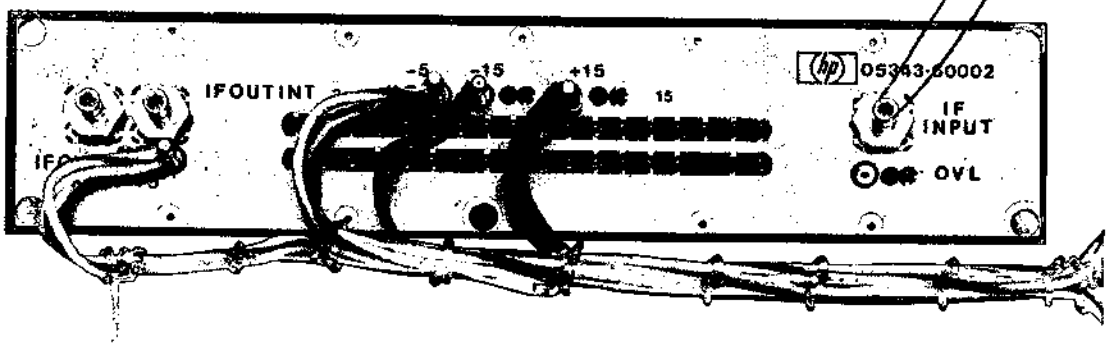


A25A1



A25 TOP

05343-60101 to A28J2



A25 BOTTOM

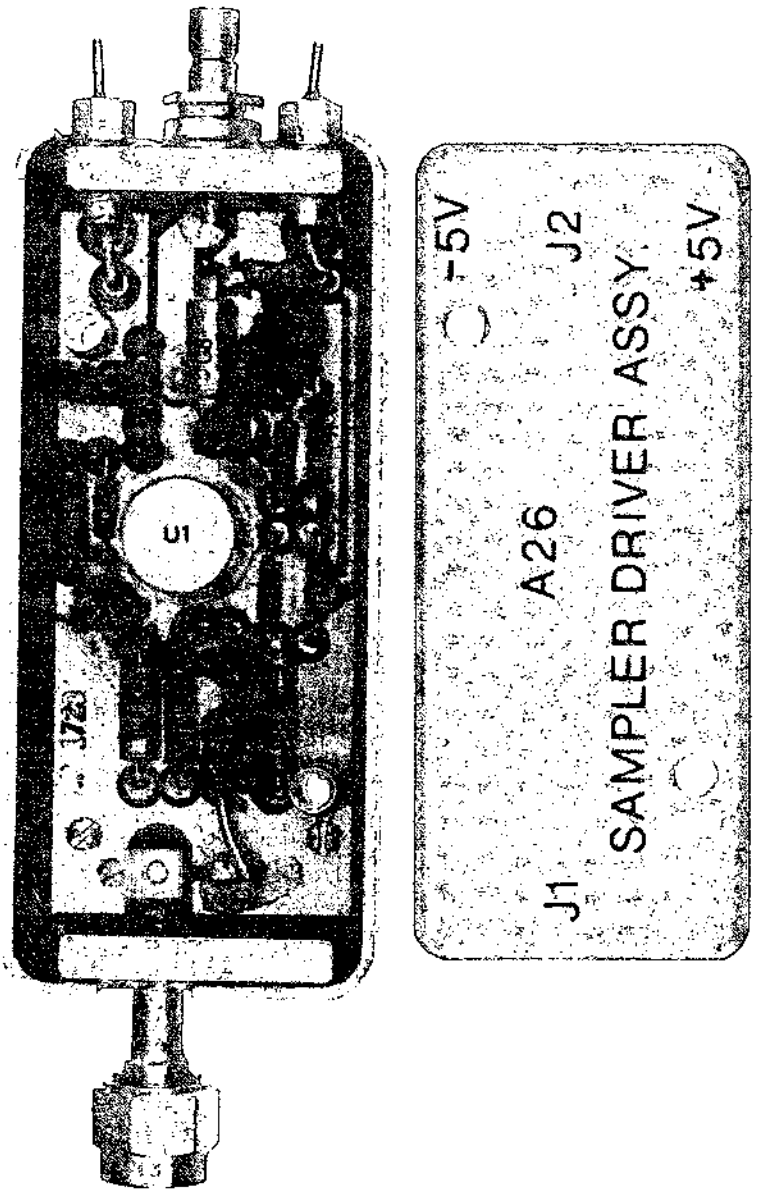
Part of Figure 8-44. A25A1 2nd Preamplifier and A25 Motherboard Assemblies

REFERENCE DESIGNATIONS

A25A1
C1-C20
CR1-CR6
DS1-DS4
L1-L11
R1-R22
RP1-TP5
U1-U4

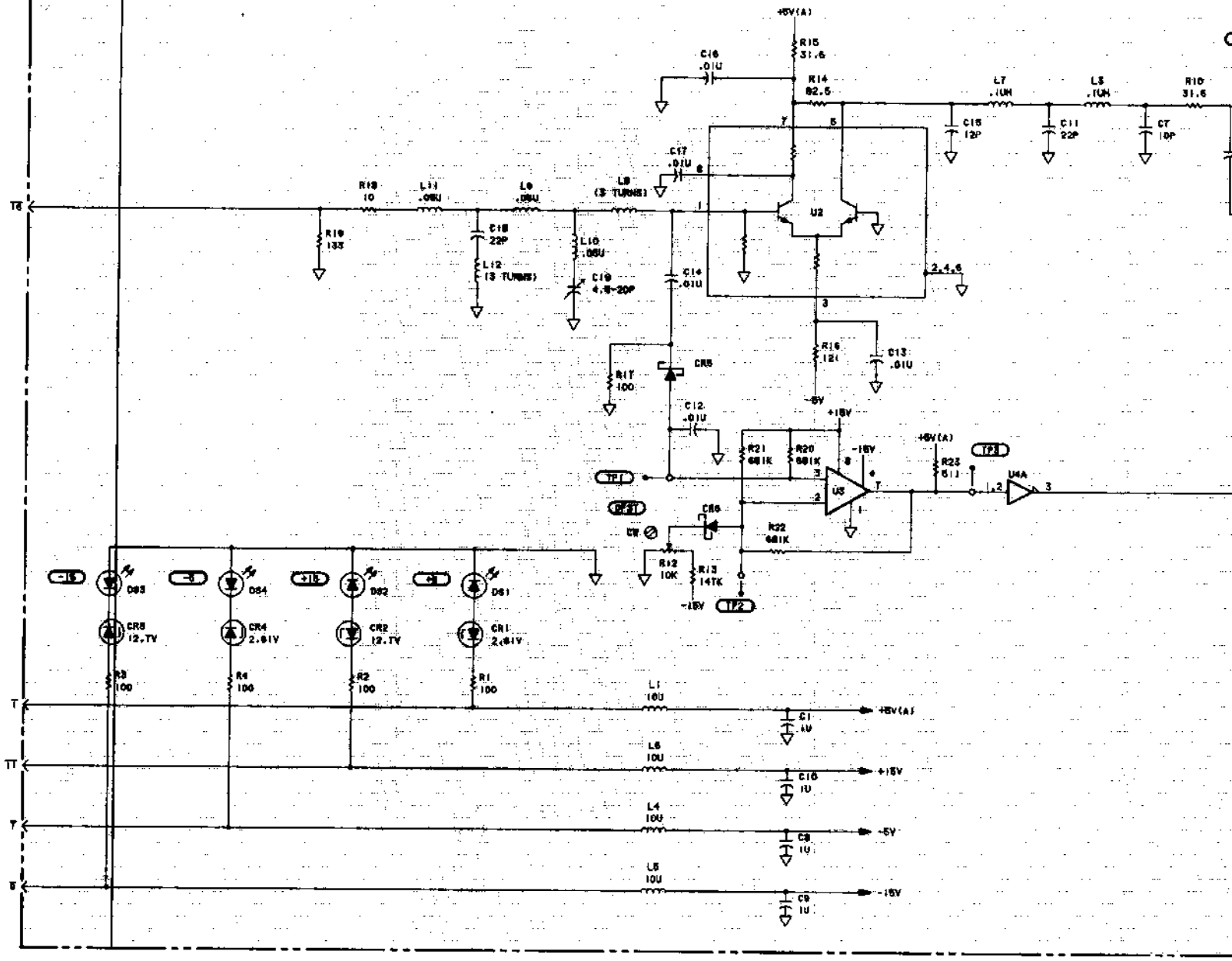
TABLE OF ACTIVE ELEMENTS

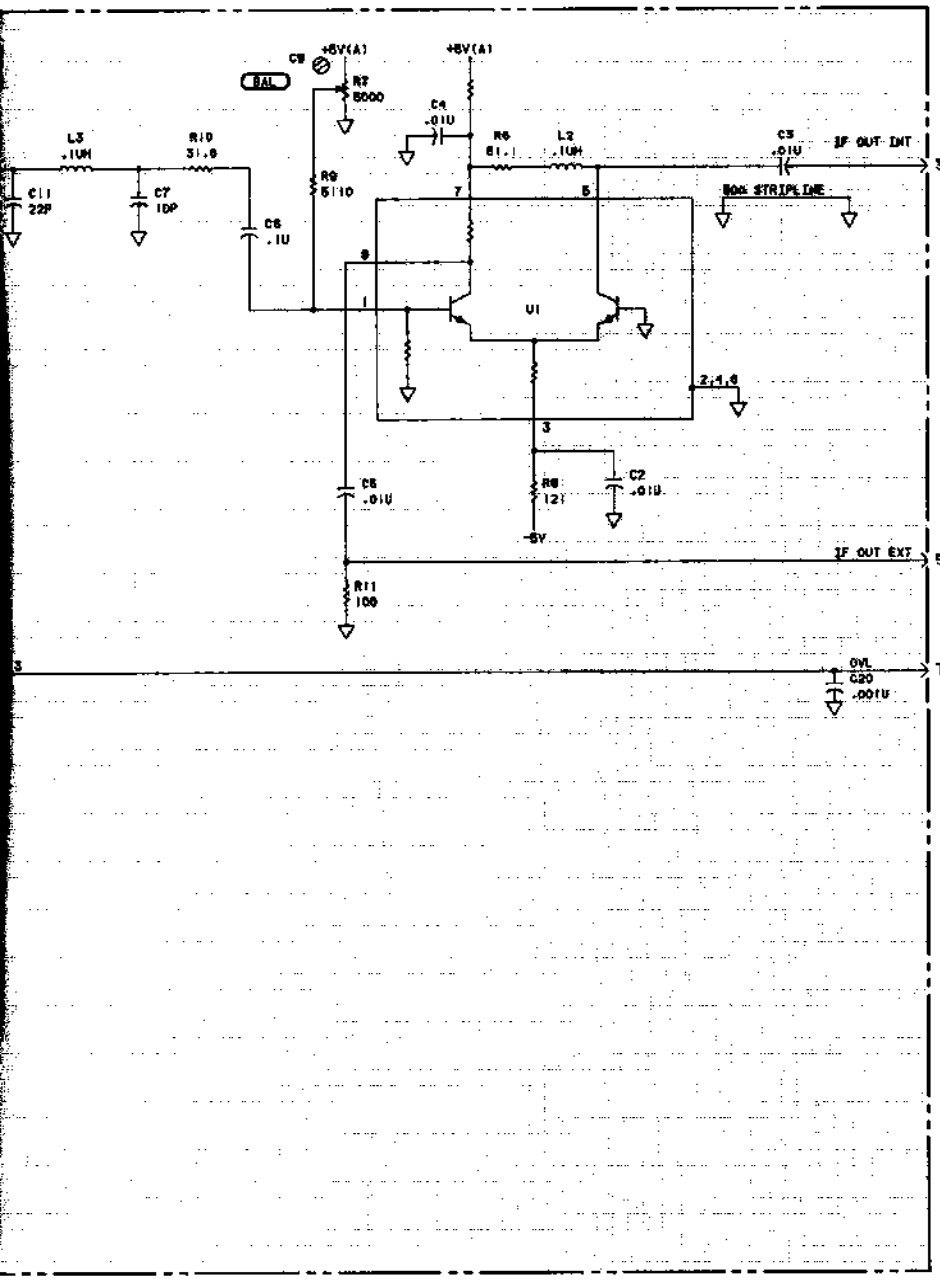
REFERENCE DESIGNATIONS	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1, CR4	1902-0216	Same
CR2, CR3	1902-0126	Same
CR5, CR6	1901-0347	Same
DS1-DS4	1990-0485	Same
U1, U2	1826-0372	Same
U3	1826-0065	LM311N
U4	1820-0254	SN7400N



Part of Figure 8-45. A26 Sampler Driver Assembly

A25A1 SECOND PREAMPLIFIER (05343-60001) SERIES 1932





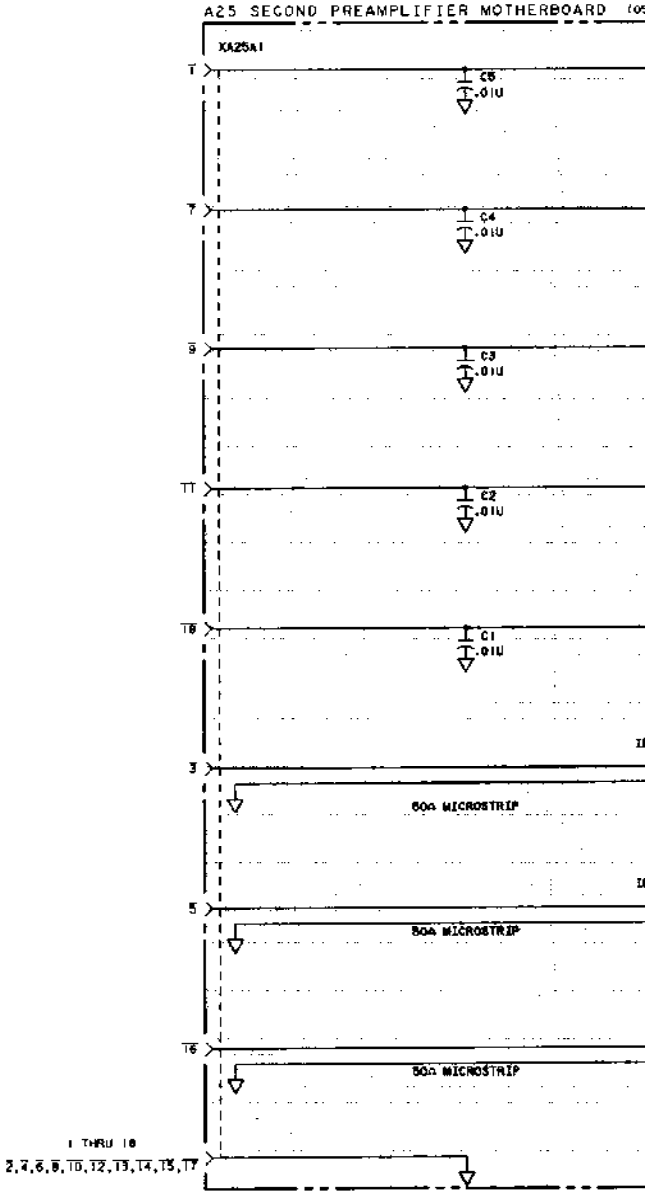


Figure 8-44. A25A1 2nd Preamplifier and A25 M

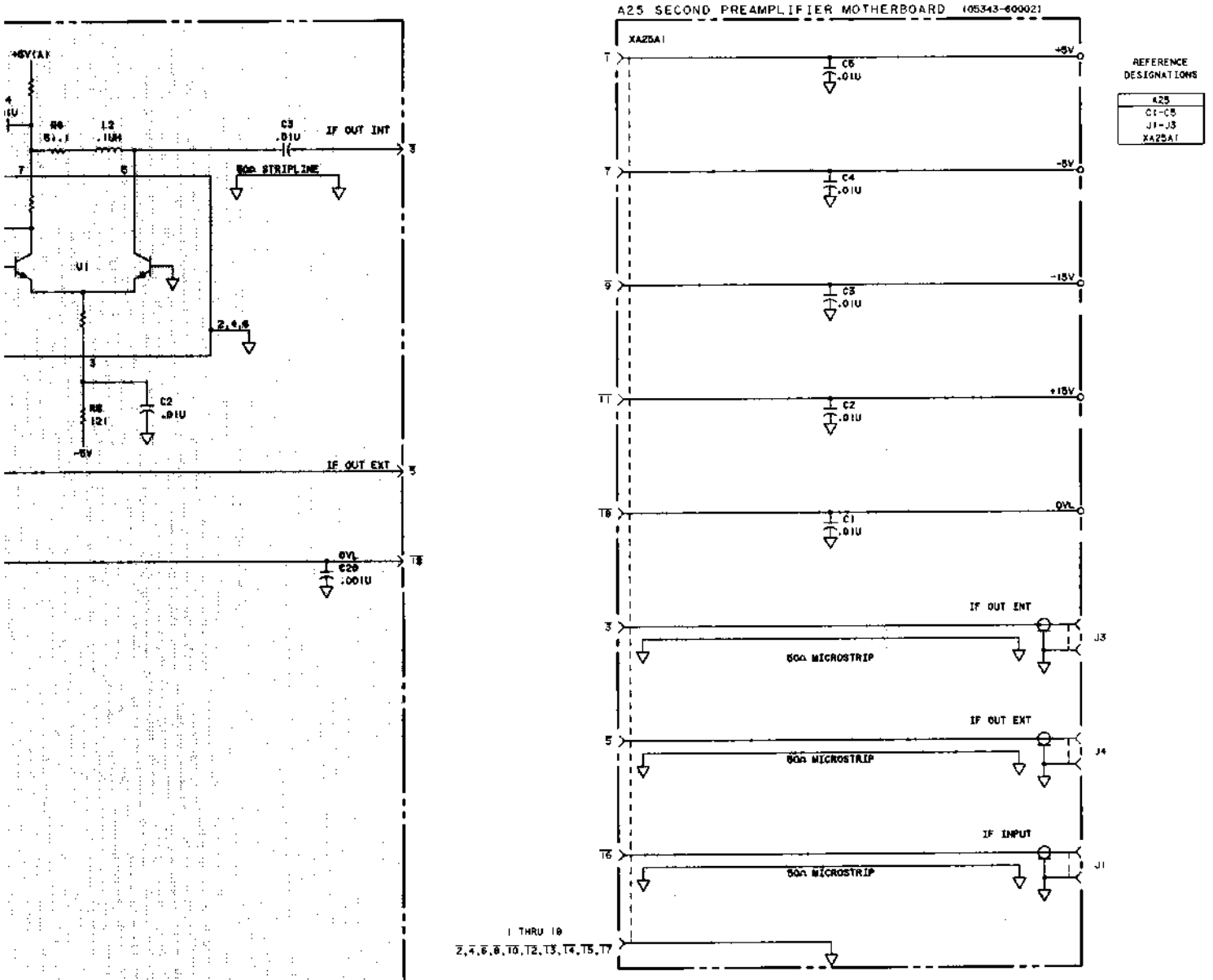


Figure 8-44. A25A1 2nd Preamplifier and A25 Motherboard Assemblies

A26 SAMPLER DRIVER ASSEMBLY

CONDITIONS:

Ground sampler driver to chassis.
Disconnect cable at A26J2.
No signal input, no output.

Q1		U1		CR2		CR1	
E	-5.19	1	+2.75	Anode	-5.187	Anode	ØV
B	-5.19	2	-1.55	Cathode	-5.19	Cathode	-0.03
C	-0.17	3	-0.82				
		4	Ø (Not Used)				
		5	Ø (Not Used)				
		6	-0.80				
		7.	-0.16				
		8	+5.02				

REFERENCE DESIGNATIONS

A26
C1-C14
CR1, CR2
L1
Q1
R1-R8
TP1, TP2
U1

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1	1901-0796	Same
CR2	1901-0179	Same
Q1	1854-0071	Same
U1	1856-0060	Same

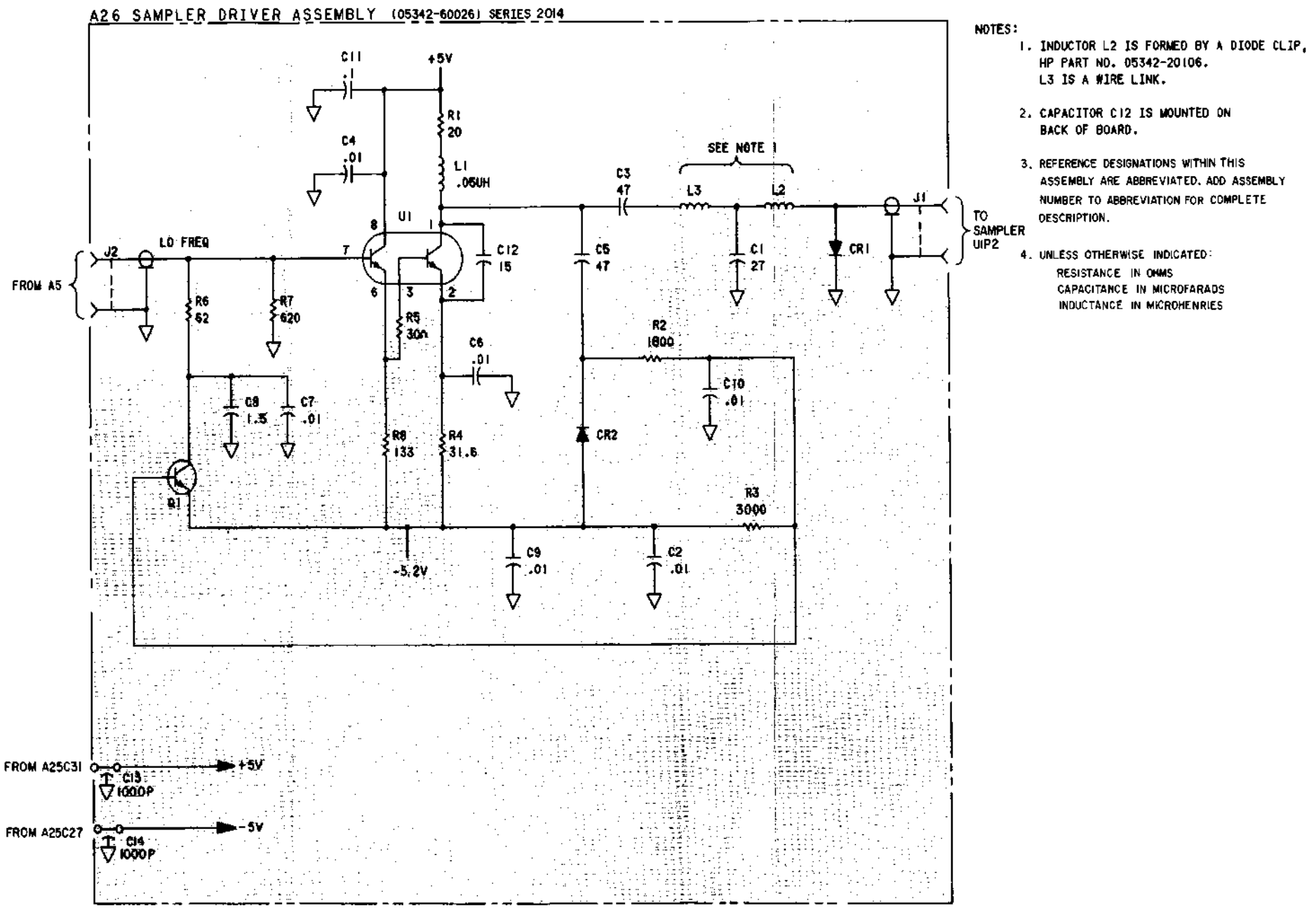
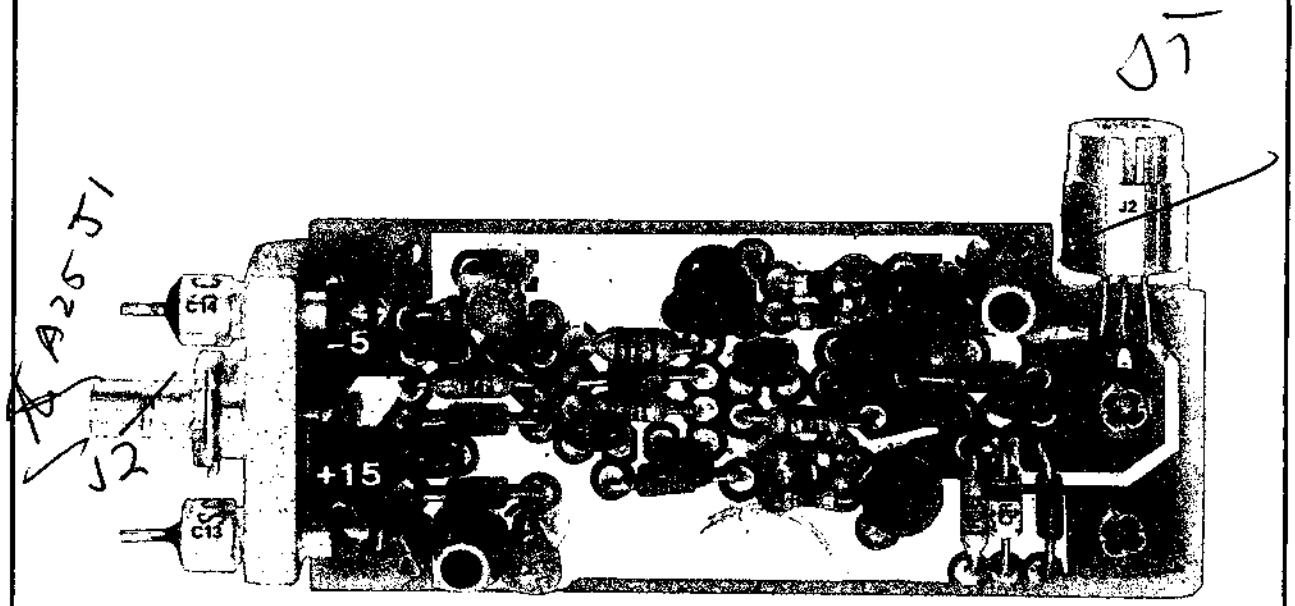


Figure 8-45. A26 Sampler Driver Assembly



Part of Figure 8-46. A28 First Preamplifier Assembly

REFERENCE DESIGNATIONS

A28
C1-C12 CR1 J1, J2 L1 Q1, Q2 R1-R17

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1	1902-3082	Same
Q1, Q2	1854-0591	Same

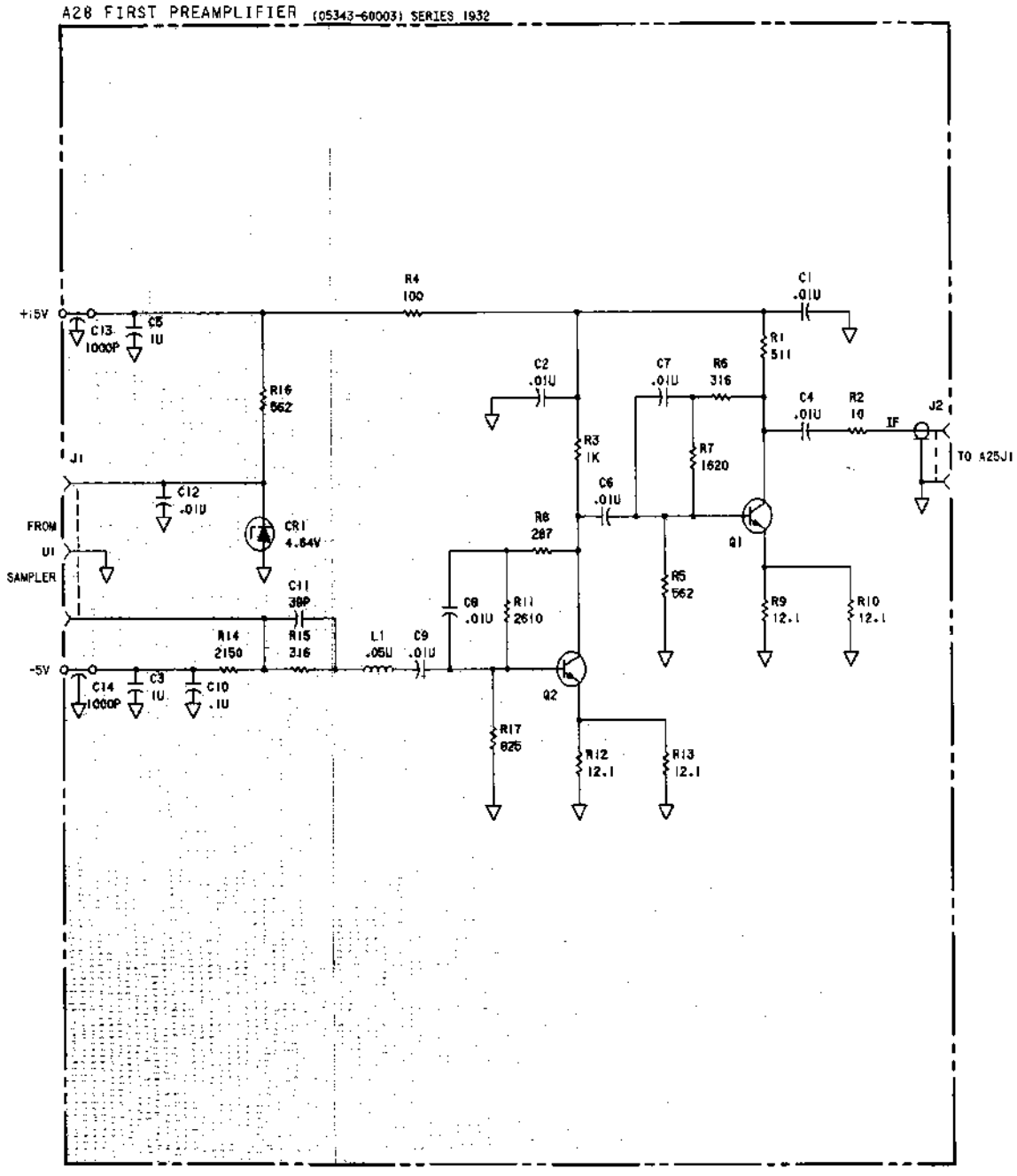


Figure 8-46. A28 First Preamplier Assembly