34 Mb/s (E3) Line Interface

For the Agilent Broadband Series Test System

E1610A

Product Features

- Cell based implementation with support for ATM, PLCP or pure-cell formats
- Operates in Terminal, Repeater, or Local Loop back modes
- Provides physical layer measurements, as well as error and alarm generation
- Internal traffic generator has 1 foreground channel and up to 100 background channels
- Works with Cell Protocol Processor

The Agilent Technologies E1610A 34 Mb/s (E3) Line Interface generates and analyses ATM cell streams contained within a E3 framing format. It is a single-slot module that provides test capability at the physical and ATM cell layers for the Agilent E4200/E4210 Broadband Series Test System.

The E1610A is capable of the following mappings:

- G.832 framing as defined in ITU-T COM 13-5-E, Rec. G.832
- G.751 PLCP framing as defined in ETS 300-337 and ETS 200-214
- G.751 ATM Transmission Convergence framing as defined in ETS 300-337 and ITU-T recommendation I.432
- Pure-cell with no framing as per ITU-T recommendation I.432

Line interface modules not only connect the device or system under test to your Broadband Series Test System, but also provide physical, convergence, and ATM cell testing capabilities.

Transmission test functionality includes:

- Traffic generation
- Cell error, loss & delay measurements
- Traffic capture & playback

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Typical Applications

The Broadband Series Test System (BSTS) is a modular test platform for high-speed ATM transmission and protocol testing. The BSTS can perform comprehensive testing of all layers, from physical through higher services. Due to its modular nature, you can create a customized configuration that suits your specific test needs. The fully-programmable BSTS is ideal for R&D engineering, product development, quality assurance, performance, type approval, and conformance testing.

The E1610A 34 Mb/s (E3) Line Interface can be used in conjunction with other BSTS line interfaces, dedicated test modules, and test software to perform these tests.

Key Features

Generate Normal or Abnormal Test Traffic

Create and detect erroneous test traffic on demand to test the robustness of a protocol implementation. Sophisticated protocol data unit builder, sequencing, and library functions let you easily create complex and realistic traffic. You can generate test traffic in the foreground channel, and use up to 100 background channels to simulate loading effects.

Cell Error, Loss & Delay Measurements

Bit rate error testing is done by placing PRBS patterns in cells, and looping these cells back through a system under test. The received cells are analyzed to detect PRBS errors. These errors can then be used as a trigger to capture data. Cell delay, interarrival time, and loss measurements are easily accomplished with the BSTS. Timestamps are inserted in cells transmitted by the line interface. These cells can then be captured, and graphs for both cell delay and cell interarrival time displayed.

Sequence numbers are transmitted in ATM cells and looped back through a system under test. The lost cells can then be detected and counted with statistics or used as a trigger to capture data.

You can generate physical and convergence layer errors and alarms. You can also capture and playback convergence layer frames.

Real-time statistics can be gathered for the physical, convergence and cell layers. Statistics can be reported as errored seconds, event counts, or as error ratios.

Traffic Capture & Playback

Traffic can be captured with a large 8 MB capture memory. Complete control is available – continuously capture with memory buffer lapping, or trigger on user-defined events. Captured traffic can be played back with automatic decoding into an English-language display. Terminology from standards documents is used wherever possible.

Since high-speed networks carry considerable volumes of traffic, you can increase your test productivity by using filters and triggers to display or capture only traffic of interest. Filters let you select virtual channels or paths of interest.

Triggers can be used to capture data matching a specific pattern. For example, triggers can be used to capture cells with header errors or sequence number errors, or upon changes in convergence layer frame bytes.

Product Numbers

- **E1610A** 34 Mb/s (E3) Line Interface
- **E4200A/B** BSTS Form-7 Transportable Chassis
- **E4210A/B** BSTS Form-13 Mainframe Chassis
- **E4209A/B** Cell Protocol Processor

Configuration & Use With Other BSTS Line Interfaces, Hardware Modules & Test Software

Line interface modules can perform physical layer testing with a minimal BSTS configuration consisting of a line interface moduleand chassis. A complete range of test software applications and dedicated test modules is available to perform upper layer testing.

The E4209 Cell Protocol Processor provides monitoring andsimulation test functions at the ATM and adaptation layers byexecuting optional protocol testing software applications. The CPP performs many functions in hardware that are usually done insoftware – such as an automatic segmentation and reassembly enginefor sophisticated real-time ATM, AAL and other higher layerprotocol testing.

Warranty & Support Options

All BSTS hardware components are warranted for a period of 3 years. Products must be returned to an authorized Agilent service center for service. At the time of purchase you may select warranty option W01, a no-charge option which converts the standard 3-year return to Agilent warranty to a 1-year on-site warranty.

Support option UK6,available at time of purchase, is a standards-compliant calibration which ensures that your BSTS test system operates within specified tolerances. A certificate of calibration is issued for compliance with ISO 9000 standards which require that records documenting the calibration of measuring and test equipment are maintained. Certificates of calibration are not available for products which donot contain components requiring calibration (such as software).

Two other types of calibration, commercial and standards-complaint,are available at any time from your local Agilent service center. Bothprovide test data and a certificate for your records.With a commercial calibration, any problems are resolved as they are detected, and test data reflecting performance of your calibrated test system is provided. The standards-compliant calibration provides comprehensive before and after test data to document problem resolution.

If you should have an out-of-warranty test system, you can arrange for service simply by contacting your local Agilent sales office.

Technical Specifications

Traffic Generation

Modes

Three Tx/Rx modes are available. In Terminal mode, full signal generation and analysis functions are available. In Repeater mode, the received signal is re-transmitted (physical layer loopback). In Local Loopback mode, the transmit signal is electrically looped to the receiver..

Total Bandwidth	• G.832: 33.920 Mb/s • G.751-PLCP: 30.528 Mb/s • G.751-ATM TC: 34.010 Mb/s • Pure-cell: 34.368 Mb/s
Modes	• User-Network Interface (UNI) or Network-Node Interface (NNI)
HEC	• Automatic generation
Fill Cells	• Idle or unassigned
Channel Priority Order	• Foreground, background, CPP (highest to lowest priority)
Channel Control	• VCI • VPI • GFC • Payload Type • Cell Loss Priority
SAR-PDU Support	• AAL-0 • AAL-1

Foreground Channel

Bandwidth	• G.832: 100 b/s to 33.920 Mb/s • G.751-PLCP: 100 b/s to 30.528 Mb/s • G.751-ATM TC: 100 b/s to 34.010 Mb/s • Pure-cell: 100 b/s to 34.368 Mb/s
Accuracy	• +/- 0.02 ppm
Distribution	• Off • Single burst • Periodic (according to the specified bandwidth)
Channel Depth	• 1500 cells (variable)
Cell Payload	• Timestamp • Single cell PRBS • Cross cell PRBS • Data pattern • Byte access

Background Channel

Number of channels	• Up to 100
Bandwidth	• G.832: 3 kb/s to 33.920 Mb/s • G.751-PLCP: 3 kb/s to 30.528 Mb/s • G.751-ATM TC: 3 kb/s to 34.010 Mb/s • Pure-cell: 3 kb/s to 34.368 Mb/s
Accuracy	• +/- 10 ppm
Distribution	• Off • Periodic
Channel density	• Bandwidth and cell distribution for each background channel is individually assignable up to maximum bandwidth
Channel Depth	• 16 cells
Cell Payload	• Single cell PRBS • Data pattern • Byte access

Cell Payloads

Payloads	• Timestamp (32-bit departure timestamp value with 100 nanosecond resolution) • Cross cell PRBS-9 • PRBS-15 (inverted and not inverted) • PRBS-23 • Single cell PRBS-9 • Data pattern or byte access
Data Patterns	• User byte • AA55h or FF00h • Incrementing (value of each successive byte is incremented by 1)
Byte Access	• Payload of all cells in the selected channel can be edited by the user in an active channel environment, or off-line as a sequence of PDUs • AAL-1 automatically inserts first payload byte containing SN/SNP values and CSI bit

Erroring Control

Error conditions can be introduced to simulate alarm signals and signal stressing. Error stressing is used to generate incorrect bytes in a test signal.

Erroring Stressing Control	• Off • On • Pulse On (error condition is normally off; pulses on) • Pulse off (normally on; pulses off) • Sequence On (normally off; alternates on/off/on) • Sequence Off (normally on; alternates off/on/off)

ATM Error Injection	• Cell header or payload bytes with bit error masking
Cell Loss	• Sequence Number in the SAR-PDU is skipped and a fill cell is inserted
PRBS Error Add	• Single bit error add to the PRBS pattern in the cell payload

G.832, G.751 & PLCP Stressing.

G.832 Alarm Generation	• Line AIS • Path FERF
G.832 Error Injection	• BIP error add • FEBE generation • CRC-7 error add • Trail trace access • Payload type (ATM, equipped, SDH TU-12s, unequipped)
G.832 Overhead Stressing	• Normal and alternative values can be defined for overheads • Pulse or sequenec controls over normal and alternative overheads
G.751 Alarm Generation	• Line AIS • Remote Alarm • National Bit
G.751 Error Injection	• Frame alignement errors using a 10-bit mask with pulse and sequence control
PLCP Alarm Generation	• Jam signal • Yellow
PLCP Error Injection	• BIP error add • FEBE generation • C1 error mask • Link statas signal set to: connected, Rx link up, or Rx link down
PLCP Overhead Stressing	• Normal and alternative values can be defined for overheads • Pulse or sequenec controls over normal and alternative overheads

ATM, PLCP, G.832 & G.751 Measurements

Measurements are sampled every 100 milliseconds and accumulated over the user-specified measurement period. Results from the most recent complete measurement period are retained..

Measurement Period	• Range 1 second to 3 days in resolutions of 1 second
Result Types	• Cumulative or latched (based on most recent measurement period)
Result Formats	• Count • Ratio • Seconds
ATM Cell Measurements	• HEC errors • Corrected headers • Cell count • Cell bandwidth • Select Cell Not Received (SCNR) alarm seconds
Cell Delay Measurements	• Cell delay • Inter-arrival time • Cell delay variation
Virtual Channel Errors	• AAL-1 SN/SNP errors • Cell loss • PRBS errors • PRBS sync loss alarm seconds
G.832 Measurements	• BIP-8 errors • CRC-7 errors • FEBE errors • Loss of signal alarm seconds • Out-of-frame alarm seconds • Loss of frame alarm seconds • Line AIS alarm seconds • FERF alarm seconds • Frame count • Coding violations • Trail traces
G.751 Measurements	• Loss of frame alarm seconds • Loss of signal alarm seconds • Line AIS alarm seconds • RAI alarm seconds • Coding violations
PLCP Measurements	• BIP errors • FEBE errors • Trailer mismatch errors • C1 code errors • C1 corrected code errors • Out-of-frame alarm seconds • Yellow alarm seconds • Jam alarm seconds • Frame count
Pure-cell Measurements	• Loss of signal alarm seconds • Scrambler sync alarm seconds • Coding violations

Traffic Capture & Playback

Provides capture of 1500 cells from the selected ATM cell stream. Capture is manual or event triggered. Manual triggering captures 1500 cells after the trigger. Event triggering captures 750 cells pre-trigger, and 750 cells post-triggers.

Manual	• Triggered on user request
ATM Cell Triggers	• Cell loss • Header error • PRBS error • SN/SNP byte error

G.832 Capture

Provides capture of 256 G.832 frames (overhead and ATM cell payload). Capture is manual or event triggered. Manual triggering captures 256 frames after the trigger. Event triggering captures 128 frames before and 128 frames after trigger.l

Manual	• Triggered on user request
On Change	• Triggered when change detected in value of selected overhead byte. Selected bits of trigger byte can be disabled using an 8-bit mask.
On Value	• Triggered when user defined value is detected in selected overhead byte. Selected bits of the user-defined value can be disabled using an 8-bit mask.
On Event	• Triggered when defined G.832 event occurs (OOF, Frameword Error, BIP Error, FEBE Error, FERF, Trail Trace Error, Trail Trace Change)

G.751 Capture

Provides capture of 256 G.751 frames (overhead and ATM cell payload). Capture is manual or event triggered. Manual triggering captures 256 frames after the trigger. Event triggering captures 128 frames before and 128 frames after trigger.l

Manual	• Triggered on user request
On Change	• Triggered when change detected in any bit of the 16 bit overhead or the Frame Alignment Signal, or a change in the RAI or National Bit is detected.

PLCP Capture

Provides capture of 256 PLCP frames (overhead and ATM cell payload). Capture is manual or event triggered. Manual triggering captures 256 frames after the trigger. Event triggering captures 128 frames before and 128 frames after trigger.l

Manual	• Triggered on user request
On Change	• Triggered when change detected in value of selected overhead byte. Selected bits of trigger byte can be disabled using an 8-bit mask.
On Value	• Triggered when user defined value is detected in selected overhead byte. Any PLCP overhead byte can be selected as trigger byte.
On Event	• Triggered when defined PLCP event occurs (Frameword Error, BIP-8 Error, FEBE, C1 Code Error, C1 Corrected Code Error, Trailer Mismatch).

Front Panel Connectors & Indicators

E3 Input	• BNC connector • 75 ohm impedance • 34.368 Mb/s • HDB3 code
E3 Output	• BNC connector • 75 ohm impedance • 34.368 Mb/s • HDB3 code • 1.0 V output level • Internal (stratum 3), External, and Recovered clock modes
External Clock Input	• BNC connector • TTL input • 50 ohm impedance • DC coupled
Trigger Output	• BNC connector • TTL output (typically > 1V into 50 ohm) • 50 ohm impedance
LED Indicators	• Failed • Error • Access • Gating • Signal • OOF • AIS • FERF • BIP • LOCS • SCNR • Reference Clock

Size, Weight & Power Dissipation

Size	• 1 slot C-size VXI card
Weight	• 1.3 kg (2.9 lb) nominal
Power Dissipation	• 25 Watts (max)

Applicable Standards

ATM Cells	• ITU-T Recommendation I.361 1995 B-ISDN ATM layer specification • Telcordia TA-NWT-001113 1993 Asynchronous Transfer Mode and ATM Adaptation Layer (AAL) Protocols Generic Requirements
G.832 Frames	• ITU-T COM 13-5-E, Rec. G.832 1995 Transport of SDH elements on PDH networks: Frame and multiplexing structures • ITU-T COM 13-5-E, Rec. G.804 1993 ATM cell mapping into plesiochronous digital hierarchy
G.751 Frames	• ETS 300-337 1995 Transmission and Multiplexing (TM) • ETS 300-214 1992 Network Aspects (NA) • ITU-T Rec. I.432 1993 B-ISDN user-network interface - Physical layer specification
Pure-Cell	• ITU-T Rec. I.432 1993 B-ISDN user-network interface - Physical layer specification
PLCP Frames	• ETS 300-214 1992 Network Aspects (NA)
Input & Output Signal	• ITU-T G703 1991 Physical/Electrical Characteristics of Hierarchical Digital Interfaces
PRBS Patterns	• PRBS-9 as per ITU-T O.153 1992 • PRBS-23 as per ITU-T O.151 1992
EMC	• Meets FTZ 1046/1984 (CISPR11, EN 55011)

Agilent Technologies Broadband Series Test System

The Agilent Technologies BSTS is the industry-standard ATM/BISDN test system for R&D engineering, product development, field trials and QA testing. The latest leading edge, innovative solutions help you lead the fast-packet revolution and reshape tomorrow's networks. It offers a wide range of applications:

- ATM traffic management and signalling
- Packet over SONET/SDH (POS)
- switch/router interworking and performance
- third generation wireless tesing
- complete, automated conformance testing

The BSTS is modular to grow with your testing needs. Because we build all BSTS products without shortcuts according to full specifications, you'll catch problems other test equipment may not detect.

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