Service Guide

Agilent Technologies
89410A Vector Signal Analyzer

Agilent Technologies

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Supersedes: 89410-90065

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The following safety notes are used throughout this manual. Familiarize yourself with each of the notes and it's meaning before operating this instrument.

WARNING: **Warning denotes a hazard. It calls attention to a procedure which, if not correctly performed or adhered to, could result in injury or loss of life. Do not proceed beyond a warning note until the indicated conditions are fully understood and met.**

CAUTION: Caution denotes a hazard. It calls attention to a procedure that, if not correctly performed or adhered to, could result in damage to or destruction of the instrument. Do not proceed beyond a caution sign until the indicated conditions are fully understood and met.

WARNING: **This is a Safety Class 1 Product (provided with a protective earthing ground incorporated in the power cord). The mains plug shall only be inserted in a socket outlet provided with a protected earth contact. Any interruption of the protective conductor inside or outside of the product is likely to make the product dangerous. Intentional interruption is prohibited.**

WARNING: **These servicing instructions are for use by qualified personnel only. To avoid electrical shock, do not perform any servicing unless you are qualified to do so.**

WARNING: **The power cord is connected to internal capacitors that may remain live for 5 seconds after disconnecting the plug from it's power supply.**

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This Agilent Technologies instrument product is warranted against defects in material and workmanship for a period of three years from date of shipment. During the warranty period, Agilent Technologies will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Agilent Technologies. Buyer shall prepay shipping charges to Agilent Technologies and Agilent Technologies shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to Agilent Technologies from another country.

Agilent Technologies warrants that its software and firmware designated by Agilent Technologies for use with an instrument will execute its programming instructions when properly installed on that instrument. Agilent Technologies does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error-free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

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In this manual...

Chapter 1 **Troubleshooting the Analyzer**

- Provides step-by-step instructions for isolating most failures to the faulty assembly

Chapter 2 **Adjusting the Analyzer**

- Provides step-by-step instructions for adjusting the analyzer

Chapter 3 **Replacing Assemblies**

- Provides step-by-step instructions to follow before and after replacing an assembly. This chapter also provides step-by-step instructions for disassembling the analyzer

Chapter 4 **Replaceable Parts**

- Provides ordering information and lists the replaceable parts

Chapter 5 **Circuit Descriptions**

- Provides the overall instrument description and individual assembly description

Chapter 6 **Voltages and Signals**

- Shows where the signals and voltages are used in the analyzer and describes each signal

Chapter 7 **Internal Test Descriptions**

- Describes the power-on test, calibration routine, fault log messages, and self tests

Chapter 8 **Backdating**

- Provides information necessary to modify this manual for instruments that differ from those currently being produced

Chapter 9 **Quick Reference**

- Provides all the block diagrams and the “A90/A91 Motherboard Voltages” table

Notation Conventions

Before you use this book, it is important to understand the types of keys on the front panel of the analyzer and how they are denoted in this book.

Hardkeys

- Hardkeys are front-panel buttons whose functions are always the same. Hardkeys have a label printed directly on the key. In this book, they are printed like this: [**Hardkey**].

Softkeys

- Softkeys are keys whose functions change with the analyzer's current menu selection. A softkey's function is indicated by a video label to the left of the key (at the edge of the analyzer's screen). In this book, softkeys are printed like this: [softkey].

Toggle Softkeys

- Some softkeys toggle through multiple settings for a parameter. Toggle softkeys have a word highlighted (of a different color) in their label. Repeated presses of a toggle softkey changes which word is highlighted with each press of the softkey. In this book, toggle softkey presses are shown with the requested toggle state in bold type as follows:
  "Press [key name on]" means "press the softkey [key name] until the selection on is active."

Shift Functions

- In addition to their normal labels, keys with blue lettering also have a shift function. This is similar to shift keys on a pocket calculator or the shift function on a typewriter or computer keyboard. Using a shift function is a two-step process. First, press the blue [**Shift**] key (at this point, the message "shift" appears on the display). Then press the key with the shift function you want to enable. Shift function are printed as two key presses, like this:
  [**Shift**] [**Shift Function**]

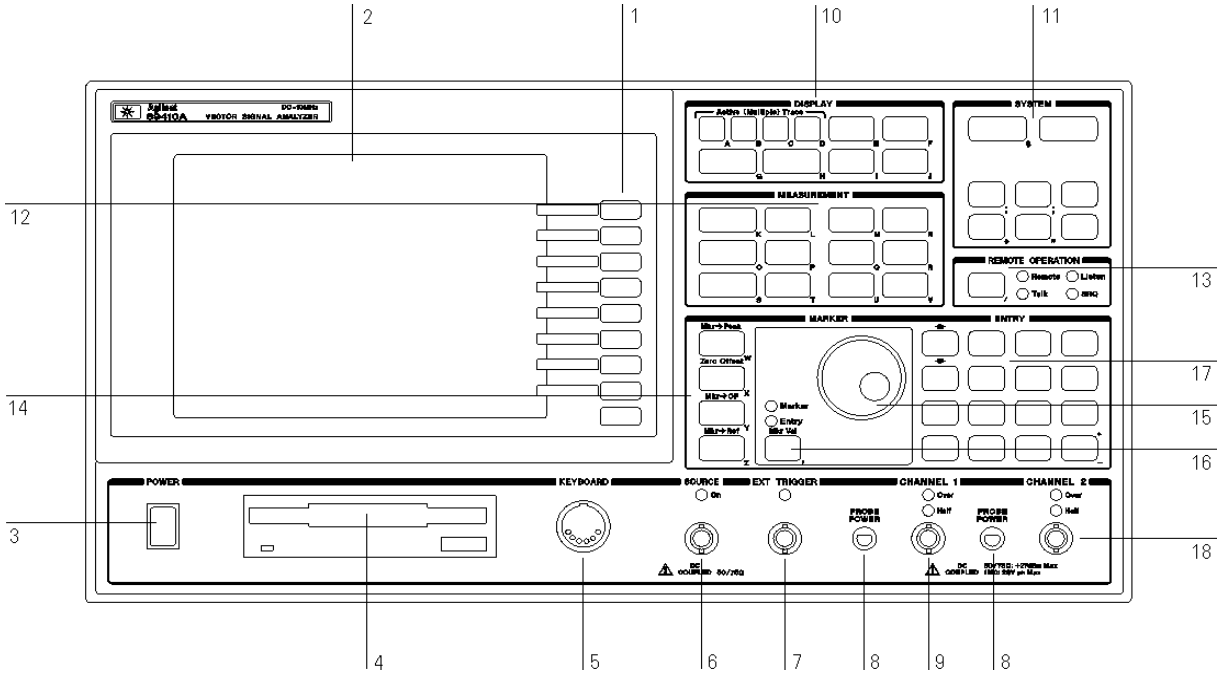
Numeric Entries

- Numeric values may be entered by using the numeric keys in the lower right hand ENTRY area of the analyzer front panel. In this book, values which are to be entered from these keys are indicted only as numerals in the text, like this:
  Press 50, [enter]

Ghosted Softkeys

- A softkey label may be shown in the menu when it is inactive. This occurs when a softkey function is not appropriate for a particular measurement or not available with the current analyzer configuration. To show that a softkey function is not available, the analyzer ''ghosts'' the inactive softkey label. A ghosted softkey appears less bright than a normal softkey. Settings/values may be changed while they are inactive. If this occurs, the new settings are effective when the configuration changes such that the softkey function becomes active.

The Agilent 89410A at a Glance



Agilent 89410A Front Panel

1-A softkey's function changes as different menus are displayed. Its current function is determined by the video label to its left, on the analyzer's screen.

2-The analyzer's screen is divided into two main areas. The menu area, a narrow column at the screen's right edge, displays softkey labels. The data area, the remaining portion of the screen, displays traces and other data.

3-The POWER switch turns the analyzer on and off.

4-Use a 3.5-inch flexible disk (DS,HD) in this disk drive to save your work.

5-The KEYBOARD connector allows you to attach an optional keyboard to the analyzer. The keyboard is most useful for writing and editing Instrument BASIC programs.

6- The SOURCE connector routes the analyzer's source output to your DUT. Output impedance is selectable: 50 ohms or 75 ohms.

7-The EXT TRIGGER connector lets you provide an external trigger for the analyzer.

8-The PROBE POWER connectors provide power for various Agilent active probes.

9-The CHANNEL 1 input connector routes your test signal or DUT output to the analyzer's receiver. Input impedance is selectable: 50 ohms, 75 ohms, or 1 megohm.

10-Use the DISPLAY hardkeys and their menus to select and manipulate trace data and to select display options for that data.

11-Use the SYSTEM hardkeys and their menus to control various system functions (online help, plotting, presetting, and so on).

12-Use the MEASUREMENT hardkeys and their menus to control the analyzer's receiver and source, and to specify other measurement parameters.

13-The REMOTE OPERATION hardkey and LED indicators allow you to set up and monitor the activity of remote devices.

14-Use the MARKER hardkeys and their menus to control marker positioning and marker functions.

15-The knob's primary purpose is to move a marker along the trace. But you can also use it to change values during numeric entry, move a cursor during text entry, or select a hypertext link in help topics.

16-Use the Marker/Entry key to determine the knob's function. With the Marker indicator illuminated, the knob moves a marker along the trace. With the Entry indicator illuminated, the knob changes numeric entry values.

17-Use the ENTRY hardkeys to change the value of numeric parameters or to enter numeric characters in text strings.

18-The optional CHANNEL 2 input connector routes your test signal or DUT output to the analyzer's receiver. Input impedance is selectable: 50 ohms, 75 ohms, or 1 megohm. For easy of upgrading, the CHANNEL 2 BNC connector is installed even if option AY7 (second input channel) is not installed.

For more details on the Agilent 89410A front panel, display the online help topic ''Front Panel.''

Before applying power

Verify that the product is set to match the available line voltage, the correct fuse is installed, and all safety precautions are taken. Note the instrument's external markings described in "Safety symbols and instrument markings" on page x.

Ground the instrument

To minimize shock hazard, the instrument chassis and cover must be connected to an electrical protective earth ground. The instrument must be connected to the ac power mains through a grounded power cable, with the ground wire firmly connected to an electrical ground (safety ground) at the power outlet. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury.

Fuses

Use only fuses with the required rated current, voltage, and specified type (normal blow, time delay). Do not use repaired fuses or short-circuited fuse holders. To do so could cause a shock or fire hazard.

Safety symbols and instrument markings

Symbols and markings in manuals and on instruments alert you to potential risks, provide information about conditions, and comply with international regulations. Table 1 defines the symbols and markings you may find in a manual or on an instrument.

Table 1 Safety symbols and instrument markings

Safety symbols	
	Warning: risk of electric shock.
	Warning: hot surface
	Caution: refer to accompanying documents.
	Laser radiation symbol: marked on products that have a laser output.
	Alternating current.
	Both direct and alternating current.
	Three-phase alternating current.
	Earth (ground) terminal
	Protective earth (ground) terminal
	Frame or chassis terminal
	Terminal is at earth potential. Used for measurement and control circuits designed to be operated with one terminal at earth potential.
	Terminal for neutral conductor on permanently installed equipment.
	Terminal for line conductor on permanently installed equipment.
	Standby (supply); units with this symbol are not completely disconnected from ac mains when this switch is off. To completely disconnect the unit from ac mains, either disconnect the power cord, or have a qualified electrician install an external switch.
Instrument markings	
	The CE mark is a registered trademark of the European Community. If it is accompanied by a year, it indicates the year the design was proven.

Table 1 Safety symbols and instrument markings (continued)

Safety symbols	
	The CSA mark is a registered trademark of the Canadian Standards Association.
	The C-tick mark is a registered trademark of the Spectrum Management Agency of Australia. This signifies compliance with the Australian EMC Framework regulations under the terms of the Radio Communications Act of 1992.
1SM 1-A	This text indicates that the instrument is an Industrial Scientific and Medical Group 1 Class A product (CISPER 11, Clause 4).

Service and Support

Any adjustment, maintenance, or repair of this product must be performed by qualified personnel. Contact your customer engineer through your local Agilent Technologies Service Center. You can find a list of local service representatives on the Web at:

http://www.agilent.com/ services/English/index.html

If you do not have access to the Internet, one of these centers can direct you to your nearest representative.

Table 2 Telephone numbers for Agilent Call Centers

United States:	Test and Measurement Call Center (800) 452 4844 (toll-free in US)
Canada:	(905) 206 4725
Europe:	(31 20) 547 9900
Japan:	Measurement Assistance Center (81) 426 56 7832 (81) 426 56 7840 (FAX)
Latin America:	(305) 267 4245 (305) 267 4288 (FAX)
Australia/ New Zealand:	1 800 629 485 (Australia) 0800 738 378 (New Zealand))
Asia-Pacific:	(852) 2599 7777 (852) 2506 9285 (FAX)

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1 Troubleshooting the Analyzer

Troubleshooting the Analyzer

This chapter contains troubleshooting tests that can isolate most failures to the faulty assembly. The section ''How to troubleshoot the analyzer'' tells you which test to start with based on the failure. The test you start with will either isolate the faulty assembly or send you to another test to continue troubleshooting.

Safety Considerations

The Agilent 89410A DC-10 MHz Vector Signal Analyzer is a Safety Class 1 instrument (provided with a protective earth terminal). Although the instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings that must be followed to ensure safe operation and retain the instrument in safe operating condition. Service must be performed by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

WARNING: Any interruption of the protective (grounding) conductor inside or outside the analyzer, or disconnection of the protective earth terminal can expose operators to potentially dangerous voltages.

An operator should not remove any covers, screws, shields or in any other way access the interior of the Agilent 89410A DC-10 MHz Vector Signal Analyzer unless instructed by an option installation note. There are no operator controls inside the analyzer.

Only fuses with the required current rating and of the specified type should be used for replacement. The use of repaired fuses or short circuiting the fuse holder is not permitted. Whenever it is likely that the protection offered by the fuse has been impaired, the analyzer must be made inoperative and secured against any unintended operation.

When power is removed from the Agilent 89410A DC-10 MHz Vector Signal Analyzer, + 11000 volts are present in the CRT for approximately 3 seconds. Be extremely careful when working in proximity to this area during this time. The high voltage can cause serious personal injury if contacted.

CAUTION: Do not connect or disconnect ribbon cables with the power switch set to on (|). Power transients caused by connecting or disconnecting a cable can damage circuit assemblies.

Equipment Required

The following table lists the recommended equipment needed to adjust and troubleshoot the analyzer. Other equipment may be substituted for the recommended model if it meets or exceeds the listed critical specifications. When substitutions are made, you may have to modify the procedures to accommodate the different operating characteristics.

Recommended Test Equipment

Instrument	Critical Specifications	Recommended Model
Frequency Standard	Accuracy ±0.5 ppm	Agilent 5061B
Frequency Synthesizer	Frequency range 3 Hz to 10 MHz Amplitude range –36 to +20 dBm Amplitude resolution 0.01 Hz Impedance 50 Ω Harmonic distortion <–30 dBc Spurious <–70 dBc External reference input	Agilent 3326A Alternate Agilent 3325A Agilent 3325B
Milliwatt Power Meter	Range ±0.2 dBm Accuracy ±0.0625 dB	W&G EPM-1 †
Spectrum Analyzer	Frequency range 100 Hz to 40 MHz Amplitude range –60 to +15 dBm Dynamic range <–67 dBc Tracking Source @ 0 dBm Impedance 50 Ω and 75 Ω External reference input	Agilent 3585B Alternate Agilent 3585A Agilent 3588A Agilent 3589A
Digital Multimeter	Accuracy 25 ppm Maximum volts range ≥400 Vdc	Agilent 3458A Alternate Agilent 3456A
Frequency Counter	Frequency range 3 to 30 MHz Resolution <1 Hz Frequency accuracy ±0.25 Hz Impedance 1 MΩ	Agilent 5334B opt 010
Network Analyzer	Range 10 kHz to 60 MHz Resolution 10 Hz Input impedance 50 Ω Amplitude range –42 dBm to +10 dBm resolution 0.25 dB dynamic accuracy 0.3 dBp-p from 10 kHz to 16 MHz	Agilent 3577B Alternate Agilent 4195A Agilent 3589A with Agilent 35689A

†Wandel & Goltermann Inc., 1800 Wyatt Drive, Suite 2, Santa Clara, CA 95054 U.S.A (408)988-7622

Recommended Test Equipment (continued)

Logic Probe	TTL/ CMOS	Agilent 545A Alternate Agilent 5006A Agilent 5005A/ B
Oscilloscope	Bandwidth ≥150 MHz Vertical sensitivity 10 mV/ div Input coupling AC, DC, 50 Ω, 1 MΩ Trigger Ext, Int	Agilent 54111D
Oscilloscope Probe	Input R ≥1 MΩ Division Ratio 1:1	Agilent 10438A
Oscilloscope Probe	Input R ≥1 MΩ Division Ratio 10:1	Agilent 10431A
50 Ω Feedthrough Termination (2 for opt AY7)	Accuracy ±0.2%	Agilent 11048C
(2) 50 Ω Termination	±2% at dc	Pomona Model 3840-50 † Alternate Agilent 11048C with Agilent 1250-0774
ThinLAN Transceiver	AUI to ThinLAN adapter	Agilent 28641B
Cables	(4) 50 Ω BNC Test clips-to-double banana plug	Agilent 8120-1840 Agilent 11002A
Adapters	BNC(f)-to-Dual Banana Plug N(m)-to-BNC(f) (2) Test Clips-to-BNC(f) BNC Tee N(f)-to-BNC(f) BNC(f)-to-Dual Banana Plug(m) BNC(f)-to-BNC(f)	Agilent 1251-2816 Agilent 1250-0780 Pomona Model 2631 † Agilent 1250-0781 Agilent 1250-1536 Agilent 1251-2277 Agilent 1250-0080
Service Kit	 Includes A10/ A35 extender board A36/ A60 extender board A61 extender board Motherboard cable extraction tool Plastic screw driver Flat-edge adjustment tool SMB extender cable (2) BNC(m)-to-SMB(f) cable (2) SMB(m)-to-SMB(m) adapter (2)	Agilent 89410-84401 Includes Agilent 89410-B1001‡ Agilent 89410-B1002‡ Agilent 89410-B1008‡ Agilent 8710-2050 Agilent 8710-2056 Agilent 8710-1928 Agilent 03585-61601 Agilent 03585-61616 Agilent 1250-0669
10 kW Series Resistor ††	Value: 10 kΩ Accuracy: 1% Power: 0.125 Ω	Agilent 0757-0442
CPU/ Memory Service Utility Disk		Agilent 89410-19463

†ITT Pomona Electronics, 1500 East Ninth Street, Pomona, CA 91769 U.S.A. (714) 469-2900 FAX (714) 629-3317

‡Individual extender boards cannot be ordered. To order all three extender boards in this kit, order Agilent 89410-66515.

††See the following for assembly.

Suggested Assembly for Series Resistor

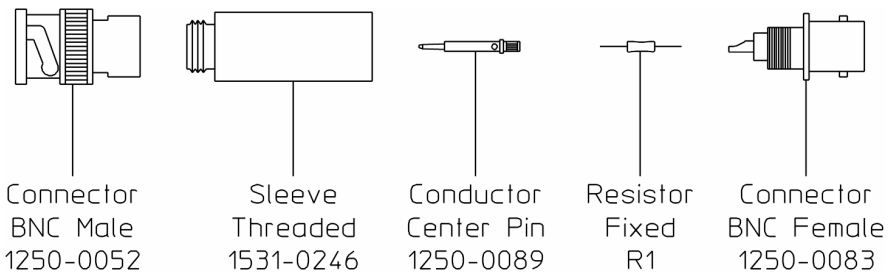
The following is a suggested assembly for the 10 kW series resistor. The 10 kΩ series resistor is required for the Input Offset adjustment.

1 Cut resistor leads to 12 mm on each end.

2 Solder one resistor lead to the center conductor of the BNC female connector.

3 Solder the conductor center pin to the other lead of the resistor.

4 Screw the sleeve and the BNC male connector into place. Tighten securely.



Troubleshooting Hints

- Check that the analyzer has the latest firmware before starting the troubleshooting procedures.
- Incorrect bias supply voltages can cause false diagnostic messages. Most troubleshooting procedures do not check the power supply voltages through the motherboard. If you suspect incorrect supply voltages to an assembly, use the ''A90/A91 Motherboard Voltages'' table on page 6-24 and an extender board to check the voltages at the assembly.
- The troubleshooting procedures do not isolate failures to cables or connectors. If you suspect a cable or connector failure, check the device for continuity.
- Cables can cause intermittent hardware failures.
- Noise or spikes in the power supply can cause the analyzer to fail.
- Measurements in this chapter are only approximate (usually ±1 dB or 10%) unless stated otherwise.
- Use chassis ground for all measurements in this chapter unless stated otherwise.

- Logic levels in this chapter are either TTL level high or TTL level low unless stated otherwise. Toggling signal levels continually change from one TTL level to the other.
- Configure a logic probe with an external bias supply for testing digital signals. This analyzer does not have easily accessible +5 V supplies.
- If you abort a self test before the self test is finished, the analyzer may fail its calibration routine. To prevent this from happening press [**Preset**] or cycle power after you abort the self test.
- The troubleshooting tests in this chapter assume only one independent failure. Multiple failures can cause false results.

How to troubleshoot the analyzer

1 Review "Safety Considerations" and "Troubleshooting Hints."

WARNING: Service must be performed by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

2 See Replacing Assemblies in chapter 3 to determine how to disassemble and assemble the analyzer.

3 Determine which test to start with by comparing the analyzer's symptoms to the symptoms in the following table.

Symptom	Troubleshooting Test
Screen blank Screen grid is distorted or not displayed After power up, >3 minutes before keys active No response when key is pressed Incorrect response when key is pressed Fatal System Error Please Cycle Power message displayed Fan not turning	Initial verification, page 1-10
Keys are active and screen grid is displayed but screen is defective	Display, page 1-25
Error messages Calibration fails Performance test fails Intermittent failure HPIB fails Serial port fails External monitor port fails Parallel port fails Sync out fails System interconnect port fails ThinLAN port fails AUI port fails Probe power fails Oven reference fails	Self tests, page 1-32
HPIB trigger fails External trigger fails	Trigger, page 1-83

External keyboard does not work	DIN connector, page 1-92
NVRAM or Battery failure message displayed Nonvolatile states not saved after power cycled	Memory battery, page 1-93

4 Follow the recommended troubleshooting test until you locate the faulty assembly.

5 Replace the faulty assembly and follow the directions in ''What to do after replacing an assembly'' in chapter 3, ''Replacing Assemblies page 3-5.''

To perform initial verification

Use this test to check signals that are vital to the operation of the analyzer.

1 Check voltage selector switch and fuse.

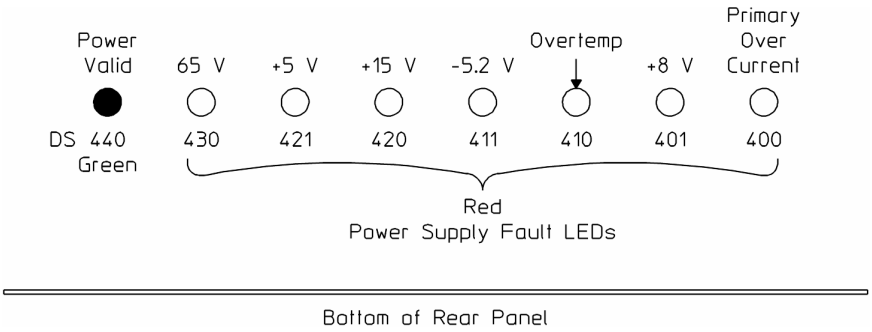
a Check that the voltage selector switch on the rear of the analyzer is set for the local line voltage.

b Check that the correct line fuse is installed in the rear panel fuse holder.
For information on the voltage selector switch and line fuse, see ''To change the line-voltage selector switch'' and ''To change the fuse'' in chapter 1 of the *Agilent 89410A Installation and Verification Guide*.

2 Check power supply LEDs and fan.

a Check that no power supply fault LEDs are lit and that DS 440 (green) is lit.

b If any fault LEDs are lit or if the green power valid LED (DS 440) is not lit, go to page 1-15, ''To troubleshoot the power supply.''



c Check that the fan is turning at a moderate speed for normal room temperature.
The fan speed increases as the analyzer's internal temperature increases. If the fan is turning too fast, check that the air flow around the analyzer is not constricted and that the ambient temperature is between 0 and 55 °C.

d If the fan is not turning, go to page 1-15, ''To troubleshoot the power supply.''
This quick check does not completely check the power supply. If a power supply failure is still suspected, go to page 1-15 ''To troubleshoot the power supply.''

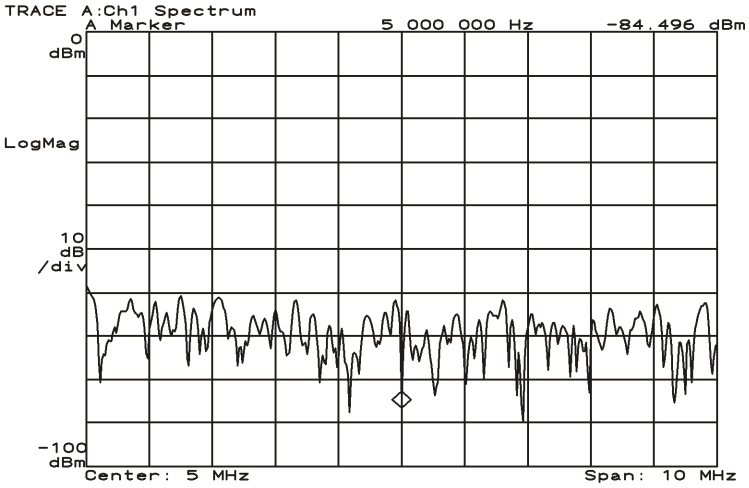
3 If the grid appears after power up, check that the calibration routine is not locking up the analyzer.

   a Set the power switch to off (O).

   b Press and hold [**Return**] (below softkeys) while setting the power switch to on (l).
   Pressing [**Return**] while setting the power switch to on (l) causes the analyzer to bypass the calibration routine.

   c If the keys are now active, go to page page 1-48, ''To troubleshoot self-test lockup failures.''

4 If the analyzer powers up normally with no error messages (see illustration below), the screen is continually updating, but the analyzer does not respond to key presses, the A80 Keyboard assembly is probably faulty.



5 Check frequency reference signals.

a Turn the analyzer upside down.

b Remove the bottom cover.

c Press [**Preset**].

d Using an oscilloscope and a 1 MΩ 10:1 probe with a grounding spanner, check the TTL signals in the following table.
The probe may load the 64 MHz, 48 MHz, and 80 MHz signals causing their amplitude level to be low.

Test Location	Ground Connection	Frequency	Probable Faulty Assembly
A91 P6 pin 16	A91 P6 pin 15	25.6 MHz	A60 Frequency Reference
A91 P6 pin 11	A91 P6 pin 12	25.6 MHz	A60 Frequency Reference
A91 P6 pin 18	A91 P6 pin 19	3.2 MHz	A60 Frequency Reference
A91 P4 pin 5	A91 P4 pin 6	378 kHz	A61 Clock
A91 P4 pin 21	A91 P4 pin 22	64 MHz	A61 Clock
A91 P4 pin 24	A91 P4 pin 23	48 MHz	A61 Clock
A91 P4 pin 25	A91 P4 pin 26	80 MHz	A61 Clock

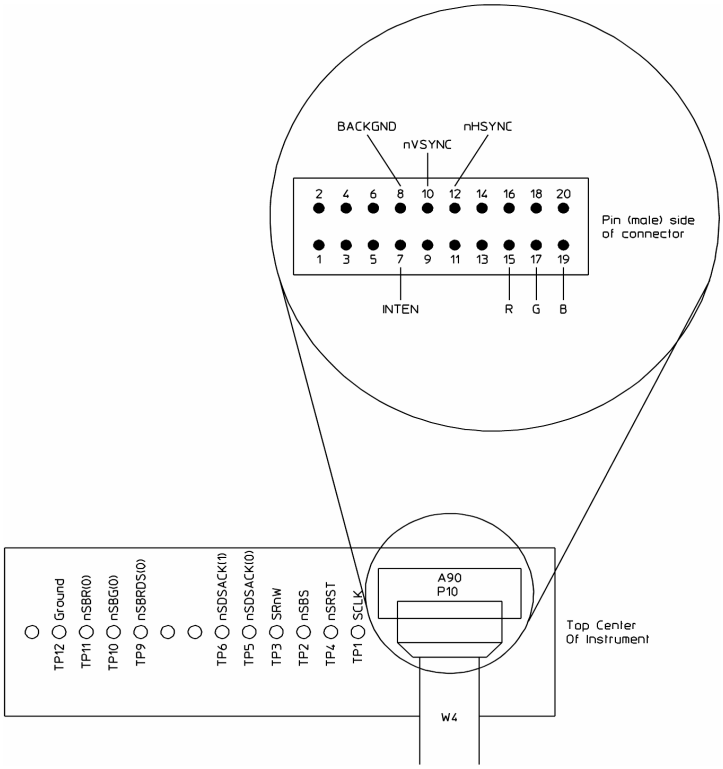
e If a signal is incorrect, replace the probable faulty assembly.
Before replacing the A60 Frequency Reference assembly, go to page 1-15, ''To troubleshoot the power supply,'' and do Step 7 to check the power supply voltages.

6 Step 6. Check signals required for power up.

a Remove the top cover.

b Connect a logic probe to A90 TP4 and its ground clip to A90 TP12.

c Set the power switch off (O) then on (I) and check that A90 TP4 is a TTL high 10 seconds after power up.



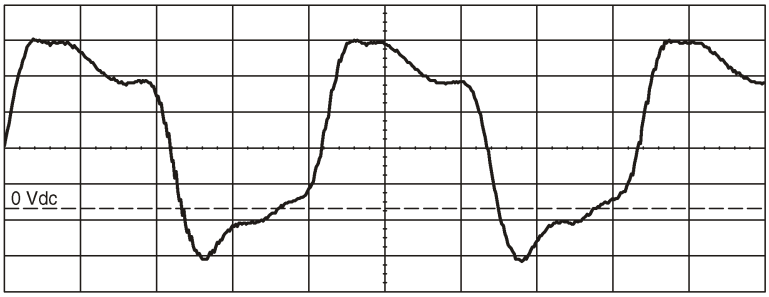
d If TP4 remains low, the A40 CPU assembly is probably faulty. Before replacing the assembly, go to page 1-15 ‘‘To troubleshoot the power supply,’’ and do Step 7 to check power supply voltages.

e Set the power switch to off (O) and disconnect the ribbon cable from A90 P10.

f Set the power switch to on (I).

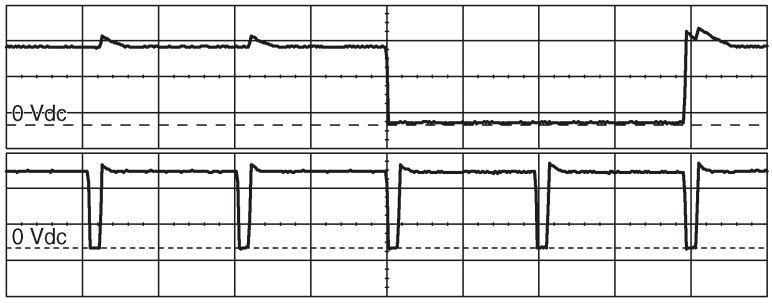
g Using an oscilloscope and 1 MΩ 10:1 probes, check the following system clock signals.

Oscilloscope Setup		Parameters	Waveform
Connect CH1 to A90 TP1		Time Duty Cycle	
CH1 V/ div	1 V/ div		
Input Impedance	1 MΩ		
CH1 Coupling	dc		
Probe Atten	10		
Display Mode	Repetitive		
Averaging	8		
Time/ div	10 ns/ div		
Trigger	Trg'd Sweep		
Trig Src	Chan1		



SCLK

Connect CH1 to A90 P10 pin 10 Connect CH2 to A90 P10 pin 12		Time Duty Cycle Time Relationship	
CH1 V/ div	2 V/ div		
Input Impedance	1 MΩ		
CH1 Coupling	dc		
Probe Atten	10		
CH2 V/ div	2 V/ div		
Input Impedance	1 MΩ		
CH2 Coupling	dc		
Probe Atten	10		
Display Mode	Repetitive		
Averaging	8		
Time/ div	20 µs/ div		
Trigger	Trg'd Sweep		
Trig Src	Chan1		



nVSYNC and nHSYNC

h If SCLK is incorrect, the A40 CPU assembly is probably faulty. Before replacing the assembly, go to page 1-15, ''To troubleshoot the power supply,'' and do Step 7 to check power supply voltages.

i If nVSYNC or nHSYNC is incorrect, the A47 DSP/Display Controller assembly is probably faulty.

j If the signals are correct, go to page 1-36 ''To troubleshoot power-up failures.''

To troubleshoot the power supply

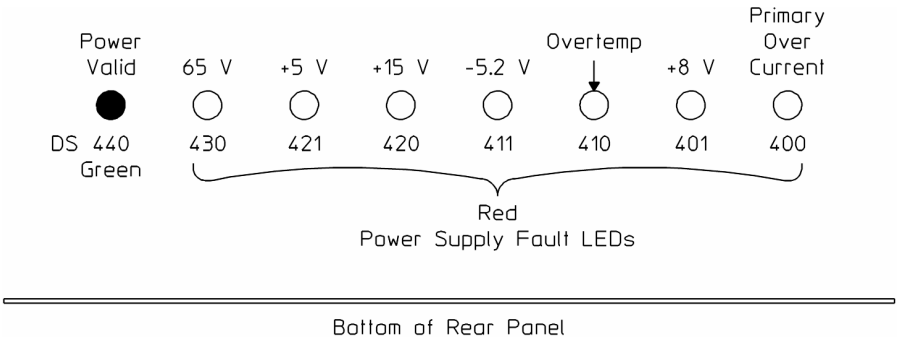
Use this test to do a complete check of the power supply and to isolate the failure between the A95 Main Power Supply assembly and A96 Primary Power Supply assembly.

WARNING: This procedure is performed with protective covers removed and power applied. Energy available at may points can, if contacted, result in personal injury.

Even with power removed, there can be sufficient stored energy in some circuits to cause personal injury. These voltages will discharge to a relatively safe level approximately five minutes after the power cord is disconnected.

---

1 Determine the next step by comparing the power supply LEDs to the following table.



Power Supply LED	Next Step
DS400 Primary Over Current is lit All LEDs are off All fault LEDs are off and DS440 is lit but a power supply problem is suspected	Step 2
DS410 Overtemp is lit DS440 Power Valid is lit but fan is not turning	Step 5
DS430, 421,420, 411, or 401 secondary supply is lit	Step 7

2 Check the A96 Primary Power Supply assembly's voltages.

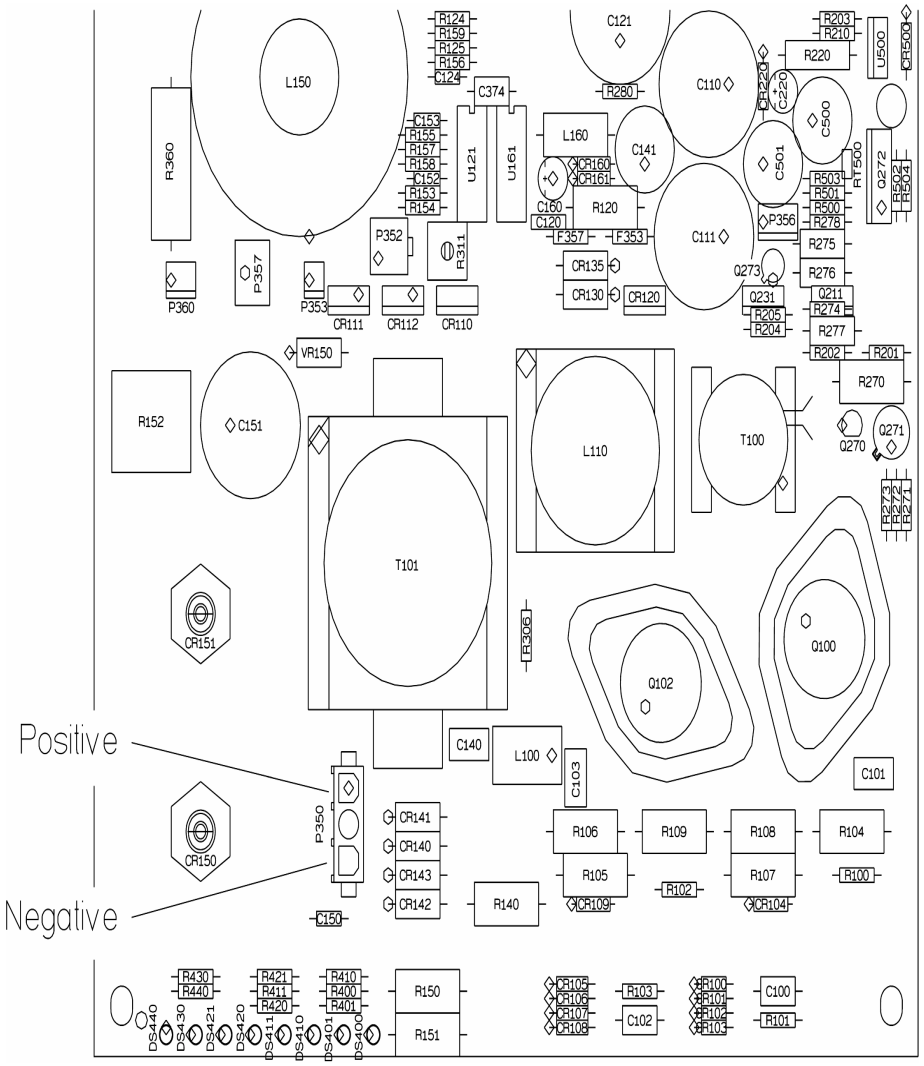
a Set the power switch to off (O) and disconnect the power cord from the rear panel.

b Remove the top cover.

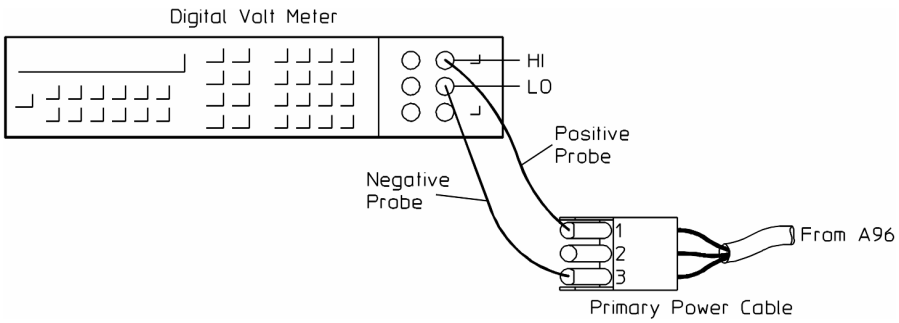
c Wait five minutes to allow time for the power supply capacitors to discharge.

d Remove the power supply shield located on top of the analyzer behind the display.

e Remove the primary power cable connected to A95 P350.



f Connect a digital voltmeter to the primary power cable as shown below.



g Connect the power cord to the rear panel.

h Calculate the differential voltage for the local line voltage using the following table.

Line Selector Switch	Differential Voltage ± 30 Vdc
115 V	Line Voltage (Vrms) x2.83
230 V	Line Voltage (Vrms) x1.414

For example, if the local line voltage is 110 Vrms, then the calculated differential voltage is 311 ±30 Vdc.

i If the measured voltage is not within ±30 Vdc of the calculated differential voltage, the A96 Primary Power Supply assembly is probably faulty.

j Disconnect the power cord from the rear panel.

k Wait five minutes to allow time for the power supply capacitors to discharge.

l Disconnect the probes from the primary power cable and reconnect the cable to A95 P350.

3 Check the A96 Primary Power Supply assembly's ac bias voltages.

a Place the analyzer on the side closest to the keypad.

b Remove the bottom cover.

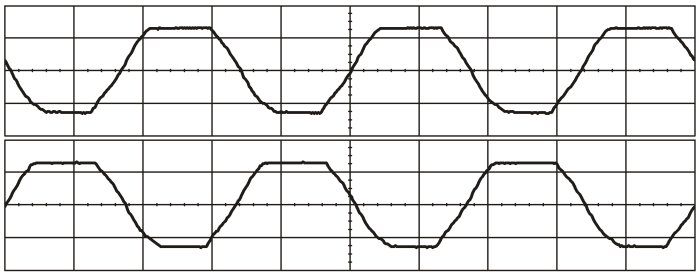
c Wait five minutes to allow time for the power supply capacitors to discharge.

d Remove the black power supply shield.

e Connect the power cord and set the power switch to on (l).

f Using an oscilloscope and two 1 MΩ 10:1 probes, check the following ac bias supplies. See page 1-19 for component location.

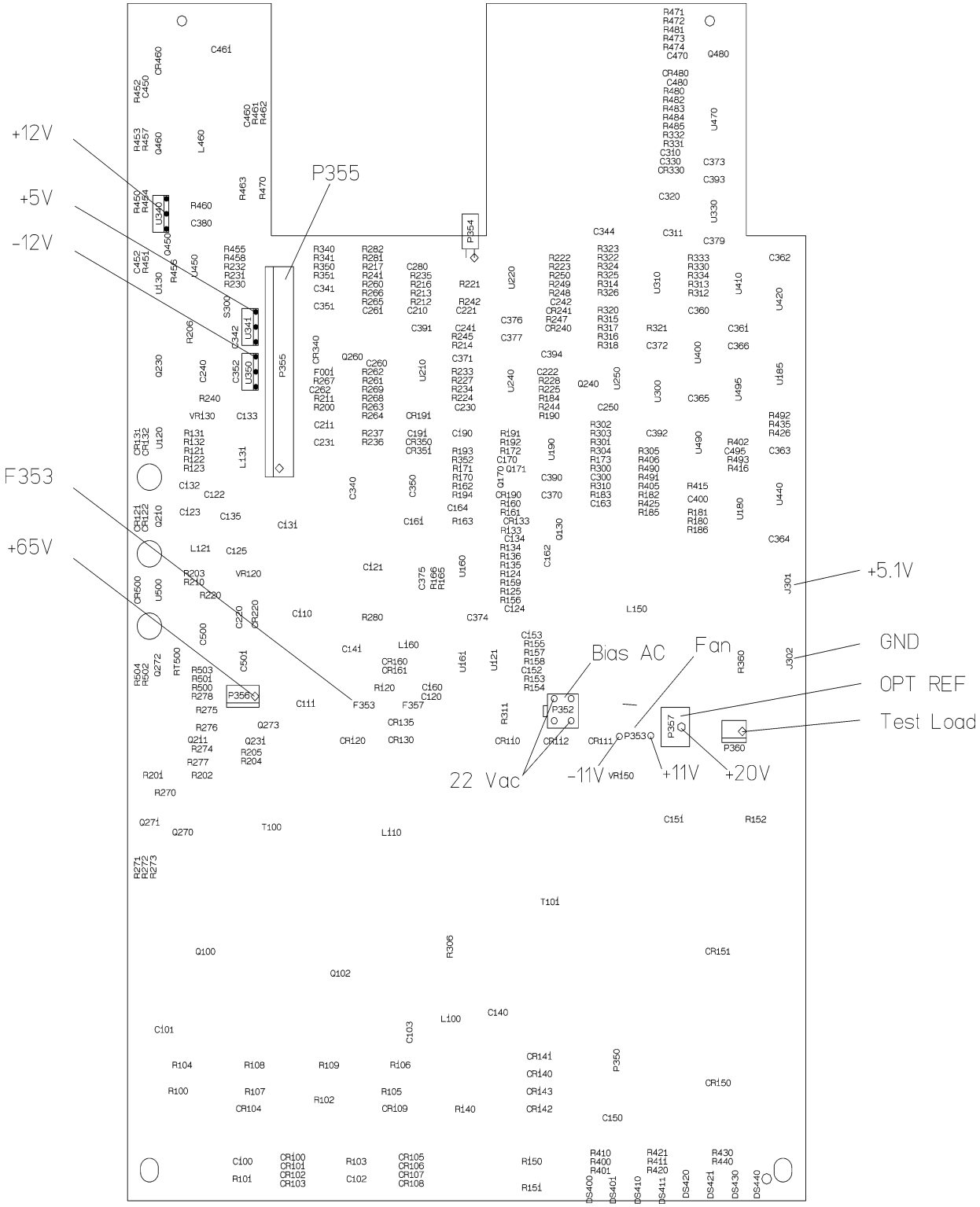
Oscilloscope Setup		Parameters	Waveform
Connect CH1 to A95 P352, pin 1		Pulse Shape	
Connect CH2 to A95 P352, pin 4		Time Relationship	
CH1 V/ div	20 V/ div		
Input Impedance	1 MΩ		
CH1 Coupling	dc		
Probe Atten	10		
CH2 V/ div	20 V/ div		
Input Impedance	1 MΩ		
CH2 Coupling	dc		
Probe Atten	10		
Display Mode	Repetitive		
Averaging	8		
Time/ div	5 ms/ div		
Trigger	Trg'd		
Trigger Level	Sweep		
Trig Src	–1.8 V		
	Chan1		



AC BIAS

g If the waveforms are incorrect, the A96 Primary Power Supply assembly is probably faulty.

A95 Component Locator, Bottom View



4 Check the A95 Main Power Supply assembly's bias supply voltages.

a Check the bias supply voltages in the following table.
The ripple should be no more than 50 mVp-p. Do not include high frequency line noise when measuring ripple.

Test Location	Nominal Voltage	Minimum Voltage	Maximum Voltage	Ripple Tolerance
U341, pin 3	+5 V	+4.5 V	+5.5 V	50 mVp-p
U340, pin 2	+12 V	+11.4 V	+12.6 V	50 mVp-p
U350, pin 3	–12 V	–12.6 V	–11.4 V	50 mVp-p

b If any of the voltages are incorrect, the A95 Main Power Supply is probably faulty.
The A95 Main Power Supply assembly has no adjustments. Therefore if a voltage is incorrect, replace the assembly.

c If the voltages are correct and the fan is turning, go to Step 7.

5 Check the supply voltage fuse for the A102 Fan assembly.

a Set the power switch to off (O).

b Wait five minutes to allow time for the power supply capacitors to discharge.

c Measure the resistance across A95 F353.

d If the resistance is greater than 0Ω, replace the fuse.

6 Check A102 Fan assembly.

a Set the power switch to off (O) and disconnect the power cord from the rear panel.

b Remove the top cover.

c Wait five minutes to allow time for the power supply capacitors to discharge.

d Remove the power supply shield located on top of the analyzer behind the display.

e Disconnect the fan power cable from A95 P353 (red and black cable).

f Connect 10 Vdc to the fan cable. The fan should be turning slowly.

g Increase the voltage to 24 Vdc. The fan should turn faster as the voltage increases.
The power to the A102 Fan assembly is controlled by a thermistor which varies the fan voltage between +8 V when the analyzer is cold and +28 V when the analyzer is hot. The thermistor is on the A95 Main Power Supply assembly.

h If the fan did not respond correctly, the Fan assembly is probably faulty.

7 Check A95 Main Power Supply assembly voltages.

a Set the power switch to off (O) and disconnect the power cord from the rear panel.

b Place the analyzer on the side closest to the keypad.

c Remove the bottom cover.

d Wait five minutes to allow time for the power supply capacitors to discharge.

e Remove the black power supply shield.

f Connect the power cord and set the power switch to on (l).

g Check the voltages in following table.
The ripple should be no more than 50 mVp-p. Do not include high frequency line noise when measuring ripple. See page 1-19 for test locations.

Test Location	Nominal Voltage ±10%	Minimum Voltage	Maximum Voltage
P353, pin 1	+11 V	+8 V	+28 V
P353, pin 2	–11 V	–11.6 V	–10.5 V
P357, pin 2	+20 V	+17.0 V	+23.0 V
J301	+5.1 V	+4.8 V	+5.2 V
P356, pin 1	+65 V	+64.7 V	+65.3 V
P355, pin 1	+8 V	+7.8 V	+8.2 V
P355, pin 3	–8 V	–8.2 V	–7.8 V
P355, pin 5	+15 V	+14.6 V	+15.5 V
P355, pin 7	–15 V	–15.5 V	–14.6 V
P355, pin 14	–5.2 V	–5.4 V	–5.0 V

If the above voltages are correct, the fan is turning, and the power supply fault LEDs are off, the power supply is operating correctly.

8 Check for power supply loading.

a Set the power switch to off (O) and disconnect the power cord from the rear panel.

b Place the analyzer on the side closest to the display.

c Wait five minutes to allow time for the power supply capacitors to discharge.

d Disconnect the +5V (red) and GND (black) cables from J301 and J302.

e Remove the screws and standoffs holding the A95 Main Power Supply assembly in the chassis. See ''To remove main power supply'' on page 3-16

f Disconnect the motherboard cable from A95 P355, the display power cable from A95 P356, and the optional oven cable from A95 P357.

g Connect A95 J302 to the chassis.

h Connect A95 P360 pins 2 and 3 together. This provides a test load for the power supply.

i Place the A95 Main Power Supply assembly on its side.
The assembly should not be touching the analyzer and it should still be connected to the A96 Primary Power Supply.

j Connect the power cord and set the power switch to on (l).

k Check the voltages in the table on page 1-21.

l If the voltages are still incorrect, the A95 Main Power Supply assembly is probably faulty.
The voltages may vary slightly from the power supply nominal values due to the change in load.

9 Isolate assembly loading power supply.

a Set the power switch to off (O) and disconnect the power cord from the rear panel.

b Wait five minutes to allow time for the power supply capacitors to discharge.

c Disconnect A95 P360 pins 2 and 3.

d Reconnect all the cables to the A95 Main Power Supply assembly.

e Reinstall the A95 Main Power Supply assembly in the analyzer.

f Replace the black power supply shield and bottom cover.

g Repeat the following steps for each assembly suspected of loading the power supply.
Use the Power Supply Voltage Distribution table on page 6- and the A90/A91 Motherboard Voltages table on page 6- to help isolate the failing assembly.

h Set the power switch to off (O).

i Remove the suspected assembly or the power cable to the assembly.

j Set the power switch to on (l).

k Check the voltages in the table on page 1-21.

To troubleshoot display failures

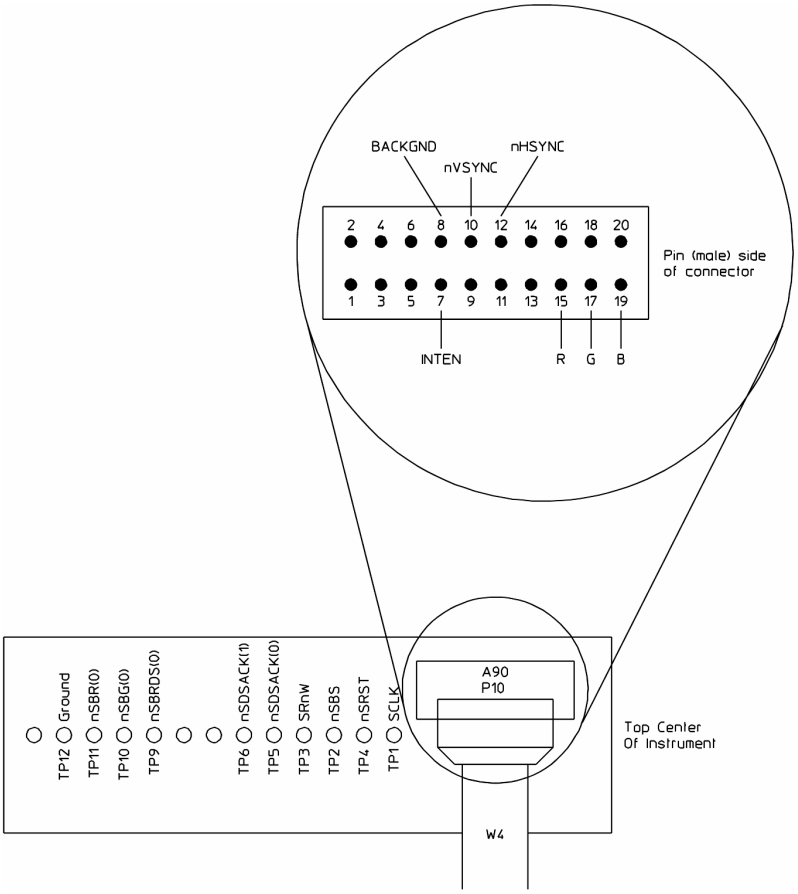
Use this test to separate A100 Display assembly failures from A47 DSP/Display Controller assembly failures. If the screen is blank or the grid is not displayed, do initial verification on page 1-10 to determine if the A40 CPU assembly is faulty.

1 Check the display controller signals.

a Set the power switch to off (O).

b Remove the top cover.

c Disconnect the ribbon cable from A90 P10.



d Set the power switch to on (l).

e Check the following display signals using a voltmeter.

Test Location	Signal Name	Amplitude (±10%)
A90 P10 pin 7	490 mVdc	INTEN
A90 P10 pin 15	R	25 to 45 mVdc
A90 P10 pin 17	G	25 to 45 mVdc
A90 P10 pin 19	B	25 to 45 mVdc

f If any of the signals are incorrect, the A47 DSP/Display Controller assembly is probably faulty.

2 Determine the probable faulty assembly by comparing the analyzer's symptoms to the following table.

Symptom	Probable Faulty Assembly
Vertical and horizontal scanning is occurring. Part of information is missing, for example only half letters. Blocks of information are missing. Information on the screen is scrambled or mixed up. Vertical or horizontal stripes appear across the screen.	A47 DSP/ Display Controller
Screen is blank. Screen is tilted, compressed, or distorted. Line across the screen.	A100 Display †

† Before replacing the A100 Display assembly, go to page 1-15 "To troubleshoot the power supply," and do Step 7 to check the +65 V power supply voltage.

3 Check the +65 Vdc power supply.

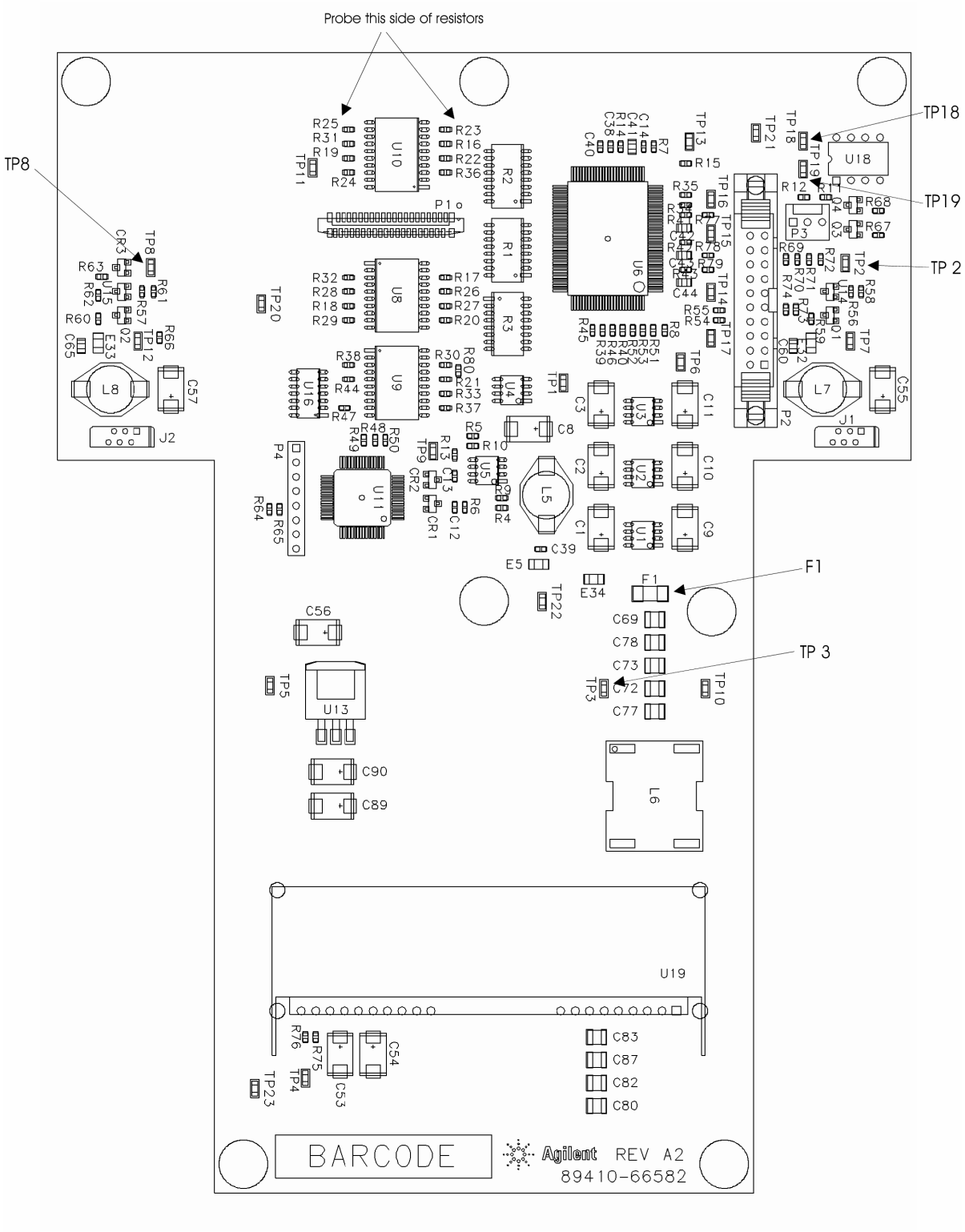
a Set the power switch to off (O).

b Place the front panel in the A82 test position. (see Chapter 3, “To place the A82 in the test position”, on page 3-12.)

c Set the power switch to on (l).

d Check for +65 Vdc ± 10% at TP3 using a Voltmeter.

e If the voltage is correct, continue with step 4.



f Check for +65 Vdc on both sides of F1.

g If the voltage is correct on one side of F1 and incorrect on the other replace F1.

h If the voltage is incorrect on both sides of F1, then the A95 Main Power Supply is probably faulty.

4 Check the programming signals from A81 to A82.

a Using a logic probe verify that TTL logic pulses are present at TP 18 and TP19 within 30 seconds of power up. These test points will remain high after programming is complete.

b If the signals are incorrect at TP18 or TP19 the A81 Keyboard Assembly is probably faulty.

5 Check the digital output signals to the LCD display.

a Using a logic probe verify that TTL logic pulses are present at the following locations:

Signal Line	Probe Location
B0	R31
B1	R19
B2	R24
B3	R23
B4	R16
B5	R22
G0	R32
G1	R20
G2	R27
G3	R26
G4	R17
G5	R25
R0	R33
R1	R21
R2	R30
R3	R29
R4	R18
R5	R28
DENA	R36
VSYNC	R38
HSYNC	R37
CLK	R44

b If any of the signals are incorrect, the A82 LCD Interface assembly is probably faulty

c Verify the back lights and inverter boards. When the display is in the test position the back lights are visible from the side of the display. Use this procedure if one or both are not lit.

a Press Display, more display setup, color setup, brightness, 100%. The brightness level controls the voltage applied to the back lights.

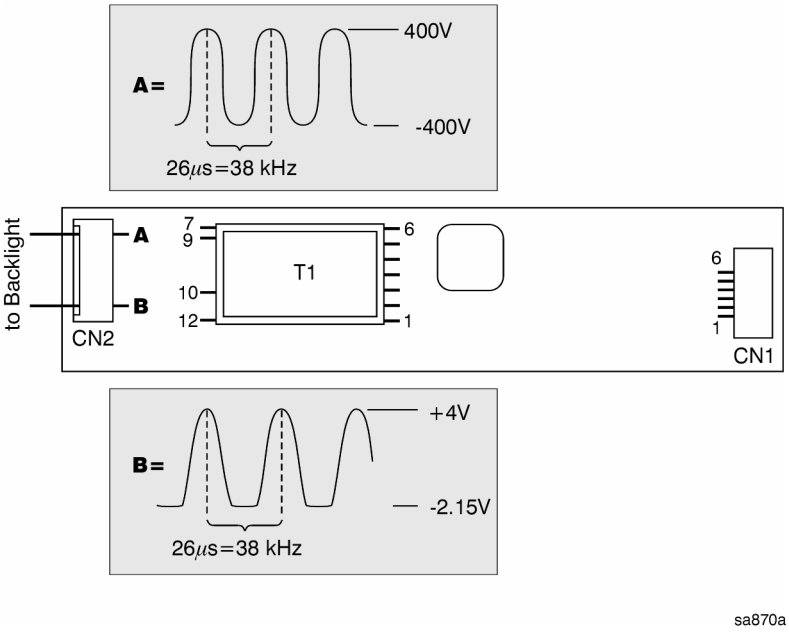
b Check for +4.5 Vdc ± 0.2 V at A82 TP2 using a voltmeter.

c If this voltage is incorrect then the A47 assembly is probably faulty.

d Check for +1.2 Vdc ± 0.2 V at A82 TP8 using a voltmeter.

e If this voltage is incorrect then the A82 assembly is probably faulty.

f Check the input and output signals of the inverter board as listed below.



Test Point	Signal or Voltage
CN 1 pin 1	+ 4.9 Vdc
CN 1 pin 2	+ 4.9 Vdc
CN 1 pin 6	+ 1.2 Vdc
CN 2 A	– 400 V to + 400 V sinewave @ 38kHz (see figure)
CN 2 B	– 2.15 V to + 4 V sinewave @ 38 kHz (see figure)

g If the inputs to the inverter are incorrect the cable is probably faulty.

h If the outputs of the inverter are incorrect then the inverter is probably faulty.

i If the outputs of the inverter are correct then the back light is probably faulty.

To perform self tests

Use this test when the keyboard is active and one of the following occurs:

- An error message is displayed
- Calibration fails
- Performance test fails
- Failure is intermittent
- Interface port fails
- Probe power fails
- Sync out fails

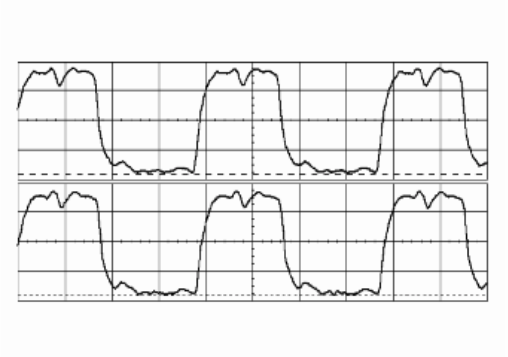
1 Check sample clocks.

a Remove the top cover.

b Set the power switch to on (l).

c Using an oscilloscope and 2 BNC(m)-to-SMB(f) cables, check the following signals.

Oscilloscope Setup		Parameters	Waveform
Connect CH1 to A60 J3 Connect CH2 to A60 J2		Time Duty Cycle Time Relationship	
CH1 V/ div Input Impedance CH1 Coupling Probe Atten	1 V/ div 50 Ω dc 1		
CH2 V/ div Input Impedance CH2 Coupling Probe Atten	1 V/ div 50 Ω dc 1		
Display Mode Averaging Time/ div Trigger Trig Src	Repetitive 8 10 ns/ div Trg'd Sweep Chan1		



Sample Clock

d If either signal is incorrect, the A60 Frequency Reference assembly is probably faulty.

e Reconnect the cables to A60 J3 and A60 J2.

2 Check for failing power-up results.

a Press the following keys:
[**System Utility**]
[auto cal **off**]
[more cal setup]
[auto zero cal **off**]
[**Return**]
[more]
[diagnostics]
[service functions]
1125
[enter]
[test log]

During the additional hardware power-up test, the A40 CPU assembly requests the hardware revision numbers from the following assemblies:
A30 Digital Source
A35 Analog Source
A36 Trigger
A55/A56 Sample RAM
A71 Pass Through
A50 Digital Filter (listed as Lo/Df in test log)
A10 Analog Input (listed as channel 1 or 2 front end in test log)
A21 A/D Converter (listed as channel 1 or 2 ADC in test log)
A43 Expanded Memory (listed as Option UFG ROM in test log)
The A10 Analog Input, A21 A/D Converter, and A36 Trigger assemblies send their revision numbers through the A30 Digital Source assembly. The following shows a passing test log entry for the Power-up functional tests.

```
                    TEST LOG


Booting System

Power-up functional tests
Mult fctn peripheral . . . . . PASS
NVRAM  . . . . . PASS
Real time clock  . . . . . PASS
DIN controller . . . . . PASS
Front panel  . . . . . PASS
DSP/bus  . . . . . PASS
Additional hardware  . . . . . PASS
Sample RAM . . . . . PASS
DSP processor  . . . . . PASS

Power-up functional tests complete
```

b Determine the probable faulty assembly and next test or step by comparing the power-up test results to the following table. The power-up tests are listed in the order they are ran. If power-up test messages match more than one entry in the table, use the entry closest to the beginning of the table. Assemblies are listed in order of probable failure when more than one assembly can cause the failure.

Power-up Troubleshooting Guide

Failing Self Test or Message Displayed	Probable Faulty Assembly	Next Test or Next Step
MC68030 Processor MC68882 Coprocessor Boot ROM Stack RAM Main RAM	A40 CPU	
Display RAM DSP RAM	A47 DSP/ Display Controller	
Program ROM	A42 Memory	
Mult fctn peripheral	A40 CPU	
NVRAM Real time clock	memory battery A42 Memory	Memory battery, page 1-93
DIN controller FP kbd interface on memory board does not respond Failure during keyboard initialization	A42 Memory	
Front panel keyboard revision problem	A80 Keyboard	
DSP/ bus	A47 DSP/ Display Controller	
DSP processor DSP processor information: Failure during Sample RAM/ DSP interface test	A55/ A56 Sample RAM A47 DSP/ Display Controller	
DSP processor	A47 DSP/ Display Controller	
LAN ROM	A43 Expanded Memory	
Additional hardware Additional hardware information: *Any of the following:*		
Digital Source not found Digital Source address read problem! Digital Source revision read problem! Unable to program Digital Source hardware	A30 Digital Source	

Power-up Troubleshooting Guide

Internal Control Path 3 open Unable to write/ read Internal Control Path 3 Unable to read Internal Control Path 3 Unable to program Source DC offset	A35 Analog Source A36 Trigger A30 Digital Source	Front-end control, page 1-60-
Extended RAM and Additional I/ O not found Extended RAM Board Bus Error	A43 Expanded Memory	

Failing Self Test or Message Displayed	Probable Faulty Assembly	Next Test or Next Step
Additional hardware (continued) Additional hardware information: *Any of the following:*		
Trigger Board not found Unable to download default Trigger GA	A36 Trigger	
Sample RAM not found Sample/ Capture RAM not found Sample RAM revision read problem! Unable to read Sample RAM hardware ID Unable to program Sample RAM hardware	A55/ A56 Sample RAM	
Pass Thru not found Pass Thru address read problem! Pass Thru revision read problem! Unable to write Pass Thru control register	A71 Pass Through	
Lo/ Df not found Lo/ Df address read problem! Lo/ Df revision read problem Lo/ Df Channel 1 not found Lo/ Df Channel 2 not found Unable to reset Lo/ Df Unable to write Lo/ Df control register IF Trigger RAM test failed	A50 Digital Filter	
Channel 1 Control Path test failed Channel 2 Control Path test failed	A10 Analog Input A21 A/ D Converter A30 Digital Source	Front-end control, page 1-60
Channel *number* ADC not found	A21 A/ D Converter, channel number	
RF section not found	Configuration Setup A42 Memory	Serial port, page 1-91
Sample RAM	A55/ A56 Sample RAM	
LAN firmware Opt UFG is incompatible with main firmware. A firmware update is required.	Firmware A43 Expanded Memory	The A43 Expanded Memory assembly's ROM may not be programmed. To program, install firmware update.

Calibration ABORT Calibration information: Check source jumper?	A35 Analog Source A10 Analog Input, channel 2 A21 A/ D Converter, channel 2	Check that the jumper on the A35 Analog Source assembly is set for 2 channel operation. Source and calibrator out, page 1-62
Calibration		Step 3

3 Step 3. Check for failing functional tests.

a Press the following keys:
[clear test log]
[**Return**]
[functional tests]
[ALL]

The power-up tests are ran at the beginning of the functional all self tests. Refer to Step 1 for power-up test failures. All the power-up tests need to pass (except for calibration) before using the Self-Test Troubleshooting Guide.
The test log can be printed by connecting a printer to the serial port or HPIB port. To print the test log to a HPIB printer, press the following keys:
[**Local/ Setup**]
[system controller]
[peripheral addresses]
[printer adrs]
printer address
[enter]
[**Plot/ Print**]
[output fmt]
[device defaults]
printer type
[**Return**]
[pcl]
[**Return**]
[output to]
[HPIB]
[**Return**]
[plot item]
[all display]
[**System Utility**]
[more]
[diagnostics]
[test log **on**]
[**Plot/ Print**]
[start plot/ print]

b If the analyzer did not finish the tests (analyzer locks up), go to page 1-48, ''To troubleshoot self-test lockup failures.''

c Determine the probable faulty assembly and next test by comparing the functional test results to the following table.

If the analyzer's test log matches more than one entry in the table, use the entry closest to the beginning of the table. Assemblies are listed in order of probable failure when more than one assembly can cause the failure.

The table lists the probable faulty assembly or assemblies and troubleshooting procedure to do before replacing an assembly. The messages in the table include only the parts of the failure messages that point to the assemblies failing. For example, many of the failure messages give the channel number (1 or 2), amplitude (mkr y: *amplitude*), and frequency (mkr x: *frequency*) of the failure.

Self-Test Troubleshooting Guide

Failing Self Test or Message Displayed	Status	Probable Faulty Assembly	Next Test
Skipping time cal *(Time for an analyzer calibration. This message can appear anywhere in the test log.)*		This is not a failure message.	
Full Sample RAM Full Sample RAM information: Cal HW Timeout in readTrigPoints() Failed to trigger *and all of the following:* Digital Source Digital filter ADC . .	ABORT PASS PASS PASS	A36 Trigger A10 Analog Input A30 Digital Source A55/ A56 Sample RAM A50 Digital Filter	Trigger, page 1-83-
Full Sample RAM *(This is probably not a sample RAM failure. The sample RAM information will state why the self test aborted.)*	ABORT	Go to next self test failing.	
Full Sample RAM . Full Sample RAM information: RAM *number* test failed	FAIL	A55/ A56 Sample RAM	
Full Sample RAM Full Sample RAM information: *Any of the following:* Address counter verification failed Counter *number* interrupt test failed Counter 2 failed Counter 1 failed	FAIL	A55/ A56 Sample RAM	
Full Sample RAM Full Sample RAM information: *Any of the following:* Single channel pre-trigger failed Single channel post-trigger failed Two channel pre-trigger failed Two channel post-trigger failed *and both of the following:* Digital Source . Digital filter	FAIL PASS PASS	A36 Trigger A55/ A56 Sample RAM	Trigger, page 1-83-
Full Sample RAM .	FAIL	A55/ A56 Sample RAM	

Failing Self Test or Message Displayed	Status	Probable Faulty Assembly	Next Test
Digital Source *and both of the following:* Digital filter ADC.	FAIL PASS PASS	A30 Digital Source	
Digital Source Digital Source information: LO sine wave test failed	FAIL	A30 Digital Source	
Digital Source	FAIL *or* ABORT	A10 Analog Input A21 A/ D Converter A30 Digital Source A50 Digital Filter	Input and ADC, page 1-71
Digital filter .	FAIL	A50 Digital Filter	
ADC.	ABORT	A35 Analog Source A21 A/ D Converter	Source and calibrator out, page 1-62-
ADC . ADC information: Channel *number*	FAIL	A21 A/ D Converter, channel *number*	
Analog source Analog source information: Any of the following: Analog source check failed, Input check passed Calibrator check failed, Input check passed Reconstruction filter check failed 75 Ω impedance check failed	FAIL	A35 Analog Source	
Analog source	FAIL *or* ABORT	A35 Analog Source A10 Analog Input A21 A/ D Converter A30 Digital Source	Source and calibrator out, page 1-62
Input Input information: *Any of the following:* channel 1 fails flatness test channel 1 fails DC gain test	FAIL *or* ABORT	A10 Analog Input A21 A/ D Converter	Input and ADC, page 1-71
Input. Input information: *Any of the following:* channel *2* fails flatness test channel 2 fails DC gain test	FAIL *or* ABORT	A10 Analog Input A21 A/ D Converter	Two channel analyzer, page 1-75

Failing Self Test or Message Displayed	Status	Probable Faulty Assembly	Next Test
Calibration Calibration information: Channel *number* fails pad test	FAIL	A10 Analog Input, channel *number*	
Calibration Calibration information: Calibrator way out of range	FAIL		To adjust calibrator, page 2-37
Calibration Calibration information: *Any of the following:* Source fails level test Calibrator level message Calibrator gain reset to 1.0 Auto-zero: can't compensate CH1 DC offset. Can't compensate CH1 DC offset.	FAIL *or* ABORT	A35 Analog Source A10 Analog Input A21 A/ D Converter A30 Digital Source	Source and calibrator out, page 1-62
Calibration Calibration information: *Any of the following:* Auto-zero: can't compensate CH2 DC offset. Can't compensate CH2 DC offset.	FAIL *or* ABORT	A10 Analog Input, channel *2* A21 A/D Converter, channel 2	Two channel analyzer,page 1-75
Calibration Calibration information: *Any of the following:* Failure in partial trigger counter Partial trigger cal: can't trigger! Bad value from partial sample counter Exceeded trigger jitter limits Cal HW Timeout in readTrigPoints() Cal HW Timeout in getTimeAvgData() Failed to trigger	FAIL *or* ABORT	A36 Trigger A10 Analog Input A55/ A56 Sample RAM A50 Digital Filter A30 Digital Source	Trigger, page 1-83
Calibration Calibration information: Hardware timeout occurred during calibration while waiting for sample RAM to acquire data.	ABORT	A36 Trigger A10 Analog Input	Check cables to A36 Trigger Trigger, page 1-83
Calibration Calibration information: *Use the information to help isolate the failure*	FAIL *or* ABORT		Performance test, page 1-58
All self tests and calibration	PASS		Step 4

4 Determine the probable faulty assembly and next test by comparing the analyzer's symptoms to the following table.

For additional information on the self tests, see the self-test descriptions starting on page 7-13

Failure	Probable Faulty Assembly	Next Test
Disk Drive	Disk Drive Diskette W5 Ribbon Cable A42 Memory	Disk drive, page 1-88
HPIB	HPIB Connector A42 Memory	Step 5
Serial Port	Serial Port A42 Memory	Serial port, page 1-91
Rear panel oven ref out	A95 F357 fuse A85 Oven	Step 6
Rear panel ext ref out	A60 Frequency Reference	
Rear panel ext ref in	A60 Frequency Reference	
Rear panel sync out or parallel port	A30 F1 fuse A30 F2 fuse A30 Digital Source	Sync out and parallel port, page 1-95
System interconnect ThinLAN AUI port	A43 Expanded Memory	System interconnect and LAN port,page 1-96
Probe Power	A95 F1 fuse A92 Probe Power	Step 7
Random Noise	A30 Digital Source	
Rear panel EXT ARM	A36 Trigger	
Front panel external trigger	A36 Trigger	
Source	A35 Analog Source A30 Digital source	Source and calibrator out, page 1-62-
Auto-range Over-range	A36 Trigger A10 Analog Input A21 A/ D Converter	Auto-range,page 1-80
Input Any of the following functions: ch *number* input Z 75 Ω ch *number* input Z 1 MΩ ch *number* coupling ch *number* alias LPF	A10 Analog Input, ch *number*	
External Keyboard	A80 F1 fuse External Keyboard A80 Keyboard	DIN connector, page 1-92

Performance test	Performance test, page 1-58
Intermittent failure	Intermittent, page 1-52-

5 Check the HPIB controller on the A42 Memory assembly.

a Press the following keys:
[**System Utility**]
[more]
[diagnostics]
[functional tests]
[I/ O]
[HPIB controller]

b If the HPIB controller test fails, the A42 Memory assembly is probably faulty.

6 Check the oven fuse on the A95 Main Power Supply assembly.

a Set the power switch to off (O).

b Turn the analyzer upside down.

c Remove the bottom cover.

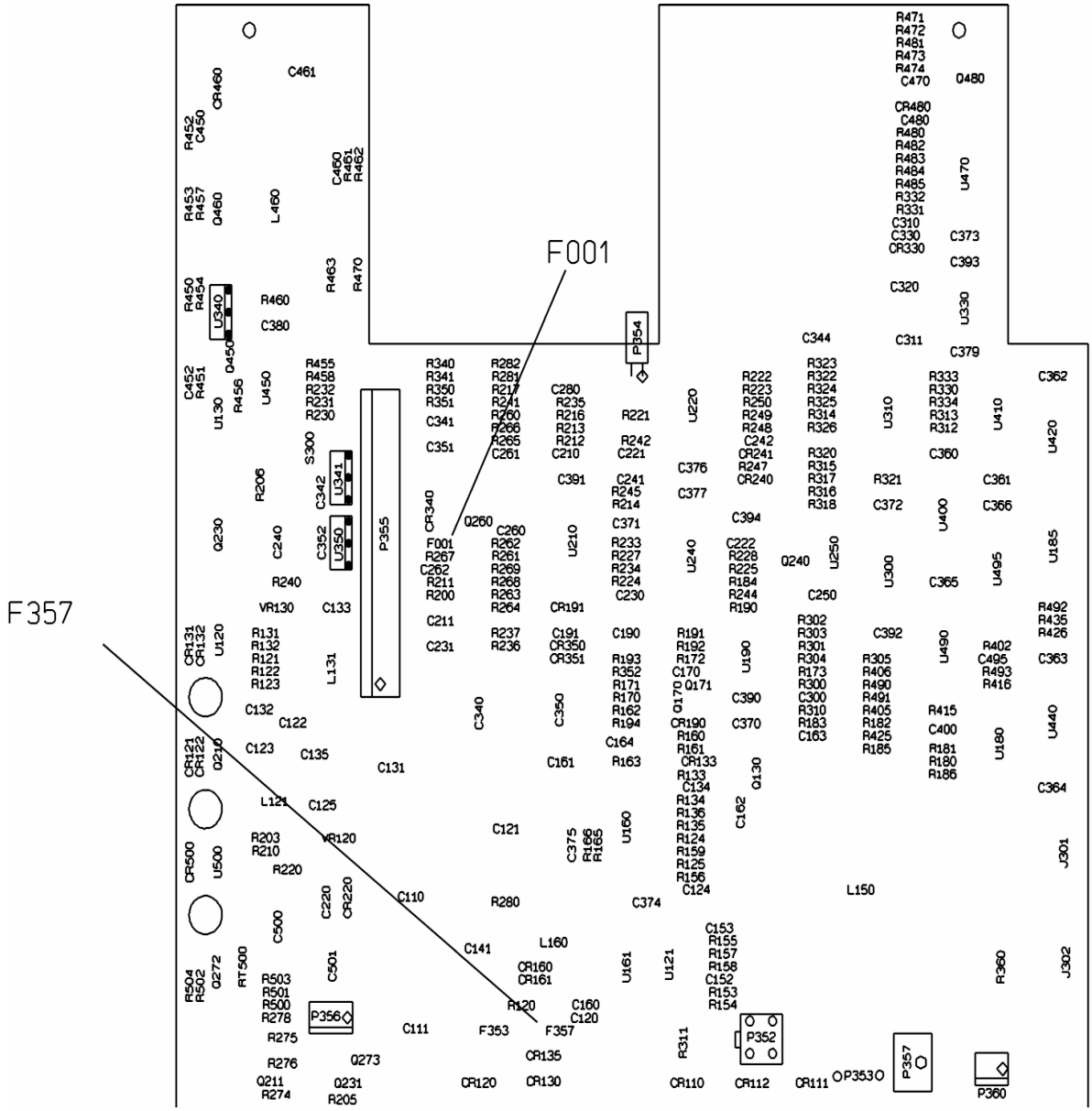
d Wait five minutes to allow time for the power supply capacitors to discharge.

e Remove the black power supply shield.

f Measure the resistance across F357.

g If the resistance is 0Ω, the A85 Oven assembly is probably faulty.

h If the resistance was greater than 0Ω, replace the fuse.



7 Check the probe power fuse on the A95 Main Power Supply assembly.

a Set the power switch to off (O).

b Turn the analyzer upside down.

c Remove the bottom cover.

d Wait five minutes to allow time for the power supply capacitors to discharge.

e Remove the black power supply shield.

f Measure the resistance across F1.

g If the resistance is 0Ω, the A92 Probe Power assembly is probably faulty.

h If the resistance was greater than 0Ω, replace the fuse.

To troubleshoot self-test lockup failures

Use this test to continue troubleshooting if calibration or the functional test ''ALL'' locks up the analyzer.

1 Check for failing self tests.

a Set the power switch to off (O).

b Press and hold [**Return**] (below softkeys) while setting the power switch to
on (l).
Pressing [**Return**] while setting the power switch to on (l) causes the analyzer to bypass the calibration routine.

c When the power-up tests are finished, press the following keys:
[**System Utility**]
[auto cal **off**]
[more cal setup]
[auto zero cal **off]**
[**Return**]
[more]
[diagnostics]
[service functions]
1125
[enter]
[test log]

d If any of the power-up tests fail, go to page 1-32, ''To perform self tests,'' and do Step 2 to determine the probable faulty assembly or next test.
The power-up test results are saved in the test log. Use the RPG knob to scroll through the test log. The test log can also be displayed at power-up by pressing and holding [.] [**3**] while setting the power switch to on (l). The fault log can be displayed at power-up by pressing and holding [.] [**4**] while setting the power switch to on (l). Fault log messages are described on page 7-9

e Press the following keys in the order listed. Allow enough time for each test to finish before pressing the next key.
[**Return**]
[functional tests]
[sample RAM]
[digital filter]
[digital source]
[ADC]
[more]
[analog source]
[input]
[calibration]
A failure may cause the self tests to be very slow. Wait three minute before assuming the analyzer is locked up.

f Determine the probable faulty assembly and next test or step by comparing the self-test results to the following table.
If the analyzer's test log matches more than one entry in the table, use the entry closest to the beginning of the table. The table lists the probable faulty assembly or assemblies and troubleshooting procedure to do before replacing an assembly. Assemblies are listed in order of probable failure when more than one assembly can cause the failure. The messages in the table include only the parts of the failure messages that point to the assemblies failing. For example, many of the failure messages give the channel number (1 or 2), amplitude (mkr y: *amplitude*), and frequency (mkr x: *frequency*) of the failure.

Failing Self Test or Message Displayed	Status	Probable Faulty Assembly	Next Test or Step
Skipping time cal *(Time for an analyzer calibration. This message can appear anywhere in the test log.)*		This is not a failure message.	
Full Sample RAM . *(This is probably not a sample RAM failure. The sample RAM information will state why the self test aborted.)*	ABORT	Go to next self test failing.	
Full Sample RAM	FAIL *or locks analyzer*	A55/ A56 Sample RAM	
Digital filter	FAIL *or locks analyzer*	A50 Digital Filter	
Digital Source	Locks analyzer	A30 Digital Source A55/ A56 Sample RAM	Step 3
Digital Source	FAIL	A30 Digital Source	
Digital Source	ABORT	A10 Analog Input A21 A/ D Converter A30 Digital Source A50 Digital Filter	Input and ADC, page 1-71
ADC	ABORT	A35 Analog Source A21 A/ D Converter	Source and calibrator out, page 1-62
ADC ADC information: Channel *number*	FAIL *or locks analyzer*	A21 A/ D Converter, channel *number*	If ADC self test locks 2 channel analyzer and there is no failure information, go to Two channel analyzer, page 1-75
Analog source	FAIL, ABORT, *or locks analyzer*	A35 Analog Source A10 Analog Input A21 A/ D Converter A30 Digital Source	Source and calibrator out, page 1-62
Input	FAIL, ABORT, *or locks analyzer*	A10 Analog Input A21 A/ D Converter	Input and ADC, page 1- or Two channel analyzer, page 1-75
Calibration	Locks analyzer	A35 Analog Source A10 Analog Input A21 A/ D Converter A30 Digital Source	Source and calibrator out, page 1-62

2 Repeat the sample RAM self test without the Digital Source assembly.

a Set the power switch to off (O).

b Pull the A30 Digital Source assembly out of the card nest about 1 inch.

c Set the power switch to on (l).

d When the power-up tests are finished, press the following keys:
[**System Utility**]
[auto cal **off**]
[more cal setup]
[auto zero cal **off**]
[**Return**]
[more]
[diagnostics]
[service functions]
1125
[enter]
[test log]
[**Return**]
[functional tests]
[sample RAM]

e If the sample RAM self test fails or aborts, the A55/A56 Sample RAM assembly is probably faulty.

f If the sample RAM self test passes, the A30 Digital Source assembly is probably faulty.

To troubleshoot intermittent failures

Use this test to help isolate intermittent failures to the assembly.

1 Check that the analyzer has the latest firmware revision.
See service note Agilent 89410A-01 for description of updates.

2 Step 2. Determine if your intermittent failure is caused by one of the following common causes.

Common Causes	Troubleshooting Procedure
Loose screws and cables	Check that the screws in the analyzer are tight and that the cables are firmly in their sockets. It is especially important to check the SMB cables connecting the front-end analog assemblies.
Loose or bent pins on motherboard connectors	Pull out each assembly connected to a motherboard and check the pins. See the ''Assembly Connections'' illustration on page 6-6 for assemblies connected to the motherboards.
Out-of-adjustment	Do the adjustments for the analyzer in chapter 2.
Air flow restricted	The analyzer cools by drawing air from the back and blowing out the sides. Check that the air flow was not restricted in these areas when the failure occurred. If the analyzer overheats, the power supply and fan will shut down and the Overtemp LED will be lit. Go to page page 1-15
Power supply voltages	Check for correct power-supply voltages. Go to page page 1-15
External voltage	Verify that the line voltage is within the electrical specification for the analyzer. See power requirements in the *Agilent 89410A Technical Data* publication.

3 Step 3. Run the functional tests in loop mode.

a Set the power switch to on (l).

b When the power-up tests are completed, press the following keys:
[**System Utility**]
[auto cal **off**]
[more cal setup]
[auto zero cal **off**]
[Return]
[**more**]
[diagnostics]
[service functions]
1125
[enter]
[test log]
[clear test log]
[Return]
[loop mode setup]
[until failure]
[**Return**]
[functional tests]
[ALL]
The analyzer runs the functional tests until a failure occurs, then writes the failure message in the test log and stops.

c If a failure message occurs, go to ''To perform self tests'' on page page 1-32 to compare the error message to the ''Self-Test Troubleshooting Guide.''

4 Determine the probable faulty assembly or next test by comparing the fault log entries to the following table.

a Press the following keys:
[**Preset**]
[Return]
[fault log]
Pressing [**Preset**] while a functional test is running will cause the self test to abort. This should not be counted as a failure.

b Compare the fault log entries to the following table.
The order that the messages are listed in the table is not significant. If fault log messages match more than one entry in the table, all assemblies listed for each message should be suspected and the assembly common to each fault log message is most likely the faulty assembly. Assemblies are listed in order of probable failure when more than one assembly can cause the

failure.See ''Fault Log Messages'' on page 7-9for detailed descriptions of each fault log message.

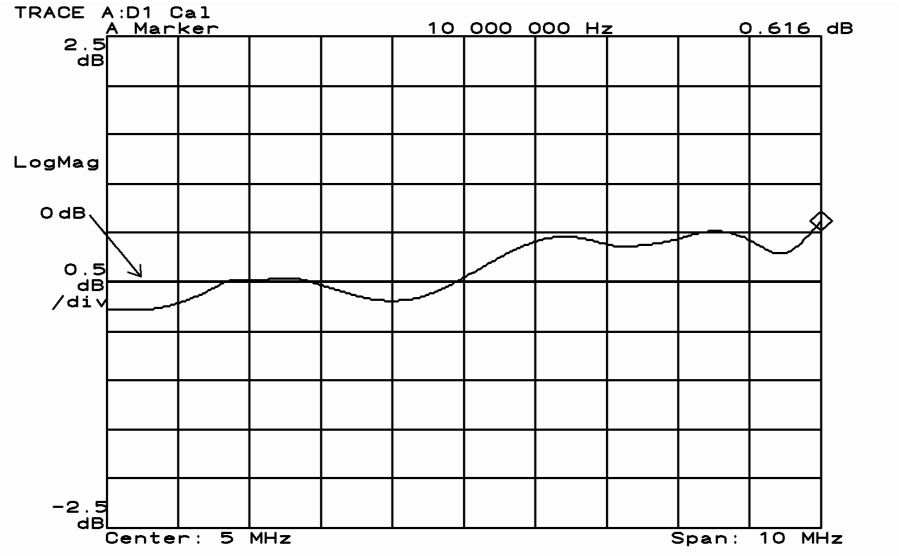
Failing Message Displayed	Probable Faulty Assembly	Next Test
System Error System Error during Calibration	A40 CPU A47 DSP/ Display Controller A42 Memory A30 Digital Source A50 Digital Filter A43 Expanded Memory A71 Pass Through	Initial verification, page 1-10
Internal Disk Trk0 Failure	A101 Disk Drive A42 Memory Disk drive cable	Disk drive, page 1-88-
NVRAM or Battery Failure Floppy Controller Timeout	memory battery A42 Memory	Memory battery, page 1-93-
Input Tripped	User over-voltage connected to input A10 Input	
Source Tripped	User over-voltage connected to source A35 Analog Source	
Real Time Clock Timeout	A42 Memory	
CPU Failure CPU Board Bus Error	A40 CPU	
Memory Board Bus Error Memory Board Failure	A42 Memory	
Display/ DSP Board Bus Error DSP Failure Display Failure	A47 DSP/ Display Controller	
Digital Source Board Bus Error Digital Source Board Failure	A30 Digital Source	
Internal Control Path 3 Failure	A35 Analog Source A36 Trigger A30 Digital Source	Front-end control, page 1-60
Trigger Board Failure	A36 Trigger A35 Analog Source A30 Digital Source	Front-end control, page 1-60
Sample/ Capture RAM Board Bus Error Sample/ Capture RAM Board Failure	A55/ A56 Sample RAM	
Pass Thru Board Bus Error Pass Thru Board Failure	A71 Pass Through	
Digital Filter Board Bus Error Digital Filter Board Failure	A50 Digital Filter	

Failing Message Displayed	Probable Faulty Assembly	Next Test
Channel 1 Control Path Failure Channel 2 Control Path Failure	A10 Analog Input A21 A/ D Converter A30 Digital Source	Front-end control,page 1-60
Calibration Failure Calibration Hardware Timeout	A10 Analog Input A35 Analog Source A21 A/ D Converter A36 Trigger A30 Digital Source Any assembly can cause these failure messages	
Calibration Failure — Source Level	A35 Analog Source A10 Analog Input A21 A/ D Converter	Source and calibrator out, page 1-62
Calibration Failure — Bad Data Calibration Failure — Channel 1 DC Gain Calibration Failure — Channel 2 DC Gain Calibration Failure — Channel 1 Flatness Calibration Failure — Channel 2 Flatness Calibration Failure — Channel 1 Auto Zero Calibration Failure — Channel 2 Auto Zero	A10 Analog Input A21 A/ D Converter A35 Analog Source	Source and calibrator out, page 1-62
Calibration Failure — Channel 1 Pads Calibration Failure — Channel 2 Pads	A10 Analog Input	
Calibration Failure — Source Level	A35 Analog Source A10 Analog Input A21 A/ D Converter	Source and calibrator out, page 1-62
Calibration Failure — Channel 1 Trigger Calibration Failure — Channel 2 Trigger	A10 Analog Input	Trigger,page 1-83

5 Check the calibration correction curves.

a Press the following keys:
[**Preset**]
[**System Utility**]
[auto cal **off**]
[more cal setup]
[auto zero cal **off**]
[**Measurement Data**]
[freq response]
[**Ref Lvl/ Scale**]
[Y ref level]
0
[dB]
[Y per div]
0.5
[dB]
[rng tracking **off**]
[ref position]
50
[%]
[ref line **on**]
Since there is no input, the display will show lines across the screen.

b Press the following keys for each of the primary calibration ranges:
The primary calibration ranges are -14, –12, –10, –8, –6, and 0 dBm.
[**Range**]
[ch1 range]
primary calibration range
[dBm]
[**System Utility**]
[more cal setup]
[save ch1 cal trace]
[into D1]
[**Measurement Data**]
[data reg]
[D1]
The following is a typical calibration correction curve display:



c If the analyzer has the optional second channel, repeat the previous two steps for channel 2.

After pressing [**Preset**], press [B] [Range] [channel 2] and substitute [ch2 range] for [ch1 range].

d If a calibration curve is not within +2.5 dB and -1 dB of the range level setting, go to page page 1-62‘’To troubleshoot source and calibrator out failures’’ or page 1-71- ‘’To troubleshoot input and ADC failures.’’

To troubleshoot performance test failures

Use this test when a performance test is failing and the self tests passed except for calibration.

1 Determine if an adjustment is causing the analyzer to fail a performance test.

   a Do the adjustments in chapter 2, ''Adjusting the Analyzer'' for the following assemblies:
   A10 Analog Input
   A21 A/D Converter
   A35 Analog Source
   A60 Frequency Reference
   A61 Clock

   b Repeat the failing performance test.

2 Determine the probable faulty assembly or next test by comparing the performance test results to the following table.
If more than one performance test fails, use the entry closest to the beginning of the table. The table lists the assembly or assemblies most likely to cause the failure. In some cases, the failure can be isolated to one assembly based on the exact failure. When the cause of the failure cannot be isolated to one assembly, an additional test is provided to help isolate the faulty assembly. Multiple probable faulty assemblies are listed in order of probability.

Failing Performance Test	Probable Faulty Assembly (in order of probability)	Troubleshooting Test
DC Offset	A10 Analog Input A21 A/ D Converter	Input and ADC, page 1-71 or Two channel analyzer, page 1-75
Amplitude Accuracy	A10 Analog Input A35 Analog Source A21 A/ D Converter	Source and calibrator out, page 1-62-
Amplitude Linearity	A10 Analog Input A21 A/ D Converter	Input and ADC, page 1-71- or Two channel analyzer,page 1-75
Frequency Accuracy	A60 Frequency Reference A61 Clock	Initial verification, page 1-10, Step 5, Use a frequency counter instead of an oscilloscope.
Amp_Phase Match	A10 Analog Input A21 A/ D Converter A36 Trigger	Amplitude failure: Two channel analyzer, page 1-75- Phase Match failure: Trigger, page 1-83
Cross Talk Anti-Alias Filter Input Coupling Input Capacitance Input resistance Input Rtn Loss	A10 Analog Input	
Harmonic Distortion Spurious Signals Intermodulation Distortion Noise	A10 Analog Input A21 A/ D Converter	Input and ADC, page 1-71 or Two channel analyzer, page 1-75
External Trigger External Arm	A36 Trigger	
Input Trigger	A10 Analog Input A36 Trigger	Trigger, page 1-83
Source Amplitude Accuracy Source Rtn Loss Source Distortion	A35 Analog Source	

To troubleshoot front-end control failures

Use this test when a control path test fails or an assembly is not found.

1 Check the digital source.

a Set the power switch to on (l).

b After the power-up routine is finished, press the following keys:
[**System Utility**]
[auto cal **off**]
[more cal setup]
[auto zero cal **off**]
[**Return**]
[more]
[diagnostics]
[service functions]
1125
[enter]
[test log]
[**Return**]
[functional tests]
[digital source]

c Determine the probable faulty assembly, next step, or test by comparing the self-test results to the following table.

Digital Source Self-test Result	Power-up tests Additional hardware information	Probable Faulty Assembly, Next Test or Step
PASS	*Two channel analyzer:* Channel *number* Control Path test failed Channel *number* Front End not found	Two channel analyzer,page 1-75
PASS	*Single channel analyzer:* Channel 1 Control Path test failed Channel 1 Front End not found	Step 2
PASS	Internal Control Path 3 open Unable to write/ read Internal Control Path 3 Unable to read Internal Control Path 3 Unable to program Source DC offset	A35 Analog Source
FAIL		A30 Digital Source
Locks up analyzer		Step 2

2 Check front-end control loop signals.

a Place the analyzer on the side closest to the display.

b Remove the bottom cover.

c Press the following keys:
[**Return**]
[loop mode setup]
[forever]
[**Return**]
[functional tests]
[power-up tests]
[more]
[additional hardware]

d Using a logic probe, check that the TTL signals listed in the following table are toggling.

Test Location	Signal Name	Probable Faulty Assembly
A91 P6 pin 16	FSA1	A60 Frequency Reference
A91 P6 pin 10	CLK25M	A60 Frequency Reference
A91 J4 pin 18A	FECLK1	A30 Digital Source
A91 J5 pin 18A	FECLK2	A30 Digital Source
A91 J6 pin 19B	FECLK3	A30 Digital Source
A91 J2 pin 29A	FEDATA	A30 Digital Source
A91 J2 pin 30A	nFEPROG	A30 Digital Source
A91 J2 pin 30B	FELATCH	A30 Digital Source
A91 J2 pin 28B	FELOOP1	A21 A/ D Converter
A91 J4 pin 17B	FERET1	A10 Analog Input
A91 P1 pin 43	FELOOP3	A36 Trigger
A91 J6 pin 18B	FERET3	A35 Analog Source

e If a signal is incorrect, replace the probable faulty assembly.

f Press [**Preset**] to stop the loop mode.
Probing the signals on the motherboard may cause the self test to fail or abort.

g If the signals are correct in the previous table, go to the next test, ''To troubleshoot source and calibrator out failures.''

To troubleshoot source and calibrator out failures

Use this test when the analog source or calibrator is suspected of failing and all self tests listed before the ADC in the Self-Test Troubleshooting Guide on page 1-32 passed.

1 Check the sine wave output.

a Set the power switch to on (l).

b Using a BNC cable, connect an oscilloscope to the SOURCE output.

c Set the oscilloscope as follows:

CH1 V/div	400 mV/div
Input Impedance	50 Ω
CH1 Coupling	dc
Probe Atten	1
Display Mode	Real Time
Time/div	200 ns/div
Trigger	Trg'd Sweep
Trig Src	Chan1
Trigger Level	0 V

d Press the following keys:
[**System Utility**]
[auto cal **off**]
[more cal setup]
[auto zero cal **off**]
[**Source**]
[source **on**]
[level]
1
[V]

e The oscilloscope should display a 1 MHz, 2 Vp-p sine wave with no dc offset. If the signal is incorrect, go to Step 7.
This is only a quick check of the source sine wave. If the source is suspected of failing at a specific frequency or amplitude, check

the source sine wave at the failing values. If the signal is incorrect, go to Step 7.

f Set the oscilloscope to 600 mV/div.

g Press the following keys:
[DC offset]
[**Marker/ Entry**]

h Rotate the RPG knob while monitoring the oscilloscope. The sine wave dc offset value should change from +1 V to -1 V as the RPG knob is turned.
To keep the sine wave displayed, adjust the oscilloscope's trigger level while varying the dc offset value.

i If the dc offset function operates correctly, go to Step 3.

2 Check the DC offset control signals.

a Place the analyzer on the side closest to the display.

b Remove the bottom cover.

c Press the following keys:
[**Preset**]
[**Source**]
[source **on**]
[DC offset]
[**Marker/ Entry**]

d Using a logic probe, check the TTL signals listed in the following table while rotating the RPG knob. The signals should toggle as the dc offset is varied from minimum to maximum.

Test Location	Signal Name
A91 J6 pin 12B	OFF[0]
A91 J6 pin 12C	OFF[1]
A91 J6 pin 13B	OFF[2]
A91 J6 pin 13C	OFF[3]
A91 J6 pin 14B	OFF[4]
A91 J6 pin 14C	OFF[5]
A91 J6 pin 15B	OFF[6]
A91 J6 pin 18A	NOFFWR

e If the signals are correct, the A35 Analog Source is probably faulty.

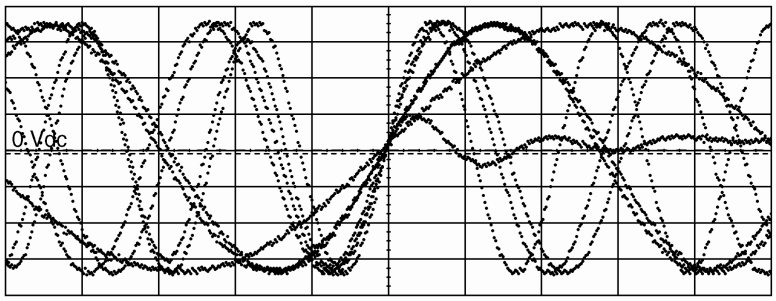
f If any of the signals are incorrect, the A30 Digital Source assembly is probably faulty.

3 Check the periodic chirp output.

a Press the following keys:
[DC offset]
0
[V]
[source type]
[periodic chirp]

b Using an oscilloscope and 1:1 probe, check the following signal.

Oscilloscope Setup		Parameters	Waveform
Connect CH1 to SOURCE		Variations	
CH1 V/ div	300 mV/ div		
Input Impedance	50 Ω		
CH1 Coupling	dc		
Probe Atten	1		
Display Mode	Repetitive		
Averaging	off		
Persistence	500 ms		
Time/ div	50 ns/ div		
Trigger	Trg'd Sweep		
Trig Src	Chan1		



Periodic Chirp

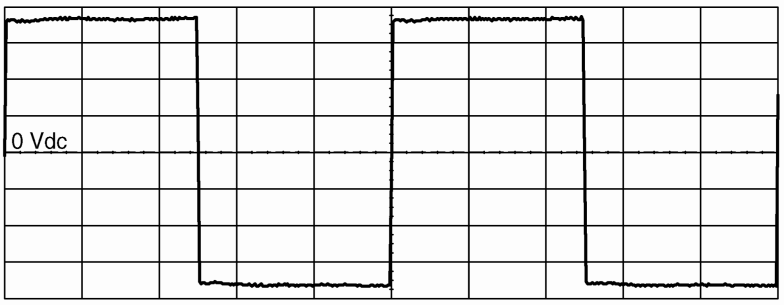
c If the signal is incorrect, go to Step 7.

4 Check the calibrator output.

a Press the following keys:
[**Preset**]
[**System Utility**]
[auto cal **off**]
[more cal setup]
[auto zero cal **off**]
[**Return**]
[more]
[diagnostics]
[service functions]
1125
[enter]
[special test modes]
[cal]
[cal signal on]

b Using an oscilloscope and 1:1 probe, check the following signal.

Oscilloscope Setup		**Parameters**	**Waveform**
Connect CH1 to SOURCE		Amplitude Time Duty Cycle Pulse Shape	
CH1 V/ div	20 mV/ div		
Input Impedance	50 Ω		
CH1 Coupling	dc		
Probe Atten	1		
Display Mode	Repetitive		
Averaging	8		
Time/ div	500 ns/ div		
Trigger	Trg'd Sweep		
Trig Src	Chan1		
Trigger Level	0 V		



Calibrator

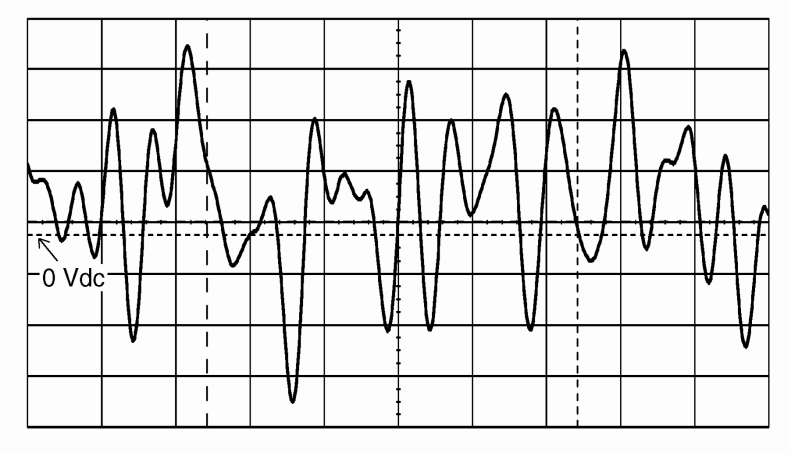
c If the signal is incorrect, go to Step 7.

5 Check the random noise output.

a Press the following keys:
[cal signal **off**]
[**Source**]
[source **on**]
[level]
1
[V]
[source type]
[random noise]

b Using an oscilloscope and 1:1 probe, check the following signal.

Oscilloscope Setup		Parameters	Waveform
Connect CH1 to SOURCE		Variations No Pattern	
CH1 V/ div	100 mV/ div		
Input Impedance	50 Ω		
CH1 Coupling	dc		
Probe Atten	1		
Display Mode	Real Time		
Resolution	7 bits		
Time/ div	200 ns/ div		
Trigger	Trg'd Sweep		
Trig Src	Chan1		



Random Noise

c If the random noise source is incorrect, the A30 Digital Source assembly is probably faulty.
This is only a quick check of the random noise signal. Do the Random Noise performance test to thoroughly check the random noise signal.

6 Step 6. Check the source attenuation.

a Connect a digital multimeter to the SOURCE output using a 50 Ω feedthrough termination and BNC cable.

b Press the following keys:
[CW (fixed sine)]
[**Return**]
[sine freq]
1
[kHz]
[level]
5
[V]
[**System Utility**]
[more]
[diagnostics]
[service functions]
[special test modes]
[source]
[**Marker/ Entry**]

c Slowly rotate the RPG knob while monitoring the digital multimeter. The sine wave's amplitude should vary as follows.

Source Attenuation	Source Amplitude (nominal)		
	dBm	Vp-p	Vrms
0	24	10.0	3.54
1	14	3.17	1.12
2	4	1.00	354 m
3	–6	317 m	112 m
4	–16	100 m	35.4 m
5	–26	31.7 m	11.2 m
6	–36	10.0 m	3.54 m
7	–46	3.17 m	1.12 m

d If all the values are incorrect, go to Step 7.

e If only a few of the values are incorrect, the A35 Analog Source is probably faulty.

f If all the values are correct, the analog source and calibrator are operating correctly. For a single channel analyzer, go to page 1-71, ''To troubleshoot input and ADC failures.'' For a two

channel analyzer, go to page 1-75, ''To troubleshoot two channel analyzer failures.''

7 Check frequency sample signals.

a Place the analyzer on the side closest to the display.

b Remove the bottom cover.

c Press [**Preset**].

d Using a logic probe, check that the TTL signals listed in the following table are toggling.

Test Location	Signal Name
A91 P6 pin 4	FSAAD
A91 P6 pin 5	FSASRC
A91 P6 pin 11	FSA2
A91 P6 pin 16	FSA1

e If any of the signals are incorrect, the A60 Frequency Reference assembly is probably faulty.

8 Check DAC signals.

a Press the following keys:
[**Preset**]
[**Source**]
[source **on**]

b Using a logic probe, check that the TTL signals listed in the following table are toggling.

Test Location	Signal Name
A91 J6 pin 4A	DAC[0]
A91 J6 pin 4C	DAC[1]
A91 J6 pin 5B	DAC[2]
A91 J6 pin 6A	DAC[3]
A91 J6 pin 6C	DAC[4]
A91 J6 pin 7B	DAC[5]
A91 J6 pin 8A	DAC[6]
A91 J6 pin 8C	DAC[7]
A91 J6 pin 9B	DAC[8]
A91 J6 pin 10A	DAC[9]
A91 J6 pin 10C	DAC[10]
A91 J6 pin 11B	DAC[11]

c If any of the signals are incorrect, the A30 Digital Source assembly is probably faulty.

d If the signals are correct, the A35 Analog Source assembly is probably faulty. Before replacing the A35 Analog Source assembly, go to page 1-15, ''To troubleshoot the power supply,'' and do Step 7 to check the -8 V power supply.

To troubleshoot input and ADC failures

Use this test to isolate input failures to the A10 Analog Input assembly or A21 A/D Converter assembly.

1 Check the input path.

a Set the synthesizer as follows:

Frequency	1 MHz
Amplitude	2 Vp-p
Function	Sine Wave

b Set the oscilloscope as follows:

CH1 V/div	30 mV/div
Input Impedance	50 Ω
CH1 Coupling	dc
Time/div	200 ns/div
Probe Atten	1

c Press the following keys:
[**System Utility**]
[auto cal **off**]
[more cal setup]
[auto zero **off**]
[**Range**]
1
[V]

d Connect the synthesizer to the front panel CHANNEL 1 input using a BNC cable.

e Remove the top cover.

f Using the oscilloscope and a BNC(m)-to-SMB(f) cable, check the following signals:

Test Location	Signal Name	Amplitude (± 10%)
A10 J2	ANALOGIN	193 mVp-p
A10 J3	TRIGGER	687 mVp-p

g If the signals are incorrect, the A10 Analog Input assembly is probably faulty.

h Reconnect A10 J3 to A36 J5 and A10 J2 to A21 J4.
This is only a quick check of the A10 Analog Input assembly. If the assembly is still suspected of failing, set the analyzer to the

failing range, impedance, and frequency. Input a full scale signal. If the input level equals the range level, A10 J2 and A10 J3 should match the amplitudes in the above table.

2 Check the dc offset DAC.

a Connect the oscilloscope to A10 J2 using the BNC(m)-to-SMB(f) cable.

b Press the following keys:
[**System Utility**]
[more]
[diagnostics]
[service functions]
1125
[enter]
[special test modes]
[input]
[**Marker/ Entry**]

c Rotate the RPG knob while monitoring the oscilloscope. The sine wave dc offset value should change from +0.4 V to -0.4 V as the RPG knob is turned.
To keep the sine wave displayed, adjust the oscilloscope's trigger level while varying the dc offset value.

d If the dc offset function is incorrect, the A10 Analog Input assembly is probably faulty.

e Reconnect A10 J2 cable to A21 J4.

3 Check the trigger offset DAC.

a Connect the oscilloscope to A10 J3 using the BNC(m)-to-SMB(f) cable.

b Press the following keys:
[dc offset]
2000
[enter]
[trig offset]

c Rotate the RPG knob while monitoring the oscilloscope. The sine wave dc offset value should change from +0.4 V to -0.4 V as the RPG knob is turned.

To keep the sine wave displayed, adjust the oscilloscope's trigger level while varying the trigger offset value.

d If the trigger offset function is incorrect, the A10 Analog Input assembly is probably faulty.

e Reconnect A10 J3 to A36 J5.

f Disconnect the synthesizer from CHANNEL 1.

4 Check the analog source to input path.

a Press the following keys:
[**Preset**]
[**Source**]
[source **on**]
[level]
0
[dBm]
[**System Utility**]
[auto cal **off**]
[more cal setup]
[auto zero cal **off**]
[**Return**]
[more]
[diagnostics]
[service functions]
[special test modes]
[input]
[source]

b Connect the oscilloscope to A10 J2 using the BNC(m)-to-SMB(f) cable.

c The oscilloscope should display a 130 ±13 mVp-p sine wave.

d If the signal is correct, go to Step 5.

e Place the analyzer on the side closest to the display.

f Remove the bottom cover.

g Set the oscilloscope as follows:

CH1 V/div	100 mV/div
Input Impedance	1 MΩ
CH1 Coupling	dc

Time/div	200 ns/div
Probe Atten	1

h Connect a high impedance 1:1 oscilloscope probe to A91 J6 pin 29B.
The signal should be 423 ±42 mVp-p.

i If the signal is incorrect, the A35 Analog Source assembly is probably faulty.

5 Check the frequency sample signals.

a Reconnect A10 J2 to A21 J4.

b Place the analyzer on the side closest to the display.

c Remove the bottom cover.

d Press [**Preset**].

e Using a logic probe, check that the TTL signals listed in the following table are toggling.

Test Location	Signal Name
A91 P6 pin 4	FSAAD
A91 P6 pin 11	FSA2
A91 P6 pin16	FSA1

f If the signals are incorrect, the A60 Frequency Reference assembly is probably faulty.

g If the signals are correct, the A21 A/D Converter assembly is probably faulty.
This test does not check the A71 Pass Through assembly. The Pass Through assembly buffers the signals from the A21 A/D Converter assembly before they go to the A50 Digital Filter assembly. There is a separate set of buffers for each channel. The Pass Through assembly is less likely to fail than the A21 A/D Converter assembly.

h If the calibration error message is ''Channel 1 fails flatness test,'' the A50 Digital Filter assembly may be failing even though the digital filter self test passes.
If replacing the A21 A/D Converter assembly does not fix the failure, the A71 Pass Through assembly or A50 Digital Filter assembly is probably faulty.

To troubleshoot two channel analyzer failures

Use this test to isolate the failure when one channel fails in a two channel analyzer.

1 Check for failing self tests and calibration routine.

a Set the power switch to on (l).

b When the power-up tests are finished, press the following keys:
[**System Utility**]
[auto cal **off**]
[more cal setup]
[auto zero cal **off**]
[Return]
[more]
[diagnostics]
[service functions]
1125
[enter]
[test log]
[Return]
[functional tests]
[ADC]
(wait for test to finish)
[more]
[input]
(wait for test to finish)
[calibration]

c Do one of the following:

- If the self tests fail but do not lockup the analyzer, note the failure messages and go to Step 2.
- If the analyzer locks up on the calibration routine but not on the ADC or Input self test, note the failure messages and go to Step 2. Follow the procedure except do not press the [calibration] softkey.
- If the analyzer locks up on the ADC or Input self test, do Step 2 to see if exchanging assemblies will allow the self tests to run. If the analyzer still locks up on the ADC or Input self test after performing Step 2, go to page 1-71 and follow ''To troubleshoot input and ADC failures'' for each channel.
- If the self tests pass, determine the failure symptom before continuing with Step 2. For example, use the performance test procedures to

isolate the failure symptom. Once the exact failure symptom is known, do the following steps but substitute the failure symptom for the self tests.

2 Exchange the assemblies in channel 1 with the assemblies in channel 2, then check for failing tests.

a Set the power switch to off (O).

b Remove the top cover.

c Exchange the A21 A/D Converter assembly and A10 Analog Input assembly in channel 1 with the A21 A/D Converter assembly and A10 Analog Input assembly in channel 2.

d Reconnect the cables as follows:

Channel 1:	A10 J2 to A21 J4
	A10 J3 to A36 J2
	A21 J1 to A60 J3
Channel 2:	A10 J2 to A21 J4
	A10 J3 to A36 J5
	A21 J1 to A60 J2

e Set the power switch to on (l).

f Press the following keys:
[System Utility]
[auto cal **off**]
[more cal setup]
[auto zero cal **off**]
[Return]
[more]
[diagnostics]
[service functions]
1125
[enter]
[test log]
[Return]
[functional tests]
[ADC]
(wait for test to finish)
[more]
[input]
(wait for test to finish)
[calibration]

g If the channel that failed before the exchange still fails, go to Step 4.
The noise floor may appear higher than usual even if a channel is

operating correctly. This is caused by the ADC dither function. The noise floor should settle after about 3 minutes and should not affect the self-test results.

3 Step 3. Exchange channel 1 and channel 2 A/D Converter assemblies, then check for failing tests.

a Set the power switch to off (O).

b Exchange the channel 1 A21 A/D Converter assembly with the channel 2 A/D Converter assembly.

c Reconnect the cables as follows:

Channel 1:	A10 J2 to A21 J4
	A10 J3 to A36 J2
	A21 J1 to A60 J3
Channel 2:	A10 J2 to A21 J4
	A10 J3 to A36 J5
	A21 J1 to A60 J2

d Set the power switch to on (l).

e Press the following keys:
[System Utility]
[auto cal **off**]
[more cal setup]
[auto zero cal **off**]
[Return]
[more]
[diagnostics]
[service functions]
1125
[enter]
[test log]
[Return]
[functional tests]
[ADC]
(wait for test to finish)
[more]
[input]
(wait for test to finish)
[calibration]

f If the channel that failed before the exchange still fails, the A10 Analog Input assembly in the failing channel is probably faulty.

g If the other channel now fails, the A21 A/D Converter assembly in the failing channel is probably faulty.

4 Check the analog source to input paths.

a Press the following keys:
[**Preset**]
[Source]
[source **on**]
[level]
0
[dBm]
[**System Utility**]
[**more cal setup**]
[auto zero cal **off**]
[**Return**]
[more]
[diagnostics]
[service functions]
[special test modes]
[input]
[channel 1 source]

b Using a BNC(m)-to-SMB(f) cable, connect the oscilloscope to channel 1 A10 J2.
The oscilloscope should display a 130 ±13 mVp-p sine wave.

c Reconnect the cable from channel 1 A10 J2 to A21 J4.

d Press the following keys:
[channel 1 front BNC]
[channel 2 source]

e Using a BNC(m)-to-SMB(f) cable, connect the oscilloscope to channel 2 A10 J2.
The oscilloscope should display a 130 ±13 mVp-p sine wave.

f Reconnect the cable from channel 2 A10 J2 to A21 J4.

g If both signals are correct, go to Step 5.

h Place the analyzer on the side closest to the display.

i Remove the bottom cover.

j Set the oscilloscope as follows:

CH1 V/div	100 mV/div
Input Impedance	1 MΩ
CH1 Coupling	dc

Time/div	200 ns/div
Probe Atten	1

k Using a a high impedance 1:1 oscilloscope probe, check that A91 J6 pin 27B is a 423 ±42 mVp-p signal.

l Press the following keys:
[channel 2 front BNC]
[channel 1 source]

m Using a high impedance 1:1 oscilloscope probe, check that A91 J6 pin 29B is a 423 ±42 mVp-p signal.

n If either signal is incorrect, the A35 Analog Source assembly is probably faulty.

5 Check the frequency sample signals.

a Place the analyzer on the side closest to the display.

b Remove the bottom cover.

c Press [**Preset**].

d Using a logic probe, check that the TTL signals listed in the following table are toggling.

Test Location	Signal Name
A91 P6 pin 4	FSAAD
A91 P6 pin 11	FSA2
A91 P6 pin 16	FSA1

e If a signal is incorrect, the A60 Frequency Reference assembly is probably faulty.

f If all signals are correct, the A50 Digital Filter assembly is probably faulty.
This test does not check the A71 Pass Through assembly. The Pass Through assembly buffers the signals from the A21 A/D Converter assembly before they go to the A50 Digital Filter assembly. There is a separate set of buffers for each channel. The Pass Through assembly is less likely to fail than the A50 Digital Filter assembly.

To troubleshoot auto-range failures

Use this test when the auto-range function is suspected of failing and the following self tests passed:

- Input
- ADC

If the analyzer has the optional second channel, perform Step 1 for both channels.

1 Check over-range and half-range circuits.

a Using a BNC cable, connect the front panel SOURCE output to the failing input channel.

b Press the following keys:
[**Preset**]
[**Source**]
[source **on**]
[level]
0
[dBm]

The channel over-range LED should be off and half-range LED should be lit.

c Press the following keys:
10
[dBm]

The over-range and half-range LEDs should be lit.

d Press the following keys:
-10
[dBm]

The over-range and half-range LEDs should be off.

e If the LEDs responded correctly, the A30 Digital Source assembly is probably faulty.

2 Check the channel 1 auto-range signals.

a Place the analyzer on the side closest to the display.

b Remove the bottom cover.

c Press the following keys:
0
[dBm]
[**Marker/ Entry**]

d Using a BNC cable, connect the SOURCE output to CHANNEL 1 input.

e Using a logic probe, check the TTL signals listed in the following table. Rotate the RPG knob to change the source's amplitude to an under-range and over-range condition.

Test Location	Signal Name	Input Range Correct	Input Under Range (< -10 dBm)	Input Over Range (> + 6 dBm)	Probable Faulty Assembly
A91 P1 pin 47	nOVRRNG1	High	High	Low	A36 Trigger
A91 P1 pin 48	nHLFRNG1	Low	High	Low	A36 Trigger
A91 J2 pin 11B	nADCOVR1	High	High	Toggling	A21 A/ D Converter

f Press the following keys:
[**Range**]
[ch1 autorange up-down]
[**Source**]

g Rotate the RPG knob until the analyzer changes its range.
When the analyzer changes its range, the signals in the above table should toggle.

h If the analyzer does not have the optional second channel and the signals are correct, the A30 Digital Source assembly is probably faulty.

3 For analyzers with the optional second channel, check the channel 2 auto-range signals.

a Press the following keys:
[**Source**]
0
[dBm]

b Using a BNC cable, connect the SOURCE output to CHANNEL 2 input.

c Using a logic probe, check the TTL signals listed in the following table. Rotate the RPG knob to change the source's amplitude to an under-range and over-range condition.

Test Location	Signal Name	Input Range Correct	Input Under Range (<-10 dBm)	Input Over Range (>+6 dBm)	Probable Faulty Assembly
A91 P1 pin 49	nOVRRNG2	High	High	Low	A36 Trigger
A91 P1 pin 50	nHLFRNG2	Low	High	Low	A36 Trigger
A91 J1 pin 11B	nADCOVR2	High	High	Toggling	A21 A/ D Converter

d Press the following keys:
[**Range**]
[channel 2]
[ch2 autorange up-down]
[**Source**]

e Rotate the RPG knob until the analyzer changes its range. When the analyzer changes its range, the signals in the above table should toggle.

f If the signals are correct, the A30 Digital Source assembly is probably faulty.

To troubleshoot trigger failures

Use this test when the trigger function is suspected of failing and the following self tests passed:

- Digital Source
- Digital Filter
- ADC

1 Check the trigger calibration signal.

a Set the power switch to on (l).

b When the power-up tests are finished, press the following keys:
[Preset]
[**System Utility**]
[auto cal **off**]
[more cal setup]
[auto zero cal **off**]
[Return]
[more]
[diagnostics]
[service functions]
1125
[enter]
[special test modes]
[cal]
[cal signal **on**]

c Place the analyzer on the side closest to the display.

d Remove the bottom cover.

e Set the oscilloscope as follows:

CH1 V/div	200 mV/div
Input Impedance	1 MΩ
CH1 Coupling	dc
Time/div	500 ns/div
Probe Atten	1

f Using a high impedance 1:1 oscilloscope probe, check that A91 J6 pin 25B is a 1±0.1 Vp-p square wave.

g If the signal is incorrect, the A35 Analog Source assembly is probably faulty.

h Return the analyzer to its normal position.

2 Check trigger modes.

a Press the following keys:
[Preset]
[System Utility]
[more cal setup]
[auto zero **off**]
[Return]
[Range]
4
[dBm]
[Source]
[source **on**]
[source type]
[periodic chirp]
[Return]
[level]
0
[dBm]
[Frequency]
[time data **zoom**]
If the analyzer has two channels, press **[Range]** [channel **both**], then [ch* range] 4 [dBm].

b Connect the SOURCE output to the front panel CHANNEL 1 input and EXT TRIGGER connectors using a BNC tee and BNC cables.

c Press the following keys while monitoring the display. Note which trigger types are functioning:
[Trigger]
[trigger type]
[IF channel 1]
[internal source]
[external]
[channel 1]
[**Return**]
[chan level]
200
[mV]
[chan slope]
[–]
[+]
The message ''WAITING FOR TRIGGER'' is displayed when the analyzer is not triggering.

d If the analyzer has the optional second channel, move the source output to the front panel CHANNEL 2 input and press the

following keys while monitoring the display. Note which trigger types are functioning:
[Trigger]
[trigger type]
[IF channel 2]
[channel 2]
[Return]
[chan level]
0
[V]
[slope]
[–]
[+]

e Compare the trigger failure to the failures listed in the following table.

Trigger Mode Failing (only one of the following categories)	Probable Faulty Assembly or Next Step
External Trigger	A36 Trigger
Trigger Slope	A36 Trigger
Trigger Level	A36 Trigger
IF channel 1 and/ or IF channel 2	A50 Digital Filter
Internal source	A30 Digital Source
Channel 1 Trigger and Channel 2 Trigger	A36 Trigger
Channel 1 Trigger or Channel 2 Trigger	Step 3

f If the failure has not been isolated, continue troubleshooting with Step 3.

3 Check channel trigger circuits.

a Set synthesizer as follows:
Frequency 1 MHz
Amplitude 724 mVp-p
Function Sine Wave

b Using a BNC(m)-to-SMB(f) cable, connect the synthesizer to A36 J2 to check channel 1 trigger or A36 J5 to check channel 2 trigger.

c Press the following keys:
[**Trigger**]
[trigger type]
[channel 1] or [channel 2]
[Return]
[chan level]
0
[V]

d If the analyzer now triggers, the A10 Analog Input assembly is probably faulty.

e If the analyzer does not trigger and channel trigger is the only function failing, the A36 Trigger is probably faulty.

f Reconnect channel 1 A10 J3 to A36 J2 and channel 2 A10 J3 to A36 J5.

4 Check trigger control lines.

a Place the analyzer on the side closest to the display.

b Set the synthesizer to 2 Vp-p and connect to the front panel CHANNEL 1 input using a BNC cable.

c Press the following keys:
[**Range**]
1
[V]
[**Trigger**]
[trigger type]
[channel 1]

d For each TTL signal listed in the following table, check that the signal is toggling using a logic probe.

Test Location	Signal Name	Probable Faulty Assembly
A91 P6 pin 10	CLK25M	A60 Frequency Reference
A91 P6 pin 11	FSA2	A60 Frequency Reference
A91 P6 pin 16	FSA1	A60 Frequency Reference
A91 P1 pin 16	GTCLK	A36 Trigger
A91 P1 pin 22	PTA	A55/ A56 Sample RAM
A91 P1 pin 23	TPSD	A36 Trigger
A91 P1 pin 26	nSTRIGa	A36 Trigger

e If the signals in the table are correct, the A36 Trigger is probably faulty.

To troubleshoot disk drive failures

Use this test to isolate disk drive failures to the A42 Memory assembly, the A101 Disk Drive assembly, or the flexible disk.

1 Check disk controller.

   a Press the following keys:
   [**System Utility**]
   [more]
   [diagnostics]
   [service functions]
   1125
   [enter]
   [functional tests]
   [I/ O]
   [disk controller]

   b If the disk controller test aborts and displays the message ''Mass Storage Unit not Present!!,'' the fuse on the Memory assembly, Disk Drive assembly or disk drive cable is probably faulty. Go to Step 2 to check the memory fuse.

   c If the disk controller test fails, the A42 Memory assembly is probably faulty.

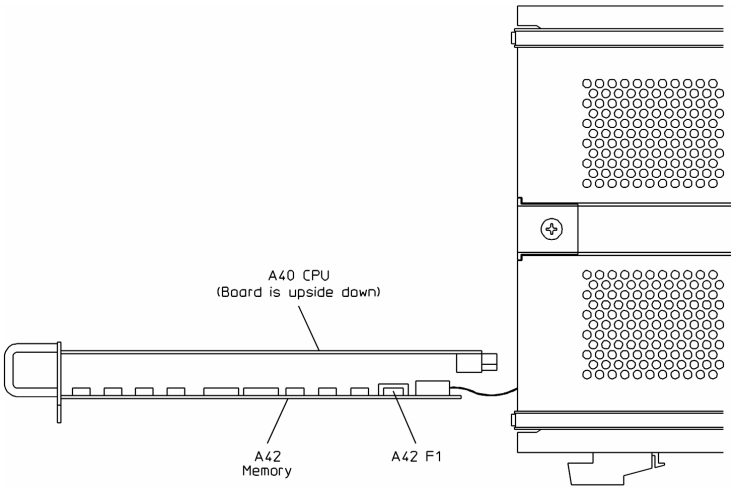
   d If the disk controller test passes, go to Step 3.

2 Check fuse on the A42 Memory assembly.

   a Set the power switch to off (O).

   b Remove the screws on each side of cover number 6.

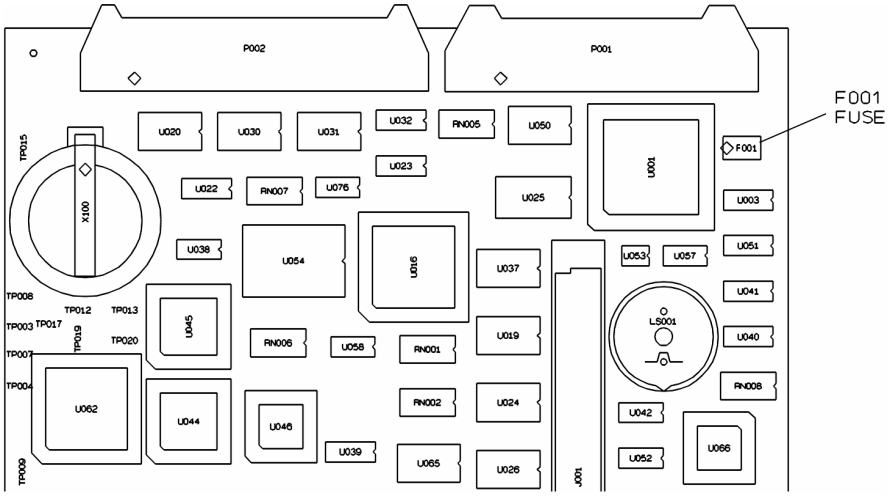
   c Pull out the assemblies attached to cover number 6 until the edge of the assemblies clear the rear panel.



d Measure the resistance across F1.

e If the resistance is 0 Ω, the Disk Drive assembly or the disk drive cable is probably faulty.

f If the resistance was greater than 0 Ω, replace the fuse.



3 Check the Disk Drive assembly.

a Insert a formatted disk into the Disk Drive assembly and press the following keys:
[**Return**]
[**Return**]
[test log]
[clear test log]
[**Return**]
[special test modes]
[I/ O]
[disk drive]
[restore]
[random seek]
[seek record]
Any number between 1 and 2771
[read]
[read/ write]

b If any of the self tests failed, insert a new formatted disk and repeat the previous step.
If the self-test message reads ''Bad or unformatted media,'' the flexible disk is most likely bad or unformatted. The analyzer can use either LIF (Logical Interchange Format) or a DOS formatted disk.

c If the disk drive self tests still fail, the Disk Drive assembly is probably faulty.

d Press the [read/ write all] key.
The read/write self test can take up to 40 minutes to complete if there are no failures.

e If the self-test message reads ''Bad or unformatted media,'' change flexible disk and repeat the read/write all self-test.

f If the self test fails a second time, the Disk Drive assembly is probably faulty.
If the self tests pass, the Disk Drive assembly and flexible disk are functioning correctly.

To troubleshoot serial port failures

Use this test to check the serial 1 and serial 2 ports on the A42 Memory assembly.

1 Check the serial port controller.

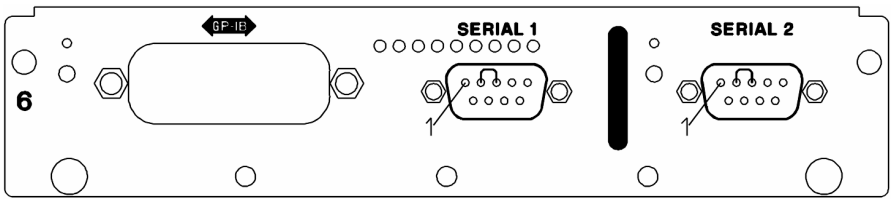
a Press the following keys:
[**System Utility**]
[more]
[diagnostics]
[service functions]
1125
[enter]
[functional tests]
[I/O]
[serial port controller]

b If the serial port test fails, the A42 Memory assembly is probably faulty.

2 Check the serial 1 and serial 2 ports.

a Connect SERIAL 1 pin 2 to pin 3.

b Connect SERIAL 2 pin 2 to pin 3.



c Press the following keys:
[**Return**]
[**Return**]
[special test modes]
[I/O]
[serial port loop back]

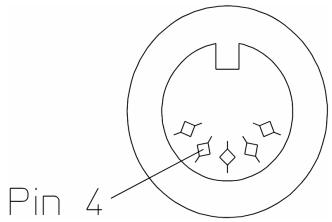
d If the self test fails, the A42 Memory assembly is probably faulty. If the self test passes, the serial ports are probably operating correctly.

To troubleshoot DIN connector failures

Use this test to determine if the fuse for the DIN connector is failing before replacing the A80 Keyboard assembly.

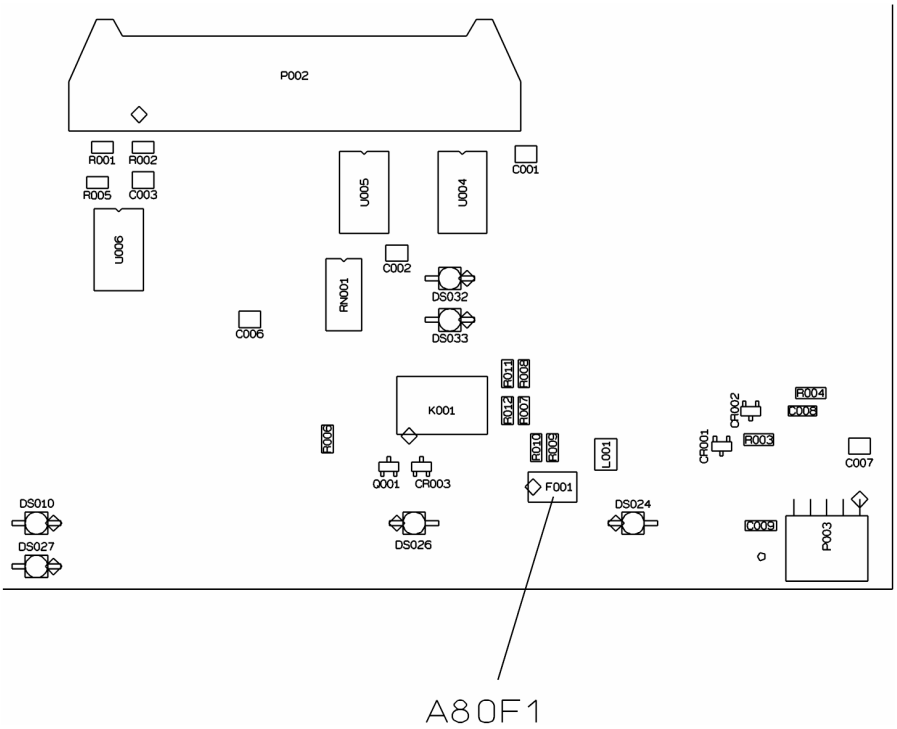
1 Set the power switch to on (l).

2 Check the voltage on pin 4 of the KEYBOARD connector for +5V.



3 If the voltage is correct, the Keyboard assembly is probably faulty.

4 If the voltage is not correct, replace the A80 F1 fuse.



To troubleshoot memory battery failures

Use this test when battery-backed-up memory is suspected of failing. This test separates A42 Memory assembly failures from memory battery failures.

1 Check battery-backed-up memory.

   a Set the power switch to on (l).

   b Press the following keys:
   [**System Utility**]
   [more]
   [time/ date setup]
   [date]
   010193
   [enter]

   c Set the power switch to off (O), then to on (l).

   d Press the following keys:
   [**System Utility**]
   [more]
   [time/ date setup]

   e If the date is 01-01-93, the battery-backed-up memory is probably functioning correctly. Go to page 1-32, ''To perform self tests,'' to continue troubleshooting.

2 Check the battery voltage.

   a Set the power switch to off (O).

   b Remove the screws on each side and across the bottom of cover number 6.

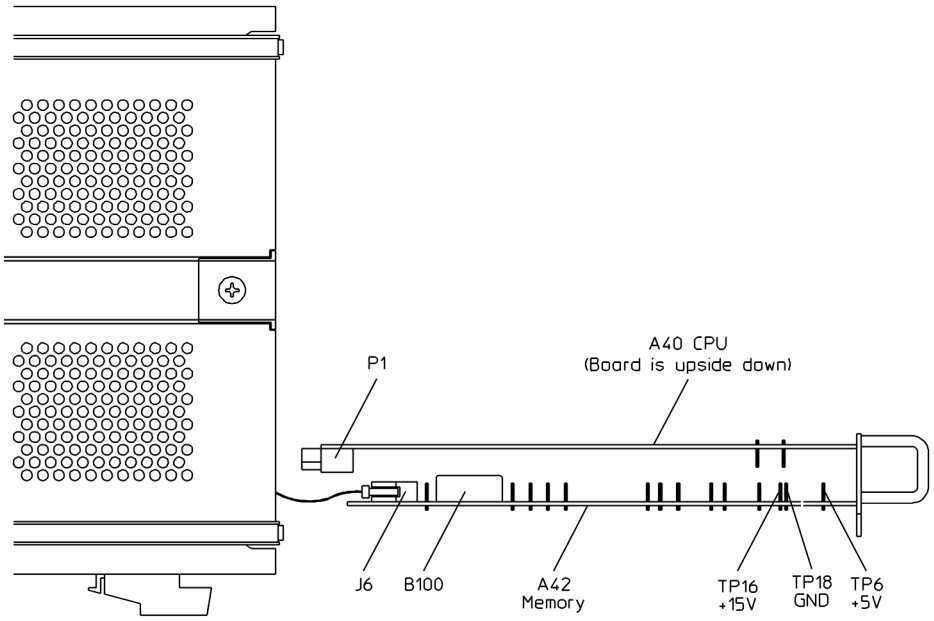
   c Pull out the assemblies attached to cover number 6 until the battery on the Memory assembly is visible.

   d Measure the voltage between the top of the battery and A42 TP18.

   e If the voltage is 3 ±1 V, the A42 Memory assembly is probably faulty.

   f If the voltage is incorrect, replace the battery (A42 B100).

CAUTION: There is danger of explosion if battery is incorrectly replaced. Replace the battery with the same or an equivalent type listed in Chapter 4, "Replaceable Parts", Discard used batteries according to the battery manufacturer's instructions.



To troubleshoot sync out and parallel port failures

Use this test to determine if the fuses for the parallel port and sync out are failing before replacing the A30 Digital Source assembly. The sync out fuse will fail if an input signal (≥-20 V) is connected to this output.

1 Set the power switch to off (O).

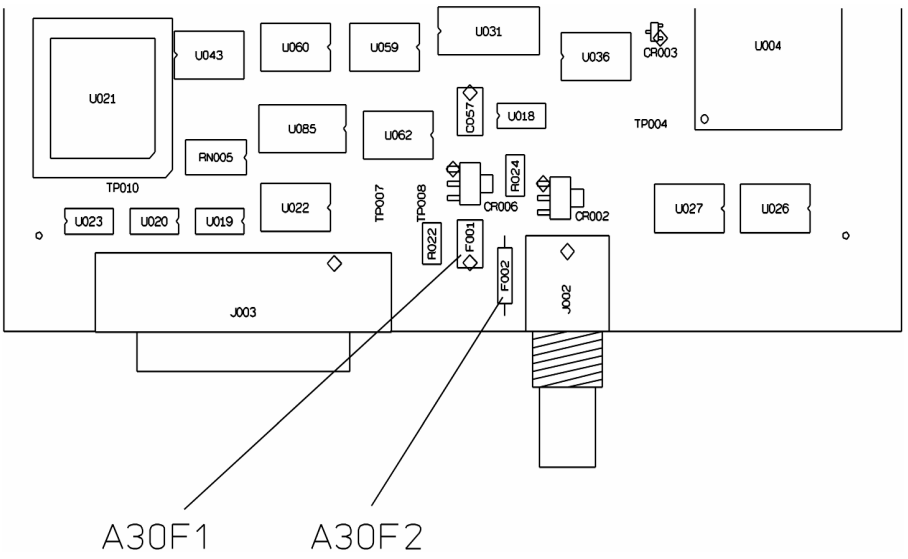
2 Remove the screws on each side of cover number 4.

3 Remove the A30 Digital Source assembly attached to cover number 4.

4 Using a multimeter, measure the resistance across F1 and across F2. The A30 F1 fuse is for sync out and the A30 F2 fuse is for the parallel port.

5 If the resistance of both fuses is 0Ω, the A30 Digital Source is probably faulty.

6 If the resistance of a fuse did not measure 0Ω, replace the fuse.



To troubleshoot system interconnect and LAN port failures

Use this test to check the system interconnect, ThinLAN, and AUI ports on the A43 Expanded Memory assembly.

1 Check the HPIB interconnect and LAN controller.

a Press the following keys:
[**Preset**]
[**System Utility**]
[auto cal **off**]
[more cal setup]
[auto zero cal **off**]
[**Return**]
[more]
[diagnostics]
[service functions]
1125
[enter]
[test log]
[**Return**]
[functional tests]
[I/ O]
[ALL]
If the analyzer is an Agilent 89440A/89441A, the message Failure of communication link with RF section may appear. This is not a failure and should be ignored.

b If the HPIB interconnect or LAN controller self tests fail, the A43 Expanded Memory assembly is probably faulty.

c If any other self test fails, go to Step 4 of ''To perform self tests'' on page 1-32.

2 Check the ThinLAN port.

a Connect a BNC tee to the ThinLAN port.

b Connect a 50Ω termination to each side of the BNC tee (use two 50 Ω terminations.)

c Press the following keys:
[**Return**]
[**Return**]
[special test modes]

[I/ O]
[ThinLAN loop back]

d If the ThinLAN loop back test fails, the A43 Expanded Memory assembly is probably faulty.

3 Check the AUI LAN port.

a Connect a ThinLAN Transceiver (AUI to ThinLAN converter) to the AUI LAN port.

b Set the switches on the ThinLAN Transceiver to their disable position.

c Connect a BNC tee to the transceiver's BNC connector.

d Connect a 50 Ω termination to each side of the BNC tee (use two 50 Ω terminations.)

e Press the [AUI LAN loop back] softkey.

f If the AUI LAN loop back test fails, the A43 Expanded Memory assembly is probably faulty.

g If the self tests pass, the LAN ports are probably operating correctly.

h Set the power switch off (O), then on (l) to return the analyzer to normal LAN operation.

2 Adjusting the Analyzer

Adjusting the Analyzer

This chapter contains the adjustment procedures for the Agilent 89410A DC-10 MHz Vector Signal Analyzer. Follow these procedures if the analyzer does not meet its specifications or if instructed in chapter 1,Troubleshooting the Analyzer or chapter 3, Replacing Assemblies to perform these adjustments. These adjustments are not required for routine maintenance.

Analyzers with the precision frequency reference (option AY5) must be off for at least 8 hours before doing the oven shutdown adjustment and must warm up for at least 48 hours before doing the oven frequency adjustment.

Before starting the input flatness adjustment, allow the Agilent 89410A Vector Signal Analyzer to warm up for at least an hour. If the analyzer has the optional second channel (option AY7), perform the input adjustments for channel 1 and repeat for channel 2.

The following table shows the assembly and components adjusted during each adjustment procedure. If the channel 1 A10 Analog Input or A35 Analog Source adjustments are done, the calibrator adjustment must also be done.

Adjustment	Assembly	Component
Oven shutdown	A85 Oven	R2
Input flatness	A10 Analog Input	C122, C143
Input capacitance	A10 Analog Input	C123
Input offset	A10 Analog Input	R61
Anti-alias filter	A10 Analog Input	L38, L39, L40, L41
ADC	A21 A/ D Converter	software
10 MHz low pass filter	A35 Analog Source	L3, L4
Autorange detect level	A36 Trigger	R113, R114
Reference oscillator	A60 Frequency Reference	C55, R66
Clock	A61 Clock	R12, C21
Display	A100 Display	
Oven frequency	A85 Oven	HR1, R12
Calibrator	A35 Analog Source	software

The fault log should be cleared after an adjustment that required cables to be disconnected. To clear the fault log press the following keys:
[**System Utility**]
[more]
[diagnostics]
[service functions]
1125
[enter]
[fault log]
[clear fault log]

Safety Considerations

Although the Agilent 89410A analyzer is designed in accordance with international safety standards, this guide contains information, cautions, and warnings that must be followed to ensure safe operation and to keep the unit in safe condition. Adjustments in this chapter are performed with power applied and protective covers removed. These adjustments must be performed by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

WARNING: **Any interruption of the protective (grounding) conductor inside or outside the unit, or disconnection of the protective earth terminal can expose operators to potentially dangerous voltages.**
Under no circumstances should an operator remove any covers, screws, shields or in any other way access the interior of the Agilent 89410A analyzer. There are no operator controls inside the analyzer.

Equipment Required

See chapter 1, Troubleshooting the Analyzer for tables listing recommended test equipment. Any equipment which meets the critical specifications given in the tables may be substituted for the recommended model.

Remote Operation

Adjustments can be setup using the remote operation capability of the Agilent 89410A analyzer. The following table lists the adjustments and corresponding HPIB codes. See the *Agilent 89400 Series HPIB Command Reference* for general information on remote operation.

Adjustment	HPIB Code
Channel 1 Input flatness setup 1	DIAG:ADJ:INP1:FLAT 1
Channel 1 Input flatness setup 2	DIAG:ADJ:INP1:FLAT 2
Channel 1 Input flatness setup 3	DIAG:ADJ:INP1:FLAT 3
Channel 2 Input flatness setup 1	DIAG:ADJ:INP2:FLAT 1
Channel 2 Input flatness setup 2	DIAG:ADJ:INP2:FLAT 2
Channel 2 Input flatness setup 3	DIAG:ADJ:INP2:FLAT 3
Channel 1 Input capacitance setup 1	DIAG:ADJ:INP1:CAP 1
Channel 1 Input capacitance setup 2	DIAG:ADJ:INP1:CAP 2
Channel 2 Input capacitance setup 1	DIAG:ADJ:INP2:CAP 1
Channel 2 Input capacitance setup 2	DIAG:ADJ:INP2:CAP 2
Channel 1 Input offset	DIAG:ADJ:INP1:FET 1
Channel 2 Input offset	DIAG:ADJ:INP2:FET 1
Channel 1 Anti-alias filter setup 1	DIAG:ADJ:INP1:AAF 1
Channel 1 Anti-alias filter setup 2	DIAG:ADJ:INP1:AAF 2
Channel 1 Anti-alias filter setup 3	DIAG:ADJ:INP1:AAF 3
Channel 2 Anti-alias filter setup 1	DIAG:ADJ:INP2:AAF 1
Channel 2 Anti-alias filter setup 2	DIAG:ADJ:INP2:AAF 2
Channel 2 Anti-alias filter setup 3	DIAG:ADJ:INP2:AAF 3
ADC	DIAG:ADJ:ADC:SDIT
10 MHz low pass filter setup 1	DIAG:ADJ:SOUR 1
10 MHz low pass filter setup 2	DIAG:ADJ:SOUR 2
Autorange detect level	DIAG:MODE:TRIG:LEV 128
Display brightness	DISP:BRIG 100 PCT

To adjust oven shutdown

This procedure adjusts the optional A85 Oven assembly's heater shutdown trip point. When the oven is cold, the heater shutdown circuit disconnects the oven output from the rear panel output connector. After the oven has been on long enough for the frequency to be stable, the heater shutdown circuit connects the oven output to the rear panel output connector.

The Agilent 89410A Vector Signal Analyzer must be off for at least 8 hours before this adjustment is made. Once power is applied, the adjustment **MUST** be completed within **FIVE MINUTES**.

Equipment Required:

Spectrum analyzer
BNC cable
Flat-edge adjustment tool,
Agilent part number 8710-1928

WARNING: This procedure is performed with protective covers removed and power applied. Energy available at may points can, if contacted, result in personal injury.

Even with power removed, there can be sufficient stored energy in some circuits to cause personal injury. These voltages will discharge to a relatively safe level approximately five minutes after the power cord is disconnected.

---

1 Remove the power supply shield.

   a Check that the power switch is off (O).
   The Agilent 89410A must be off for at least 8 hours before doing this adjustment.

   b Remove the power supply shield. The power supply shield is located behind the display.

2 Set up the spectrum analyzer.

a Set the spectrum analyzer as follows:

Center Frequency	**10 M Hz**
Frequency Span	**1 M Hz**
Reference Level	**–60 dBm**

b Connect the spectrum analyzer to the Agilent 89410A's OVEN REF OUT connector using the BNC cable.

3 Check that the 10 MHz signal is ≤-70 dBm.

a Set the power switch to on (l).

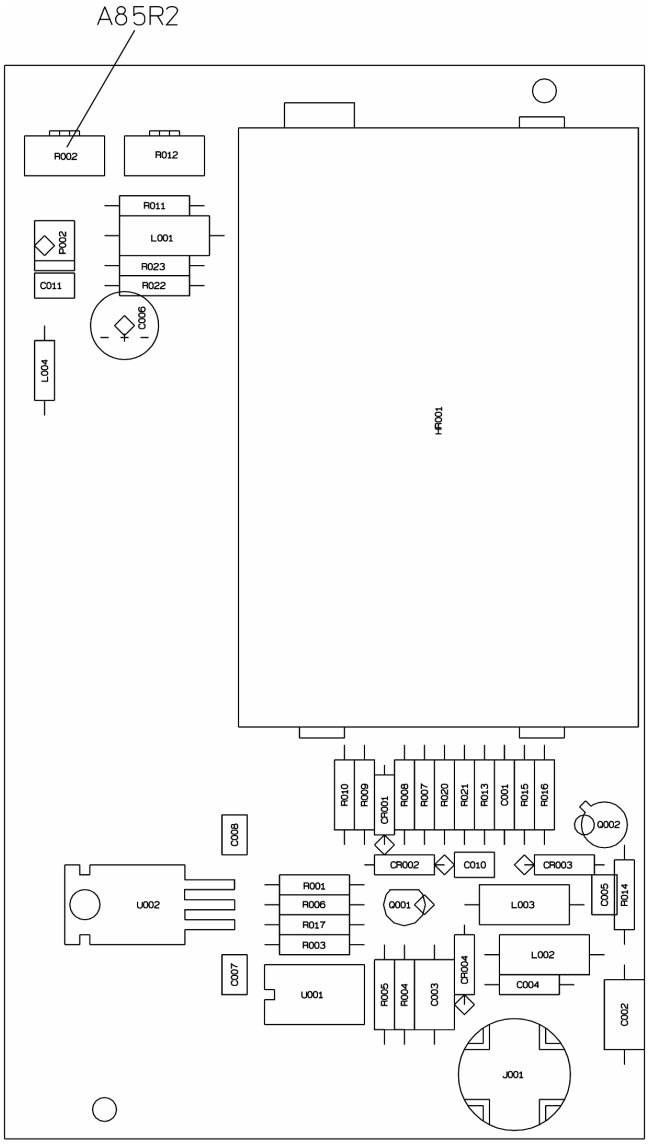
b Check that the amplitude of the 10 MHz signal is ≤-70 dBm (oven is cold).

4 Adjust A85 R2.

a Change the spectrum analyzer's reference level to 10 dBm.

b Turn A85 R2 counterclockwise until the 10 MHz signal's amplitude is > 0 dBm.

c Turn A85 R2 clockwise until the signal's amplitude just returns to approximately -70 dBm, then turn R2 an additional 10 degrees clockwise.



5 Replace the power supply shield.

a Set the power switch to off (O).

b Replace the power supply shield.
To continue the oven adjustments, allow the Agilent 89410A to warm up for at least 48 hours then do the oven frequency adjustment on page 2-34.

To adjust input flatness

This procedure adjusts the A10 Analog Input assembly's first and second 20 dB attenuators to improve input assembly flatness.

Equipment Required:

Network analyzer
Extender board, Agilent part number 89410-B1001
BNC cable
SMB(f)-to-BNC(m) cable
(2) N(m)-to-BNC(f) adapters
Flat-edge adjustment tool, Agilent part number 8710-1928

1 Place the A10 Analog Input assembly on an extender board.

   c Set the power switch to off (O).

   d Remove screws holding the A10 Analog Input assembly in the card nest.

   e Place the assembly on an extender board.

   f Set the power switch to on (l).

2 Set up the Agilent 89410A.

   a Press the following keys:
   [**System Utility**]
   [more]
   [diagnostics]
   [service functions]
   1125
   [enter]
   [adjustments]
   [channel 1 input] or [channel 2 input]
   [pad flatness]
   [setup 1]

3 Set up the network analyzer.

a Set the network analyzer as follows:

Receiver	**reference channel**
Attenuation	**20 dB**
Resolution BW	**1 kHz**
Source	
Sweep Mode	**continuous**
Sweep Time	**1 s**
Sweep Type	**log frequency**
Amplitude	**-22 dBm**
Start Frequency	**10 kHz**
Stop Frequency	**1 MHz**
Display format	**log magnitude**

b Connect the network analyzer's reference channel to A10 J2 using an N(m)-to-BNC(f) adapter and SMB(f)-to-BNC(m) cable.

c Connect the network analyzer's source to the Agilent 89410A's input using an N(m)-to-BNC(f) adapter and BNC cable.

4 Normalize the measurement.

a Wait for a complete sweep on the network analyzer.

b Store the trace data in a storage register.

c Set the network analyzer to divide the reference channel by the storage register.

5 Adjust A10 C122.

a Press the [setup 2] softkey.

b Set the network analyzer's reference level to the value at 10 kHz.

c Center the trace on the network analyzer's display, then set the scale to 0.1 dB/div.

d Adjust C122 for a flat trace using the flat-edge adjustment tool.

6 Normalize the measurement.

a Press the [setup 1] softkey.

b Set the network analyzer's input to the reference channel.

c Wait for a complete sweep on the network analyzer.

d Store the trace data in a storage register.

e Set the network analyzer to divide the reference channel by the storage register.

7 Adjust A10 C143.

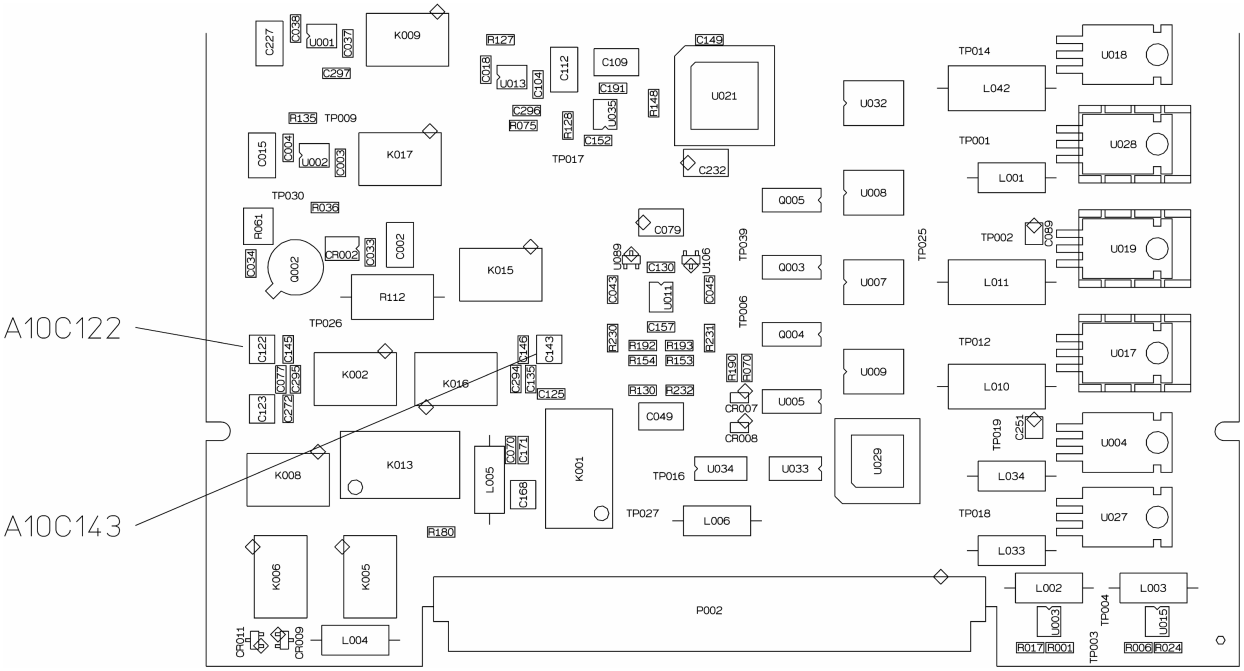
a Press the [setup 3] softkey.

b Set the network analyzer's reference level to the value at 10 kHz.

c Center the trace on the network analyzer's display, then set the scale to 0.1 dB/div.

d Adjust C143 for a flat trace using the flat-edge adjustment tool.

To continue the input adjustments, go to the next adjustment.



To adjust input capacitance

This procedure adjusts the A10 Analog Input assembly's input capacitance for a constant value over all input ranges and attenuator settings.

Perform the previous adjustment before doing this adjustment.

Equipment Required:

Network analyzer
Extender board, Agilent part number 89410-B1001
BNC cable
SMB(f)-to-BNC(m) cable
50 Ω feedthrough termination
10 kΩ series resistor
(2) N(m)-to-BNC(f) adapters
Flat-edge adjustment tool, Agilent part number 8710-1928

1 Set up the Agilent 89410A.

   a Disconnect the network analyzer's source and receiver from the Agilent 89410A.

   b Press the following keys:
   [**Return**]
   [input capacitance]
   [setup 1]

2 Step 2. Set up the network analyzer.

a Set the network analyzer as follows:

Receiver	**reference channel**
Attenuation	**20 dB**
Resolution BW	**1 kHz**
Source	
Sweep Type	**linear frequency sweep**
Sweep Mode	**continuous**
Sweep Time	**1 s**
Amplitude	**-22 dBm**
Start Frequency	**10 kHz**
Stop Frequency	**1 MHz**
Display format	**log magnitude**

b Connect the network analyzer's reference channel to A10 J2 using an N(m)-to-BNC(f) adapter and SMB(f)-to-BNC(m) cable.

c Connect a 10 kΩ series resistor to the Agilent 89410A's input.

d Connect a 50 Ω feedthrough termination to the 10 kW series resistor.

e Connect the network analyzer's source to the 50Ω feedthrough termination using an N(m)-to-BNC(f) adapter and a BNC cable.

3 Normalize the measurement.

a Wait for a complete sweep on the network analyzer.

b Store the trace data in a storage register.

c Set the network analyzer to divide the reference channel by the storage register.

4 Adjust A10 C123.

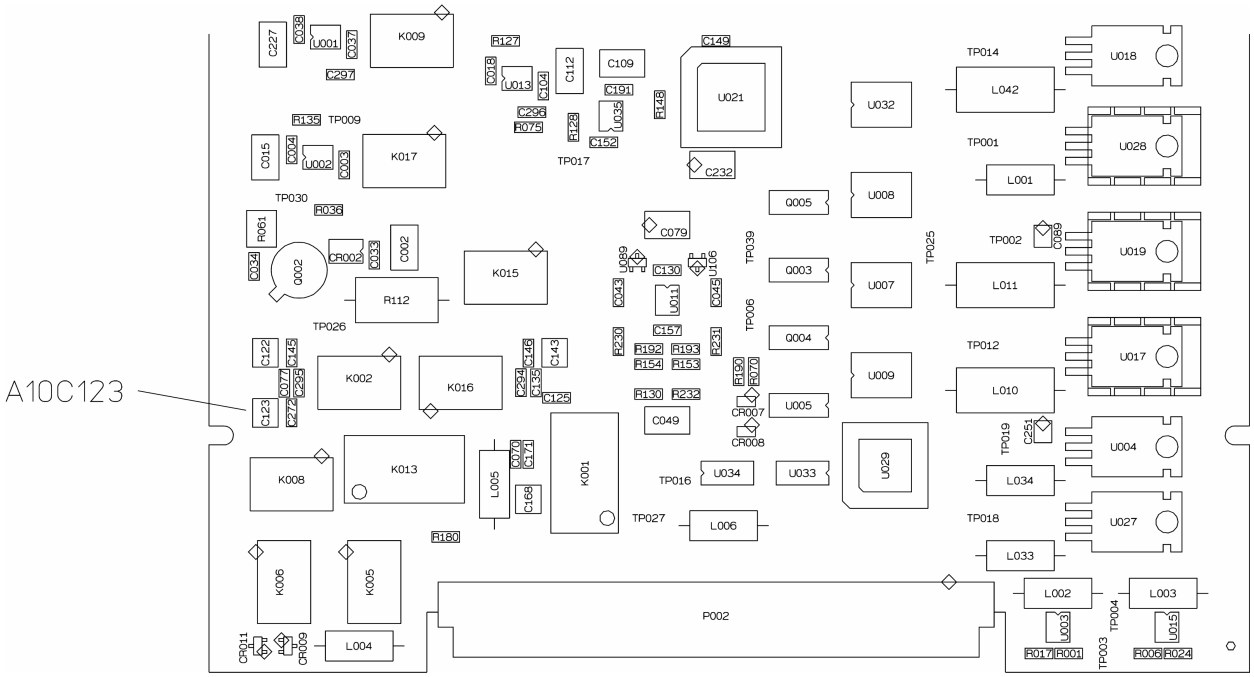
a Press the [setup 2] softkey.

b Set the network analyzer's reference level to the value at 10 kHz.

c Center the trace on the network analyzer's display, then set the scale to 0.5 dB/div.

d Adjust C123 for a flat trace using the flat-edge adjustment tool.

To continue the input adjustments, go to the next adjustment.



To adjust input offset

This procedure adjusts the A10 Analog Input assembly's offset voltage to zero volts.

Perform the previous adjustment before doing this adjustment.

Equipment Required:

Digital multimeter
Extender board, Agilent part number 89410-B1001
50Ω termination
Flat-edge adjustment tool, Agilent part number 8710-1928

1 Remove all external connections.

2 Connect a 50Ω termination to the input.

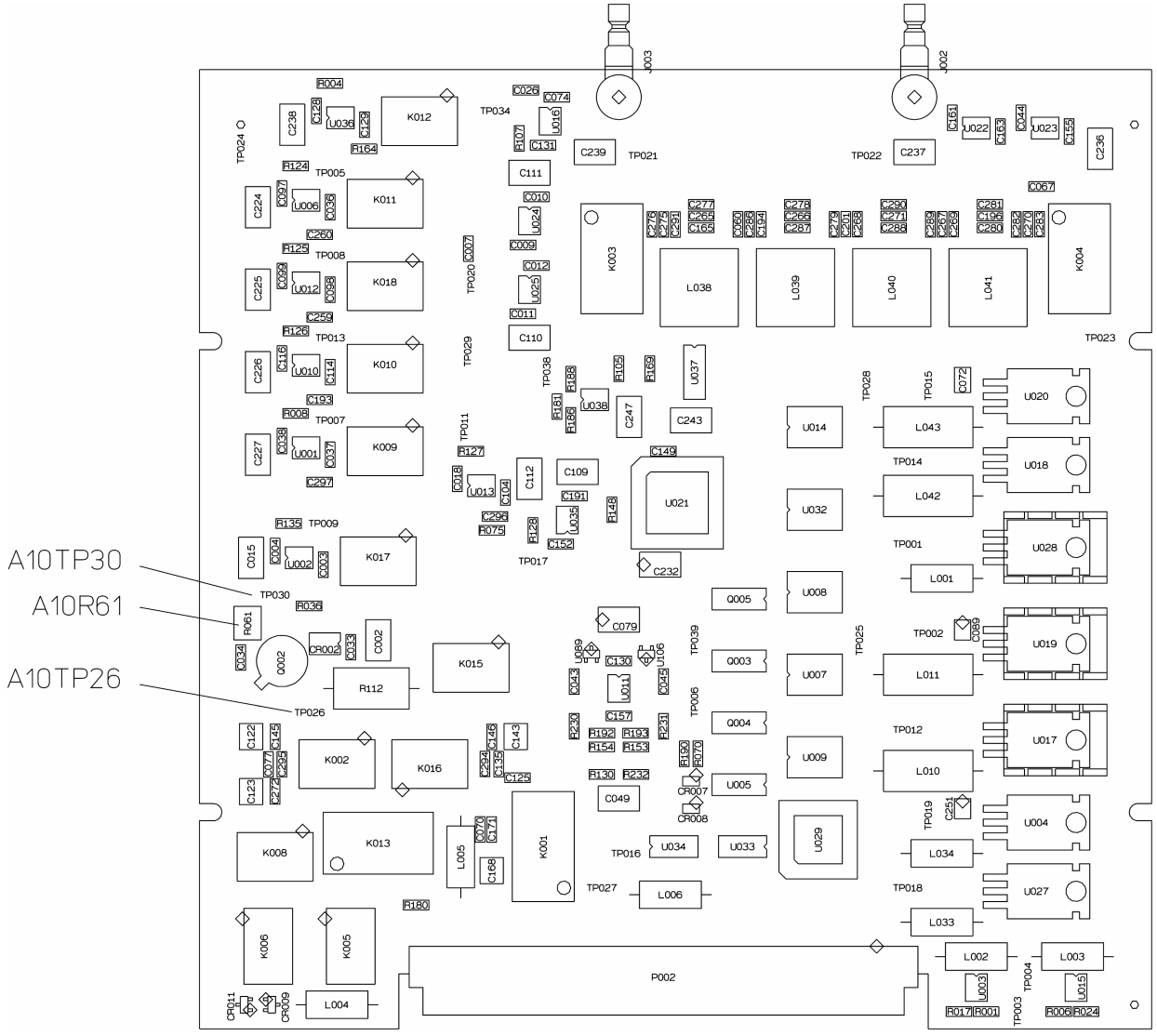
3 Press the following keys:
[**Return**]
[FET offset]
[setup 1]

4 Set the multimeter to Vdc.

5 Connect the multimeter to A10 TP30 and A10 TP26 (gnd) using test leads.

6 Adjust A10 R61 for a multimeter reading of 0 ±100 mV using the flat-edge adjustment tool.

To continue the input adjustments, go to the next adjustment.



To adjust anti-alias filter

This procedure adjusts the corner frequency, pass band ripple, and band stop rejection of the A10 Analog Input assembly's anti-alias filter.

Perform the previous adjustment before doing this adjustment.

Equipment Required:

Network analyzer
Extender board, Agilent part number 89410-B1001
BNC cable
SMB(f)-to-BNC(m) cable
(2) N(m)-to-BNC(f) adapters
Flat-edge adjustment tool, Agilent part number 8710-1928

1 Set up the Agilent 89410A.

   a Remove all external connections from the Agilent 89410A.

   b Press the following keys:
   [**Return**]
   [anti-alias filter]
   [setup 1]

2 Set up the network analyzer.

   a Set the network analyzer as follows:

Receiver	**reference channel**
Attenuation	**0 dB**
Resolution BW	**10 Hz**
Source	
Sweep Mode	**manual**
Manual Frequency	**15.4 MHz**
Amplitude	**-13 dBm**
Display format	**log magnitude**

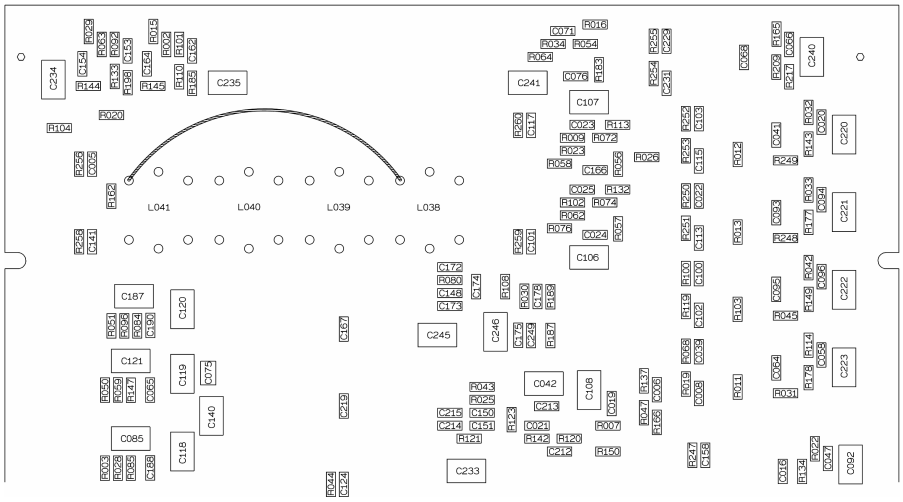
   b Connect the network analyzer's reference channel to A10 J2 using an N(m)-to-BNC(f) adapter and SMB(f)-to-BNC(m) cable.

   c Connect the network analyzer's source to the Agilent 89410A's input using an N(m)-to-BNC(f) adapter and BNC cable.

3 Adjust L38.

a Attach a jumper to the pins shown in the following illustration.

A10 Analog Input Component Locator, Back View

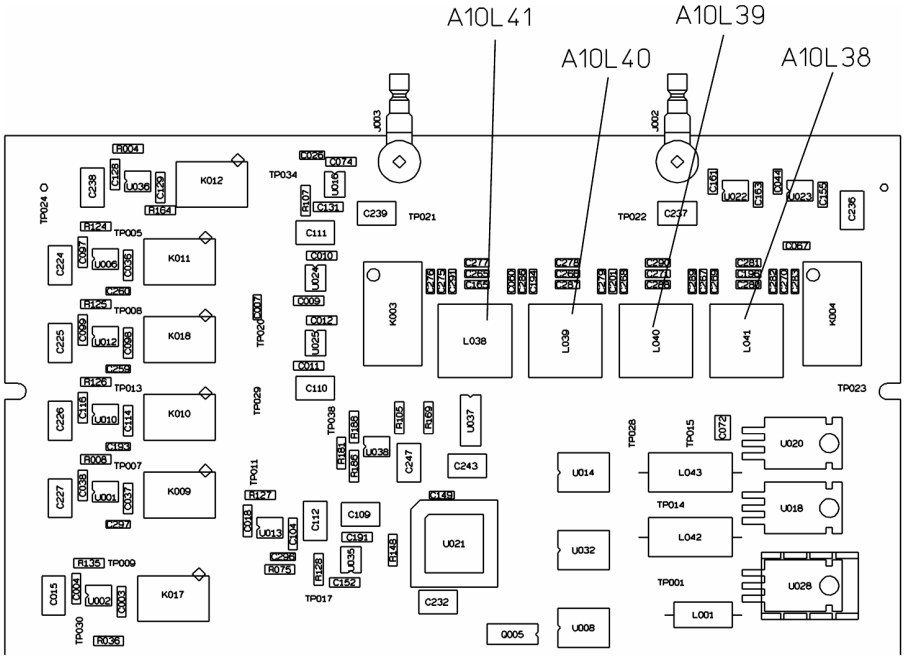


b Adjust the network analyzer's reference level so the signal is visible.

c Adjust L38 for a minimum marker reading using the flat-edge adjustment tool.

d Remove the jumper.

A10 Analog Input Component Locator, Front View



4 Normalize the measurement.

a Press the [setup 2] softkey.

b Set the network analyzer as follows:

Receiver	**reference channel**
Attenuation	**0 dB**
Resolution BW	**1 kHz**
Source	
Sweep Mode	**continuous**
Sweep Type	**linear frequency sweep**
Sweep Time	**1 s**
Amplitude	**-13 dBm**
Start Frequency	**100 kHz**
Stop Frequency	**20.1 M Hz**
Display format	**log magnitude**

c Wait for a complete sweep on the network analyzer.

d Store the trace data in a storage register.

e Set the network analyzer to divide the reference channel by the storage register.

5 Adjust A10 L39, L40, and L41.

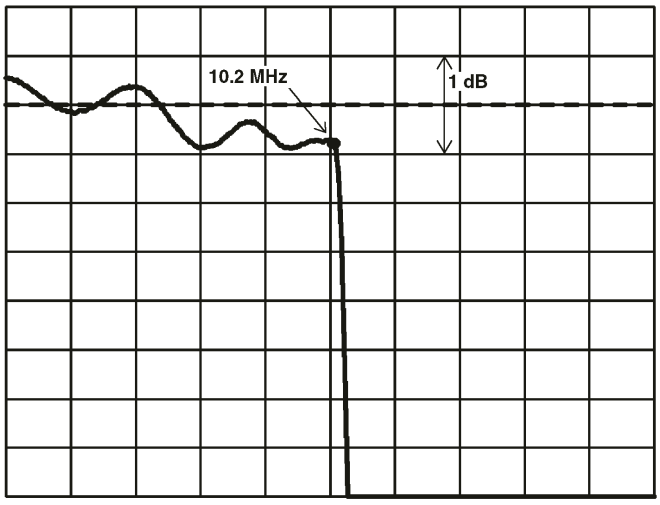
a Press the [setup 3] softkey.

b Set the network analyzer's reference level 0 dB.

c Set the reference position at 80% of the display and the scale to 0.5 dB/div.

d Put the marker at 10.2 MHz.

e Adjust A10 L39, L40, and L41 for less than 1 dB ripple from 100 kHz to 10.2 MHz using the flat-edge adjustment tool. L39, L40, L41 Correctly Adjusted



6 Normalize the measurement.

a Press the [setup 2] softkey.

b Change the network analyzer to the following:

Receiver	**reference channel**
Resolution BW	**10 Hz**
Source	
Sweep Time	**40 s**
Start Frequency	**15.6 MHz**
Stop Frequency	**54 MHz**

c Wait for a complete sweep on the network analyzer.

d Store the trace data in a storage register.

e Set the network analyzer to divide the reference channel by the storage register.

7 Check that there is at least 90 dB of rejection from 15.6 MHz to 54 MHz.

a Press the [setup 3] softkey.

b Set the network analyzer's reference level to 0 dB.

c Set the scale to 10 dB/div.

d Set the reference position to 100%.

e Wait for a complete sweep on the network analyzer.

f Check that there is at least 90 dB of rejection from 15.6 MHz to 54 MHz.
If there is not 90 dB of rejection between 15.6 MHz and 54 MHz, repeat the anti-alias filter adjustments starting at **Step 1**.

8 Reinstall the A10 Analog Input assembly.

a Set the power switch to off (O).

b Place the assembly in the card nest.

c Reconnect the following using original cables:
A10 J2 to A21 J4 (red cable)
A10 J3 to A36 J2 (channel 1, orange cable)
A10 J3 to A36 J5 (channel 2, orange cable)

If only the input assembly adjustments are being done, go to Chapter 2, "To adjust calibrator"to adjust the calibrator. The calibrator adjustment

must be done after the channel 1 A10 Analog Input assembly or the A35 Analog Source assembly is adjusted.

This completes the A10 Analog Input assembly adjustments.

To adjust ADC

This procedure adjusts the A21 A/D Converter assembly's ADC. The Agilent 89410A optimizes the ADC circuits. This procedure only needs to be done if an A21 A/D Converter assembly is replaced.

Equipment Required:

None

1 Set the power switch to on (l).

2 Press the following keys:
[**System Utility**]
[more]
[diagnostics]
[service functions]
1125
[enter]
[adjustments]
[ADC settle dither]

3 Wait until the Agilent 89410A completes the adjustment.
It takes about 6 minutes to perform the ADC software adjustment.
The message box will disappear when the adjustment is done.

This completes the A21 A/D Converter assembly adjustment.

To adjust 10 MHz low pass filter

This procedure adjusts the A35 Analog Source assembly's reconstruction filter. The reconstruction filter is a 10 MHz low pass filter.

Equipment Required:

Network analyzer
Extender board, Agilent part number 89410-B1001
(2) BNC cables
(2) N(m)-to-BNC(f) adapters
BNC(f)-to-test clips
Flat-edge adjustment tool, Agilent part number 8710-1928

1 Place the A35 Analog Source assembly on an extender board.

   a Set the power switch to off (O).

   b Remove screws holding the A35 Analog Source assembly in the card nest. Do not remove the screws in the center of the cover.

   c Place the assembly on an extender board.

   d Set the power switch to on (I).

2 Set up the Agilent 89410A.

   a Press the following keys:
   [**System Utility**]
   [more]
   [diagnostics]
   [service functions]
   1125
   [enter]
   [adjustments]

[analog source]
[setup 1]

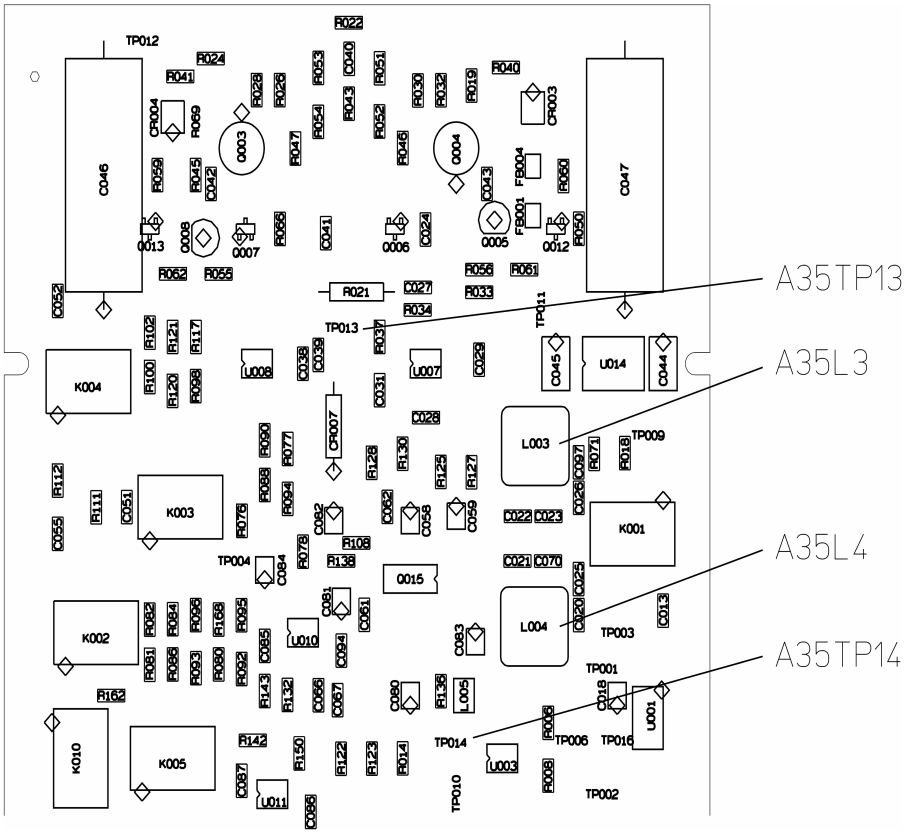
3 Set up the network analyzer.

a Set the network analyzer as follows:

Receiver	**reference channel**
Attenuation	**20 dB**
Resolution BW	**100 Hz**
Display format	**log magnitude**
Source	
Sweep Mode	**continuous**
Sweep Type	**linear frequency sweep**
Sweep Time	**3 s**
Amplitude	**-40 dBm**
Start Frequency	**10 MHz**
Stop Frequency	**30 MHz**

b Connect the network analyzer's reference channel to the Agilent 89410A's source using an N(m)-to-BNC(f) adapter and BNC cable.

c Connect the network analyzer's source to A35 TP14 (AMPIN) and TP13 (Ground) using an N(m)-to-BNC(f) adapter, BNC cable, and BNC(f)-to-test clips adapter.



4 Normalize the measurement.

a Wait for a complete sweep on the network analyzer.

b Store the trace data in a storage register.

c Set the network analyzer to divide the reference channel by the storage register.

5 Adjust A35 L3 and A35 L4.

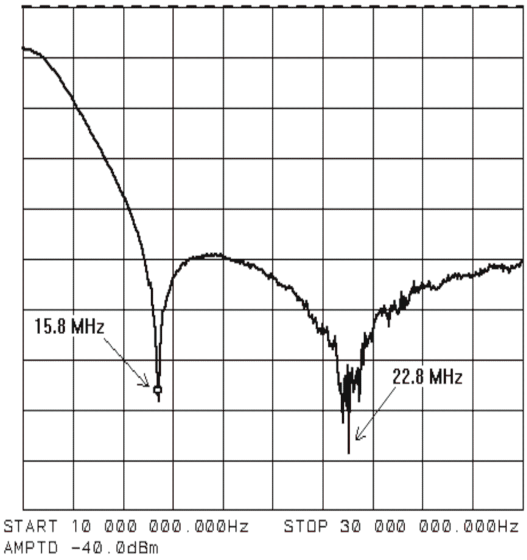
a Press the [setup 2] softkey.

b Set the network analyzer's reference level to 10 dB.

c Set the scale to 10 dB/div.

d Adjust A35 L3 for zero transmission at 15.8 MHz using the flat-edge adjustment tool.

e Adjust A35 L4 for zero transmission at 22.8 MHz using the flat-edge adjustment tool. L3 and L4 correctly adjusted



6 Reinstall the A35 Analog Source assembly.

a Set the power switch to off (O).

b Place the assembly in the card nest.
If only the source assembly adjustments are being done, go to page 2-37 to adjust the calibrator. The calibrator adjustment must be done after the channel 1 A10 Analog Input assembly or A35 Analog Source assembly is adjusted.

This completes the A35 Analog Source assembly adjustments.

To adjust auto-range detect level

This procedure adjusts the A36 Trigger assembly's ±12 Vdc regulators. The regulators are used to set the over-range and half-range detect levels in the auto-range circuits.

Equipment Required:

Digital multimeter
Extender board, Agilent part number 89410-B1002
Flat-edge adjustment tool, Agilent part number 8710-1928
Test clips-to-dual banana plug cable

1 Place the A36 Trigger assembly on an extender board.

   a Set the power switch to off (O).

   b Remove screws holding the A36 Trigger assembly in the card nest.

   c Place the assembly on an extender board.

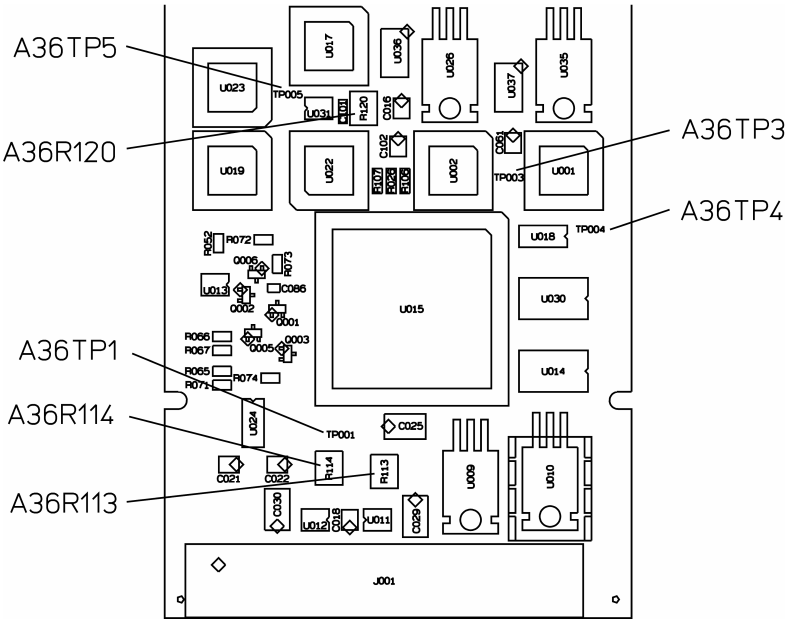
   d Set the power switch to on (l).

2 Adjust A36 R113.

   a Set the digital voltmeter to Vdc.

   b Connect the digital voltmeter to A36 TP3 and TP1 (ground).

   c Adjust A36 R113 for a voltmeter reading of 1.259 ±0.003 Vdc using the flat-edge adjustment tool.



3 Adjust A36 R114.

a Connect the digital voltmeter to A36 TP4 and TP1 (ground).

b Adjust A36 R114 for a voltmeter reading of -1.259 ±0.003 Vdc using the flat-edge adjustment tool.

4 Adjust A36 R120.

a Connect the digital voltmeter to A36 TP5 and TP1 (ground).

b Press the following keys:
[**System Utility**]
[auto cal **off**]
[more]
[diagnostics]
[service functions]
1125
[enter]
[special test modes]
[trigger]
[level DAC]
128
[enter]

c Adjust A36 R120 for a voltmeter reading of 0 ±2 mVdc using the flat-edge adjustment tool.

5 Reinstall the A36 Trigger assembly.

a Set the power switch to off (O).

b Place the assembly in the card nest.

c Reconnect the following using original cables:
A36 J3 to rear panel EXT ARM (white cable)
A36 J4 to front panel EXT TRIGGER (blue cable)
A36 J2 to A10 J3 (channel 1)
A36 J5 to A10 J3 (channel 2)

This completes the A36 Trigger assembly adjustments.

To adjust reference oscillator

This procedure adjusts the A60 Frequency Reference assembly's reference oscillator.

Equipment Required:

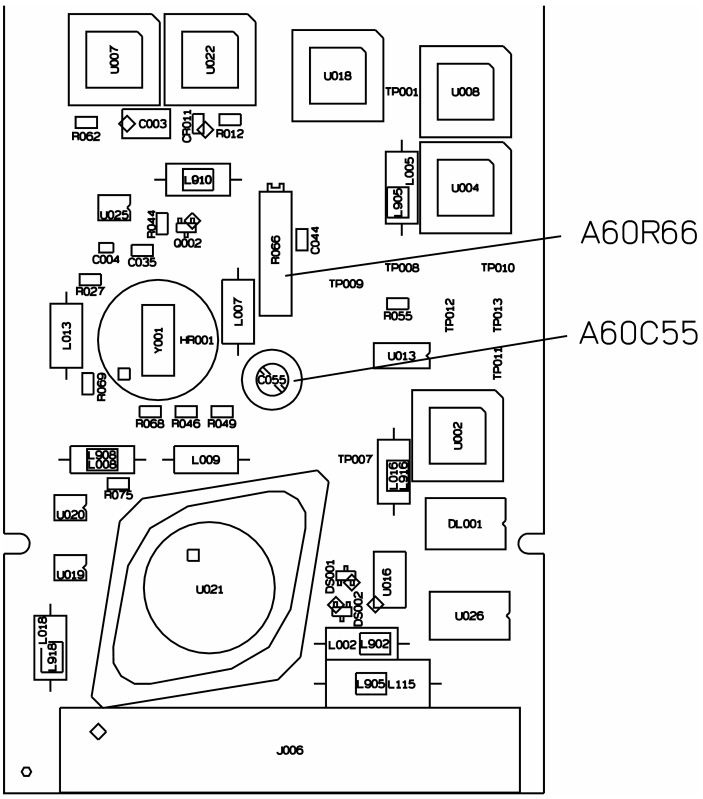
Frequency counter
Extender board, Agilent part number 89410-B1002
SMB(f)-to-BNC(m) cable
Flat-edge adjustment tool, Agilent part number 8710-1928
Plastic screw driver, Agilent part number 8710-2056

1 Place the A60 Frequency Reference assembly on an extender board.

   a Set the power switch to off (O).

   b Remove screws holding the A60 Frequency Reference assembly in the card nest.

   c Place the assembly on an extender board.



2 Adjust A60 C55.

   a Center A60 R66 by turning the potentiometer to the end and then 10 turns back.
   This is the fine frequency adjustment potentiometer. It needs to be centered before the coarse frequency adjustment is done.

   b Connect the frequency counter to A60 J2 using the SMB(f)-to-BNC(m) cable.

   c Set the power switch to on (l).

   d Adjust A60 C55 for a frequency counter reading of 25.6 MHz ±50 Hz using the flat-edge adjustment tool.

3 Reinstall the A60 Frequency Reference assembly.

   a Set the power switch to off (O).

   b Place the assembly in card nest.

   c Set the power switch to on (l).

4 Wait 5 minutes, then adjust A60 R66.

   a Wait 5 minutes for the frequency oscillator to stabilize.

   b Adjust A60 R66 for a frequency counter reading of 25.6 MHz ±10 Hz using the plastic screw driver.

5 Reconnect the cables.

   a Set the power switch to off (O).

   b Reconnect the following using original cables:
   A60 J2 to A10 J1 (channel 2)
   A60 J3 to A10 J1 (channel 1)
   A60 J4 to rear panel EXT REF IN (green cable)
   A60 J5 to rear panel EXT REF OUT (gray cable)

This completes the A60 Frequency Reference assembly adjustments.

To adjust oven frequency

This procedure adjusts the optional A85 Oven assembly's frequency. The Agilent 89410A must be on for at least 48 hours before this adjustment is made.

Equipment Required:

Oscilloscope
Frequency standard
BNC cable
Flat-edge adjustment tool, Agilent part number 8710-1928

WARNING: This procedure is performed with protective covers removed and power applied. Energy available at may points can, if contacted, result in personal injury.

Even with power removed, there can be sufficient stored energy in some circuits to cause personal injury. These voltages will discharge to a relatively safe level approximately five minutes after the power cord is disconnected.

---

1 Remove the power supply shield.

   a Set the power switch to off (O).

   b Remove the power supply shield. The power supply shield is located behind the display.

   c Set the power switch to on (l).

2 Set up the oscilloscope.

a Connect the frequency standard's output to the oscilloscope's external trigger. Check that the frequency standard is properly terminated.

b Set the oscilloscope as follows:

Channel 1	
Volts/ Div	**100 mV/ div**
Offset	**0 V**
Coupling	**1 MΩ ac**
Timebase	
Time/ Div	**50 ns/ div**
Sweep	**Triggered**
Trigger	
Level	**0 V**
Slope	**Positive**
Mode	**Edge**
Source	**External Trigger**
Display	
Mode	**Real Time**
Screen	**Single**

c Connect the rear panel OVEN REF OUT connector to the oscilloscope's channel 1 input.

3 Adjust A85 HR1.

a Adjust A85 R12 to the center of its adjustment range.

b Remove the oven adjustment screw.

c Adjust the A85 HR1, FREQ ADJ, for a stable (not moving) display on the oscilloscope.

4 Adjust A85 R12.

a Change the oscilloscope timebase to 10 ns per division.

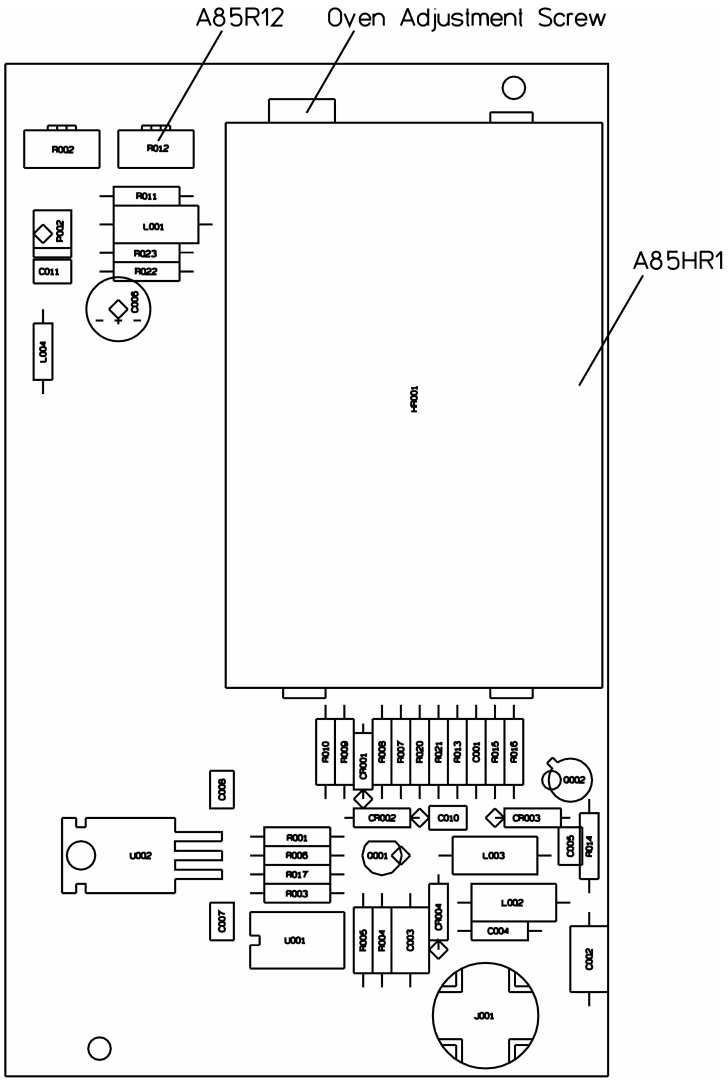
b Adjust A85 R12 for a stable display on the oscilloscope.

5 Replace the oven screw and power supply shield.

a Set the power switch to off (O).

b Replace the oven adjustment screw.

c Replace the power supply shield.



This completes the A85 Oven assembly adjustments.

To adjust calibrator

This procedure determines the exact amplitude of the calibrator signal and stores the results in Monitor Flash ROM. The calibrator signal is the amplitude reference used by the calibration routine. This procedure must be done if the channel 1 A10 Analog Input assembly, channel 1 A21 A/D Converter, or the A35 Analog Source assembly is adjusted. This procedure must also be done if the A40 CPU assembly is replaced.

CAUTION: The Monitor Flash ROM can only be written to a limited number of times. Do this procedure only when required.

Equipment Required:

Milliwatt power meter
Synthesizer
(2) BNC cables
N(f)-to-BNC(f) adapter

1 Set up the Agilent 89410A.

   a Replace all covers.

   b Set the power switch to on (l).

   c Press the following keys:
   [**System Utility**]
   [single cal]
   [more]
   [diagnostics]
   [service functions]
   1125
   [enter]
   [special test modes]
   [cal]
   [calibrator cal]
   [**System Utility**]

2 Set up the synthesizer.

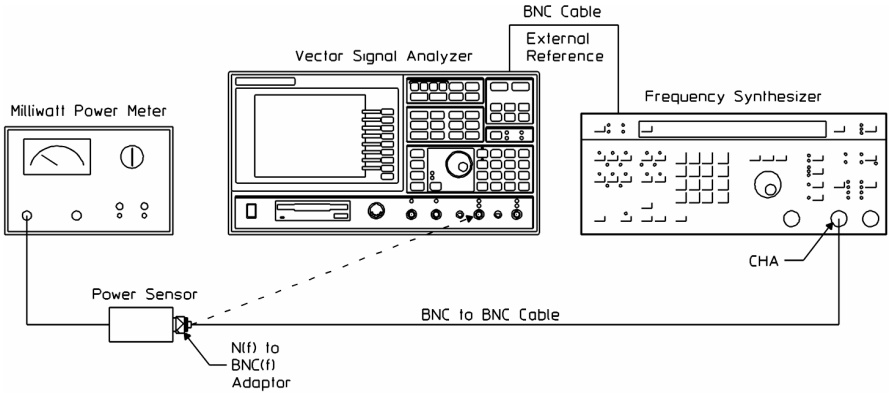
a Set the synthesizer as follows:

Frequency	**3.2 M Hz**
Amplitude	**0 dBm**
Function	**sine wave**

b Connect the synthesizer's external reference to the Agilent 89410A's EXT REF IN. See the following illustration for setup.

c Connect the synthesizer's output to the milliwatt power meter.

d Adjust the synthesizer's amplitude to read 0 dBm on the milliwatt power meter.



3 Determine and store the exact amplitude of the calibrator signal.

a Connect the synthesizer's output to Agilent 89410A's channel 1.

b Press the [single cal] softkey.

c Wait for the program to finish.
The program takes about 2 minutes to complete.

The exact amplitude of the calibrator signal is now stored in Monitor Flash ROM.

3 Replacing Assemblies

Replacing Assemblies

This chapter tells you what to do before and after you replace an assembly and shows you how to disassemble the analyzer.

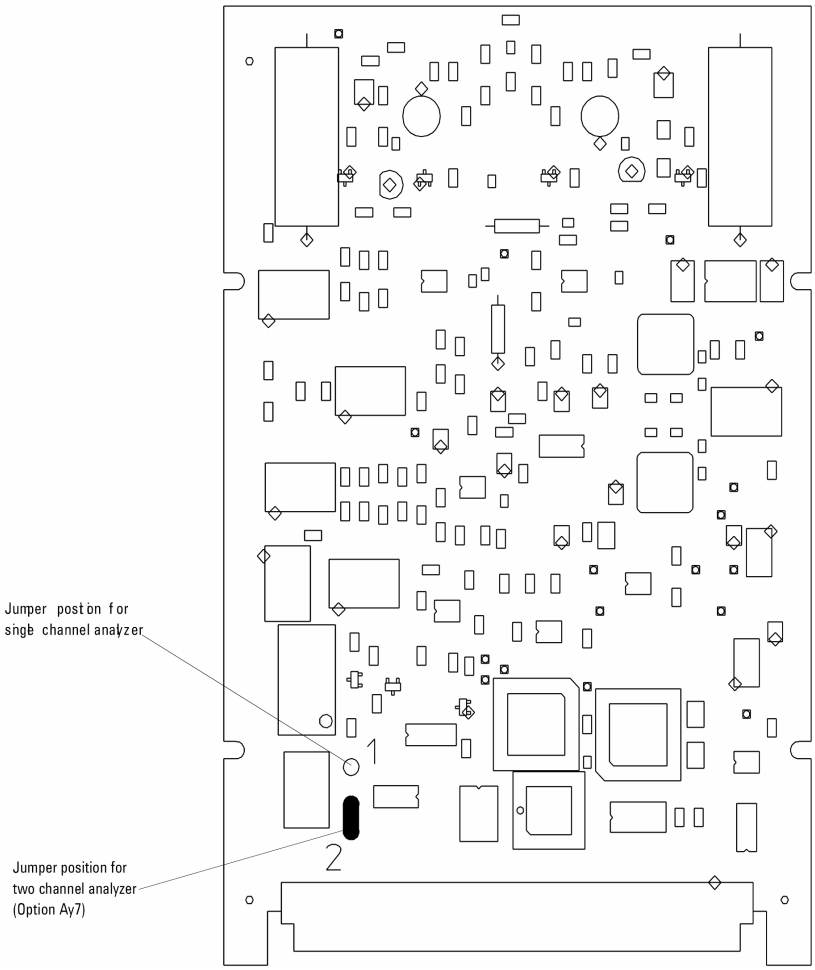
WARNING: **Disconnect the power cord from the rear panel before disassembly or assembly of the Agilent 89410A.**
Even with power removed, there can be sufficient stored energy in some circuits to cause personal injury. These voltages will discharge to a relatively safe level approximately five minutes after the power cord is disconnected.

CAUTION: Do not connect or disconnect cables from circuit assemblies with the line power turned on (|).

To protect circuits from static discharge, remove or replace assemblies only at static-protected work stations.

What to do before replacing the analog source

Before replacing the A35 Analog Source assembly, check that the jumper is in the correct position.



What to do after replacing an assembly

Option and configuration information is stored in the A40 CPU assembly and A42 Memory assembly. Providing only one assembly is replaced at a time, the option and configuration information will be stored in the replaced assembly at power up. If both the A40 and A42 must be replaced at the same time, refer to the procedures in service note 89410-09.

Follow this procedure after you replace an assembly.

1 Reinstall all assemblies and cables that were removed during troubleshooting.

2 After replacing the A40 CPU assembly, store the serial number in memory.

CAUTION: The serial number cannot be changed after it is stored in memory. Check the serial number before you enter it.

Press the following keys, then use the alpha numeric keys to enter the serial number.
[**System Utility**]
[diagnostics]
[service functions]
[define serial number]

3 After replacing the A40 CPU assembly, A42 Memory assembly, or A43 Expanded Memory assembly, install new firmware. The revision of software installed in these assemblies must match.

4 After replacing the A43 Expanded Memory assembly, set the LAN address (see the *Installation and Verification Guide*).

5 Do the required adjustments listed in the following table.

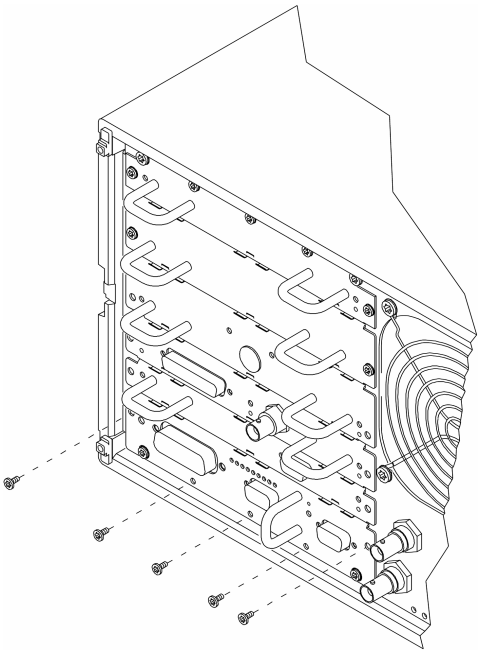
6 Do the self test (page 1-32).

7 Do the required performance tests listed in the following table (see the *Installation and Verification Guide*).

Assembly Replaced	Adjustment	Performance Test
A10 Analog Input , channel 1	Input flatness, page 2-10- Input capacitance, page 2-13- Input offset, page 2-16 Anti-alias filter, page 2-18 Calibrator, page 2-37	Amplitude accuracy Amp_phase match (option AY7 only) Input trigger Harmonic distortion Input capacitance DC offset Spurious signals Noise
A10 Analog Input, channel 2	Input flatness, page 2-10 Input capacitance, page 2-13- Input offset, page 2-16- Anti-alias filter, page 2-18	Amplitude accuracy Amp_phase match (option AY7 only) Input trigger Harmonic distortion Input capacitance DC offset Spurious signals Noise
A11 Front Panel Connector		
A12 Rear Panel Connector		
A21 A/ D Converter, channel 1	ADC, page 2-24- Calibrator, page 2-37	Amplitude accuracy Amp_phase match (option AY7 only) Harmonic distortion DC offset Spurious signals Noise
A21 A/ D Converter, channel 2	ADC, page 2-24	Amplitude accuracy Amp_phase match (option AY7 only) Harmonic distortion DC offset Spurious signals Noise
A30 Digital Source		
A35 Analog Source	10 MHz low pass filter, page 2-25 Calibrator, page 2-37	Amplitude accuracy Source amplitude accuracy Source distortion
A36 Trigger	Autorange detect level, page 2-29	Amp_phase match Input trigger External trigger External arm
A40 CPU	Calibrator, page 2-37	
A42 Memory		
A43 Expanded Memory		
A47 DSP/ Display Controller		
A50 Digital Filter		
A55 Sample RAM		
A56 Expanded Sample RAM		

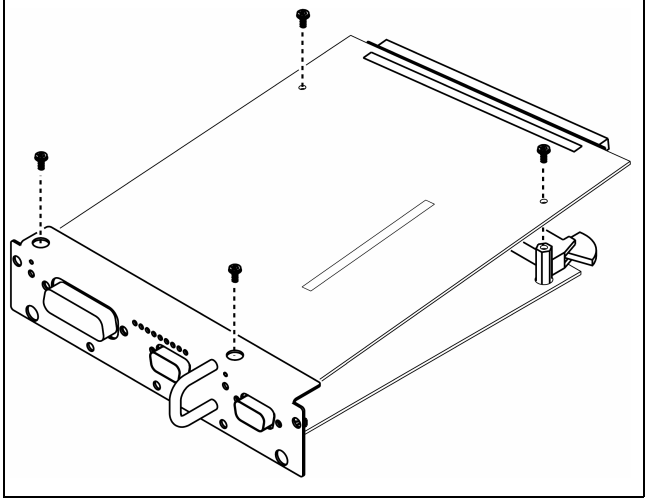
A60 Frequency Reference	Reference oscillator, page 2-32	Frequency accuracy
A61 Clock	Clock, page 2-34	Frequency accuracy
A71 Pass Through		
A81 Keyboard		
A82 Flat Panel Display Interface		
A85 Oven	Oven shutdown, page 2-7 Oven frequency, page 2-34	Frequency accuracy
A90 Digital Motherboard		
A91 Analog Motherboard		
A92 Probe Power		
A95 Main Power Supply		
A96 Primary Power Supply		
A100 Display		
A101 Disk Drive		

To remove CPU and memory

1 Using a T-10 torx driver, remove the five screws from the # 6 cover. 	**2** Pull the assemblies out of the card nest and disconnect the cables. The cables can be pulled about two inches out of the card nest.

3

Remove the four screws that hold the assemblies together. Use a T-8 torx driver to remove the two front screws and a T-10 torx driver to remove the two rear screws.



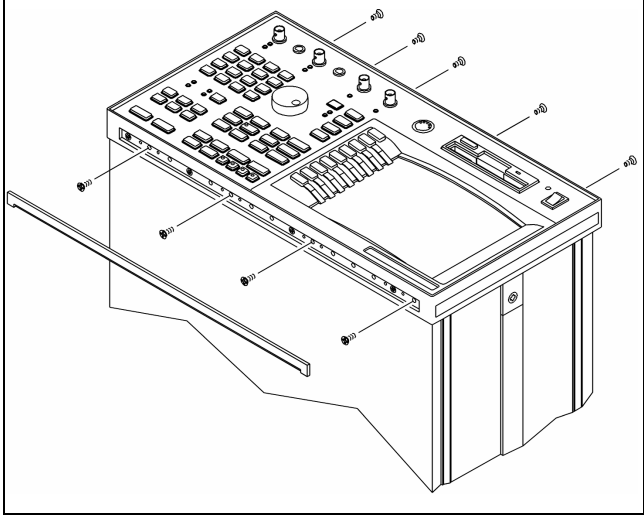
4

Unplug the A40 CPU assembly from the A42 Memory assembly.

To remove front panel

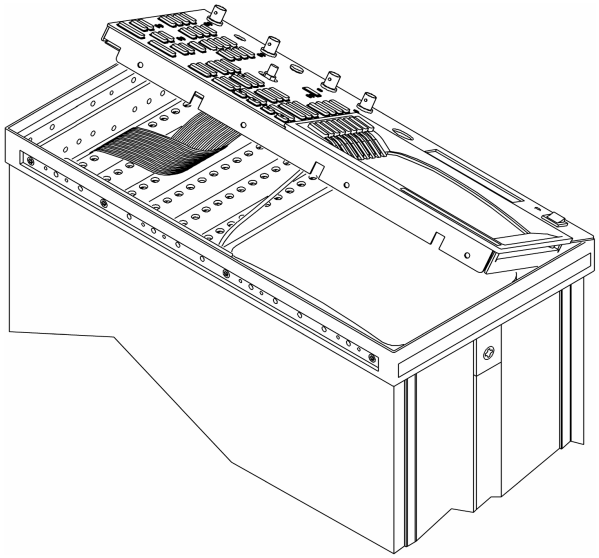
1

Remove trim strip from top of front frame. Using a T-10 torx driver, remove four screws from top and five screws from bottom of front frame.



2

Pull the top of the front panel out of the frame.



3

Disconnect the ribbon cable from the A82 Flat Panel Display Interface assembly. Disconnect the ribbon cable from the Keyboard assembly. Disconnect the coaxial cables connected to the front panel BNCs. Disconnect the probe power cables connected to the A91 Analog Motherboard assembly. Disconnect the power switch cable.

To remove the Flat Panel Display

1 Remove the front panel (see ''To remove front panel''page 3-10).	**2** Unplug the 3 pin connector from the A82 Flat Panel Interface assembly. .
3 Using a T-10 torx driver, remove the six screws from the A82 shield. Remove the A82 shield, then disconnect the ribbon cable from the A82.	**4** Using a T-10 torx driver, remove the four screw from the display bracket. Remove the display bracket by sliding down slightly towards the power switch, then lifting off.

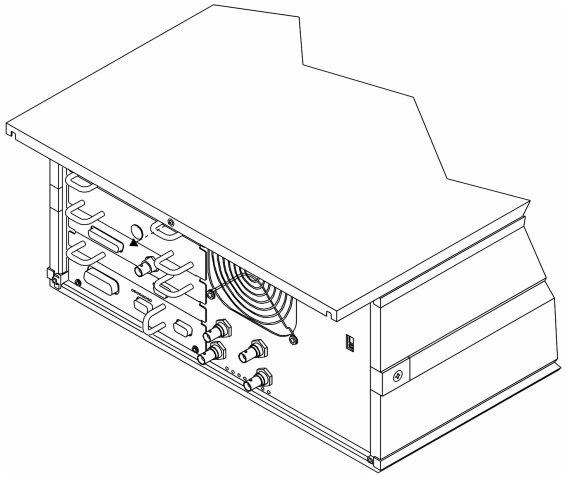
To place the A82 in the test position

1

Remove the front panel (see ‘’To remove front panel’’page 3-10).

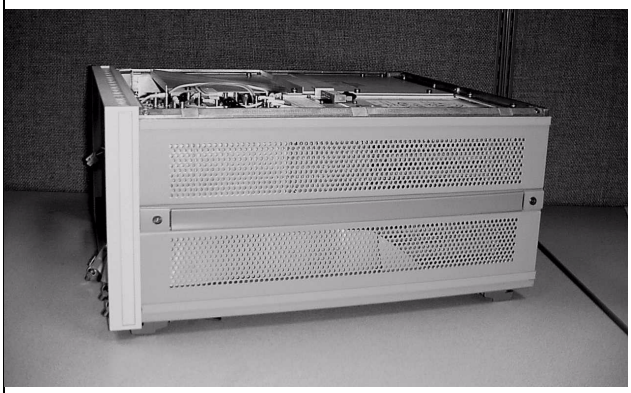
2

Using a T-15 torx driver, remove the screw from the back of the top cover. Slide the cover off.



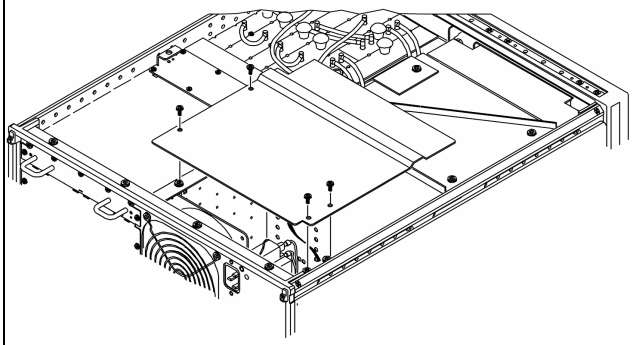
3

Using a 2 point posidrive, remove the screw from both end caps of the right side strap handle. Remove the strap handle and side cover.



4

Using a T-15 torx driver, remove the four screws from the power supply shield. Remove the power suppply shield.



5

Unplug the 3 pin connector from the A82 Flat Panel Interface assembly.

6

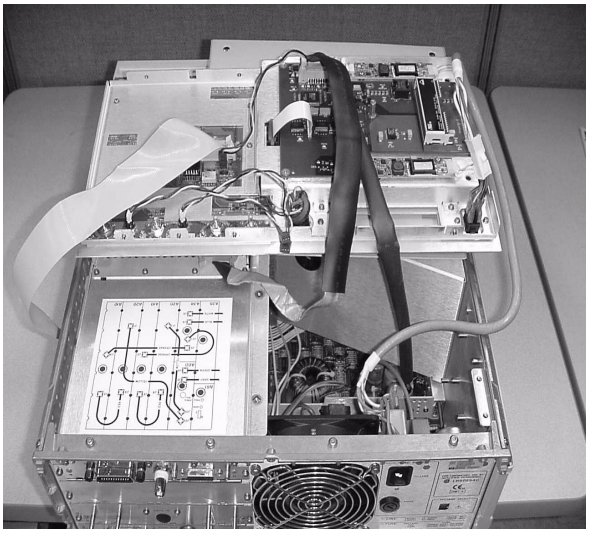
Using a T-10 torx driver, remove the six screws from the A82 sheild. Remove the A82 shield.

7

Reconnect the 3 pin connector to the A82 Flat Panel Interface assembly.

8

Route W4, W6, and W17 to the top and reconnect to the front panel assembly. W4 will need to be unplugged from A90P10 in order to route it under the air dam.



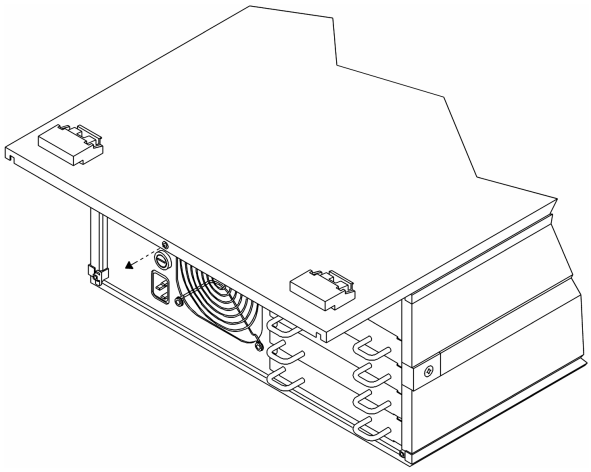
To remove disk drive

1

Remove the front panel (see ‘’To remove front panel’’page 3-10).

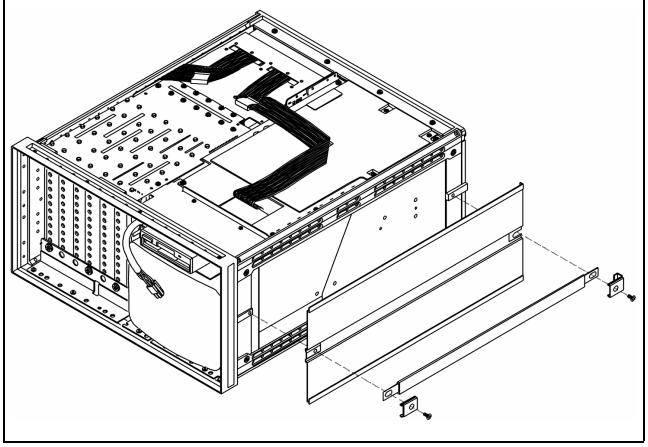
2

Using a T-15 torx driver, remove the screw from the back of the bottom cover. Slide the cover off.



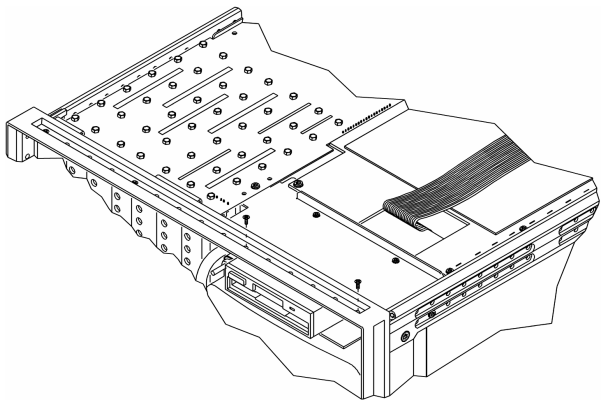
3

Using a 2 point pozidriv, remove the screw from both end caps on the strap handle nearest the Disk Drive assembly. Remove the strap handle and side cover.



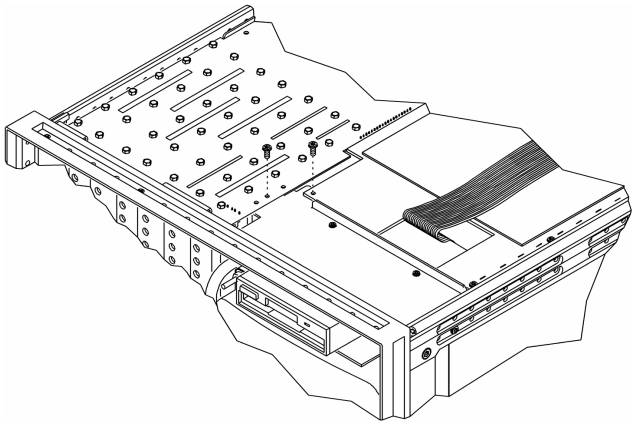
4

Using a 2 point pozidriv, remove the two screws from the front frame.



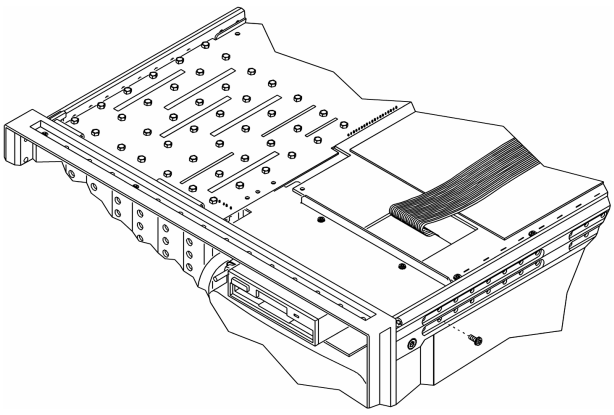
5

Using a T-15 torx driver, remove the two screws from the disk drive bracket.



6

Using a T-15 torx driver, remove the screw from the side strut.

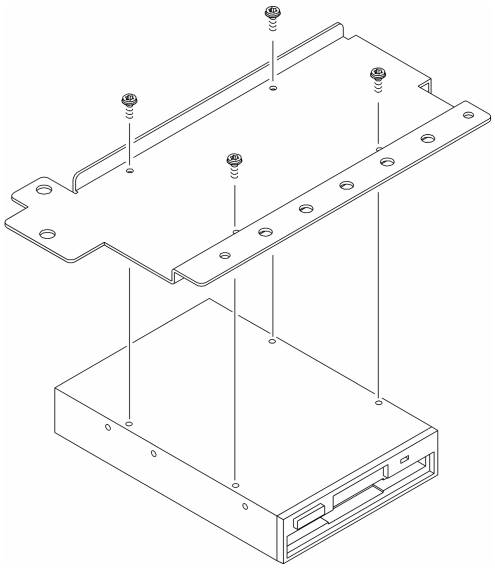


7

Note the polarity of the disk drive cable (the cable is not keyed to the Disk Drive assembly and can be incorrectly connected). Disconnect the disk drive cable from the Disk Drive assembly. Carefully guide the Disk Drive assembly, dust cover, and bracket out the front.

8

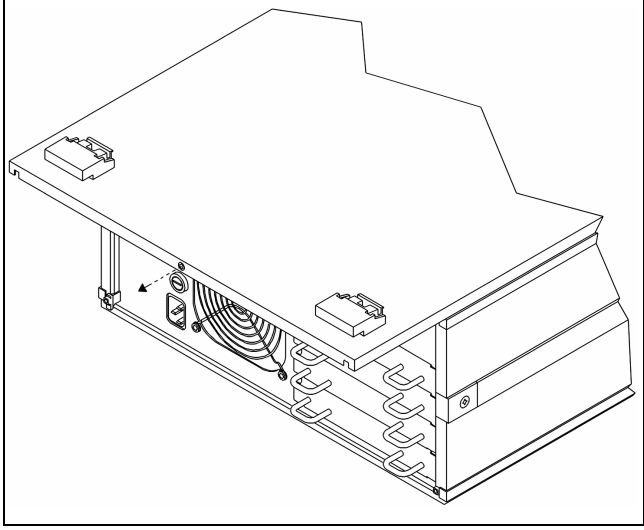
Using a T-10 torx driver, remove the four screws from the disk drive bracket.



To remove main power supply

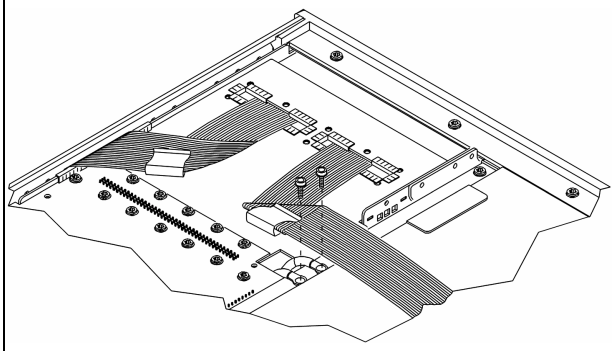
1

Using a T-15 torx driver, remove the screw from the back of the bottom cover. Slide the cover off.



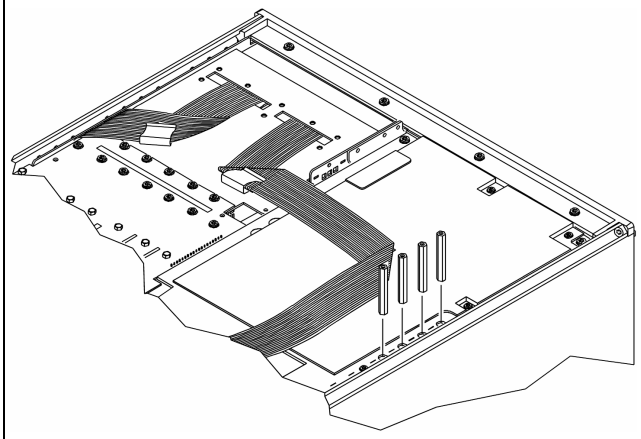
2

Using a 2.5 mm hex driver, remove the screws that fasten the red cable to A95 J301 and the black cable to A95 J302.



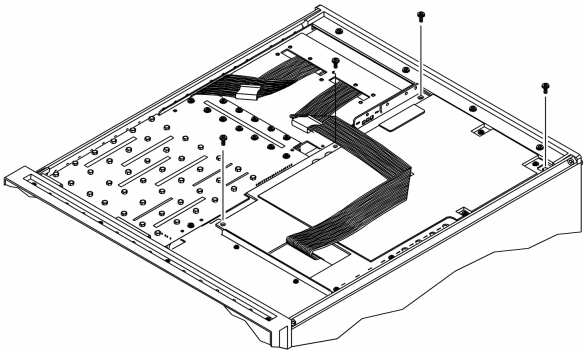
3

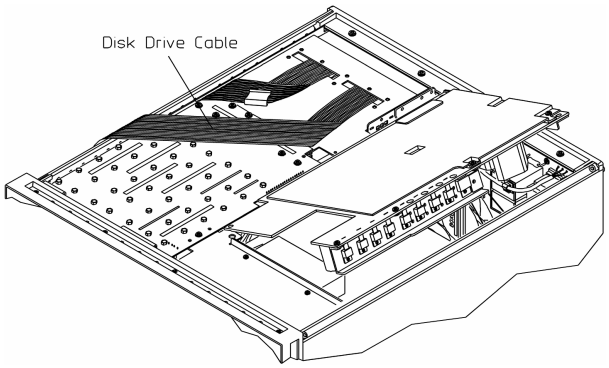
Using a 6 mm nut driver, remove the four standoffs.



4

Using a T-15 torx driver, remove the four screws from the A95 Main Power Supply assembly.

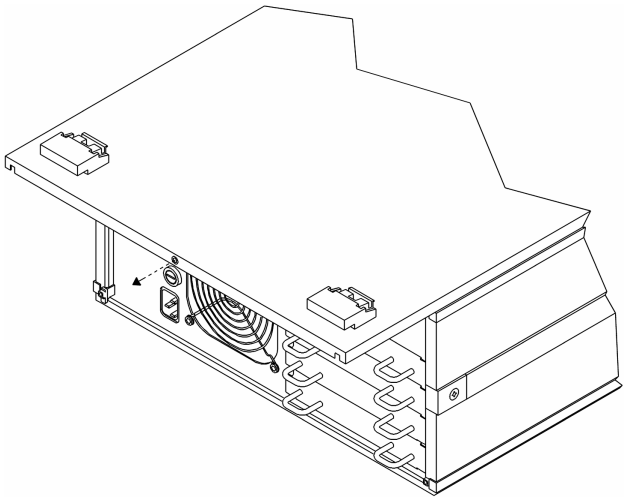


5 Note the polarity of the disk drive cable (the cable is not keyed to the Disk Drive assembly and can be incorrectly connected). Disconnect the disk drive cable from the Disk Drive assembly.	**6** Lift the A95 Main Power Supply assembly up and disconnect all cables. 

To remove analog motherboard

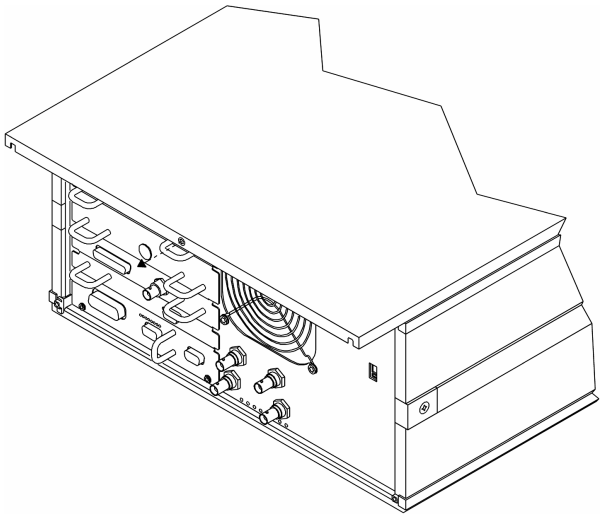
1

Using a T-15 torx driver, remove the screw from the back of the bottom cover. Slide the cover off.



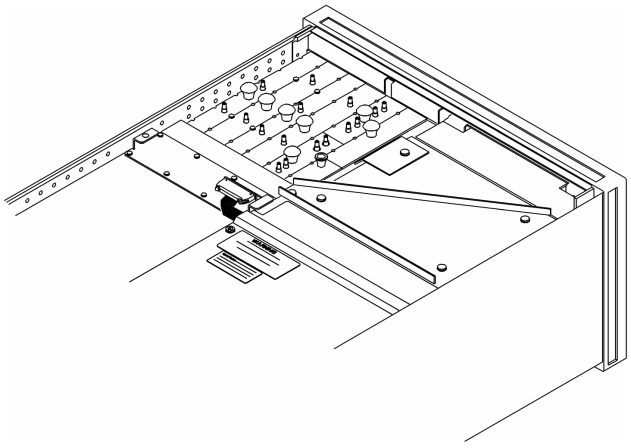
2

Using a T-15 torx driver, remove the screw from the back of the top cover. Slide the cover off.



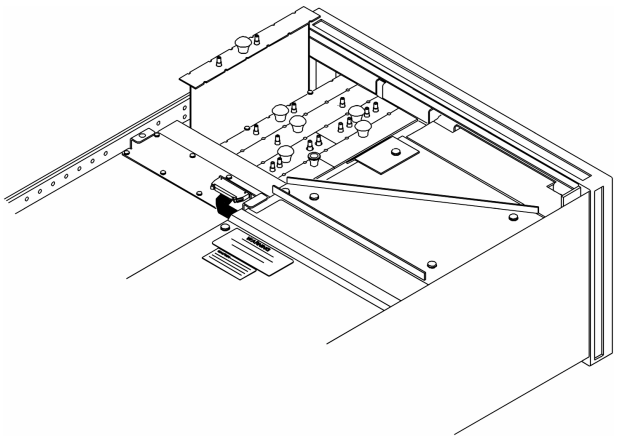
3

Disconnect the coaxial cables from the assemblies.



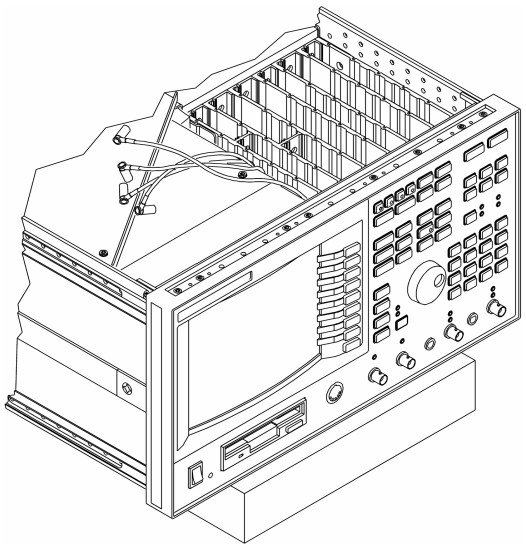
4

Using a 5 mm nut driver, remove the screws holding the assemblies in the card nest. Remove all the assemblies from the card nest.



5

Raise the front of the analyzer off the bench by placing a book under the analyzer's front frame.

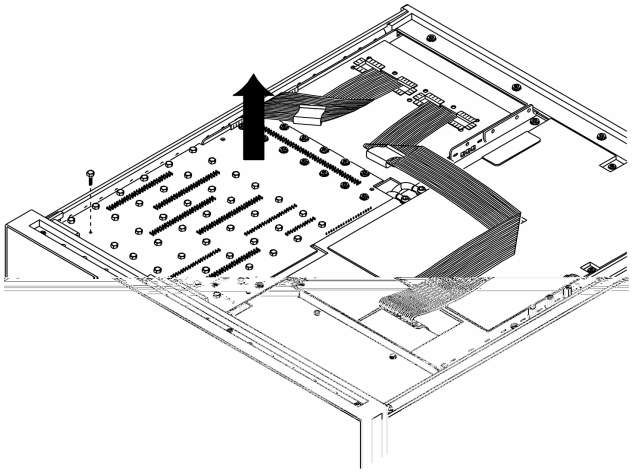


6

Position the motherboard cable extraction tool (from the service kit) inside the cardnest over the coaxial cable connector for the A35 Analog Source assembly. Carefully lower the tool allowing the center to come up as the tool is lowered into position. Once in position, push the center down to push the cable out of the A91 Analog Motherboard. Repeat for the A10 Analog Input assemblies.

7

Remove the screws from the A91 Analog Motherboard. Use a 5 mm nut driver for 42 screws, a T-10 torx driver for 13 screws, and a T-15 torx driver for 1 screw.



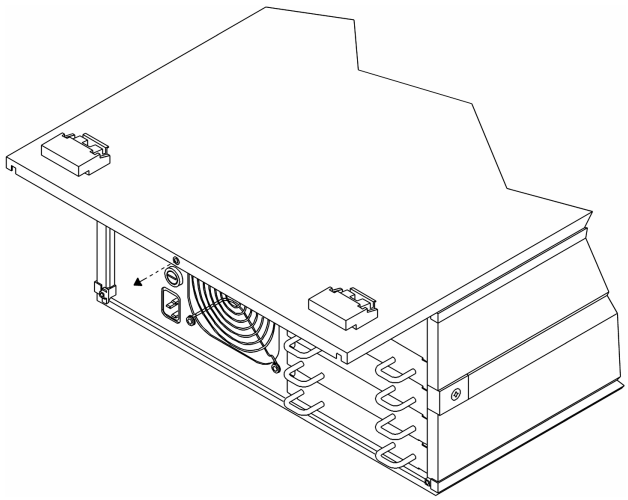
8

Lift up the A91 Analog Motherboard unplugging it from the A90 Digital Motherboard. Disconnect the power supply cable from A91 P2 and the probe power cables from A91 P3 and P5.

To remove rear panel

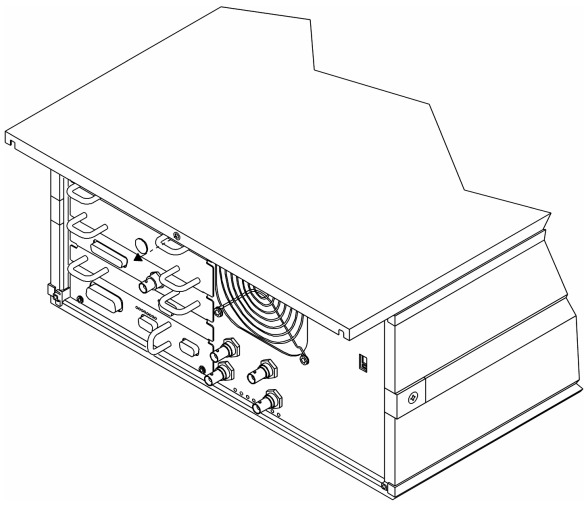
1

Using a T-15 torx driver, remove the screw from the back of the bottom cover. Slide the cover off.



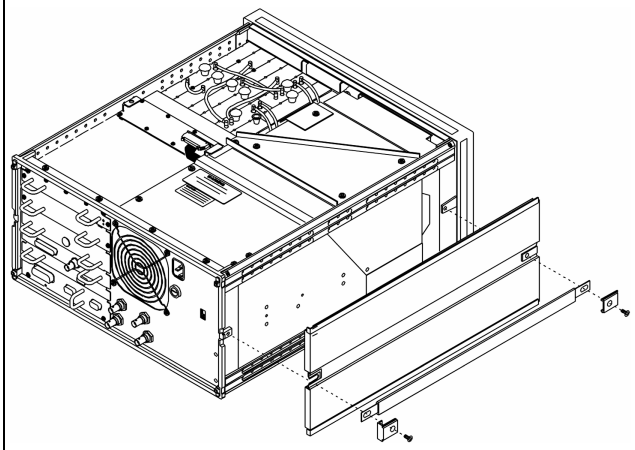
2

Using a T-15 torx driver, remove the screw from the back of the top cover. Slide the cover off.



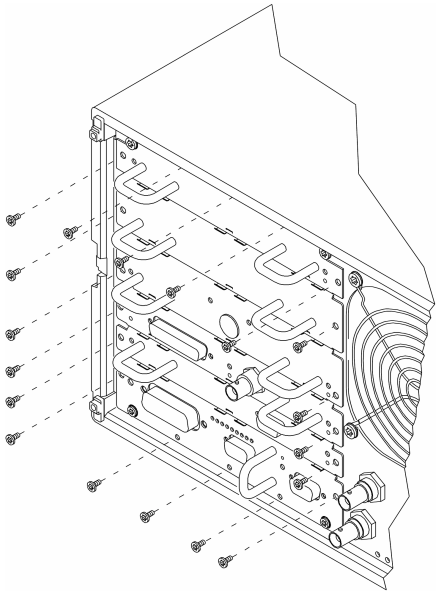
3

Using a 2 point pozidriv, remove the screw from both end caps of both strap handles. Remove the strap handles and side covers.



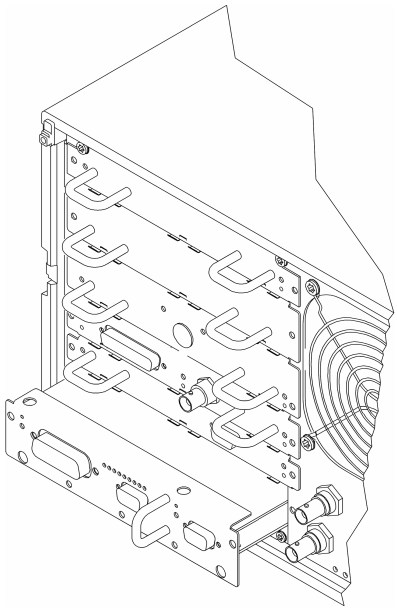
4

Using a T-10 torx driver, remove the screws from the assembly covers.



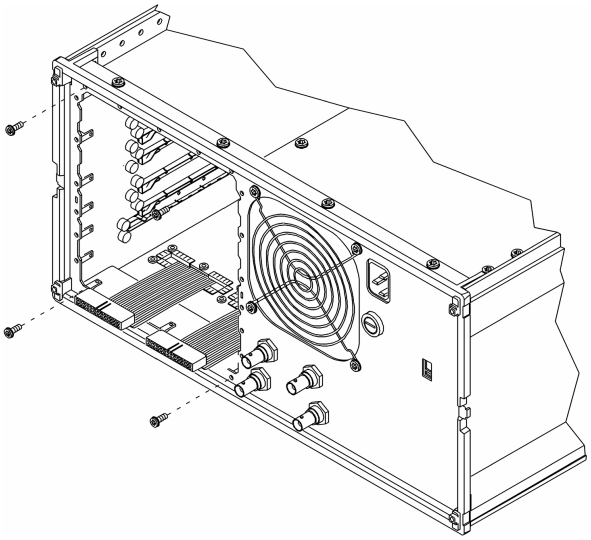
5

Remove all assemblies attached to the covers. When removing cover # 6, pull the assemblies out and disconnect the cables. Assemblies not attached to a cover may be left in the card nest.



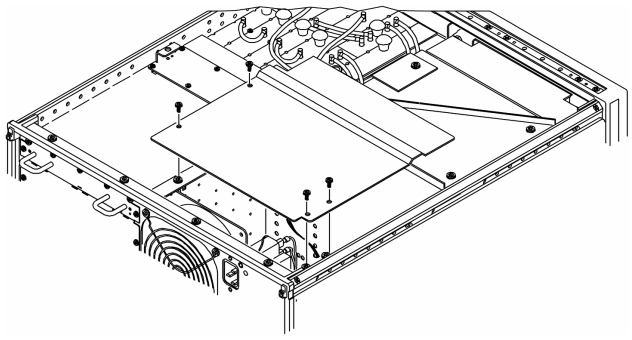
6

Using a T-10 torx driver, remove the four screws that fasten the rear panel to the card nest.



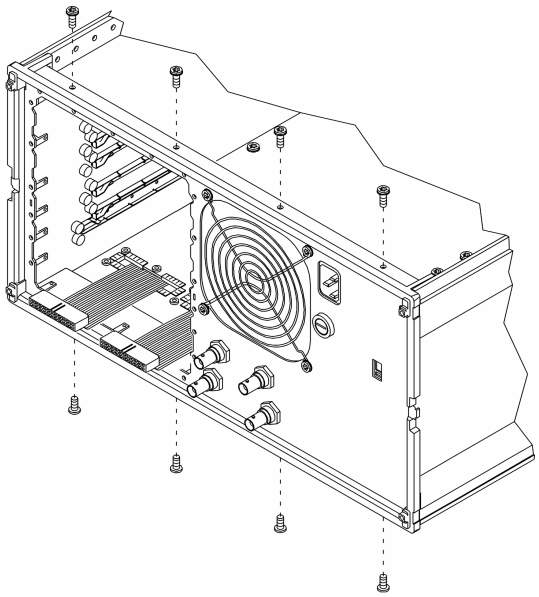
7

Using a T-15 torx driver, remove the four screws from the power supply shield. Remove the power supply shield.



8

Using a T-15 torx driver, remove the four screws on top and bottom of rear frame.

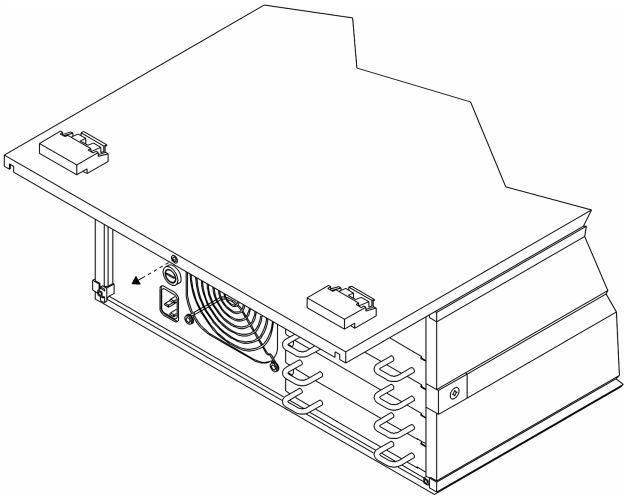


9 Disconnect the cables connected to A36 J3, A60 J4, and A60 J5. Remove the gray cable from the cable clamp on the right rear of the display. Disconnect the fan cable from A95 P353. Disconnect the primary power cables from A95 P350 and A95 P352. Disconnect the power switch cable from the A96 Primary Power Supply assembly, fuse holder, and line filter (use a 7 mm nut driver to disconnect the orange wire from the line filter). For analyzers with the oven option, disconnect the cable to OVEN REF OUT. Pull the top of the rear panel out of the frame.	

To remove digital motherboard

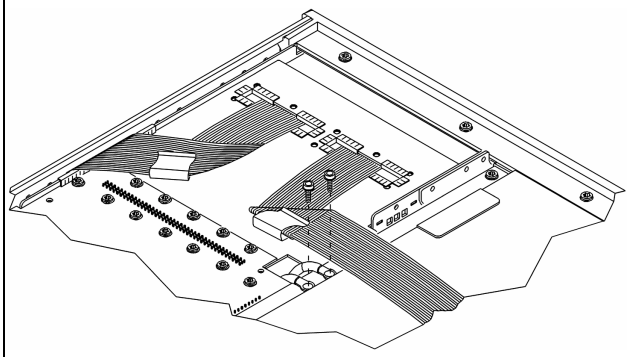
1

Using a T-15 torx driver, remove the screw from the back of the bottom cover. Slide the cover off.



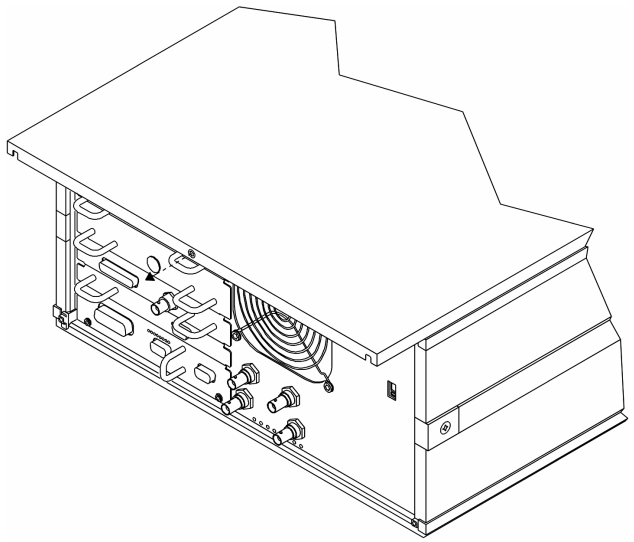
2

Using a 2.5 mm hex driver, remove the screws that fasten the red cable to A95 J301 and the black cable to A95 J302.



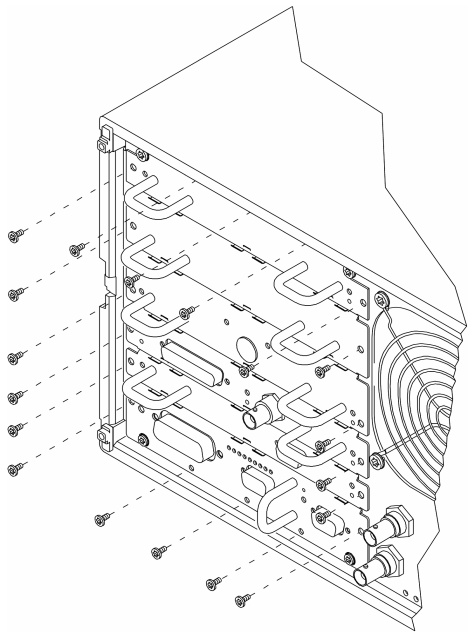
3

Using a T-15 torx driver, remove the screws from the back of the top cover. Slide the cover off.



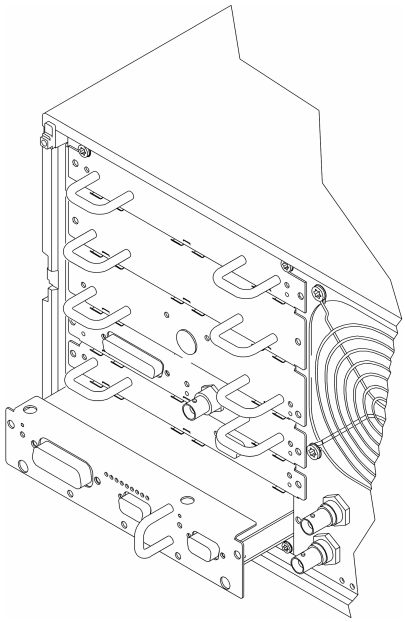
4

Using a T-10 torx driver, remove the screws from the assembly covers.



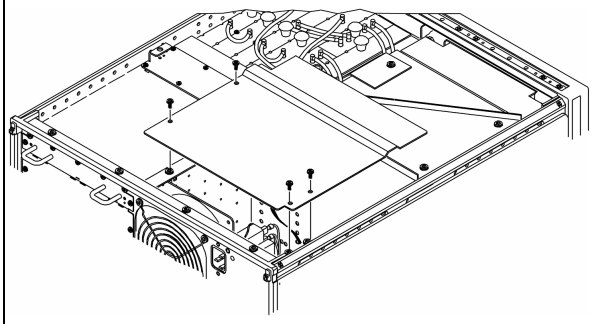
5

Unplug all assemblies from the A90 Digital Motherboard. To unplug the assembly behind cover # 3, remove assembly attached to cover # 3.



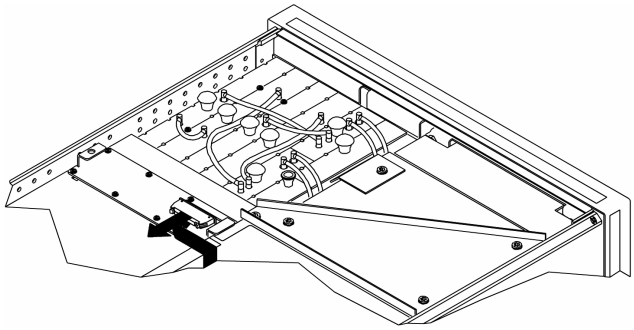
6

Using a T-15 torx driver, remove the four screws from the power supply shield. Remove the power supply shield.



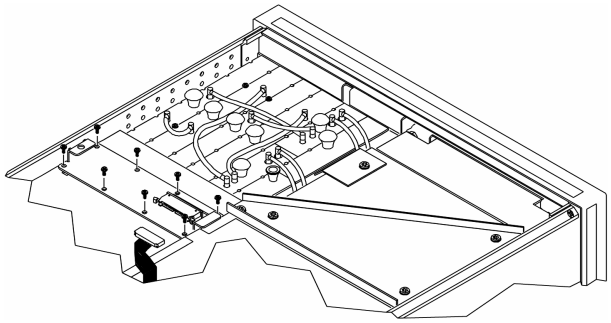
7

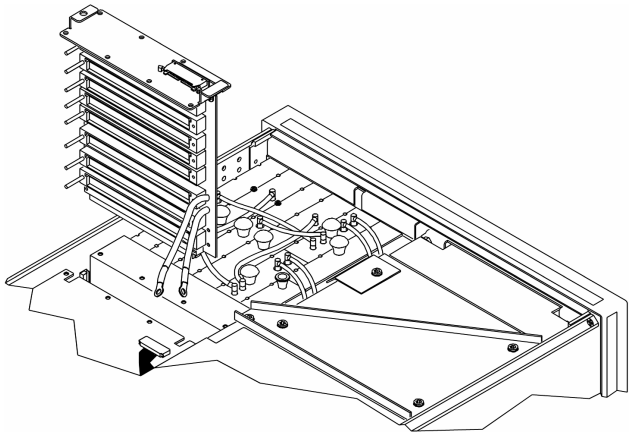
Disconnect the display cable from the A90 Digital Motherboard.



8

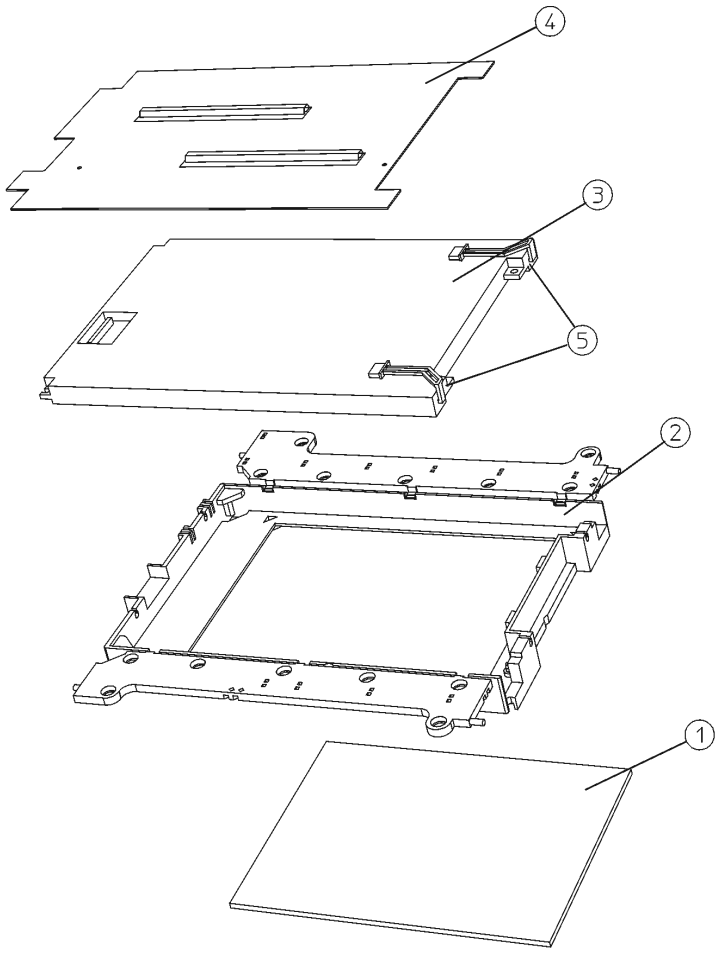
Using a T-10 torx driver, remove the eight screws from the A90 Digital Motherboard.



9 Pull the A90 Digital Motherboard out of the card nest. 	

A100 Display, Backlights, and Filter

Display Parts



Refer to firgure above. The display assembly consist of:

- EMI filter (1)
- display mount (2)
- LCD with backlights (3)
- display shield board (4)

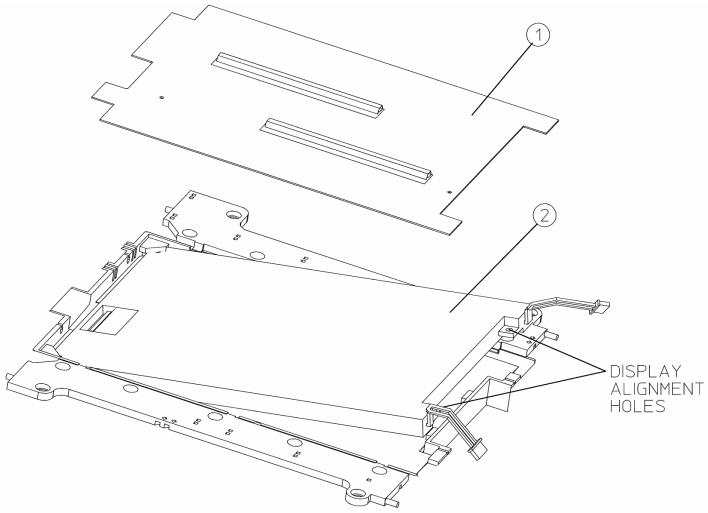
Display Removal

CAUTION: The new flat panel display comes with a protective plastic sheet over the glass. Remove this plastic very slowly to avoid damage due to ESD.

CAUTION: The surface of the display is very easily scratched. Avoid touching it with your bare hands or other objects. Use a blower to remove any dust from the display surface.

1. Remove the rubber mount that houses the display assembly from the front frame
2. Pull open the flaps of the rubber mount.
3. Remove the display shield board (1).
4. Now it is possible to carefully lift up on the display (2) to remove it from the rubber mount.

A2 Display Replacement



Display Replacement

1 Carefully slide the display into the rubber mount. Align the pins on the mount with the holes in the display.

2 Replace the display shield.

3 Close the flaps on the rubber mount.

4 Carefully place the display mount into position in the front frame assembly as shown in Display Removal procedure.

5 Plug the flat flex cable into the display connector.

Backlight Removal/ Replacement

There are two backlight assemblies installed in the flat panel display.

NOTE: The backlight lamps should be replaced as a pair, even if only one lamp is bad. The other one might fail shortly.

Refer to the "Display Removal" procedure on page 3-27. Unplug the backlight cables from the backlight connectors

It is not necessary to remove the display mount from the front frame to change the backlights.

The following Figure shows how the backlights slide out of the display. Carefully pull on the tab on the backlight assembly (2) to slide the backlight partially out of the display. Once the end of the backlight casing is exposed, you can pull it straight out from the display.

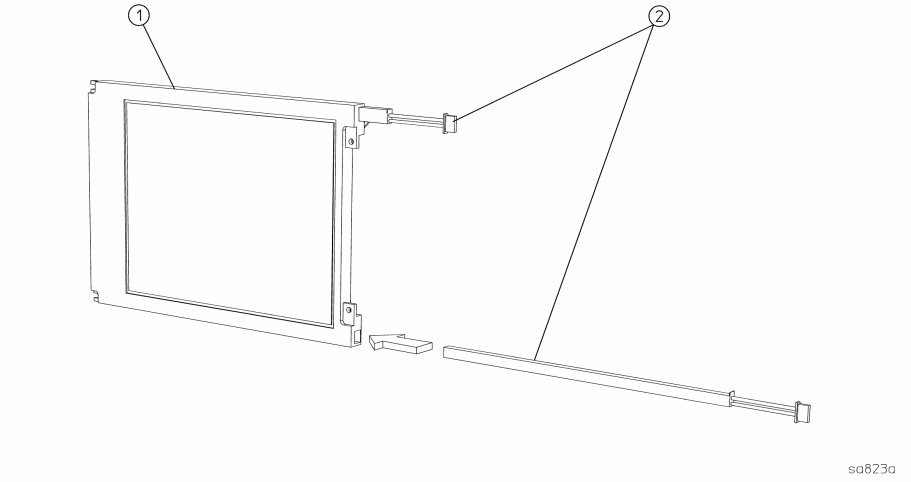
NOTE: Do not touch the bulb encased in the plastic backlight assembly.

---

1 Insert the new backlight assembly (2) by sliding it into the display, non-wired end first, taking care not to force it. It is keyed so it will only fit properly one way. Slide it all the way in to the end of the casing.

2 Connect the backlight cables to the backlight connectors.

Display Backlight Replacement



4 Replaceable Parts

Replaceable Parts

This chapter contains information for ordering replacement parts for the Agilent 89410A DC-10 MHz Vector Signal Analyzer.

Ordering Information

Replacement parts are listed in the following ten tables:

- Assemblies
- Cables
- Instrument Covers and Handles
- Assembly Covers and Brackets
- Front Panel Parts
- Rear Panel Parts
- Chassis Parts
- Card Nest Parts
- Screws, Washers, and Nuts
- Miscellaneous Parts

To order a part listed in one of the tables, quote the Agilent Technologies part number (Agilent Part Number), the check digit (CD), indicate the quantity required, and address the order to the nearest Agilent Technologies sales and service office (see the inside back cover of this guide). The check digit verifies that an order has been transmitted correctly, ensuring accurate and timely processing of the order. The first time a part is listed in the table, the quantity column (Qty) lists the total quantity of the part used in the analyzer. For the corresponding name and address of the manufacturers' codes shown in the tables, see ''Code Numbers.''

CAUTION: Many of the parts listed in this chapter are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unnecessary damage.

Non-Listed Parts

To order a part that is NOT listed in the replaceable parts tables, indicate the instrument model number, instrument serial number, description and function of the part, and the quantity of the part required. Address the order to the nearest Agilent Technologies sales and service office (see the inside back cover of this guide).

Direct Mail Order System

Within the U.S.A., Agilent Technologies can supply parts through a direct mail order system. Advantages of the Direct Mail Order System are:

Direct ordering and shipment from the Agilent Parts Center.

No maximum or minimum on any mail order. There is a minimum order for parts ordered through a local Agilent sales and service office when the orders require billing and invoicing.

Transportation charges are prepaid. A small handling charge is added to each order.

No invoicing. A check or money order must accompany each order.

Mail order forms and specific ordering information are available through your local Agilent Technologies sales and service office.

Code Numbers

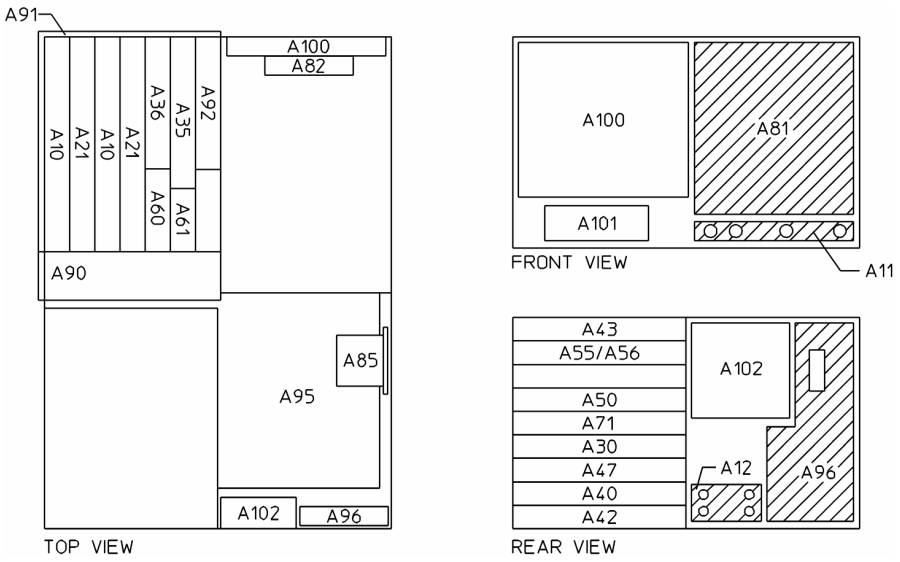
The following table provides the name and address for the manufacturers' code numbers (Mfr Code) listed in the replaceable parts tables.

Mfr No.	Mfr Name	Address
03480	Heyco Molded Products	Kentworth, NJ 07033 U.S.A.
05791	Lyn-Tron Inc	Burbank, CA 91505 U.S.A.
06691	House of Metrics LTD	Spring Valley, NY 10977 U.S.A.
06915	Richco Plastic Co	Chicago, IL 60646 U.S.A.
09328	Dreefs Switch Inc.	Waukegan, IL 60087 U.S.A.
10421	Epson America Inc.	Dallas, TX 75284 U.S.A.
10938	Qualtek Electronics	Cleveland, OH 44194 U.S.A.
27264	Molex Inc	Lisle, IL 60532 U.S.A.
28480	Agilent Technologies, Inc	Palo Alto, CA 94304 U.S.A.
30817	Instrument Specialties Co. Inc.	Placentia, CA 92670 U.S.A.
34785	Dek Inc.	St Charles, IL 60174 U.S.A.
43744	Panasonic Industrial Co	Secaucus, NJ 07094 U.S.A.
56501	Thomas & Betts Corp	Bridgewater, NJ 08807 U.S.A
57003	Chomerics Shielding Technology	Carson, CA 90745 U.S.A.
71400	Cooper Industries Inc	St Louis, MO 63178 U.S.A.
73734	Federal Screw Products Co.	Chicago, IL 60618 U.S.A.
75915	Littelfuse Inc.	Des Plaines, IL 60016 U.S.A.
76381	3M Co.	Seattle, WA 98124 U.S.A.
86928	Seastrom Mfg Co.	Glendale, CA 91201 U.S.A.
90949	Amphenol Corporation	Danbury, CT 06810 U.S.A.
H9027	Schurter Ag	Petaluma, CA 94952 U.S.A.
S4307	Schaffner Ag	Union, NJ 07083 U.S.A.

Assemblies

After replacing an assembly, see ''What to do after replacing an assembly'' in chapter 3,page 3-5 for required adjustments and performance tests.

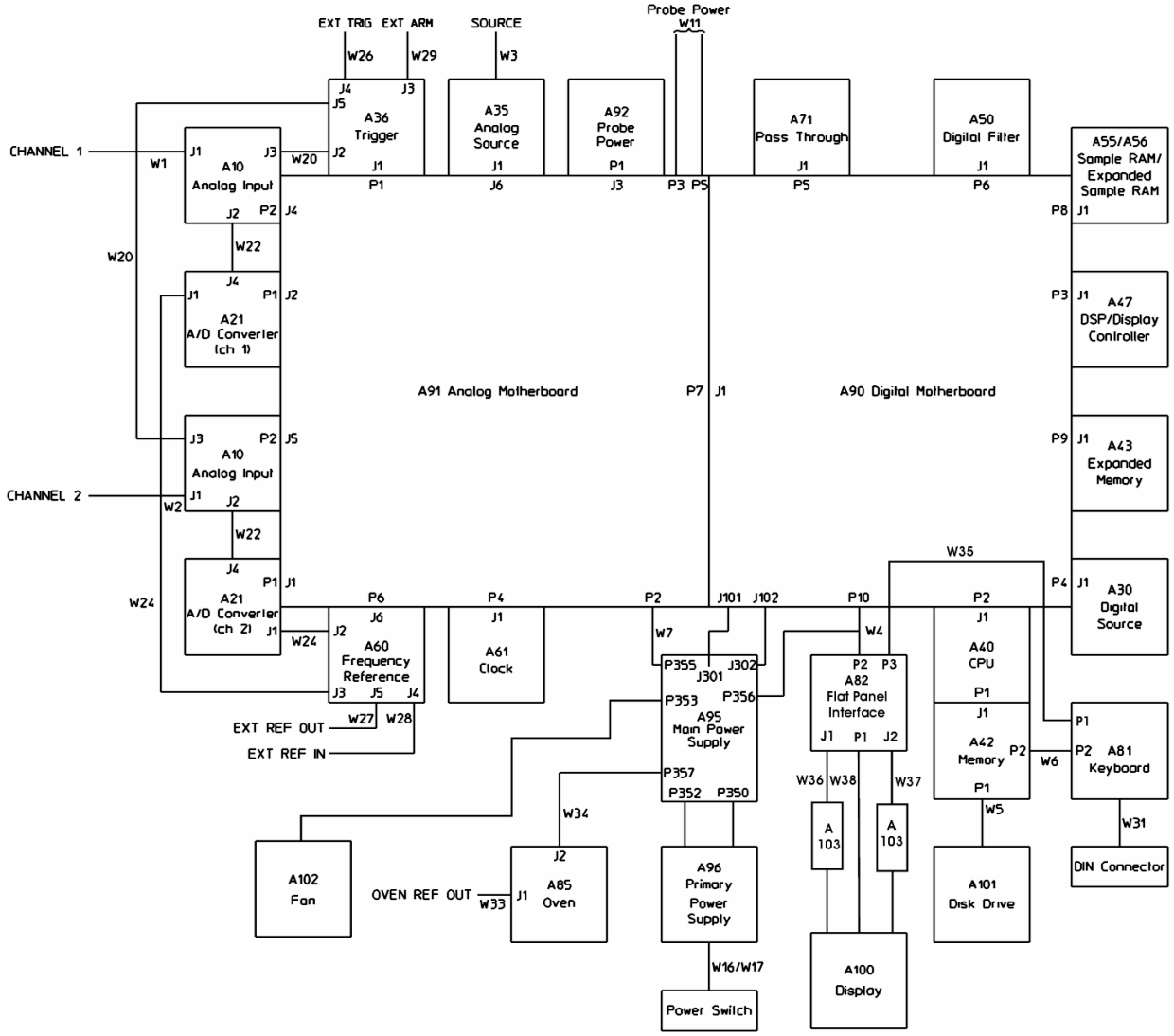
CAUTION: Do not replace the A40 CPU assembly and the A42 Memory assembly at the same time. Option and configuration information will be lost if both assemblies are replaced at the same time. If both assemblies must be replaced, refer to the procedures in service note 89410A-09.



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A10	89410-69510	9	1	ANALOG INPUT	28480	89410-69510
A11	89410-66511	4	1	FRONT PANEL CONNECTOR	28480	89410-66511
A12	89410-66512	5	1	REAR PANEL CONNECTOR	28480	89410-66512
A21	89410-69521	1	1	A/ D CONVERTER	28480	89410-69521
A30	89410-69530	3	1	DIGITAL SOURCE	28480	89410-69530
A35	89410-69535	8	1	ANALOG SOURCE †	28480	89410-69535
A36	89410-69536	9	1	TRIGGER	28480	89410-69536
A40	89410-69540	5	1	CPU	28480	89410-69540
A41	89410-69541		1	89441V CPU	28480	89410-69541
A42	89410-69542	7	1	MEMORY	28480	89410-69542
A43	89410-69543	2	1	EXPANDED MEMORY OPTION UFG	28480	89410-69543
A47	89410-69547	0	1	DSP/ DISPLAY CONTROLLER	28480	89410-69547
A50	89410-69550	7	1	DIGITAL FILTER	28480	89410-69550
A55	89410-69555	2	1	SAMPLE RAM	28480	89410-66555
A56	89410-69556	3	1	EXPANDED SAMPLE RAM OPTION AY9	28480	89410-66556
A60	89410-69560	9	1	FREQUENCY REFERENCE	28480	89410-69560
A61	89410-66561	4	1	CLOCK	28480	89410-66561
A71	89410-69571	1	1	PASS THROUGH	28480	89410-69571
A81	89410-66581	7	1	KEYBOARD	28480	89410-66581
A82	89410-69582		1	FLAT PANEL DISPLAY INTERFACE	28480	89410-69582
A85	89410-66585	2	1	OVEN OPTION AY5	28480	89410-66585
A90	89410-66590	9	1	DIGITAL MOTHERBOARD	28480	89410-66590
A91	89410-66591	0	1	ANALOG MOTHERBOARD	28480	89410-66591
A92	89410-66592	1	1	PROBE POWER	28480	89410-66592
A95	89410-69595	0	1	MAIN POWER SUPPLY	28480	89410-69595
A96	89410-66596	5	1	PRIMARY POWER SUPPLY	28480	89410-66596
A100	2090-0396	7	1	FLAT PANEL DISPLAY	28480	2090-0396
A101	0950-3671	9	1	DISC 3.5" FLOPPY DRIVE †	10421	SMD-340
A102	3160-0845	4	1	FAN-ASSY	28480	03561-68501
A103	0950-3379		2	INVERTER BOARD	28480	0950-3379

†See ''What to do before replacing the analog source or disk drive'' on page 3-4.

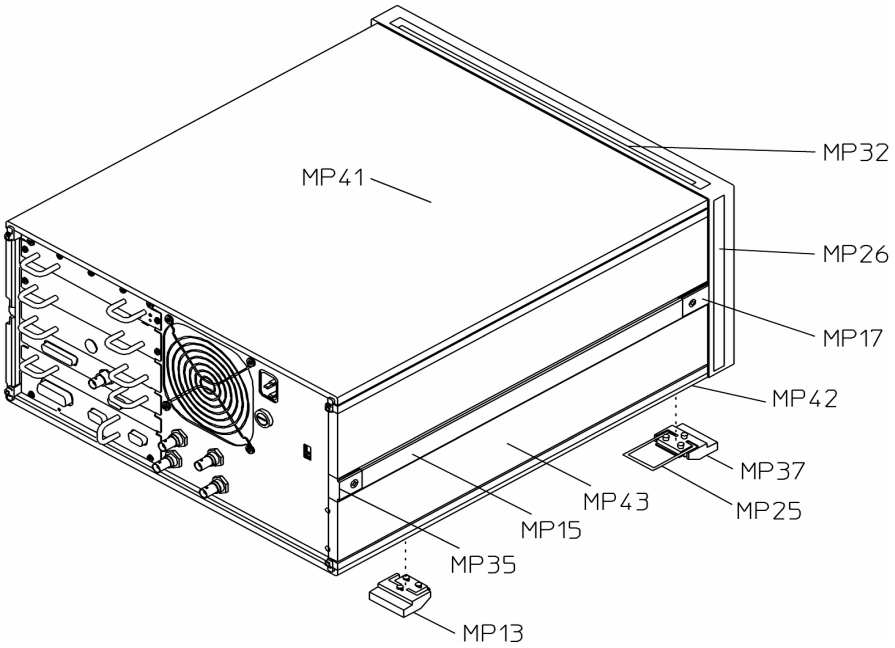
Cables



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
W1-W3	89410-61601	3	3	CBL-ASM CXL SMB/ SMB 130MM	28480	89410-61601
W4	89410-61603	5	1	CBL-ASM RBN FDIP/ FDIP 450MM	28480	89410-61603
W5	89410-61604	6	1	CBL-ASM RBN RBNF/ RBNF 700MM	28480	89410-61604
W6	89410-61606	8	1	CBL-ASM RBN RBNF/ RBNF 750MM	28480	89410-61606
W7	89410-61611	5	1	CBL-ASM DSC FHSG/ FHSG 2050 WH	28480	89410-61611
W11	89410-61616	9	2	CBL-ASM TWS 200 ML	28480	89410-61616
W14	89410-61613	7	1	CBL-ASM FFST/ FFST 95 BR/ WH	28480	89410-61613
W16	89410-61634	2	1	CBL-ASM JKT-POWER	28480	89410-61634
W17	03563-61636	8	1	CBL-ASM MHSG1ETRM 67MM LG ML	28480	03563-61636
W20	03577-61641	1	2	CBL-ASM CXL FSMB/ FSMB 135MM OR	28480	03577-61641
W22	03585-61602	4	2	CBL-ASM CXL FSMB/ FSMB 76MM RD	28480	03585-61602
W24	03585-61604	6	2	CBL-ASM CXL FSMB/ FSMB 177MM YL	28480	03585-61604
W26	03585-61606	8	1	CBL-ASM CXL FSMB/ FSMB 406MM BL	28480	03585-61606
W27	03585-61612	6	1	CBL-ASM CXL FSMB/ FBNC 762MM GY	28480	03585-61612
W28	03585-61613	7	1	CBL-ASM CXL FSMB/ FBNC 762MM GN	28480	03585-61613
W29	03585-61614	8	1	CBL-ASM CXL FSMB/ FBNC 863MM WH	28480	03585-61614
W31	89410-61617		1	CBL-ASM DSC CDIN/ CRP 205MM ML	28480	89410-61617
W33	8120-2682	2	1	CABLE ASSY-COAX 50-OHM 8.5-IN-LG 30PF/ FT	28480	8120-2682
W34	89410-61619	3	1	CBL-ASM DSC 325MM ML	28480	89410-61619
W35	89410-61623		1		28480	89410-61623
W36	8120-8750		1		28480	
W37	8120-8750		1		28480	
W38	8120-8480		1		28480	
	9170-1727		1	FERRITE BEAD FOR W38	28480	

Instrument Covers and Handles

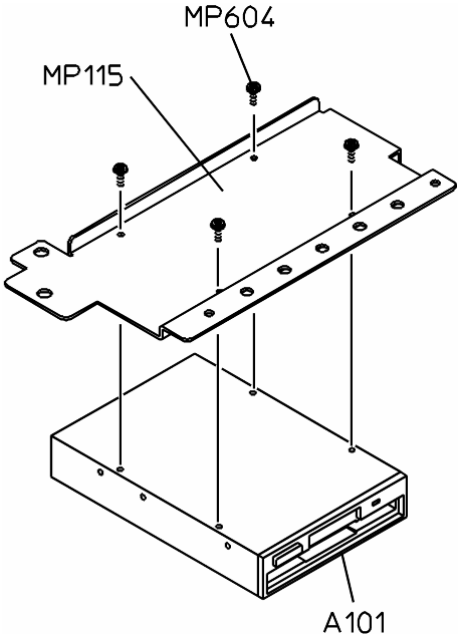
The reference designator for the screws that fasten the handles to the analyzer is MP610.



Assembly Covers and Brackets

Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP13	5041-9167	8	2	MOLD FOOT	28480	5041-8801
MP15	5063-9210	4	2	SHTF ASSY-SD HNDL 497D	28480	5062-3704
MP17	5041-9186	8	2	MOLD STRP HDL CAP FRT	28480	5041-8819
MP25	1460-1345	5	2	TILT STAND SST	28480	1460-1345
MP26	5041-9173	3	2	TRIM-FRT FRM SD 221.5H	28480	5001-0541
MP32	5041-9176	9	1	MOLD TRM-TOP FM	28480	5041-8802
MP35	5041-9187	1	2	MOLD STRP HDL CAP RR	28480	5041-8820
MP37	5041-9168	3	2	MOLD FOOT-NON SKID	28480	5041-8822
MP41	5002-1047	1	1	SHTF CVR-TOP FM 497D	28480	5062-3735
MP42	5002-1088	5	1	SHTF CVR-BTM FM 497D	28480	5062-3747
MP43	5002-3989	6	2	SHTF CVR-SD RS182H497D	28480	5062-3847
MP45	8160-0360	3	7	RFI ROUND STRIP STL MSH/ SIL RBR SN-PL	57003	02-0101-0053-05
MP46	8160-0558	1	6	STMP RFI FNGRS 176MM LG BECUTN	30817	97-542-02-X 176 MM LG
	5063-9229	1	1	FRONT HANDLE KIT	28480	5062-3991

The reference designator for the screws that fasten the front of the A40 CPU assembly to the A42 Memory assembly is MP621. The reference designator for the screws that fasten the rear of the A40 CPU assembly to the A42 Memory assembly is MP604. The reference designator for the screws that fasten the assembly covers to the top of the analyzer is MP615. The reference designator for the screws that fasten the assembly covers to the rear of the analyzer is MP604.

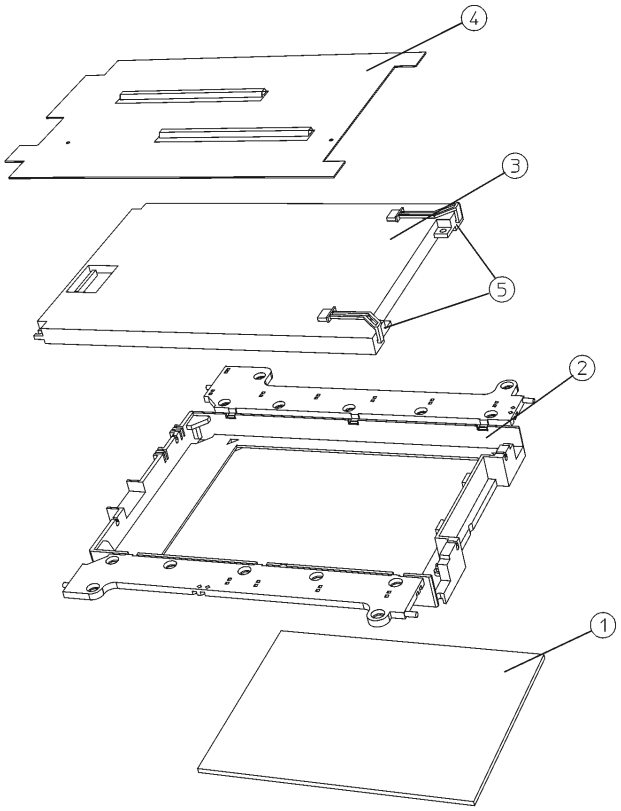


Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP100	89410-44702	9	1	GSKT BUMPER PCB PORON	28480	89410-44702
MP110	89410-04175	6	1	SHTF COVER-EMPTY SLOT # 2 STLN	28480	89410-04175
MP111	89410-04176	7	1	SHTF CVR-EMPTY SLOT # 1 STLN	28480	89410-04176
MP115	89410-01201	3	1	SHTF BKT-DISK AL	28480	89410-01201
MP120	89410-04110	9	1	SHTF CVR-10 BD ALSK	28480	89410-04110
MP121	89410-04120	1	1	SHTF CVR-21 BD ALSK	28480	89410-04120
	5180-0409	0	1	ASSY COVER SPRING CLIP	28480	5180-0409

Front Panel Parts

The reference designator for the nuts that fasten A11 to MP200 is MP612. The reference designator for the screws that fasten MP201 and A81 to MP200 is MP214. The reference designators for the screws that fasten the front panel to the chassis are MP217 and MP219.

Display Parts

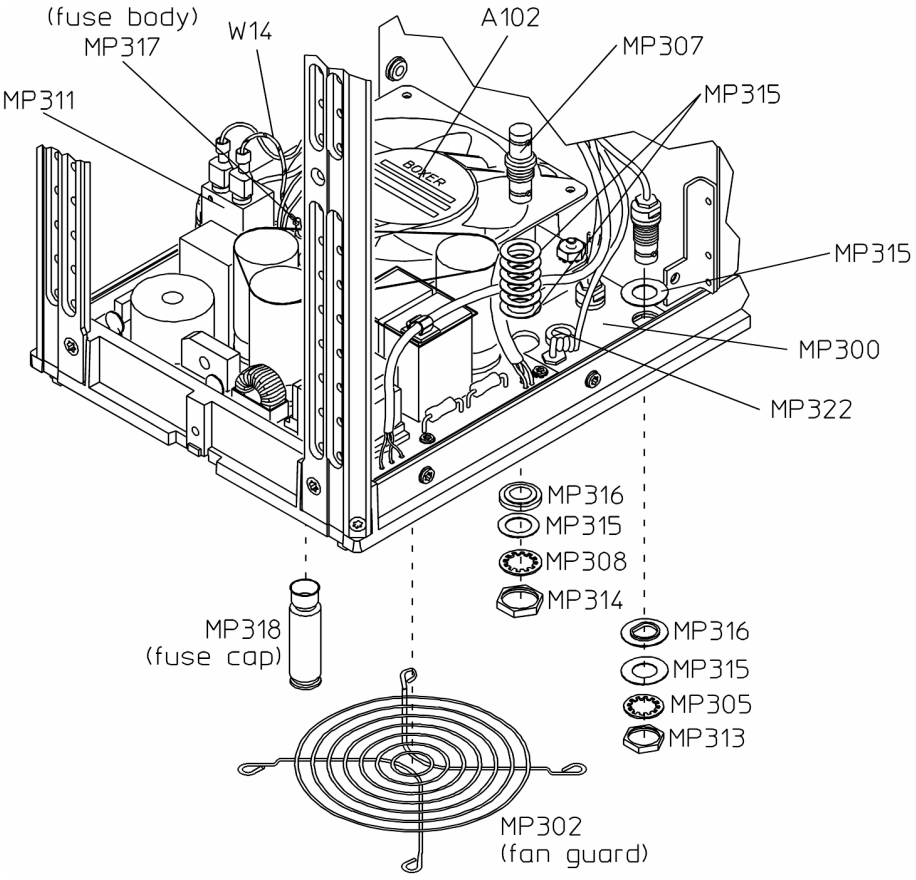


Item	Description	Agilent Part Number
1	Display EMI Filter	1000-1001
2	Display Mount	E4406-40004
3	FlatPanel Display	2090-0396
4	Display Shield Board (includes gaskets)	E4406-60052
5	Backlight	0960-1314

Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP200	89410-64333		1	PNL-FRT DRS ALPT	28480	89410-64333
MP201	89410-44304		1	MOLD-BEZEL	28480	89410-44304
MP204	89410-41903		1	KYPD ELASTOMERIC "89410A"	28480	89410-41903
MP205	89441-34315		1	PLT-NAME "89441A VECTOR SIGNAL"	28480	89410-34315
MP205	89410-34316		1	PLT-NAME "89441V VECTOR SIGNAL"	28480	89410-34316
MP205	89410-34315		1	PLT-NAME "89410A VECTOR SIGNAL"	28480	89410-34316
MP206	1250-2431	7	4	CON-ADAPT BNC-SMB PNL MNT	90949	903-430A518
MP207	08712-40005		1	MOLD RPG KNOB	28480	01650-47401
MP211	1251-4933	0	2	CONN-POST TYPE 2.5-PIN-SPCG CRP	27264	22-01-1033
MP212	3101-3014	1	1	SW— RKR	09328	WI32/ 217MZ
MP213	5041-5896	7	4	MOLD INSULATOR-CONN	28480	5041-5896
MP214	0515-0430	3	14	SCREW-MACHINE ASSEMPLY M3 X 0.5 6MM-LG	28480	0515-0430
MP217	0515-2039	2	1	SCR-MCH M3.5 8MM LG FHTX SST *	28480	0515-2039
MP219	0515-1946	8	8	SCR-MCH M3.0 6MM LG FHTX SST	28480	0515-1946
MP224	3050-0067	9	8	WASHER-FL MTLC 5/ 16 IN .375-IN-ID	73734	31-550
	0960-1314		1	DISPLAY BACKLIGHT	28480	0960-1314
	89410-00604		1	DISPLAY SHIELD	28480	89410-00604
	89410-01216		1	DISPLAY BRACKET	28480	89410-01216
	89410-04710		2	METAL SPACER	28480	89410-04710
	89410-00204		1	SUB PANEL	28480	89410-00204

Rear Panel Parts

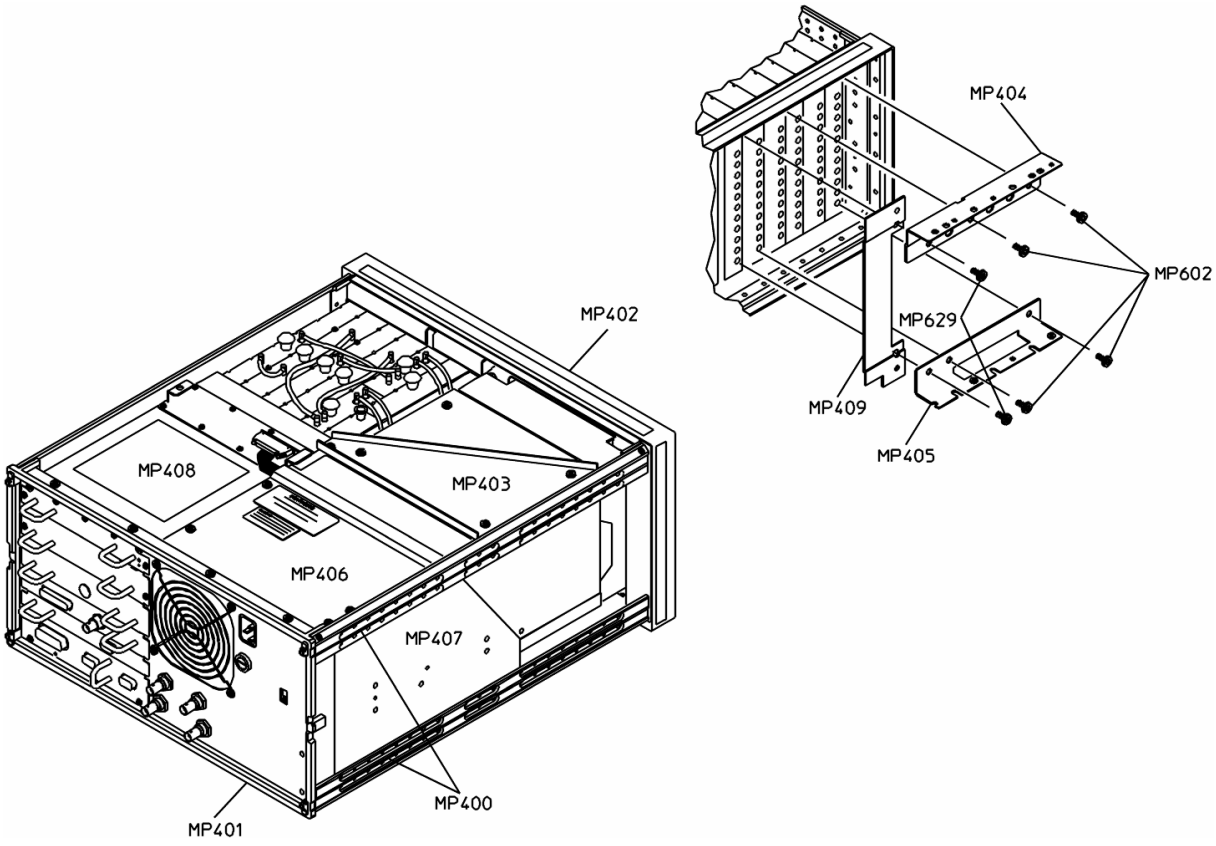
The reference designator for the screws that fasten the A96 Primary Power Supply assembly to MP300 is MP603. The reference designator for the screws that fasten MP311 and MP309 to MP300 is MP612. The reference designator for the screws and washers that fasten the fan and MP302 to MP300 is MP609 and MP613. The reference designators for the washers used with MP317 are MP319, and MP320.



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP300	89410-00201	1	1	SHTF PANEL-REAR ALSK	28480	89410-00201
MP302	3160-0562	2	1	FAN-GUARD	10938	08128
MP305	2190-0099	2	3	WASHER-LK INTL T 7/ 16 IN .472-IN-ID	28480	2190-0099
MP307	1250-0161	6	1	ADAPTER-COAX STR F-BNC F-BNC	28480	1250-0161
MP308	2190-0068	5	1	WASHER-LK INTL T 1/ 2 IN .505-IN-ID	28480	2190-0068
MP309	0360-0042	4	2	TERMINAL-SLDR LUG PL-MTG FOR-# 6-SCR	28480	0360-0042
MP310	8150-4556	6	1	JMPR 18GA GRNYEL 75MM 8x8	28480	8150-4556
MP311	9135-0136	9	1	FILTER-LINE FASTON-TERMS	S4307	FN 322-6/ 05
MP313	2950-0035	8	3	NUT-HEX-DBL-CHAM 15/ 32-32-THD	28480	2950-0035
MP314	2950-0054	1	1	NUT-HEX-DBL-CHAM 1/ 2-28-THD .125-IN-THK	28480	2950-0054
MP315	3050-0604	0	13	WASHER-FL MTLC 7/ 16 IN .5-IN-ID	86928	5710-94-16
MP316	5040-8313	5	4	MOLD WSHR-SH D-SHAPE	28480	5040-8313
MP317	2110-0543	3	1	FUSEHOLDER BODY EXTR PST; BAYONET; TND	H9027	FEC 031.1631
MP318	2110-0545	5	1	FUSEHOLDER CAP BAYONET; 6.3A 250V MAX	H9027	FEK031.1613
MP319	3050-0835	9	1	WASHER-FL NM 9/ 16 IN .63-IN-ID .75-IN-OD	28480	3050-0835
MP320	2190-0575	9	1	WASHER-LK INTL T 1/ 2 IN .64-IN-ID	28480	2190-0575
MP322	9170-1497	1	5	INC CORESHIELD BEAD	28480	9170-1497

Chassis Parts

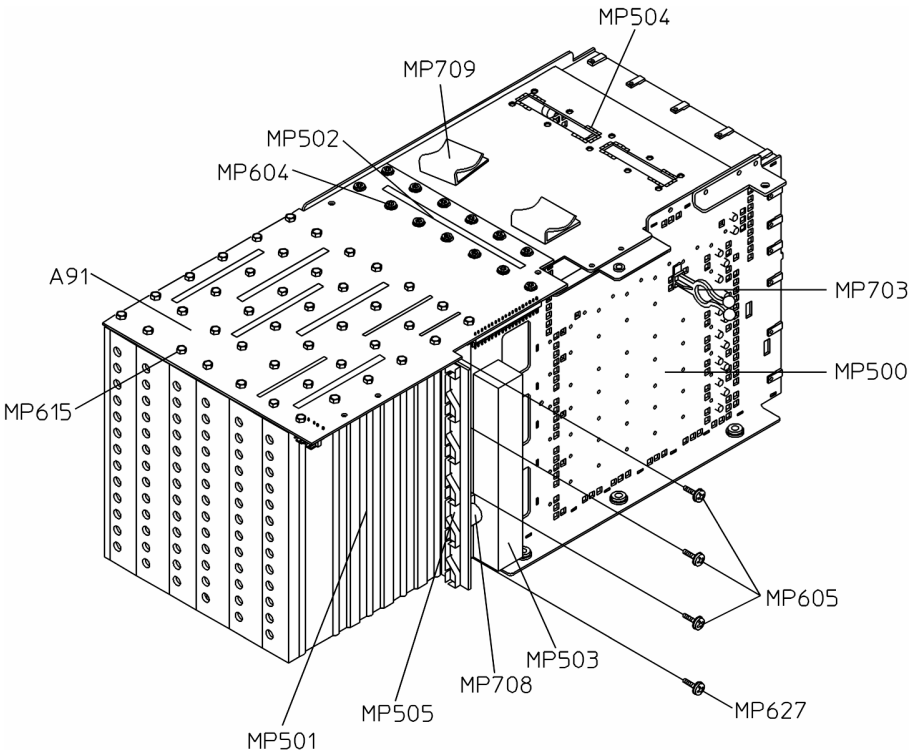
The reference designator for the screws that fasten MP403, MP406, MP407, A95 Main Power Supply assembly, and the rear panel to the chassis is MP605. The reference designator for the standoffs that fasten the A95 Main Power Supply assembly to the chassis is MP710. The reference designator for the screws and washers that fasten the black and red power cables to the chassis is MP623 and MP614. The reference designator for the screws that fasten MP401 and MP402 to the chassis is MP611. The reference designator for the screws that fasten MP404, MP405, A100 Display assembly, and A101 Disk Drive assembly to the chassis is MP630.



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP400	5021-5837	2	4	CSTG STRT-CRNR 497.8D II AL	28480	5021-5837
MP401	5021-5808	7	1	CSTG FRM-RR FM 221.5H II AL	28480	5021-5808
MP402	5022-1190		1	CSTG FRM-FRT FM 221.5H	28480	35650-46603
MP403	89410-01203	5	1	SHTF BKT-CRT AL	28480	89410-01203
MP404	89410-01210	4	1	SHTF BKT-CARDNEST FRONT TOP AL	28480	89410-01210
MP405	89410-01211	5	1	SHTF BKT-CARDNEST FRONT BTM AL	28480	89410-01211
MP406	89410-04101	8	1	SHTF COVER-PLENUM AL	28480	89410-04101
MP407	89410-01204	6	1	SHTF BKT-SIDE AL	28480	89410-01204
MP408	89410-34302	4	1	LBL CABELING ANALOG CARDNEST:K	28480	89410-34302
MP409	89410-01209		1	SHTF-BRACKET92 BRDFRONT	28480	89410-01209

Card Nest Parts

The reference designator for the screws that fasten the card nest to the rear panel is MP604.



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP500	89410-60101	6	1	SHTF ASSY-CARDNEST REAR AL	28480	89410-60101
MP501	89410-60603	3	1	MCHD-XTRU CARD NEST	28480	89410-60603
MP502	0905-0394	5	1	GSKT SEAL .10W	28480	0905-0394
MP503	89410-46702	3	1	GSKT-AIR DAM W/ ADH	28480	89410-46702
MP504	0400-0163	6	1	GROMMET-CHAN .109-IN-GRV-WD	06915	PGS-2
MP505	89410-01208	0	1	SHTF-BRKT92 BRDREAR	28480	89410-01208

Screws, Washers, and Nuts

Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP600	2950-0043	8	4	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	28480	2950-0043
MP601	2190-0016	3	6	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
MP602	0515-2008	5	4	SCR-MACH M SX.08 8MM LG	28480	0515-2008
MP603	0515-2145	1	7	SCREW-MACHINE M3.0 8MM LG PHTX SST	28480	0515-2145
MP604	0515-0372	2	41	SCREW-MACHINE ASSEMPLY M3 X 0.5 8MM-LG	28480	0515-0372
MP605	0515-0433	6	20	SCREW-MACHINE ASSEMPLY M4 X 0.7 8MM-LG	28480	0515-0433
MP609	0515-0383	5	4	SCREW-MACHINE ASSEMPLY M4 X 0.7 16MM-LG	28480	0515-0383
MP610	0515-1132	4	4	SCREW-MACH M5 X 0.8 10MM-LG	28480	0515-1132
MP611	0515-2086	9	16	SCR-SPC M4.0 7MM LG FHTX SST	28480	0515-2086
MP612	0535-0031	2	10	NUT-HEX W/LKWR M3 X 0.5 2.4MM-THK	28480	0535-0031
MP613	0535-0043	6	7	NUT-HEX W/LKWR M4 X 0.7 3.2MM-THK	06691	934KEPS-M4
MP614	2190-0004	9	2	WASHER-LK INTL T NO. 4 .115-IN-ID	28480	2190-0004
MP615	0515-1821	8	84	SCR-TPG M3.0 11MM LG HH STZN	28480	0515-1821
MP621	0515-0367	5	2	SCREW-MACHINE ASSEMPLY M2.5 X 0.45	28480	0515-0367
MP623	0515-2784	5	2	SCREW-SKT-HD-CAP M3 X 0.5 8MM-LG	28480	0515-0482
MP627	0515-0390	4	5	SCREW-MACHINE ASSEMPLY M4 X 0.7 6MM-LG	28480	0515-0390
MP629	0515-0386	8	2	SCREW-MACHINE ASSEMPLY M5 X 0.8 10MM-LG	28480	0515-0386
MP630	0515-1382	6	6	SCREW-MACH M3.5 X 0.6 6MM-LG	28480	0515-1382
	0380-0643		4	GPIB MOUNTING SCREW	28480	0380-0643
	2190-0586		4	GPIB WASHER	28480	2190-0586

Miscellaneous Parts

Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP703	1400-1547	3	2	CLP-CBL.4-.5DIA.NYL6/ 6	06915	STL-8-01-450
MP704	1400-0249	0	8	CABLE TIE .062-.625-DIA .091-WD NYL	56501	TY-23M-8
MP705	7120-3416	1	1	LABEL-WARNING 1.25-IN-WD 2.75-IN-LG	28480	7120-3416
MP706	7120-3528	6	2	LABEL-WARNING .6-IN-WD 1.8-IN-LG VINYL	28480	7120-3528
MP707	1400-0611	0	1	CLAMP-FL-CA 1-WD	76381	3484-1000
MP708	1400-1229	8	2	CLAMP-CABLE .375-DIA 1-WD NYL	34785	021-0375
MP709	1400-0611	0	2	CLAMP-FL-CA 1-WD	76381	3484-1000
MP710	0380-4035	5	4	STDF HEX 6MM M4.0X.737MM L SS	05791	SS5083-4070-37-01
MP720	5061-2819	8	1	DISK-TRANSPORTATION	28480	5061-2819
	89400-84401		1	FIRMWARE UPDATE KIT		
A82F1	2110-0965		1	FUSE-.5A125V TIME DELAY		
A30F1	2110-0892	5	1	FUSE-.125A125VSMT	75915	R459.125
A30F2	2110-0671	8		FUSE .125A 125V NTD .28X.096	75915	R251.125T1
A42B100	1420-0314	2	1	BATTERY 3V .16A-HR LITHIUM POLYCARBON	43744	BR-2325
A42F1	2110-0858	3	1	FUSE-2A 125V NTD BI UL-REC SMT	75915	R459002
A80F1	2110-0858	3	1	FUSE-2A 125V NTD BI UL-REC SMT	75915	R459002
A95F1	2110-0684	3	1	FUSE-2A 125V NTD .3X.103 UL	75915	R251002T1
A95F353	2110-0665	0	1	FUSE-1A 125V NTD .28X.096	75915	R251001T1
A95F357	2110-0684	3	1	FUSE-2A 125V NTD .3X.103 UL	75915	R251002T1
	2110-0342	0	1	FUSE 8A 250V NTD 1.25X.25 UL	71400	ABC-8
	2110-0055	2	1	FUSE 4A 250V NTD 1.25X.25 UL	75915	312 004

5 Circuit Descriptions

Circuit Descriptions

This chapter contains the overall instrument description and individual assembly descriptions for the Agilent 89410A DC-10 MHz Vector Signal Analyzer. The overall instrument description contains an overall block diagram and describes the following processes: measurement flow, measurement computation, system management, front-end setup, and triggering. The individual assembly descriptions give additional information for each assembly. For signal descriptions and information on voltage and signal distribution, see Chapter 6 “Voltages and Signals”.

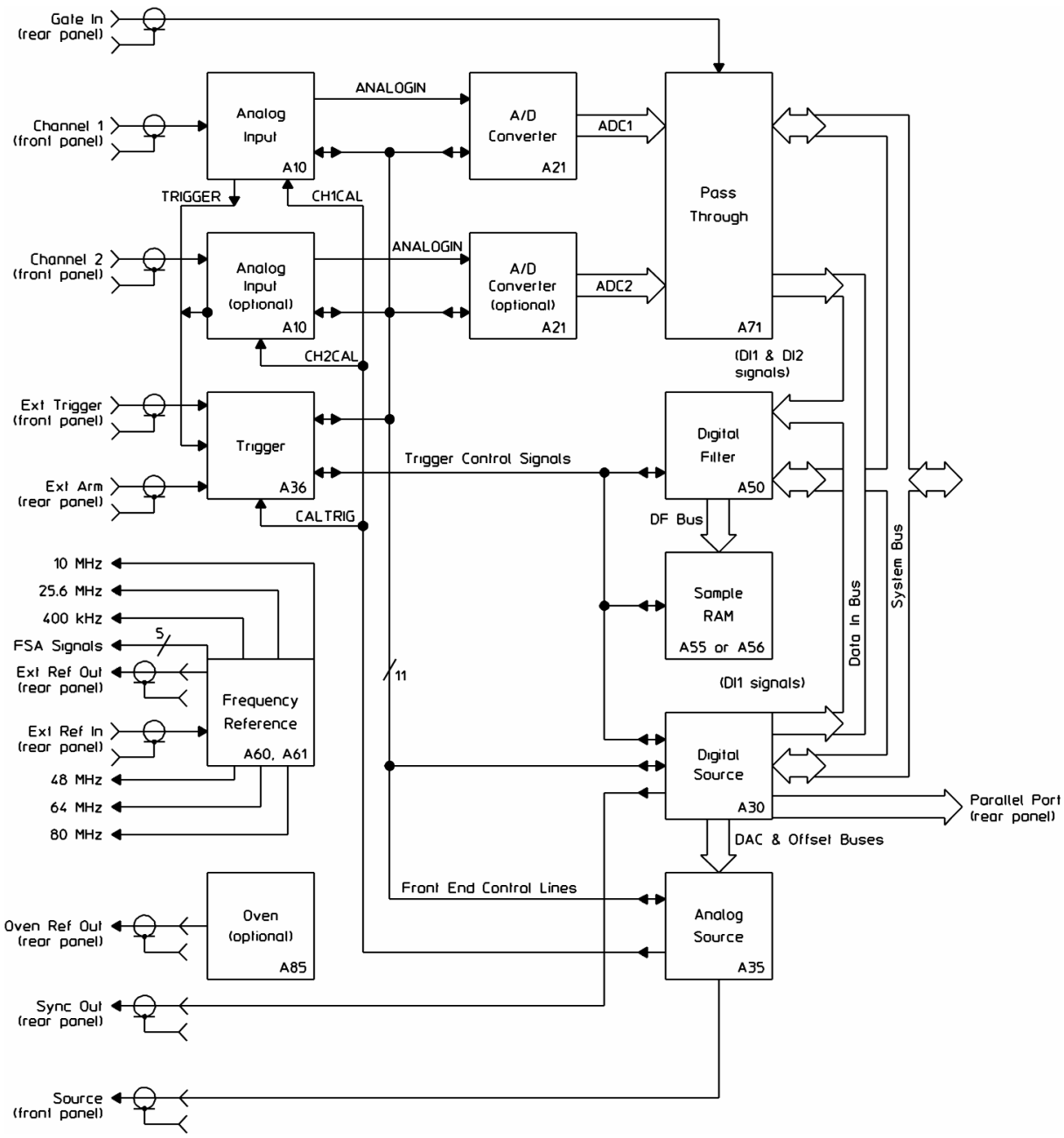
Overall Instrument Description

The Agilent 89410A DC-10 MHz Vector Signal Analyzer uses analog and digital circuits to make spectrum and network measurements. For frequency domain measurements, the analyzer uses the Fast Fourier Transform (FFT) algorithm. All measurement control, setup, and computations are performed by two processors—a CPU and a DSP. The CPU resides on the A40 CPU assembly and the DSP resides on the A47 DSP/Display Controller assembly. Nearly every assembly in the analyzer contains at least one gate array that is programmed at power-up or reset by the CPU assembly. The CPU and DSP/Display Controller assemblies talk to the other assemblies over the system bus. The system bus is used for programming, control, and measurement data transfer.

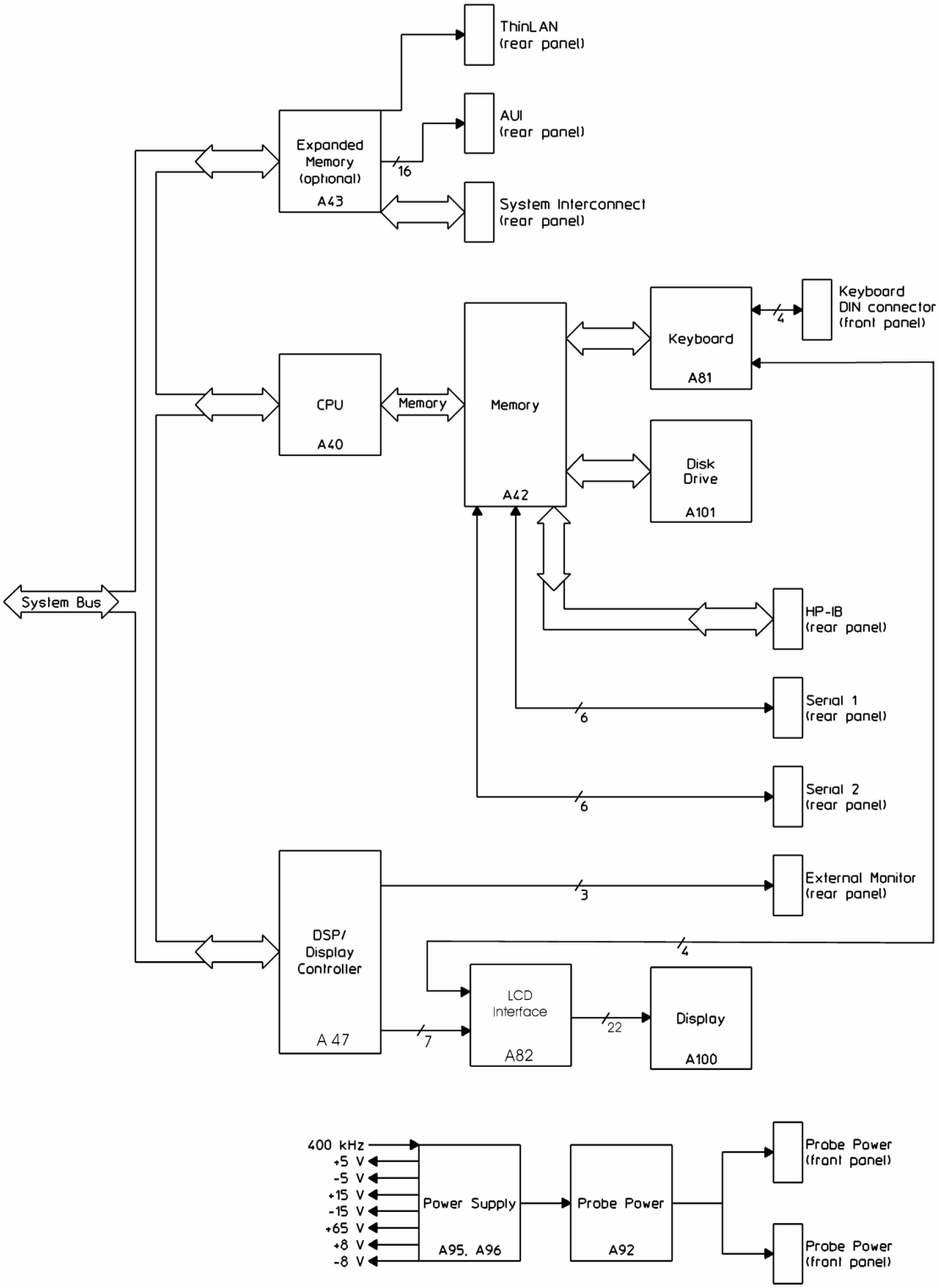
Overall Block Diagram

The following figure shows the overall block diagram for the analyzer. Each block in the diagram represents a function performed in the analyzer. The assembly (or assemblies) that perform the function are listed in the block.

Overall Block Diagram



Overall Block Diagram, continued



Input to Sample RAM

The input signal is first conditioned by the A10 Analog Input assembly. The Analog Input assembly sets the amplitude level, provides the selected input termination and anti-alias filtering. The Analog Input assembly sends the conditioned input signal to the A21 A/D Converter assembly over the ANALOGIN line. The Analog Input assembly also sends a conditioned version of the input signal over the TRIGGER line to the A36 Trigger assembly. The Trigger assembly uses the input signal for channel triggering and to detect over-range and half-range conditions.

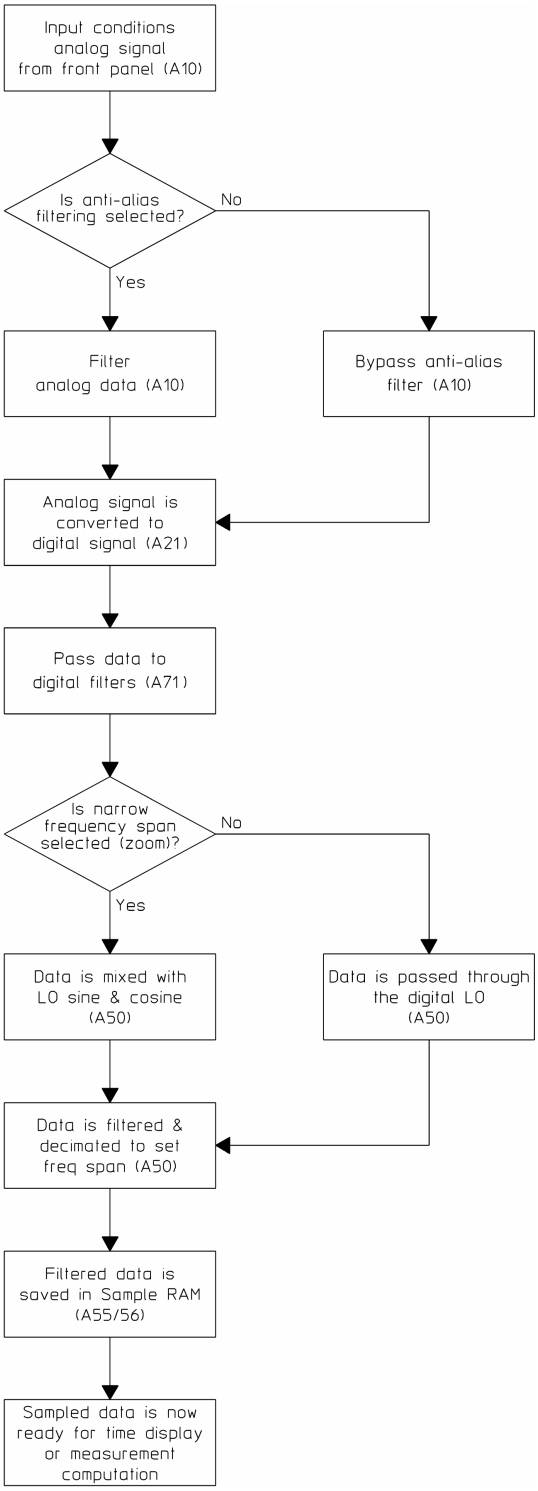
The A21 A/D Converter assembly converts ANALOGIN to parallel digital data. The rate the A/D Converter assembly samples data is determined by SMPLCLK (Sample Clock). SMPLCLK is a buffered version of the FSA (Frequency Sample) clock provided by the A60 Frequency Reference assembly. The A/D Converter sends the sampled digital data to the A71 Pass Through assembly over the 24-line ADC bus.

The A71 Pass Through assembly buffers the sampled digital data before sending the data to the A50 Digital Filter assembly over the Data In bus.

The A50 Digital Filter assembly filters the data and sends two separate sets of data (real and imaginary) for each channel to the A55 Sample RAM or optional A56 Expanded Sample RAM assembly over the DF Bus. During single channel measurements using channel 1, the Digital Filter assembly sends the channel 1 data through both its channel 1 and channel 2 paths. During single channel measurements using channel 2, the Digital Filter assembly sends the channel 2 data only through its channel 2 path.

The A55 Sample RAM or optional A56 Expanded Sample RAM assembly collects the filtered data and saves it in static RAM until it is instructed to transfer the data to the DSP for further processing. During single channel measurements using channel 1, the Sample RAM assembly saves the data in channel 2 RAM, then in channel 1 RAM after channel 2 RAM is full. During single channel measurements using channel 2, the Sample RAM assembly saves the data in channel 2 RAM.

Input to Sample RAM

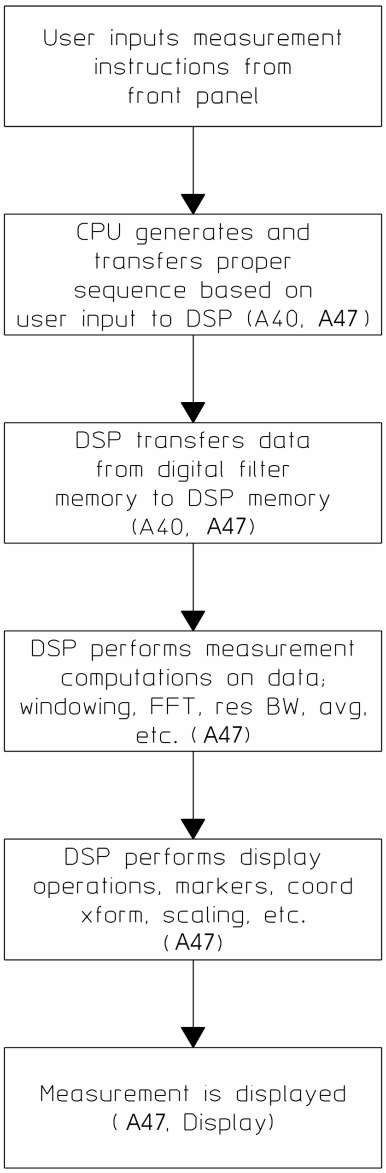


Measurement Computation

The A40 CPU assembly manages the measurement while the A47 DSP/Display Controller assembly performs the measurement computations and controls the display. The CPU assembly generates the measurement sequence based on the user input. The CPU assembly downloads the selected sequence to the DSP/Display Controller assembly. The DSP/Display Controller assembly runs the sequence until instructed by the CPU assembly to stop and do something else. Once a sequence is running, the DSP/Display Controller assembly is in control of the measurement process and the system bus.

The A47 DSP/Display Controller assembly transfers filtered data from the A55 Sample RAM or optional A56 Expanded Sample RAM assembly over the system bus. The DSP/Display Controller assembly performs the desired measurement computations on the data, for example: windowing, FFT, averaging, resolution BW reduction, spectral products. After the measurement computations are completed, the DSP/Display Controller assembly performs the display operations and displays the measurement.

Measurement Computations



System

The A40 CPU assembly is the system manager. The CPU assembly can determine if an assembly is loaded and active by requesting the assembly's identification number. During the power-up routine, the CPU assembly programs the gate arrays on the A50 Digital Filter, A30 Digital Source, A36 Trigger, A21 A/D Converter, and A55 Sample RAM or optional A56 Expanded Sample RAM assemblies. The CPU assembly's System Bus Arbiter controls who has control of the system bus—the A40 CPU or the A47 DSP/Display Controller assembly.

Instrument Memory

Memory for the analyzer resides in many locations. The A40 CPU assembly contains three types of memory: Flash Programmable ROM for its monitor ROM, Static RAM for the CPU stack, and dynamic RAM for multiple purposes including storing measurements. The A42 Memory assembly contains flash ROM for storing programs for both the A40 CPU assembly and the A47 DSP/Display Controller assembly. The DSP/Display Controller assembly contains static RAM for storing measurement data being processed and Video RAM for storing the data being displayed. The A55 Sample RAM or optional A56 Expanded Sample RAM assembly acts as FIFO memory for the A50 Digital Filter assembly. The Sample RAM assembly stores the filtered measurement data until the DSP/Display assembly is ready to process the data.

Front End Setup

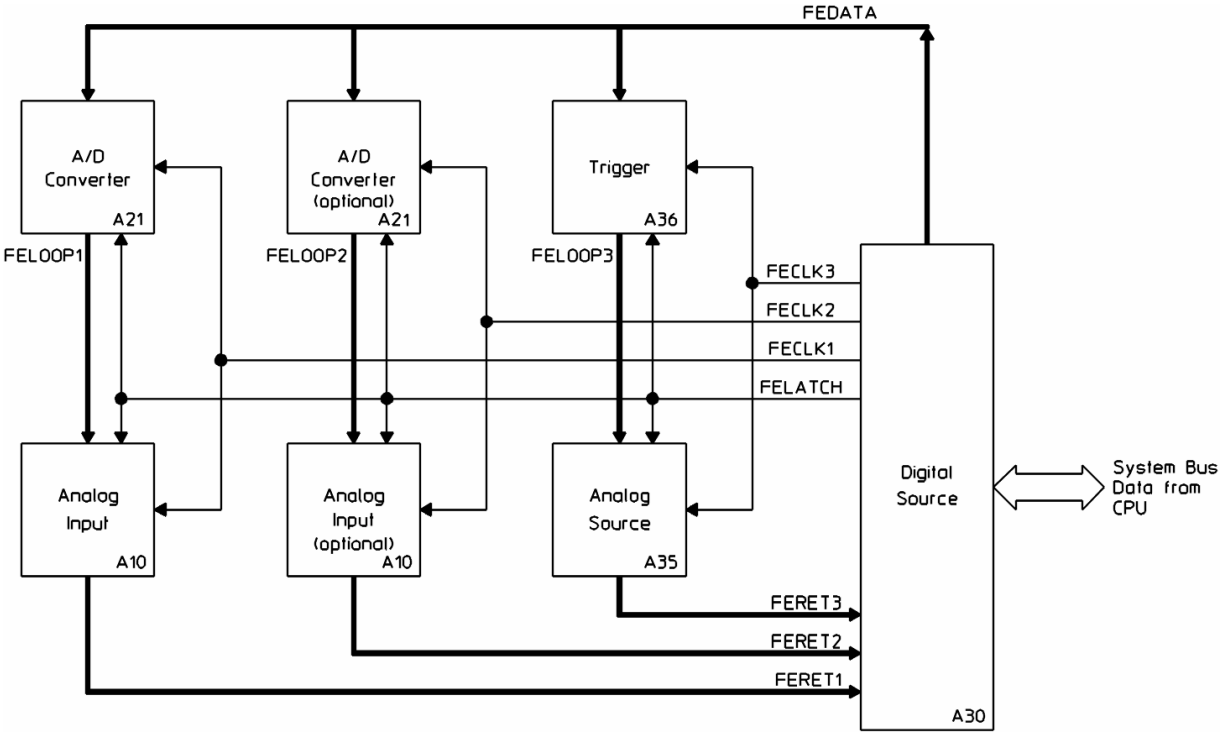
The A40 CPU assembly, via the system bus, programs the A30 Digital Source assembly and provides it with the data for the front-end control lines. The front end control lines program and setup the A10 Analog Input, A21 A/D Converter, A36 Trigger, and A35 Analog Source assemblies.

The A30 Digital Source assembly converts the parallel data from the A40 CPU assembly to serial data and sends the data to the A36 Trigger and A21 A/D Converter assemblies using the FEDATA line. The Trigger and A/D Converter assemblies transfer the data to the A35 Analog Source and A10 Analog Input assemblies using the FELOOP1, FELOOP2, and FELOOP3 lines. The Analog Source and Analog Input assemblies transfer the data back to the Digital Source assembly using the FERET1, FERET2, and FERET3 lines.

For example, to setup the channel 1 A10 Analog Input and A21 A/D Converter assemblies, the A30 Digital Source assembly outputs data over the FEDATA line. FECLK1 clocks FEDATA through the A/D Converter assembly to the Analog Input assembly via the FELOOP1 line. Once the data is in the proper position, the Digital Source assembly pulses the

FELATCH line which latches the data into the A/D Converter and Analog Input assemblies. To check for functional channel 1 Analog Input and A/D Converter assemblies, the Digital Source assembly clocks data through the channel 1 A/D Converter and Analog Input assemblies back to the Digital Source assembly via the FERET1 line. The Digital Source assembly then compares the data sent (FEDATA) to the data returned (FERET1).

Front-end Loops



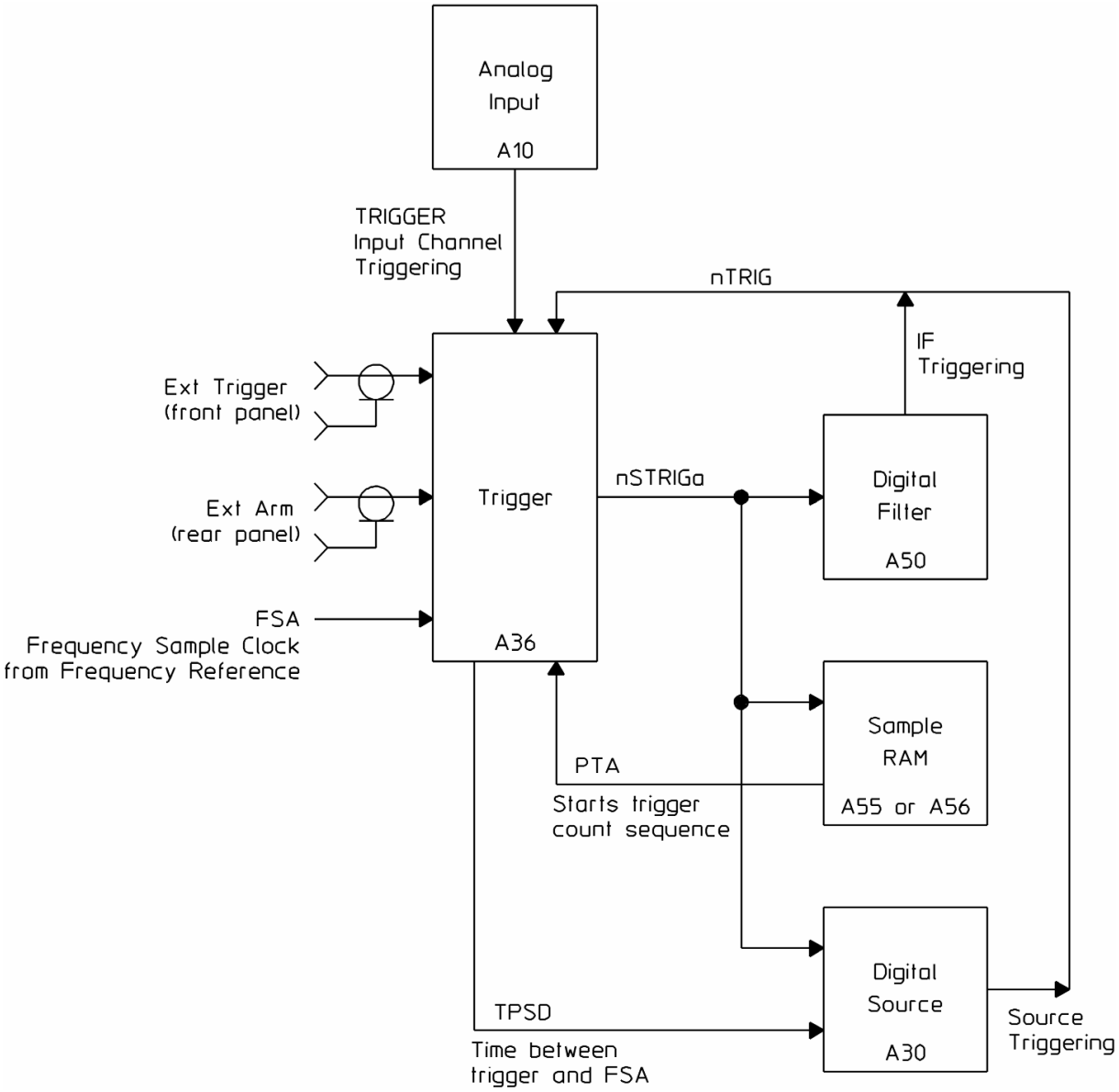
Triggering

The A36 Trigger assembly implements external trigger, external arm, source trigger, IF trigger, input channel trigger, and input over-range and half-range detection. The A30 Digital Source assembly provides the trigger (nTRIG) for source triggering. The A50 Digital Filter assembly provides the trigger (nTRIG) for IF triggering. The A10 Analog Input assemblies each provide a signal (TRIGGER) for input channel triggering and input over-range and half-range detection.

The triggering process starts when PTA (Pretrigger Acquired) goes high. The A55 Sample RAM or A56 Expanded Sample RAM assembly sets PTA high after it acquires enough data for pretriggering. After PTA goes high and the triggering conditions are met, the A36 Trigger assembly forces nSTRIGa (System Trigger Analog) low. A high-to-low transition on nSTRIGa synchronizes the operations on the A50 Digital Filter, A55 Sample RAM or optional A56 Expanded Sample RAM, and the A30 Digital Source assemblies with the trigger point. If HPIB triggering is selected, the A40 CPU assembly tells the Sample RAM assembly when to set the PTA signal high.

One of the main tasks of the A36 Trigger assembly is to count the time between the selected trigger and the frequency sample event (FSA2). The Trigger assembly starts counting on the first trigger point after receiving PTA from the A55 Sample RAM or A56 Expanded Sample RAM assembly. The Trigger assembly sends the count data to the A30 Digital Source assembly using the TPSD line. The Digital Source assembly then transfers the count data to the A40 CPU assembly over the system bus.

Trigger Signals



A10 Analog Input

The Analog Input assembly conditions the input signal before the A21 A/D Converter assembly converts the signal to digital data. The input signal can be a signal (0 Hz to 10 MHz) that is connected to the front panel input connector or the calibration signal from the A35 Analog Source assembly.

Front End Interface. Provides the control interface for the assembly.

Relay Drivers. Provide the control lines that open and close all the relays.

50/ 75 Ohm Input Termination. Allows the input signal to be terminated into either 50 or 75 ohms. If 50 or 75 ohm input impedance is not selected, the 1 Meg Buffer terminates the input signal into 1 Meg ohm.

Overload Detection. Detects overloads on signals terminated in 50 or 75 ohms. If an overload is detected, the Front End Interface informs the A30 Digital Source assembly.

Overload Protection. Disconnects the input signal if an overload is detected.

Signal Selection. Selects either the input signal or the calibrator signal.

Attenuator. Provides two 20 dB attenuator pads.

AC/ DC Couple. Provides ac or dc coupling.

1 Meg Buffer. Provides 1 Meg ohm input impedance.

3/ 13 dB Preamplifier. Amplifies the input signal by 3 dB or 13 dB.

DC Offset Correction DAC. Generates a dc offset voltage.

DC Offset Summing Amplifier. Sums the input signal with the dc offset voltage. The calibration routine determines how much dc offset voltage is needed to cancel the assembly's internal dc offset.

Gain Stages. Provide from 0 to 8 dB of signal amplification, in 2 dB increments.

Anti-Alias Filter & Bypass. Provide alias protection up to 10 MHz and a filter bypass path. The anti-alias filter is adjustable.

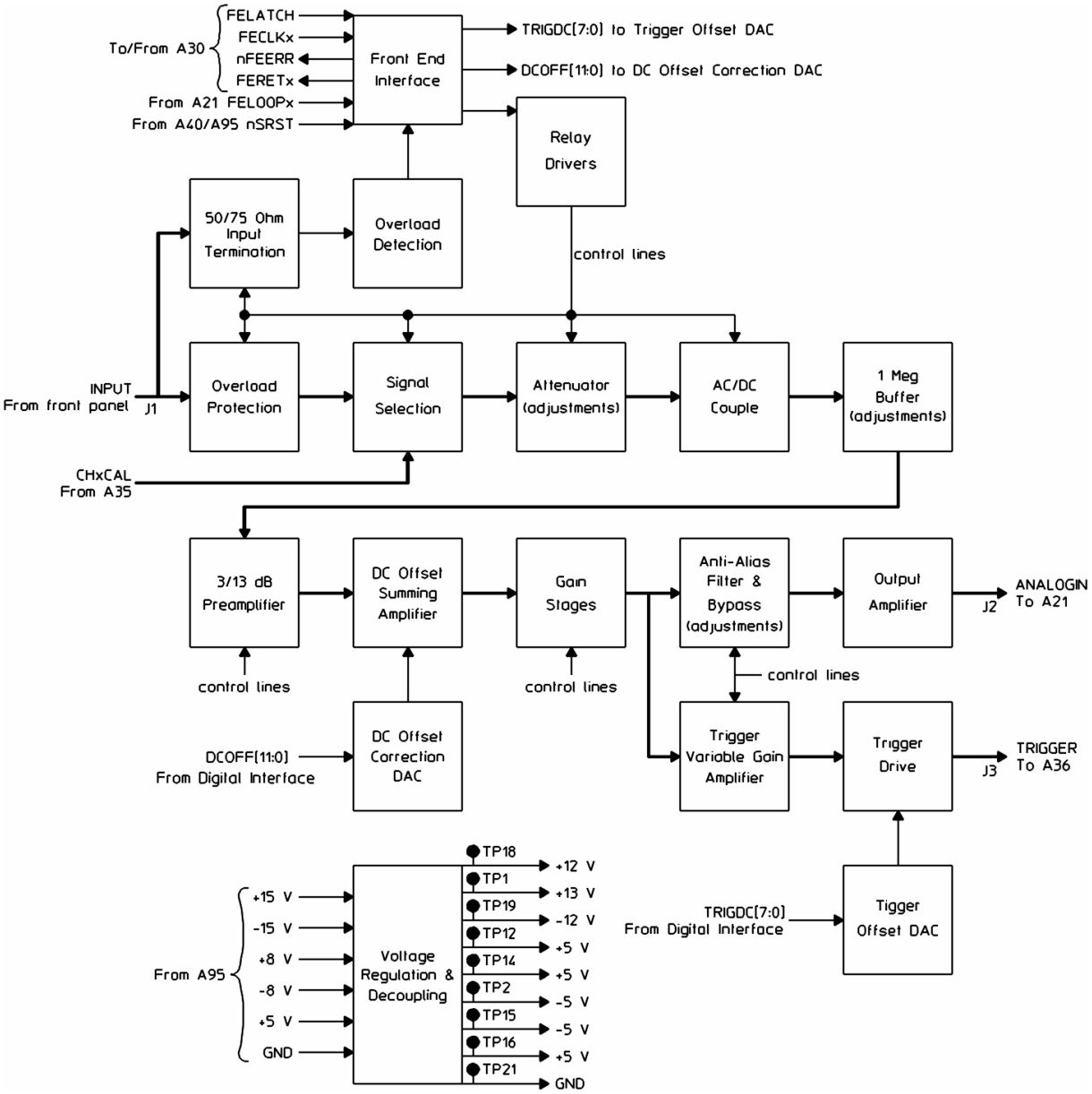
Output Amplifier. Provides the final amplification before the input signal is routed to the A21 A/D Converter assembly.

Trigger Variable Gain Amplifier. Amplifies the input signal by 6 dB or 12 dB.

Trigger Offset DAC. Generates a dc offset voltage.

Trigger Drive. Sums the input signal with the dc offset voltage. The output of the Trigger Drive is routed to the A36 Trigger assembly for input triggering and for over-range and half-range detection.

A10 Analog Input Block Diagram



A11 Front Panel Connector

The Front Panel Connector assembly provides RFI filtering for the front panel connectors' outer shell.

A12 Rear Panel Connector

The Rear Panel Connector assembly provides RFI filtering for the rear panel connectors' outer shell.

A21 A/ D Converter

The A/D Converter assembly converts the output of the A10 Analog Input assembly to digital data. The digital data is sent to the A71 Pass Through assembly.

Sample Clock Interface & Clock Generation. Changes the phase of the sample clock (SMPLCLK) providing all the clocks needed for timing.

Analog Summing Node. Adds dither to the analog input signal (ANALOGIN).

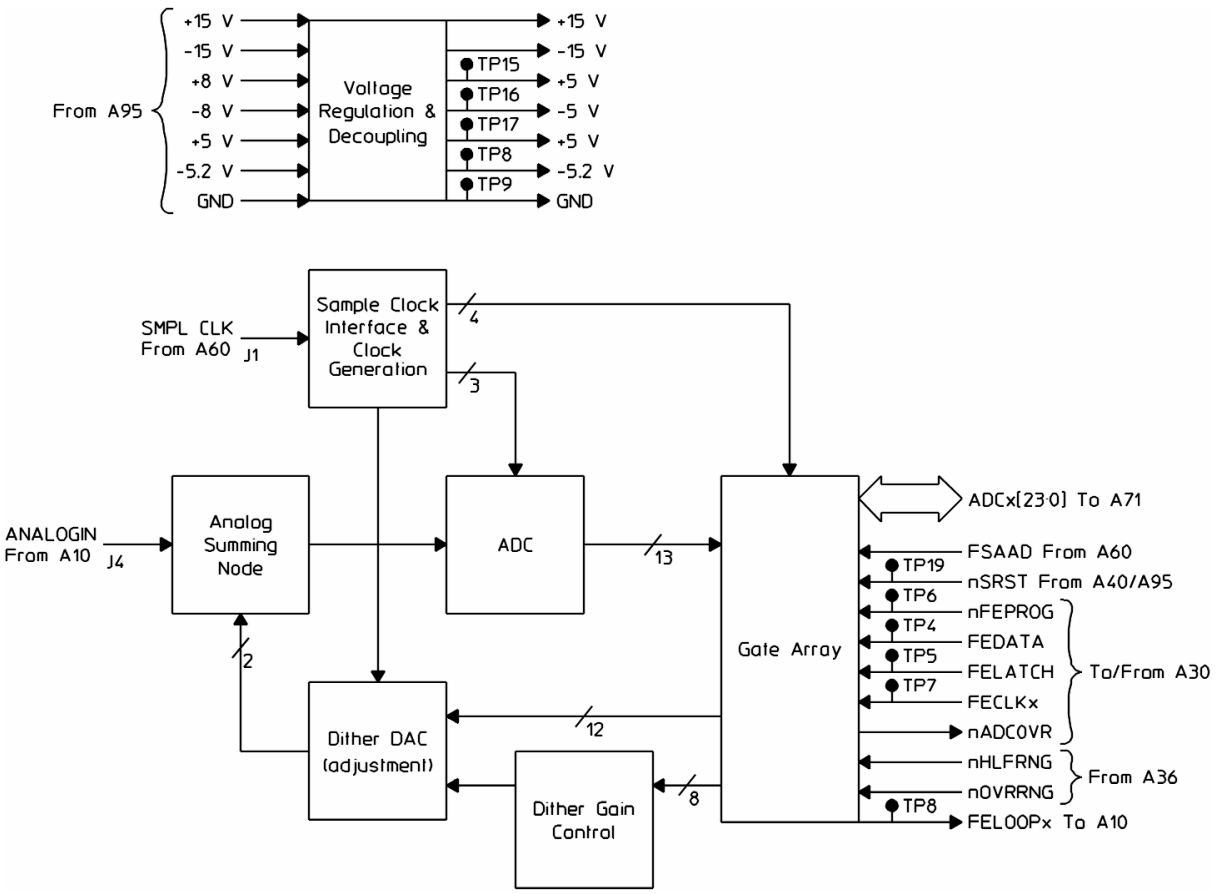
ADC. Converts the input signal to a 12-bit digital word at the sample clock rate.

Gate Array. Removes the dither that was added to the input signal. The input signal is then sent to the A71 Pass Through assembly. This circuit also interfaces with other assemblies in the front-end loop.

Dither DAC. Converts digital data from the Gate Array to dither (noise). This circuit is adjustable.

Dither Gain Control. Changes the reference voltage in the Dither DAC so the scaling matches the ADC.

A21 A/ D Converter Block Diagram



A30 Digital Source

The Digital Source assembly is one of two assemblies that together function as the analyzer's source. The Digital Source assembly provides digital data to the A35 Analog Source assembly. The Analog Source assembly converts the digital data to the analog source signal and the calibration signals.

Front End Interface. Controls the data loops that configure and program the front-end assemblies. This circuit also verifies that the assemblies in the front-end loop are functional.

Front End Status Interface. Monitors the status of the front-end assemblies. If input over-range, input half-range, ADC overload, or an error condition is detected, the System Bus Interface interrupts the assembly controlling the system bus.

System Bus Interface. Provides the interface between this assembly and the A40 CPU and A47 DSP/Display Controller assemblies.

Trigger Partial Sample Delay Data Interface. Provides the interface for receiving the TPSD counter value from the A36 Trigger assembly. This circuit also interfaces with the System Bus Interface.

Analog Source DC Offset Control. Generates the control lines that set the dc offset voltage on the A35 Analog Source assembly.

LO/ DF Synchronize Control. Synchronizes the local oscillators on the A50 Digital Filter assembly with the local oscillator on this assembly.

Centronics Controller. Allows the analyzer to send data to printers with Centronics interfaces.

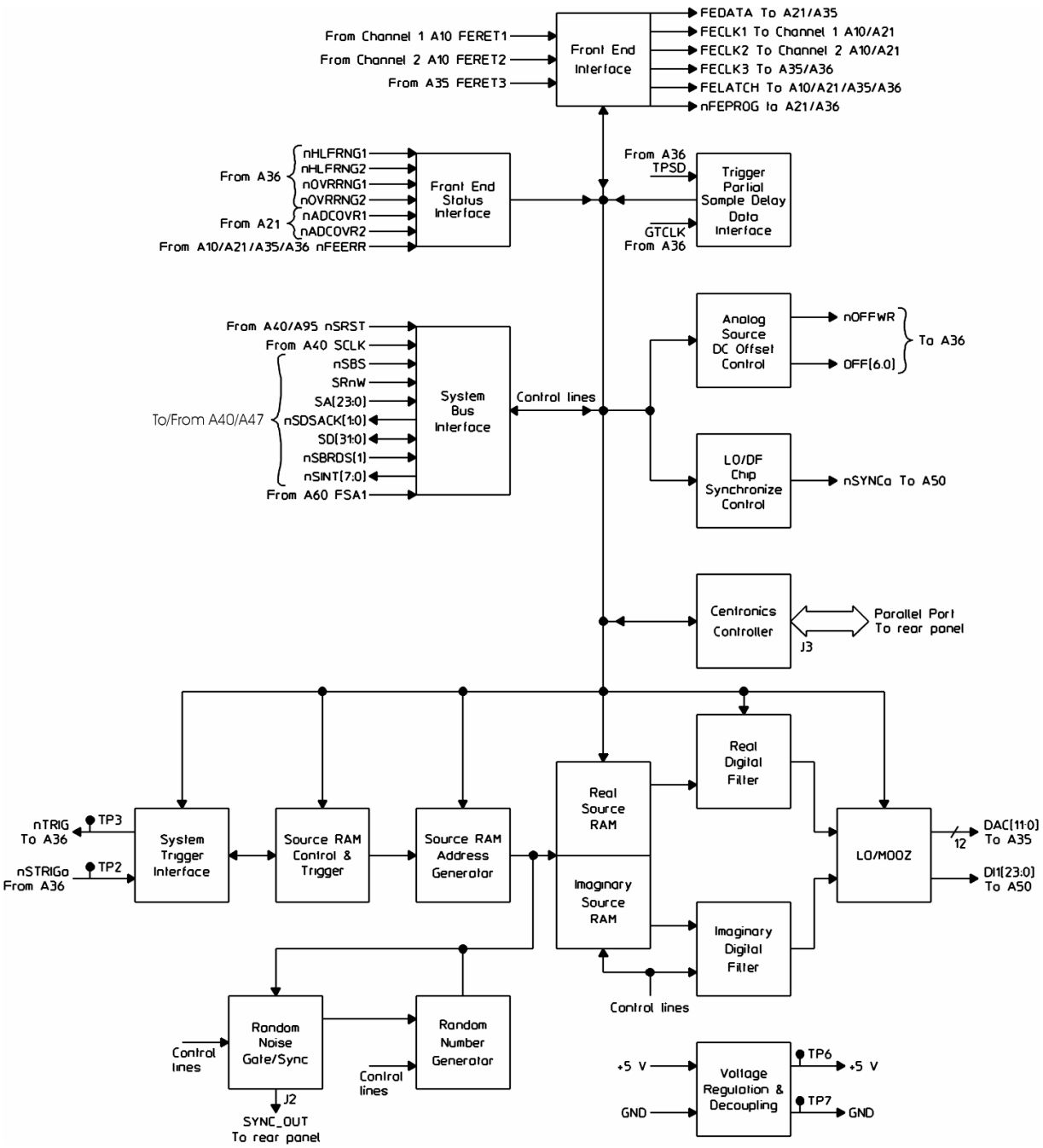
System Trigger Interface. Provides an interface between this assembly and the A36 Trigger assembly for trigger signals.

Source RAM Control & Trigger. Controls the Source RAM Address Generator. During triggered measurements, this circuit provides a programmable delay between the trigger and the start of the source output.

Source RAM Address Generator. Generates addresses for the Real and Imaginary Source RAM.

Random Number Generator. Generates a new pair of pseudo random numbers for each sample clock. The Real and Imaginary Source RAM outputs noise when addressed by this circuit.

A30 Digital Source Block Diagram



Random Noise Gate/ Sync. Provides gating control to the Random Number Generator. The Real and Imaginary Source RAM outputs burst random noise when the Random Number Generator is being gated by this circuit. This circuit also outputs a synchronizing signal to the rear panel.

Real Source RAM. Stores the real part of the waveform. The Source RAM Address Generator or the Random Number Generator selects the data output to the Real Digital Filter.

Imaginary Source RAM. Stores the imaginary part of the waveform if the source is operating in broadband (MOOZ) mode. The Source RAM Address Generator or the Random Number Generator selects the data output to the Imaginary Digital Filter.

Real Digital Filter. Filters the real source data.

Imaginary Digital Filter. Filters the imaginary source data.

LO/ MOOZ. Can filter and center the source data over a band limited range, or pass the source data through without filtering or shifting the frequency. The output of this circuit is the input for the A35 Analog Source assembly. This circuit also outputs data to the A50 Digital Filter assembly for internal diagnostics.

A35 Analog Source

The Analog Source assembly is the second of two assemblies that together function as the analyzer's source. The Analog Source assembly converts the digital data from the A30 Digital Source assembly to the analog source signal. The Analog Source assembly also provides precision amplitude calibration signals to the A10 Analog Input assemblies.

Front-End Interface. Interfaces with other assemblies in the front-end control loop.

Cal Trigger. Buffers DAC[0]. The resulting signal is a 1 V p-p square wave. The A36 Trigger assembly uses this signal to calibrate out calibrator delay.

Calibrator. ttenuates and conditions the 1 V p-p square wave to a square wave with a -17 dBm precision amplitude fundamental.

Waveform DAC. Converts the digital source data to an analog waveform. The waveform's amplitude can range from +1 V to -1 V.

10 M Hz Low Pass Reconstruction Filter. Limits the analog waveform's bandwidth and improves source rolloff. This circuit also contains a selectable path that bypasses the filter. This circuit contains a service adjustment.

DC Offset DAC. Converts digital data to a dc voltage. The dc voltage can range from +5 V to -5 V. This circuit also provides the reference voltages for the Waveform DAC.

Summer/ Buffer. Sums and scales the voltage from the DC Offset DAC with the signal generated by the Waveform DAC. The amplitude of the resulting signal ranges from +0.5 V to -0.5 V.

Source Output Amplifier. Amplifies the signal. The signal's amplitude can be up to 24 dBm.

Distortion Correction. Corrects signal distortion in the Source Output Amplifier.

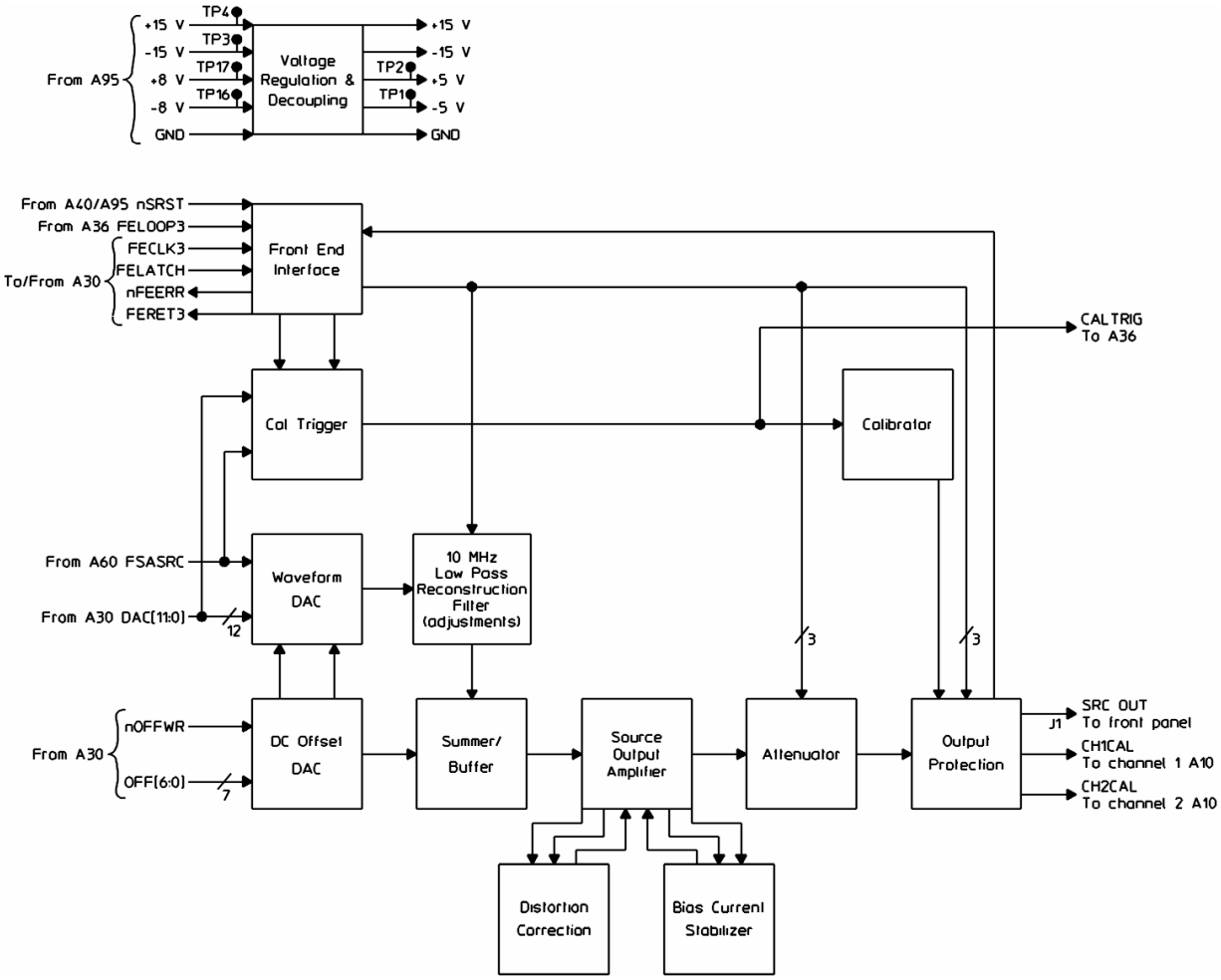
Bias Current Stabilizer. Stabilizes the bias current in the Source Output Amplifier.

Attenuator. Provides from 0 to 70 dB of signal attenuation, in 10 dB increments.

Output Protection. Protects the source from damaging voltages and connects the selected output signal to the selected signal path. If an

over-voltage condition is detected, this circuit disconnects the source signal connected to the front panel and informs the A30 Digital Source assembly. When the over-voltage condition is removed, this circuit reconnects the source signal to the front panel. This circuit connects either the calibrator or source signal to the front panel source BNC or to one of the A10 Analog Input assemblies. This circuit also provides either 50 or 75 ohm output impedance.

A35 Analog Source Block Diagram



A36 Trigger

The Trigger assembly generates the system trigger. This circuit also provides over-range and half-range detection for the A10 Analog Input assemblies.

Channel 1 Scaling. Buffers the channel 1 input signal. The input signal is routed to the Trigger Comparator for input triggering and to the Channel 1 Over-range/Half-range circuit for over-range and half-range detection.

Channel 1 Over-range/ Half-range. Determines if the channel 1 input exceeded its positive or negative half-range or over-range limit.

Channel 2 Scaling. Buffers the channel 2 input signal. The input signal is routed to the Trigger Comparator for input triggering and to the Channel 2 Over-range/Half-range circuit for over-range and half-range detection.

Channel 2 Over-range/ Half-range. Determines if the channel 2 input exceeded its positive or negative half-range or over-range limit.

External Trigger Input. Buffers the trigger signal connected to the front panel. The external trigger is routed to the Trigger Comparator for external triggering.

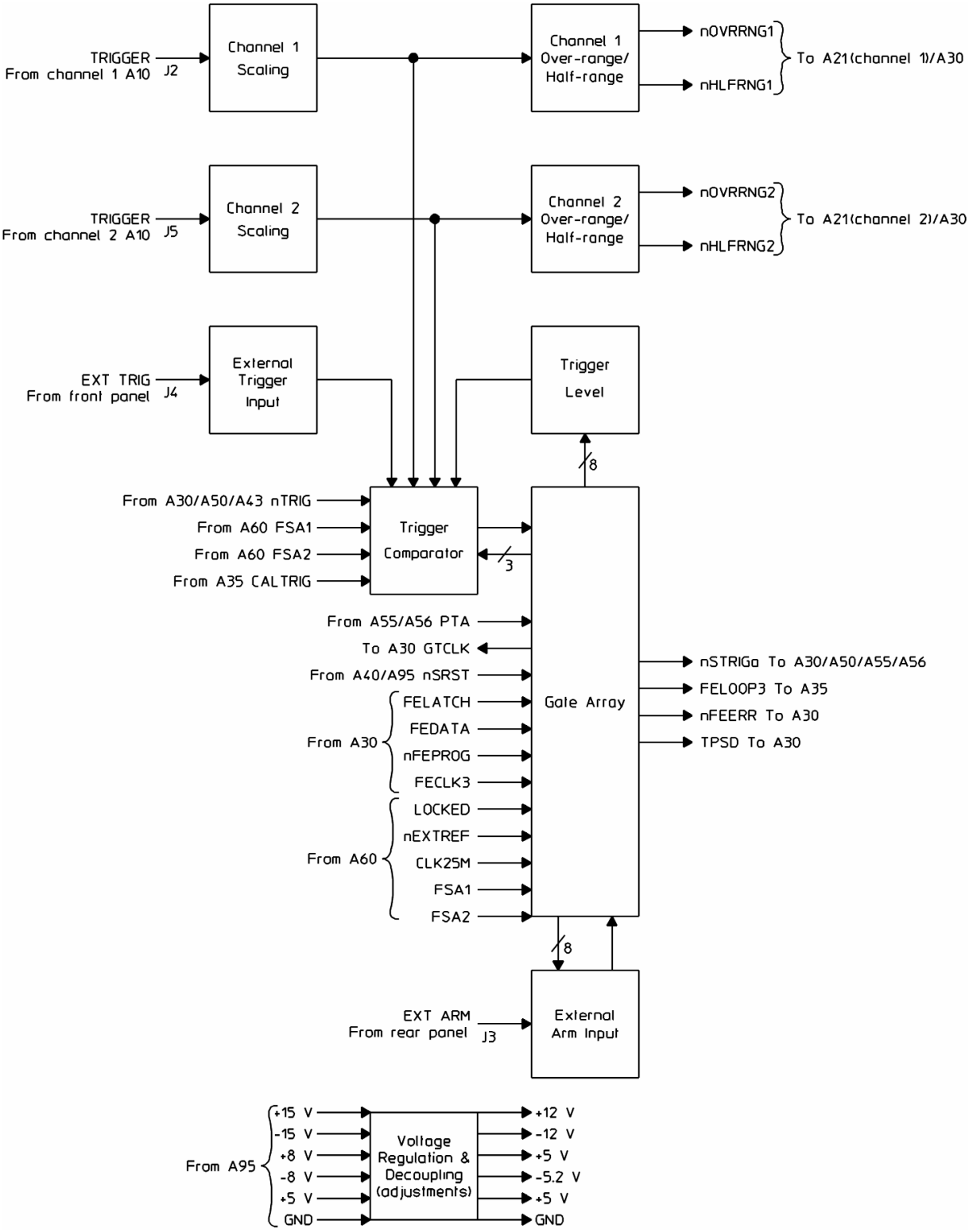
Trigger Level. Converts digital data from the Gate Array to a voltage.

Trigger Comparator. Compares the selected trigger to the voltage from the Trigger Level circuit. When the trigger exceeds the voltage, this circuit sends the trigger to the Gate Array.

Gate Array. Controls triggering and interfaces with the front-end assemblies.

External Arm Input. Sends an external arm to the Gate Array when the external arm input exceeds the voltage set by the Gate Array.

A36 Trigger Block Diagram



A40 CPU

The CPU assembly controls the entire analyzer. It performs multiple tasks, such as:

- Initiating the power-up sequence and calibration routines
- Configuring the measurement hardware
- Monitoring the hardware for faults or overloads
- Handling system bus arbitration
- Running the self tests

Bus Steering. Connects the CPU address and data bus to either the system address and data bus or the buffered address and data bus.

DRAM Controller. Controls and refreshes the DRAM circuit.

DRAM. Provides 4 megabytes of dynamic RAM.

System Bus Control. Controls the system bus. When requested by the A47 DSP/Display Controller assembly, this circuit can give the DSP/Display Controller assembly control of the system bus.

Clock Generation. Generates the system clock and the clocks for the A40 CPU and A42 Memory assemblies.

ID Register. Stores the assembly's type and revision code. The CPU & HW Reset circuit requests this information at power up.

SRAM Control. Selects the device in the Static RAM circuit.

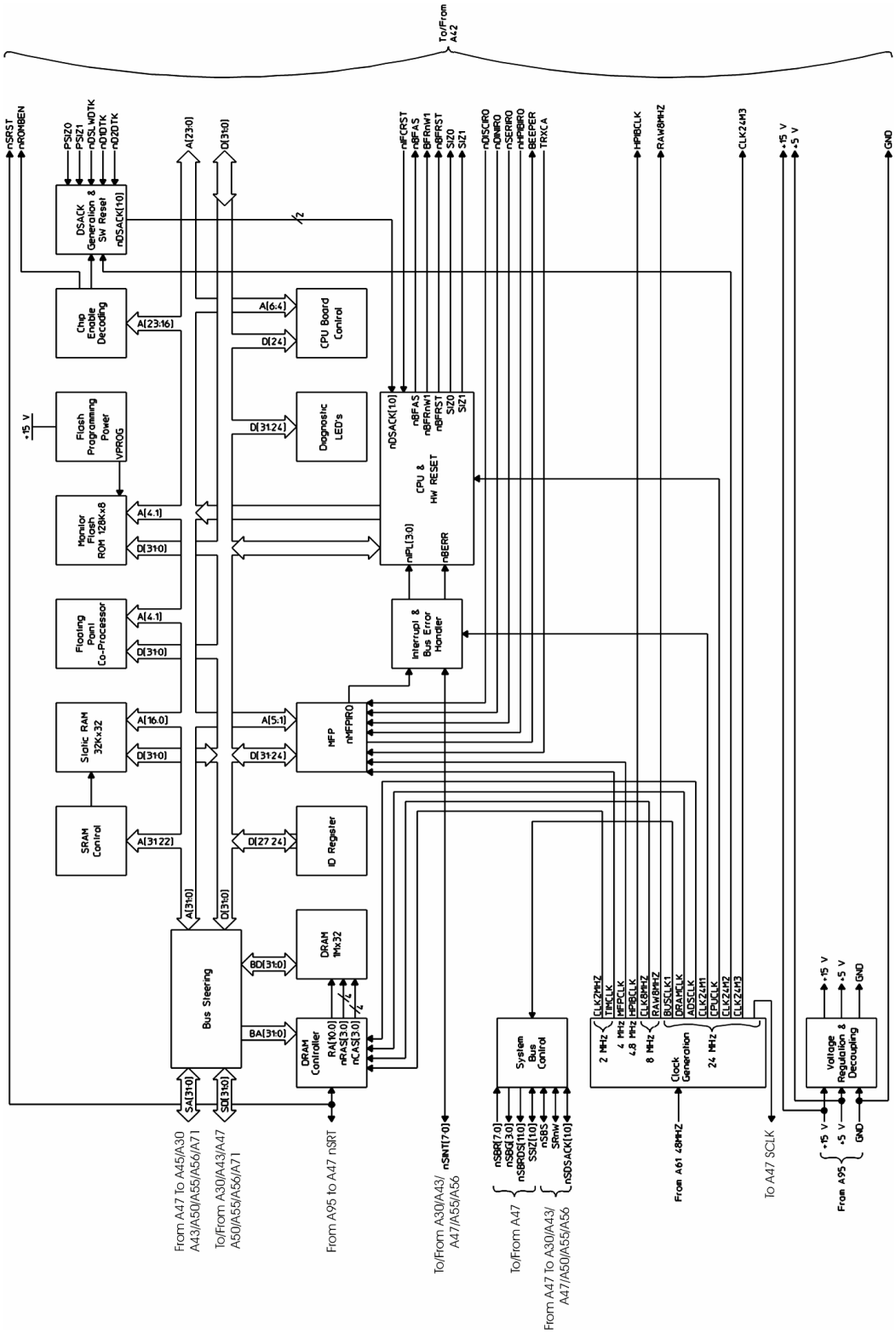
Static RAM. Contains four 32 kilobyte static RAM devices.

MFP (multiple function peripheral). Handles interrupts. When the MFP receives an interrupt, it interrupts the Interrupt & Bus Error Handler, which in turn interrupts the CPU & HW Reset circuit. The CPU & HW Reset circuit then reads a status byte from the MFP to determine the cause of the interrupt.

Interrupt & Bus Error Handler. Processes interrupts for the CPU. This circuit sets the interrupt priority level and returns an interrupt acknowledge to the circuit that generated the interrupt.

Floating Point Co-Processor. Performs floating point mathematical operations. This circuit works as a slave co-processor to the CPU & HW Reset circuit. This allows the CPU & HW Reset circuit to perform other functions while the Floating Point Co-Processor performs math-intensive operations.

A40 CPU Block Diagram



CPU & Hardware Reset. Controls the address and data busses and places the analyzer in a known state after receiving a reset. A reset occurs at power up and when the this circuit receives a reset instruction. After receiving a reset, this circuit initializes the analyzer from the information stored in Monitor Flash ROM. This circuit also processes interrupts from the Interrupt & Bus Error Handler. The CPU & HW Reset circuit has access to battery-backed CMOS on the A42 Memory assembly. This allows the A40 CPU assembly to store and update information such as the analyzer's address, default disk, and peripheral addresses.

Monitor Flash ROM. Stores the firmware used to initialize the analyzer.

Flash Programming Power. Provides a voltage that allows the Monitor Flash ROM circuit to be reprogrammed. This allows the firmware to be easily updated.

Diagnostics LEDs. Latch and display data lines for diagnostics. See chapter 1, Troubleshooting the Analyzer'' and chapter 7, ''Internal Test Descriptions'' for information on interpreting the diagnostic LEDs.

CPU Assembly Control. Enables or disables internal cache memory in the CPU & HW Reset circuit.

Chip Enable Decoding. Enables the data bus buffers on the A42 Memory assembly. When the Memory assembly's data bus buffers are enabled, the A40 CPU assembly's data bus (D[31:0]) and the Memory assembly's data bus (ROMD[31:0]) are connected together through the buffers.

DSACK Generation & SW Reset. Asserts nDSACK[1:0] based on the size of the operand and DSACK (data transfer and size acknowledgment) requests from the A42 Memory assembly.

A42 Memory

The Memory assembly provides the A40 CPU assembly with ROM, Flash ROM, NVRAM, a real-time clock, and interfaces to the front panel, flexible disk drive, COM 1 connector, COM 2 connector, and HPIB connector.

Bus Buffers. Connect the A42 Memory assembly's data bus to the A40 CPU assembly's data bus when enabled by the CPU assembly. The Bus Buffers also provide control and clock signals to the Device Select & Decode circuit and Beeper circuit.

Beeper. Provides an audible sound to prompt the user. The Beeper can be turned off.

Device Select & Decode. Provides address decoding for various circuits.

ID Register. Stores the assembly's type and revision code. The A40 CPU assembly requests this information at power up.

Flash Program ROMs. Store the analyzer's program code.

Flash Program Voltage. Provides a voltage that allows the Flash Program ROMs to be reprogrammed. This allows the analyzer's program code to be easily updated.

ROM Board Control Registers. Provide single bit read/write registers for control lines to and from HPIB, Disk Drive, and Flash ROM.

Battery & Control Circuit. Provides battery backup for the Real Time Clock and Non-Volatile CMOS RAM.

Real Time Clock. Keeps track of the current time and data.

Non-Volatile CMOS RAM. Stores the following user-accessible states. These states are unchanged by power-up or [**Preset**].

[**Display**]
[more display setup]
[color setup]
[contrast]
[brightness]
[color #]
[hue]
[saturation]
[luminosity]
[**Disk Utility**]
[default disk]
[**Plot/ Print**]
[plot/ print setup]
[plotter pen setup]
[**Local/ Setup**]
[system controller]
[addressable only]
[analyzer adrs]
[peripheral addresses]
[plotter adrs]
[printer adrs]
[ext disk adrs]
[ext disk unit]
[Serial 1 setup]
[Serial 2 setup]
[**System Utility**]
[auto cal]
[keyboard type]
[time/ date setup]
[beeper]

Floppy & FIFO Controller. Allows the analyzer to store or retrieve data from the internal 3.5-inch flexible A101 Disk Drive assembly. It provides all the control signals necessary to operate the Disk Drive assembly.

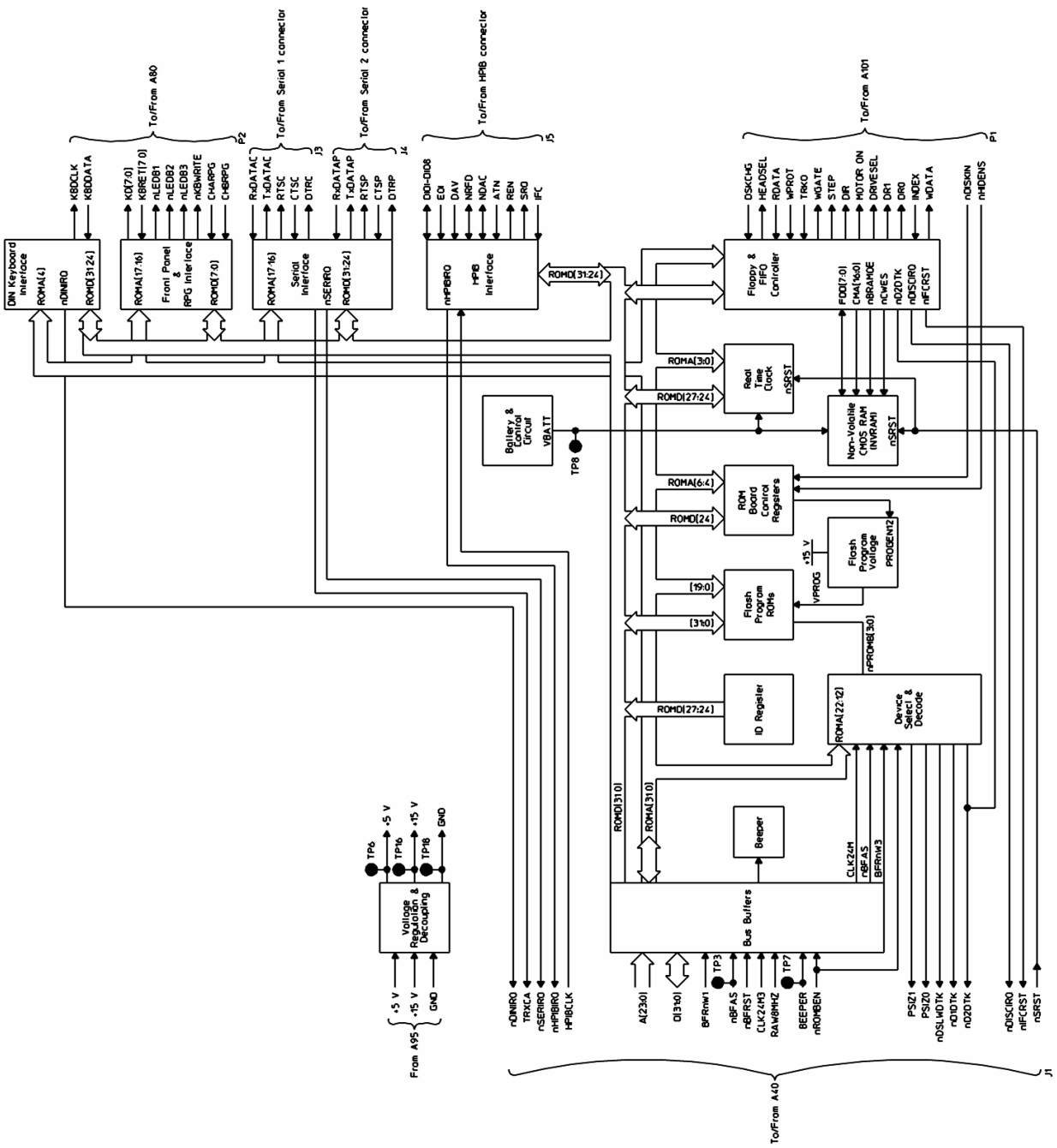
HPIB Interface. Allows the analyzer to communicate with other devices such as plotters, printers, or a host computer via an HPIB cable. This circuit handles all HPIB functions for the analyzer.

Serial Interface. Allows the analyzer to communicate with printers and plotters. This circuit handles all serial port functions for the analyzer.

Front Panel & RPG Interface. Provides the interface to the A80 Keyboard assembly.

DIN Keyboard Interface. Provides the interface to the optional PC style keyboard. The DIN connector for the optional keyboard is on the A80 Keyboard assembly.

A42 Memory Block Diagram



A43 Expanded Memory

The Expanded Memory assembly provides a dual port DRAM, a LAN interface, flash EPROM, non-volatile memory, and an HPIB interface.

Address Buffer. Buffers the system bus address lines.

Data Buffer. Buffers the system bus data lines.

Interface Control. Provides the interface between this assembly and the A40 CPU and A47 DSP/Display Controller assemblies.

DRAM. Provides 4 megabyte of dynamic RAM and can be expanded by plugging in a 4, 8, or 16 megabyte SIMM module. This circuit is configured in a dual port mode, accessible from both the system bus and the LAN circuit. The memory can be configured to be located at any arbitrary 4 megabyte boundary in the address space.

DRAM Controller. Controls and refreshes the DRAM circuit.

Flash ROM. Provides 512 kilobytes of flash EPROM.

Non-volatile memory. Provides 1024-bit serial non-volatile memory for storing setup information (for example, the LAN address).

LAN. Provides a local area network (LAN) interface. This circuit has access to one port of the DRAM.

AUI. Provides an AUI port for connection to the users LAN.

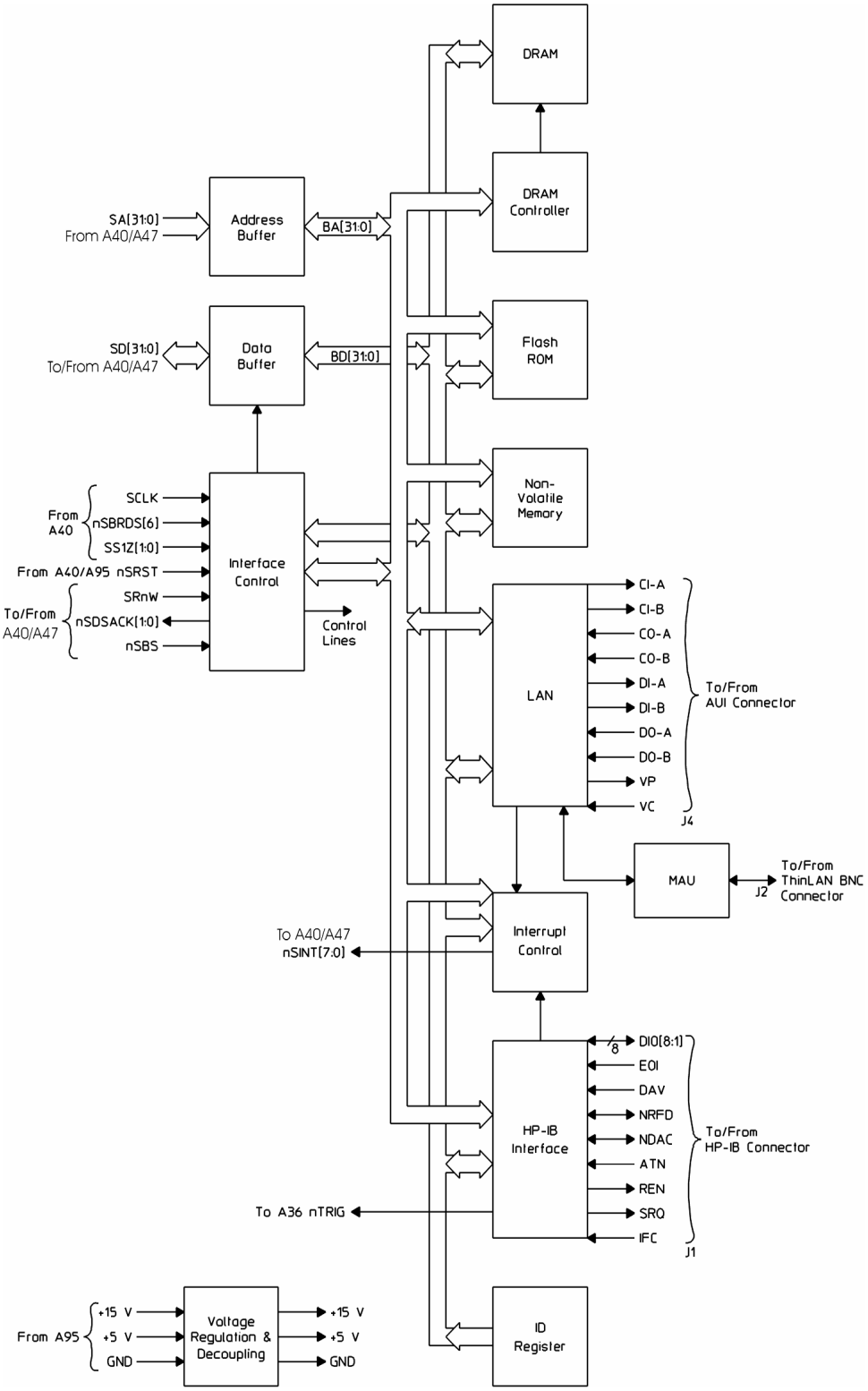
MAU. Provides a ThinLAN BNC port for connection to the users LAN.

Interrupt Control. Interrupts the assembly controlling the system bus.

HPIB Interface. Allows the analyzer to communicate with the RF or microwave spectrum analyzer that is used with the Agilent 89411A Down Converter. This circuit also provides an HPIB trigger to the A36 Trigger assembly.

ID Register. Stores the assembly's type and revision code. The A40 CPU assembly requests this information at power up.

A43 Expanded Memory Block Diagram



A47 DSP/ Display Controller

The DSP/Display Controller assembly handles data transfers, transforms the data for different display types, and controls the A100 Display assembly.

Control Logic. Interfaces with other assemblies on the system bus and provides the control lines to the circuits in this assembly. This circuit can request and be given control of the system bus.

Clock Generator. Generates a 20 MHz and a 32 MHz clock. These clocks provide timing for this assembly.

Host/ Assembly Data Transceivers. Buffer the system bus data lines.

Host/ Assembly Address Transceivers. Buffer the system bus address lines.

ID Register. Stores the assembly's type and revision code. The A40 CPU assembly requests this information at power up.

Control Register. Stores control bits for circuits in this assembly.

DSP Address Transceivers/ Latches. Buffer and latch the buffered system bus address lines.

DSP Data Transceivers/ Latches. Buffer and latch the buffered system bus data lines.

DSP (digital signal processor). Transforms data for different display type and stores the data in the A RAM and B RAM circuits. This circuit is a floating point math processor.

A RAM. Stores data from the DSP. Part of the memory in the A RAM circuit is reserved for accesses to the system bus.

B RAM. Stores data from the DSP.

Host/ GSP Data Transceivers. Buffer the buffered data lines and place the graphics data in VRAM.

GSP (graphics system processor). Provides the address and strobe lines for the VRAM circuit and the horizontal and vertical synchronize lines.

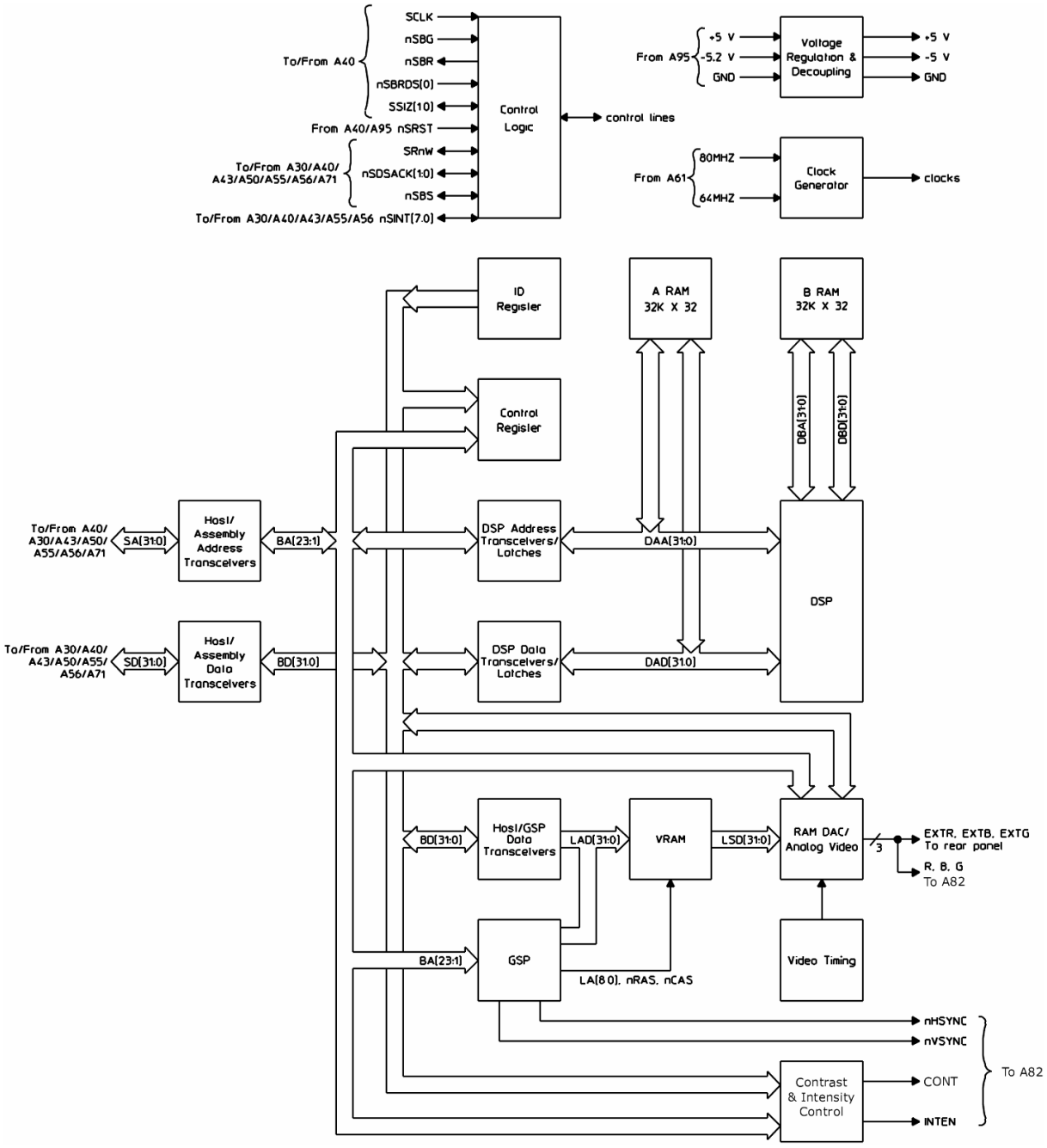
VRAM (video RAM). Stores the graphics data.

RAM DAC/ Analog Video. Converts the data in VRAM to analog signals. The analog signals contain red, blue, and green video information.

Video Timing. Provides the timing for the RAM DAC/Analog Video circuit.

Contrast& Intensity Control. Sets the display contrast and intensity brightness.

A47 DSP/ Display Controller Block Diagram



A50 Digital Filter

The Digital Filter assembly mixes, decimates, and filters the digital input data from the A71 Pass Through assembly. This assembly can also provide an IF trigger to the A36 Trigger assembly.

Clock. Provides all the timing clocks for this assembly.

System Bus Interface. Provides the interface between this assembly and the A40 CPU and A47 DSP/Display Controller assembly.

LO/ DF Chip Synchronize Control. Provides the synchronizing signals for this assembly.

Input Buffer. Buffers the channel 1 input data from the A71 Pass Through assembly. During diagnostics, the A30 Digital Source assembly's output can be the input for this circuit.

Input Buffer/ MUX. Buffers the channel 1 or channel 2 input data from the A71 Pass Through assembly. During two channel measurements, this circuit buffers the channel 2 input data. During single channel measurements, this circuit buffers the input data from the selected channel (either channel 1 or channel 2). During diagnostics, the A30 Digital Source assembly's output can be the input for this circuit.

LO. Mixes the input data into complex real and imaginary data. This circuit can also provide additional decimation on the complex data.

Real Digital Filter. Filters and decimates the real data from the LO.

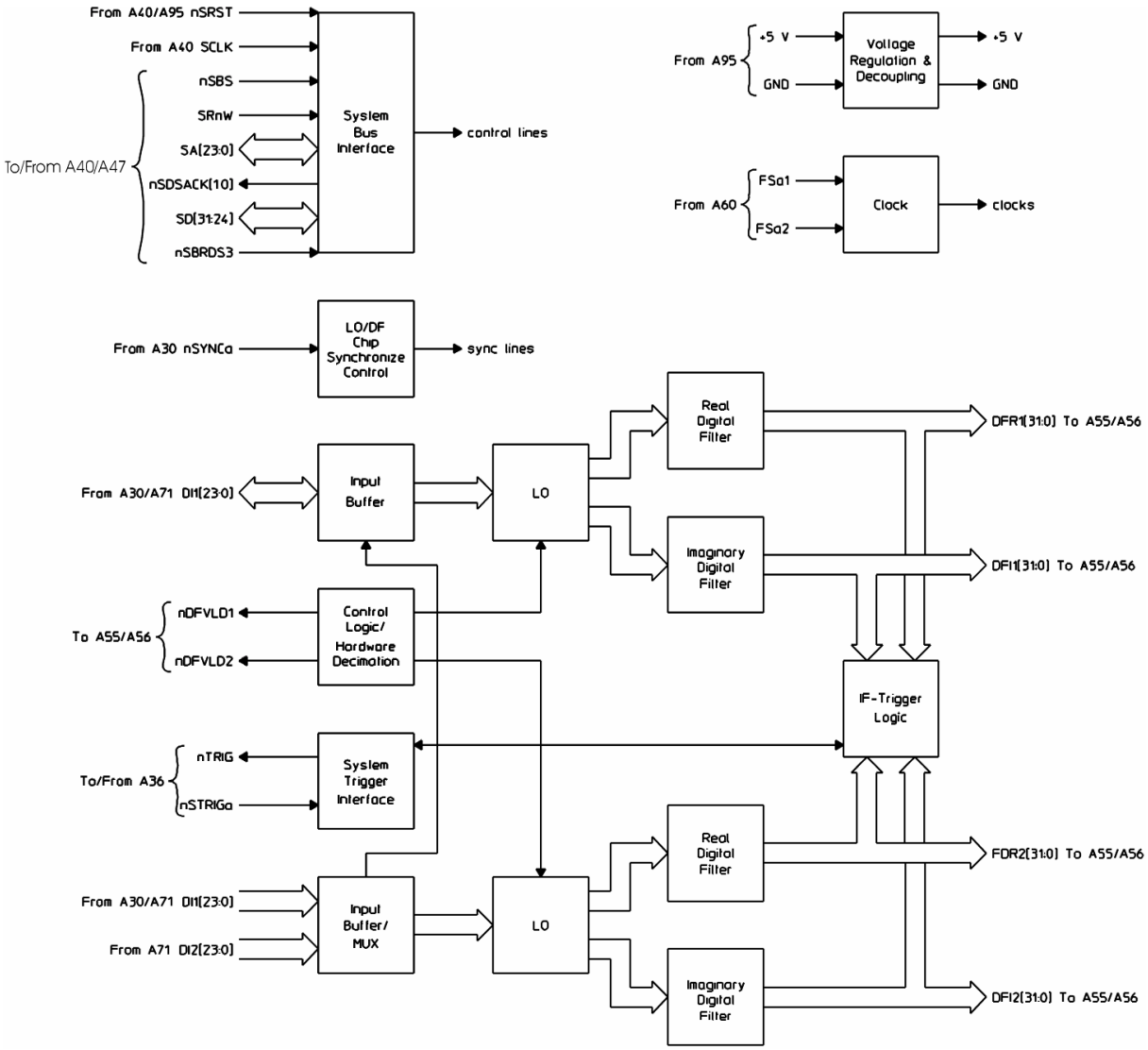
Imaginary Digital Filter. Filters and decimates the imaginary data from the LO. The output of this circuit is only used in zoom mode.

Control Logic/ Hardware Decimation. Informs the A55 Sample RAM or optional A56 Expanded Sample RAM assembly when the output data from the Digital Filter circuits is valid. This circuit also provides control lines to the LO circuits for additional decimation.

System Trigger Interface. Provides the interface to the A36 Trigger assembly for trigger signals.

IF-Trigger Logic. Can detect a trigger in a selected frequency band. If IF triggering is selected, this circuit tells the System Trigger Interface circuit when the trigger occurs.

A50 Digital Filter Block Diagram



A55 Sample RAM / A56 Expanded Sample RAM

The Sample RAM or optional Expanded Sample RAM assembly performs data-acquisition on the input data from the A50 Digital Filter assembly. The Sample RAM assembly provides 512 kilobytes of RAM and the Expanded Sample RAM provides 8.192 megabytes of RAM.

Latch Buffer Real 1. Latches the digital data that represents the real portion of the channel 1 input signal.

Latch Buffer Imaginary 1. Latches the digital data that represents the imaginary portion of the channel 1 input signal.

Latch Buffer Real 2. During two channel measurements, this circuit latches the digital data that represents the real portion of the channel 2 input signal. During single channel measurements, this circuit latches the digital data that represents the real portion of the active channel (either channel 1 or 2).

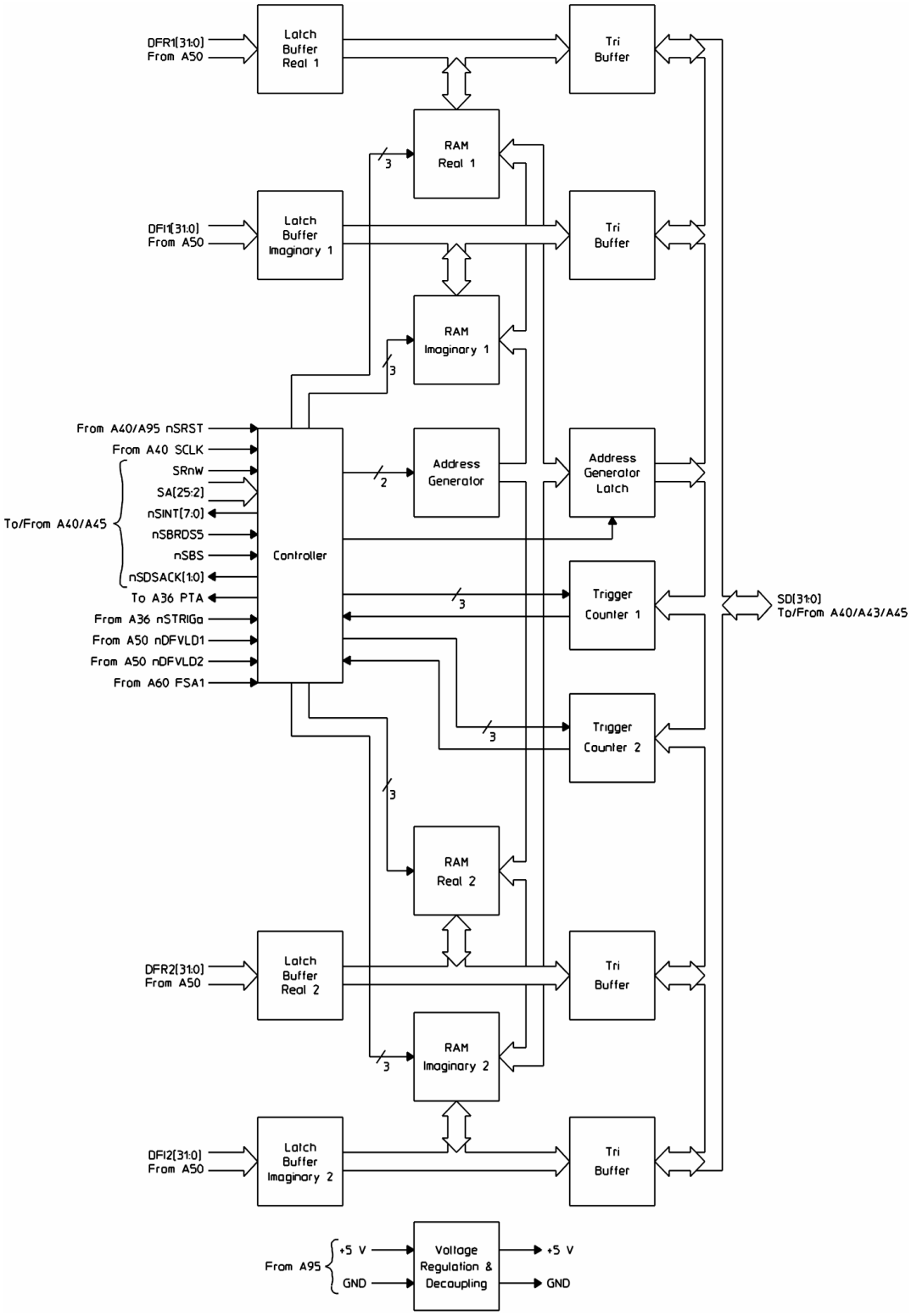
Latch BufferImaginary 2. During two channel measurements, this circuit latches the digital data that represents the imaginary portion of the channel 2 input signal. During single channel measurements, this circuit latches the digital data that represents the imaginary portion of the active channel (either channel 1 or 2).

RAM Real 1. During two channel measurements, this circuit stores the digital data that represents the real portion of the channel 1 input signal. During single channel measurements using channel 1,
this circuit stores the digital data that represents the real portion of the channel 1 input signal after RAM Real 2 is full. This circuit is not used during single channel measurements using channel 2.

RAM Imaginary 1. During two channel measurements, this circuit stores the digital data that represents the imaginary portion of the channel 1 input signal . During single channel measurements using channel 1, this circuit stores the digital data that represents the imaginary portion of the channel 1 input signal after RAM Imaginary 2 is full. This circuit in not used during single measurements using channel 2.

RAM Real 2. During two channel measurements, this circuit stores the digital data that represents the real portion of the channel 2 input data. During single channel measurements, this circuit stores the digital data that represents the real portion of the active channel (either channel 1 or 2).

A55 Sample RAM and A56 Expanded Sample RAM



RAM Imaginary 2. During two channel measurements, this circuit stores the digital data that represents the imaginary portion of the channel 2 input data. During single channel measurements, this circuit stores the digital data that represents the imaginary portion of the active channel (either channel 1 or 2).

Address Generator. Sets the RAM addresses.

Address Generator Latch. Latches the addresses generated by the Address Generator.

Tri Buffers. Buffer the digital data from the input data lines to the system data lines. During diagnostics, this circuit can buffer the digital data from the system data lines to the input data lines. The Tri Buffers are bidirectional transceivers.

Controller. Interfaces with assemblies on the system bus and controls this assembly.

Trigger Counter 1 and Trigger Counter 2. Provide timing to the Controller circuit. The timing is used for settling time, pre and post trigger delay, and block measurement.

A60 Frequency Reference

The Frequency Reference assembly provides the sample clock, 25.6 MHz reference, and 400 MHz reference to various assemblies.

External Reference Signal Conditioner. Conditions the external frequency reference. The optional A85 Oven assembly can supply the external frequency reference.

External Reference Output. Routes the external reference input to the rear panel.

External Reference Detector. Detects the presence of the external reference and informs the Loop Filter circuit and the A36 Trigger assembly.

Phase Detector. Compares the phase of the signal from the Divide-by-8 with the phase of the signal from External Reference Signal Conditioner and generates a voltage equal to the phase difference. This circuit can phase lock to an external frequency reference of 1, 2, 5, or 10 MHz.

Loop Filter. Amplifies and filters the phase-difference voltage from the Phase Detector. It then routes the voltage to the 51.2 MHz VCXO. If the Unlock Detector indicates that the loop is unlocked, this circuit selects a wider loop bandwidth in an attempt to phase lock.

Unlock Detector. Monitors the feedback voltage to the 51.2 MHz VCXO. If the feedback voltage is either too high or too low (approx ±11 V), indicating that the external reference PLL is unlocked, this circuit informs the Loop Filter and the A36 Trigger assembly.

51.2 MHz VCXO. Generates a 51.2 MHz signal. When an external frequency reference is present, feedback phase-locks the 51.2 MHz VCXO to the external reference. This circuit contains a frequency adjustment.

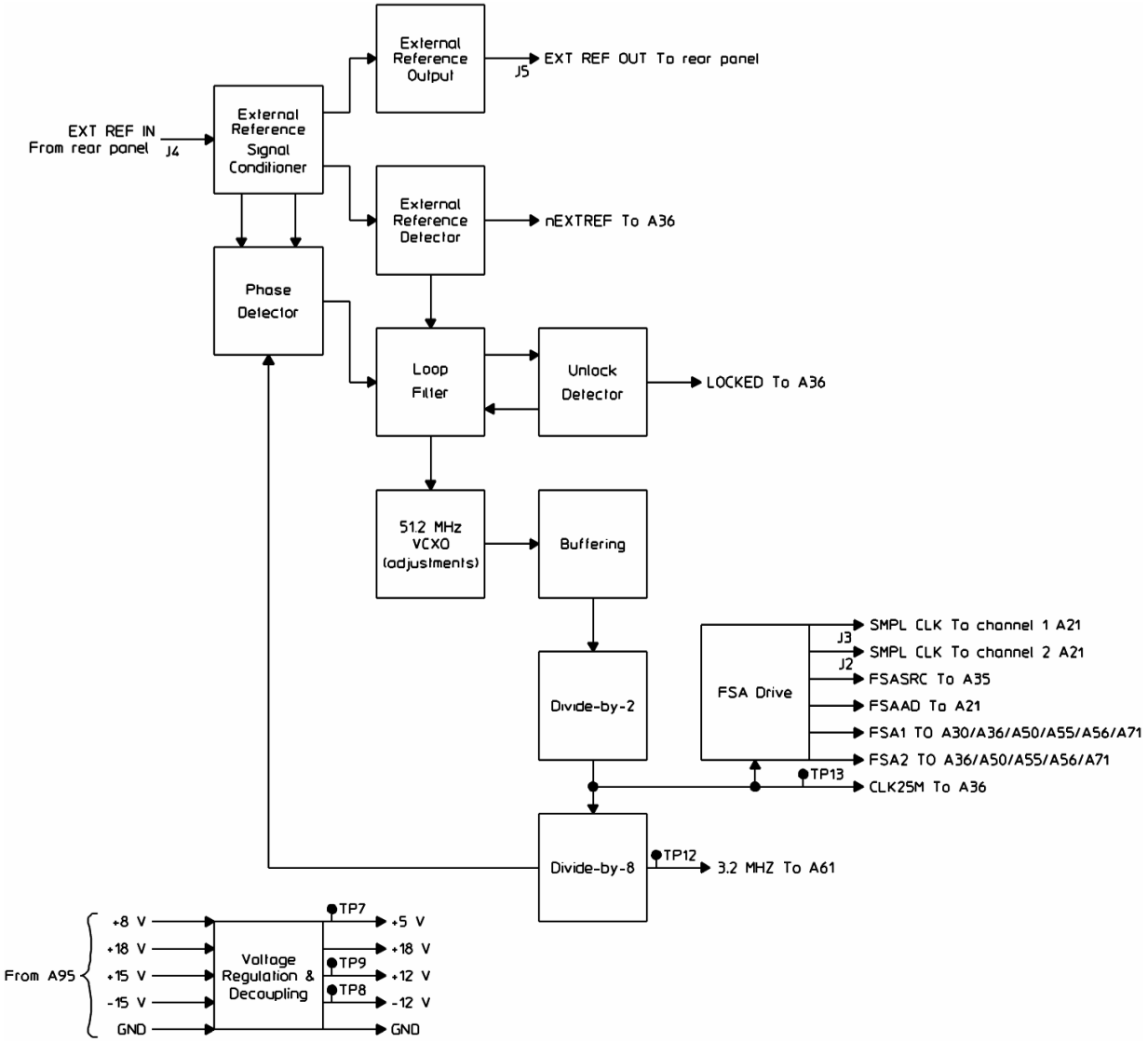
Buffering. Buffers the 51.2 MHz signal.

Divide-by-2. Divides the 51.2 MHz signal down to 25.6 MHz.

FSA Drive. Outputs the 25.6 MHz signal to various assemblies as the system sample clock.

Divide-by-8. Divides the 25.6 MHz signal down to 3.2 MHz.

A60 Frequency Reference Block Diagram



A61 Clock

The Clock assembly provides 377.953 kHz, 48 MHz, 64 MHz, and 80 MHz frequency references.

16 MHz Phase Locked Loop. Generates a 16 MHz signal. Feedback from the Divide-by-5 phase locks this circuit to the 3.2 MHz signal from the A60 Frequency Reference assembly.

Divide-by-5. Divides the 16 MHz signal down to 3.2 MHz.

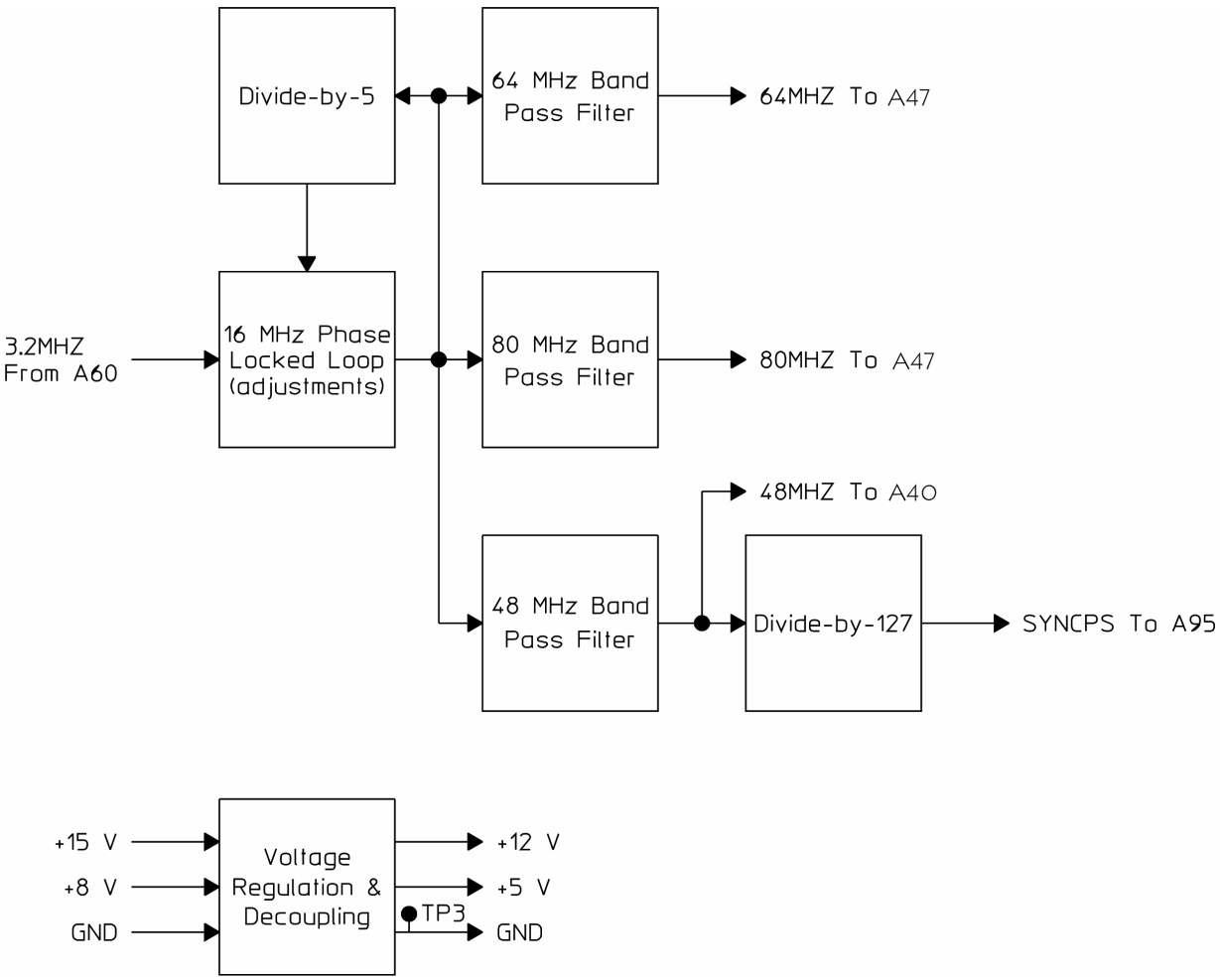
64 MHz Band Pass Filter. Filters the 16 MHz signal, passing only the 4th harmonic to the A47 DSP/Display assembly.

80 MHz Band Pass Filter. Filters the 16 MHz signal, passing only the 5th harmonic to the A47 DSP/Display assembly.

48 MHz Band Pass Filter. Filters the 16 MHz signal, passing only the 3rd harmonic to the A40 CPU assembly and the Divide-by-127 circuit.

Divide-by-127. Divides the 48 MHz signal down to 377.953 kHz.

A61 Clock Block Diagram



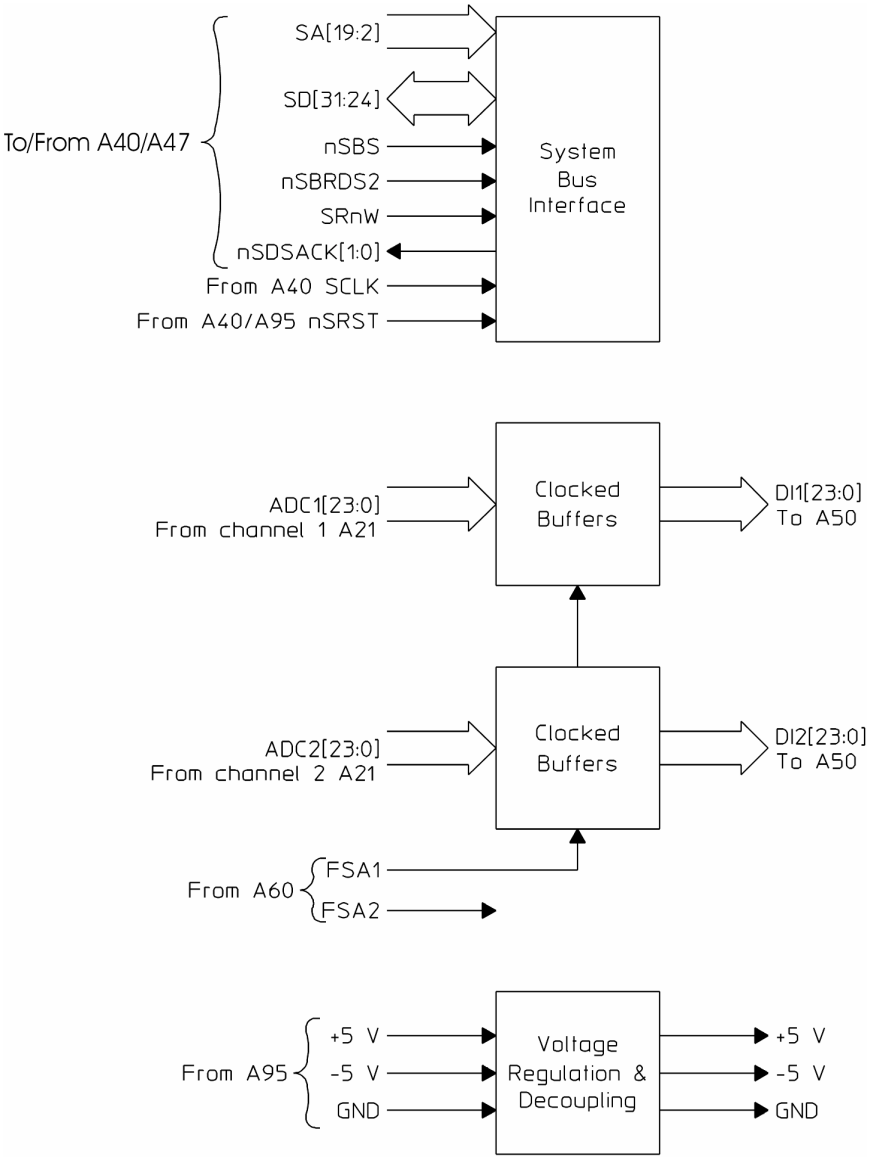
A71 Pass Through

The Pass Through assembly buffers the channel 1 and 2 input signals. The channel 1 and 2 input signals are routed from the A21 A/D Converter assemblies, through this assembly, to the A50 Digital Filter assembly.

Clocked Buffers. Buffer the channel 1 and 2 input signals. The system sample clock (FSA1) provides the timing for passing the signals to the A50 Digital Filter assembly.

System Bus Interface. Provides the interface between this assembly and the A40 CPU and A47 DSP/Display Controller assemblies.

A71 Pass Through Block Diagram



A81 Keyboard

The Keyboard assembly consists of keys, an RPG, a DIN keyboard connector, and LED indicators.

Keyboard Driver. Drives the keyboard column lines high one line at a time.

Keys. Return a low to the A42 Memory assembly when a key is pressed. The Memory assembly determines which key was pressed based on the column line driven high and the row line that went low.

LED Decoders. Turn the LEDs on and off.

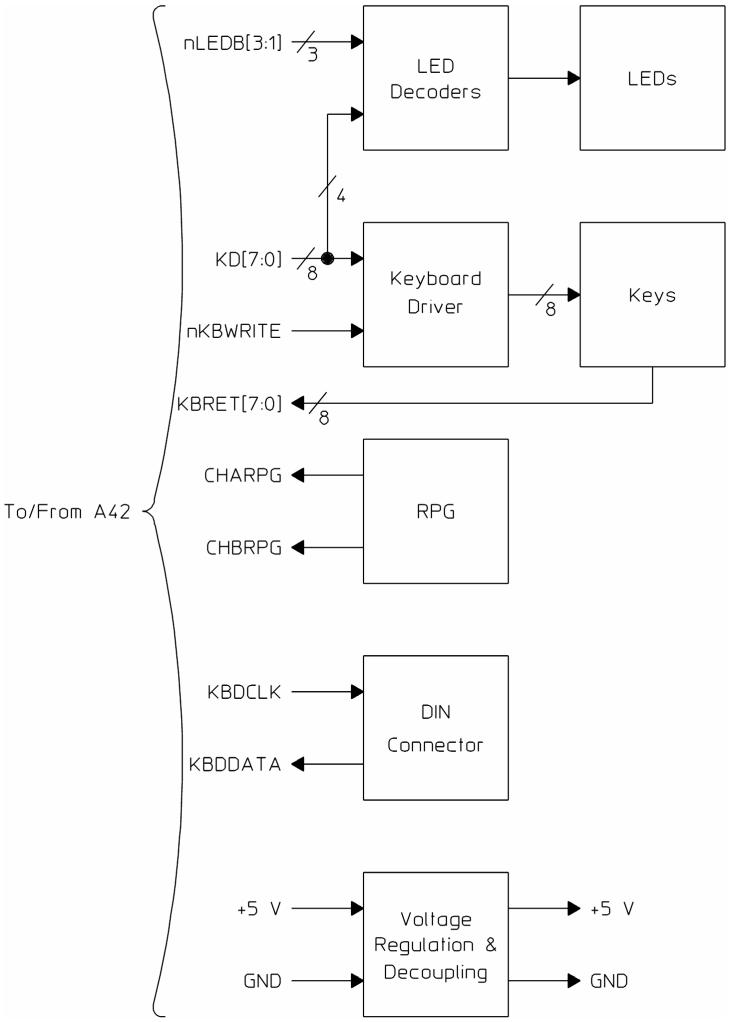
LEDs. Light up to indicate a variety of status conditions.

RPG. Indicates the RPG's direction and offset.

DIN Connector. Is the interface connector for external keyboards.

A82 Control Decoders. Provides the power up programming and control information to the A82 LCD interface.

A81 Keyboard Block Diagram



A82 LCD Interface Circuit Descriptions

DC/ DC converter. Convert +65V supply by A95 to +5V for on board use.

Voltage Regulation. Convert +5V to 3.3V for on board use.

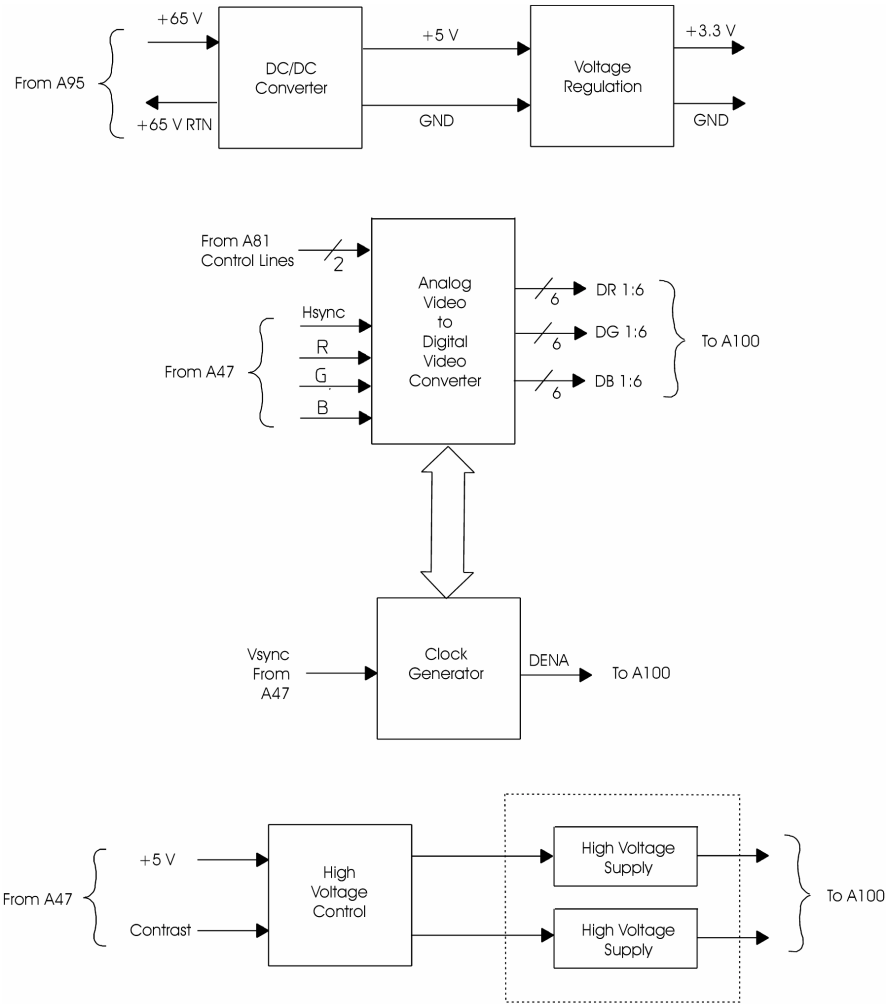
Analog Video to Digital Video Converter. Converts analog RGB and Sync signals to digital format required for the LCD display.

Clock Generator. Provides clock and timing signals for on board use and clocking data into the LCD.

High Voltage Control. Provides power up timing for the high voltage supplies and a control signal for the high voltage supplies based on the contrast signal from the A47.

High Voltage Supplies. Generate the supplies required for the LCD backlights.

A82 LCD Interface Block Diagram



A85 Oven

The optional Oven assembly provides a stable 10 MHz frequency reference to the rear panel (OVEN REF OUT). A BNC-to-BNC jumper connects the OVEN REF OUT connector to the EXT REF IN connector on the rear panel.

A90 Digital Motherboard

The Digital Motherboard provides a common point of contact for voltage and signal distribution. See ''A90 & A91 Motherboards'' in chapter 6, page 6-16 for a list of all signals that are distributed via the motherboards.

A91 Analog Motherboard

The Analog Motherboard provides a common point of contact for voltage and signal distribution. See ''A90 and A91 Motherboards'' in chapter 6,page 6-16 for a list of all signals that are distributed via the motherboards.

A92 Probe Power

The Probe Power assembly provides the power for the active probe connectors on the front panel. This assembly regulates +18 V and -15 V from the power supply to +15 V and –12.6 V.

A95 Main Power Supply

The Main Power Supply assembly is a switching power supply that provides the voltages for all the assemblies in the analyzer. See ''Power Supply Voltage Distribution'' in chapter 6 for a list of the assemblies that use each voltage.

Bias Supply Regulator. Provides æ12 V and +5 V to control and protection circuits on this assembly. This circuit also provides unregulated +22 V to the A85 Oven assembly.

Power Down. Generates a system reset (nSRST) when power is removed from the analyzer.

Synchronize. Synchronizes the Pulsewidth Modulator with the analyzer.

Pulsewidth Modulator. Varies the on time of the pulses that drive the FETs in the FET Drive circuit.

FET Drive. The FETs in this circuit switch high dc voltage across the transformer. The transformer outputs +5 V, ±11 V, ±18 V, and +70 V.

Primary Current Limit. Detects excessive current in the FET Drive circuit. The output of this circuit is routed to the Fault Detector/Shutdown circuit.

Fault Detector/ Shutdown. Turns off the Pulsewidth Modulator if a fault or over-temperature condition is detected. When the Pulsewidth Modulator is turned off, the output of the FET Drive circuit drops to zero volts.

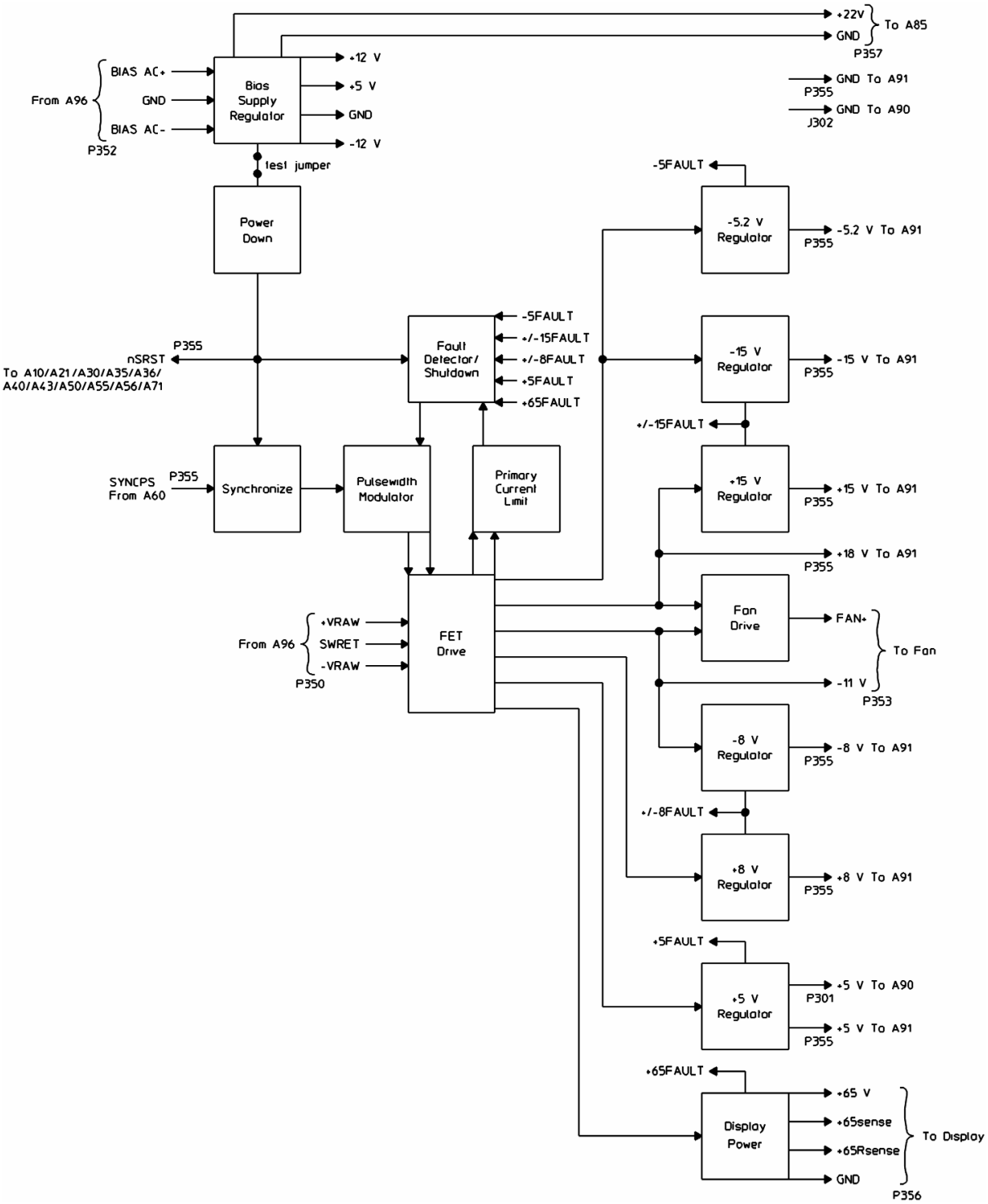
–5.2 V Regulator. Regulates -18 V from the FET Drive circuit to –5.2 V. This circuit also detects over-voltage and over-current conditions. The outputs of both detectors are connected, then routed to the Fault Detector/Shutdown circuit.

–15 V Regulator. Regulates -18 V from the FET Drive circuit to –15 V.

+ 15 V Regulator. Regulates +18 V from the FET Drive circuit to +15 V. Both circuits detect over-voltage conditions. The outputs of both over-voltage detectors are connected, then routed to the Fault Detector/Shutdown circuit.

Fan Drive. Provides the A102 Fan assembly with a variable voltage (+FAN) that controls the fan speed. +FAN can vary from +8 V to +28 V. A temperature sensor provides a control signal that changes with temperature. When the temperature increases, Fan Drive increases the fan speed. When the temperature decreases, Fan Drive decreases the fan speed.

A95 Main Power Supply Block Diagram



–8 V Regulator. Regulates -11 V from the FET Drive circuit to –8 V.

+ 8 V Regulator. Regulates +11 V from the FET Drive circuit to +8 V. Both circuits detect over-voltage and over-current conditions. The outputs of all four detectors are connected, then routed to the Fault Detector/Shutdown circuit.

+ 5 V Regulator. Filters +5 V from the FET Drive circuit. This circuit also detects over-voltage and over-current conditions. The outputs of both detectors are connected, then routed to the Fault Detector/Shutdown circuit.

Display Power. Regulates +70 V from the FET Drive circuit to +65 V. This circuit detects over-voltage and under-voltage conditions. The outputs of both detectors are connected, then routed to the Fault Detector/Shutdown circuit. This circuit also limits current to about 1 ampere.

A96 Primary Power Supply

The Primary Power Supply assembly provides bias power and high dc power for the A95 Main Power Supply assembly.

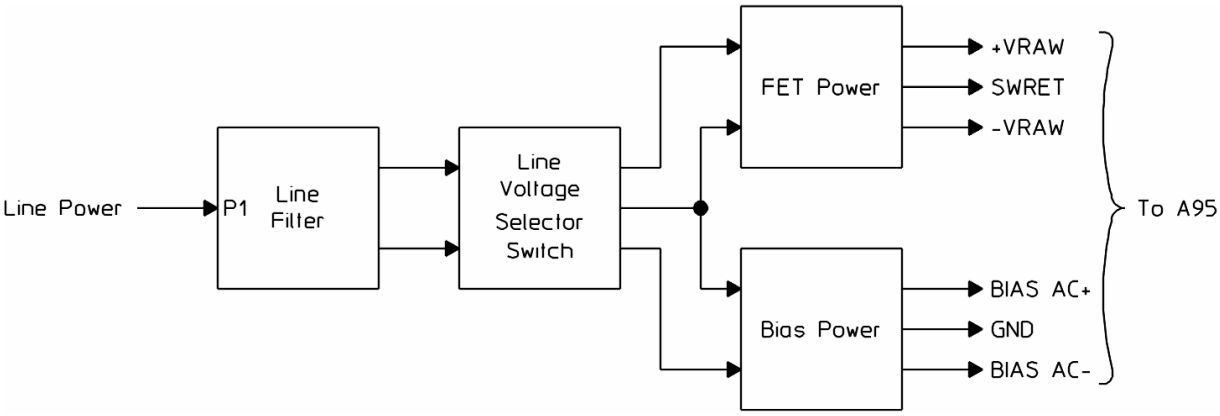
Line Filter. Reduces noise conducted onto the power lines by the switching FETs on the A95 Main Power Supply assembly.

Line Voltage Selector Switch. Allows the analyzer to operate on either 115 Vac or 230 Vac. This switch is located on the analyzer's rear panel.

FET Power. Rectifies and filters the ac line voltage. The rectified and filtered voltage is routed to the FET Drive circuit on the A95 Main Power Supply assembly.

Bias Power. Rectifies and filters the ac line voltage providing approximately ±22 Vac to the Bias Supply Regulator circuit on the A95 Main Power Supply assembly.

A96 Primary Power Supply Block Diagram



A100 Display

The Display assembly shows processed data sent by A47 DSP/Display Controller assembly.

A101 Disk Drive

The internal Disk Drive assembly stores and retrieves information from 3.5-inch flexible disks. This assembly is controlled by the A42 Memory assembly.

A102 Fan

The Fan assembly cools the analyzer. The fan speed varies with the analyzer's temperature. As the analyzer's temperature increases, the fan speed increases. As the temperature decreases, the fan speed decreases. The A95 Main Power Supply assembly provides the variable voltage that controls the fan speed.

6 Voltages and Signals

Voltages and Signals

This chapter shows where the signals and voltages are used in the analyzer and describes each signal. The signals are described in groups as shown in the following table.

Section Title	Describes signals routed ...
RF Cables	through RF cables
A42 Memory	between A42 Memory and A40 CPU
A81 Keyboard	between A81 Keyboard and A42 Memory
A90/ A91 Motherboard	through A90 Digital Motherboard and A91 Analog Motherboard
A101 Disk Drive	between A101 Disk Drive and A42 Memory
Interface Connectors	through the HPIB, Serial 1, Serial 2, Parallel Port, External Monitor, DIN, ThinLAN, and AUI connectors.

NOTE: Signals with a mnemonic that start with a lower case ''n'' are active low.

Signal levels listed as low or high are TTL levels unless stated otherwise.

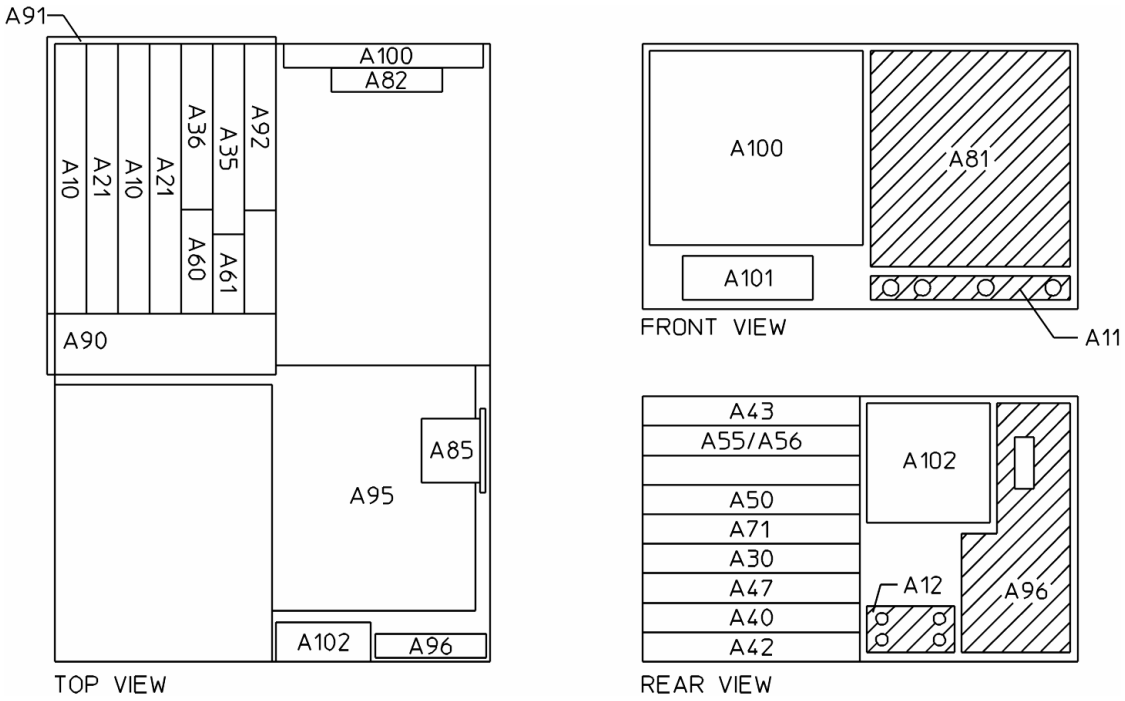
Measurements given in dBm are terminated in 50 ohms unless stated otherwise.

Assembly Locations and Connections

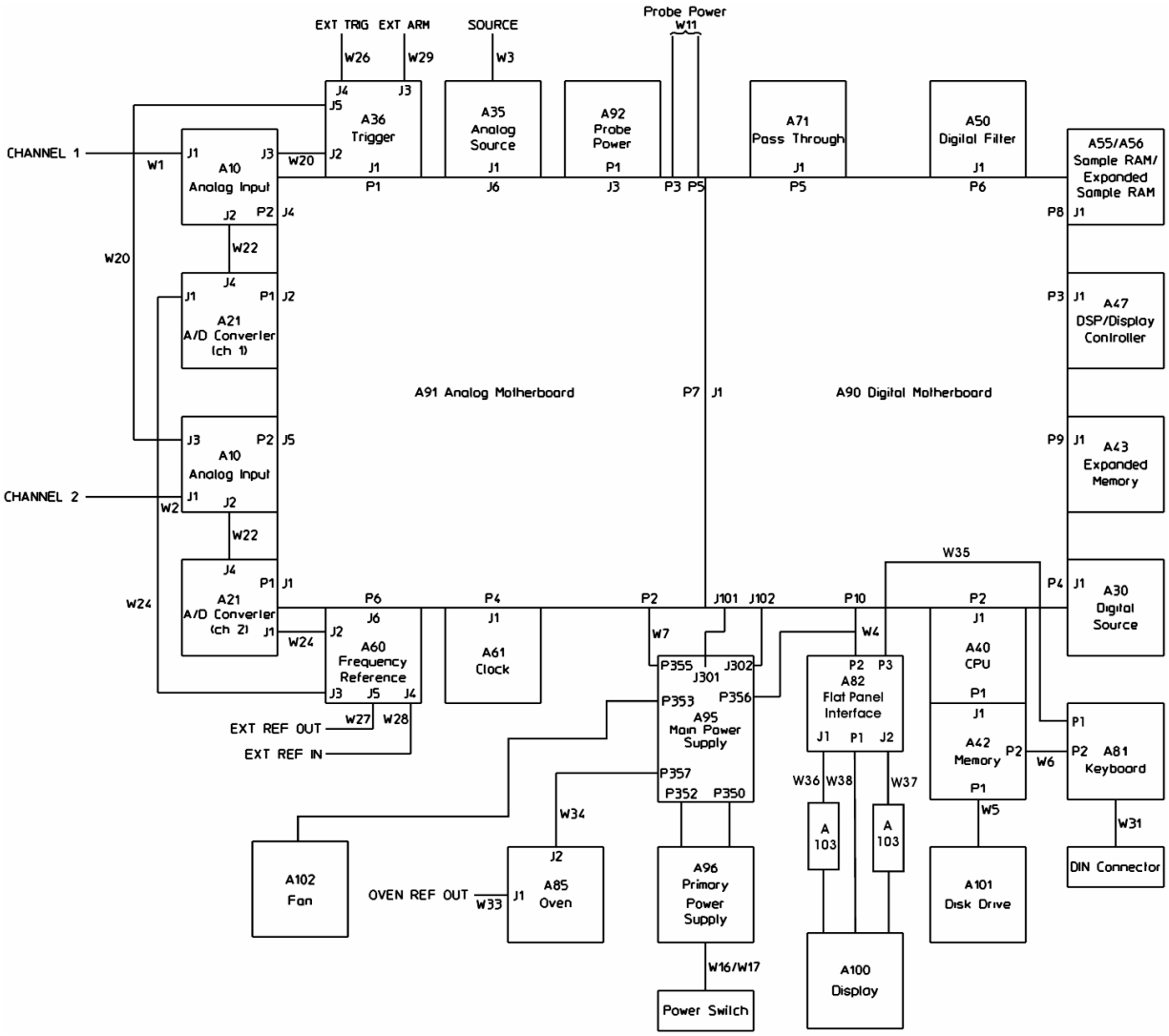
The following figures show the assembly locations and assembly connections.

A10 Analog Input (2 for option AY7)
A11 Front Panel Connector
A12 Rear Panel Connector
A21 A/ D Converter (2 for option AY7)
A30 Digital Source
A35 Analog Source
A36 Trigger
A40 CPU
A42 Memory
A43 Expanded Memory (option UFG)
A47 DSP/ Display Controller
A50 Digital Filter
A55 Sample RAM
A56 Expanded Sample RAM (option AY9)
A60 Frequency Reference
A61 Clock
A71 Pass Through
A81 Keyboard
A82 LCD Interface
A85 Oven (option AY5)
A90 Digital Motherboard
A91 Analog Motherboard
A92 Probe Power
A95 Main Power Supply
A96 Primary Power Supply
A100 Display
A101 Disk Drive
A102 Fan

Assembly Locations



Assembly Connections



Power Supply Voltage Distribution

The following table shows the power supply voltages used by each assembly in the analyzer. In addition, the table also shows the path taken by these voltages. Some assemblies use the power supply voltages as supplied by the A95 Main Power Supply assembly. However, most assemblies contain voltage regulation and voltage decoupling circuits to provide additional regulation and decoupling for their own use.

Power Supply Voltage Distribution

From	Path	To	Voltages											
			+5	−5.2	+8	−8	+15	−15	+18	+22	+65	−11	FAN+	Gnd
Power Supply	A91	A10	X		X	X	X	X						X
	A91	A21	X	X	X	X	X	X						X
	A90	A30	X											X
	A91	A35			X	X	X	X						X
	A91	A36	X		X	X	X	X						X
	A91/ A90	A40		X			X	X						X
	A90	A40	X											X
	A91/ A90/ A40	A42					X							X
	A90/ A40	A42	X											X
	A91/ A90	A43		X			X	X						X
	A90	A43	X											X
	A91/ A90	A47		X			X	X						X
	A90	A47	X											X
	A90	A50	X											X
	A90	A55/ 56	X											X
	A91	A60			X		X	X	X					X
	A91	A61			X		X							X
	A91/ A90	A71		X										X
	A90	A71	X											X
	A90/ A40/ A42	A80	X											X
	W34	A85								X				X
	A91	A92						X	X					X
	W4	A82									X			X
	A90/ A40/ A42	A101	X											X
		A102										X	X	

RF Cables

Signals routed through RF cables are shown in the following table. The table shows where the cables are connected and uses bold face type to show where the signal is generated.

Signal Name	A10	A21	A35	A36	A60	A85	Front panel	Rear panel
ANALOGIN	**J2**	J4						
EXT ARM				J3				**EXT ARM**
EXT REF IN					J4			**EXT REF IN**
EXT REF OUT					**J5**			EXT REF OUT
EXT TRIG				J4			**EXT TRIGGER**	
INPUT								
(channel 1)	J1						**CHANNEL 1**	
(channel 2)	J1						**CHANNEL 2**	
OVEN REF						**J100**		OVEN REF OUT
SMPL CLK								
(channel 1)		J1			**J3**			
(channel 2)		J1			**J2**			
SRC OUT			**J1**				**SOURCE**	
TRIGGER								
(channel 1)	**J3**			J2				
(channel 2)	**J3**			J5				

† The signal source is shown in boldface type.

ANALOGIN. Analog Input — This is the input signal after the A10 Analog Input assembly conditions it. The signal's amplitude is -9.8 dBm (72 mVrms) with the analyzer set to the 0 dBm range and a 0 dBm (0.2236 Vrms) signal connected to the input connector. The A21 A/D Converter assembly converts this analog signal to digital data.

EXT ARM. External Arm — This is the external arm input.

EXT REF IN. External Reference Input — This is the external reference input from the optional A85 Oven assembly or from an external source. The signal can be a 1 MHz, 2 MHz, 5 MHz, or 10 MHz sine or square wave.

EXT REF OUT. External Reference Output — This is the external reference input buffered and routed to the rear panel.

EXT TRIG. External Trigger — This is the external trigger input.

INPUT. Input — This is the input signal for the receiver. The input signal can range from dc to 10 MHz.

OVEN REF. Oven Reference — This is a stable 10 MHz frequency reference. Its amplitude is approximately 5 dBm. A BNC-to-BNC jumper connects the OVEN REF OUT connector to the EXT REF IN connector.

SMPL CLK. Sample Clock — This is the system sample clock. This clock operates at 25.6 MHz.

SRC OUT. Source Output — This is the source output. The source output is a sine wave or arbitrary waveform with an amplitude up to 24 dBm.

TRIGGER. Trigger — This is the input signal routed to the A36 Trigger assembly for input triggering, over-range detection, and half-range detection.

A42 Memory

The following table lists signals routed between the A42 Memory assembly and the A40 CPU assembly. This table shows several things – if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

A42 Memory Signals and Voltages

Signal Name	Pin (s)	A40 P1	A42 P1	Signal Name	Pin(s)	A40 P1	A42 P1
A[0]	C14	S	•	D[15]	A9	↔	↔
A[1]	A15	S	•	D[16]	B9	↔	↔
A[2]	B15	S	•	D[17]	C9	↔	↔
A[3]	C15	S	•	D[18]	A10	↔	↔
A[4]	A16	S	•	D[19]	B10	↔	↔
A[5]	B16	S	•	D[20]	C10	↔	↔
A[6]	C16	S	•	D[21]	A11	↔	↔
A[7]	A17	S	•	D[22]	B11	↔	↔
A[8]	B17	S	•	D[23]	C11	↔	↔
A[9]	C17	S	•	D[24]	A12	↔	↔
A[10]	A18	S	•	D[25]	B12	↔	↔
A[11]	B18	S	•	D[26]	C12	↔	↔
A[12]	C18	S	•	D[27]	A13	↔	↔
A[13]	A19	S	•	D[28]	B13	↔	↔
A[14]	B19	S	•	D[29]	C13	↔	↔
A[15]	C19	S	•	D[30]	A14	↔	↔
A[16]	A21	S	•	D[31]	A15	↔	↔
A[17]	B20	S	•	AgilentIBCLK	A3	S	•
A[18]	C20	S	•	nBFAS	A24	S	•
A[19]	A21	S	•	nBFRST	C26	S	•
A[20]	B21	S	•	nD1DTK	C24	—	S
A[21]	C21	S	•	nD2DTK	A25	•	S
A[22]	A22	S	•	nDINIRQ	B27	•	S
A[23]	B22	S	•	nDISCIRQ	A27	•	S
BEEPER	B29	S	•	nDSLWDTK	C25	•	S
BFRnW1	C22	S	•	nAgilentIBIRQ	B24	•	S
CLK24M3	B26	S	•	nIFCRST	B30	•	S
D[0]	A4	↔	↔	nROMBEN	A29	S	•
D[1]	B4	↔	↔	nSERIRQ	C27	•	S

A42 Memory Signals and Voltages

D[2]	C4	↔	↔	nSRST	A23	S	•
D[3]	A5	↔	↔	PSIZ0	B28	•	S
D[4]	B5	↔	↔	PSIZ1	A28	•	S
D[5]	C5	↔	↔	RAW8MHZ	C28	S	•
D[6]	A6	↔	↔	SIZ0	B23	S	—
D[7]	B6	↔	↔	SIZ1	C23	S	—
D[8]	C6	↔	↔	TRXCA	B25	—	S
D[9]	A7	↔	↔	+5 V	C32, A2	•	•
D[10]	B7	↔	↔	+15 V	B32	•	•
D[11]	C7	↔	↔	GND	A1, B1, C1, B2	•	•
D[12]	A8	↔	↔	GND	C2,<I >B3,<I >C3, C29	•	•
D[13]	B8	↔	↔	GND	A30, C30, C31	•	•
D[14]	C8	↔	↔	GND	A32, A31, B31	•	•

S This assembly is the source of the signal.
• This assembly uses the signal.
↔This signal is bidirectional.
— This assembly does not use this signal.

A[23:0]. Address Bus — This is the processor address bus from the A40 CPU assembly.

BEEPER. Beeper — This line controls the frequency of the beeper tone.

BFRnW1. Buffered Read/Write — A low on this line enables write operations to the A42 Memory assembly.

CLK24M3. 24 MHz Clock — This is a 50% duty cycle, 24 MHz clock. This clock provides the timing for the A42 Memory assembly.

D[31:0]. Data Bus — This is the processor data bus from the A40 CPU assembly.

AgilentIBCLK. HPIB Clock — This is a 40% duty cycle, 4.8 MHz clock. This clock provides the timing for the HPIB controller on the A42 Memory assembly.

nBFAS. Buffered Address Strobe — A low on this line starts a memory access cycle. This line pulses low when a valid address is on the address bus (A[23:0]).

nBFRST. Buffered Reset — A low on this line resets the digital logic on the A40 CPU assembly and A42 Memory assembly.

nD1DTK. DSACK Request — This line is not used.

nD2DTK. DSACK Request – This line goes low when the A42 Memory assembly's non-volatile RAM, Disk Controller, Disk FIFO or Flash ROM requests the A40 CPU assembly to assert nDSACK[1:0] (data transfer and size acknowledgment).

nDINIRQ. DIN Interrupt Request – The A42 Memory assembly's DIN keyboard controller forces this line low to request service from the A40 CPU assembly. This line goes low when a key is pressed on the keyboard connected to the DIN connector.

nDISCIRQ . Disk Interrupt Request – The A42 Memory assembly's disk controller forces this line low to request service from the A40 CPU assembly.

nDSLWDTK . DTACK Request – This line goes low when the A42 Memory assembly's keyboard or RPG controller requests the A40 CPU assembly to assert nDSACK[1:0] (data transfer and size acknowledgment).

nAgilentIBIRQ . HPIB Interrupt Request – The A42 Memory assembly's HPIB controller forces this line low to request service from the A40 CPU assembly.

nIFCRST . IFC Reset Request – A low on this line requests a system reset from the A40 CPU assembly. This line goes low when the analyzer is under HPIB control and a system reset is requested over the HPIB bus.

nROMBEN. ROM Bus Enable – A low on this line enables the data bus buffers on the A42 Memory assembly. When the Memory assembly's data bus buffers are enabled, the A40 CPU assembly's data bus (D[31:0]) and the Memory assembly's data bus (ROMD[31:0]) are connected together through the buffers.

nSERIRQ. Serial Interrupt Request – The A42 Memory assembly's serial interface forces this line low to request service from the A40 CPU assembly.

nSRST. System Reset – A low on this line resets the digital logic on all the assembly in the analyzer. This line pulses low during power-up and power-down, and when the processor is externally reset.

PSIZ0 — PSIZ1. Port Data Size – These lines determine the size of the operand. When PSIZ0 is high and PSIZ1 is low, the operand size is 8 bits. When PSIZ0 is low and PSIZ1 is high, the operand size is 16 bits. When both PSIZ0 and PSIZ1 are high, the operand size is 24 bits. When both PSIZ0 and PSIZ1 are low, the operand size is 32 bits.

RAW8MHZ. 8 MHz Clock – This is a 50% duty cycle, 8 MHz clock. This clock provides the timing for the A42 Memory assembly's Serial controller.

SIZ0 — SIZ1. Data Size – These lines are not used.

TRXCA. Serial Clock – This is a 50% duty cycle, 307.7 kHz clock. This clock is generated by the A42 Memory assembly's Serial controller. This clock is not used.

A81 Keyboard

The following table lists signals routed between the A81 Keyboard assembly and the A42 Memory assembly. This table shows several things – if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Keyboard Signals	Pin(s)	A42P2	A80P2
CHARPG	7	•	S
CHBRPG	5	•	S
KBDCLK	3	S	•
KBDDATA	2	•	S
KBRET[0]	20	•	S
KBRET[1]	19	•	S
KBRET[2]	18	•	S
KBRET[3]	17	•	S
KBRET[4]	15	•	S
KBRET[5]	13	•	S
KBRET[6]	11	•	S
KBRET[7]	9	•	S
KD[0]	31	S	•
KD[1]	29	S	•
KD[2]	27	S	•
KD[3]	25	S	•
KD[4]	24	S	•
KD[5]	23	S	•
KD[6]	22	S	•
KD[7]	21	S	•
nKBWRITE	39	S	•
nLEDB1	37	S	•
nLEDB2	35	S	•
nLEDB3	33	S	•
+5 V	40, 38	•	•
GND	1, 6, 8, 10, 12, 14, 16, 26-36 (odd)	•	•

S This assembly is the source of the signal. • This assembly uses the signal.

CHARPG – CHBRPG. Channel A RPG – Channel B RPG — These lines indicate the RPG's direction and offset.

KBDCLK. Keyboard Clock — This clock synchronizes the transfer of keyboard data from an external keyboard to the A42 Memory assembly.

KBDDATA. Keyboard Data — This is 8-bit serial data from an external keyboard to the A42 Memory assembly.

KBRET[7:0]. Keyboard Return — A low on a line indicates that a key in that row was pressed.

KD[7:0]. Key Data — These data lines drive the keyboard column lines and turn the LEDs on and off. nKBWRITE clocks KD[7:0] into the keyboard column driver and nLEDB[3:1] latches KD[6:4, 0] into the LED decoders. The A42 Memory assembly determines which key was pressed based on the KD line that was high when a KBRET line went low.

nKBWRITE. Keyboard Write — This line clocks KD[7:0] into the keyboard column driver.

nLEDB[3:1]. LED — These lines latch KD[6:4, 0] into the LED decoders that turn the LEDs on and off.

A90 and A91 Motherboards

The motherboard connectors on the A10 Analog Input assemblies and the A35 Analog Source assembly are integrated DIN connectors. The connectors have a space for a coaxial connector at each end. Pin locations 30A through 32C contain a coaxial connector and pin locations 1A through 3C are empty. Therefore, pin 4A is the first pin connecting signals to the Motherboard.

The following table lists all signals routed through the A90 Digital Motherboard and the A91 Analog Motherboard. The table uses bold face type to show which assembly can generate the signal. A description of each signal follows the ''A90/A91 Motherboard Voltages'' table,page 6-24 .

A90/ A91 Motherboard Signals

Signal Name	Assembly Using Signal																	
	A10	A10	A21	A21	A35	A36	A60	A61	A95	A90/ A91	A40	A47	A30	A71	A50	A55 / A56	A43	A82
	A91 Analog Motherboard Connector										A90 Digital Motherboard Connector							
	J4	J5	J2	J1	J6	P1	P6	P4	P2	P7/ J1	J2	J3	J4	J5	J6	J8	J9	J10
	Connector Pin Number																	
3.2MHZ							18	28										
48MHZ								24		58	58							
64MHZ								21		107		144						
80MHZ								25		7		44						
ADC1[0]			11C							140				18				
ADC1[1]			12B							39				68				
ADC1[2]			13A							89				118				
ADC1[3]			13C							139				168				
ADC1[4]			14B							38				19				
ADC1[5]			15A							138				169				
ADC1[6]			15C							37				20				
ADC1[7]			16B							87				70				
ADC1[8]			17A							137				120				
ADC1[9]			17C							36				170				
ADC1[10]			18B							136				21				
ADC1[11]			19A							35				71				
ADC1[12]			19C							85				121				
ADC1[13]			20B							135				171				
ADC1[14]			21A							34				32				
ADC1[15]			21C							134				182				
ADC1[16]			22B							33				33				
ADC1[17]			23A							83				83				
ADC1[18]			23C							133				133				
ADC1[19]			24B							32				183				
ADC1[20]			25A							132				34				
ADC1[21]			25C							31				84				
ADC1[22]			26B							81				134				
ADC1[23]			27A							131				184				
ADC2[0]				11C						49				1				
ADC2[1]				12B						99				151				
ADC2[2]				13A						149				2				
ADC2[3]				13C						48				52				
ADC2[4]				14B						148				152				
ADC2[5]				15A						47				3				
ADC2[6]				15C						97				53				
ADC2[7]				16B						147				153				
ADC2[8]				17A						46				4				
ADC2[9]				17C						146				154				
ADC2[10]				18B						45				5				
ADC2[11]				19A						95				55				
ADC2[12]				19C						145				155				

A90/ A91 Motherboard Signals, continued

Signal Name	Assembly Using Signal																	
	A10	A10	A21	A21	A35	A36	A60	A61	A95	A90 / A 91	A40	A47	A30	A71	A50	A55 / A56	A43	A82
	A91 Analog Motherboard Connector										A90 Digital Motherborad Connector							
	J4	J5	J2	J1	J6	P1	P6	P4	P2	P7/ J1	J2	J3	J4	J5	J6	J8	J9	J10
	Connector Pin Number																	
ADC2[13]				20B						44				6				
ADC2[14]				21A						144				56				
ADC2[15]				21C						43				156				
ADC2[16]				22B						93				7				
ADC2[17]				23A						143				157				
ADC2[18]				23C						42				8				
ADC2[19]				24B						142				58				
ADC2[20]				25A						41				108				
ADC2[21]				25C						91				158				
ADC2[22]				26B						141				9				
ADC2[23]				27A						40				59				
B												50						19
BACKGND												148						8
CALTRIG					25B	27												
CH1CAL	25B				29B													
CH2CAL		25B			27B													
CLK25M						15	10											
DAC[0]					4A					30			31					
DAC[1]					4C					130			81					
DAC[2]					5B					29			131					
DAC[3]					6A					79			181					
DAC[4]					6C					129			32					
DAC[5]					7B					28			182					
DAC[6]					8A					128			33					
DAC[7]					8C					27			83					
DAC[8]					9B					77			133					
DAC[9]					10A					127			183					
DAC[10]					10C					26			34					
DAC[11]					11B					126			84					
DFI1[31:0]															†			
DFI2[31:0]															†			
DFR1[31:0]															†			
DFR2[31:0]															†			
DI1[23:0]													‡	‡	‡			
DI2[23:0]														‡	‡			
FECLK1	18A		29C							17			89					
FECLK2		18A		29C						68			139					
FECLK3					19B	42				118			189					

The source of the signal is shown in boldface type.
† See the ''Digital Filter Signals'' table for connector pin numbers.
‡ See the ''Digital Input Signals'' table for connector pin numbers.

A90/ A91 Motherboard Signals, continued

Signal Name	Assembly Using Signal																	
	A10	A10	A21	A21	A35	A36	A60	A61	A95	A90 / A91	A40	A47	A30	A71	A50	A55 / A56	A43	A82
	A91 Analog Motherboard Connector										A90 Digital Motherboard Connector							
	J4	J5	J2	J1	J6	P1	P6	P4	P2	P7/ J1	J2	J3	J4	J5	J6	J8	J9	J10
	Connector Pin Number																	
FEDATA			29A	29A		45				18			39					
FELATCH	18B	18B	30B	30B	19C	44				15			40					
FELOOP1	17C		28B															
FELOOP2		17C		28B														
FELOOP3					18C	43												
FERET1	17B									16			90					
FERET2		17B								116			140					
FERET3					18B					117			190					
FSA1						18	16			13			28	28	28	28		
FSA2						17	11			12				78	78	78		
FSAAD			27C	27C			4											
FSASRC					12A		5											
G												49						17
GTCLK						16				62			29					
INTEN												147						7
LOCKED						32	26											
nADCOVR1			11B							122			136					
nADCOVR2				11B						121			137					
nDFVLD1															42	42		
nDFVLD2															92	92		
nEXTREF						33	25											
nFEERR	19C	19C			20C	40				66			41					
nFEPROG			30A	30A		39				115			191					
nHLFRNG1			31B			48				22			36					
nHLFRNG2				31B		50				21			37					
nHSYNC												150						12
nOFFWR					18A					120			134					
nOVRRNG1			32A			47				72			86					
nOVRRNG2				32A		49				70			87					
nSBG[0]											16	139						
nSBR[0]											66	89						
nSBRDS[0]											123	28						
nSBRDS[1]											116		22					
nSBRDS[2]											115			22				
nSBRDS[3]											114				22			
nSBRDS[5]											112					22		
nSBRDS[6]											111						28	
nSBS											122	29	23	23	23	23	29	
nSDSACK[0]											121	30	73	73	73	73	30	
nSDSACK[1]											21	130	123	123	223	223	130	

The source of the signal is shown in boldface type.

A90/ A91 Motherboard Signals, continued

Signal Name	Assembly Using Signal																	
	A10	A10	A21	A21	A35	A36	A60	A61	A95	A90 / A91	A40	A47	A30	A71	A50	A55 / A56	A43	A82
	A91 Analog Motherboard Connector										A90 Digital Motherboard Connector							
	J4	J5	J2	J1	J6	P1	P6	P4	P2	P7/ J1	J2	J3	J4	J5	J6	J8	J9	J10
	Connector Pin Number																	
nSINT[0]											119	32	74			74	32	
nSINT[1]											20	131	124			224	131	
nSINT[2]											68	83	174			274	83	
nSINT[3]											118	33	25			25	33	
nSINT[4]											19	132	175			275	132	
nSINT[5]											117	34	26			26	34	
nSINT[6]											18	133	176			276	133	
nSINT[7]											17	134	27			27	134	
nSRST	18C	18C	31A	31A	21C	41			7	20	70	81	173	173	273	273	81	
nSTRIGa						26				11			30		30	30		
nSYNCa													77		77			
nTRIG						24				110			179		279		138	
nVSYNC												149						10
OFF[0]					12B					25			184					
OFF[1]					12C					125			35					
OFF[2]					13B					24			185					
OFF[3]					13C					74			186					
OFF[4]					14B					124			187					
OFF[5]					14C					23			38					
OFF[6]					15B					123			188					
PTA						22				109						277		
R												48						15
SA[31:0]											†	†	†			†	†	
SCLK											120	31	24	24	24	24	31	
SD[31:0]											†	†	†			†	†	
SRnW											72	79	172	172	272	272	79	
SSIZ[0]											23	128					128	
SSIZ[1]											22	129					129	
SYNCPS								5	6									
TPSD						23				60			92					

The source of the signal is shown in boldface type.

† See the System Address and System Data Signals table for connector pin numbers.

Digital Filter Signals

Signal Name	Assembly		Signal Name	Assembly		Signal Name	Assembly		Signal Name	Assembly	
	A50	A55/ A56		A50	A55/ A56		A50	A55/ A56		A50	A55 / A56
	A90 Connector			A90 Connector			A90 Connector			A90 Connector	
	J6	J8		J6	J8		J6	J8		J6	J8
	Pin Number			Pin Number			Pin Number			Pin Number	
DFI1[0]	32	32	DFI2[0]	118	118	DFR1[0]	134	134	DFR2[0]	102	102
DFI1[1]	282	282	DFI2[1]	168	168	DFR1[1]	184	184	DFR2[1]	152	152
DFI1[2]	33	33	DFI2[2]	119	119	DFR1[2]	135	135	DFR2[2]	103	103
DFI1[3]	83	83	DFI2[3]	169	169	DFR1[3]	185	185	DFR2[3]	153	153
DFI1[4]	233	233	DFI2[4]	120	120	DFR1[4]	136	136	DFR2[4]	104	104
DFI1[5]	283	283	DFI2[5]	170	170	DFR1[5]	186	186	DFR2[5]	154	154
DFI1[6]	34	34	DFI2[6]	121	121	DFR1[6]	137	137	DFR2[6]	105	105
DFI1[7]	84	84	DFI2[7]	171	171	DFR1[7]	187	187	DFR2[7]	155	155
DFI1[8]	234	234	DFI2[8]	122	122	DFR1[8]	138	138	DFR2[8]	106	106
DFI1[9]	284	284	DFI2[9]	172	172	DFR1[9]	188	188	DFR2[9]	156	156
DFI1[10]	35	35	DFI2[10]	123	123	DFR1[10]	139	139	DFR2[10]	107	107
DFI1[11]	285	285	DFI2[11]	173	173	DFR1[11]	189	189	DFR2[11]	157	157
DFI1[12]	36	36	DFI2[12]	124	124	DFR1[12]	140	140	DFR2[12]	108	108
DFI1[13]	86	86	DFI2[13]	174	174	DFR1[13]	190	190	DFR2[13]	158	158
DFI1[14]	236	236	DFI2[14]	125	125	DFR1[14]	141	141	DFR2[14]	109	109
DFI1[15]	286	286	DFI2[15]	175	175	DFR1[15]	191	191	DFR2[15]	159	159
DFI1[16]	37	37	DFI2[16]	126	126	DFR1[16]	142	142	DFR2[16]	110	110
DFI1[17]	87	87	DFI2[17]	176	176	FR1[17]	192	192	DFR2[17]	160	160
DFI1[18]	237	237	DFI2[18]	127	127	DFR1[18]	143	143	DFR2[18]	111	111
DFI1[19]	287	287	DFI2[19]	177	177	DFR1[19]	193	193	DFR2[19]	161	161
DFI1[20]	38	38	DFI2[20]	128	128	DFR1[20]	144	144	DFR2[21]	162	162
DFI1[21]	288	288	DFI2[21]	178	178	DFR1[21]	194	194	DFR2[20]	112	112
DFI1[22]	39	39	DFI2[22]	129	129	DFR1[22]	145	145	DFR2[22]	113	113
DFI1[23]	89	89	DFI2[23]	179	179	DFR1[23]	195	195	DFR2[23]	163	163
DFI1[24]	239	239	DFI2[24]	130	130	DFR1[24]	146	146	DFR2[24]	114	114
DFI1[25]	289	289	DFI2[25]	180	180	DFR1[25]	196	196	DFR2[25]	164	164
DFI1[26]	40	40	DFI2[26]	131	131	DFR1[26]	147	147	DFR2[26]	115	115
DFI1[27]	90	90	DFI2[27]	181	181	DFR1[27]	197	197	DFR2[27]	165	165
DFI1[28]	240	240	DFI2[28]	132	132	DFR1[28]	148	148	DFR2[28]	116	116
DFI1[29]	290	290	DFI2[29]	182	182	DFR1[29]	198	198	DFR2[29]	166	166
DFI1[30]	41	41	DFI2[30]	133	133	DFR1[30]	149	149	DFR2[30]	117	117
DFI1[31]	291	291	DFI2[31]	183	183	DFR1[31]	199	199	DFR2[31]	167	167

The source of the signal is shown in boldface type.

Digital Input Signals

Signal Name	Assembly			Signal Name	Assembly		
	A30	A71	A50		A30	A71	A50
	A90 Connector				A90 Connector		
	J4	J5	J6		J4	J5	J6
	Pin Number				Pin Number		
DI1[0]	142	142	242	DI2[0]		35	1
DI1[1]	192	192	292	DI2[1]		185	251
DI1[2]	43	43	43	DI2[2]		36	2
DI1[3]	93	93	93	DI2[3]		86	52
DI1[4]	143	143	243	DI2[4]		136	252
DI1[5]	193	193	293	DI2[5]		186	3
DI1[6]	44	44	44	DI2[6]		37	53
DI1[7]	194	194	294	DI2[7]		87	253
DI1[8]	45	45	45	DI2[8]		137	4
DI1[9]	145	145	245	DI2[9]		187	254
DI1[10]	195	195	295	DI2[10]		38	5
DI1[11]	46	46	46	DI2[11]		188	55
DI1[12]	146	146	246	DI2[12]		39	255
DI1[13]	196	196	296	DI2[13]		89	6
DI1[14]	47	47	47	DI2[14]		139	56
DI1[15]	197	197	297	DI2[15]		189	256
DI1[16]	48	48	48	DI2[16]		40	7
DI1[17]	148	148	248	DI2[17]		90	257
DI1[18]	198	198	298	DI2[18]		140	8
DI1[19]	49	49	49	DI2[19]		190	58
DI1[20]	149	149	249	DI2[20]		41	207
DI1[21]	199	199	299	DI2[21]		191	258
DI1[22]	50	50	50	DI2[22]		42	9
DI1[23]	200	200	300	DI2[23]		92	59

The source of the signal is shown in boldface type.

System Address and System Data Signals

Signal Name	Assembly Using Signal								Signal Name	Assembly Using Signal						
	A40	A47	A30	A71	A50	A55 / A56	A43			A40	A47	A30	A71	A50	A55 / A56	A43
	A90 Digital Motherboard Connector									A90 Digital Motherboard Connector						
	J2	J3	J4	J5	J6	J8	J9			J2	J3	J4	J5	J6	J8	J9
	Connector Pin Number									Connector Pin Number						
SA[0]	136	15	12			12	15		SD[0]	150	1	1			1	1
SA[1]	36	115	62			62	115		SD[1]	50	101	151			251	101
SA[2]	135	16	112	112	212	212	16		SD[2]	149	2	2			2	2
SA[3]	85	66	162	162	262	262	66		SD[3]	49	102	52			52	102
SA[4]	35	116	13	13	13	13	116		SD[4]	148	3	152			254	3
SA[5]	134	17	163	163	263	263	17		SD[5]	48	103	3			3	103
SA[6]	34	117	14	14	14	14	117		SD[6]	147	4	53			53	4
SA[7]	133	18	64	64	64	64	18		SD[7]	47	104	153			253	104
SA[8]	83	68	114	114	214	214	68		SD[8]	146	5	4			4	5
SA[9]	33	118	164	164	264	264	118		SD[9]	46	105	154			254	105
SA[10]	132	19	15	15	15	25	19		SD[10]	145	6	5			5	6
SA[11]	32	119	65	65	65	65	119		SD[11]	45	106	55			55	106
SA[12]	131	20	115	115	215	215	20		SD[12]	144	7	155			255	7
SA[13]	81	70	165	165	265	265	70		SD[13]	44	107	6	6	107		
SA[14]	31	120	16	16	16	16	120		SD[14]	143	8	56			56	8
SA[15]	130	21	166	166	266	266	21		SD[15]	93	58	156			256	58
SA[16]	30	121	17	17	17	17	121		SD[16]	43	108	7			7	108
SA[17]	129	22	67	67	67	67	22		SD[17]	142	9	157			257	9
SA[18]	79	72	117	117	217	217	72		SD[18]	42	109	8			8	109
SA[19]	29	122	167	167	267	267	122		SD[19]	141	10	58			58	10
SA[20]	128	23	18		18	18	23		SD[20]	91	60	108			208	60
SA[21]	28	123	68		68	68	123		SD[21]	41	110	158			258	110
SA[22]	127	24	118		218	218	24		SD[22]	140	11	9			9	11
SA[23]	77	74	168		268	268	74		SD[23]	40	111	59			59	111
SA[24]	27	124	19			19	124		SD[24]	139	12	109	109	209	209	12
SA[25]	126	25	169			269	25		SD[25]	89	62	159	159	259	259	62
SA[26]	26	125	20			20	125		SD[26]	39	112	10	10	10	10	112
SA[27]	125	27	70			70	27		SD[27]	138	13	160	160	260	260	13
SA[28]	25	126	120			220	126		SD[28]	38	113	11	11	11	11	113
SA[29]	124	27	170			270	27		SD[29]	137	14	61	61	61	61	14
SA[30]	74	77	21			21	77		SD[30]	87	64	111	111	211	211	64
SA[31]	24	127	71			71	127		SD[31]	37	114	161	161	261	261	114

The source of the signal is shown in boldface type.

The following table lists all the voltages routed through the A90 Digital Motherboard and the A91 Analog Motherboard.

A90/ A91 Motherboard Voltages

Voltage	Assembly																				
	A10	A10	A21	A21	A35	A36	A60	A61	A92	Probe Power		A95	A90/ A91	A95	A40	A47	A30	A71	A50	A55/ A56	A43	A82
	A91 Analog Motherboard Connector													A90 Digital Motherboard Connector								
	J4	J5	J2	J1	J6	P1	P6	P4	J3	P3	P5	P2	P7/ J1	J101/ J102	J2	J3	J4	J5	J6	J8	J9	J10
	Connector Pin Number																					
+5 V	13A-C	13A-C	8A-C	8A-C		7-8		1-2				3-4		J101	52-53 98-99	52-53 98-99	98-99 102 103	98-99 102 103	98-99 150 151 202 203	98-99 150 151 202 203	52-53 98-99	
-5.2 V			9A-C	9A-C		5-6						1 2	5-6 55 104 105 106		54 57 94 97	54 57 94 97	94 97 104 107	94 97 104 107	97 101 200 204	97 101 200 204	54 57 94 97	
+8 V	5A-C	5A-C	2A-C	2A-C	16A-C	12	45-46 48	15 16				15										
-8 V	7A-C	7A-C	3A-C	3A-C	17A-C	11	41-44	11-12				13										
-12.6 V									1A-C 3A-C	3	3											
+15 V									5A-C 7A-C	1	1											
+15 V	9A-C	9A-C	5A-C	5A-C	22A-C	1	35-37	7-8	15A-C			11			55 96	55 96	96 105	96 105	96 205	96 205	55 96	
-15 V	11A-C	11A-C	6A-C	6A-C	23A-C	2	32-34	3 4	13A-C			9	2 53 102 103		56 95	56 95	95 106	95 106	95 206	95 206	56 95	

+18 V							49		11A-C			8	2 4									
GND	4A-C 6A-C 8A-C 10A-C 12A-C 14A-C 16A-C 20A-C 21A-C 22A-C 23A-C 24A-C 25A 25C 26A-C 27A-C 28A-C 29A-C	4A-C 6A-C 8A-C 10A-C 12A-C 14A-C 16A-C 20A-C 21A-C 22A-C 23A-C 24A-C 25A 25C 26A-C 27A-C 28A-C 29A-C	1A, C 4A, C 7A-C 10A-C 12A, C 13B 14A, C 15B 16A, C 17B 18A, C 19B 20A, C 21B 22A, C 23B 24A, C 25B 26A, C 27B 28A, C 29B 32C	1A, C 4A, C 7A-C 10A-C 12A, C 13B 14A, C 15B 16A, C 17B 18A, C 19B 20A, C 21B 22A, C 23B 24A, C 25B 26A, C 27B 28A, C 29B 32C	1A, C 2B 3A, C 4B 5A, C 6B 7A, C 8B 9A, C 10B 11A, C 13A 14A 15A, C 19A 20A-B 21A-B 24A-C 25A, C 26A-C 27A, C 28A-C 29A, C 30A, C 32A, C	3-4 9-10 13-14 19 28-29 31 37 46	1-3 6-9 12-15 19-20 28-31 38-40 47	6 9-10 13-14 17-18 20 22-23 26-27 29	2A-C 4A-C 6A-C 8A-C 10A-C 12A-C 14A-C 16A-C	2	2	10 12 14	1, 14 19 50-52 54 56-57 59,61 63,65 67,69 71,73 75-76 78,80 82,84 86,88 90,92 94,96 98 100 101 114 119 150	J102	51 59 61 63 65 67 69 71 73 75 76 78 80 82 84 86 88 90 92 100	43 45 51 59 61 63 65 67 69 71 73 75 76 78 80 82 84 86 88 90 92 100 143 145	51, 54 57, 60 63, 66 69, 72 75-76 79, 82 85, 88 91 100 101 110 113 116 119 122 125 126 129 132 135 138 141 144 147 150	51, 54 57, 60 63, 66 69, 72 75-76 79, 82 85, 88 91 100 101 110 113 116 119 122 125 126 129 132 135 138 141 144 147 150	51, 54 57, 60 63, 66 69, 72 75-76 79, 82 85, 88 91, 94 100 201 207 210 213 216 219 222 225 226 229 232 235 238 241 244 247 250	51, 54 57, 60 63, 66 69, 72 75-76 79, 82 85, 88 91, 94 100 201 207 210 213 216 219 222 225 226 229 232 235 238 241 244 247 250	51 59 61 63 65 67 69 71 73 75 76 78 80 82 84 86 88 90 92 100	9 11 13 14 16 18 20

3.2M HZ. 3.2 MHz Clock — This is a 3.2 MHz, TTL-level signal. This signal provides a phase reference for the A61 Clock assembly.

48M HZ. 48 MHz — This is a 48 MHz, TTL-level signal. The A40 CPU assembly divides this signal to generate the system clock.

64M HZ. 64 MHz — This is a 64 MHz, TTL-level signal. This signal provides timing for the A47 DSP/Display Controller assembly.

80M HZ. 80 MHz — This is an 80 MHz, TTL-level signal. This signal provides timing for the A47 DSP/Display Controller assembly.

ADC1 [23:0]. ADC Output Channel 1 — These ECL-level data lines are the digital representation of the channel 1 input signal.

ADC2 [23:0]. ADC Output Channel 2 — These ECL-level data lines are the digital representation of the channel 2 input signal.

B. Blue — This line contains the video information for the color blue.

BACKGND. Background — This line sets the A100 Display assembly's contrast.

CALTRIG. Calibration Trigger — This is a 1 volt peak-to-peak square wave. During the calibration routine, this signal calibrates the trigger comparator circuit on the A36 Trigger assembly.

CH1CAL. Channel 1 Calibration — This is a -17 dBm, calibration signal from the A35 Analog Source assembly. During the calibration routine, this signal calibrates the input circuit on the channel 1 A10 Analog Input assembly. See "Calibration Routine Description" in chapter 7, ''Internal Test Descriptions", page 7-5 for further details.

CH2CAL. Channel 2 Calibration — This is a -17 dBm, calibration signal from the A35 Analog Source assembly. During the calibration routine, this signal calibrates the input circuit on the channel 2 A10 Analog Input assembly. See "Calibration Routine Description" in chapter 7, ''Internal Test Descriptions,''page 7-5 for further details.

CLK25M . 25 MHz Clock — This is a 25.6 MHz, TTL-level clock. This clock provides the timing for counters in the A36 Trigger assembly that are not affected by external sample.

DAC[11:0]. DAC Output to Analog Source — These lines are the digital representation of the source signal. The A35 Analog Source assembly converts these lines to the source signal.

DFI1[31:0]. Digital Filter Imaginary 1 — These data lines contain digital data that represent the imaginary portion of the channel 1 input signal.

DFI2[31:0]. Digital Filter Imaginary 2 — These data lines contain digital data that represents the imaginary portion of the channel 2 input signal during two channel measurements and the imaginary portion of the selected channel (either channel 1 or channel 2) during single channel measurements.

DFR1[31:0]. Digital Filter Real 1 — These data lines contain digital data that represent the real portion of the channel 1 input signal.

DFR2[31:0]. Digital Filter Real 2 — These data lines contain digital data that represents the real portion of the channel 2 input signal during two channel measurements and the real portion of the selected channel (either channel 1 or channel 2) during single channel measurements.

DI1[23:0]. Digital Input 1 — These data lines are the digital representation of the channel 1 input signal. The A50 Digital Filter assembly digitally filters this data into 32-bit real (DFR) and imaginary data (DFI).

DI2[23:0]. Digital Input 2 — These data lines are the digital representation of the channel 2 input signal. The A50 Digital Filter assembly digitally filters this data into 32-bit real (DFR) and imaginary data (DFI).

FECLK1. Front-end Clock 1 — This is the serial data clock for the channel 1 data loop (FEDATA, FELOOP1, and FERET1).

FECLK2. Front-end Clock 2 — This is the serial data clock for the channel 2 data loop (FEDATA, FELOOP2, and FERET2).

FECLK3. Front-end Clock 3 — This is the serial data clock for source/trigger data loop (FEDATA, FELOOP3, and FERET3).

FEDATA. Front-end Data — This is the serial data line that configures the front-end assemblies. FEDATA is routed to the channel 1 A21 A/D Converter assembly, renamed FELOOP1 and routed to the channel 1 A10 Analog Input assembly, renamed FERET1 and routed back to the A30 Digital Source assembly. Likewise, FEDATA is routed to the channel 2 A/D Converter assembly, renamed FELOOP2 and routed to the channel 2 Analog Input assembly, renamed FERET2 and routed back to the Digital Source assembly. FEDATA is also routed to the A36 Trigger assembly, renamed FELOOP3 and routed to the A35 Analog Source assembly, renamed FERET3 and routed back to the Digital Source assembly.

FELATCH. Front-end Latch — A negative pulse on this line informs the gate arrays and shift registers that the serial bitstream is in the correct position and ready to be latched.

FELOOP1. Front-end Loop 1 — This serial data line configures the channel 1 A10 Analog Input assembly. This line is FEDATA renamed FELOOP1 between the channel 1 A21 A/D Converter assembly and channel 1 Analog Input assembly.

FELOOP2. Front-end Loop 2 — This serial data line configures the channel 2 A10 Analog Input assembly. This line is FEDATA renamed FELOOP2 between the channel 2 A21 A/D Converter assembly and channel 2 Analog Input assembly.

FELOOP3. Front-end Loop 3 — This serial data line configures the A35 Analog Source assembly. This line is FEDATA renamed FELOOP3 between the A36 Trigger assembly and Analog Source assembly.

FERET1. Front-end Return 1 — This serial data line returns the configuration data to the A30 Digital Source assembly. This line is FELOOP1 renamed FERET1 between the channel 1 A10 Analog Input assembly and Digital Source assembly. Comparing the data sent (FEDATA) to the data returned (FERET1) can determine the presence of a functional channel 1 Analog Input assembly and channel 1 A21 A/D Converter assembly.

FERET2. Front-end Return 2 — This serial data line returns the configuration data to the A30 Digital Source assembly. This line is FELOOP2 renamed FERET2 between the channel 2 A10 Analog Input assembly and Digital Source assembly. Comparing the data sent (FEDATA) to the data returned (FERET2) can determine the presence of a functional channel 2 Analog Input assembly and channel 2 A21 A/D Converter assembly.

FERET3. Front-end Return 3 — This serial data line returns the configuration data to the A30 Digital Source assembly. This line is FELOOP3 renamed FERET3 between the A35 Analog Source assembly and Digital Source assembly. Comparing the data sent (FEDATA) to the data returned (FERET3) can determine the presence of a functional Analog Source and A36 Trigger assembly.

FSA1 - FSA2. Frequency Sample — These are the system sample clocks. These clocks operate at 25.6 MHz. FSA2 is offset 10 nanoseconds from FSA1.

FSAAD. Frequency Sample A/D — This is the system sample clock for the A21 A/D Converter assembly. This clock operates at 25.6 MHz.

FSASRC. Frequency Sample Source — This is the system sample clock for the A35 Analog Source assembly. This clock operates at 25.6 MHz.

G. Green — This line contains the video information for the color green.

GTCLK. Gated Clock — This is a 6.4 MHz, CMOS-level signal. This signal provides timing for the A36 Trigger assembly during triggered measurements. This signal is only active for about 400 cycles once per measurement.

INTEN . Intensity — This line sets the A100 Display assembly's intensity.

LOCKED . Locked — This line goes low when the A60 Frequency Reference assembly locks to the external reference input. nEXTREF is low when an external reference is connected to the rear panel BNC.

nADCOVR1. ADC Overload 1 — This line goes low when the channel 1 input to the A21 A/D Converter assembly's ADC exceeds its positive or negative limit.

nADCOVR2. ADC Overload 2 — This line goes low when the channel 2 input to the A21 A/D Converter assembly's ADC exceeds its positive or negative limit.

nDFVLD1. Digital Filter Valid 1 — This line goes low when DFI1 and DFR1 are valid.

nDFVLD2. Digital Filter Valid 2 — This line goes low when DFI2 and DFR2 are valid.

nEXTREF. External Reference — This line goes low when the A60 Frequency Reference assembly detects an external reference. A transition on this line in either direction forces nFEERR low. LOCKED goes low when the A60 Frequency Reference assembly locks to the external reference.

nFEERR. Front-end Error — This line goes low when the serial path on the A10 Input, A21 A/D Converter, A35 Analog Source, or A36 Trigger assembly requires attention. A low on this line sets an interrupt flag on the A30 Digital Source assembly.

nFEPROG. Front-end Program — A low on this line configures the gate arrays on the A21 A/D Converter and A36 Trigger assemblies for programming.

nHLFRNG1. Half Range 1 — A low on this line indicates that the channel 1 input exceeded its positive or negative half-range limit.

nHLFRNG2. Half Range 2 — A low on this line indicates that the channel 2 input exceeded its positive or negative half-range limit.

nHSYNC. Horizontal Synchronization — A low on this line causes a horizontal retrace on the A100 Display assembly. Between each nHSYNC pulse, 576 pixels are sent to the Display assembly.

nOFFWR. Offset Write — A low on this line enables a write operation on the offset bus (OFF[6:0]).

nOVRRNG1. Over Range 1 — A low on this line indicates that the channel 1 input exceeded its positive or negative over-range limit.

nOVRRNG2. Over Range 2 — A low on this line indicates that the channel 2 input exceeded its positive or negative over-range limit.

nSBG[0]. System Bus Grant — This line goes low when the A40 CPU assembly grants control of the system bus to the A47 DSP/Display Controller assembly.

nSBR[0] . System Bus Request — This line goes low when the A47 DSP/Display Controller assembly requests control of the system bus.

nSBRDS[0]. System Board Select 0 — A low on this line selects the A47 DSP/Display Controller assembly. This line goes low when the assembly controlling the system bus wants to address the DSP/Display Controller assembly.

nSBRDS[1]. System Board Select 1 — A low on this line selects the A30 Digital Source assembly. This line goes low when the assembly controlling the system bus wants to address the Digital Source assembly.

nSBRDS[2]. System Board Select 2 — A low on this line selects the A71 Pass Through assembly. This line goes low when the assembly controlling the system bus wants to address the Pass Through assembly.

nSBRDS[3] . System Board Select 3 — A low on this line selects the A50 Digital Filter assembly. This line goes low when the assembly controlling the system bus wants to address the Digital Filter assembly.

nSBRDS[5]. System Board Select 5 — A low on this line selects the A55 Sample RAM or optional A56 Expanded Sample RAM assembly. This line goes low when the assembly controlling the system bus wants to address the Sample RAM or Expanded Sample RAM assembly.

nSBRDS[6]. System Board Select 6 — A low on this line selects the optional A43 Expanded Memory assembly. This line goes low when the assembly controlling the system bus wants to address the Expanded Memory assembly.

nSBS. System Bus Strobe — This line goes low during a write cycle when the address and data lines are valid.

nSDSACK[1:0]. System Data Strobe Acknowledge — These lines tell the assembly controlling the system bus when the selected assembly reads from or writes to the system data bus. During a write cycle, the selected assembly places data on the system data bus and forces one or both of these lines low. During a read cycle, the selected assembly reads the data on the system data bus and forces one or both of these lines low. These lines also indicate the data size. When both nSDSACK0 and nSDSACK1 go low, 32 bits of data are valid on SD0-31. When nSDSACK0 is high and nSDSACK1 goes low, 16 bits of data are valid on SD16-31. When nSDSACK0 goes low and nSDSACK1 is high, 8 bits of data are valid on SD24-31.

nSINT[7:0]. System Interrupt — These are the system bus interrupt lines. A low on nSINT[7:5] interrupts the A47 DSP/Display Controller assembly. A low on nSINT[4:0] interrupts the A40 CPU assembly. On the CPU assembly, nSINT[4] has the highest priority and nSINT[0] has the lowest priority.

nSRST. System Reset — A low on this line resets the digital logic on all the assemblies. This line pulses low during power-up and power-down, and when the processor is externally reset.

nSTRIGa. System Trigger Analog — A high-to-low transition on this line provides the system with a synchronous trigger. This line goes low when trigger conditions have been met. This line goes high after the trigger is armed.

nSYNCa. Synchronous Analog — This line synchronizes local oscillator circuits on the A50 Digital Filter assembly and A30 Digital Source assembly.

nTRIG. Trigger — When this trigger mode is selected, a low on this line triggers the analyzer. This line is ignored when this trigger mode is not selected. The A30 Digital Source, A50 Digital Filter, and A43 Expanded Memory assemblies can force this line low.

nVSYNC. Vertical Synchronization — A low on this line causes a vertical retrace on the A100 Display assembly.

OFF[6:0]. Offset — These are the offset data lines. The A35 Analog Source assembly converts these data lines to the source offset voltage.

PTA. Pretrigger Acquired — A high on this line starts the A36 Trigger assembly's trigger state machine sequencing. This line goes high after the A55 Sample RAM or A56 Expanded Sample RAM assembly acquires enough data for pretriggering. After nSTRIGa goes low, this line goes low to clear the arm trigger condition.

R. Red — This line contains the video information for the color red.

SA[31:0] . System Address — This is the system address bus. The A40 CPU assembly and A47 DSP/Display Controller assembly use these lines to address different circuits on all digital assemblies.

SCLK. System Clock — This is a 24 MHz clock. This clock synchronizes the transfer of data on the system bus.

SD[31:0]. System Data — These are the system bus bidirectional data lines. During a system bus cycle, these lines transmit data between the digital assemblies.

SRnW. System Read Write — A low on this line enables a write operation on the system bus (SD[31:0]).

SSIZ[1:0]. Data Size — These lines determine the size of the operand. When SSIZ0 is high and SSIZ1 is low, the operand size is 8 bits. When SSIZ0 is low and SSIZ1 is high, the operand size is 16 bits. When both SSIZ0 and SSIZ1 are high, the operand size is 24 bits. When both SSIZ0 and SSIZ1 are low, the operand size is 32 bits.

SYNCPS. Synchronize Power Supply — This is a 377.953 kHz signal. This signal synchronizes the A95 Main Power Supply assembly with the analyzer.

TPSD . Trigger Partial Sample Delay — This serial data line is an 10-bit representation of the time between the selected trigger and FSA2 multiplied by approximately 250. This serial data line is used during triggered measurements and during the calibration routine.

A101 Disk Drive

The following table lists signals routed between the A101 Disk Drive assembly and the A42 Memory assembly. This table shows several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Disk Drive Signals	Pin(s)	A42 P3	A101
DIR	17	S	•
DR0	25	S	•
DR1	23	S	•
DRIVESEL	21, 29	S	•
DSKCHG	1	•	S
HEADSEL	3	S	•
INDEX	27	•	S
MOTOR ON	19, 31	S	•
nDISKIN	22	•	S
nHIDENS	33	•	S
RDATA	5	•	S
STEP	15	S	•
TRK0	9	•	S
WDATA	13	S	•
WGATE	11	S	•
WPROT	7	•	S
+5 V	24, 26, 28	•	•
Gnd	2-20 (even)	•	•
Not Used	30, 32, 34	—	—

S This assembly is the source of the signal.
• This assembly uses the signal.
— This assembly does not use this signal.

DIR. Direction – This line sets the direction for the disk head. A high on this line sets the direction away from the spindle. A low on this line sets the direction toward the spindle.

DR0 - DR1. Drive Select – When DR0 and DR1 are low, the A101 Disk Drive assembly is enabled.

DRIVESEL. Drive Select – A low on this line selects the A101 Disk Drive assembly.

DSKCHG. Disk Change – This line goes low when a flexible disk is removed from the A101 Disk Drive assembly. This line remains low until a flexible disk is installed and STEP goes low.

HEADSEL. Head Select – A low on this line selects the lower disk drive head. A high on this line selects the upper disk drive head.

INDEX. Index – This line pulses low with each revolution of the flexible disk.

MOTOR ON. Motor On – A low on this line turns on the disk drive motor.

nDISKIN. Disk In – This line goes low when a flexible disk is inserted in the A101 Disk Drive assembly.

nHIDENS. High Density Select – This line goes low when a high density flexible disk is inserted in the A101 Disk Drive assembly.

RDATA. Read Data – This line pulses low for each bit detected on the flexible disk.

STEP. Step – A low on this line moves the disk drive head. When STEP and DIR are low, the head moves toward the disk spindle. When STEP is low and DIR is high, the head moves away from the disk spindle.

TRK0. Track 00 – This line is low when the head is positioned over track 0 on the flexible disk.

WDATA. Write Data – When WGATE is low, a low pulse on this line writes a bit to the disk.

WGATE. Write Gate – When this line is low, information may be written to the A101 Disk Drive assembly under control of the WDATA line.

WPROT. Write Protect – This line is low when a write-protected disk is installed in the A101 Disk Drive assembly.

Interface Connectors

This section describes the signals at the interface connectors.

HPIB

The following table lists signals at the HPIB connector (A42 J5 or optional A43 J1). A description of each signal follows the table.

HPIB Connector Signals	Pin
ATN	11
DAV	6
DIO1	1
DIO2	2
DIO3	3
DIO4	4
DIO5	13
DIO6	14
DIO7	15
DIO8	16
EOI	5
IFC	9
NDAC	8
NRFD	7
REN	17
SRQ	10
Shield	12
Logic Gnd	24
GND6	18
GND7	19
GND8	20
GND9	21
GND10	22
GND11	23

The descriptions that follow for the HPIB lines are general descriptions only. For a detailed description of how the analyzer interprets the HPIB lines, see the *Agilent 89400 Series HPIB Command Reference*.

ATN . Attention — This line is controlled by the controller in charge. When this line is low, the DIO lines contain interface commands. When this line is high, the DIO lines contain data.

DAV. Data Valid — This line goes low when valid data is on the bus and NRFD is high. This line is controlled by the HPIB controller.

DIO1 — DIO8. Data Input/Output — These are inverted data lines that conform to IEEE specification IEEE-488. When ATN is low, these lines contain interface commands. When ATN is high, these lines contain data.

EOI. End or Identify — If ATN is high, a low on this line marks the end of a message block. If ATN is low, a low on this line requests a parallel poll.

IFC. Interface Clear — This line goes low to halt all current operations on the bus, unaddress all other devices, and disable serial poll. The system controller becomes the controller in charge. This line was used only during development.

NDAC. Not Data Accepted — This line goes high when the DIO lines have been latched by the acceptor.

NRFD. Not Ready for Data — This line goes high when the acceptor is ready to accept data.

REN. Remote Enable — This line is low when the HPIB has control and high during local operation.

SRQ. Service Request — This line is low when a device on the HPIB needs service.

Serial 1 and Serial 2

Serial 1 and Serial 2 are identical, 9-pin, EIA-574 ports. Both ports can interface with printers or plotters. The following table lists signals at the Serial 1 and Serial 2 ports (A42 J3 and A42 J4). A description of each signal follows the table.

Serial 1 and Serial 2 Connector Signals	Pin
CTS	8
DTR	4
RTS	7
RxDATA	2
TxDATA	3
Logic Gnd	5
Not Used	1, 6, 9

CTS. Clear To Send — This line goes high when the peripheral device is ready.

DTR . Data Terminal Ready — This line goes high when the analyzer is ready.

RTS. Request To Send — This line is tied high. Some devices require this line to be high before transferring data.

RxDATA. Receive Data — This is the serial EIA-574 receive data line. This line transmits data from peripheral devices one byte at a time.

TxDATA . Transmit Data — This is the serial EIA-574 transmit data line. This line transmits data to peripheral devices one byte at a time.

Parallel Port

The Parallel Port is a 25-pin, Centronics port that can interface with printers or plotters. The following table lists signals at the Parallel Port connector (A30 J3). A description of each signal follows the table.

Signal Name	Pin
BUSY	11
nACK	10
nFAULT	15
nIP	16
nSTROBE	1
PA0	2
PA1	3
PA2	4
PA3	5
PA4	6
PA5	7
PA6	8
PA7	9
PE	12
SELECT	13
Logic Gnd	18
Not Used	14, 17, 19 - 25

BUSY. Busy – The printer sets this line high when it cannot receive data due to data entry, a full buffer, or error status.

nACK. Acknowledge – The printer pulses this line low after it accepts a byte of data and is ready for more data.

nFAULT. Fault – The printer sets this line low if it reaches an error state.

nIP. Input Prime – This line pulses low to reset the printer and clear the print buffer.

nSTROBE. Strobe – This line pulses low when a byte of data is ready. A low pulse on this line clocks the data into the printer.

PA0 - PA7. Printer Data Bus –This is the 8-bit parallel data bus. These lines transmit a byte of data to the printer.

PE. Paper Error – The printer sets this line high when it is out of paper.

SELECT. Selected – The printer sets this line high to indicate that it has been selected.

External Monitor

The following table lists signals at the External Monitor connector (A47 J2). A description of each signal follows the table.

External Monitor Connector Signals	Pin
EXTB	3
EXTG	2
EXTR	1
Logic Gnd	4 - 8, 10, 11
Not Used	9, 12, 15
nl Vsync	14
nl Hsync	13

EXTB. External Blue –This line contains the video information for the color blue.

EXTG. External Green –This line contains the video synchronization signal and the video information for the color green.

EXTR. External Red –This line contains the video information for the color red.

DIN Keyboard

The following table lists signals at the DIN keyboard connector (A80 P3). A description of each signal follows the table.

DIN Keyboard Connector Signals	Pin
KEYCLK	1
KEYDAT	3
+5 V	4
Logic Gnd	2
Not Used	5

KEYCLK. Keyboard Clock – This clock synchronizes the transfer of keyboard data from the external keyboard to the A42 Memory assembly.

KEYDAT. Keyboard Data – This is 8-bit serial data from an external keyboard to the A42 Memory assembly.

ThinLAN

The optional ThinLAN (BNC) port (A43 J2) allows the analyzer to be connected to the local area network (LAN).

AUI

The optional Attachment Unit Interface (AUI) port (A43 J4) allows the analyzer to be connected to the local area network (LAN). The following table lists signals at the AUI port. A description of each signal follows the table.

External Monitor Connector Signals	Pin
CI-A	2
CI-B	9
CI-S	1
CO-A	7
CO-B	15
CO-S	8
DI-A	5
DI-B	12
DI-S	4
DO-A	3
DO-B	10
DO-S	11
PG	shell
VC	6
VP	13
VS	14

CI-A — CI-B. Control In circuit A/B — These control lines transfer encoded signals from the A43 Expanded Memory assembly's LAN circuit.

CI-S. Control In circuit Shield — This line is connected to logic ground.

CO-A — CO-B. Control Out circuit A/B — These control lines transfer encoded signals to the A43 Expanded Memory assembly's LAN circuit.

CO-S. Control Out circuit Shield — This line is connected to logic ground.

DI-A — DI-B. Data In circuit A/B — These data lines transfer encoded signals from the A43 Expanded Memory assembly's LAN circuit.

DI-S. Data In circuit Shield — This line is connected to logic ground.

DO-A — DO-B. Data Out circuit A/B — These data lines transfer encoded signals to the A43 Expanded Memory assembly's LAN circuit.

DO-S. Data Out circuit Shield — This line is connected to logic ground.

PG. Protective Ground (Conductive Shell) — This line is connected to chassis ground.

VC. Voltage Common — This line is the ground return to the power source for VP.

VP. Voltage Plus — This line provides a voltage between +12 and +15 Vdc.

VS. Voltage Shield — This line is connected to logic ground.

7 Internal Test Descriptions

Internal Test Descriptions

This chapter describes the power-on test, calibration routine, fault log messages, and self tests. This chapter also contains a list of the HPIB commands for each self test.

Power-on Test Descriptions

The power-on test is run when the analyzer is powered up. The calibration routine is run immediately following the power-on test. If an error occurs during the calibration routine, a failure message is recorded in the fault log and test log. The power-on tests exercise circuits in the A40 CPU, A42 Memory, and A47 DSP/Display Controller assemblies. The power-on tests also check the presence and revision of the A10 Input, A21 A/D Converter, A30 Digital Source, A35 Analog Source, A36 Trigger, A50 Digital Filter, A55 Sample RAM or optional A56 Expanded Sample RAM, and A71 Pass Through assemblies. The high-level tests are also self tests (see ''Self-Test Descriptions'' on page page 7-13). If an error occurs during the high-level tests, an error message is entered in the test log.

Calibration Routine

The calibration routine measures the characteristics of the hardware, adjusts the hardware, and corrects measurement results when hardware adjustments are not possible. The entire analyzer is characterized with each calibration. This allows changes to the instrument configuration without performing a recalibration. The calibration routine occurs immediately following the power-on tests and periodically afterwards to compensate for any drift. With the exception of the auto-zero calibration data, all calibration results are stored in NVRAM on the A42 Memory assembly. Therefore, only auto-zero calibrations are necessary on power-on. To manually start the calibration routine, press [**System Utility**] [single cal]. To prevent the calibration routine from automatically occurring, press [**System Utility**] [auto cal **off**]. Preventing the calibration routine from occurring does not prevent auto-zero calibrations from occurring. To prevent auto-zero calibrations from automatically occurring, press [**System Utility**] [more cal setup] [auto zero cal **off**]. The calibration routine will not occur until manually enabled. However, auto-zero calibrations are enabled at power-on or preset.

If calibration fails because of a hardware failure, the calibration data in NVRAM is not updated and the calibration routine is repeated up to two more times. Each time calibration fails, a calibration failure message is added to the fault log. To view the fault log, press [**System Utility**] [more] [diagnostics] [service functions] 1125 [enter] [fault log]. To view the calibration correction curves, see page 1-. If calibration fails all three times, a calibration failure error message is displayed on the screen for approximately 5 seconds.

If you abort a self test before the self test is finished, the analyzer may fail its calibration routine. To prevent this from happening, press [**Preset**] or cycle power after you abort a self test.

The calibration routine performs the following calibrations:

- Front-end dc offset
- Front-end primary
- Front-end secondary
- Trigger delay counter
- Trigger dc offset
- Trigger delay
- Source amplitude
- Source dc offset
- Source dc offset gain

The front-end dc offset calibration determines the setting for the dc offset DAC on the A10 Analog Input assembly. The dc offset DAC compensates for the residual dc on each input channel by adding a dc signal of equal magnitude and opposite polarity to the residual signal. All signals are disconnected and the offset DAC is set to a nominal value. The residual dc is measured. The offset DAC is changed by a small amount and the residual dc is measured again. The two measurement results are used to compute the setting for the dc offset DAC. Ten offset calibrations are performed for each channel. The calibrations are performed on the -30 to -12 dBm ranges — once for ac coupling and once for dc coupling. The front-end dc offset calibration is an auto-zero calibration.

The front-end primary calibration performs six primary calibrations on each input channel. The primary calibrations are used to compute the correction vector for the frequency response (magnitude and phase) of the input at any given range. For each primary calibration, the A30 Digital Source assembly generates a calibration signal with a comb spectrum. Each component of the comb spectrum has a known amplitude and phase relative to the source trigger. The hardware is set up for the particular primary calibration and an auto-zero calibration is performed. Then, source triggering is enabled and time averaged measurements of the calibration signal are made. The calibration signal is inverted and another set of time averaged measurements are made.

The front-end secondary calibration is very similar to the primary calibrations except they are only performed at a single frequency point. They also differ in that the calibration hardware setup does not conform to a normal instrument setup that can be obtained from the front panel. The primary purpose of the secondary calibrations is to compensate for the gain and delay variations introduced by the two 20 dB attenuators and the 3/13 dB preamplifier on the A10 Input assembly.

The trigger partial delay counter calibration determines the characteristics of the trigger partial delay counter on the A36 Trigger assembly. Two numbers are needed to determine the characteristics of the counter — the minimum number the counter will return for zero trigger delay relative to the sample clock and the maximum number returned for a trigger with slightly less than one sample clock of delay. To determine these two numbers, the A30 Digital Source assembly generates a sine wave. Input triggering is selected and the trigger point is moved relative to the sample clock by adjusting the phase of the sine wave. The phase is adjusted until the maximum and minimum counts have been determined.

The trigger dc offset calibration determines the setting for the trigger offset DAC on the A10 Analog Input assembly. The trigger offset DAC compensates for the residual dc at the trigger point by adding a dc signal of equal magnitude and opposite polarity to the residual dc signal. On the A10 Analog Input assembly, the input signal is split with one path leading to the A36 Trigger assembly for input triggering. To determine the dc offset at the trigger point, the A30 Digital Source assembly generates a 1 MHz sine wave and a front-end dc offset calibration is performed. The trigger offset DAC is set to a nominal value and input triggering is selected. The amplitude of the sine wave near the trigger point is measured using a positive trigger slope and using a negative trigger slope. The trigger offset DAC is set to a slightly different value, and again the amplitude of the sine wave near the trigger point is measured using a positive trigger slope and a negative trigger slope. The measurement results are used to compute the setting for the trigger offset DAC. The trigger dc offset calibration is an auto-zero calibration.

The trigger delay calibration determines the amount of relative delay for input trigger, source trigger, and external trigger. The data is used to correctly position the time record (or spectrum phase) relative to the trigger event. The calibrator on the A35 Analog Source assembly generates an 800 kHz square wave. Source triggering is selected and the phase of the calibration signal at the fundamental frequency is determined. The measurement is then repeated using calibration triggering (closely mimics external triggering), and input triggering. The phase results are converted to delays and combined with the primary calibration data to determine an appropriate trigger correction.

The source amplitude calibration, source dc offset calibration, and source dc offset gain calibration are performed simultaneously. They provide the correction data necessary to generate a source signal with a known amplitude and dc offset. The source is turned off (all attenuators are in) and the residual dc in the input channel is measured. This value will be subtracted from the rest of the offset measurements. The A30 Digital Source assembly generates a 1.5 MHz sine wave, and the dc offset DAC on

the A35 Analog Source assembly is set to the nominal value corresponding to zero volts offset. The source amplitude and dc offset are measured. The dc offset DAC is then changed by a small amount, and the source amplitude and dc offset are measured again. The source amplitude is computed by averaging the two amplitude measurements and applying the corrections from the front-end primary calibrations. The two offset measurements are used to compute a DAC setting that will produce zero volts offset and also to compute the gain of the offset DAC.

Fault Log Messages

Calibration Failure. This error message occurs if the calibration routine generates correction vectors that exceed the maximum allowable error vectors or if the calibration routine is bypassed because of a hardware failure.

Calibration Failure — Channel 1 Auto Zero. This error message occurs if the calibration routine is unable to reduce channel 1 residual dc to the allowable level. The calibration routine adjusts the dc offset correction DAC on the channel 1 A10 Analog Input assembly.

Calibration Failure — Channel 2 Auto Zero. This error message occurs if the calibration routine is unable to reduce channel 2 residual dc to the allowable level. The calibration routine adjusts the dc offset correction DAC on the channel 2 A10 Analog Input assembly.

Calibration Failure — Channel 1 dc Gain. This error message occurs if the calibration routine generates correction vectors for channel 1 dc gain that exceed the maximum allowable error vectors.

Calibration Failure — Channel 2 dc Gain. This error message occurs if the calibration routine generates correction vectors for channel 2 dc gain that exceed the maximum allowable error vectors.

Calibration Failure — Channel 1 Flatness. This error message occurs if the calibration routine generates correction vectors for channel 1 flatness that exceed the maximum allowable error vectors.

Calibration Failure — Channel 2 Flatness. This error message occurs if the calibration routine generates correction vectors for channel 2 flatness that exceed the maximum allowable error vectors.

Calibration Failure — Channel 1 Pads. This error message occurs if the calibration routine generates correction vectors for the attenuator pads on the channel 1 A10 Input assembly that exceed the maximum allowable error vectors.

Calibration Failure — Channel 2 Pads. This error message occurs if the calibration routine generates correction vectors for the attenuator pads on the channel 2 A10 Input assembly that exceed the maximum allowable error vectors.

Calibration Failure — Channel 1 Trigger. This error message occurs if the calibration routine cannot correct channel 1 trigger delay or trigger dc offset within allowable limits.

Calibration Failure — Channel 2 Trigger. This error message occurs if the calibration routine cannot correct channel 2 trigger delay or trigger dc offset within allowable limits.

Calibration Failure — Source Level. This error message occurs if the calibration routine generates correction vectors for the source level that exceed the maximum allowable error vectors.

Calibration Hardware Timeout. This error message occurs if an assembly did not respond within one second of receiving a command during the calibration routine.

Channel 1 Control Path Failure. This error message occurs if the data sent by the A30 Digital Source assembly to the channel 1 A21 A/D Converter assembly does not match the data returned from the channel 1 A10 Input assembly.

Channel 2 Control Path Failure. This error message occurs if the data sent by the A30 Digital Source assembly to the channel 2 A21 A/D Converter assembly does not match the data returned from the channel 2 A10 Input assembly.

CPU Board Bus Error. This error message occurs if the A40 CPU assembly failed to return its identification number over the system bus.

CPU Failure. This error message occurs if the A40 CPU assembly's power-on test fails.

Digital Filter Board Bus Error. This error message occurs if the A50 Digital Filter assembly failed to return its identification number over the system bus.

Digital Filter Board Failure. This error message occurs if the power-on test could not detect the A50 Digital Filter assembly.

Digital Source Board Bus Error. This error message occurs if the A30 Digital Source assembly failed to return its identification number over the system bus.

Digital Source Board Failure. This error message occurs if the power-on test could not detect the A30 Digital Source assembly.

Display/ DSP Board Bus Error. This error message occurs if the A47 DSP/Display assembly failed to return its identification number over the system bus.

Display Failure. This error message occurs if the A47 DSP/Display Controller assembly's display controller test fails.

DSP Failure. This error message occurs if the A47 DSP/Display Controller assembly's power-on digital signal processor test fails.

Extended RAM / Additional I/ O Board Failure. This error message occurs if the power-on test could not detect the A43 Expanded Memory assembly.

Extended RAM Board Bus Error. This error message occurs if the A43 Expanded Memory assembly failed to return its identification number over the memory bus.

Floppy Controller Timeout. This error message occurs if the A42 Memory assembly's disk drive controller did not respond within 10 ms of receiving a command.

Input Tripped. This error message occurs if the A10 Input assembly detects an overload at its input. The Input assembly disconnects the overload signal from its input.

Internal Control Path 3 Failure. This error message occurs if the data sent by the A30 Digital Source assembly to the A36 Trigger assembly does not match the data returned from the A35 Analog Source assembly.

Internal Disk Trk0 Failure. This error message occurs if the A101 Disk Drive assembly did not locate track 0 (as indicated by a low on T00n) when instructed by the A42 Memory assembly to move to track 0.

Memory Board Bus Error. This error message occurs if the A42 Memory assembly failed to return its identification number over the memory bus.

Memory Board Failure. This error message occurs if the A42 Memory assembly's power-on test fails.

NVRAM or Battery Failure. This error message occurs if the A42 Memory assembly's IIC Controller determined that non-volatile RAM or RAM battery power failed.

Pass Thru Board Bus Error. This error message occurs if the A71 Pass Through assembly failed to return its identification number over the system bus.

Pass Thru Board Failure. This error message occurs if the power-on test could not detect the A71 Pass Through assembly.

Real Time Clock Timeout. This error message occurs if the A42 Memory assembly's real-time clock did not respond within one second of receiving a command.

Sample/ Capture RAM Board Bus Error. This error message occurs if the A55 Sample RAM or optional A56 Expanded Sample RAM assembly failed to return its identification number over the system bus.

Sample/ Capture RAM Board Failure. This error message occurs if the power-on test could not detect the A55 Sample RAM or optional A56 Expanded Sample RAM assembly.

Source Tripped. This error message occurs if the A35 Analog Source assembly detects an over-voltage signal connected to its output. The Analog Source assembly disconnects its output from the over-voltage signal.

System Error . This error message occurs if the A40 CPU assembly detects a run-mode error. Any assembly on the system bus or the A42 Memory assembly can cause a run-mode error.

System Error during Calibration. This error message occurs if a system error occurs during the calibration routine.

Trigger Board Failure. This error message occurs if the power-on test could not detect the A36 Trigger assembly.

Self-Test Descriptions

Twenty-eight self tests are available that can be run in groups or individually. The following table lists the group of self tests that are run when you select [functional tests], [all]. This group does not include any of the self tests that require a formatted flexible disk. The table lists the assemblies used by each self test and shows the assembly that would most likely cause the failure. To run these self tests in the order shown, press the following keys:

[**System Utility**]
[more]
[diagnostics]
[service functions]
1125
[enter] (only required the first time you select service functions)
[functional tests]
[all]

To run a single self test, press the softkey shown in the table instead of [all]. To determine the key path for the self-test softkeys, see "Self-Test Menu Map and HPIB Commands" starting on page 7-22

Certain instrument malfunctions cause multiple self-test failures. Therefore, to determine the most likely cause when more than one self test fails, look at the following table for assemblies common to all failing self tests.

Functional Tests All Self-Test Group

Self Test	Assemblies																
	A61	A40	A42	A47	A43	A101	A60	A71	A55/ A56	A36	A30	A50	A21 Ch1	A35	A10 Ch1	A21 Ch2	A10 Ch2
Mult fctn peripheral †	O	X	O														
NVRAM †	O	O	X														
Real time clock †	O	O	X														
DIN controller †	O	O	X														
Disk controller	O	O	X			X											
Front panel †	O	O	X														
DSP/ bus †	O	O	O	X	0			0	X		0	0					
Additional hardware †																	
Expanded Memory/ Additional I/ O	0	0	0	0	X												
Digital Source	0	0	0	0							X						
Analog Source	0	0	0	0							0			X			
Trigger	0	0	0	0						X	0			0			
Sample RAM	0	0	0	0					X		0						
Pass Thru	0	0	0	0				X	0		0						
Lo/ Df	0	0	0	0			0		0		0	X					
Channel 1 Front End	0	0	0	0			0		0		0	0	X		X		
Channel 1 ADC	0	0	0	0			0		0		0	0	X		X		
Channel 2 Front End	0	0	0	0			0		0		0	0				X	X
Channel 2 ADC	0	0	0	0			0		0		0	0				X	X
DSP processor †	O	O	O	X			O		0								
Full sample RAM †	O	O	O	O			O	0	X	X	0	0	0	0	0		
Digital source	O	O	O	O			O		X		X	X	0		0		
Digital filter	O	O	O	O			O	O	X		X	X	O	0	X		
ADC	O	O	O	O			O	O	O		O	O	X	O	X	X	X
Analog source	O	O	O	O			O	O	O	0	O	O	X	X	X		0
Input	O	O	O	O			O	O	O	0	O	O	O	O	X	0	X
Calibration	O	O	O	O			O	O	O	0	O	O	O	O	0	0	0

X This assembly is the most likely cause of the failure message.
0 This assembly is used by the self test but is not the most likely cause of the failure message.
No symbol means that the assembly is not used by the self test
† High -level power-on test, the power supply and display are used in every test

Self Tests that Perform a Measurement

The following self tests perform measurements:

- ADC
- analog source
- digital filter
- digital source
- input

These self tests measure the internal circuitry by routing signals via internal test paths to the data acquisition hardware. The measurements bypass any standard corrections and do not perform calibration data corrections. Therefore, all self-test measurements using analog data have limits larger than the standard calibration tolerances. Some tests monitor overloads, others require spectrum data, and others require time record data. After the data is collected, it is compared to an internal reference specification to determine if the self test passed or failed. The pass or fail information along with any additional information is placed in the Test Log.

Individual Self-Test Descriptions

[adc]. This test checks the ADC on the A21 A/D Converter assembly. This test consists of 7 tests — positive overflow, negative overflow, positive limit, negative limit, 1st pass, 2nd pass, and zero. The positive and negative overflow tests set up the ADC test mode to cause positive and negative overflows, then check the A50 Digital Filter assembly's digital filter for interrupt flags. The positive and negative limit tests check the ADC's positive and negative limits. The 1st and 2nd pass tests connect the calibration signal from the A35 Analog Source assembly to the A10 Analog Input assembly. The 1st pass test sets the 2nd pass result to zero and checks the signal into the ADC for the proper value and the A50 Digital Filter assembly's gate array for interrupts or overloads. The 2nd pass test sets the 1st pass result to zero and checks the signal into the ADC for the proper value and the Digital Filter assembly's gate array for interrupts or overloads. The zero test checks for minimal output when the signal is removed.

[additional hardware] . This test checks the hardware revision and address of all assemblies on the system bus and front-end loops.

[analog source] . This test uses channel 1 to check the A35 Analog Source assembly. This test consists of 5 tests — input, calibration and source; impedance; attenuator; reconstruction filter; and dc offset DAC. The input, calibration and source test measures the calibration signal and the source signal. The nominal value of the calibration signal is -17 dBm in a single channel analyzer and –14 dBm in a two channel analyzer. The nominal value of the source signal is –16 dBm in a single channel analyzer and –13 dBm in a two channel analyzer. The impedance test measures both the 50 ohm and 75 ohm source impedance. The attenuator test measures the source level with all attenuator pads switched out and with each attenuator pad switched in. The reconstruction filter test measures the source signal with and without the reconstruction filter to verify that the filter corrects for rolloff. The dc offset DAC test measures the dc offset at zero, with the DAC value stepped up, and with the DAC value stepped down. A dc coupling problem on the A10 Input assembly could cause the dc offset DAC test to fail.

[AUI LAN loop back]. This test checks the LAN controller on the A43 Expanded Memory assembly. This softkey is only visible on analyzers with option UFG/UTH providing the LAN firmware is compatible with the analyzer's firmware. In this test, the A40 CPU assembly writes to the A43 Expanded Memory assembly, then reads the registers for verification. This test also checks the AUI connector using an external

loopback mode. See ''To troubleshoot system interconnect and LAN failures'' on page 1-96 for the procedure to use with this softkey.

[calibration]. This test runs the calibration routine. See ''Calibration Routine'' earlier in this chapter for a description of the calibration routine.

[digital filter]. This test checks the A50 Digital Filter assembly. The full sample RAM test should pass before doing this test. This test consists of 3 tests — IF trigger memory, baseband, and zoom. The IF trigger test does a full memory test of IF trigger memory. The baseband test configures the channel 1 A21 A/D Converter assembly to provide a square wave to the digital filters and makes a baseband measurement. The baseband test then configures the A30 Digital Source assembly to provide a square wave to the digital filters and makes a baseband measurement. The zoom test configures the channel 1 A21 A/D Converter assembly to provide a square wave to the digital filters and makes a zoomed measurement.

[digital source]. This test checks the A30 Digital Source assembly. The full sample RAM test and digital filter test should pass before doing this test. This test consists of 5 tests — full memory, real RAM square wave, imaginary RAM square wave, LO sine wave, and zoom. The full memory test checks the source real and imaginary RAMS and the gate RAM. The real RAM square wave test loads the real source RAM with an 800 kHz square wave. The signal is connected to the A50 Digital Filter assembly and measured. The nominal value for the 800 kHz signal is -10 dBm. The imaginary RAM square wave test loads the imaginary source RAM with an 800 kHz square wave. The signal is connected to the A50 Digital Filter assembly and measured. The LO sine wave test configures the digital source for sine wave generation. The zoom test checks the digital source in zoom mode.

[DIN controller]. This test checks the DIN controller on the A42 Memory assembly. During this test, interrupts are masked and the key queue is disabled. The CPU assembly reads the DIN controller's data port and command port, then clears the data port. An internal diagnostic test is also performed on the DIN controller. This test does not require the external keyboard to be connected.

[disk controller]. This test checks the floppy controller on the A42 Memory assembly. In this test, the A40 CPU assembly writes to the floppy controller, then reads the registers for verification.

[DSP/ bus]. This test checks for the presence of the A47 DSP/Display Controller assembly by reading a register. This test then tries to load a kernel into the DSP processor. This test also checks DSP to main memory communications by loading a program into the DSP that will write some test values back into the main memory.

[DSP processor]. This test checks the DSP on the A47 DSP/Display Controller assembly. This test is a more thorough check of DSP functionality than the DSP/bus test.

[front panel]. This test checks the front panel interface on the A42 Memory assembly. In this test, the A40 CPU assembly reads a memory register in the front panel interface.

[full sample RAM]. This test verifies that the sample RAM on the A55 Sample RAM assembly or optional A56 Expanded Sample RAM assembly is functional. This test consists of four tests — full memory test, counter 2 interrupt/counter test, single channel software triggered measurement test, and two channel software triggered measurement test. The full memory test checks both RAMs. The counter 2 interrupt/counter test checks the counter 2 interrupt and address generator. The single channel software triggered measurement test checks pre-triggering and post-triggering on counter 2. The two channel software triggered measurement test checks pre-triggering and post-triggering on counter 1.

[HPIB controller]. This test checks the HPIB interface on the A42 Memory assembly. In this test, the A40 CPU assembly sets the HPIB interface to a listen only state, then tests for a listen only state.

[HPIB interconnect]. This test checks the HPIB interface on the optional A43 Expanded Memory assembly. This softkey is only visible in analyzers with option UFG. In this test, the A40 CPU assembly sets the HPIB interface to a listen only state, then tests for a listen only state.

[input]. This test checks the analyzer's input channels. In this test, each input measures a signal from the calibrator and a signal from the source. The nominal value of the calibration signal is -17 dBm in a single channel analyzer and -14 dBm in a two channel analyzer. The nominal value of the source signal is –16 dBm in a single channel analyzer and –13 dBm in a two channel analyzer.

[LAN controller]. This test checks the LAN controller on the A43 Expanded Memory assembly. In this test, the A40 CPU assembly writes to the A43 Expanded Memory assembly, then reads the registers for verification. This test also checks two internal loop-back modes.

[LAN ROM]. This test checks the LAN ROM on the A43 Expanded Memory assembly. This softkey is only visible in analyzers with option UFG. In this test, the checksums for the ROM are computed and compared with the values recorded in the ROM at the time it was programmed.

[long conf self test]. This test performs most of the self tests. The tests are performed in the following order:

[mult fctn peripheral]
[NVRAM]
[real time clock]
[disk controller]
[DIN controller]
[front panel]
[DSP/ bus]
[additional hardware]
[DSP processor]
[full sample RAM]
[digital source]
[digital filter]
[ADC]
[analog source]
[input]
[trigger]
[calibration]

[mult fctn peripheral]. This test checks the multi-function peripheral (MFP) on the A40 CPU assembly. In this test, the CPU writes to the MFP, then reads the registers for verification.

[NVRAM]. This test checks the non-volatile RAM (NVRAM) on the A42 Memory assembly. In this test, the A40 CPU assembly writes to and reads from the NVRAM.

[parallel port loop back]. This test is currently not available.

[quick conf self test]. This test runs the calibration routine. Any calibration errors are entered in the Test Log. See ''Calibration Routine'',page 7-5 earlier in this chapter for a description of the calibration routine.

[random seek]. This test verifies that the A 101 Disk Drive assembly's head can move to a random sector on the flexible disk. In this test, the disk controller on the A40 CPU assembly instructs the disk-drive head to move to a random record. This test requires a formatted flexible disk.

[read]. This test verifies that the A101 Disk Drive assembly can read a flexible disk. In this test, the A40 CPU assembly's disk controller instructs the Disk Drive assembly to read the current record on the flexible disk. While the current record is being read, the disk controller monitors the RDDATAn signal to verify the read operation. The current record is set by the [seek record] test. This test requires a formatted flexible disk.

[read/ write]. This test verifies that the A101 Disk Drive assembly can read and write to a flexible disk. In this test, the A40 CPU assembly's disk controller instructs the Disk Drive assembly to read the current record on the flexible disk. While the current record is being read, the disk controller monitors the RDDATAn signal to verify the read operation. The disk controller then instructs the Disk Drive assembly to write to the current record. While the current record is being written to, the disk controller monitors the WDATAn signal to verify the write operation. The current record is set by the [seek record] test. This test requires a formatted flexible disk that is not write protected.

[read/ write all]. This test verifies that the A101 Disk Drive assembly can read and write to all records of a flexible disk. In this test, the A40 CPU assembly's disk controller instructs the A101 Disk Drive assembly to read every available record on the flexible disk (excluding privileged tracks). While the flexible disk is being read, the disk controller monitors the RDDATAn signal to verify the read operation. The disk controller then instructs the A101 Disk Drive assembly to write to every available record on the flexible disk (excluding privileged tracks). While the flexible disk is being written to, the disk controller monitors the WDATAn signal to verify the write operation. This test stops on the first error. The execution time for this test depends upon the size of the disk. For example, if there are no errors, this test takes approximately one hour for a double-sided, low-density disk. This test requires a formatted flexible disk that is not write protected.

[real time clock]. This test verifies that the real-time clock on the A42 Memory assembly is able to communicate and that the time is changing.

[restore]. This test verifies that the A101 Disk Drive assembly's head can move away from track 0, then back to track 0. In this test, the A40 CPU assembly's disk controller instructs the disk-drive head to move away from track 0, then back to track 0. The disk controller monitors the T00n signal to verify the move operation. This test requires a formatted flexible disk.

[sample RAM]. This test checks the sample RAM on the A55 Sample RAM assembly or optional A56 Expanded Sample RAM assembly. In this test, the A40 CPU assembly writes to a sample RAM address, then reads the address for verification.

[seek record]. This test verifies that the A101 Disk Drive assembly's head can move to a user specified record on the flexible disk. In this test, the disk controller on the A40 CPU assembly instructs the disk-drive head to move to a user specified record. The user specified record number must be in the range of valid record numbers. The default record number is 0. This test requires a formatted flexible disk.

[serial port controller]. This test verifies that the RS-232 interface on the A40 CPU assembly is capable of sending and receiving data. In this test, the RS-232 interface is placed in its internal loop back mode. A test string is sent, received, and checked for integrity.

[serial port loop back]. This test checks the serial port connectors. In this test, the user connects the transmit data line to the receive data line. Data is sent out on the transmit data line and read back on the receive data line. See ''To troubleshoot serial port failures'' on page 1- for the procedure to use with this softkey.

[ThinLAN loop back]. This test checks the LAN controller on the A43 Expanded Memory assembly. This softkey is only visible on analyzers with option UFG providing the LAN firmware is compatible with the analyzer's firmware. In this test, the A40 CPU assembly writes to the A43 Expanded Memory assembly, then reads the registers for verification. This test also checks the ThinLan connector using an external loopback mode. See ''To troubleshoot system interconnect and LAN port failures'' on page 1- for the procedure to use with this softkey.

[trigger]. This test checks the trigger circuitry on the A36 Trigger assembly. This test consists of four tests—range, mode, level, and slope. The range test connects the source to channel 1 and 2, then increases the amplitude while monitoring the half range, overload, and ADC overload bits. The mode test monitors the trigger MUX during measurements that use channel 1 trigger, channel 2 trigger, calibration trigger, source trigger, channel 1 IF trigger, and channel 2 IF trigger. The level test connects the source to channel 1 and 2, then compares the measured trigger level to the trigger level. The trigger level is checked at 0 V, 100 mV, and -100 mV. The slope test connects a low frequency sine wave from the source to channel 1 and 2, then measures the minimum and maximum values for positive and negative trigger slopes.

Self-Test Menu Map and HPIB Commands

The analyzer's self tests can be run from the front panel or from a controller via HPIB. To run a test from the front panel, press [**System Utility**] [more] [diagnostics] [service functions] 1125 [enter] followed by the appropriate softkeys shown in the following table. To run a test via HPIB, send the equivalent HPIB command shown in the table.

Self Test	HPIB Command
[diagnostics]	–
[quick conf self test]	SYST:TEST:QCON
[long conf self test]	SYST:TEST:LCON
[fault log]	DIAG:FLOG ON| OFF
[test log]	DIAG:TLOG ON| OFF
[clear test log]	SYST:TLOG:CLE
[service functions]	–
[special test modes]	–
[I/O]	–
[disk drive]	–
[ALL]	DIAG:MODE:DISK:ALL
[restore]	DIAG:MODE:DISK:REST
[random seek]	DIAG:MODE:DISK:RAND
[seek record]	DIAG:MODE:DISK:SEEK n
[read]	DIAG:MODE:DISK:READ
[read/write]	DIAG:MODE:DISK:WRIT
[read/write all]	DIAG:MODE:DISK:RWR
[serial port loop back]	DIAG:MODE:LBAC
[parallel port loop back]	DIAG:MODE:PAR:LBAC
[ThinLAN loop back]	DIAG:MODE:TLAN:LBAC
[AUI LAN loop back]	DIAG:MODE:ALAN:LBAC

Self Test	HPIB Command
[functional tests]	–
[ALL]	SYST:TEST:LCON
[power-up tests]	–
[ALL]	DIAG:FUNC:POW:ALL
[mult fctn peripheral]	DIAG:FUNC:POW:MFP
[NVRAM]	DIAG:FUNC:POW:NVR
[real time clock]	DIAG:FUNC:POW:RTCL
[DIN controller]	DIAG:FUNC:POW:DCON
[front panel]	DIAG:FUNC:POW:FPAN
[DSP/ bus]	DIAG:FUNC:POW:DSPB
[additional hardware]	DIAG:FUNC:POW:HARD
[DSP processor]	DIAG:FUNC:POW:DSP
[sample RAM]	DIAG:FUNC:POW:SRAM
[LAN ROM]	DIAG:FUNC:POW:SRAM
[I/ O]	–
[ALL]	DIAG:FUNC:IO:ALL
[disk controller]	DIAG:FUNC:IO:DISK
[DIN controller]	DIAG:FUNC:IO:DIN
[serial port controller]	DIAG:FUNC:IO:SER
[HPIB controller]	DIAG:FUNC:IO:HPIB
[HPIB interconnect]	DIAG:FUNC:IO:HPIB:INT
[LAN controller]	DIAG:FUNC:IO:LAN
[full sample RAM]	DIAG:FUNC:SRAM
[digital filter]	DIAG:FUNC:DFIL
[digital source]	DIAG:FUNC:DSO
[ADC]	DIAG:FUNC:ADC
[analog source]	DIAG:FUNC:ASO
[input]	DIAG:FUNC:INP
[trigger]	DIAG:FUNC:TRIG
[calibration]	DIAG:FUNC:CAL

8 Backdating

Backdating

This chapter documents earlier instrument configurations and associated servicing procedures. Use the following table to adapt this guide to your instrument.

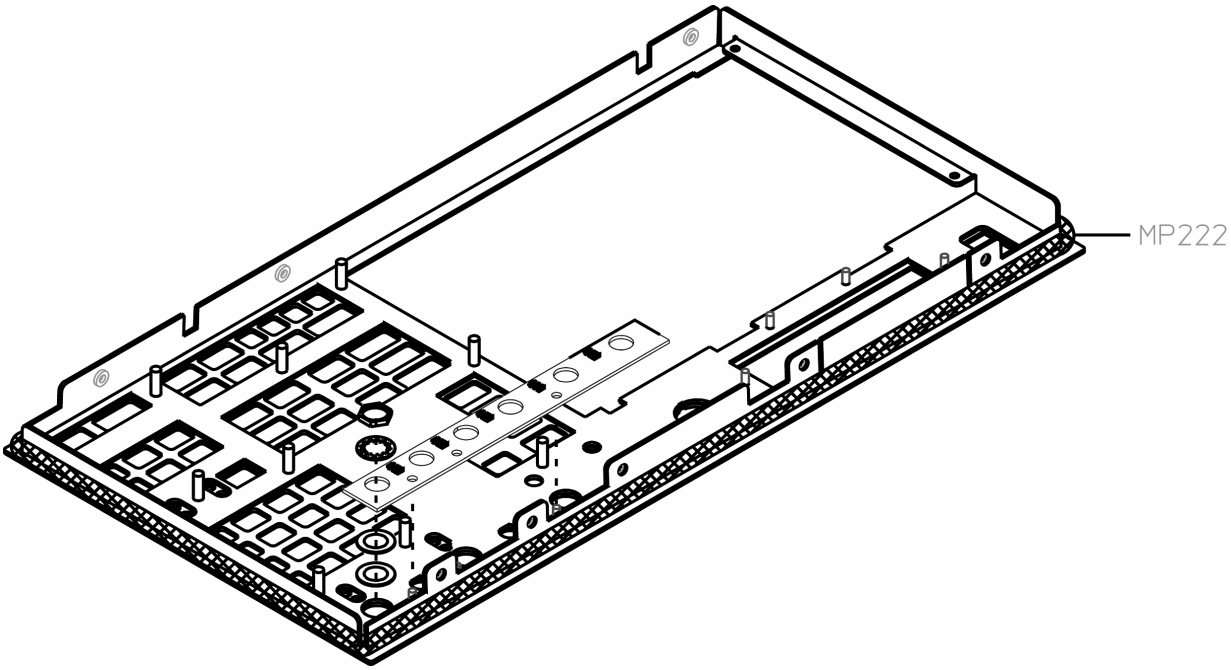
If instrument serial number is lower than	Make change
3331A00282	A and B
3342A00370	B
US40514521	C

Change A

On page 4-14, change the part number of MP201 to 89410-64302 for instruments with revision ''A'' A80 Keyboard assembly.

Change B

MP222 (Agilent 8160-0799) was used but was not required on these instruments.



Change C

Use the following table to adapt the changes to your manual:

Chapter	Page Number	Instructions
1	1-24, 1-25, 1-32, 1-48	Change all the reference designations of A47 to A45.
	1-33, 1-48, 1-67, 1-72	Change all the reference designations of A71 to A70.
	1-31, 1-33, 1-37, 1-38, 1-39, 1-44, 1-49, 1-52, 1-53, 1-55, 1-64, 1-65, 1-67, 1-69, 1-70, 1-71, 1-72, 1-74, 1-75	Change all the reference designations of A21 to A20.
	1-26 to 1-29	Delete.
2	2-3, 2-22, 2-23, 2-34	Change all the reference designations of A21 to A20.
	2-36	Add the following line: To Adjust Clock, refer to Chapter 8, page 8-5.
		Add the following line: To Adjust Display, refer to Chapter 8, page 8-7.
3	3-5	Change all the reference designations of A47 to A45.
	3-5	Change all the reference designations of A21 to A20.
	3-6	Change all the reference designations of A71 to A70.
	3-6	Change all the reference designations of A81 to A80.
	3-9 to 3-11	Replace "To remove the Flat Panel Display" with "To remove display" on page 8-9.

	3-24 to 3-28	Delete.
	3-92	Delete.
4	4-6, 4-7, 4-8	Replace with the following pages: page 8-11 through page 8-13 for Assemblies, Parts List and Cables.
	4-11	Replace with page 8-14 for "Assembly Covers and Brackets".
	4-12	Replace with page 8-15 for "Front Panel Parts".
5	5-1	Change all the reference designations of A81 to A80.
	5-1, 5-5, 5-7, 5-21, 5-22, 5-32,5-43, 5-44, 5-49, 5-52, 5-53, 5-63	Change all the reference designations of A71 to A70.
	5-1, 5-10, 5-39, 5-46, 5-51	Change all the reference designations of A47 to A45.
	5-1, 5-5, 5-7, 5-8, 5-11, 5-13, 5-16, 5-18, 5-21, 5-22, 5-24, 5-30, 5-49, 5-52, 5-53, 5-63	Change all the reference designations of A21 to A20.
	5-5	Repalce with "Overall Block Diagram" on page 8-18.
	5-42	Replace with "A45 DSP/ Display Controller Block Diagram" on page 8-20.
	5-55	Replace with "A80 Keyboard Block Diagram" on page 8-21
	5-57	Delete.
6	6-3, 6-15, 6-16, 6-17, 6-18, 6-21, 6-22, 6-36	Change all the reference designations of A47 to A45.
	6-1, 6-2, 6-3, 6-12	Change all the reference designations of A81 to A80.
	6-5, 6-15, 6-16, 6-17, 6-18	Change all the reference designations of A82 to A100.
	6-3, 6-5, 6-15, 6-16, 6-17, 6-18, 6-20, 6-21, 6-22, 6-27	Change all the reference designations of A71 to A70.
	6-3, 6-5, 6-6, 6-8, 6-15, 6-16, 6-17, 6-18, 6-22, 6-24, 6-25, 6-26	Change all the reference designations of A21 to A20.
	6-3, 6-4	Replace with "Assembly Locations and Connections" on page 8-22.
7	7-3, 7-9, 7-13, 7-15, 7-16	Change all the reference designations of A21 to A20.
	7-3, 7-10, 7-13	Change all the reference designations of A71 to A70.
9	9-10, 9-27	Change all the reference designations of A21 to A20.
	9-22, 9-27	Change all the reference designations of A71 to A70.

To adjust clock

This procedure adjusts the A61 Clock assembly's 16 MHz phase locked loop. The 16 MHz phase locked loop provides the reference clock for the Agilent 89410A.

Equipment Required:

Digital multimeter
Frequency counter
Extender board, Agilent part number 89410-B1008
1 MW 10:1 oscilloscope probe
BNC(f)-to-dual banana plug
Flat-edge adjustment tool, Agilent part number 8710-1928

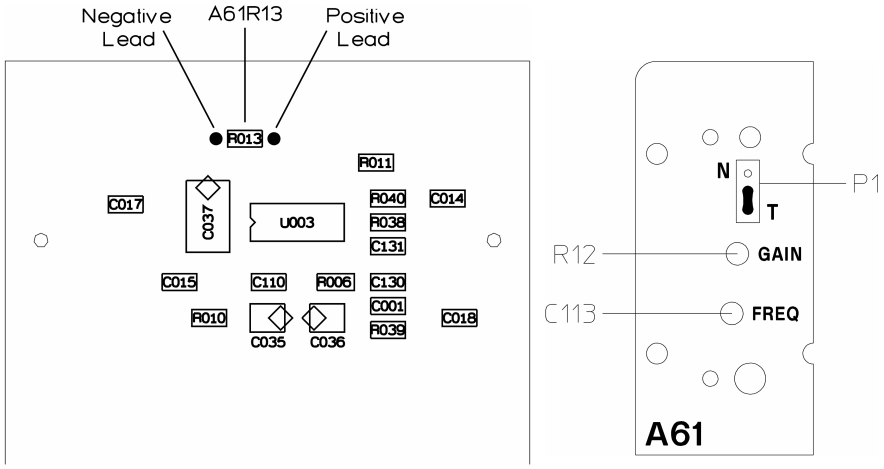
1 Place the A61 Clock assembly on an extender board.

   a Set the power switch to off (O).

   b Remove screws holding the A61 Clock assembly in the card nest.

   c Place the assembly on an extender board.

   d Set the power switch to on (l).



2 Adjust A61 R12.

   a Connect the digital multimeter leads across R13 as shown in the illustration.

   b Adjust A61 R12 for 400 ±20 mVdc using the flat-edge adjustment tool.

3 Step 3. Adjust A61 C113.

   a Move jumper A61 P1 to test position.

   b Connect the frequency counter to jumper using a 1 MW 10:1 probe.

   c Set the frequency counter to 1 MW input.

   d Adjust A61 C113 for a frequency counter reading of 3.2 MHz ±50 Hz using the flat-edge adjustment tool.

   e Move jumper A61 P1 back to normal position.

   f Set the frequency counter to 1 second gate time.

   g Check that the frequency counter reads 3.2 MHz ±15 Hz.

4 Reinstall the A61 Clock assembly.

   a Set the power switch to off (O).

   b Place the assembly in the card nest.

This completes the A61 Clock assembly adjustments.

To adjust display

This procedure adjusts the A100 Display assembly's alignment, intensity, and focus. These adjustments are optional and should rarely be required. Do not perform these adjustments unless the display is visibly out of adjustment.

Equipment Required:

Plastic screw driver, Agilent part number 8710-2056

1 Remove side cover.

   a Set the power switch to off (O).

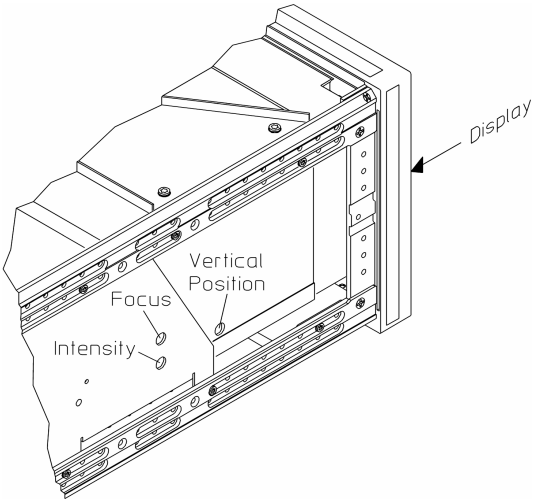
   b Remove screws holding the handle and side cover on the display side of the Agilent 89410A.

   c Remove the handle and side cover.

2 Adjust the display vertical position.

   a Set the power switch to on (l).

   b Adjust the vertical position control until the display is centered.



3 Adjust display focus.

   a Press the [**Preset**] hardkey.

   b Adjust the focus control for best readability.

4 Adjust display intensity.

   a Press the following keys:
   [**Display**]
   [more display setup]
   [color setup]
   [default system colors]
   [brightness]
   100
   [%]

   b The display should be bright with a black background. Only adjust the intensity control if the display is dim.
   The intensity level of the display is adjusted at the factory to be ≤150 NITs (without bezel). The life of the display may be reduced if the intensity level is set higher than 150 NITs.

5 Replace side cover.

   a Set the power switch to off (O).

   b Replace side cover and handle.

This completes the A100 Display assembly adjustments.

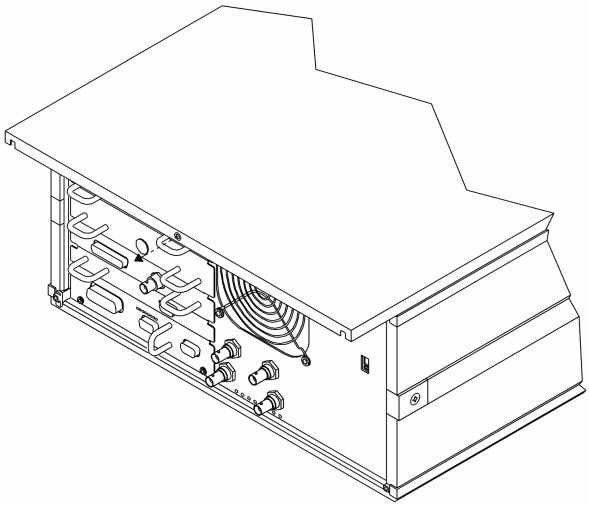
To remove display

1

Remove the front panel (see ''To remove front panel''page 3-10).

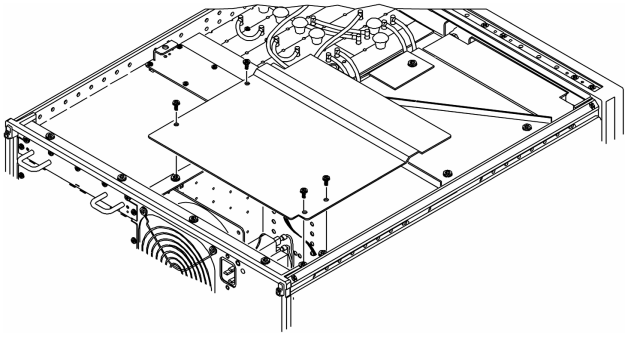
2

Using a T-15 torx driver, remove the screw from the back of the top cover. Slide the cover off.



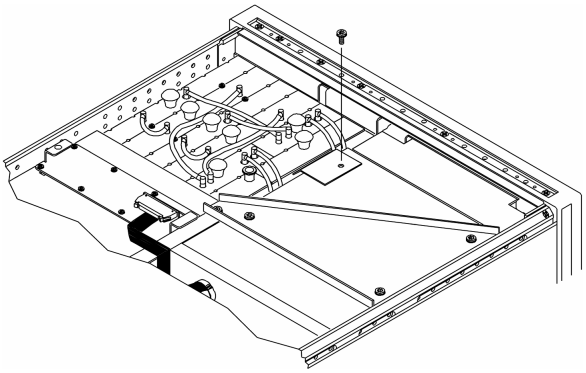
3

Using a T-15 torx driver, remove the four screws from the power supply shield. Remove the power supply shield.



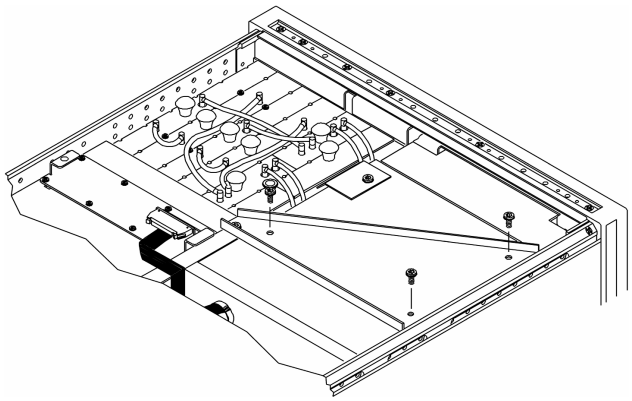
4

Using a T-15 torx driver, remove the screw from the assembly bracket.



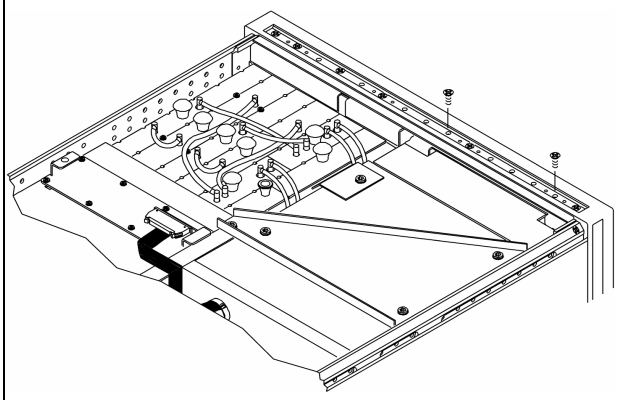
5

Using a T-15 torx driver, remove the three screws from the display bracket.



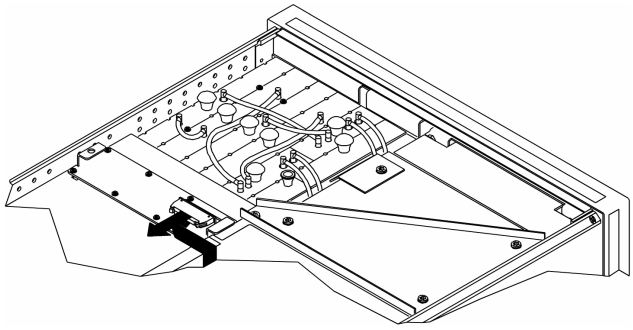
6

Using a 2 point pozidriv, remove the two screws from the front frame.



7

Disconnect the display cable from the A90 Digital Motherboard.



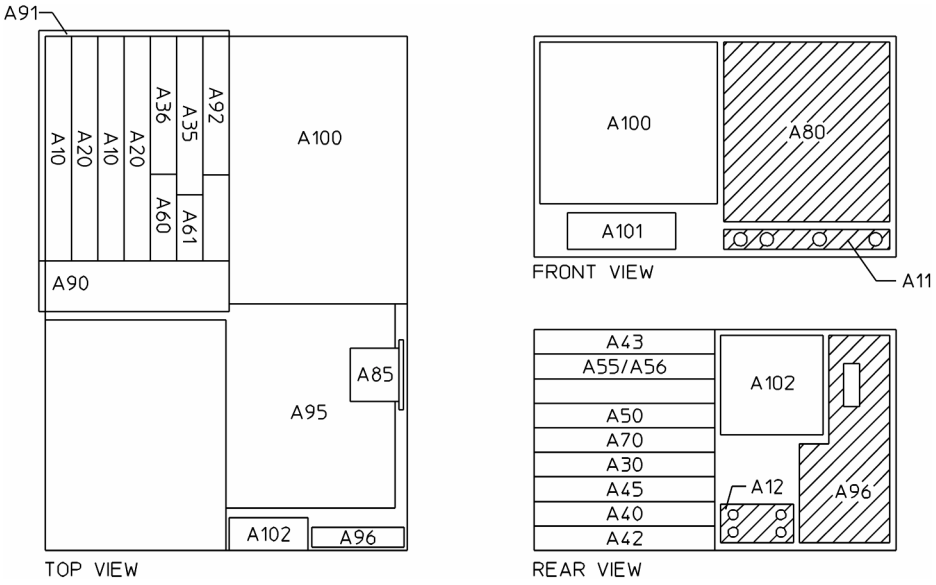
8

Remove the cables from the clamps on the back of the display. Move the power cable out of the way and slide the display part way out. Disconnect the display cable from the A95 Main Power Supply assembly.

Assemblies

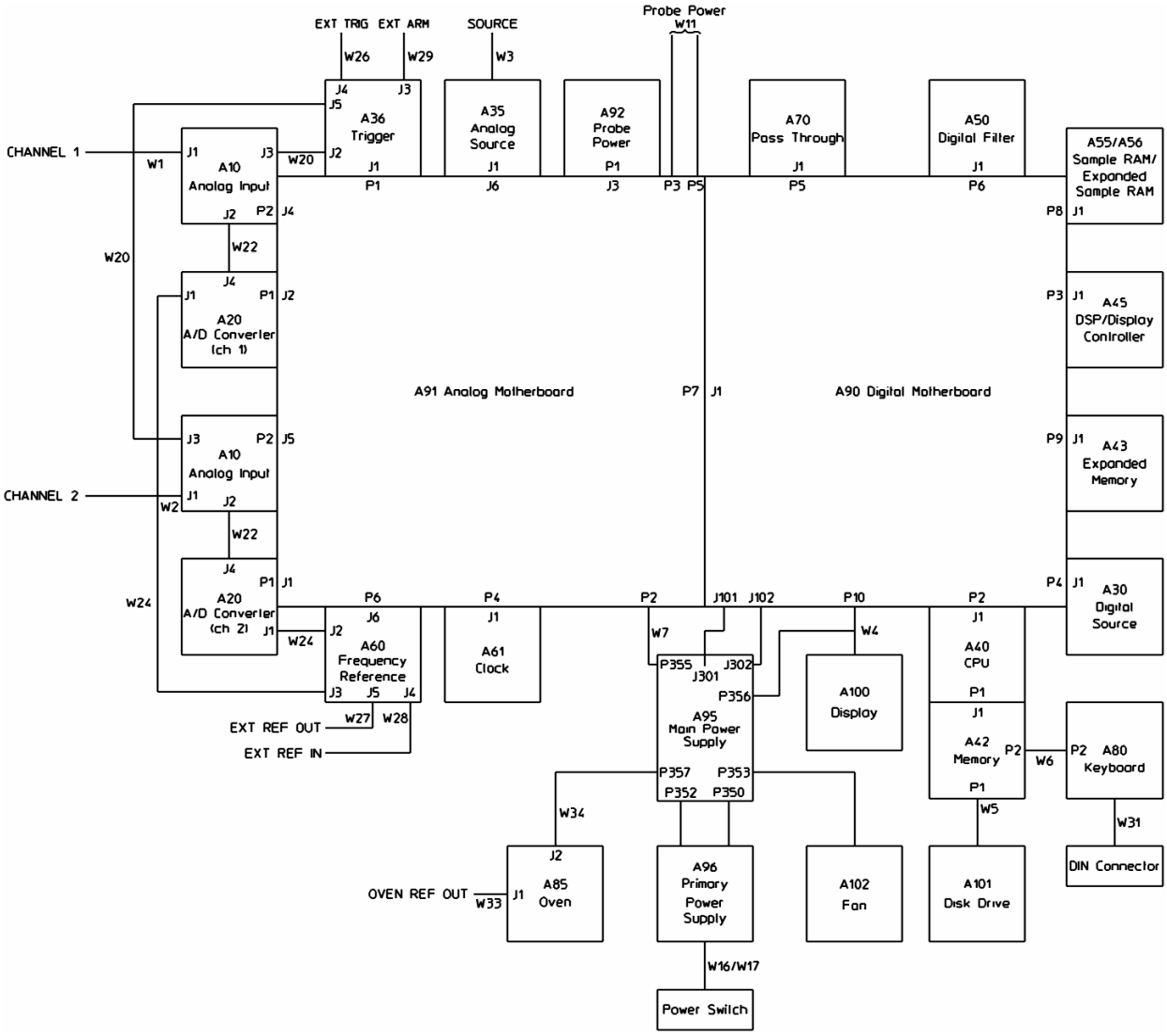
After replacing an assembly, see ''What to do after replacing an assembly'' in chapter 3,page 3-5 for required adjustments and performance tests.

CAUTION: Do not replace the A40 CPU assembly and the A42 Memory assembly at the same time. Option and configuration information will be lost if both assemblies are replaced at the same time. If both assemblies must be replaced, power up the instrument after replacing one assembly and before replacing the other assembly.



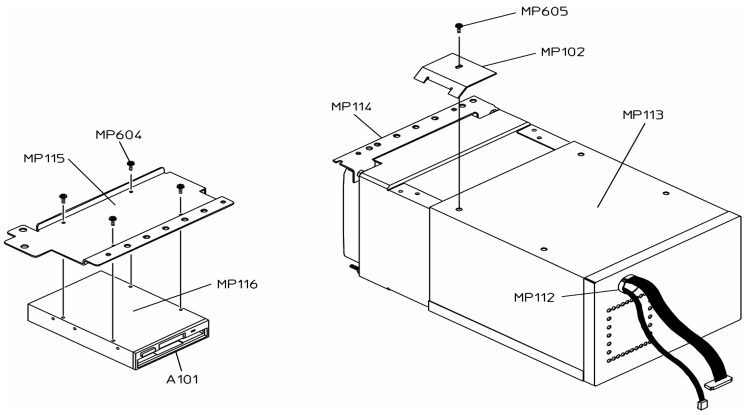
Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A10	89410-69510	9	1	ANALOG INPUT	28480	89410-69510
A11	89410-66511	4	1	FRONT PANEL CONNECTOR	28480	89410-66511
A12	89410-66512	5	1	REAR PANEL CONNECTOR	28480	89410-66512
A20	89410-69520	1	1	A/D CONVERTER	28480	89410-69520
A30	89410-69530	3	1	DIGITAL SOURCE	28480	89410-69530
A35	89410-69535	8	1	ANALOG SOURCE †	28480	89410-69535
A36	89410-69536	9	1	TRIGGER	28480	89410-69536
A40	89410-69540	5	1	CPU	28480	89410-69540
A42	89410-69542	7	1	MEMORY	28480	89410-69542
A43	89410-69543	2	1	EXPANDED MEMORY OPTION UFG	28480	89410-69543
A45	89410-69545	0	1	DSP/DISPLAY CONTROLLER	28480	89410-69545
A50	89410-69550	7	1	DIGITAL FILTER	28480	89410-69550
A55	89410-69555	2	1	SAMPLE RAM	28480	89410-66555
A56	89410-69556	3	1	EXPANDED SAMPLE RAM OPTION AY9	28480	89410-66556
A60	89410-69560	9	1	FREQUENCY REFERENCE	28480	89410-69560
A61	89410-66561	4	1	CLOCK	28480	89410-66561
A70	89410-69570	1	1	PASS THROUGH	28480	89410-69570
A80	89410-66580	7	1	KEYBOARD	28480	89410-66580
A85	89410-66585	2	1	OVEN OPTION AY5	28480	89410-66585
A90	89410-66590	9	1	DIGITAL MOTHERBOARD	28480	89410-66590
A91	89410-66591	0	1	ANALOG MOTHERBOARD	28480	89410-66591
A92	89410-66592	1	1	PROBE POWER	28480	89410-66592
A95	89410-69595	0	1	MAIN POWER SUPPLY	28480	89410-69595
A96	89410-66596	5	1	PRIMARY POWER SUPPLY	28480	89410-66596
A100	5180-8484	7	1	DISPLAY 7.5" COLOR	28480	2090-0210
A101	0950-2141	9	1	DISC 3.5" FLOPPY DRIVE †	10421	SMD-340
A102	3160-0845	4	1	FAN-ASSY	28480	03561-68501

Cables



Assembly Covers and Brackets

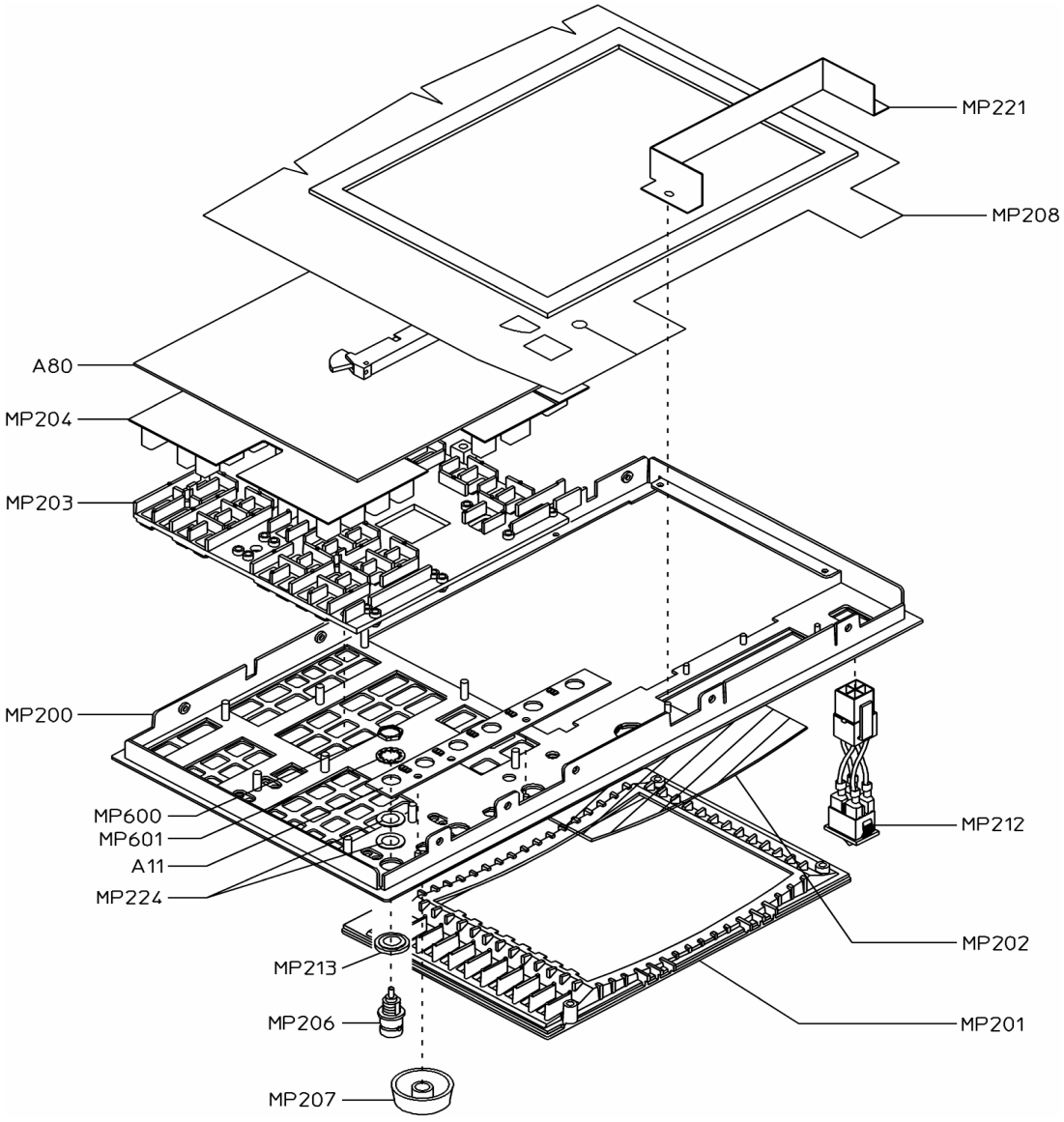
The reference designator for the nuts that fasten MP114 to the A100 Display assembly is MP613. The reference designator for the screws that fasten the front of the A40 CPU assembly to the A42 Memory assembly is MP621. The reference designator for the screws that fasten the rear of the A40 CPU assembly to the A42 Memory assembly is MP604. The reference designator for the screws that fasten the assembly covers to the top of the analyzer is MP615. The reference designator for the screws that fasten the assembly covers to the rear of the analyzer is MP604.



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP100	89410-44702	9	1	GSKT BUMPER PCB PORON	28480	89410-44702
MP102	89410-01215	9	1	SHTF-RETAINER92 BRD	28480	89410-01215
MP110	89410-04175	6	1	SHTF COVER-EMPTY SLOT # 2 STLN	28480	89410-04175
MP111	89410-04176	7	1	SHTF CVR-EMPTY SLOT # 1 STLN	28480	89410-04176
MP112	0400-0085	1	1	GROMMET-SNAP BUSHING .875-IN-ID	03480	2163 BLK (SB-1093-14)
MP113	89410-00603	7	1	SHTF SHIELD-CRT MU METAL MU	28480	89410-00603
MP114	89410-01202	4	1	SHTF BKT-DISPLAY FRONT AL	28480	89410-01202
MP115	89410-01201	3	1	SHTF BKT-DISK AL	28480	89410-01201
MP116	4040-2321	2	1	DUST COVER DISC DRIVE	28480	4040-2321
MP120	89410-04110	9	1	SHTF CVR-10 BD ALSK	28480	89410-04110
MP121	89410-04120	1	1	SHTF CVR-20 BD ALSK	28480	89410-04120
	5180-0409	0	1	ASSY COVER SPRING CLIP	28480	5180-0409

Front Panel Parts

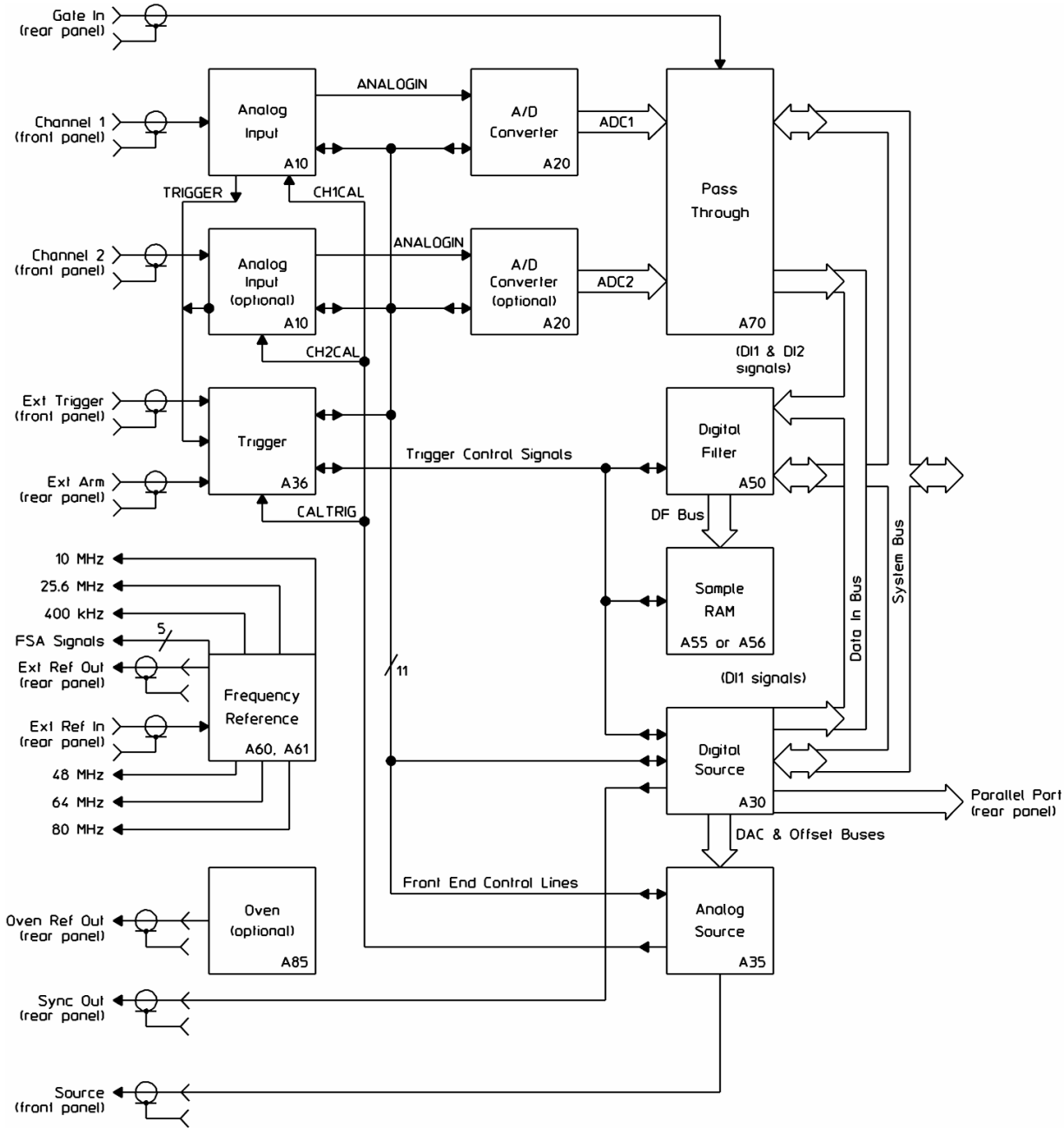
The reference designator for the nuts that fasten A11 to MP200 is MP612. The reference designator for the screws that fasten MP201 and A80 to MP200 is MP214. The reference designators for the screws that fasten the front panel to the chassis are MP217 and MP219.



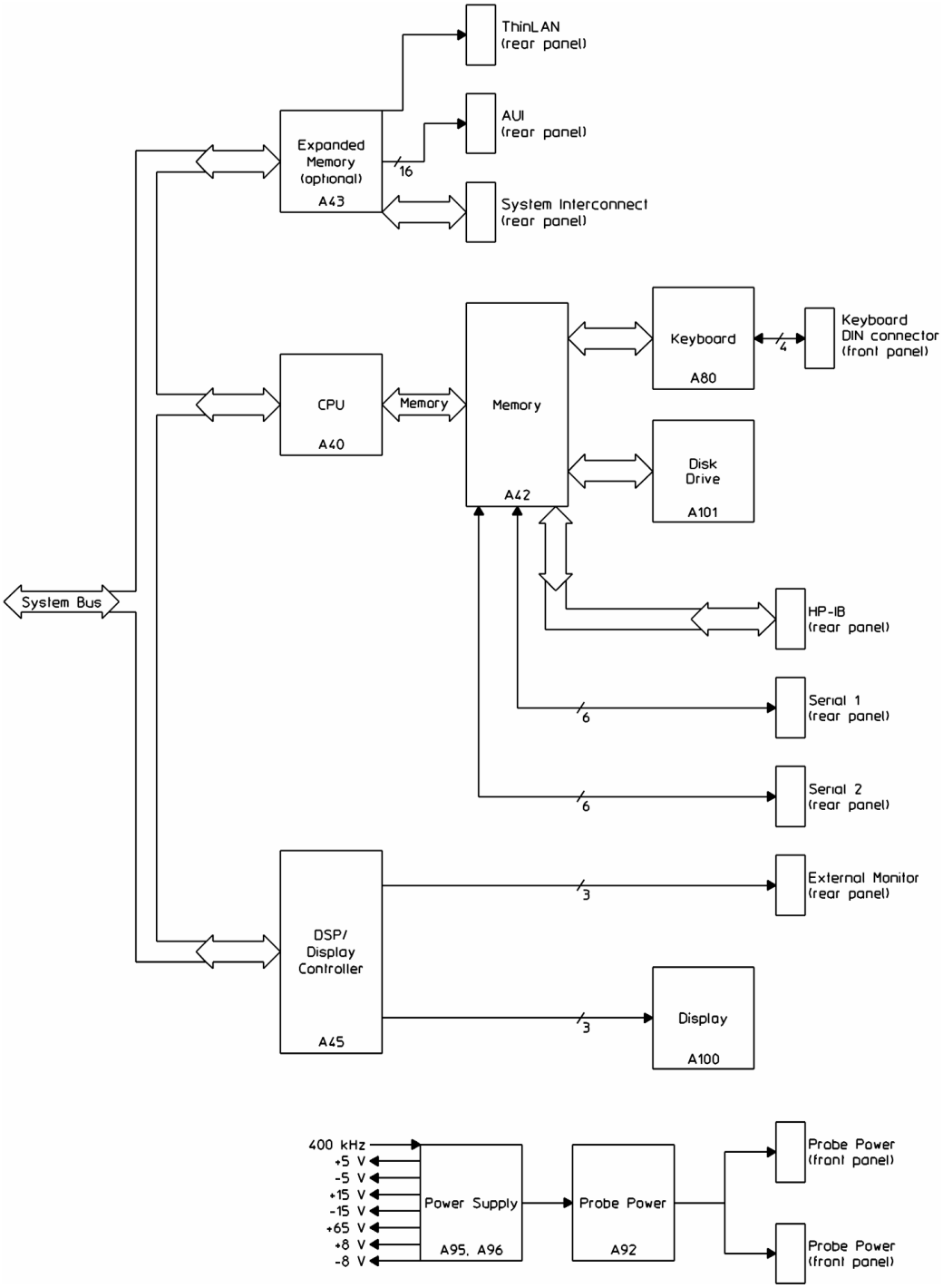
Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP200	89410-64332	8	1	PNL-FRT DRS ALPT	28480	89410-64311
MP201	89410-44303	5	1	MOLD-BEZEL	28480	89410-44302
MP202	89410-49301	4	1	LNZ-CLEAR RFI WINDOW W/ BUSSBAR	28480	89410-49301
MP203	89410-44703	8	1	MOLDED-KEYBOARD SPACER	28480	89410-44701
MP204	89410-41902	4	1	KYPD ELASTOMERIC "89410A"	28480	89410-41901
MP205	89410-34315	3	1	PLT-NAME "89410A VECTOR SIGNAL	28480	89410-34301
MP205	89441-34315		1	PLT-NAME "89441V VECTOR SIGNAL	28480	89441-34315
MP205	89440-34316		1	PLT-NAME "89441V VECTOR SIGNAL	28480	89440-34316
MP206	1250-2431	7	4	CON-ADAPT BNC-SMB PNL MNT	90949	903-430A518
MP207	08712-40005	7	1	MOLD RPG KNOB	28480	01650-47401
MP208	89410-00603	5	1	GSKT RFI BAND-AID BEZEL	28480	89410-00601
MP210	89410-43001	9	18	MOLD-LIGHT PIPE KEYPAD	28480	89410-43001
MP211	1251-4933	0	2	CONN-POST TYPE 2.5-PIN-SPCG CRP	27264	22-01-1033
MP212	3101-3587	1	1	SW—RKR	09328	WI32/ 217MZ
MP213	5041-5896	7	4	MOLD INSULATOR-CONN	28480	5040-0345
MP214	0515-0430	3	14	SCREW-MACHINE ASSEMPLY M3 X 0.5 6MM-LG	28480	0515-0430
MP217	0515-2039	2	1	SCR-MCH M3.5 8MM LG FHTX SST *	28480	0515-2039
MP219	0515-1946	8	8	SCR-MCH M3.0 6MM LG FHTX SST	28480	0515-1946
MP221	89410-01207	9	1	SHTF TUNNEL-RFI AL	28480	89410-01207
MP224	3050-0067	9	8	WASHER-FL MTLC 5/ 16 IN .375-IN-ID	73734	31-550

Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP400	5021-5837	2	4	CSTG STRT-CRNR 497.8D II AL	28480	5021-5837
MP401	5021-5808	7	1	CSTG FRM-RR FM 221.5H II AL	28480	5021-5808
MP402	35650-46603	0	1	CSTG FRM-FRT FM 221.5H II+ALPT	28480	35650-46603
MP403	89410-01203	5	1	SHTF BKT-CRT AL	28480	89410-01203
MP404	89410-01210	4	1	SHTF BKT-CARDNEST FRONT TOP AL	28480	89410-01210
MP405	89410-01211	5	1	SHTF BKT-CARDNEST FRONT BTM AL	28480	89410-01211
MP406	89410-04101	8	1	SHTF COVER-PLENUM AL	28480	89410-04101
MP407	89410-01204	6	1	SHTF BKT-SIDE AL	28480	89410-01204
MP408	89410-34302	4	1	LBL CABELING ANALOG CARDNEST:K	28480	89410-34302
MP409	89410-01209	1	1	SHTF-BRACKET92 BRDFRONT	28480	89410-01209

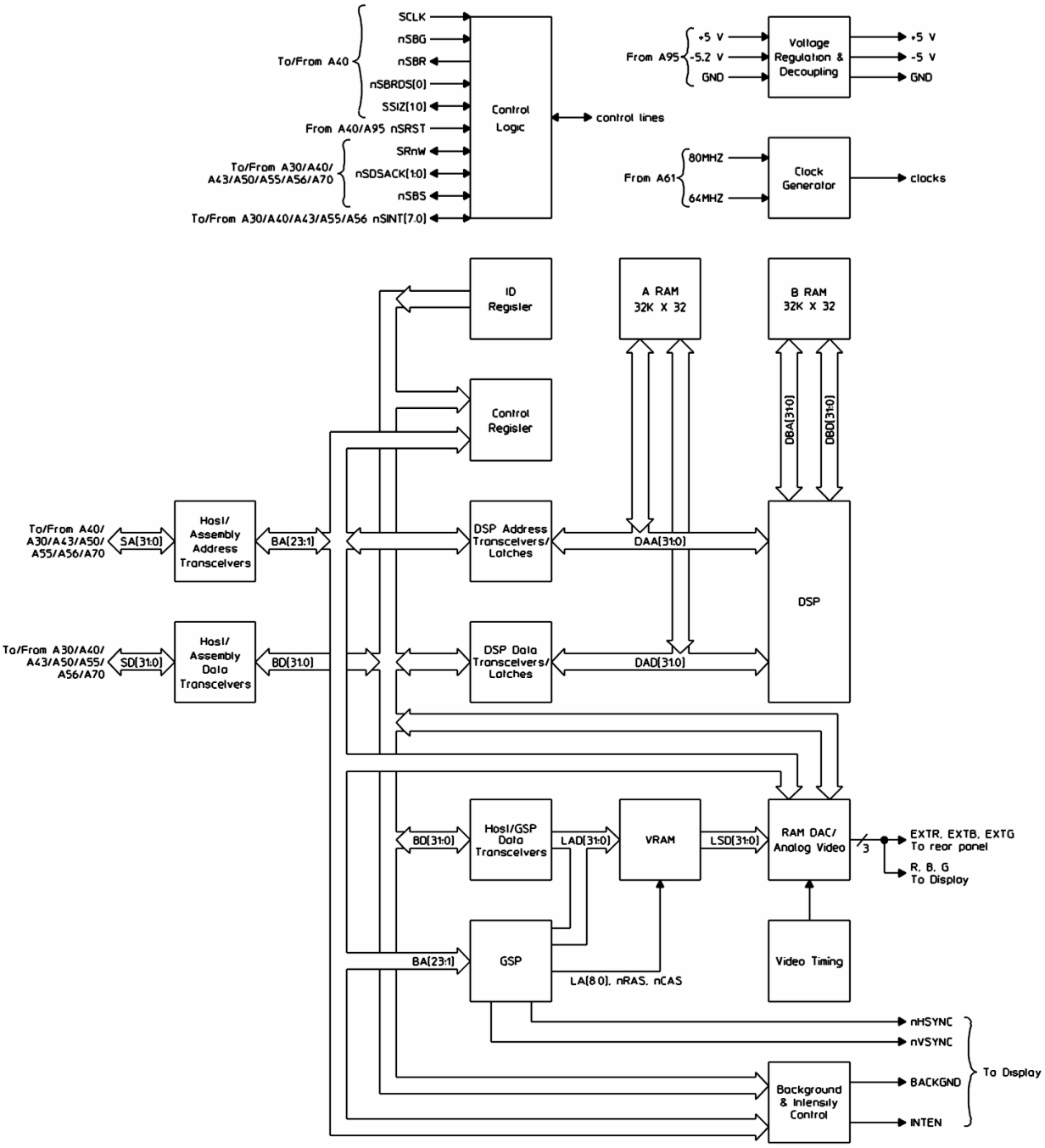
Overall Block Diagram



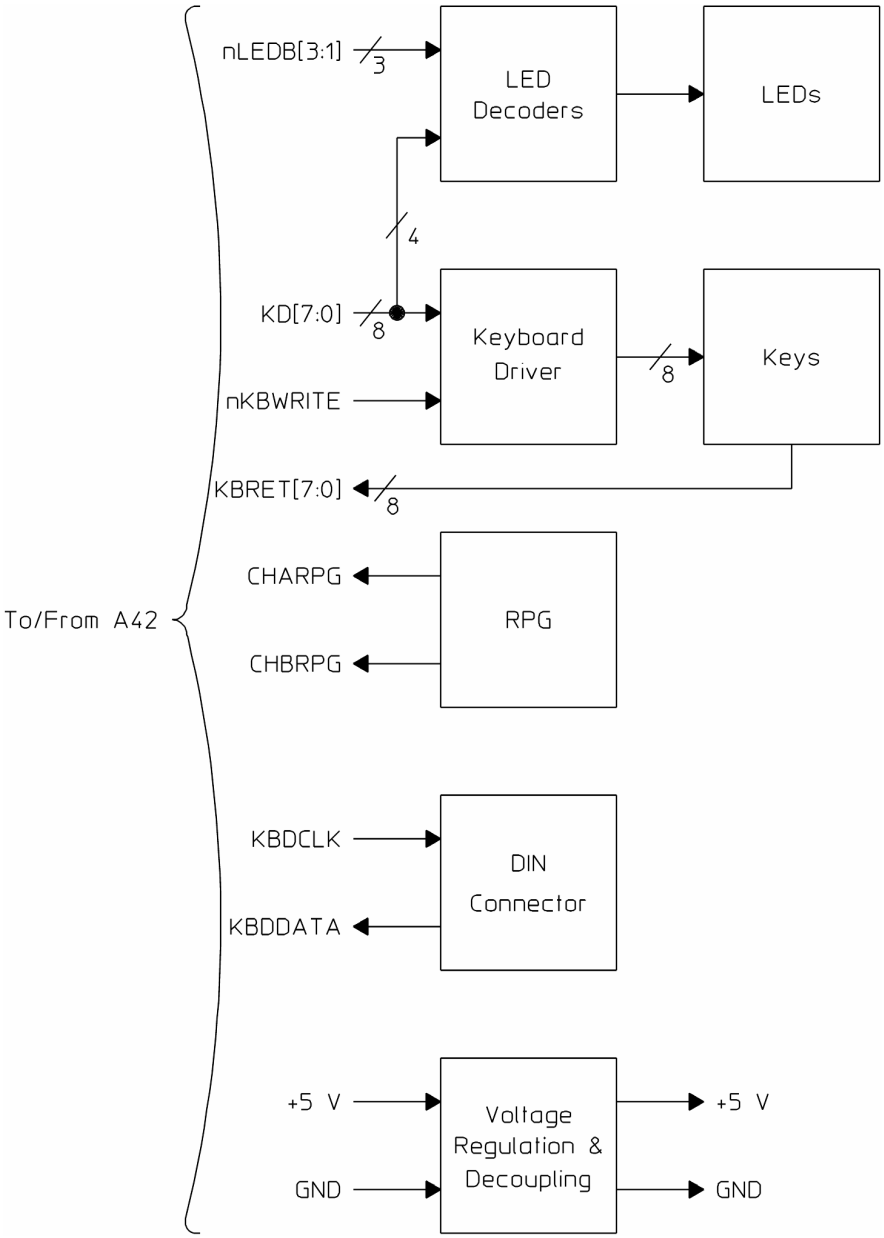
Overall Block Diagram, continued



A45 DSP/ Display Controller Block Diagram



A80 Keyboard Block Diagram

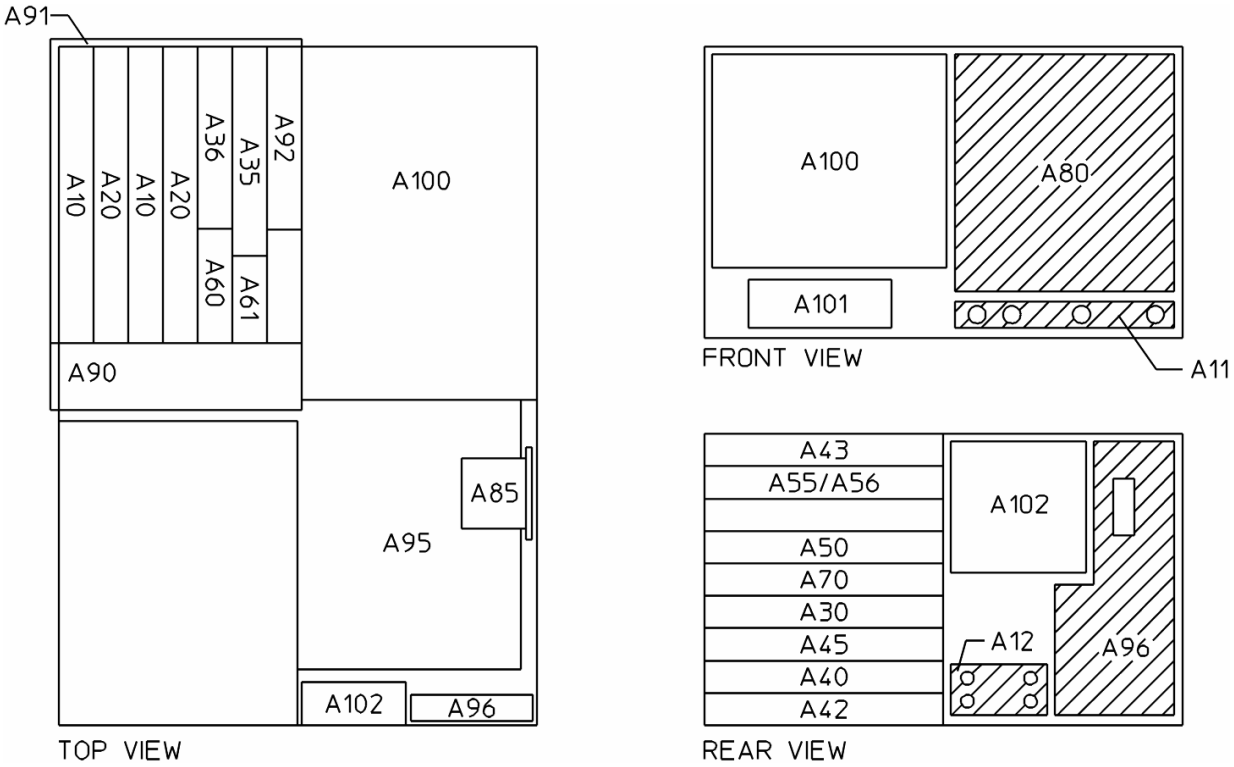


Assembly Locations and Connections

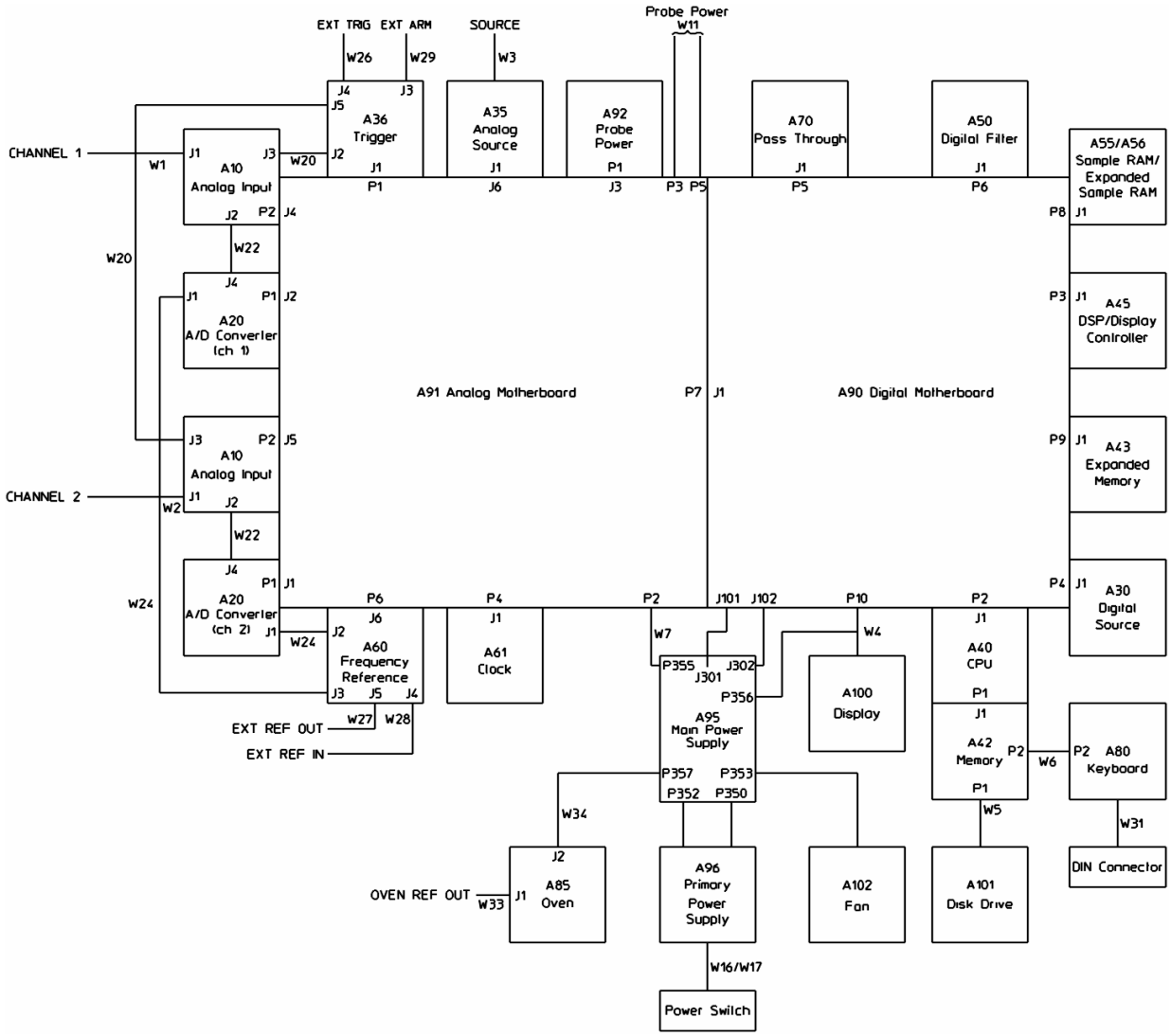
The following figures show the assembly locations and assembly connections.

A10 Analog Input (2 for option AY7)
A11 Front Panel Connector
A12 Rear Panel Connector
A21 A/ D Converter (2 for option AY7)
A30 Digital Source
A35 Analog Source
A36 Trigger
A40 CPU
A42 Memory
A43 Expanded Memory (option UFG)
A45 DSP/ Display Controller
A50 Digital Filter
A55 Sample RAM
A56 Expanded Sample RAM (option AY9)
A60 Frequency Reference
A61 Clock
A71 Pass Through
A80 Keyboard
A85 Oven (option AY5)
A90 Digital Motherboard
A91 Analog Motherboard
A92 Probe Power
A95 Main Power Supply
A96 Primary Power Supply
A100 Display
A101 Disk Drive
A102 Fan

Assembly Locations



Assembly Connections

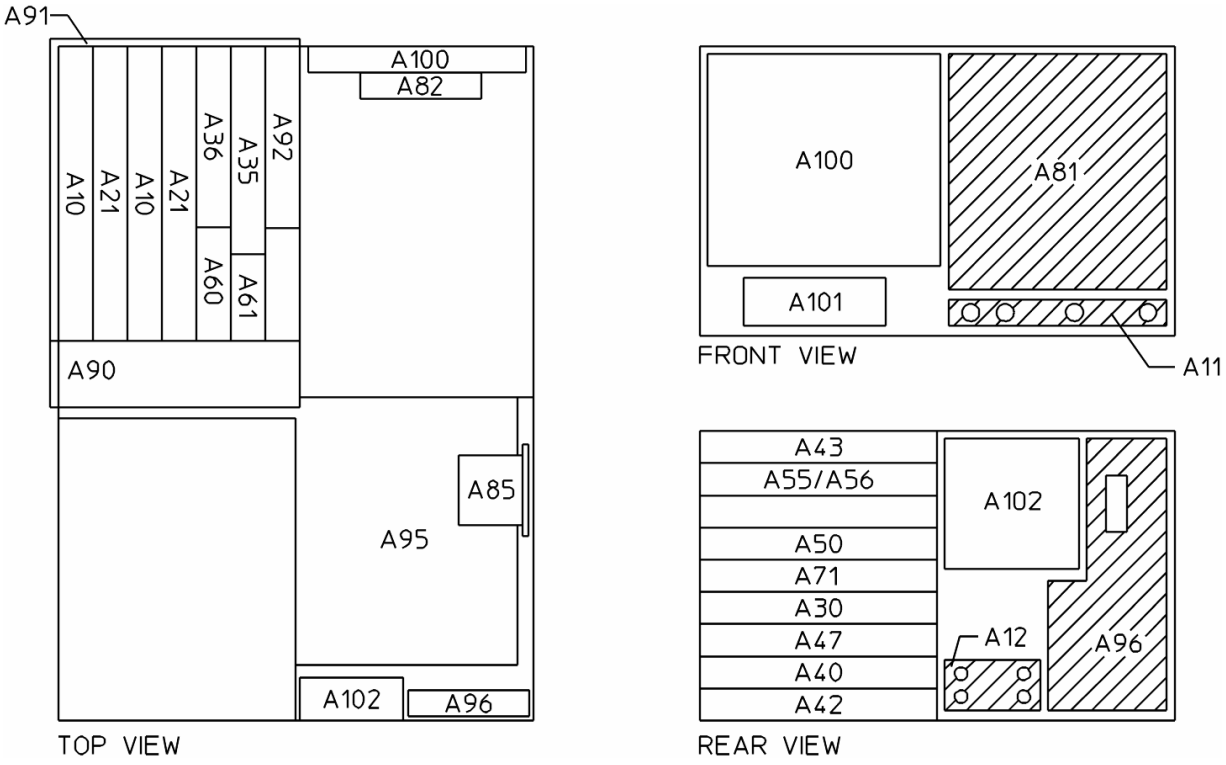


9 Quick Reference

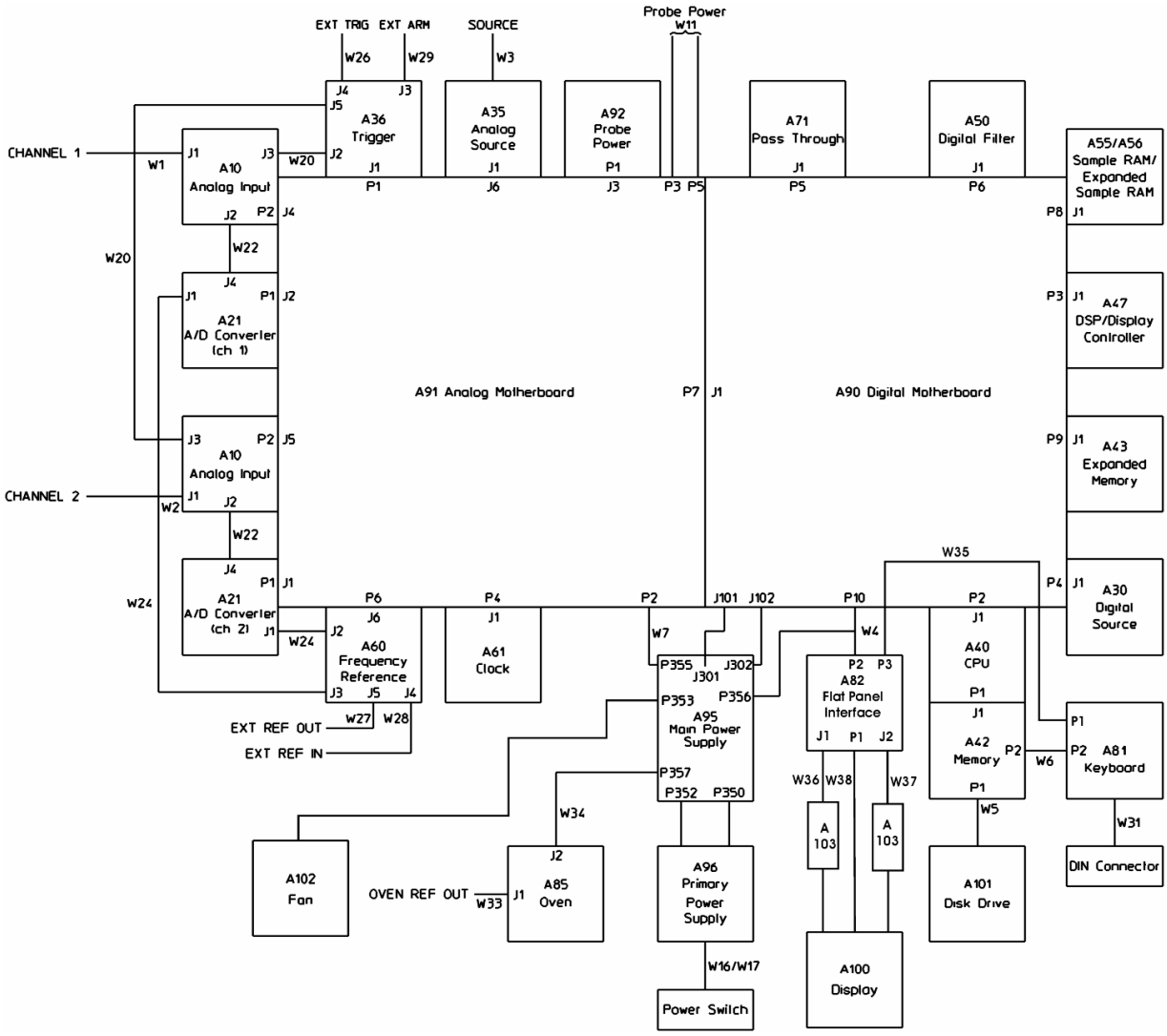
Quick Reference

This chapter contains all the block diagrams and the ''A90/A91 Motherboard Voltages'' table for the Agilent 89410A DC-10 MHz Vector Signal Analyzer. All block diagrams, except the overall block diagrams, show the connector numbers for signals routed through RF cables. The block diagrams do not show connector numbers for signals routed through the analyzer's Motherboard assemblies.

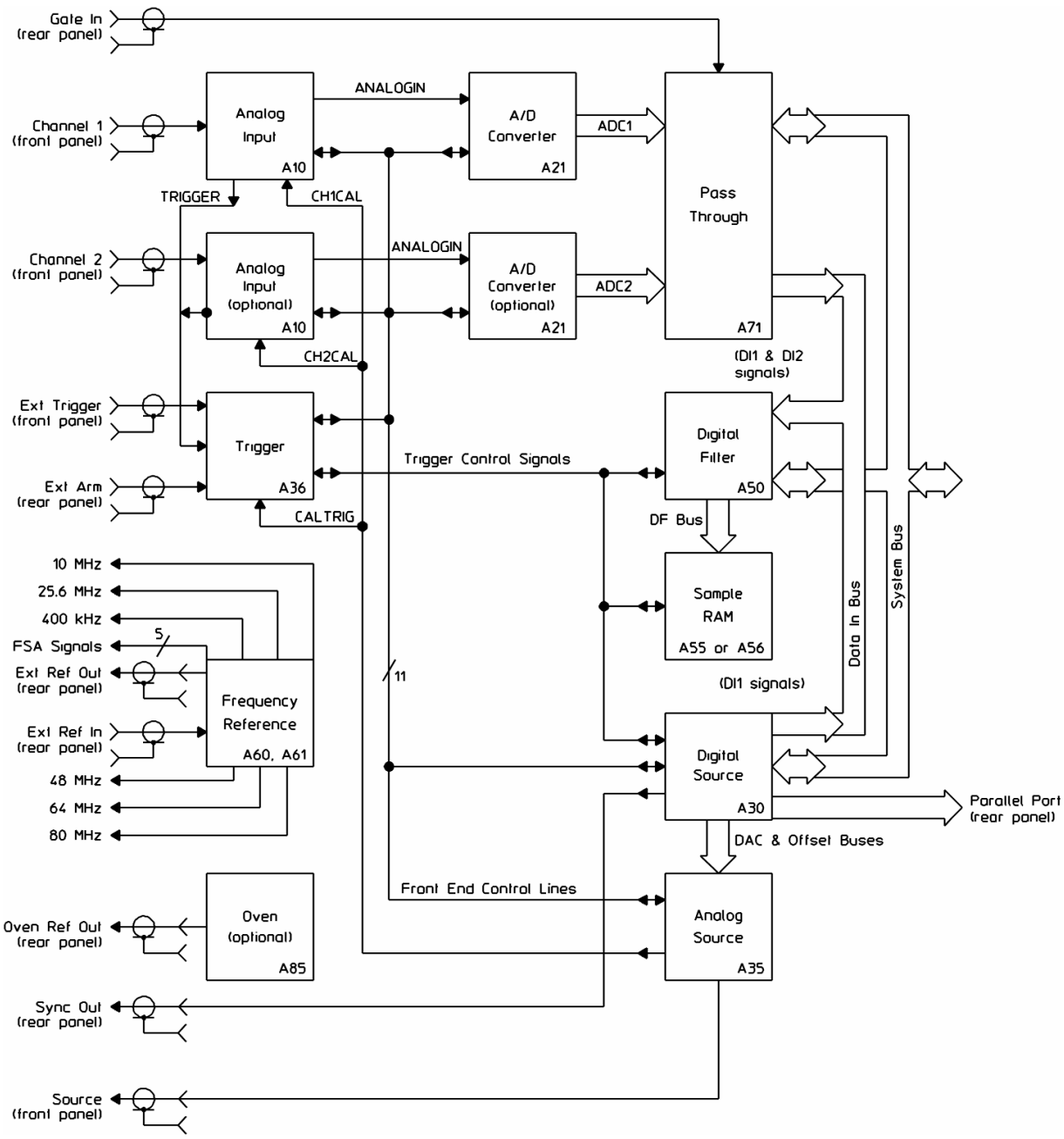
Assembly Locations



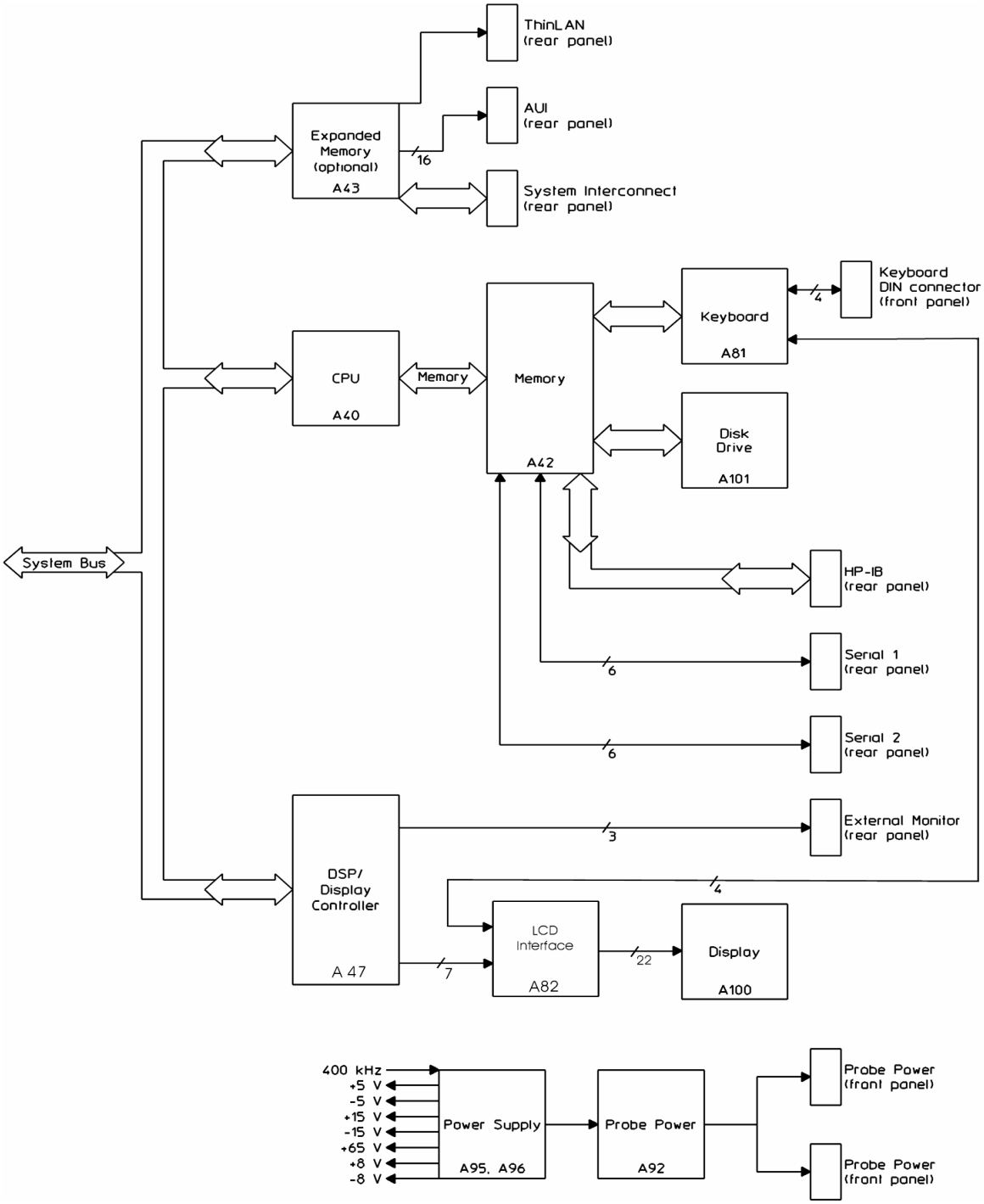
Assembly Connections



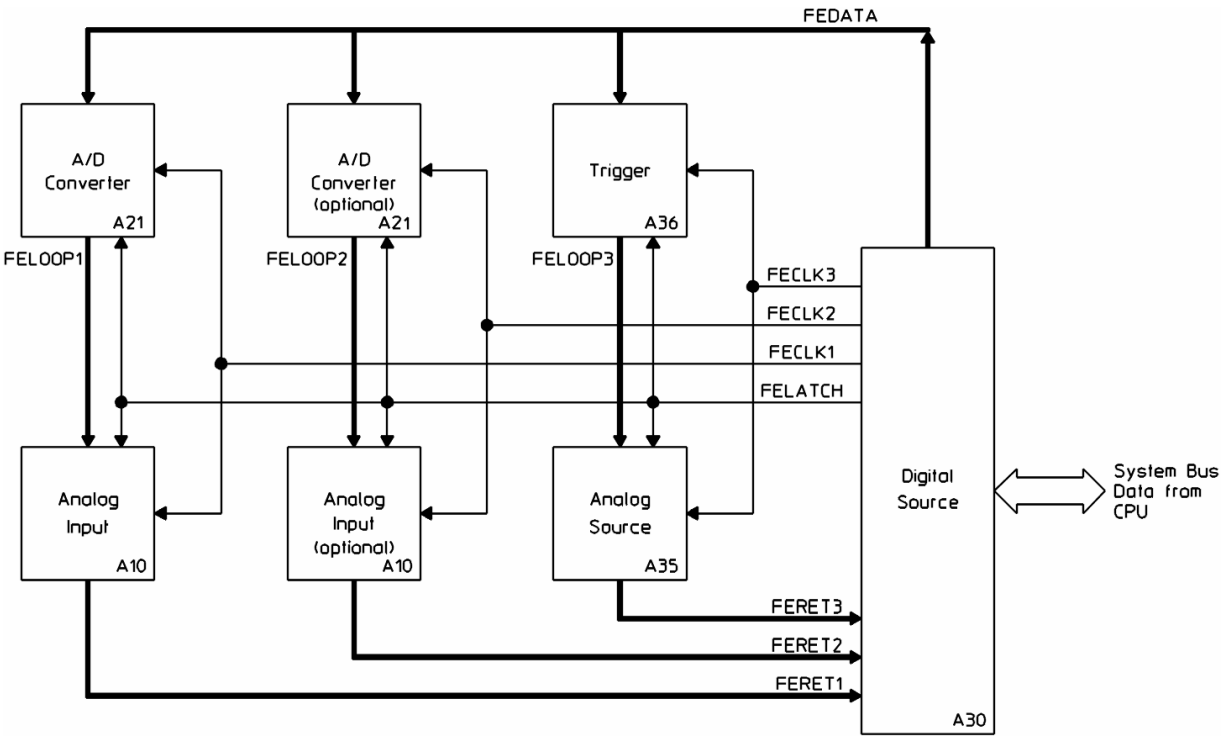
Overall Block Diagram



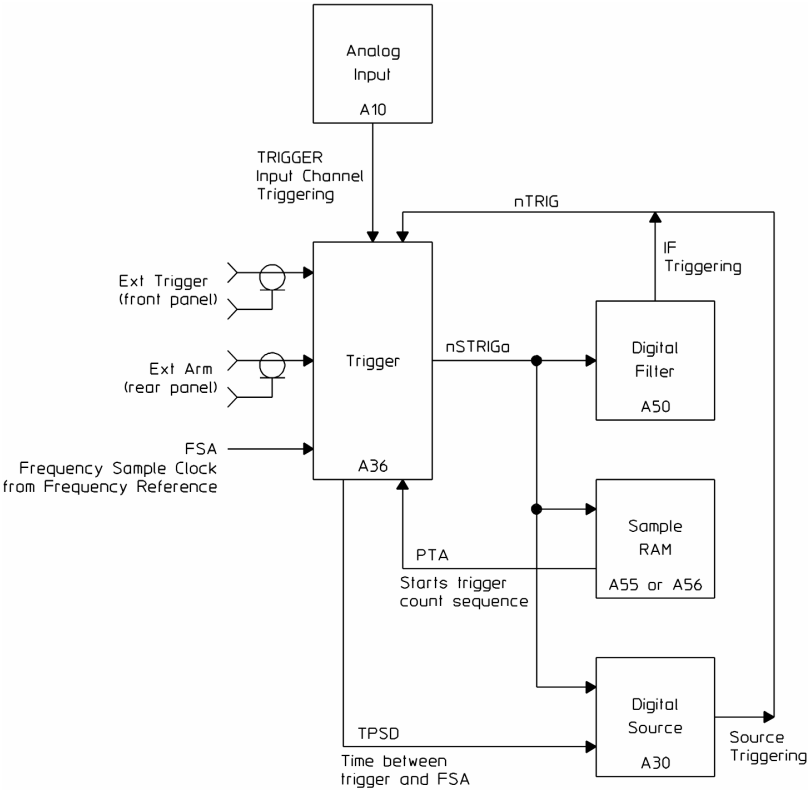
Overall Block Diagram, continued



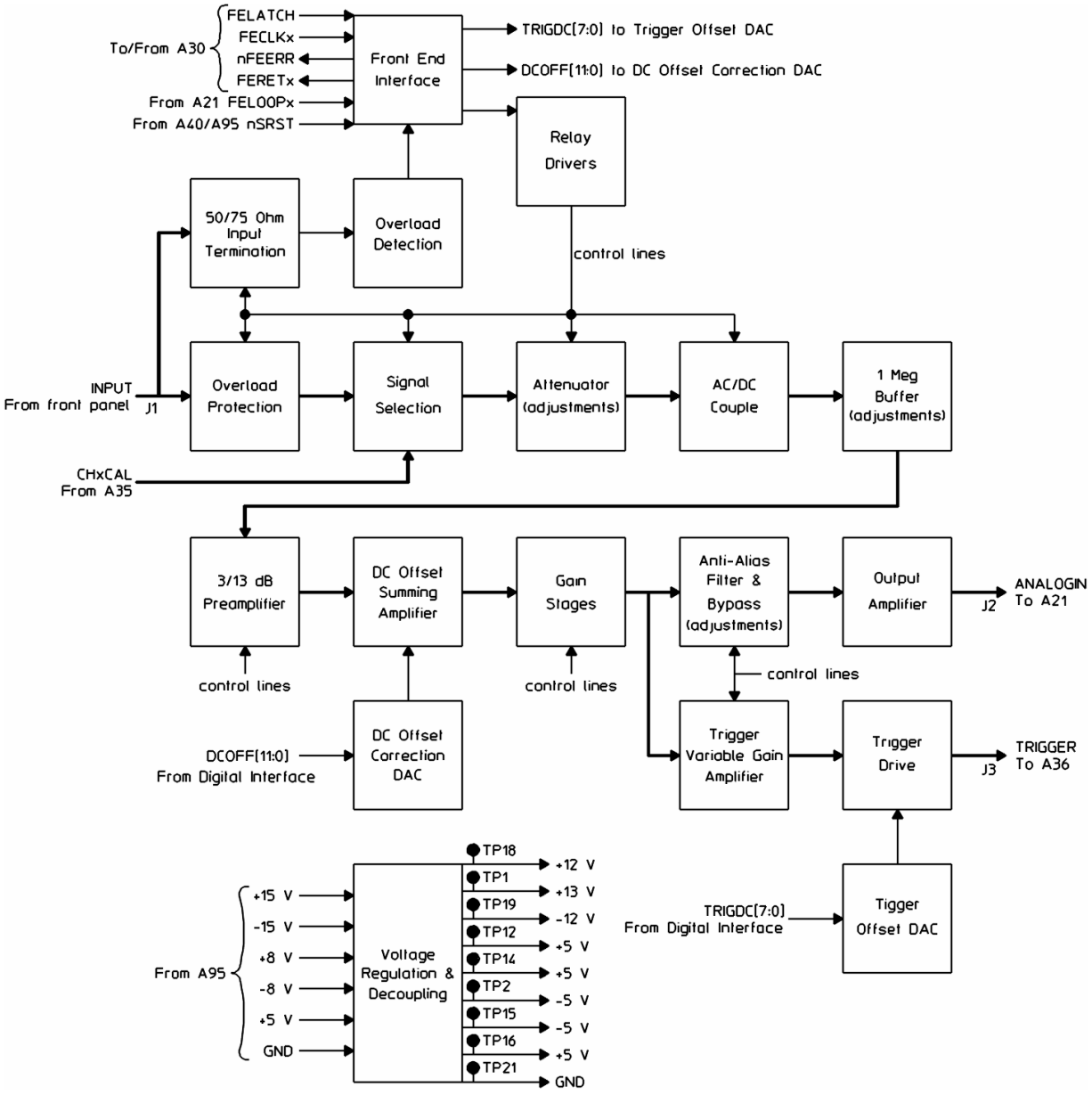
Front End Loops



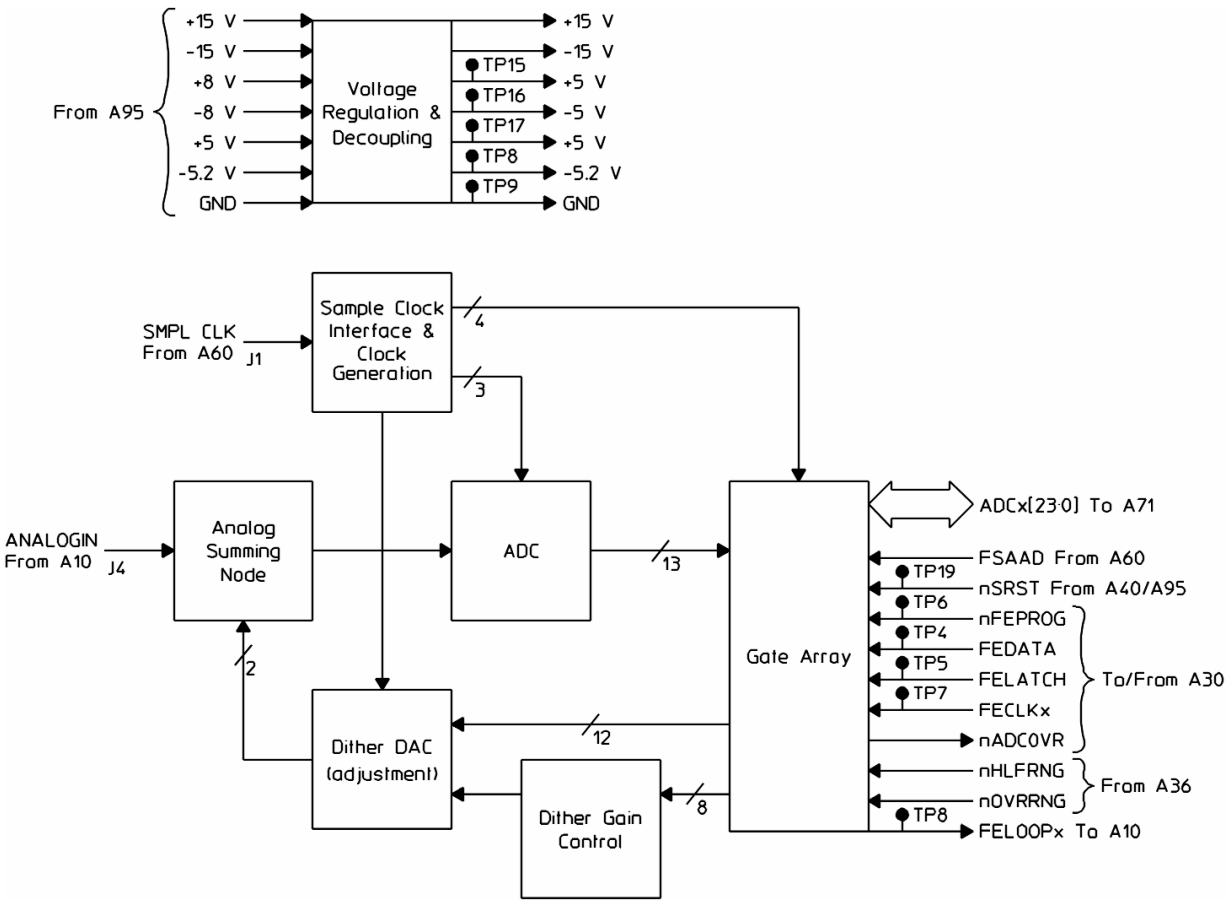
Trigger Signals



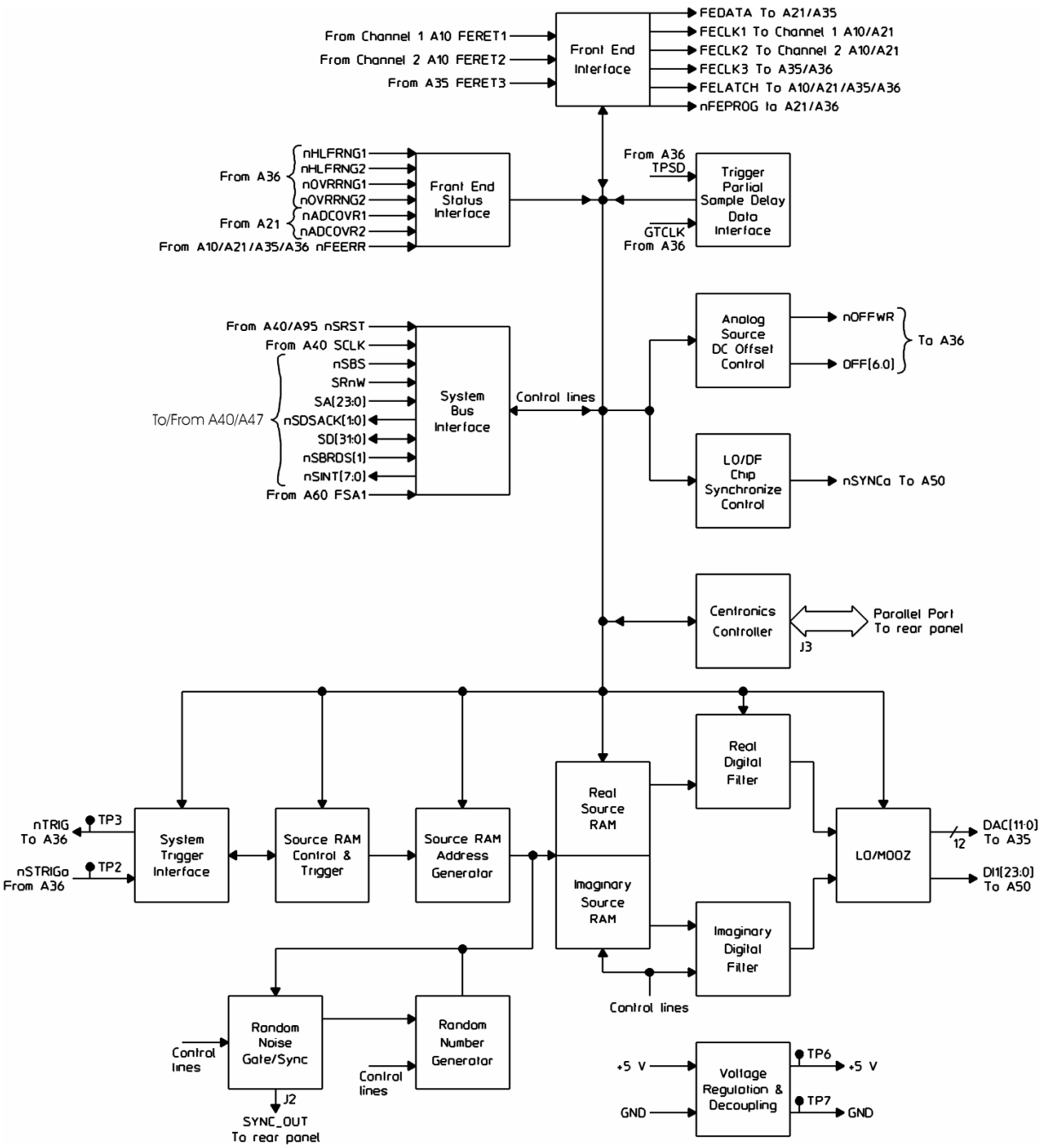
A10 Analog Input Diagram



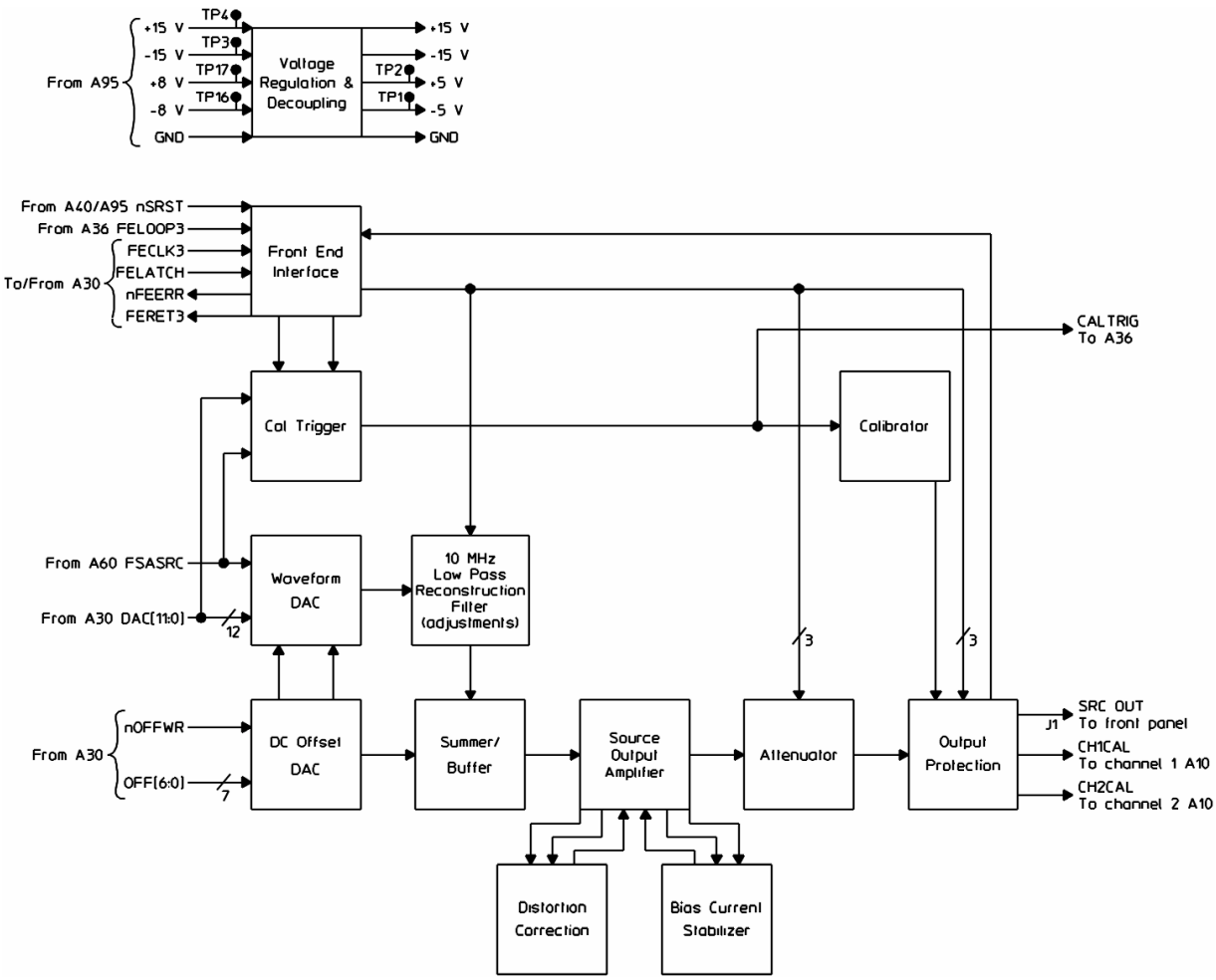
A21 A/ D Converter Block Diagram



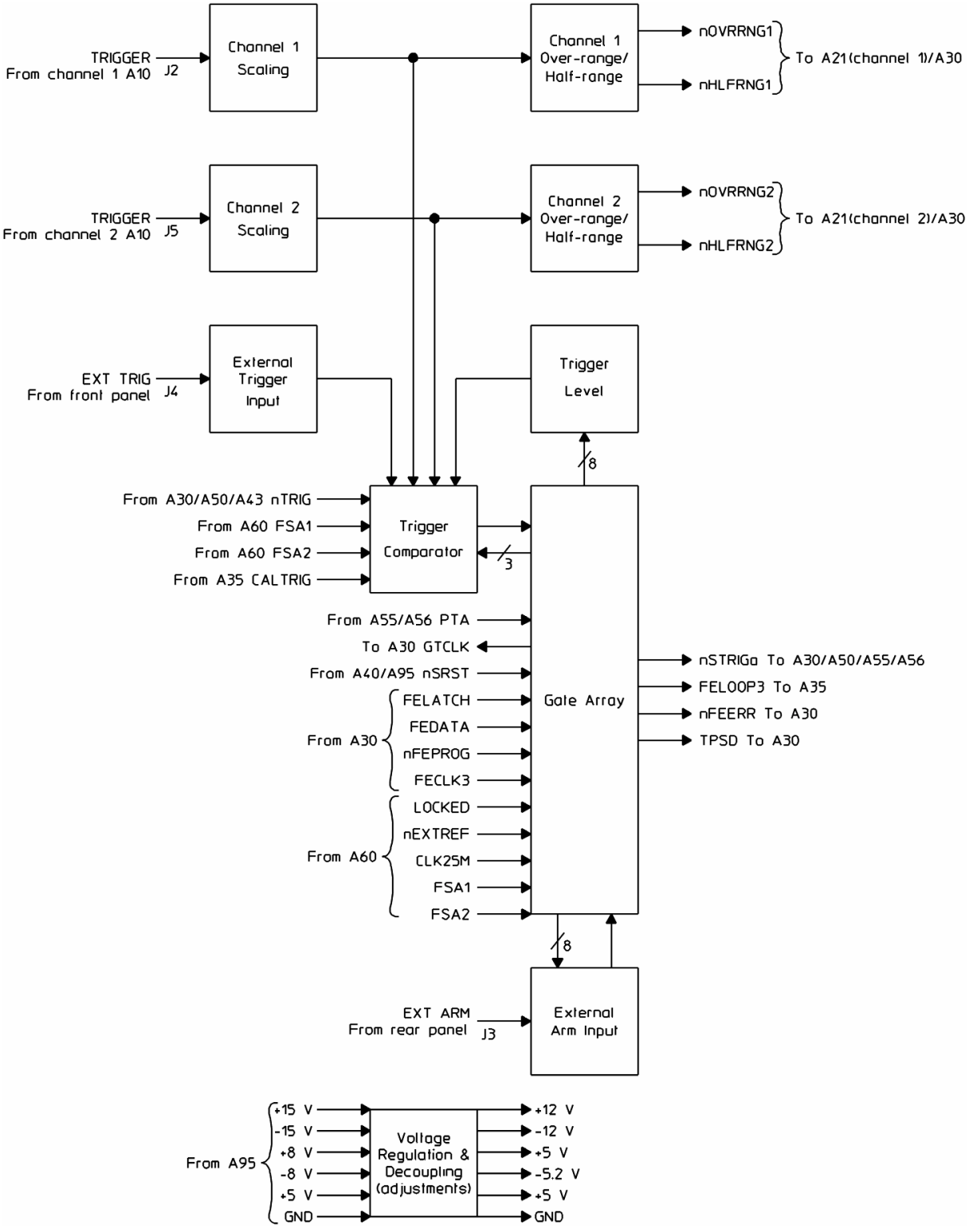
A30 Digital Source Block Diagram



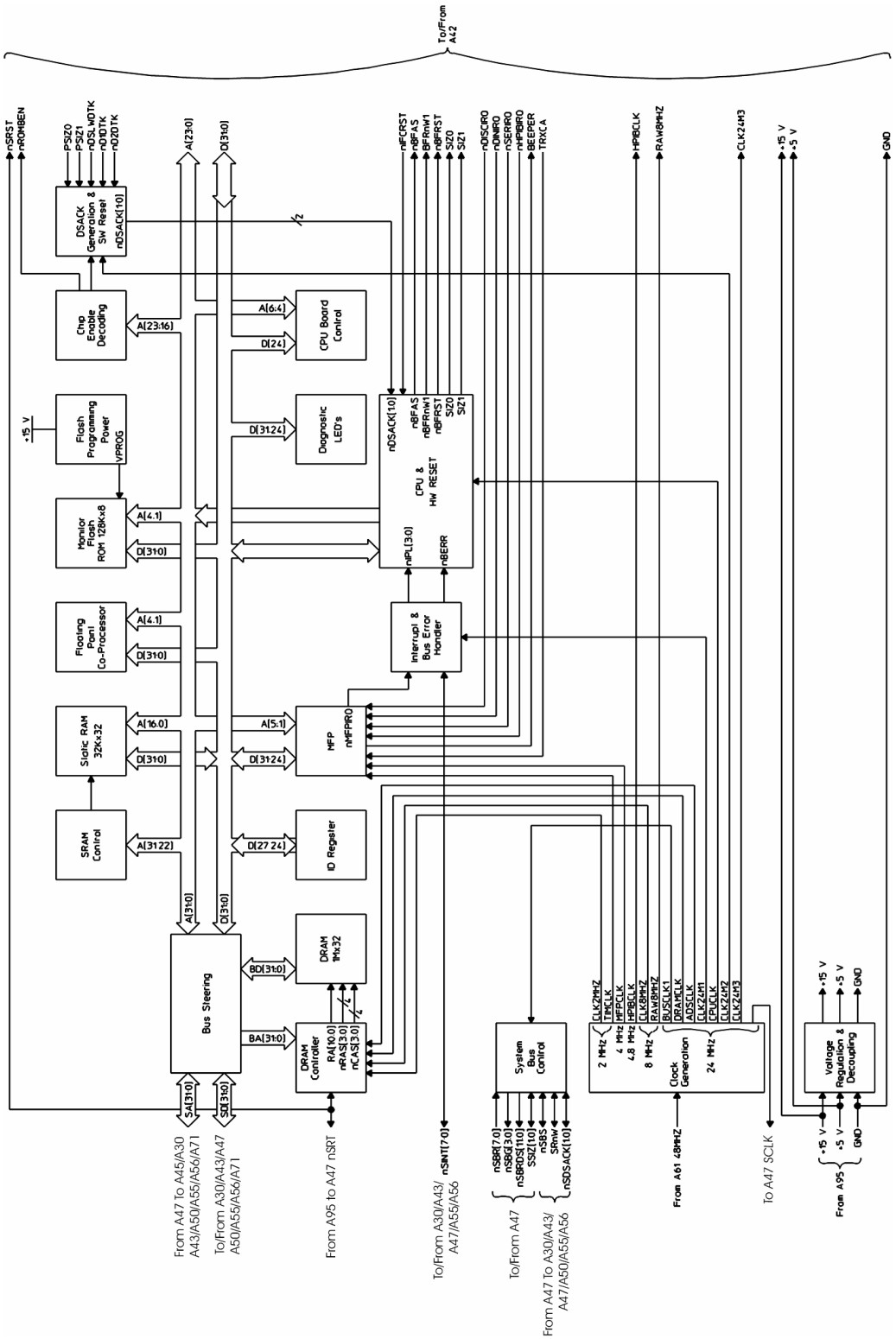
A35 Analog Source Block Diagram



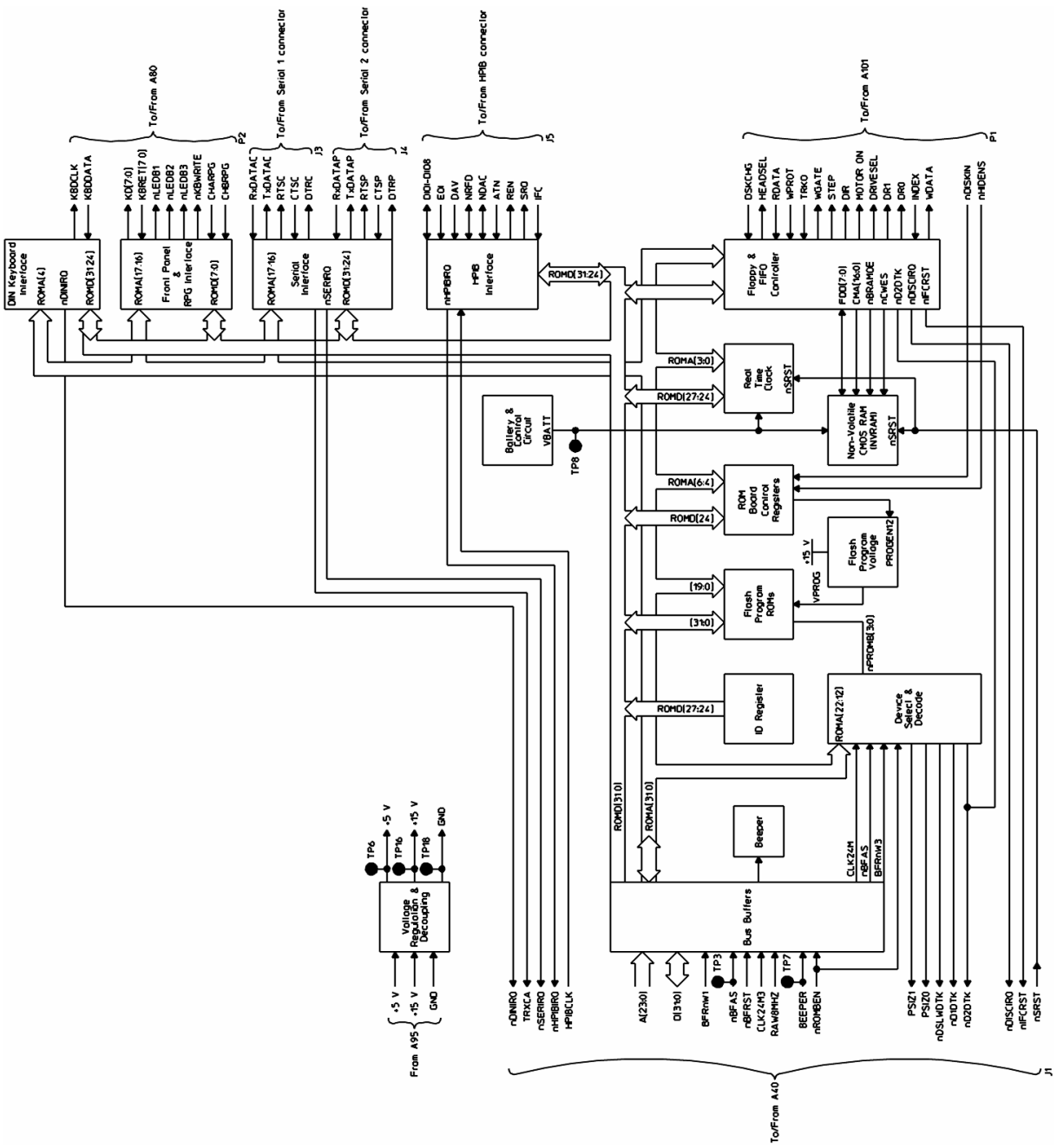
A36 Trigger Block Diagram



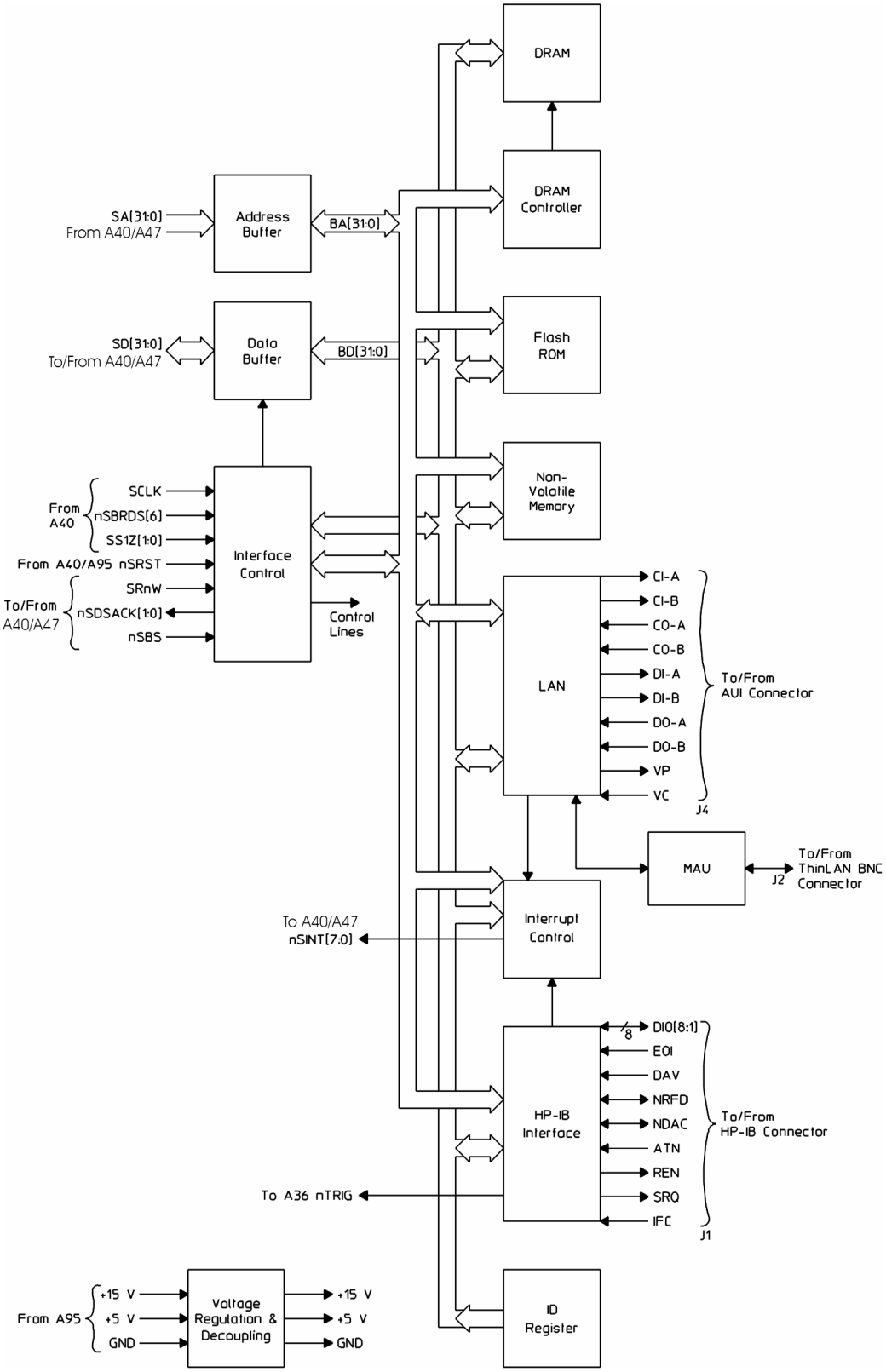
A40 CPU Block Diagram



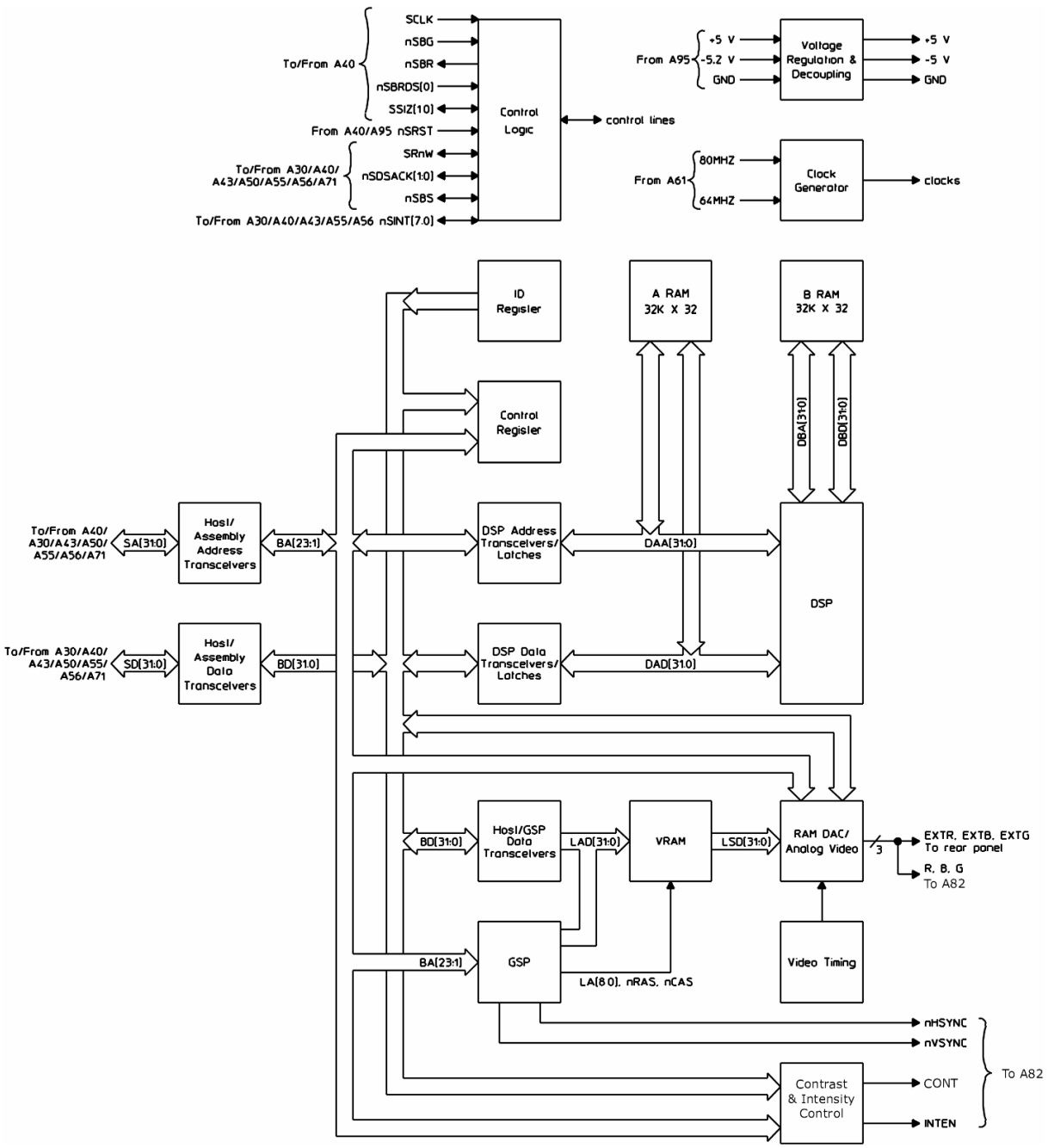
A42 Memory Block Diagram



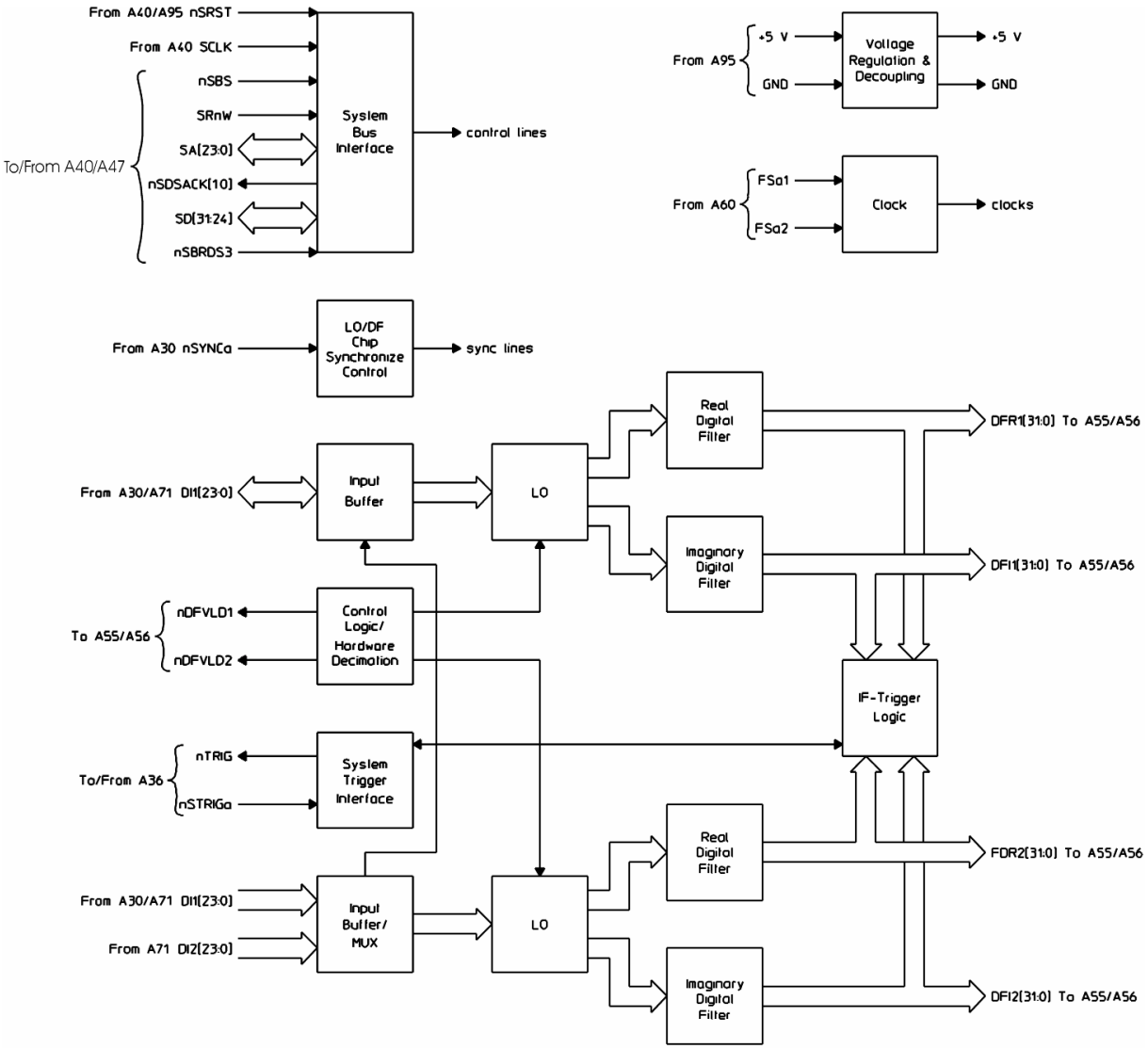
A43 Expanded M emory Bock Diagram



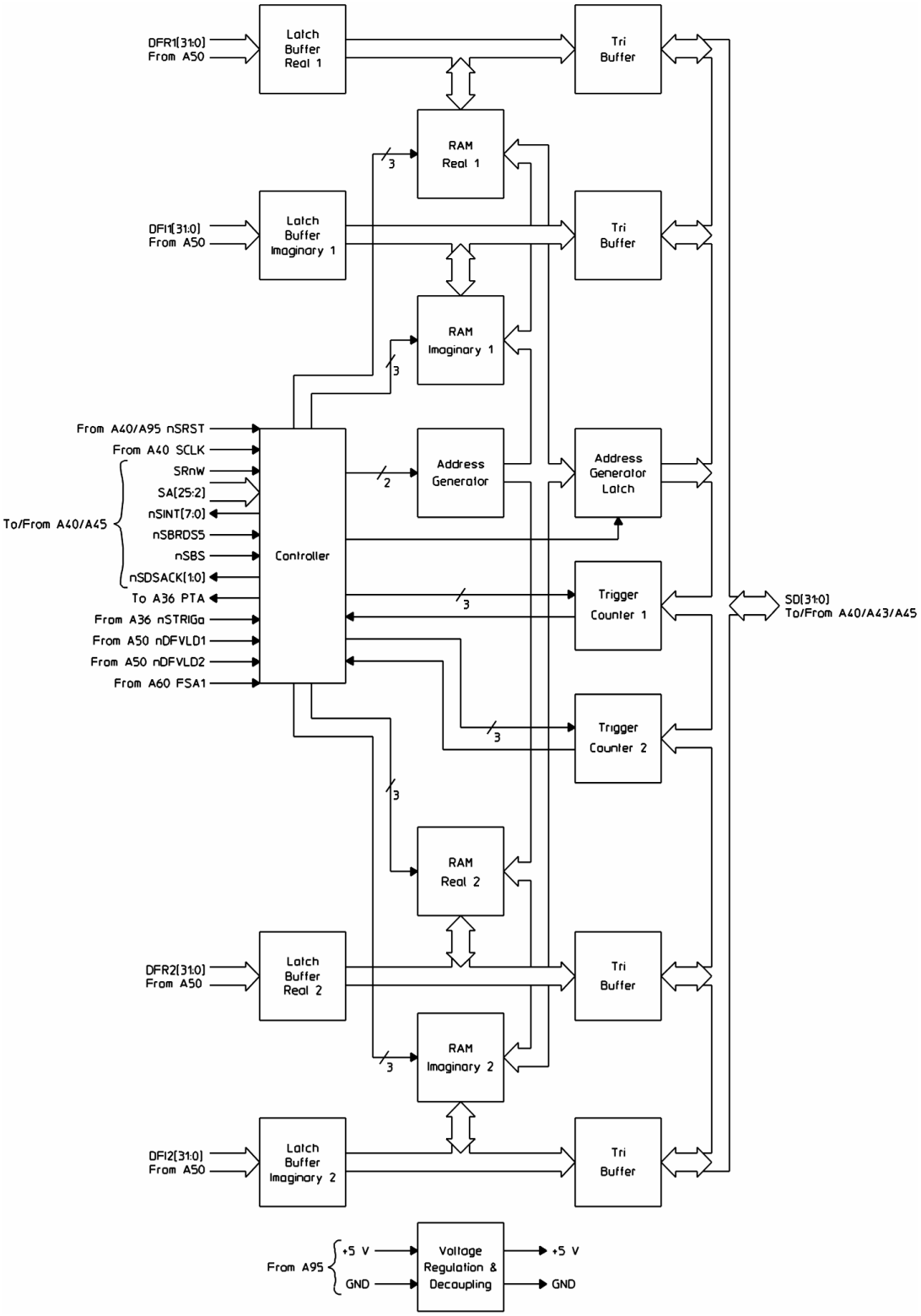
A47 DSP/ Display Controller Block Diagram



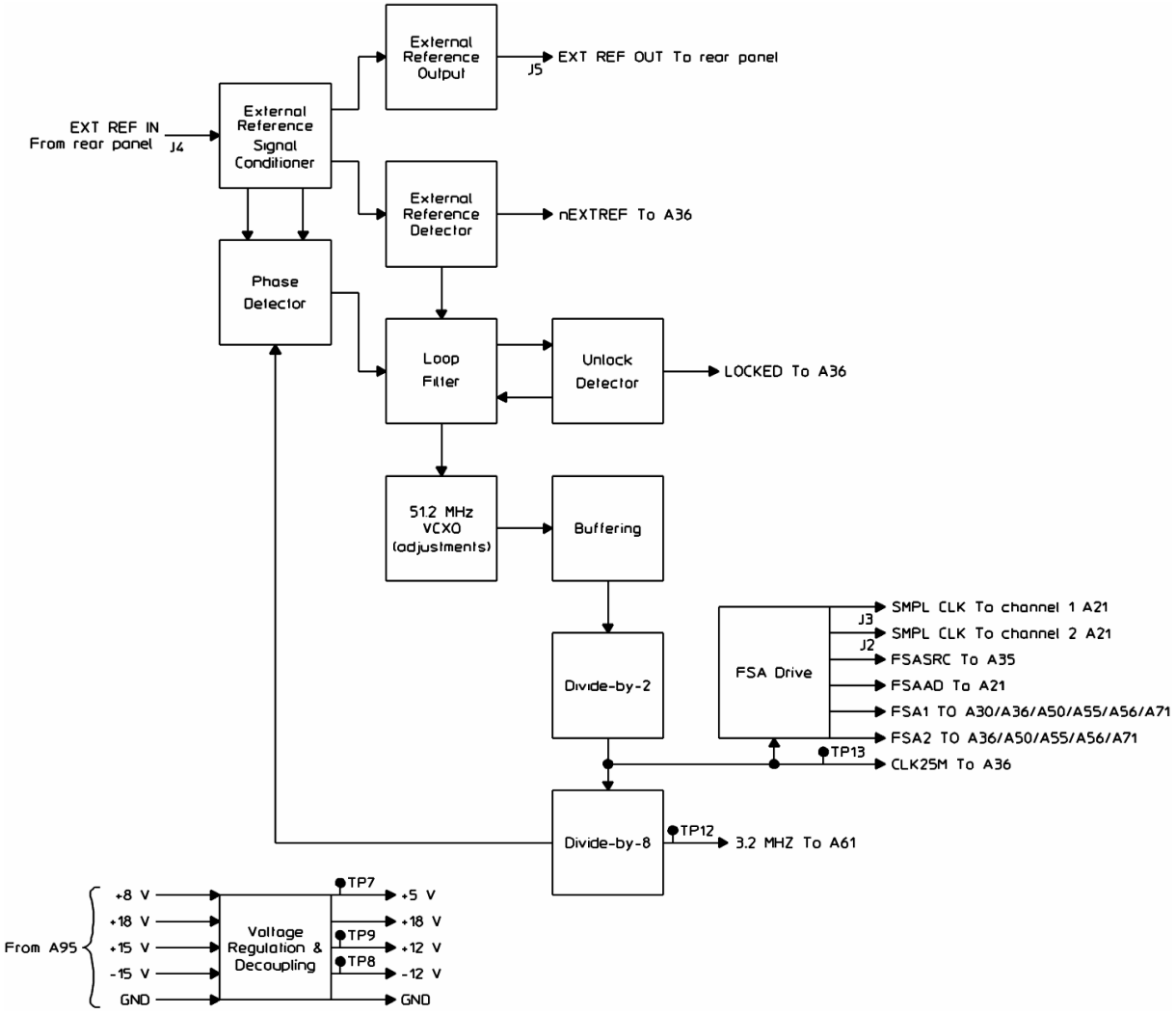
A50 Digital Filter Block Diagram



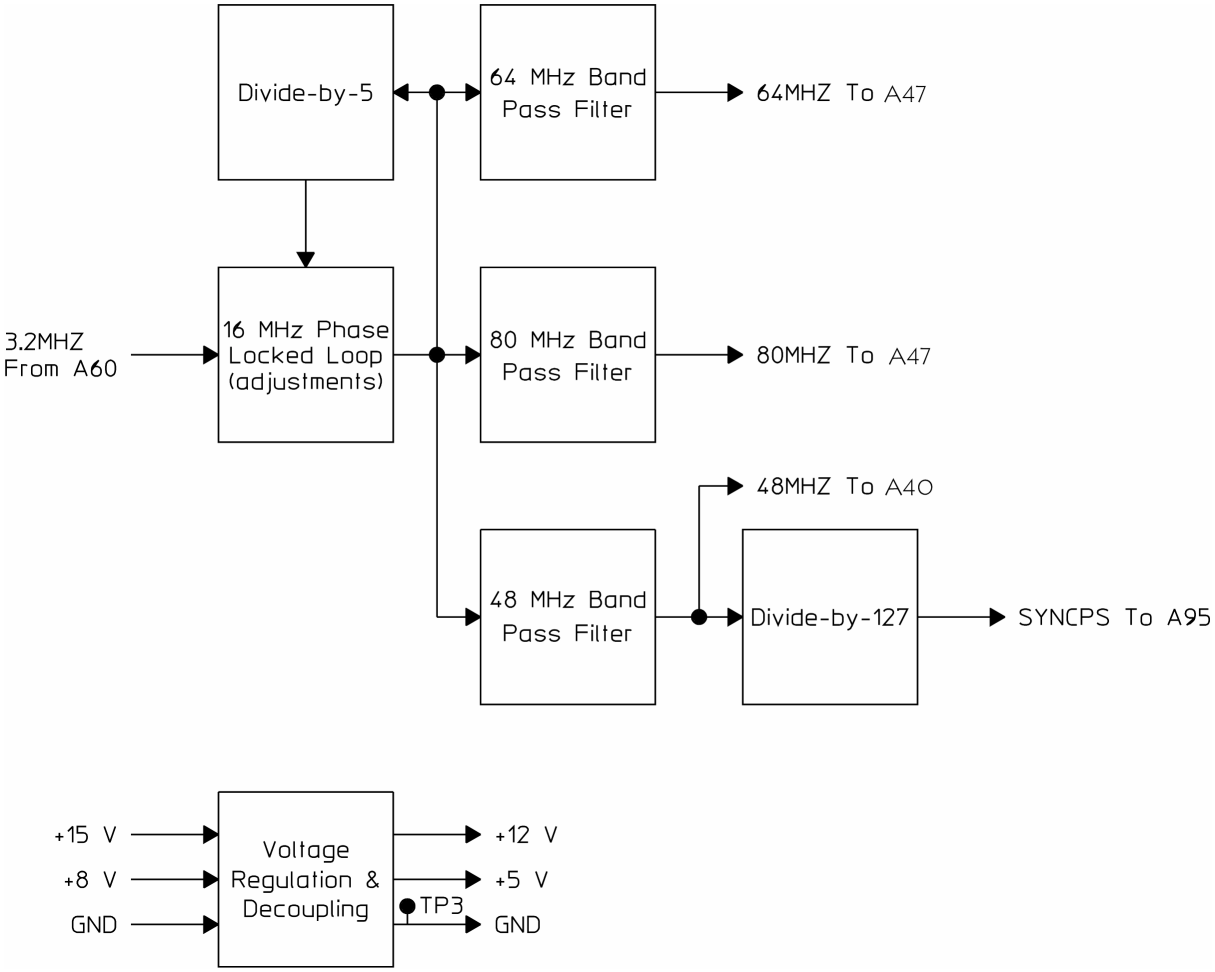
A55 Sample RAM and A56 Expanded Sample RAM



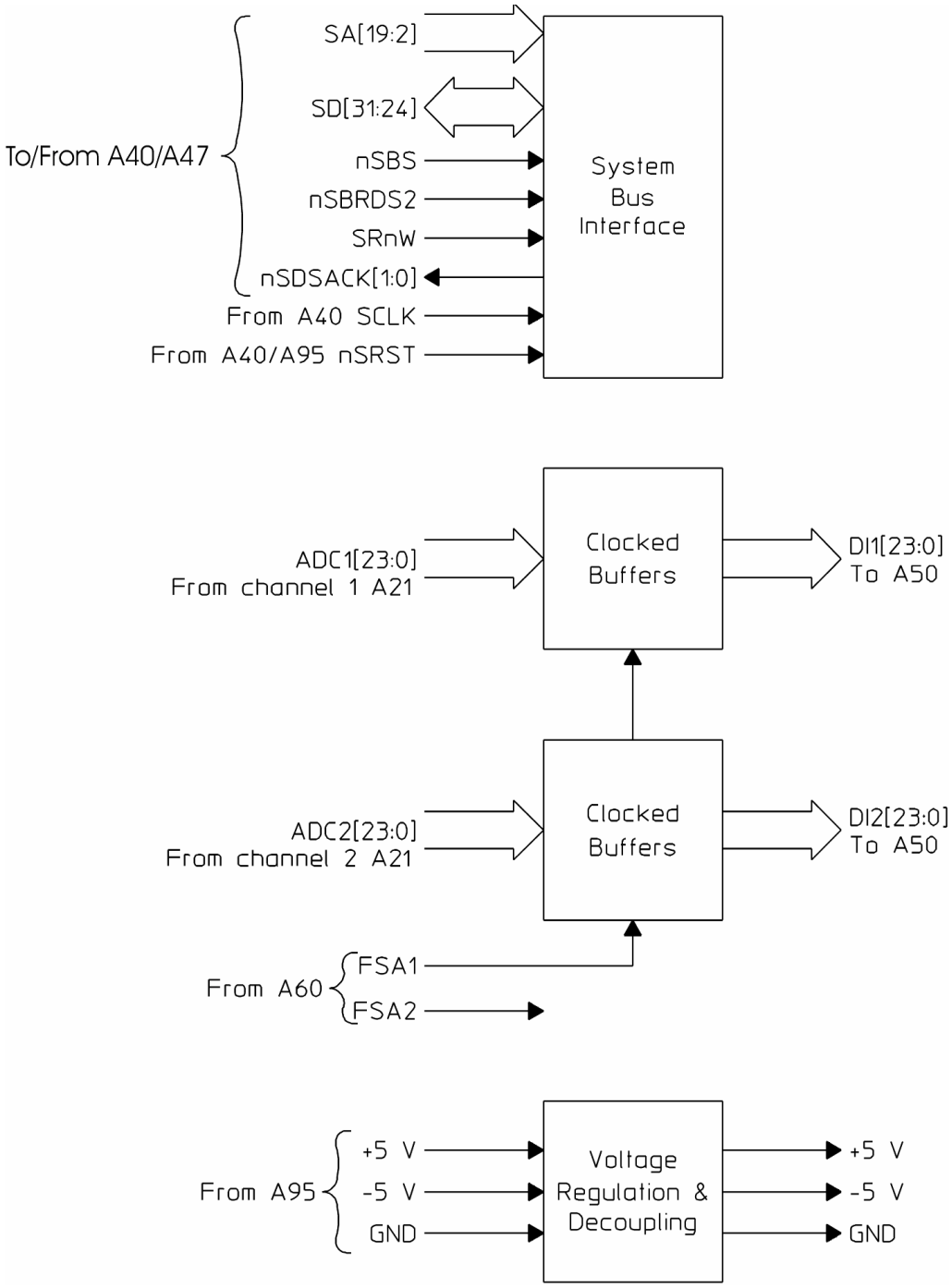
A60 Frequency Reference Block Diagram



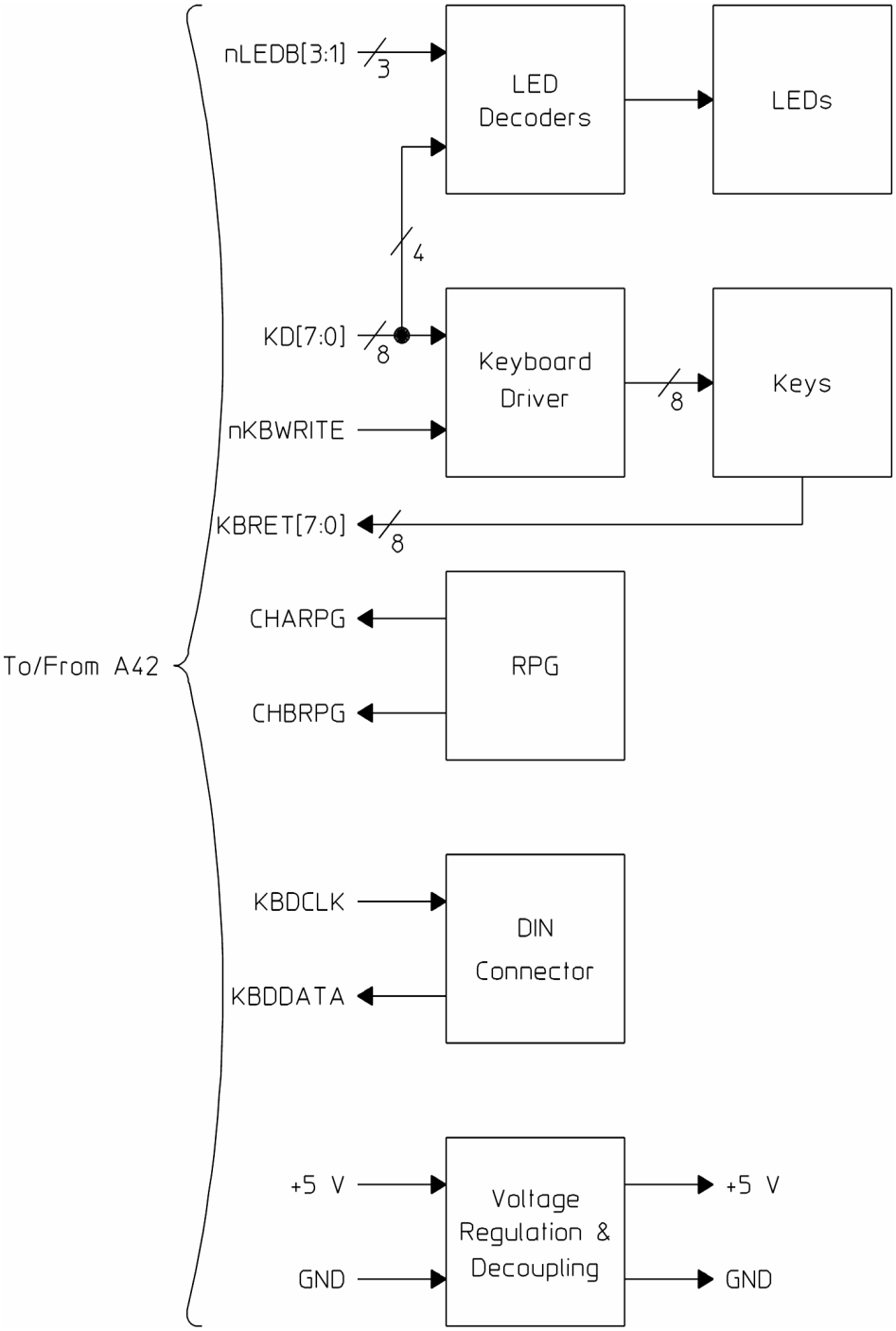
A61 Clock Block Diagram



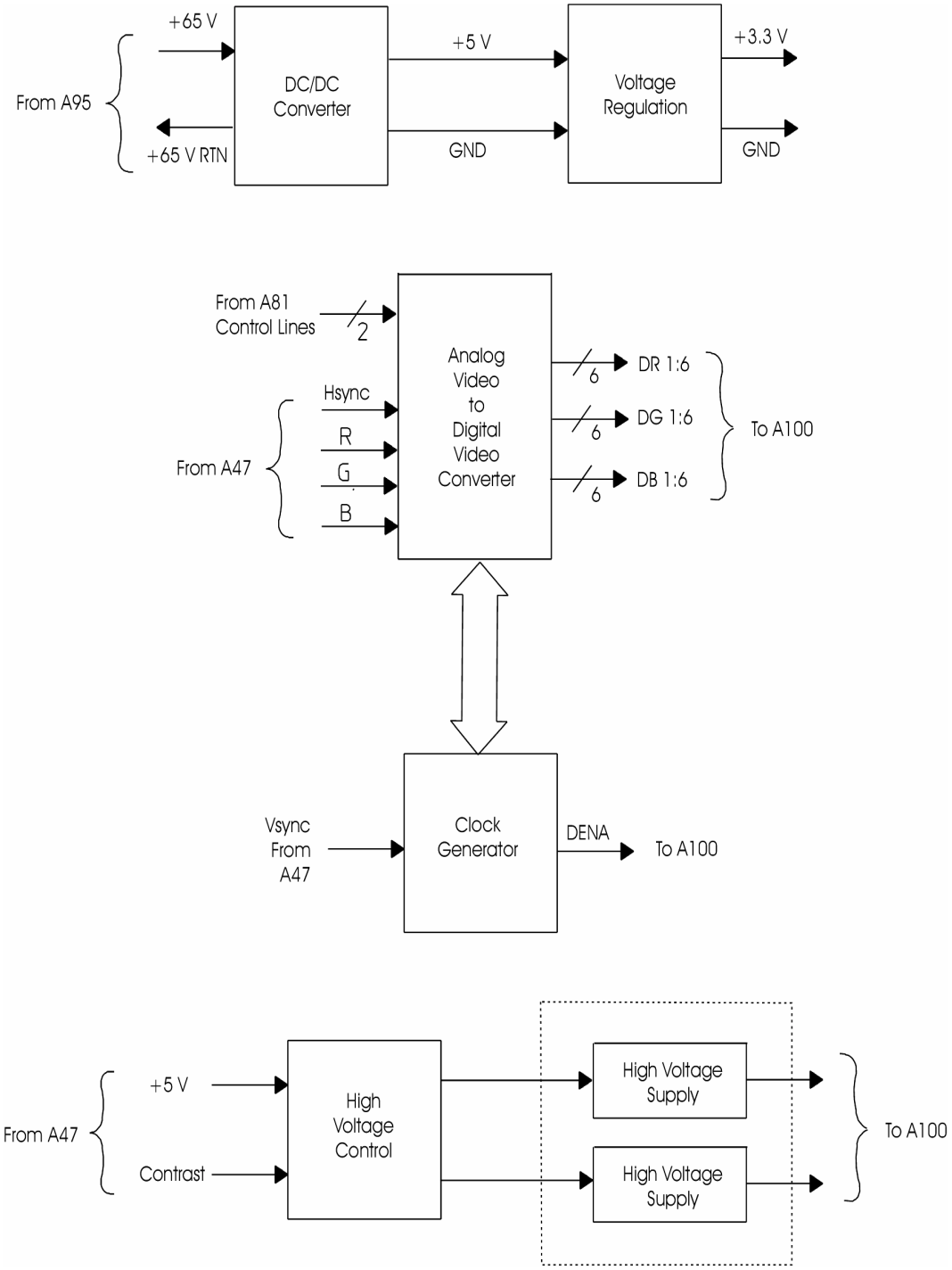
A71A71 Pass Through Block Diagram



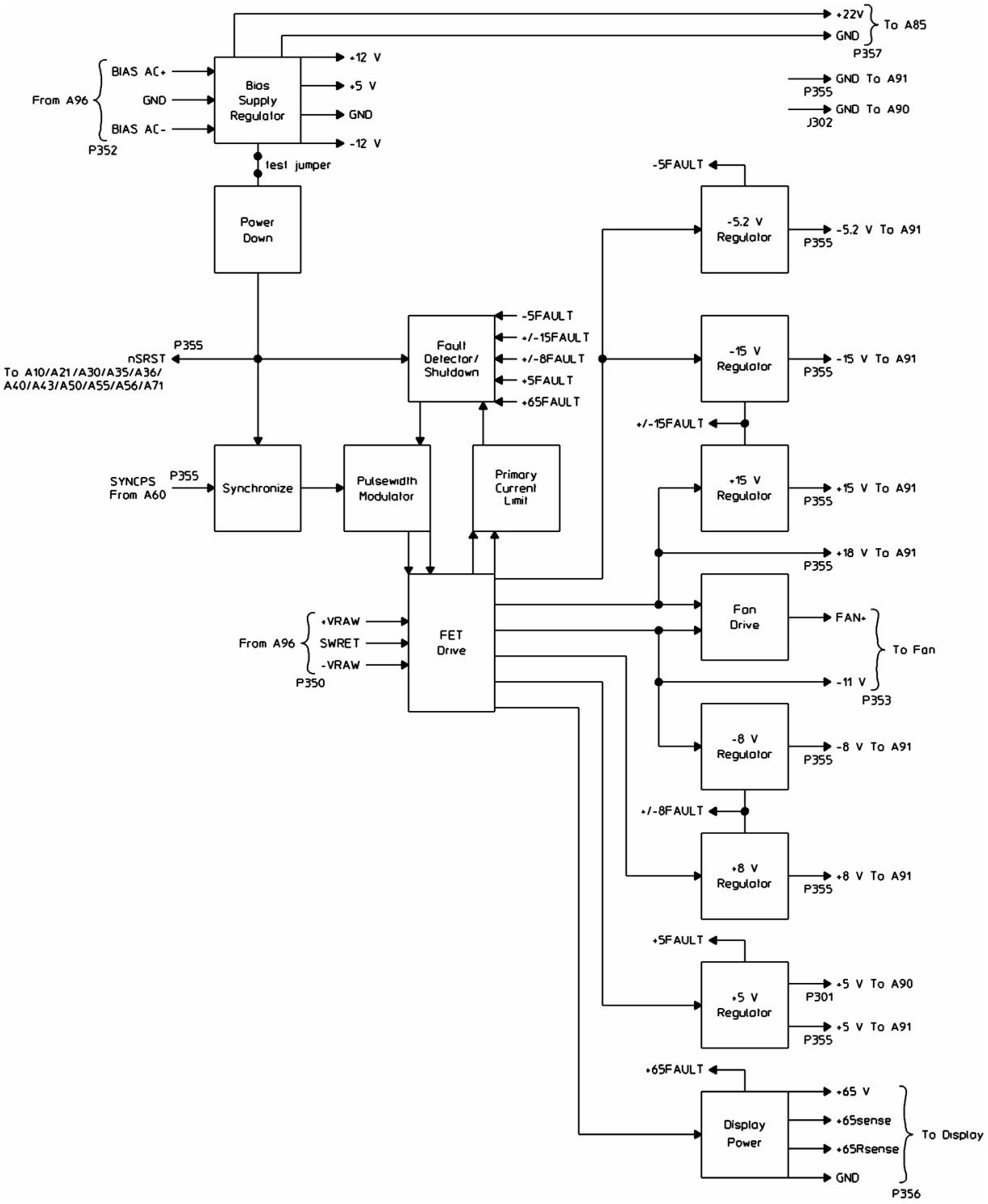
A81 Keyboard Block Diagram



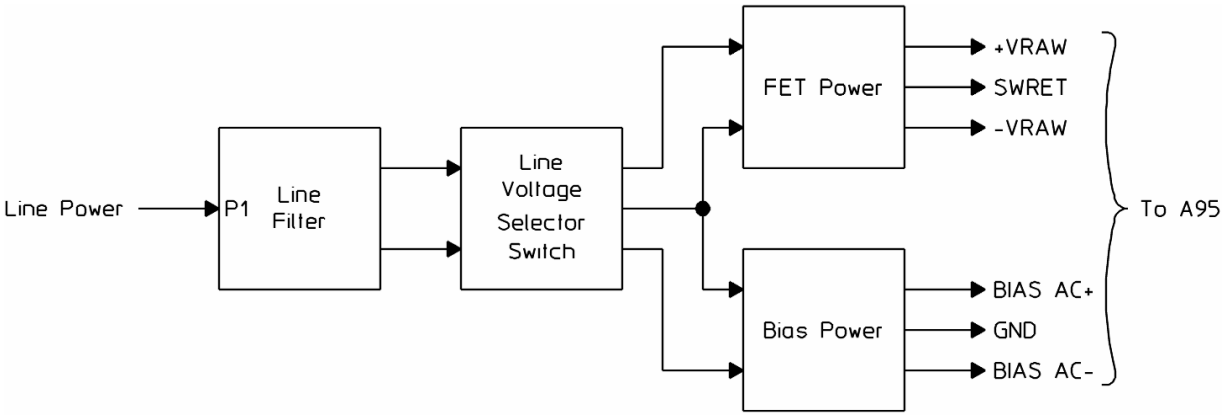
A82 LCD Interface Block Diagram



A95 Main Power Supply Block Diagram



A96 Primary Power Supply Block Diagram



Voltage	Assembly																				
	A10	A10	A21	A21	A35	A36	A60	A61	A92	Probe Power		A95	A90/ A91	A95	A40	A47	A30	A71	A50	A55/ A56	A43	A82
	A91 Analog Motherboard Connector													A90 Digital Motherboard Connector								
	J4	J5	J2	J1	J6	P1	P6	P4	J3	P3	P5	P2	P7/ J1	J101/ J102	J2	J3	J4	J5	J6	J8	J9	J10
	Connector Pin Number																					
+5 V	13A-C	13A-C	8A-C	8A-C		7-8		1-2				3-4		J101	52-53 98-99	52-53 98-99	98-99 102 103	98-99 102 103	98-99 150 151 202 203	98-99 150 151 202 203	52-53 98-99	
-5.2 V			9A-C	9A-C		5-6						1 2	5-6 55 104 105 106		54 57 94 97	54 57 94 97	94 97 104 107	94 97 104 107	97 101 200 204	97 101 200 204	54 57 94 97	
+8 V	5A-C	5A-C	2A-C	2A-C	16A-C	12	45-46 48	15 16				15										
-8 V	7A-C	7A-C	3A-C	3A-C	17A-C	11	41-44	11-12				13										
-12.6 V									1A-C 3A-C	3	3											
+15 V									5A-C 7A-C	1	1											
+15 V	9A-C	9A-C	5A-C	5A-C	22A-C	1	35-37	7-8	15A-C			11	2, 53 102 103		55 96	55 96	96 105	96 105	96 205	96 205	55 96	
-15 V	11A-C	11A-C	6A-C	6A-C	23A-C	2	32-34	3 4	13A-C			9	2 4		56 95	56 95	95 106	95 106	95 206	95 206	56 95	
+18 V							49		11A-C			8										
GND	4A-C 6A-C 8A-C 10A-C 12A-C 14A-C 16A-C 20A-C 21A-C 22A-C 23A-C 24A-C 25A 25C 26A-C 27A-C 28A-C 29A-C	4A-C 6A-C 8A-C 10A-C 12A-C 14A-C 16A-C 20A-C 21A-C 22A-C 23A-C 24A-C 25A 25C 26A-C 27A-C 28A-C 29A-C	1A, C 4A, C 7A-C 10A-C 12A, C 13B 14A, C 15B 16A, C 17B 18A, C 19B 20A, C 21B 22A, C 23B 24A, C 25B 26A, C 27B 28A, C 29B 32C	1A, C 4A, C 7A-C 10A-C 12A, C 13B 14A, C 15B 16A, C 17B 18A, C 19B 20A, C 21B 22A, C 23B 24A, C 25B 26A, C 27B 28A, C 29B 32C	1A, C 2B 3A, C 4B 5A, C 6B 7A, C 8B 9A, C 10B 11A, C 13A 14A, A 15C 19A 20A-B 21A-B 24A-C 25A, C 26A-C 27A, C 28A-C 29A, C 30A, C 32A, C	3-4 9-10 13-14 19 28-29 31 37 46	1-3 6-9 12-15 19-20 28-31 38-40 47	6 9-10 13-14 17-18 20 22-23 26-27 29	2A-C 4A-C 6A-C 8A-C 10A-C 12A-C 14A-C 16A-C	2	2	10 12 14	1, 14 19 50-52 54 56-57 59, 61 63, 65 67, 69 71, 73 75-76 78, 80 82, 84 86, 88 90, 92 94, 96 98 100 101 114 119 150	J102	51 59 61 63 65 67 69 71 73 75 76 78 80 82 84 86 88 90 92 100	43 45 51 59 61 63 65 67 69 71 73 75 76 78 80 82 84 86 88 90 92 100 143 145	51, 54 57, 60 63, 66 69, 72 75-76 79, 82 85, 88 91 100 101 110 113 116 119 122 125 126 129 132 135 138 141 144 147 150	51, 54 57, 60 63, 66 69, 72 75-76 79, 82 85, 88 91 100 101 110 113 116 119 122 125 126 129 132 135 138 141 144 147 150	51, 54 57, 60 63, 66 69, 72 75-76 79, 82 85, 88 91, 94 100 201 207 210 213 216 219 222 225 226 229 232 235 238 241 244 247 250	51, 54 57, 60 63, 66 69, 72 75-76 79, 82 85, 88 91, 94 100 201 207 210 213 216 219 222 225 226 229 232 235 238 241 244 247 250	51 59 61 63 65 67 69 71 73 75 76 78 80 82 84 86 88 90 92 100	9 11 13 14 16 18 20

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