Service Guide

Agilent Technologies

- **81101A one Channel 50 MHz Pulse Generator**

Agilent Technologies

Part No. 81101-91060
Edition E0901

Contents

NOTICE

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Safety Information

The following general safety precautions must be observed during all phases of operation of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Agilent Technologies Inc. assumes no liability for the customer's failure to comply with these requirements.

General

This product is a Safety Class 1 instrument (provided with a protective earth terminal). The protective features of this product may be impaired if it is used in a manner not specified in the operation instructions.

Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

All Light Emitting Diodes (LEDs) used in this product are Class 1 LEDs as per IEC 60825-1.

Environmental Conditions

This instrument is intended for indoor use in an installation category II, pollution degree 2 environment. It is designed to operate at a maximum relative humidity of 95% and at altitudes of up to 2000 meters. Refer to the specifications tables for the ac mains voltage requirements and ambient operating temperature range.

Before Applying Power

Verify that the product is set to match the available line voltage, the correct fuse is installed, and all safety precautions are taken. Note the instrument's external markings described under in Safety Symbolsl below.

Ground the Instrument

To minimize shock hazard, the instrument chassis and cover must be connected to an electrical protective earth ground. The instrument must be connected to the ac power mains through a grounded power cable, with the ground wire firmly connected to an electrical ground (safety ground) at the power outlet. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury.

Fuses

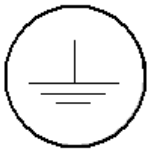
Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuse holders. To do so could cause a shock or fire hazard.
Do Not Operate in an Explosive Atmosphere
Do not operate the instrument in the presence of flammable gases or fumes.

Do Not Remove the Instrument Cover

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made only by qualified service personnel.
Instruments that appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by qualified service personnel.

Safety Symbols

Caution (refer to accompanying documents)



Protected conductor symbol.

In the manuals:

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, or the like, which, if not correctly performed or adhered to could result in damage to or destruction of part or all of the product. not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

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Installation

Please refer to the Quick Start Guide and the Reference Guide
see Manuals

Using the Instrument..

Please refer to the Quick Start Guide and the Reference Guide
see Manuals

Repair Strategy...

Repair by exchange Boards/Assies is provided for the
Agilent 81100 Pulse/Pattern Generator Family.
These Boards/Assies are not repairable in the field and
the Assy Exchange Program is used!
Exchange Part is the complete Board/Assy.

Serial Numbers (Mainframe and Channels) stays with the customer.

Please refer to Chapter 4, Exchanging the Modules
and Chapter 5, Assembly-level Parts List

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Troubleshooting

```
Please refer to the model's Reference Guide,
   p/n 811xx-91021
for more information on Warnings and Errors.

 In addition refer to Section,

   |CONFIG| Screen - Selftest
            Chapter 2 - Programming Reference
                        - :SYST:ERR?
                        - :SYST:WARN?
                        - :SYST:WARN:STR?
                        - :SYST:WARN:BUFF?
```

Initial Tests ...

There could be a number of reasons why the instrument shows no signs of operation. If the instrument appears to be dead, proceed as indicated below.

Connect the AC Line Power Cord to the instrument's rear main power inlet.
Switch the Power Switch to **ON**

If the display is 'working', proceed with Selftests.

If the display stays dark, do the following
PRELIMINARY CHECKS

```
        |
        * Is AC Line Power available?
         ->      N        Provide AC Line Power!
        |
        Y
        |
        * Is AC Line properly connected?
         ->      N        Connect AC Line Power!
        |
        Y
        |
        * Is AC Line Fuse OK?
         ->      N        Change AC Line Fuse!
        |
        Y
        |
        * Is the Display'working' now? FANs running?
         ->      N        Proceed Power Supply Tests
        |
        Y
        |
        * Proceed with Selftests
```

Power Supply Tests ...

There are three fans on the rear of the unit. Are they running?

The **Power Supply Module** do have a fan of it's own.
Check if this fan is running!

If not, follow the procedure to open the unit
in Chapter Exchanging the Boards.

The two cable sets (A, B) coming out of the power supply module are connected to the Mother/CPU Bd. and to the left and right of the connectors A, B there are Test Points to measure the voltages!

Power Supply Voltages

output voltage	variations
+5 V	+.25 V / -.125 V
+5 VA	+.5 V / -.3 V
+12 V	+.6 V / -.36 V
-12 V	-.6 V / +.36 V
-5.2 V	-.26 V / +.156 V
-2 V	-.1 V / +.1 V
+24 V	+1.2 V / -.72 V

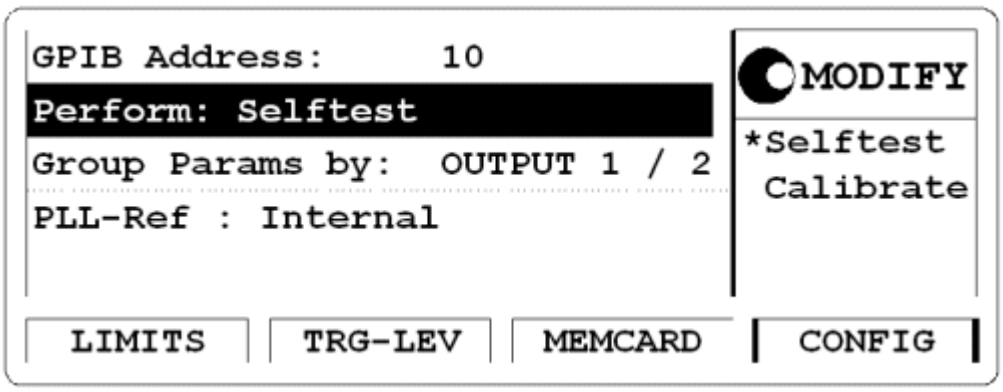
Selftests ...

The **Power-Up Selftest** runs the following tests:

- Interface
- uProcessor — uP Selftest Failure Messages —
  - ROM
  - RAM
- Modules — Module Selftest Failure Messages —

If this test fails you can press the HELP key to see a list of the specific error messages resulting from the test.
If the list is longer than the single screen, use the curser key to scroll the list.
Note that a long error list can result from a single initial error.
Therefore, begin to solve problems starting with the first message in the list and after the problem is cleared run the Selftest again.

The 81100 Family has an **additional built-in selftest.**
From the initial setup of the 811xxA select MORE |CONFIG| screen and set up as follows:



Above is the CONFIG screen of the 81110A.
(The 81101A/81104A screen do not show the capability to Calibrate the unit.)
(The 81101A screen do not show the capability to Group Params by: OUTPUT)

Press ENTER and wait till the Selftest ends.

In this test some additional tests to the above shown tests are done!

If the Selftest fails, a flashing **E** is displayed.
Press HELP to see the list of error messages.

Together with the Performance Test and the Applications info a confidence level of >96% can be assumed. This is because not all possible settings and functions could be done and checked.

For every error message there are troubleshooting tips given in this chapter. If none of these hints may help, there might be a problem with address decoding or the data bus drivers.

After a problem is cleared run Selftest again.

The unit tests the following components in the listed order:

1. comparator of clock input
2. comparator of external input
3. PLL
4. period divider of FPGA on Timing Board (*)
5. data-in register of TIGER-ICs
6. pattern memory)
7. strobe out
8. trigger out
9. Frontends
10. VCOs of TIGER-ICs

(*) Test #4 is not done during power up.

The following block schematic shows the

Test Points

of the above listed tests.

There are several possible causes for a failed test. A faulty element may produce a long error list. In the following, there is a list of some components, that affect different tests at the same time:

faulty components	affected tests
ADC circuit	**Clock In, Ext. In, PLL, Strobe Out, Trigger Out, Low/High Level**
Threshold DAC	**Clock In, Ext. In**
Clock Input circuit	**Clock In, Strobe Out**
PLL circuit	**PLL, Period Divider**
Period TIGER IC	**Period TIGER, Pattern RAM, Strobe Out, Trigger Out, Low/High Level, VCOs**
Delay/Width TIGER IC	**Delay TIGER, Width TIGER, Low/High Level, VCOs**
Period FPGA(Timing Brd.)	**VCOs**
Hardware register 0	**Clock In, Ext. In, PLL, Strobe Out, Trigger Out, Low/High Level**
Hardware register 1	**Clock In, Ext. In, Pattern RAM, Strobe Out, Trigger Out, Low/High Level, VCOs**
Hardware register 2	**Strobe Out, Trigger Out**
Hardware register 3	**Strobe Out, Trigger Out, Low/High Level, VCOs**
Hardware register 4	**Clock In, Ext. In, Period Divider**

Replacing Boards
Before replacing any board, make sure that the unit is calibrated properly and check the Power Supply.

If there are error messages concerning different boards, begin with the first error and try to fix it with the tips given in 'Error Description' and look in the above table.

Replacing Timing Board
Replace Timing Board, if only some of the following components fail:

Clock Input comparator, External Input comparator, PLL, Period divider, Period TIGER IC, Pattern RAM, Strobe Out, Trigger Out, VCO 0 or 1

Replacing Delay-Width Board
Replace Delay-Width Board of the channel displayed in the error message, if only some of the following components fail:
Delay TIGER, Width TIGER, VCO >= 2

A Delay-Width Board should only be replaced together with its corresponding Frontend Board.

Replacing Frontend Board
Replace Frontend Board of the channel displayed in the error message, if only the following tests fail:
Low/High Level

A Frontend Board should only be replaced together with its corresponding Delay-Width Board.

For replacing boards, follow the procedure in Chapter Exchanging the Boards.

Self Test Messages ...

A complete list of all Self Test Messages can be found here.

Register Usage ...

The 81100 Firmware uses the Standard Event Status, Operation Status, and Questionable Status registers for reporting instrument status, in accordance with the SCPI standard. The following lists the bits used in each register, and what they are used for:

Register: STANDARD EVENT STATUS REGISTER Bit: 7
This bit is set every time the instrument is powered on.

Register: STANDARD EVENT STATUS REGISTER Bit: 0
This bit is set in response to the *OPC command

Register: OPERATION STATUS REGISTER Bit: 1
This condition is set whenever the instrument starts changing its output signals.

Register: OPERATION STATUS REGISTER Bit: 1
This condition is cleared whenever the instrument has finished changing its output signals, the external signals are stable now.

Register OPERATION STATUS REGISTER Bit: 2
This condition is set whenever the instrument starts changing its range.

Register: OPERATION STATUS REGISTER Bit: 2
This condition is cleared whenever the instrument has finished changing its range, the external signals are stable now.

Register: OPERATION STATUS REGISTER Bit: 4
This condition is set whenever the instrument starts a frquency measurement.

Register: OPERATION STATUS REGISTER Bit: 4
This condition is cleared whenever the instrument has finished a frequency measurement, the measurement result can be obtained now.

Register: QUESTIONABLE STATUS REGISTER Bit: 0
Set/clear the QUEStionable STATus bit for VOLTage.

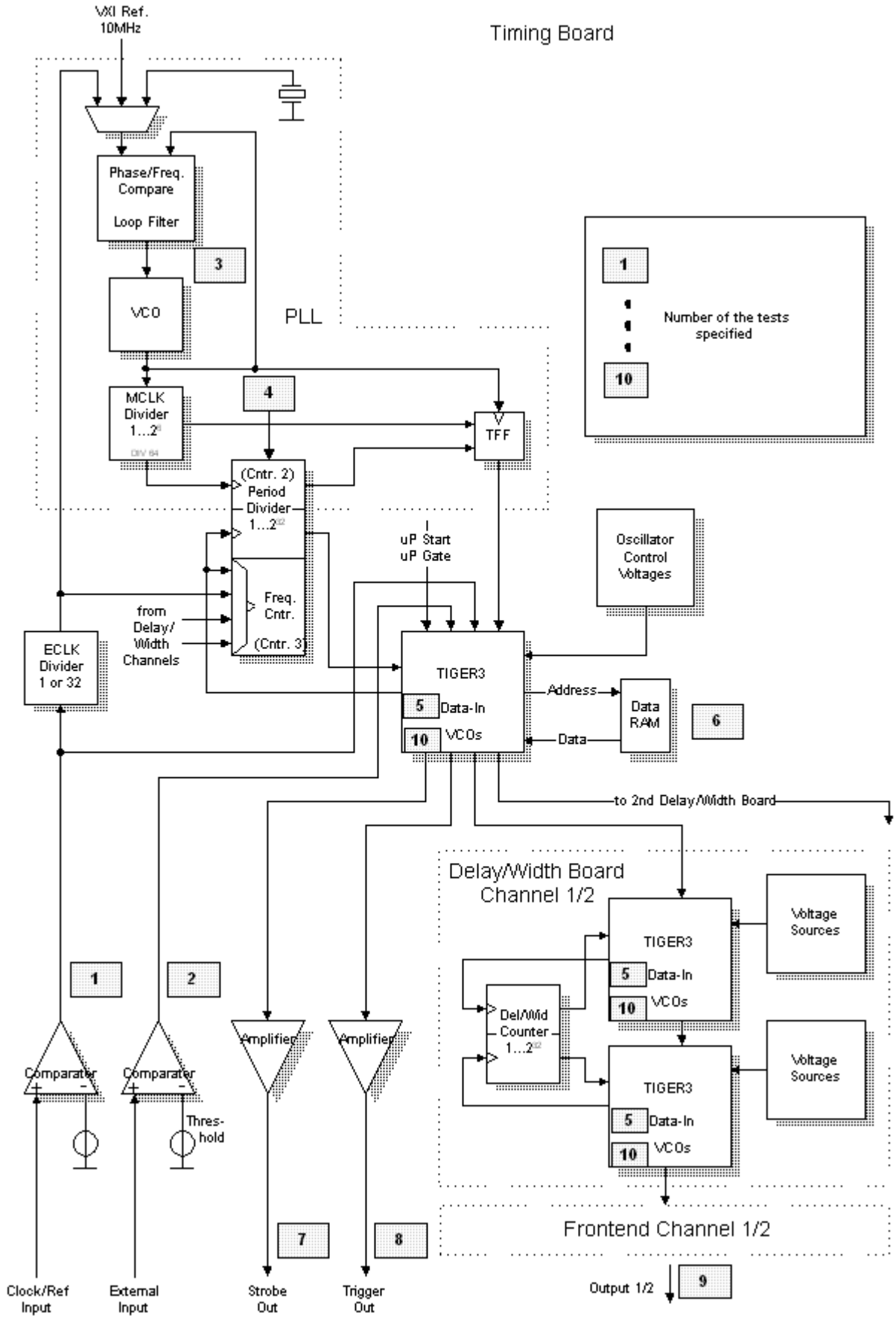
```
Register:         QUESTIONABLE STATUS REGISTER        Bit: 1
Set/clear the QUEStionable STATus bit for CURRent.

Register:         QUESTIONABLE STATUS REGISTER        Bit: 2
Set/clear the QUEStionable STATus bit for TIME.

Register:         QUESTIONABLE STATUS REGISTER        Bit: 5
Set/clear the QUEStionable STATus bit for VOLTage.
```

Verify Installation ...

After replacing a board do a complete Performance Test (and follow the Applications info) to make sure the unit is working within specification (with all features).



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Troubleshooting

Self Test Messages ...

Possible self test messages are:

- Microprocessor Selftest Failure Messages -

GPIB: **-330, Self-test failed;**
Selftest error: Microprocessor board failed
Local: **Selftest error: Microproc. board failed**
Hardware on the (Firmware-)uProcessorboard doesn't work.

GPIB: **-330, Self-test failed;**
ROM test failed
Local: **ROM test failed**
Flash Eprom's test failed on (Firmware-)uProcessorboard

GPIB: **-330, Self-test failed;**
RAM test failed
Local: **RAM test failed**
Static RAM's test failed on (Firmware-)uProcessorboard

GPIB: **-330, Self-test failed;**
Crystal Reference for uP lost
Local: **Crystal Reference for uP lost**
A loss of crystal reference has been detected and the VCO
is running at approximately half of maximum speed,
determined from an internal voltage reference.
Normally the external crystal frequency is VCO reference.

GPIB: **-330, Self-test failed;**
VCO for uP has not locked
Local: **VCO for uP has not locked**
VCO is enabled, but has not yet locked. Normally VCO has
locked on to the desired frequency.

GPIB: **-330, Self-test failed;**
Unexpected Reset of uP
Local: **Unexpected Reset of uP**
The reset was caused by
- the powerup reset circuit
- the software watchdog circuit
- the system protection submodule halt monitor
- a loss of frequency reference to the clock submodule
- the test submodule
Normally the last reset was caused by an external signal
or by the CPU executing a reset instruction.

GPIB: **-330, Self-test failed;**
Internal Serial Device Bus failed
Local: **Internal Serial Device Bus failed**
Internal serial device bus traffic over feedback path
has failed.

- Module Selftest Failure Messages -

Clock Input comparator test failed
The test of the clock input comparator failed.
Possible cause:
External clock input connected to signal source.
Voltage comparator out of order
Hardware registers 0, 1 and/or 4 out of order
Threshold DAC out of order
ADC circuit not working correctly

Description of this test:
The impedance of the clock input is set to 50 Ohm.
Comparator is enabled.
Threshold is set to its minimum (0x0000).
It is checked, if the measured signal is equal to a logical '0'. (V_ADC value is smaller than 1470.)
Threshold is set to its maximum (0x0FFF).
It is checked, if the measured signal is equal to a logical '1'. (V_ADC value is greater than 1470.)

Troubleshooting:
Make sure, that nothing is connected to clock input.
Check impedance of clock input.
(Hardware register 1 may also be faulty.)
Check whether clock input comparator is enabled.
(Hardware register 4 may also be faulty.)
Check threshold.
Check comparator output.
Check V_ADC value.
(Hardware register 0 may also be faulty.)

Ext. Input comparator test failed
The test of the external input comparator failed.
Possible cause:
External input connected to signal source.
Voltage comparator out of order
Hardware registers 0, 1 and/or 4 out of order
Threshold DAC out of order
ADC circuit not working correctly

Description of this test:
The impedance of the external input is set to 50 Ohm.
Comparator is enabled.
Threshold is set to its minimum (0x0000).
It is checked, if the measured signal is equal to a logical '0'. (V_ADC value is smaller than 1470.)
Threshold is set to its maximum (0x0FFF).
It is checked, if the measured signal is equal to a logical '1'. (V_ADC value is greater than 1470.)

Troubleshooting:
Make sure, that nothing is connected to external input.
Check impedance of external input.
(Hardware register 1 may also be faulty.)
Check whether external input comparator is enabled.
(Hardware register 4 may also be faulty.)
Check whether external input comparator is enabled.
Check threshold.
Check comparator output.
Check V_ADC value.(Hardware register 0 may also be faulty.)

PLL test (internal xxx MHz) failed
The test of the PLL failed at the displayed internal PLL frequency (250 Mhz, 333 MHz, 500 MHz, 666 MHz, 1000 MHz).
Possible cause:
PLL IC out of order
VCO of PLL out of order
Missing internal reference frequency
Hardware register 0 out of order
ADC circuit not working correctly

Description of this test:
VCO of PLL is switched on, if it isn't already on.
Internal referencefrequency is selected.
PLL frequency is set to 250 MHz
(below itsminimum of 333 MHz).
It is checked,
if signal PLL_LOW has its maximum level
(V_ADC value > 1210) and
signal PLL_HIGH has its maximum level
(V_ADC value > 3180).
PLL frequency is set to its minimum of 333 MHz.
It is checked,
if signal PLL_LOW has its minimum level
(V_ADC value < 1210) and
signal PLL_HIGH has its maximum level
(V_ADC value > 3180).

```
        PLL frequency is set to 500 MHz
        (between its minimum of 333 MHz and maximum of 666 Mhz).
        It is checked,
          if signal PLL_LOW has its minimum level
                (V_ADC value < 1210) and
             signal PLL_HIGH has its maximum level
                (V_ADC value > 3180).
        PLL frequency is set to its maximum of 666 MHz.
        It is checked,
          if signal PLL_LOW has its minimum level
                (V_ADC value < 1210) and
             signal PLL_HIGH has its maximum level
                (V_ADC value > 3180).
        PLL frequency is set to 1000 MHz,
        beyond its maximum of 666 MHz.
        It is checked,
          if signal PLL_LOW has its minimum level
                (V_ADC value < 1210) and
             signal PLL_HIGH has its minimum level
                (V_ADC value < 3180).
        VCO of PLL is switched off, if it was off before
        this selftest.

Troubleshooting:
        Check internal reference frequency (10 Mhz).
                (Hardware register 0 may also be faulty.)
        Check PLL IC.
                (Hardware register 0 may also be faulty.)
        Check VCO of PLL.
                (Hardware register 0 may also be faulty.)
        Check signals PLL_LOW and PLL_HIGH.
        Check V_ADC value.
                (Hardware register 0 may also be faulty.)
```

Period divider test failed

```
The test of the period divider in the FPGA on the timing
board failed.
Possible cause:
        Counter 2 in FPGA out of order
        MCLK divider out of order
        PLL out of order
        Hardware register 4 out of order

Description of this test:
        VCO of PLL is switched on, if it isn't already on.
        PLL frequency is set to 500 MHz.
        MCLK divider factor is set to 64.
        Counter mode of FPGA is enabled, counter 2 is used
          as master for measurement.
        A preset value of 0xFFFFFFFF is loaded for counter 2
          and a reset for this counter is done.
        Counting is started. ('start_count' bit is set.)
        After 0.5 sec counting isstopped by disabling MCLK
        divider.
        It is checked, if the current contents of counter 2
          is between 0xFF000000 and 0xFFF00000.
        MCLK divider is enabled and 'start_count' bit is unset.
        The old preset value of counter 2 is reloaded and a
        reset for this counter is done.
        VCO of PLL is switched off, if itwas off before this
        selftest.

Troubleshooting:
        If PLL test has failed before, go back to
          troubleshooting for PLL.
        Make sure, that the frequency at input of MCLK Divider
          is 500 MHz and at output of MCLK Divider approximately
          500 MHz / 64 = 7.8125 MHz.
```

Period TIGER IC test failed
Delay TIGER IC test failed (ch. x)
Width TIGER IC test failed (ch. x)

```
The test of the DATAIN-shift-register on the
  Period/Delay/Width TIGER IC (channel x) failed.
Possible cause:
        TIGER IC out of order
```

Description of this test:
The shift-in-register of the Period TIGER IC is tested first, if a delay-width board is available, the shift in register of the Delay and the Width TIGER ICs are checked afterwards.
Testing is done by comparing the shifted in value (0xA5A) with the read out value.

Pattern RAM test failed
The test of the pattern RAM failed.
Possible cause:
Pattern RAM out of order
Period TIGER IC out of order
Hardware register 1 out of order

Description of this test:
Period TIGER IC is enabled to access pattern RAM.
(Every read or write access to the RAM generates a clock edge which increments the burst counter. The burst counter generates the address signal for the RAM.)
Period TIGER IC is reseted.
Correct burst mode is selected.
Burst counter in TIGER IC is loaded with its maximum value.
Pattern RAM access is enabled.
The following data is written into RAM periodically (all addresses are tested):
0x26, 0x6E, 0xA7, 0xEF, 0x30, 0x70, 0xB8, 0xF1, 0x09, 0x02, 0x4A, 0x83, 0xCB, 0x14, 0x5C, 0x95, 0xDD
Pattern RAM access is disabled.
Period TIGER IC is reseted.
Burst counter in TIGER IC is loaded with its maximum value.
Pattern RAM access is enabled.
Data is read from RAM and compared with the value written in before.
Pattern RAM access is disabled.
Period TIGER IC is disabled to access pattern RAM.
Period TIGER IC is reseted.

Troubleshooting:
Check whether pattern RAM is enabled and disabled. (Hardware register 1 may also be faulty.)
Check whether addresses are changing.
Check Period TIGER IC.

Trigger and strobe Levels

Test Limits:

level mode	value	into 50 Ohm lower limit	into 50 Ohm upper limit	into open lower limit	into open upper limit
TTL-LOW	0V	-0.2V	0.5V	-0.4V	1.0V
TTL-HIGH 2.5V	2.1V	2.7V	4.2V	5.4V	
ECL-LOW	-1.8V	-1.9V	-1.5V	-3.0V	-2.0V
ECL-HIGH -0.8V	-0.95V	-0.7V	-1.9V	-1.4V	
CASS-LOW -1V	-1.2V	-0.8V	-2.4V	-1.6V	
CASS-HIGH	0V	-0.2V	0.2	-0.4V	0.4V

Strobe Out test failed (TTL low)
Strobe Out test failed (TTL high)
Strobe Out test failed (ECL low)
Strobe Out test failed (ECL high)
The test of the strobe out signal at the level given in brackets failed.
Possible cause:
Strobe output circuit out of order
Hardware register 0, 1, 2 and/or 3 out of order
Period TIGER IC not working
Clock input circuit not working
ADC circuit not working correctly

Description of this test:
Clock input impedance is set to 50 Ohm.
Clock input is enabled.
Period TIGER IC is set into reset.
uP trigger event is cleared.
Period TIGER IC is set into this mode:
clock source: External Clock

```
                clock mode:       Continuous
                pulse type:       Burst
                trigger source:   TRIGIN (uP)
                clock edge:       positive
                arm edge:         positive
                formatter mode:   RZ
                burst length:     2
        Reset of Period TIGER IC is released.
        uP trigger event is set.
        TTL mode is set.
        A positive edge is generated by changing the
          clock-in-threshold from 0x0000 to 0x0FFF.
          (After setting 0x0000, there is a wait cycle
          of 10.0 ms; after setting 0x0FFF, there is a wait
          cycle of 1.0 ms.)
        It is checked, if TTL high level is
          see Test Limits
        A positive edge is generated by changing the
          clock-in-threshold from 0x0000 to 0x0FFF.
          (After setting 0x0000, there is a wait cycle
           of 1.0 ms; after setting 0x0FFF, there is a wait
           cycle of 1.0 ms.)
        It is checked, if TTL low level is
          see Test Limits
        ECL mode is set.
        A positive edge is generated by changing the
          clock-in-threshold from 0x0000 to 0x0FFF.
          (After setting 0x0000, there is a wait cycle of 100.0 ms;
          after setting 0x0FFF, there is a wait cycle of 1.0 ms.)
        It is checked, if ECL high level is
          see Test Limits
        A positive edge is generated by changing the
          clock-in-threshold from 0x0000 to 0x0FFF.
          (After setting 0x0000, there is a wait cycle of 1.0 ms;
           after  setting 0x0FFF, there is a wait cycle of 1.0 ms.)
        It is checked, if ECL low level is
          see Test Limits

Troubleshooting:
        If clock input test has failed before, go back to
          troubleshooting for clock input.
        If only TTL errors or only ECL errors occur, check whether
          TTL-ECL switch is working.
         (Hardware register 2 may also be faulty.)
        Check whether signal TRIGOUT_N is low (high) and TRIGOUT_C
         is high (low) for low (high) level at strobe output
         connector.
        Check hardware register 3 for uP trigger event
         (Signals UPTRIGN, UPTRIGC).
        Check Period TIGER IC.
        Check V_ADC value.
         (Hardware register 0 may also be faulty.)

Trigger Out test failed (TTL low)
Trigger Out test failed (TTL high)
Trigger Out test failed (ECL low)
Trigger Out test failed (ECL high)
The test of the trigger out signal at the level given in
  brackets failed.
Possible cause:
        Trigger output circuit out of order
        Hardware register 0, 1, 2 and/or 3 out of order
        External width mode of Period TIGER IC not working
        ADC circuit not working correctly

Description of this test:
        Before starting this selftest, the TIGER ICs must be set
         to external width mode.
        TTL mode is set.
        uP trigger event is cleared.
          (There is a wait cycle of 100.0 ms afterwards.)
        It is checked, if TTL low level is
          see Test Limits
        uP trigger event is set.
          (There is a wait cycle of 1.0 ms afterwards.)
        It is checked, if TTL high level is
          see Test Limits
```

```
          ECL mode is set.
          uP trigger event is cleared.
            (There is a wait cycle of 100.0 ms afterwards.)
          It is checked, if ECL low level is
            see Test Limits
          uP trigger event is set.
            (There is a wait cycle of 1.0 ms afterwards.)
          It is checked, if ECL high level is
            see Test Limits

Troubleshooting:
          If only TTL errors or only ECL errors occur, check
            whether TTL-ECL switch is working.
           (Hardware register 2 may also be faulty.)
          Check whether signal TRIGOUT_N is low (high) and
            TRIGOUT_C is high (low) for low (high) level at strobe
            output connector.
          Check hardware register 3 for uP trigger event
           (Signals UPTRIGN, UPTRIGC).
          Check Period TIGER IC.
          Check V_ADC value.
           (Hardware register 0 may also be faulty.)

Low Lev error (no offs, xx ohm, ch. x)
High Lev error (no offs, xx ohm, ch. x)
The test of the low/high level without offset and a source
  impedance of xx ohm on Frontend (channel x) failed.
Possible cause:
          Frontend out of order
          Wrong calibration of Frontend
          Hardware register 0, 1 and/or 3 out of order
          External width mode of Period, Delay or Width
            TIGER ICs not working
          ADC circuit not working correctly

Low Lev error(pos offs, xx ohm, ch. x)
High Lev error (pos offs, xx ohm, ch. x)
Low Lev error  (neg offs, xx ohm, ch. x)
High Lev error (neg offs, xx ohm, ch. x)
The test of the low/high level with positive/negative offset
  and a source impedance of xx ohm on Frontend (channel x) failed.
Possible cause:
          Frontend offset amplifier out of order
          Frontend out of order
          Wrong calibration of Frontend
          Hardware register 0, 1 and/or 3 out of order
          External width mode of Period, Delay or Width TIGER ICs
            not working
          ADC circuit not working correctly

Description of this test:
          Before starting this selftest, the TIGER ICs must be set to
            external width mode.
          Depending on the channels being available, the Frontends
            are tested according to their specific characteristics.
          For every Frontend type the following procedures are done:

          Parameters are set to measure high and low
            level (offset = 0 V).
          uP trigger event is cleared.
          It is checked, if the low level voltage is in the allowed
            range. (See below)
          uP trigger event is set.
          It is checked, if the high level voltage is in the allowed
            range. (See below.)

          Parameters are set to measure high and low level with a
            positive offset of 1.0 V.
          uP trigger event is cleared.
          It is checked, if the low level voltage is in the allowed
            range. (See below.)
          uP trigger event is set.
          It is checked, if the high level voltage is in the allowed
            range. (See below.)

          If a negative offset is tested:
          Parameters are set to measure high and low level with a
```

```
  negative offset of -1.0 V.
uP trigger event is cleared.
It is checked, if the low level voltage is in the allowed
  range. (See below.)
uP trigger event is set.
It is checked, if the high level voltage is in the allowed
  range. (See below.)
Common settings for every Frontend type:
termination voltage:       0.0 V
termination resistor:      50.0 Ohm
source impedance of connected Frontend:     50.0 Ohm
rise time:        5.0 ns   (Exception: HP 81112A      0.8 ns)
fall time:        5.0ns    (Exception: HP 81112A      0.8 ns)
Specific settings:
81101A/81105A/81111A               10 V
source impedance:                  50.0 Ohm
test levels:
         no offset:
                  -4.0 V   (allowed: -4.3 V to -3.7 V)
                   4.0 V   (allowed:  3.7 V to  4.3 V)
         with pos. offset (1.0 V):
                  -3.0 V   (allowed: -3.3 V to -2.7 V)
                   5.0 V   (allowed:  4.6 V to  5.4 V)
         with neg. offset (-1.0 V):
                  -5.0 V   (allowed: -5.4 V to -4.6 V)
                   3.0 V   (allowed:  2.7 V to  3.3 V)


81112A/81131A              3.8 V
source impedance:                  50.0 Ohm
test levels:
no offset:
                  -0.5 V   (allowed: -0.62 V to -0.38 V)
                   0.5 V   (allowed:  0.38 V to  0.62 V)
with pos. offset (1.0 V):
                  0.5 V    (allowed: 0.38 V to 0.62 V)
                  1.5 V    (allowed: 1.34 V to 1.66 V)
with neg. offset (-1.0 V):
                  -1.5 V   (allowed: -1.66 V to -1.34 V)
                  -0.5 V   (allowed: -0.62 V to -0.38 V)

81132A                     2.5 V
source impedance:                  50.0 Ohm
test levels:
no offset:
                  -0.5 V   (allowed: -0.55 V to -0.45 V)
                   0.5 V   (allowed:  0.45 V to  0.55 V)
with pos. offset (1.0 V):
                  0.5 V    (allowed: 0.45 V to 0.55 V)
                  1.5 V    (allowed: 1.35 V to 1.65 V)
with neg. offset (-1.0 V):
                  -1.5 V   (allowed: -1.65 V to -1.35 V)
                  -0.5 V   (allowed: -0.55 V to -0.45 V)


Troubleshooting:
         Check calibration of Frontend (recalibrate it).
         If only positive or negative offset failed, check
           offset amplifier.
         Check internal termination of Frontend.
         Check hardware register 3 for uP trigger event
           (Signals UPTRIGN, UPTRIGC).
         Check TIGER ICs.
         Check V_ADC value. (Hardware register 0 may also be faulty.)
```

VCO x failed test for 360MHz
VCO x failed test for 540MHz
VCO x failed test for 720MHz

```
The VCO with internal number x failed the selftest at the lower
  frequency limit / operating frequency / upper frequency limit.
The VCOs are numbered as follows:
         0        Period TIGER VCO 1
         1        Period TIGER VCO 2
         2        Delay TIGER VCO 1 (channel 2)
         3        Delay TIGER VCO 2 (channel 2)
         4        Width TIGER VCO 1 (channel 2)
         5        Width TIGER VCO 2 (channel 2)
```

```
        6       Delay TIGER VCO 1 (channel 1)
        7       Delay TIGER VCO 2 (channel 1)
        8       Width TIGER VCO 1 (channel 1)
        9       Width TIGER VCO 2 (channel 1)

Possible cause:
        VCO uncalibrated
        corresponding TIGER IC not working
        corresponding DAC not working
        FPGA on the timing board not working
          (measurement failed)
        PLL not working (measurement failed)
        Hardware register 1 out of order

Description of this test:
        VCO of PLL is switched on, if it isn't already on.
        Depending on the Delay-Width Boards being available,
          the VCOs in the TIGER ICs are tested. (Description of
          VCO-test (see below.)
        The Period TIGER is tested last.
          (Description of VCO-test see below.
        VCO of PLL is switched off, if it was off before this
          selftest.
        The test of a VCO is done in the following way:
        TIGER IC is set into reset.
        TIGER IC is set into this mode:
                clock source:     Internal VCO
                clock mode:       Continuous
                pulse type:       Pulses
                trigger source:   TRIGIN (uP)
                clock edge:       positive
                arm edge:         positive
                formatter mode:   RZ
                burst length:     1
        External divider is disabled.
        Internal period divider factor is set to 64.
        Oscillator is enabled for calibration.
        Reset of TIGER IC is released.
        Pulses are started by triggering the Period TIGER IC
          with the uP trigger event.
        It is checked, if the measured frequencies are in the
          allowed ranges:
                tested:  360 MHz  allowed:          342 MHz to 378 MHz
                tested:  540 MHz  allowed:          513 MHz to 567MHz
                tested:  720 MHz  allowed: 684 MHz to 756MHz
        External divider is enabled.

Troubleshooting:
        If PLL test has failed before, go back to troubleshooting
          for PLL.
        Check whether external divider of the corresponding
          TIGER IC is disabled.
        Check hardware register 3 for uP trigger event.
        Check if Period FPGA (frequency measurement) is working
          correctly.
        Check corresponding TIGER IC.

Complete Listing of Firmware ERRORs + Description

Complete Listing of BIOS ERRORs + Description
```

3

Block Theory

a. µProcessor Board

b. Timing Board

c. Output Channels

d. Power Supply

Block Theory
3 a

µProcessor Board

General

The µProcessor Board controls the 811xxA. It receives data from Flash-EEPROM and battery-backed Static RAM, the Keyboard and the GPIB interface. It communicates with the boards in the instrument through the VXI-Interface. The µP. Bd. is designed around the MC 68331 Microprocessor

Functional units are:

- CPU - Motorola 68331 running at 16.7MHz
- 2MB Flash-EEPROM
- 256KB unbuffered RAM
- 256KB buffered RAM
- Battery, Battery Backup and Reset
- Beeper
- Oscillator
- GPIB interface
- PCMCIA slot for use with memory cards up to 2MB
- Display and Keyboard interface
- VXI interface
- 2 VXI slots

Features

- GPIB programmable
- Interface - same as in Agilent 8110A (display and keyboard are the same, new version of RPG board requiered)
- Address space of Flash-EEPROM and PCMCIA card can be exchanged on startup by pressing a special key combination (‘1’ & ‘3’), to allow easy software update (CPU running on memory card!).

Block Diagram

Functional Units on the µP Board ...

The Microprocessor PC Board's functional units, and what they are for:

Battery Backup and Reset	Sets conditions during power-up
Battery	Supports the Static RAMs when the instrument is not powered
Beeper	Gives an audible warning tone and makes a 'click' when a key is pressed
Boot Control	Decides whether to boot the Microprocessor from the flash EPROMs or from the Memory Card
Oscillator	Provides clock pulses for the Microprocessor
GPIB Interface	For accessing the instrument externally - uploading and downloading of data, - or for control
Display and Keyboard Interface	Interface to the display, keyboard and Rotary Pulse Generator (RPG)
PCMCIA slot	Allows the usage of PCMCIA memory cards. The memory card contains battery-backed RAMs containing different firmware and store/recall data settings to that held in the Flash EEPROMs
Flash EEPROMs	Contains the firmware that is used to specify and control the instrument.
Buffered RAM	Contains data that is regularly changing, but has to be persistent when the power is down.
Unbuffered RAM	Contains data that is regularly changing, but may be lost when the power is down.
VXI Interface	Controls the VXI/VME bus, used to access the instrument specific modules.
VXI Slots	Two slots to plug in the instrument specific VXI modules.

Detailed Description ...

Battery Backup and Reset
When power is applied to the Microprocessor Board, the timer (formed by U4 and associated components) holds down the MPU Reset line for a period exceeding 100ms. This allows time for a general MPU reset and a longer period for the MPU clock PLL to stabilise. One half of the Static RAMs (Buffered RAM) are backed up by the battery when the instrument is switched OFF and during reset. U4 disconnects the battery and enables the Power Supply Voltage via Q1 when the instrument is switched ON and after reset.
(This section is on schematic sheet 1.)

Beeper
The beeper is directly driven by the MPU and inverter U32. An MPU high output level is inverted to low by U32 for the other pin of the beeper. The reverse applies when the MPU output goes low. The MPU pin toggling is driven by the firmware wich provides a number of frequencies for the beeper.
(This section is on schematic sheet 1.)

Boot Control
If the front panel keys '1' and '3' are pressed during switch-on, the system is booted from the Memory Card instead of the Flash EEPROMs.
Gate U33 combines the two keyboard signals and sets D-Flipflop U5. Data from the Flipflop controls the multiplexer U3, which generates the correct chip selects for the Flash EEPROMs and the memory card out of the corresponding chip selects from the MPU.

During MPU reset the general-purpose IO lines are regarded as input lines. After reset they are configured as required (by taking low certain lines on the MPU Databus) because they are used as mode select lines for the general IO lines.
In this case, line 4 and line 9 are set to low by U32.
(This section is on schematic sheet 1.)

Display and Keyboard Interface

Display Enabling

This description does not cover the Display Unit, which can be considered as a replaceable unit.
The Display is blanked at system initialization to prevent displaying of random information. It is activated by writing to U27 to set signal LDISPBL.
Shift register U2 controlling U34/U43 provides correct setup and hold times between Read/Write and valid Data Bus. Additionally, the software waits 2ms between Read/Write cycle.
Resistors R13 - R15 reduce overshoot.
(This section is on schematic sheet 1.)

Buffering

Buffer U51 restores data rise and fall times due to RFI filtering. The main reason for buffering is to disable the data bus if used by other circuits inside the shielded case, thus minimising RFI.
(This section is on schematic sheet 2.)

Keyboard

Whenever a key is pressed an interrupt is generated by gate U36. U28 sequencially latches data to produce 4 columns with a 'travelling' low level. If a key is pressed it connects a column to one of 8 rows formed by the inputs to latch U23. By reading the 12 bit 'word' thus formed, the MPU can calculate which key was pressed, as each key has a unique row-column combination.
(This section is on schematic sheet 4.)

Rotary Pulse Generator

This description does not cover the RPG, which can be considered as a replaceable unit.
U33 buffers the RPG interrupt signal. U33 also provides the MPU with a biffered directional signal.
(This section is on schematic sheet 1.)

GPIB Interface

U22 divides the system clock frequency by 4 to produce the GP-IB clock at approximately 4.2MHz. U24 is the GP-IB controller.
The LDRD (Low Data Read) signal is inverted by U44 to become HDRD (High Data Read). The Databus is buffered by U23. Data and control lines are buffered by U25 and U26.
(This section is on schematic sheet 4.)

Oscillator

The MPU is clocked by an internal PLL oscillator, using an external crystal. The crystal oscillates at 32.768kHz, prodicing final operating frequencies of 8.38MHz during reset and 16.78MHz during normal operation. The crystal, Y1, is tuned by R11/R12 and C2, C3.
(This section is on schematic sheet 1.)

PCMCIA Slot

This description does not cover the Memory Card, which can be considered as a replacable unit.
Buffering of address and data busses is provided by U53 - U55.
(These sections are on schematic sheet 2 and sheet 6.)

Flash EEPROMs

These EEPROMs contain the current version of the firmware used in the instrument, but can be superceded by firmware stored on a memory card, which can take precedence at Bootup. The MPU can download a copy of the firmware in the memory card to the Flash EEPROMs.
(This section is on schematic sheet 3.)

Static RAMs

These RAMs contain data that varies during operation.
U18 - U21 contain data that must be retained, such as configuration information. These RAM ICs are battery-backed to retain data during reset or after switch off. U14 - U17 are not battery-backed.

(This section is on schematic sheet 2.)

VXI-Slots

Buffering

The address- and databus is buffered by U8 - U10.
The control signals on the VXI bus are buffered by U11.

Control Signals

The control signals for the VXI bus are generated by the VXI-Interface (U29).

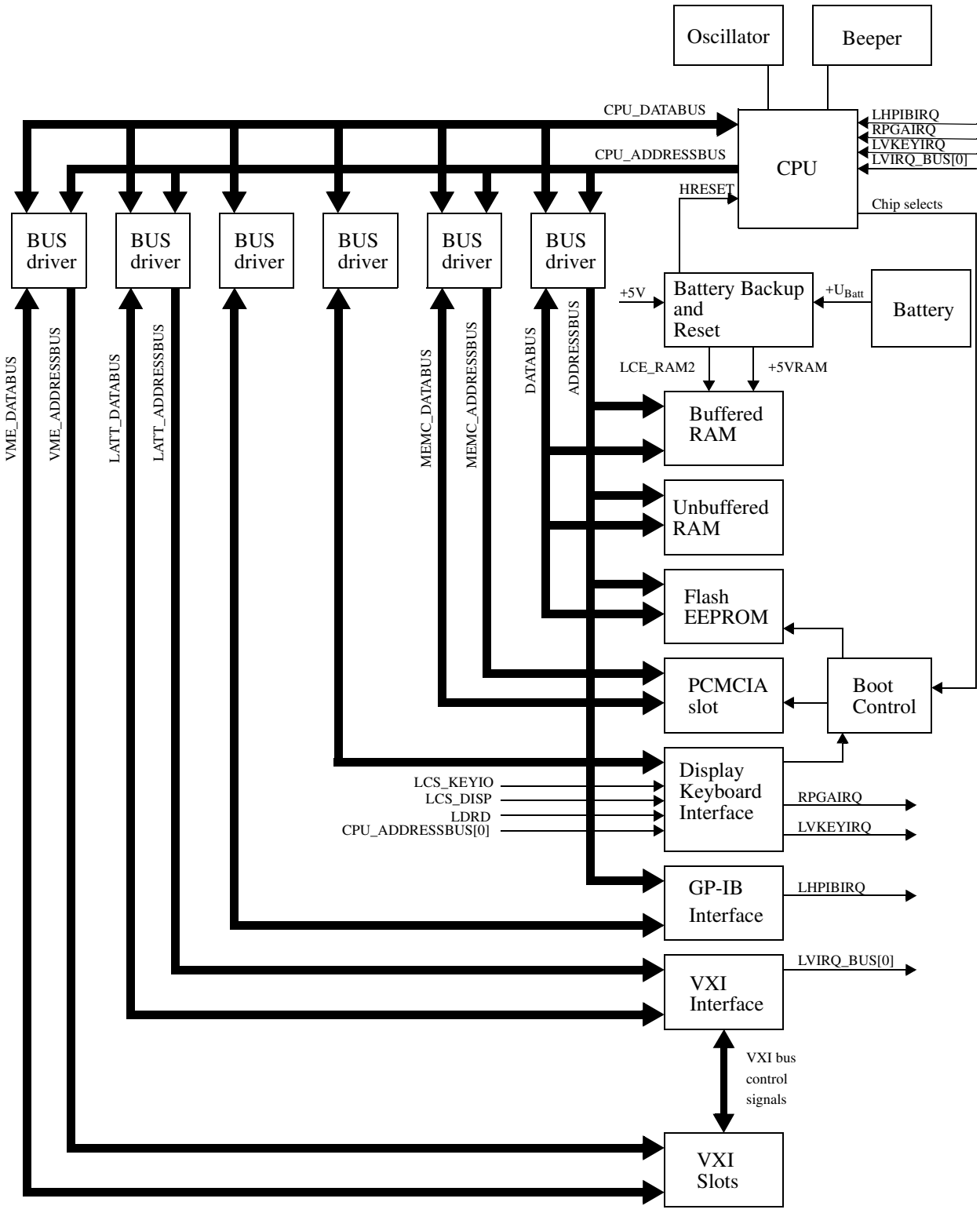
(This section is on schematic sheet 2 and sheet 7.)

VXI-Interface

The VXI-Interface implements the requiered control signal protocol for the VXI bus. The required data and address lines are buffered by U10 to avoid the programmable logic device to block the MPU if the programmed image is corrupt.
A completed access to the VXI bus is reported to the MPU by driving LDSACK1 to low. If the device on the VXI bus doesn't respond correctly, the cycle is aborted by the MPU's internal timeout generation.
The programming of U29 is done via U30. The access to U30 is enabled/disabled by signal LLATT_PROG (directly from the MPU). The enabling/disabling of U30 avoids accidently erasing of U29.

(This section is on schematic sheet 5.)

1.0 uProcessor Block Diagramm



3 b

Block Theory, Timing Boards

I. 81101A, 81104A, 81110A

II. 81130A

Block Theory
3 b I

Timing Board 81101A, 81104A, 81110A

General

The main task of the Timing Board is to generate the period signal, which drives the Delay/Width Board.
The heart of the Timing Board is a timing generator IC (TIGER3 : **TI**ming **GE**neratoR **3**rd generation), which is basically an astable oscillator when it is running without external drive or triggering, or a monostable oscillator when triggered from the PLL or a source external to the Timing Board. Triggering from the PLL provides greater period accuracy and stability. Voltage sources and counters control the period of the TIGER3 output signals.
TIGER3 is also capable of producing a specified number of pulses, called a burst.

Functional units are:

- Clock/Reference Input
- External Input
- Strobe Output
- Trigger Output
- ECLK Divider
- PLL
- TIGER3
- Data RAM
- Oscillator Control Voltages
- Low noise supply voltage generation
- DVT BIOS hardware
- Address decoding, control registers and Cal-EEPROM

Block Diagram

Detailed Description ...

DVT BIOS Hardware (Sheets 1 to 4)
The DVT BIOS hardware has the function to interface between the VXI-Bus and the module specific hardware on the Timing Board. This interface is accomplished via a local processor. This board is realized as a plug-in board to the Timing Board. The complete VXI-interface-hardware is located near the J1-connector on the board.

The board has buffers to the VXI-Bus, the module hardware and a FPGA. The FPGA does the arbitration between the local CPU and the VXI-Bus, contains the VXI-Bus configuration registers and other VXI-Bus specific functions.

The BIOS Board consists of the MC68331 CPU, SRAM, Flash-EEPROM, buffers to the Timing Board, interfaces to an emulator, terminal and an EEPROM-load and debugging tool.

Address Decoding, Control Register and Cal-EEPROM (Sheets 5 and 6)
This functional unit provides all address signals, write- and read-strobes, reset signals and registered control signals, which are necessary to control the Timing Board, the Delay/Width Boards and the Amplifier Boards.

The Cal-EEPROM stores the calibration tables of the
- Period Tiger,
- ADC circuit,
- input-threshold DAC's.

At switch-on the Processor reads the calibration tables and keeps it in its local RAM. For debug/service it is possible to suppress the usage of the calibration data from the EEPROM, by shortening the pins 1 and 2 of J5 during the startup phase.

Low Noise Supply Voltage Generation
All VXI supply voltages (-24V, -12V, -5.2V, -2V, +5V, +12V, +24V) are LC-filtered at the board input (Sheet 2) by 3.3µH inductors and 22µF or 10µF Tantalum capacitors. These filters are especially useful to suppress power-supply noise (in the region of about 100kHz up to 1MHz). Ceramic capacitors are distributed all over the board to suppress high frequency noise.

For noise sensitive devices, especially the oscillators and their controlling circuits, linear regulators (Sheet 12) generate additional voltages. These voltages are
- VCC_OSC (+8.3V, U401),
- VEE_OSC (-8.3V, U402),
- +20VVCO (U407),
- VP_PLL (+6.3V, U408, Q403),
- +10VVCO (U408, Q405),
- -4.8V_TG (U404, Q402).

The TTL I/O interface of the Tiger uses +3.5V, generated by U403 and Q404.
The amplifiers need +31V and -31V. The DC/DC converter circuits of U501 and U551 with surrounding components generate these voltages.

The +31V is realized by generating an offset voltage of approximately 7V out of the +12V power supply. This offset voltage is added to the +24V supply voltage. The same principle is used for the -31V. Thereby it is to observe that the DC/DC converters U501/U551 regulate its output voltage so that they receive a positive feedback voltage of 1.25V. With the +31V this is achieved by two resistors that divide the output voltage. This is not possible with the -31V since this voltage is negative. Therefore a current mirror circuit made up of Q552, Q553 and Q554 is used to invert the polarity of the feedback voltage.

External Input (Sheet 14 and 16)
A signal at the external input can start, stop or gate the period generator. In external width mode the period and width of the signal from the external input are maintained.

The external input circuit converts the input voltage to an ECL signal

The external input signal enters through connector J602. The input impedance is either 50Ohm if relay K602 is closed or about 10kOhm (high impedance) if the relay is open.

The high-speed comparator U601 has an input threshold voltage of 0V and an input voltage range of about +/-3V, so the external input signal must be attenuated and level-shifted. Diodes CR605 to 607 prevent the comparator from hazardous voltages. A resistor/capacitor network and the threshold generation (U603,

U604) attenuate and shift the input signal.

The threshold voltage is generated and adjusted by the DAC U603 and the operational amplifiers U604. To prevent that the internal threshold voltage causes any damage to the connected external signal source it is compensated to a level of 0V regarding the input connector J602 using the operational amplifier U605.

Clock/Reference Input (Sheet 14 and 16)
The Clock/Ref. input can be used as reference clock for the PLL (5MHz or 10MHz nom.) or as external clock source.

The Clock/Reference input circuit works in exactly the same way as the external input.

Strobe Output (Sheet 15)
The Strobe output amplifier converts the differential ECL-level strobe signal of the Tiger IC to an either TTL or ECL compatible single ended output. In Burst mode Tiger delivers one pulse per burst and in pattern mode a user-defined NRZ pattern.

Diodes CR705 shift the Tiger output signal to a lower level, which drives the differential amplifier Q710/Q711.

When TTL levels are selected, the signal LTTLHECLSTR switches transistors Q708 and Q712 on and so sets the highlevel to about 5V (unloaded output) and the amplitude current to approximately 100mA. This gives a highlevel of 2.5V and a lowlevel of 0V with an external 50Ohm-termination resistor connected to ground.

In ECL level mode transistors Q708 and Q712 are off, so the amplitude current is reduced to 36mA and the highlevel voltage is about -1.6V if the output is unloaded. When the output is terminated with 50Ohm to ground the highlevel is -0.8V and the lowlevel is -1.8V.

If in ECL level mode the output is terminated with 50Ohm to ground and the transistor Q711 is off, a current flows from ground through the termination resistor and the resistors R734 to R738 to the voltage source made of transistor Q709 and the surrounding network of resistors and diodes. This happens vice versa if transistor Q710 is off. Since this voltage source cannot sink current a current load is mandatory. This function is achieved by transistor Q714 and the resistor R730 which form a current source that is switched on by the transistor Q712 in ECL level mode.

Trigger Output (Sheet 15)
The Trigger output sends one RZ pulse (50% dutycycle) per generated period.
The trigger amplifier circuit is identical to the Strobe output.

External Clock Divider (Sheet 10)
The divider is build from a 8bit counter and a 2-to-1 multiplexer to select divide factor 1 or 32. The divide factor 32 is used to measure an external frequency larger than 10MHz with the FPGA U104.
For lower frequencies the divide ratio is 1.

Phase Locked Loop PLL (Sheet 9)
The PLL consists primarily of a RF oscillator (Y302) with a frequency range of 330MHz to 670MHz, a PLL frequency synthesizer chip (U302) and a loop filter.

The oscillator sends its output signal AC-coupled to an ECL-splitter circuit U305, which converts the single ended signal into two differential ECL signals, one for phase-frequency-compare and one to a divider. U306 and surrounding components regulate the dutycycle of the splitter output to 50%.

A flipflop divides the output of the 20MHZ-reference oscillator Y301 by two. The multiplexer U301 allows selecting from 3 different reference sources:
- the VXI reference,
- an external reference clock,
- the internal reference.

The selected reference clock is applied to the PLL IC U302.

Inside the IC the clock signal is passed through a reference divider. A second divider processes the output from the VCO (Splitter), and the two divided signals are phase-frequency-compared, producing an output voltage.

This signal is filtered with the active integrator circuit U303 and some passive components. A LC low-pass-filter suppresses the unwanted spectral components. U 304 limits the range of the output voltage of the loop filter to about 0V to 12V, a range suitable for tuning the VCO to frequencies between 330MHz and 670MHz. An ECL divider and a cascaded divider in FPGA U104 divide the second output signal of splitter U305 to 1mHz up to 330MHz. The arrangement of the circuits (U353-356, U104) is such, that the output signal has always 50% dutycycle.

TIGER3 (Sheet 7)
The TIGER (TIming GEneratoR) has 4 signal inputs:

- mPTRIG from the CPU
- EXTIN from external input
- MCLK_DIV from the PLL
- ECLK_PerTG from Clock input

The inputs can start, stop or gate the TIGER oscillator. mPTRIG and EXTIN can also start, stop or gate the PLL clock or the clock signal from the Clock/Reference input by enabling or disabling the clock path through the TIGER IC.

The TIGER has 4 used signal outputs:

- TRIGDEL1 drives Delay/Width board 1
- TRIGDEL2 drives Delay/Width board 2
- TRIGOUT drives the Trigger Output
- STROUT drives the Strobe Output

TRIGOUT and STROUT levels are ECL compatible, while the TRIGDEL outputs are open collector outputs which generate a swing of about 300mV when externally terminated to Ground.

The TIGER has a burst counter which allows generating a counted number of pulses (1 to 65536). Instead of putting out pulses the TIGER can also send a pattern stream. The pattern comes from an external high speed BiCMOS RAM, which is addressed from the TIGER burst counter.

The TIGER is programmed from the CPU with a 3 wire serial interface. The signals SDATA0, SHFTCLKPERTG and WRCLKPERTG are LVCMOS compatible.

The TIGER has 2 internal oscillators to allow range free period, delay or width sweeps. DAC's and operational amplifiers generate differential control voltages for the oscillators. The control voltages are in an range of about -0.8V to -3.2V.

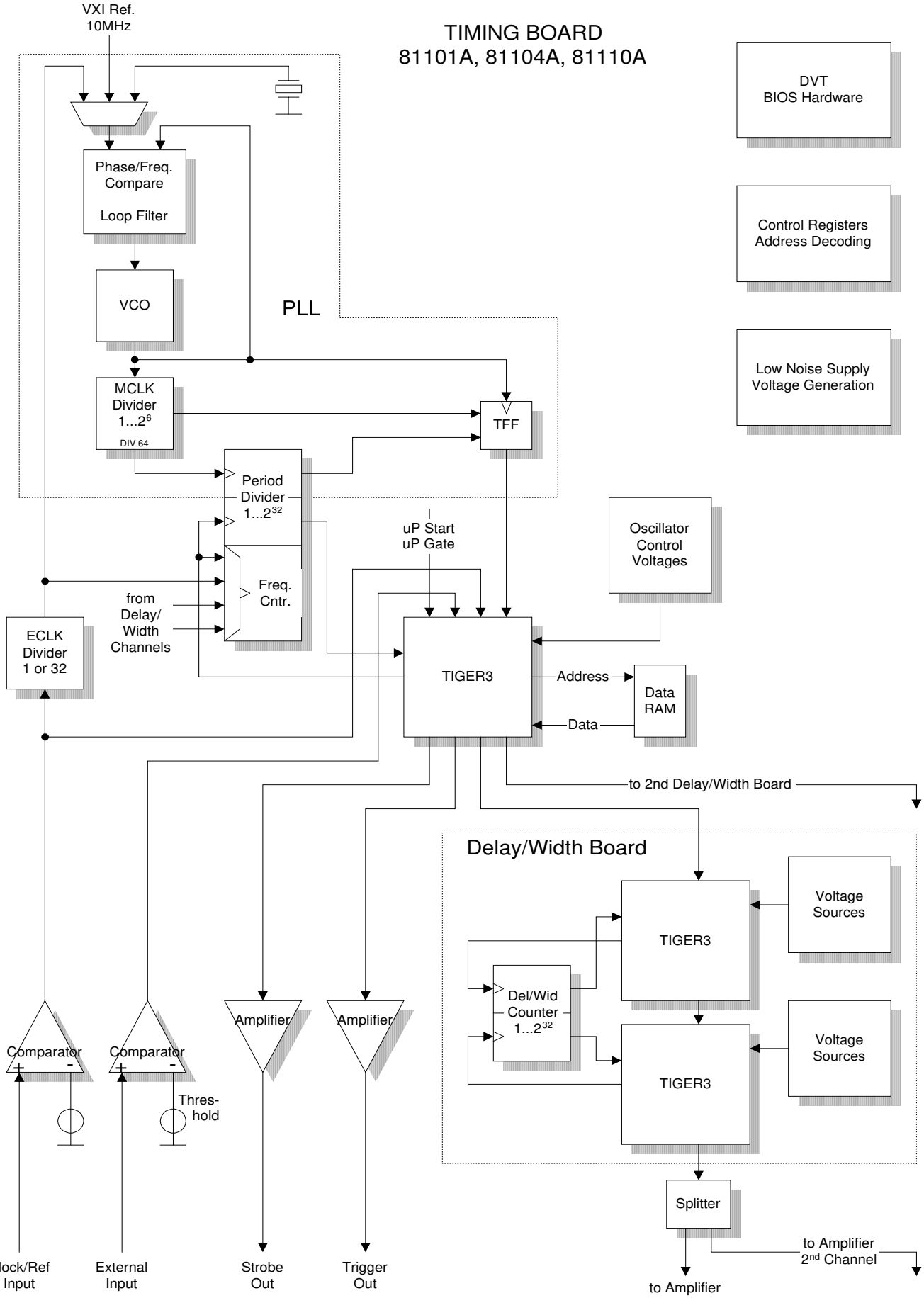
The TIGER oscillators are temperature sensitive, which means they change oscillation frequency with temperature. To compensate that behavior additional DAC's and a temperature diode on the TIGER IC generate a compensation voltage, which is added to the control voltage.

Data RAM (Sheet 7)
The 32kByte fast SRAM is loaded from the CPU via bus driver U103. The address lines always are driven from the TIGER IC. At every read or write access of the CPU to the RAM the burst counter of the TIGER increments automatically. So no additional address driver for the RAM is necessary.

In pattern mode the TIGER reads the data from the RAM through its RAMD inputs. Resistors R107 to R114 limits the highlevel on the datalines to a level that is save for the TIGER LVCMOS inputs.

Oscillator Control Voltages (Sheet 8)
The control voltage sources control the period of the TIGER oscillators. They deliver a voltage in the range of -0.8V to -3.2V. The voltages are arranged as differential pairs to suppress common mode disturbances. 12bit Digital-to-Analog converters U201A/B and operational amplifiers U202…204 set the voltage level.

Because the TIGER oscillator changes its oscillation frequency with temperature the temperature of the TIGERs is sensed with on-chip temperature diode. The diodes are biased with a 100mA constant current. The current source is build with U209. A portion of this temperature voltage is added to the control voltages to compensate the temperature drift. Because the drift differs from part to part the DAC's U201C/D set the appropriate level of compensation.



Block Theory
3 b II

Timing Board 81130A

General

The module generates two parallel clock and/or data streams.
Data streams comprise user memory data and memory based PRBS.
Additionally a trigger output signal is provided.
Tasks of the Timing Board are:
- Generate a period signal
- Generate a sequence of data patterns
- Multiplex these parallel data to a high-speed serial data-stream
- Format the data-stream with delay and pulse-width
- Generate a trigger output signal

Functional units are:

- External Input
- Clock/Reference Input
- MCLK and HRLS Input and Outputs
- Trigger Output
- MCLK Divider
- PLL
- System Clock Divider
- Start/Stop Logic
- Trigger Clock Divider and MUX
- Sequencer Clock Divider
- Sequencer
- Data RAM
- Timing ECL Gate Array
- Low noise supply voltage generation
- DVT BIOS hardware
- Address decoding, control registers and Cal-EEPROM

Block Diagram

Detailed Description ...

DVT BIOS Hardware (Sheets 1 to 4)
The DVT BIOS hardware has the function to interface between the VXI-Bus and the module specific hardware on the Timing Board. This interface is accomplished via a local processor. This board is realized as a plug-in board to the Timing Board. The complete VXI-interface-hardware is located near the J8-connector on the board.

The board has buffers to the VXI-Bus, the module hardware and a FPGA. The FPGA does the arbitration between the local CPU and the VXI-Bus, contains the VXI-Bus configuration registers and other VXI-Bus specific functions.

The BIOS Board consists of the MC68331 CPU, SRAM, Flash-EEPROM, buffers to the Timing Board, interfaces to an emulator, terminal and an EEPROM-load and debugging tool.

Address Decoding, Control Register and Cal-EEPROM
(Sheets 5 and div.)
This functional unit provides all address signals, write- and read-strobes, reset signals and registered control signals, which are necessary to control the Timing/Data Board, and the Amplifier Boards.

The Cal-EEPROM stores the calibration tables of the
- Timing ECL Gate Array,
- ADC circuit,
- Trigger levels,
- Input-threshold and termination voltage DAC's.

At switch-on the Processor reads the calibration tables and keeps it in its local RAM.

Low Noise Supply Voltage Generation(Sheets 24 and div.)
All VXI supply voltages (-12V, -5.2V, -2V, +5V, +12V, +24V) are LC-filtered at the board input (Sheet 2) by 3.3µH inductors and 47µF or 1µF Tantalum capacitors. These filters are especially useful to suppress power-supply noise (in the region of about 100kHz up to 1MHz). Ceramic capacitors are distributed all over the board to suppress high frequency noise.

For noise sensitive devices, especially the oscillators and their controlling circuits, linear regulators generate additional voltages.
These voltages are
- VCC_OSC (+7.8V, U419, Q416),
- VEE_PLL (-8.3V, U631),
- +20VVCO (+20V, U630),
- VP_PLL (+6.3V, U420, Q414),
- VCC_OSC (+10V, U419, Q415),
- VCC_SW (+5V, U420, Q419).

The data SRAM's and parts of the address decoding use +3.5V, generated by U553 and Q550.

External Input (Sheet 24 and 25)
A signal at the external input can start, stop or gate the period generator.

The external input circuit converts the input voltage to an ECL signal. The external input signal enters through connector J304. The input impedance is 50 Ohm.
The high frequency components of the input signal are attenuated and AC coupled to the non-inverting comparator input. The low frequency components are also attenuated, inverted by U351 and coupled to the inverting input of the comparator. U351 also adds the threshold voltage.
Diodes CR359 to 363 prevent the comparator from hazardous voltages.
The threshold voltage is generated and adjusted by the DAC U416 and the operational amplifiers U417

Clock/Reference Input (Sheet 14 and 16)
The Clock/Ref. input can be used as reference clock for the PLL (1, 2, 5 or 10MHz nom.) or as external clock source.

The Clock/Reference input signal is AC coupled to the input of the comparator. There is no DC path. So no threshold generation is needed, the comparator threshold is 0V.
Diodes CR350 and 364 prevent the comparator from hazardous voltages

Phase Locked Loop PLL (Sheets 14, 18 and 19)
The internal PLL consists primarily of a RF oscillator (U101) with a frequency range of 330MHz to 670MHz, a PLL frequency synthesizer chip (U807) and a loop filter.

The oscillator sends its output signal AC-coupled to an ECL-splitter circuit U102, which converts the single ended signal into two differential ECL signals, one for phase-frequency-compare and one to a divider. U104 and surrounding components regulate the dutycycle of the splitter output to 50%.

A flip-flop divides the output of the 20MHZ-reference oscillator Y800 by two. The multiplexer U810 allows selecting from three different reference sources:
- the VXI reference,
- an external reference clock,
- the internal reference.

The selected reference clock is applied to the PLL IC U807. Inside the IC the clock signal is passed through a reference divider. A second divider process the output from the VCO (Splitter) and the two divided signals are phase-frequency-compared, producing an output current. The current/charge is proportional to the phase difference between the compared signals. When the phase difference is zero the output current is also zero.

This signal is filtered with the active integrator circuit U808 and some passive components. A LC low-pass-filter suppresses the unwanted spectral components. U 304 limits the range of the output voltage of the loop filter to about 0V to 12V, a range suitable for tuning the VCO to frequencies between 330MHz and 670MHz.

The external tracking PLL also uses oscillator U101. Phase comparator U800 compares the signal from the external clock input and the clock from the system clock counter. The output signal from the comparator is filtered by U801, U806, U804 and surrounding components. The gain of the filter is variable with the switches U803 and U805.This is necessary for the PLL to work stable with different external clock speeds.
To decide how to set the gain switches the frequency of the external clock input can be measured by the ASIC U127. For high frequencies the clock has to be divided by counter U123.

MCLK Divider (Sheet 14)
For data output frequencies lower than 170kHz the MCLK has to be divided. Counter U107 and flip-flop U108 allow division up to 512 while maintaining a dutycycle of the output signal of 50%. Multiplexer U103 selects if a divided or undivided MCLK will be distributed.

System Clock Divider (Sheet 15)
The System Clock divider has 2 reasons:
First it divides the MCLK so that the tracking PLL is able to synchronize the MCLK frequency onto a external clock signal (See PLL description).
Second it generates the Clock for Start/Stop circuitry.
The divider is build from two cascaded 8bit counters (U112/113) and a following flip-flop (U110), all 3 components are clocked by the MCLK. Again a multiplexer (U111) selects between divided and undivided clock.

Start/Stop Logic (Sheet 20)
The timing system of the 81130A board uses a non-startable MCLK.
This is to increase the accuracy of the timing system, because units with a startable clock system tend to decrease the pulsewidth/period of the first few output-cycles.
So to start the system another signal, called HRLS (High Run Low Stop), enables clock processing at the end of the clock

distribution tree. HRLS is distributed in parallel with the MCLK. The µP or a signal at the external input can start, stop or gate pulse/data generation of the board. Because these signals are asynchronous they have to be synchronized to the board clock. This is done in two steps, first synchronizing to the System Clock (U812/813/815) and then to the MCLK (U817).

MCLK and HRLS Inputs and Outputs
The MCLK and HRLS signals have to be distributed. ECL-splitter circuits U820 and U821 generate 8 copies of these signals. The data generation section is running with one of these signals, but can run with an external HRLS and MCLK signal also. Two other splitter-circuits (U822/823) generate more copies for use in the data generation section of the board.

Trigger Divider and Output (Sheets 22 and 23)
The trigger output generates either a periodical clock signal or a sequence trigger signal.

Counters U406 and U407 divide the MCLK signal to generate the periodical clock signal. The divider ratio can be in the range of 1 to 65536 (16-bit divider). Multiplexer U403 selects between divide ratio 1, 2 or variable or sequence trigger.

The board sequencer generates a sequence trigger signal, which is written into the FIFO U600 (sheet 9). In this trigger mode the trigger counter generates the read clock for the FIFO. After levelshifting and retiming of the data it is coupled to the MUX U403.

The output signal of that MUX drives the trigger amplifier, which is composed of a splitter buffer U412, levelshifting diodes CR400 and CR401 and two differential amplifiers build mainly of transistors Q401 to Q404.

The trigger amplifier has variable output levels. DAC U414 and current sources U422/Q405 and U422/Q406 generate the amplitude current. DAC U414 and U415/Q407/Q408 generate the highlevel voltage.

Sequencer Clock Divider
The sequencer (description see below) has an upper operating frequency limit of 42MHz. So it cannot run with the MCLK signal directly. The sequencer clock counter, build with U116, U117 and U122, is gated by HRLS and divides the MCLK by a minimum ratio of 16. The maximum divide ratio is 65536 (16 bit).

Sequencer
The basic architecture of the cell sequencer is a Moore state machine

Basically the state machine is implemented with memory (SRAM) with the address lines used as inputs. The outputs of the memory are the outputs of the state machine. Some of the outputs are fed back to inputs; they are called state bits and represent the test state. Depending on the test state the state machine can have different reactions to the inputs. Inputs and outputs are clocked into registers, so reactions take place at defined time stamps.

Sequencer Inputs:
- 3 TC outputs of the counter CPLD
- 7 state bits
- µP-event
- external event

Sequencer Outputs:
- 7 control signals for the counters
- 21 load bits for the counters
- 7 state bits
- a µP interrupt bit
- trigger signal

The Counter CPLD comprises three 20bit counter. Each counter

generates a TC signal at a counter value of 100000hex. The TC propagates through another register in the MUX PLD, so that the sequencer receives a TC at 100001hex.
One counter counts the length of address segments, a second counter counts loops, and the third counter is the address counter, which generates the address for the data RAM. The address counter has a special shadow register where it can store the actual count value in case it is loaded. The value of the shadow register can be reloaded into the counter under control of the sequencer.
Because all counters get their load value from the same inputs just one counter can be loaded at a time (except the counters shall be loaded with the same value).
Every counter has 2 control inputs, load-enable and count-enable (LD and CE), that determine whether the counter stops, counts or loads a new value.

Data RAM and FIFO's ((Sheets 9 and 10)
The Data RAM (64k*16, U601/621) contains the user pattern. It is addressed from the Counter CPLD. Because the RAM is just 64k words deep only 16 of the 20 address bits are used. The RAM is upgradable to 256k.

The FIFO's (U605/606/625/626) are the 'rubber band' between the circuits which are running with the Sequencer Clock and the ECL gate array. The 'rubber band' is necessary for delay generation (see below). The ECL gate array gets its clock, called Master Clock, from a cable at the front panel of the module and divides this clock to the same frequency as the Sequencer Clock. This clock is then used as read clock for the FIFO's.
In the dual channel mode the two 9-bit wide FIFO's are read out from different read clocks, so that the two datastreams can have different delays.

ECL Gate Array (Sheets 12 and 13)
The ECL Gate Array (U702/752) has 3 functions:
- Delay generation and data formatting for 2 channels
- Multiplexing of stimulus data
- Demultiplexing of receive data

Delay is built in two steps. The first step is the counted delay. Delay counters are clocked with the Master Clock (MCLK). The counters are preloaded with a delay value and decrement that value by every MCLK. Once the counters reach '0', always the data period value is reloaded. Now the counters periodically generate the data period (see the picture as an example).
The delay steps that can be generated by this way are equal to the Master Clock period (1.515ns ... 3.03ns).

The second step is the so-called Analog Delay. External DAC's (U700/750) generate a voltage that controls the analog delay. The maximum analog delay is larger than the largest Master Clock period (3.03ns). The analog delay allows for a delay resolution of 2ps.

Each ECL gate array has 2 independent delay generators. This allows RZ formatting of the output data (RZ = Return to Zero). NRZ data (Non Return to Zero) just needs one delay generator so that the two outputs of the ECL gate array can have different delays, while in RZ mode both outputs must have the same delays for the positive and the negative edge.

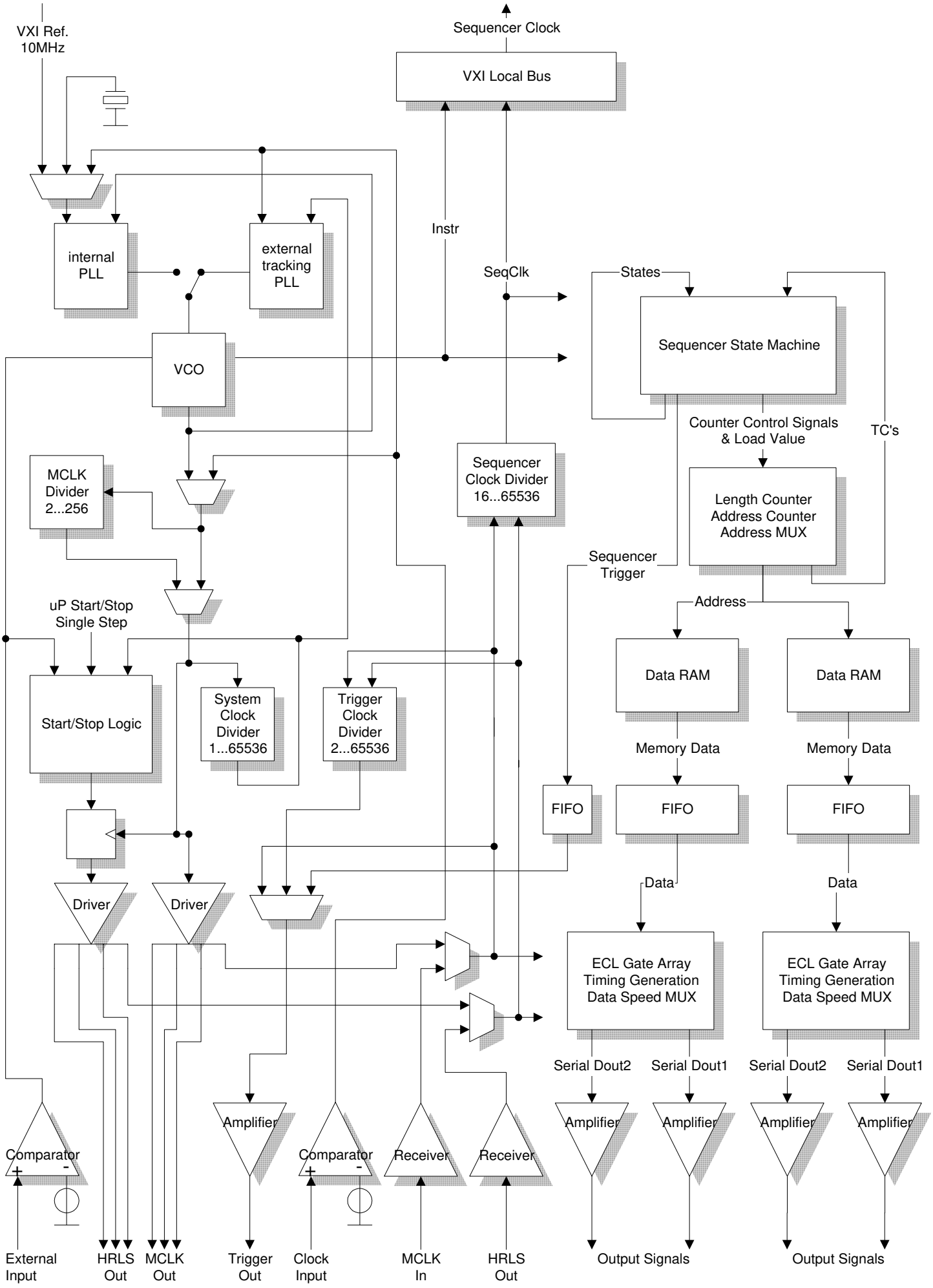
The example shows an output pattern in NRZ mode and in RZ mode. For simplicity the analog delay is set to '0'. The counted delay1 is 11 MCLK cycles, delay2 is 14 MCLK cycles. Data period is 1/8 of MCLK period. Output pattern is 1 1 0 . . .

The next function of the ECL gate array is data multiplexing. The gate array reads data from the FIFO's 16bit wide. These 16 bits are then parallel loaded into two 8bit shift registers. Then the

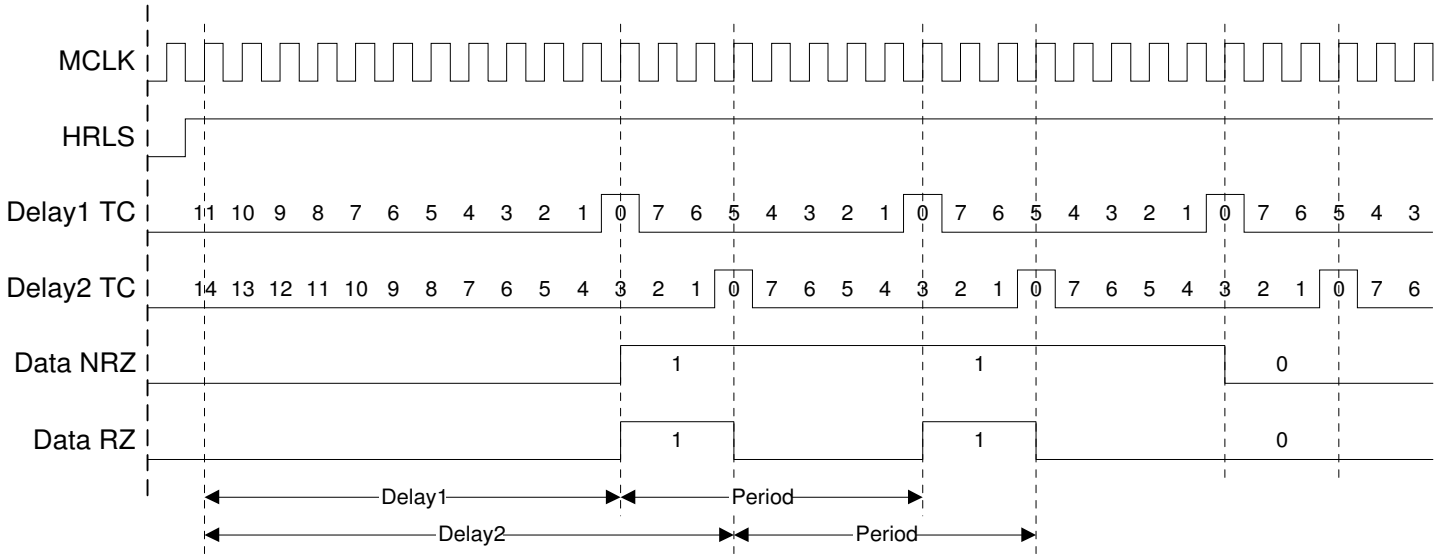
data is shifted out serially. The MUX-factor is the ratio of output data speed to FIFO data speed, e.g. a MUX-factor of 4 means that in every read cycle 4 data bits are put out. The output data speed is then 4 times the FIFO data speed. At a MUX factor of 16 the output bits of the second 8bit shift register are shifted into the first shift register so that 16 bits can be shifted out before a new read has to occur.

The timing diagram shows two cases:
a MUX factor of 8 with both ECL gate array outputs active and
a MUX factor of 16 with one output active.

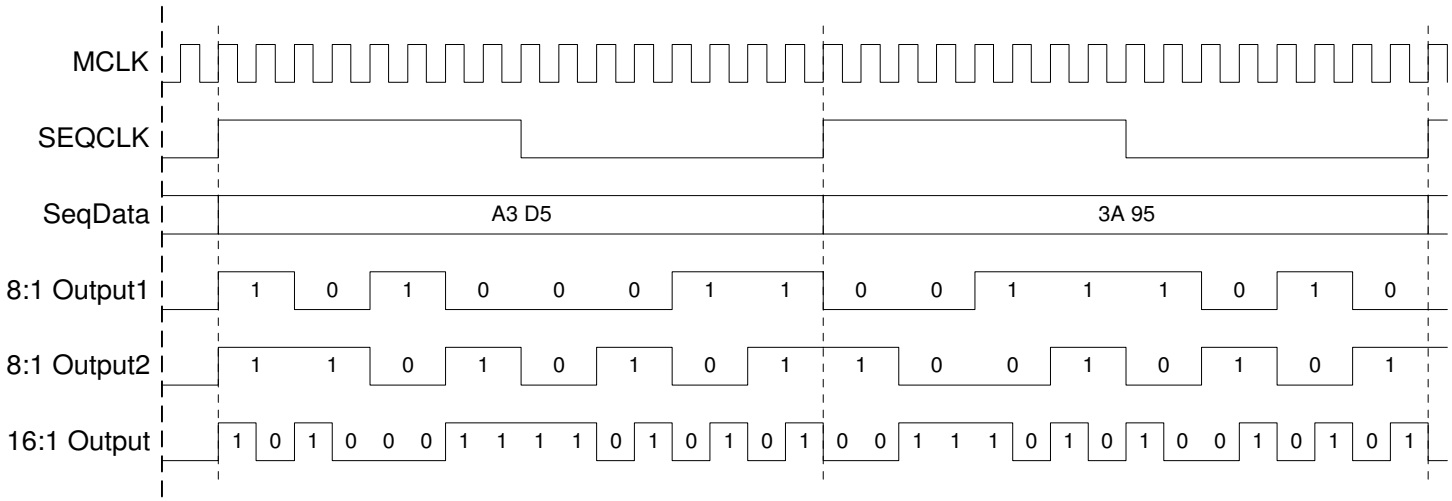
81130A Timing Board
BLOCK DIAGRAM



Output pattern in NRZ and RZ mode



MUX factor 8 with both outputs active
MUX factor 16 with one output active



3 c

Block Theory, Output Channels

Block Theory
3 c I

Delay/Width Board

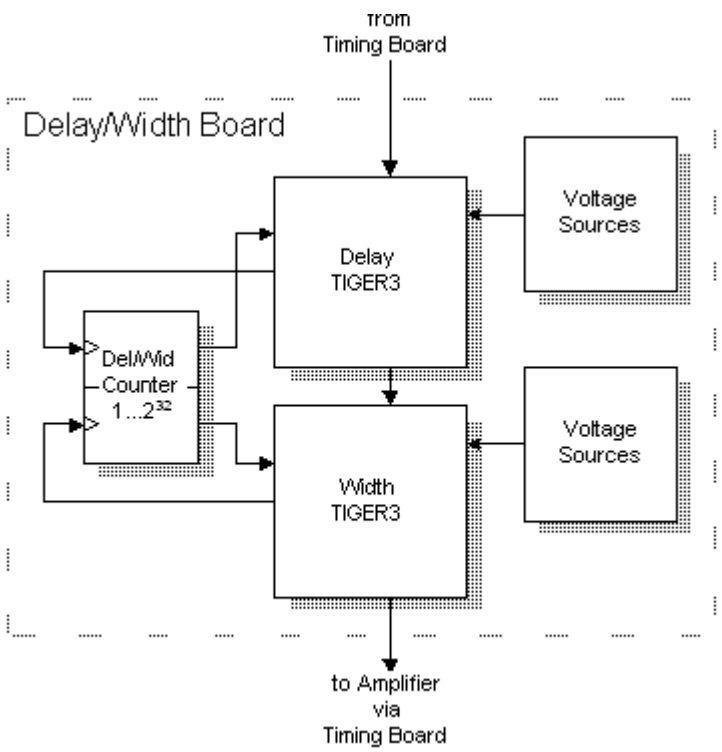
General

The Delay/Width Board receives a differential period signal from the Timing Board. The Delay/Width Board delays every input pulse and sets the pulse width. After that processing a differential signal is routed back to the Timing Board.

Functional units are:

- Delay TIGER
- Width TIGER
- Control Voltage Sources
- Counter FPGA
- Cal-EEPROM

Block Diagram



Detailed Description ...

Delay TIGER (Sheets 1)

The Delay TIGER receives the signal TRIGDelTG from the Period TIGER. Depending on the selected data format that pulse is either a RZ signal with 50% dutycycle or a NRZ signal (in Data NRZ mode only). It is a CML logic signal with a highlevel of 0V and a swing of about 300mV.

In one of the RZ modes the TIGER triggers on the rising edge of the period signal and generates an output pulse with a certain pulse width. The width of that signal represents the delay time; a short width means a short delay and a larger width gives a larger delay. This signal, a CML level signal, is named TRIGWidTG.

In NRZ mode the Delay TIGER triggers on both edges of its input signal and delays both edges with the same value, so the output signal has the same width as the input signal.

A startable oscillator and a counter, which counts the number of oscillator periods, generate the delay. The period of the oscillator and the number of pulses, which are generated per trigger signal, are programmable, giving a programmable delay.

Width TIGER (Sheets 1)
The Width TIGER triggers on the TRIGWidTG signal from the Delay TIGER and generates the signal WidTGOUT, which is routed back to the Timing Board.

In RZ pulse or pattern mode the Width TIGER triggers on the negative slope of the TRIGWidTG signal and generates a signal with the chosen pulse width. In NRZ mode the TIGER triggers on both slopes and maintains the pulse width of the input signal and in double pulse mode it triggers on both slopes and generates two pulses with the same pulse width.

Control Voltage Sources (Sheet 2 and 3)
The control voltage sources control the period of the TIGER oscillators. They deliver a voltage in the range of -0.8V to -3.2V. The voltages are arranged as differential pairs to suppress common mode disturbances. 12bit Digital-to-Analog converters U201A/B and U301A/B, operational amplifiers U202...204 and U302...304 set the voltage level.

Because the TIGER oscillator changes its oscillation frequency with temperature the temperature of the TIGERs is sensed with on-chip temperature diode. The diodes are biased with a 100mA constant current. The current source is build with U209/U309. A portion of this temperature voltage is added to the control voltages to compensate the temperature drift. Because the drift differs from part to part the DAC's U201C/D and U301C/D set the appropriate level of compensation.

Counter FPGA (Sheet 1)
The counter FPGA is the companion to the TIGER IC because it expands the delay and width counter of the TIGERs. The TIGERs have 7bit counters only, which allow a delay or width of just up to 200ns. Larger times are obtained by cascading the TIGER counters with the 32bit counters of the counter FPGA. The counters get the signals DELTGDIVCLK and WIDTGDIVCLK from the TIGERS and send back the signals TCDELCNTR and TCWIDCNTR.

Cal EEPROM (Sheet 1)
The Cal-EEPROM keeps the tables with the calibration data of the Delay- and the Width-TIGER. Calibration data comprises the period/DAC pairs and the drift values of the oscillators.

At switch-on the Processor of the Timing Board reads the calibration tables and keeps it in its local RAM.

Block Theory
3 c II

10 V Output Amplifier Board

General

The 10 V Output Amplifier Board receives a differential signal from the Delay/Width Board. The 10 V Output Amplifier Board generates the variable transitions and sets the amplitude and offset. After that processing a output signal is available.

Functional units are:

- SLAVE IC
- Linear Amplifier
- Offset Control
- Output Mode Switches
- Power Monitors
- Board Detection and Interrupt Request Register

Block Diagram

Detailed Description ...

Slave IC
The SLAVE IC is an integrated circuit which provides a preamplifier with the opportunity to adjust the transition times and amplitude of the output signal.

Linear Amplifier
The linear amplifier is a current feedback push pull amplifier with cascode output stages. It multiplies the output signal of the SLAVE IC with a factor of 4.5 to achive the requested output amplitude. For special purposes like calibration it is possible to disable one side of the push pull output stage.
Since there are different signal pathes for low and high frequency signals it is important for undisturbed pulse shapes to adjust the gain of the low frequency path to match the high frequency path.
The dependence of the output stage transistors bias point on the signal amplitude is eliminated by a special offset current source which is controlled by the BIAS_REF parameters.
Because it may be necessary to adjust min. transition times and overshoot there are capacitor diodes in the current feedback path.

Offset Control
An additional bipolar current source is used to adjust the output voltage window. Due to inductive decoupling it has no influence on the high frequency behavior of the amplifier.

Output Mode Switches
The output switch unit provides different modes for output impedance and channel addition.
output disabled, signal is led to the neighbour channel

```
 and internal termination
output enabled
normal / complement
no channel addition
         output impedance 50 Ohm
         output impedance 1 KOhm
channel addition
         output impedance 50 Ohm
         output impedance 1 KOhm
```

Power Monitors

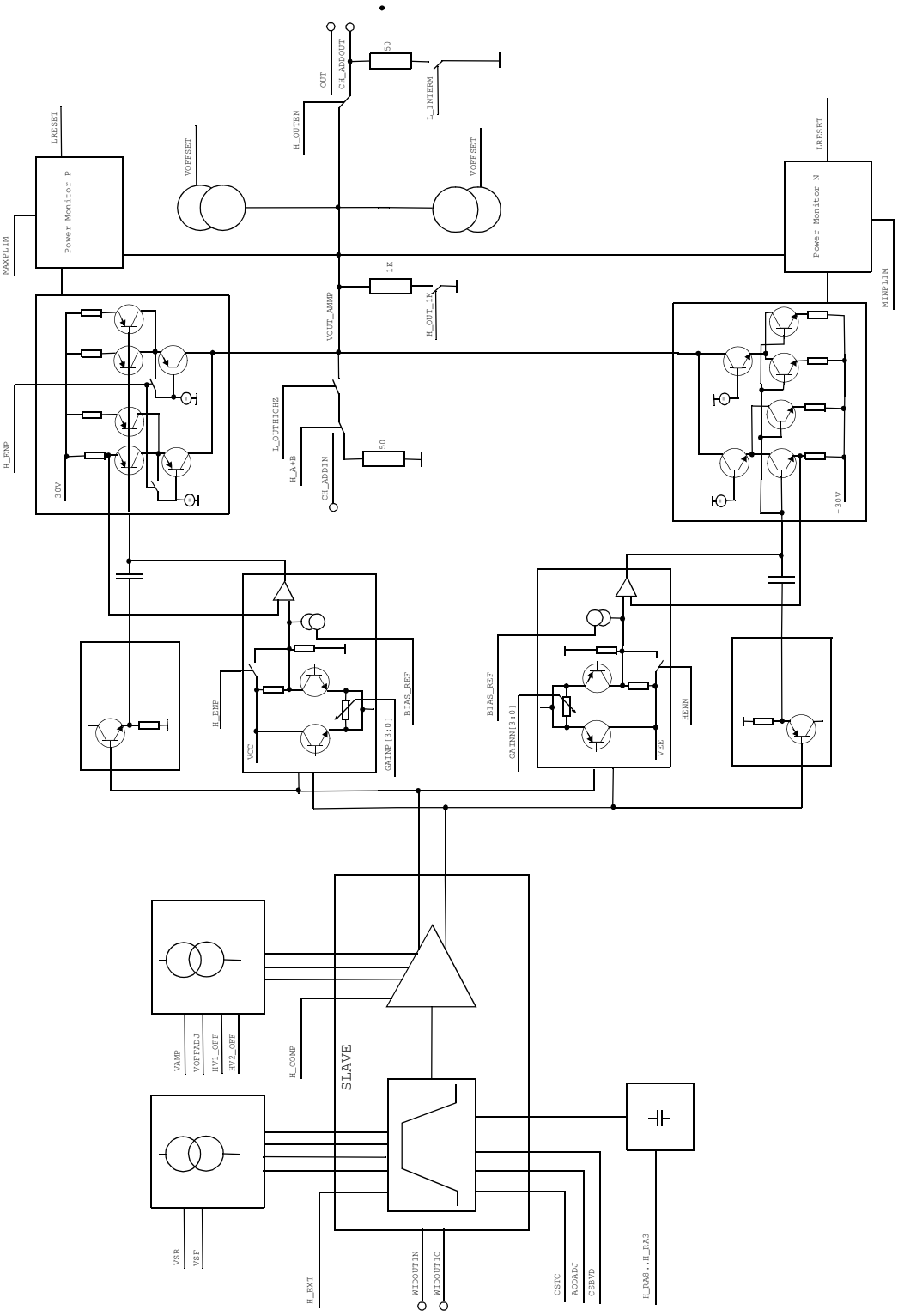
The power monitors watch the currents and voltages of the output stage. If the power dissipation of the output transistors exceeds the limits a interrupt is initiated by setting
LRESET = Low (edge triggered interrupt).
In addition all frontend registers switch to reset state. The power limits are adjustable by MAXPLIM and MINPLIM voltages.
The output voltage is limited by hard limits (-20.5 ..+20.5 V) and additional programmable soft limits, which are programmed in relation to output amplitude and offset.

Board Detection and Interrupt Request Register

Any read access to the frontend board returns the (7 bit) board ID 0x0A and the state of the interrupt request register. Interrupts are initiated by falling edges of L_INT (Bit 5 Latch 1). Setting L_INT to "0" disables interrupts. In normal operation modes the interrupt request register has to be set to "1".
An interrupt occurence is indicated by value "0".

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IntReq	ID6	ID5	ID4	ID3	ID2	ID1	ID0

3.0 10V Output Amplifier Block Diagram



Block Theory
3 c III

3.8 V Output Amplifier Board

General

The 3.8 V Output Amplifier Board receives a differential signal from the Delay/Width Board. The 3.8 V Output Amplifier Board generates differential output signals and sets the amplitude and offset.
After that processing a differential output signal is available.

Functional units are:

- Levelshifter
- Pulse Shaper (differential amplifier)
- Output stage (differential amplifier)
- Transition Timer Converter
- Output Mode Switches
- Voltage Monitors
- Board Detection and Interrupt Request Register

Block Diagram

Detailed Description ...

Levelshift
he ECL input levels are shifted to values between -3.3V and -4.2V.

Pulse Shaping
The first amplifier stage is to provide a proper shaped signal for the output stage. Threfore it is neccesary to adjust the common emitter current in dependence on amplitude.

Output Stage
The output stage is composed of two differential amplifiers.
The output currents of these amplifiers are added and internal terminated with 50 W into termination voltage VH. This termination voltage VH determines the high level of the output signal.
The amplitude depends on the common emitter current (IAmp) of the output amplifiers.

Transition Time Converter and Output Mode Switches
The output switch unit provides different modes for output signals and transition times..

output disabled
output enabled
single ended
differential
fast transition times < 600 ps / 900 ps
slow transition times about 1.6ns

Voltage Monitors

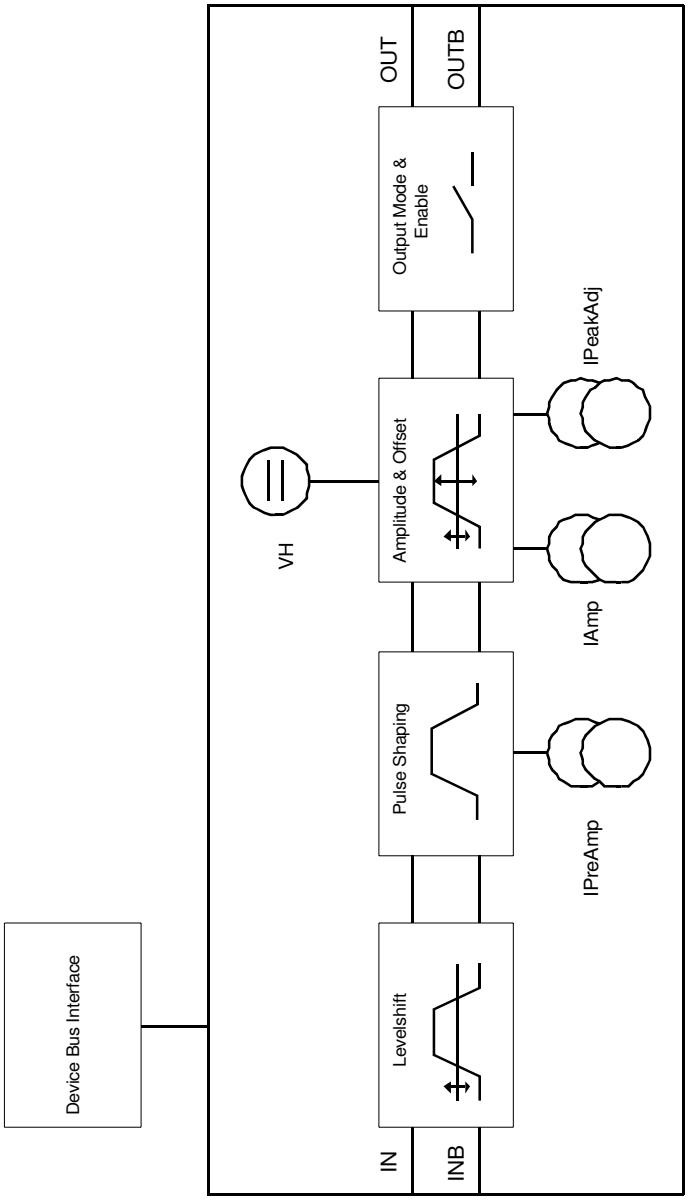
If the output voltage exceeds the limits an interrupt is initiated by setting LRESET = Low (edge triggered interrupt). In addition all frontend registers switch to reset state.
The output voltage is limited to 6.5V and −3.5V.

Board Detection and Interrupt Request Register

Any read access to the frontend board returns the (7 bit) board ID 0x0B and the state of the interrupt request register. Interrupts are initiated by falling edges of L_INT (Bit 5 Latch 1). Setting L_INT to "0" disables interrupts. In normal operation modes the interrupt request register has to be set to "1".
An interrupt occurence is indicated by value "0".

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IntReq	ID6	ID5	ID4	ID3	ID2	ID1	ID0

4.0 3.8V Output Amplifier Block Diagram



Block Theory
3 c IV

2.5 V Output Amplifier Board

General

The 2.5 V Output Amplifier Board receives a differential ECL signal from the Delay/Width Board and converts it to a differential output signal with variable levels.

In principle the amplifier is a differential stage driven by a preamplifier. A current source delivers the amplitude current IAMP to the differential stage. This current is variable by means of a DAC.
Resistors connected from the output lines to the highlevel voltage source VHIL determine the output impedance, which is 50W.
A DAC sets the level of the highlevel voltage source.

Output highlevel HIL and lowlevel LOL can be calculated by:

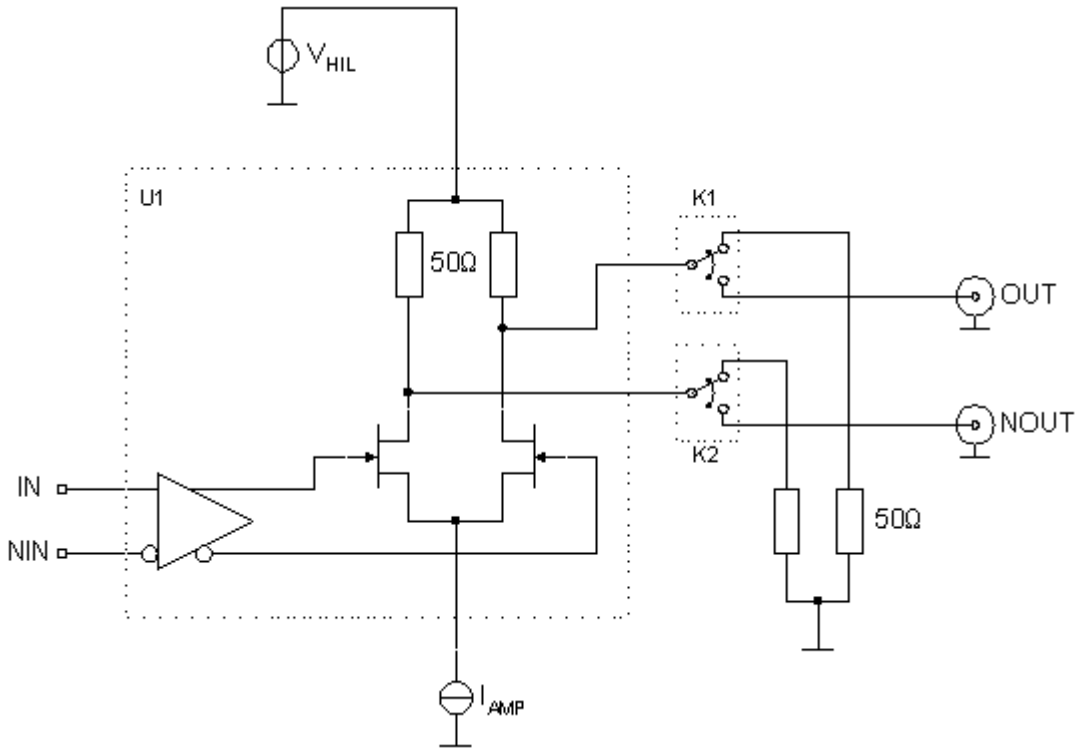
Highlevel:
HIL = (VHIL * RL +VTERM * ROUT) / (RL + ROUT)

Lowlevel:
LOL = (VHIL * RL + VTERM * ROUT - IAMP * ROUT * RL) / (RL +ROUT)

A EEPROM on the amplifier board holds the calibration data of the voltage and current source.

Relays allow switching the outputs off. In OFF mode the signal is switched to an on-board 50 Ohm resistor.

Block Diagram



4

Exchanging the Boards

This section contains at the moment the procedure for exchanging the following:

Power Supply	0957-3741
Mother/CPU Board	81101-69501 81104-69501 81110-69501 81130-69501
Battery on CPU Bd.	1420-0557
Timing Board	81101-69513 81104-69513 81110-69513 81130-69503
Output Channel AY	81101-69515 81105-69515 81111-69515 81112-69507
Frontend Board	81131-69505 81132-69509

Warning

SHOCK HAZARD

Only service-trained personnel who are aware of the hazards involved should remove, configure and install the instrument. Before you perform the board exchange, disconnect the AC power and field wiring from the mainframe after the switch OFF.

Caution

STATIC ELECTRICITY may damage
STATIC SENSITIVE DEVICES
Handle the boards only at 'Static Safe' work stations.

Static electricity is a major cause of component failure. To prevent damage to the electrical components in the mainframe and the plug-in boards, observe anti-static techniques whenever handling a board!

Before replacing any board, make sure that the unit is calibrated properly and check the Power Supply.

If there are error messages concerning different boards, begin with the first error and try to fix it with the tips given in 'Error Description' of Chapter 2, Troubleshooting.

Installing is the reverse of the procedure given for removing.

Terms used and what they mean ...

Some of the terms used in this chapter can be misleading in the wrong context. For example, the word *replacement* can refer to the act of changing a faulty subassembly, *or* replacing a working one after it has been removed from the instrument.

Here are some of the terms used in this chapter, and what we mean by them:

Fit To attach a subassembly to the instrument, usually taken to mean a subassembly that was not there before. (see *Retrofit*)

Install To place any subassembly to/into the instrument.

Refit To put a subassembly back into the instrument, after removal for any reason.

Replace To remove a faulty subassembly, and fit a new (working) one.

Remove To take any subassembly (working or not) away from/out of the instrument.

Retrofit To attach a subassembly to the instrument, in this case, to provide function(s) that were not fitted to the instruemnt when it was purchased.

The Tools you need ...

The following tools enable all fixings to be removed and replaced:

* Medium cruciform screwdriver (fan assy)
* Torx screwdriver, T-10 (PC boards, case)
* Torx screwdriver, T-25 (case handles)
* 6mm diameter nutdriver (BIOS Bd.)
* 7mm diameter nutdriver (HP-IB cable)
* 12mm diameter nutdriver (RPG Head unit)
* 14mm diameter nutdriver (BNC connectors)

Prepare the unit for repair ...

- Write down the *original serial number* of the mainframe.
  You need this info if the Mother-/CPU Bd. must be replaced to re-enter it to the unit after repair,
  so the mainframe serial number stays with the customer!

  The serial number label you may find on the rear of the unit.

  To see the serial number of the mainframe on the display

  do the following:

  Press HELP, [SERIAL #]

  The 81100 display lists the instrument’s products and serial number.
  The display on your instrument should look similar to this:

  FRAME: 81110A 165 MHz

  Serial No: DE38700135

  OUTPUTS

  Ch1-Bd.: 81111A

  Ch2-Bd.: 81111A

(The 81101A screen do not show the OUTPUTS)

The serial number given for the **FRAME** applies to the Mainframe, the Power Supply, the Microprocessor Board, and the Timing Board. The number(s) available of the Output Channel(s) applies to the installed numbers of outputs and Model Number. The serial number(s) are shown on the rear.

- Save your settings.
  It is helpful to make data backups of your daily used settings.
  If not already done, do it now to an extra memory card.

- Switch OFF the power switch on the mainframe.

- Disconnect the AC power wire from the mainframe.

- Disconnect the BNC/SMA cable(s) connected to the instrument.

Note

- **Some of the subassemblies need to be removed in a specific order, and the instructions have been written with this in mind.**

- **The instructions can also be used in reverse to provide the steps needed for retrofiting subassemblies.**

Opening the unit ...

- Remove the Rubber Bumpers (if not already removed because unit is used in a rack)

- Remove the carrying handles from each side of the case removing 2 screws each. Both sides have the same fixings.

- Remove the cover top from the case removing the 9 screws on the rear securing the cover top to the case.

- Remove the cover bottom from the case removing the 6 screws on the rear securing the cover bottom to the case.

Open unit: e.g. 81110A with 2 x 81111A

What to do with the Boards/Assy ...

- Each exchange board/assy is shipped with a
  part number / serial number label.

  This information is needed if the defective board/assy is coming back to the factory for repair.

Note

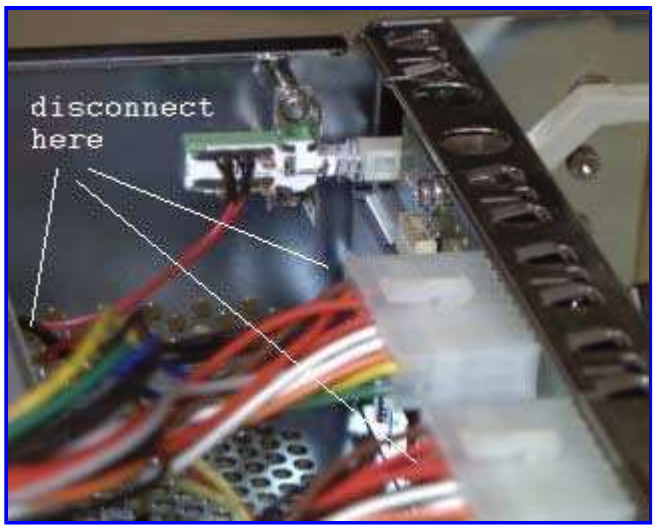
- Before disconnecting/removing any cable, mark the cables (and their connectors) so they correspond again at time of reassembling.

Replacing Boards/Assies

- Replacing Power Supply Module

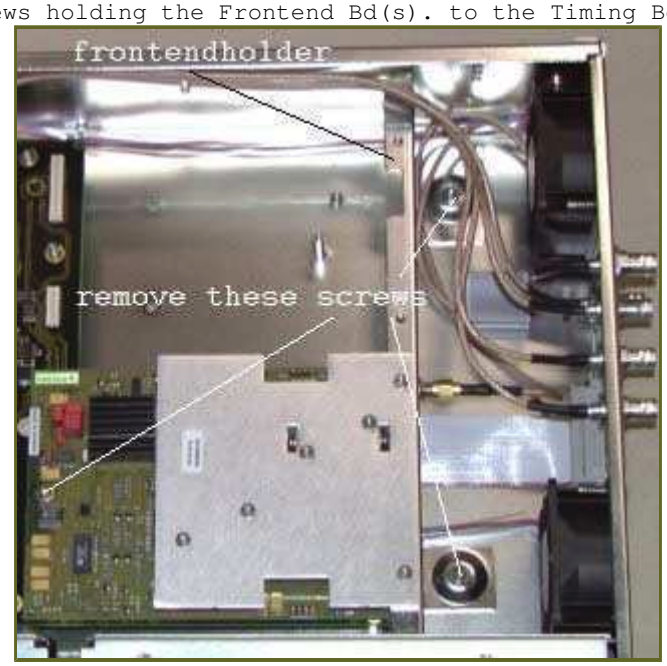
---

* Remove the four screws holding the Power Supply Module to the side of the case
* Remove the three power supply cables from the Mother-/CPU Bd and power switch



* Cut the 'Tierap' holding the thermal-resistor to the cable

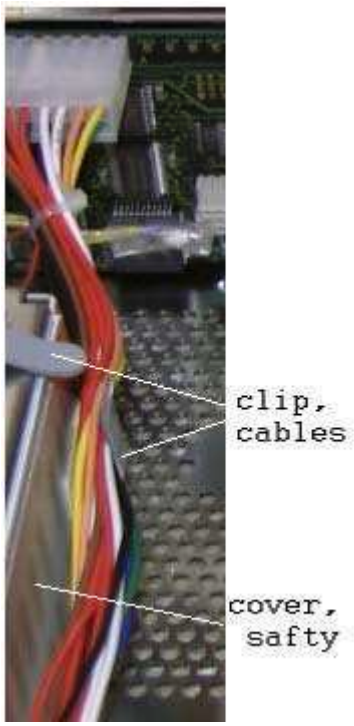
* Remove the front assy
* Remove the screws of the frontendholder (from the top side)
* Remove the screws holding the Frontend Bd(s). to the Timing Bd.



81101A with rear panel output

* Carefully remove the Frontend Bd(s). from the Timing Bd.
  and move it a little to aside
* Move the Power Supply Module in direction of the frontpanel
* Remove the Power Supply Module out of the case
* Put the new Power Supply Module into the case, press it in
  direction to the rear panel and fasten the four screws!

At implementing the Power Supply Module exch. p/n 0957-2779
* first fasten to the module frame the cover safety
p/n 81110-04102 using a double sided adhesive tape
* and the two clip, cable p/n 1400-1625



- *Replacing the Output Channel Assy* 81101A, 81105A,
---------- 81111A/'12A

The serial number of the Output Channel Assy doesn't need to be entered anywhere.

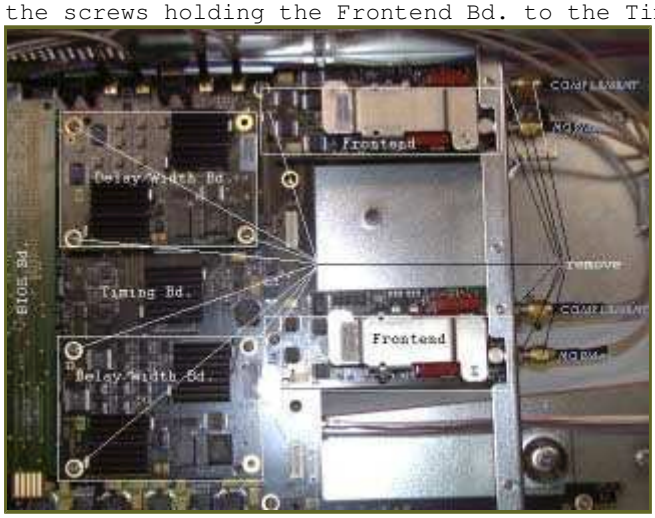
Replacing Delay-Width Board
Replace Delay-Width Board of the channel displayed in the error message, if only some of the following components fail:
Delay TIGER, Width TIGER, VCO >= 2

A Delay-Width Board must be replaced together with its corresponding Frontend Board.

Replacing Frontend Board
Replace Frontend Board of the channel displayed in the error message, if only the following tests fail:
Low/High Level

A Frontend Board must be replaced together with its corresponding Delay-Width Board.

* Remove the SMA-cables from the Frontend Bd.
* Remove the nut fixing the Frontend Bd. to the holder
* Remove the screws holding the Frontend Bd. to the holder
* Remove the screws holding the Frontend Bd. to the Timing Bd.



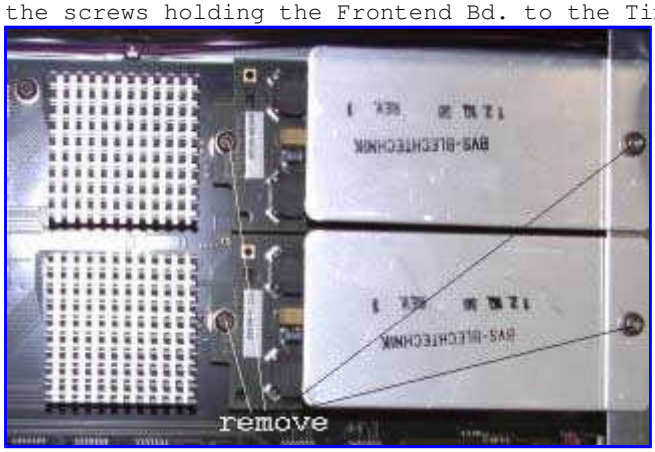
81110A with 2 x 81112A

* Carefully remove the Frontend Bd. from the connectors of the Timing Bd.
* Remove the srews holding the Delay/Width Bd. to the Timing Bd.
* Carefully remove the Delay/Width Bd. from the connectors of the Timing Bd.

- *Replacing the Frontend Board* 81131A, 81132A,

Replace Frontend Board of the channel displayed in the error message, if only the following tests fail:
Low/High Level

* Remove the cables from the Frontend Bd.
* Remove the nut fixing the Frontend Bd. to the holder
* Remove the screws holding the Frontend Bd. to the Timing Bd.



* Take care to the thermal inface between the heatsink sheet, metal and the heatsink of the Frontend Bd.
* Carefully remove the Frontend Bd. from the connectors of the Timing Bd.

- *Replacing Timing Board*

Replace Timing Board together with the BIOS Board, if only some of the following components fail:
Clock Input comparator, External Input comparator, PLL, Period divider, Period TIGER IC, Pattern RAM, Strobe Out, Trigger Out, VCO 0 or 1

* Follow the procedure to remove the Output Channel Assy
* If the unit is a two-channel instrument mark the Frontend Bd's. and their corresponding Delay/Width Bd's!
  ! Do not mix the Frontend Bd's. !
  ! and their corresponding Delay/Width Bd's !
* Remove the frontendholder
* Remove the three screws fastening the BIOS Bd. to the Timing Bd.
  Remove the BIOS Bd.
  Remove also the three spacers the BIOS Bd. was fastened to

* Remove the screws holding the Timing Bd. to the case
  Do not forget the one screw at the frontendholder!

* Mark the SMA-cables connected to the Timing Bd.!
* Remove the SMA-cables from the connectors
* Carefully remove the Timing Bd. out of the interface connectors of the Mother Bd.

- Replacing Mother-/CPU Board

Replace Mother-/CPU Board, if only some of the following components fail:
uProcessor, Motherboard, Interface,

* Follow the procedure to remove the Output Channel Assy and the Timing Bd.
* Remove the three cables of the Power Supply Module
* Remove the HP-IB cable and the cables connecting the fans

* Remove the screws holding the Mother-/CPU Bd. to the frontpanel subassy
* Carefully remove the Mother-/CPU Bd. from the 'filter connector'

After replacing the Mother-/CPU Board the mainframe serial number must be re-entered to the unit.

This can ONLY be done using a controller!

Note

!

:DIAG:OPTION "<serial_number>"

Sets the instruments serial number.
"<serial_number>" is an ASCII string with a length up to 16.
for example: "DE38700135"

!

- Replacing the battery on the Mother-/CPU Board

---

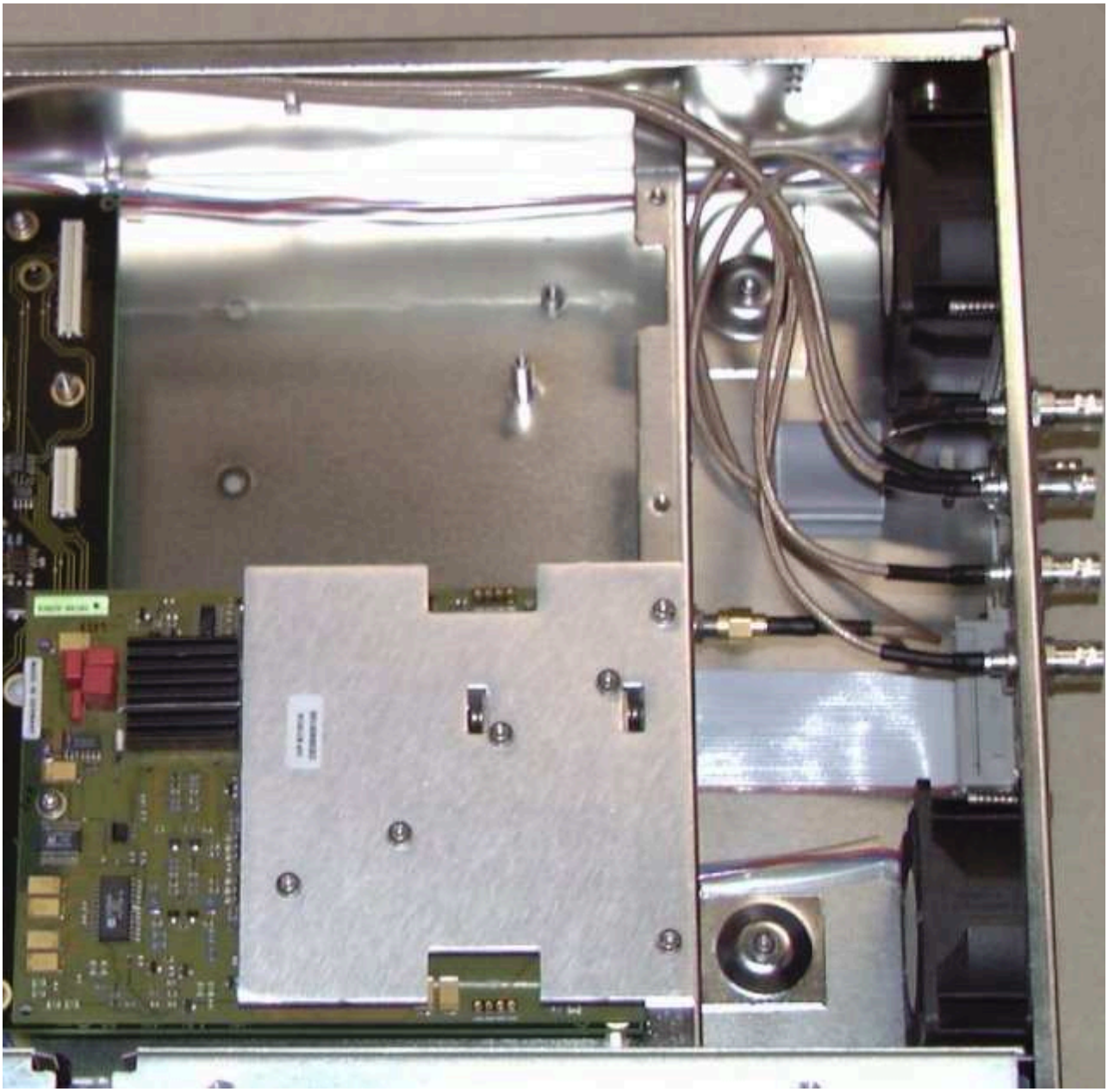
* Remove the Front Frame Assy (two screws on each frame side)
* Remove the metal plate holding the battery onto the Mother-/CPU Board
* Replace the battery

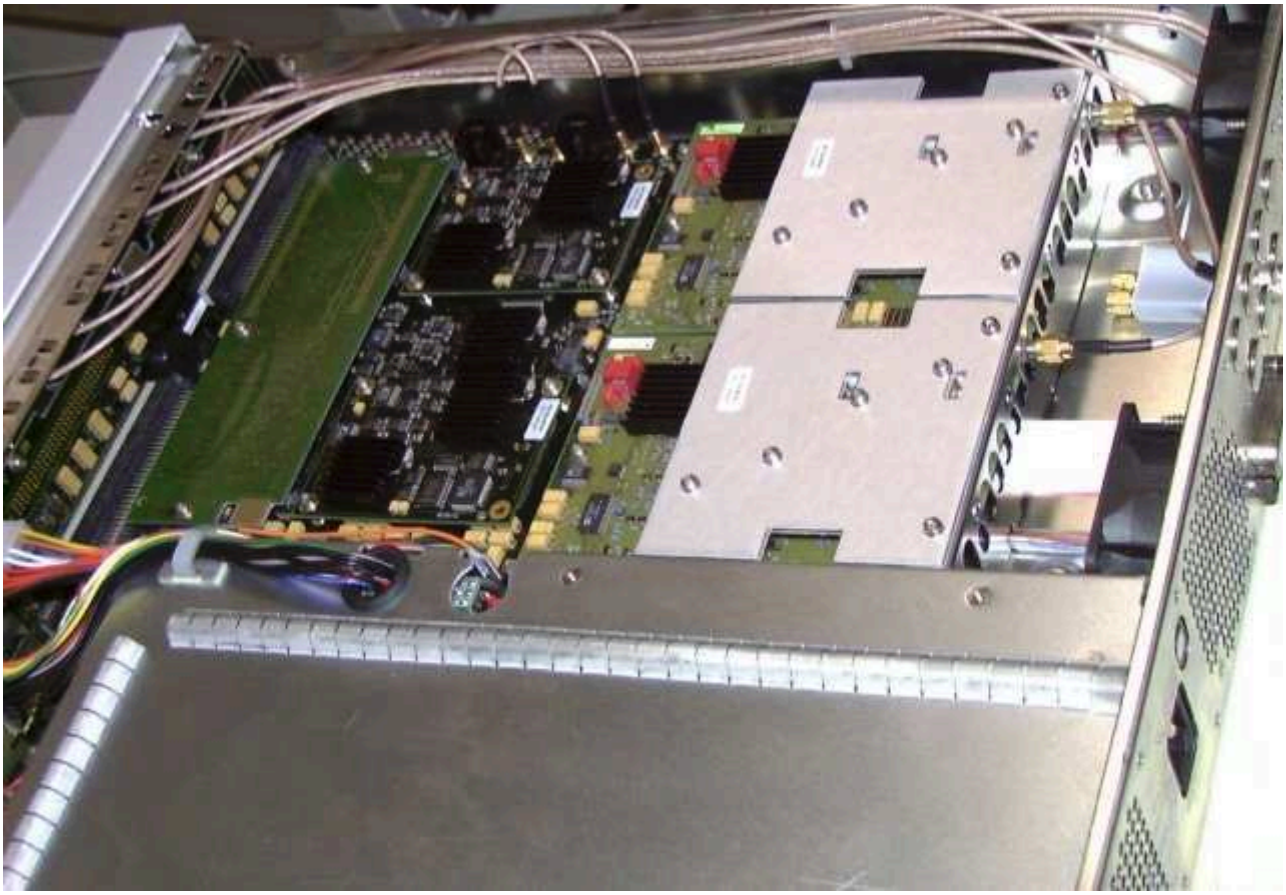
Note

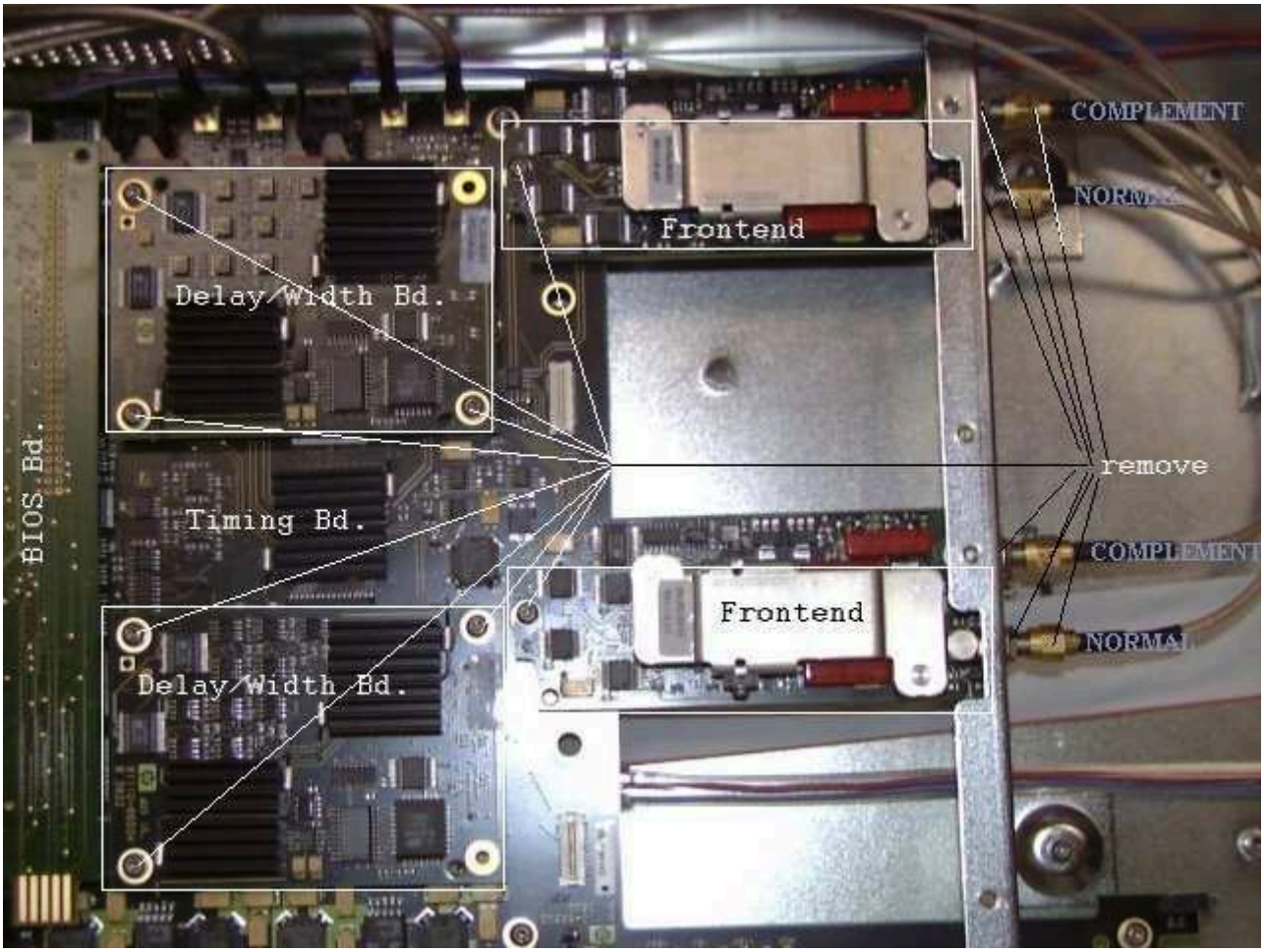
- Please send back the defective board/assy with a ***detailed failure description***!

Installing the Board/Assy ...

- Installing is the reverse of the procedure given for removing.






COMPLEMENT
NORMAL
Frontend
Delay/Width Bd.
BIOS Bd.
remove
Timing Bd.
COMPLEMENT
Frontend
NORMAL
Delay/Width Bd.

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71034 Boeblingen
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Agilent Technologies
Innovating the HP Way

May 18, 2000

After installing a new Bd. (p/n 811xx-66513/-69513 or 811xx-66515/-69515 or 81112-69507)
in an older unit, the following error may accure at power up selftest :
modules test fails
and error queue is: HW 1/CAL DATA CORRUPTED
It is the new BIOS SW in an old unit!

Please do the following:
* place the unit in an safe and calm area!
* switch unit ON
* press the [Help] key two times (>> clear the error queue)
* WAIT 30 min for warm up!

* press [More]
- 'press' [Config]
- on the screen select with the cursor key down
Perform: Selftest
(do not start the selftest!)
- press one key after the other to start temperature cal

.4907031143304

the display shows:
" Calibrate VCO drift ..... please wait "
wait 30 min until ready!

- if no fail
- press one key after the other to end temperature cal

.4907031142912

the display shows some seconds:
" Store Calibration data ..... please wait "
the display shows:
" BURN CALIBRATION DATA PASSED "

* switch unit OFF and ON again
NO ERROR should be visible!

Boeblingen **V**erification **S**olutions Operation
Agilent Technologies Deutschland GmbH
Germany
bvs-pdga_support@agilent.com
http://www.agilent.com/find/dvt

5

Assembly-level Parts List &

Mechanical Parts Drawing

This section contains at the moment the assembly-level parts lists of the following models:

81101A
81104A
with 81105A
81110A
with 81111A / 81112A
81130A
with 81131A / 81132A

Replaceable Assemblies

List of Exchange Assemblies

Model	Description	original p/n	EXCHANGE p/n
	81101A		
	BD AY MOTHER/CPU	81101-66501	81101-69501
	BD AY TIMING	81101-66513	81101-69513
	AY CHANNEL 50 MHZ *	81101-66515	81101-69515
	81104A		
	BD AY MOTHER/CPU	81104-66501	81104-69501
	BD AY TIMING	81104-66513	81104-69513
81105A	AY CHANNEL 80 MHZ *	81105-66515	81105-69515
	81110A		
	BD AY MOTHER/CPU	81110-66501	81110-69501
	BD AY TIMING	81110-66513	81110-69513
81111A	AY CHANNEL 165 MHZ *	81111-66515	81111-69515
81112A	AY CH 3.8V, 330 MHZ *	81112-66507	81112-69507
	81130A		
	BD AY MOTHER/CPU	81130-66501	81130-69501
	BD AY TIMING	81130-66503	81130-69503
81131A	BD AY 3.8V, 400 MHZ	81131-66505	81131-69505
81132A	BD AY 2.5V, 660 MHZ	81132-66509	81132-69509
	Agilent 81100		
	POWER SUPPLY, 120W	0950-3741	0957-3741
	MONITOR-CRT	2090-0293	2097-0293

* The AY CHANNEL (Frontend AND Delay/Width Bd.) have to be replaced together!
If you replace only one board or mix them up,
the unit may not work correct/work out of specification!

To replace the boards special information is needed!
Please see the Information Sheet you get with the Exch. Board!

Please send back the defective part with a

detailed failure description!

Therefore, copy the page at the end of this chapter, fill in the requested information and send it back together with the defective part.

To find exchange information:
- Refer to the procedure in this Guide to replace the boards. (Chapter 4, Exchanging the Boards)
- Refer to the procedure in this Guide to run the self test (Chapter 3, Troubleshooting - Self Test...)

List of Non Exchange Assemblies

Item	Part Number	Description
Agilent 81100		
SW1	0960-0865	RPG MODULE
*MP172, MP173	1400-1625	CLIP, CABLE *
	1420-0557	BATTERY 3V
MP3	81110-04101	COVER TOP
* MP312	81110-04102	COVER SAFETY *
MP5	81110-24510	CONNECTOR CASE
MP6,MP7	81110-24701	SPACER FRONTEND
MP14	81110-44301	LABEL CONFIG
MP15	81110-44302	LABEL CE/CSA
MP231	81110-46001	BUMPER FRONT
MP232	81110-46002	BUMPER REAR
MP309	81110-47401	CURSOR KNOB RPG
MP16	81110-47402	KEY CAP LINE SW
MP1	81110-60101	CHASSIS MAIN
MP301	81110-60201	FRONT PANEL ASSY
MP4	81110-61210	BRACKED FRONTEND
W3	81110-61601	CABLE AY PWR SW
W1	81110-61602	CABLE AY HP-IB
W4	81110-61603	CABLE AY RIB40
W2	81110-61604	CABLE AY DISPL
A1	81110-66502	BD AY, RPG
W5,W6	81110-68501	FAN ASSY
	81100-68700	FRONT PANEL AY 811xxA do not order
	81100-68710	BASE CHASSIS AY 811xxA do not order

81101A, '04A, '05A, '10A , '11A, '12A		
W10,W11,W12,W13	**81110-61610**	**CABLE AY BNC-SMA**
W14,W15,W16,W17	**81110-61611**	**CABLE AY BNC-MCX1**
*** MP2**	**81110-64112**	**COVER BOTTOM ***
81101A		
MP310	**81101-40201**	**PANEL FRONT**
81104A, 81105A		
MP310	**81104-40201**	**PANEL FRONT**
81110A		
MP310	**81110-40202**	**PANEL FRONT**
81130A, '31A, '32A		
MP310	**81130-40201**	**PANEL FRONT**
MP4	**81130-61201**	**BRACKED FRONTEND**
W10,W11,W12,W13 W14,W15,W16	**81130-61610**	**CABLE AY FFP**
*** MP2**	**81130-64111**	**COVER BOTTOM ***
81132A		
MP7	**E4842-04101**	**THERMAL INTERFACE**

* The NEW Cover Bottom is ONLY possible to be
installed together with the new Power Supply, 120W!
The new power supply is backward compatible
and don't need the safety cover and cable clips any longer.

For older units with power supply p/n 0957-2779 installed
81101A SN DE38900597 and below
81104A SN DE38900465 and below
81110A SN DE38900804 and below
use
cover bottom p/n 81110-64102

81130A SN DE38900304 and below
use
cover bottom p/n 81130-64101

Board Exchange Information Sheet

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Germany

Agilent Technologies
Innovating the HP Way

May 18, 2000

After installing a new Bd. (p/n 811xx-66513/-69513 or 811xx-66515/-69515 or 81112-69507)
in an older unit, the following error may accure at power up selftest :
modules test fails
and error queue is: HW 1/CAL DATA CORRUPTED
It is the new BIOS SW in an old unit!

Please do the following:
* place the unit in an safe and calm area!
* switch unit ON
* press the [Help] key two times (>> clear the error queue)
* WAIT 30 min for warm up!

* press [More]
- 'press' [Config]
- on the screen select with the cursor key down
Perform: Selftest
(do not start the selftest!)
- press one key after the other to start temperature cal

.4907031143304

the display shows:
" Calibrate VCO drift ..... please wait "
wait 30 min until ready!

- if no fail
- press one key after the other to end temperature cal

.4907031142912

the display shows some seconds:
" Store Calibration data ..... please wait "
the display shows:
" BURN CALIBRATION DATA PASSED "

* switch unit OFF and ON again
NO ERROR should be visible!

Boeblingen **V**erification **S**olutions Operation
Agilent Technologies Deutschland GmbH
Germany
bvs-pdga_support@agilent.com
http://www.agilent.com/find/dvt

Board Exchange Information Sheet

811__-6____

Customer: _____

Date: _____

CSO number: _____ CE name: _____

CSC: _____ phone no.: _____

Self Test message: _____

_____

Detailed failure description: _____

_____

_____

_____

_____

_____

_____

Feedback information: _____

_____

_____

_____

_____

_____

_____

copy this page - fill in the information - and send it back together with the defective board!
additional you may fax the completed page to
(+49) 7031-464-6532, BVS PL24 Product Support

Design Gateway - Material List sorted by Reference Designator - May.18, 2000

Material List, Rev, Status: 81100-68700 , 3903 , RLSE
Description : FRONT PANEL AY 811XXA

Ref.D.	Comp.Number	Rev.	Component Description	Qty-per
A1	81110-66502	3739	RPG Board	1.0000
DS1	2090-0293		MONITOR-CRT 10 IN MONO NORITAKE	1.0000
MP301	81110-60201		FRONT PANEL ASSY	1.0000
MP303	81110-41901		RUBBERMAT	1.0000
MP304	08110-44101		PLATE	1.0000
MP305	08110-44102		PLATE	1.0000
MP306	08110-46501		KEYPAD FOIL	1.0000
MP311	08114-47105		GASKET FOAM	1.0000
SW1	0960-0865		OPTICAL ENCODER	1.0000
W2	81110-61604		CablAy Displ	1.0000
W4	81110-61603		Cbl Ay Rib40	1.0000

End of Report

Design Gateway - Material List sorted by Reference Designator - May.25, 2000

Material List, Rev, Status: 81100-68710 , 4021 , RLSE
Description : BASE CHASSIS AY 811XXA

Ref.D.	Comp.Number	Rev.	Component Description	Qty-per
A1	81110-66401	3817	MOTHER+uP BOARD	1.0000
MP1	81110-60111		CHASSIS MAIN	1.0000
MP10	8160-0797		RFI STRIP-FINGERS BE-CU 15.2-MM-WD	1.0000
MP11	8160-0797		RFI STRIP-FINGERS BE-CU 15.2-MM-WD	1.0000
MP16	81110-47402		KEY CAP LINE SWI	1.0000
MP17	0960-0996		FILTER PLATE MOUNTED LEADED CERAMIC	1.0000
MP100	0380-0643		STANDOFF-HEX .255-IN-LG 6-32-THD	1.0000
MP101	0380-0643		STANDOFF-HEX .255-IN-LG 6-32-THD	1.0000
MP102	2190-0321		WASHER-LK INTL T NO. 8 .168-IN-ID	1.0000
MP103	2190-0321		WASHER-LK INTL T NO. 8 .168-IN-ID	1.0000
MP104	5022-1629		SCREW-TPG 4.8 x	1.0000
MP105	5022-1629		SCREW-TPG 4.8 x	1.0000
MP106	5022-1629		SCREW-TPG 4.8 x	1.0000
MP107	5022-1629		SCREW-TPG 4.8 x	1.0000
MP109	7120-6153		LABEL-WARNING 12.5-MM-DIA POLYE	1.0000
MP117	1400-0611		CLAMP-FL-CA 1-WD PVC	1.0000
MP121	1400-1582		CLIP-CABLE AL	1.0000
MP122	1400-1582		CLIP-CABLE AL	1.0000
MP154	0515-0433		SCREW-MACHINE ASSEMBLY M4 X 0.7 8MM-	1.0000
MP155	0515-0433		SCREW-MACHINE ASSEMBLY M4 X 0.7 8MM-	1.0000
MP156	0515-0433		SCREW-MACHINE ASSEMBLY M4 X 0.7 8MM-	1.0000
MP157	0515-0433		SCREW-MACHINE ASSEMBLY M4 X 0.7 8MM-	1.0000
MP172	1400-1625		CLIP-CABLE STL	1.0000
MP173	1400-1625		CLIP-CABLE STL	1.0000
MP174	1420-0557		BATTERY 3V .95A-HR LI MANGANESE DIOX	1.0000
MP215	0950-3741		PWR-SPLY; POWER-150W; NO.-OF-OUTPUTS	1.0000
MP231	5040-1148		SHAFT-SHORT/GRAY	1.0000
MP302	08110-24502		MEMORY CARD TUBE	1.0000
MP306	08168-24756		SPACER SHOCK ABS	1.0000
MP307	08168-24756		SPACER SHOCK ABS	1.0000
MP308	5040-9352		CAP FIBER DIAM.	1.0000
MP309	5040-9352		CAP FIBER DIAM.	1.0000
MP313	0460-0616		TAPE-INDL .5-IN-W .005-IN-T	0.0017
MP400	0515-0430		SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP401	0515-0430		SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP402	0515-0430		SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP403	0515-0430		SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP404	0515-0430		SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP405	0515-0430		SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP406	0515-0430		SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP407	0515-0430		SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP408	0515-0430		SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP409	0515-0430		SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
W1	81110-61602		HP-IB-Cable Assy	1.0000
W3	81110-61601		Cble Ay Pwr Sw	1.0000
W5	81110-68501	3824	FAN ASSY	1.0000
W6	81110-68501	3824	FAN ASSY	1.0000

========== End of Report ==========

Design Gateway - Material List sorted by Reference Designator - Jun.28, 2000

Material List, Rev, Status: 81101A , 4023 , RLSE
Description : 50 MHz PULSE GENERATOR

Ref.D.	Comp.Number		Rev.	Component Description	Qty-per
	81100-44301			LBL Model/SN The	1.0000
	81100-90061			Reply Card	1.0000
	81101-40211			Panel Front	1.0000
	81101-91020			Agilent 81101A Q	1.0000
	81101-91021			Reference Guide	1.0000
	81101A	#0BW	4023	Service Manual	0.0000
	81101A	#1CM	3832	RACK MOUNT KIT	0.0000
	81101A	#1CN	3832	HANDLE KIT	0.0000
	81101A	#1CP	3832	RACK MOUNT& HANDLE KIT	0.0000
	81101A	#1CR	3832	RACK SLIDE KIT	0.0000
	81101A	#AB0	3832	QUICK ST GU TAIWAN CHINESE	0.0000
	81101A	#AB1	3832	QUICK ST GU KOREAN	0.0000
	81101A	#AB2	3832	QUICK ST GU CHINESE	0.0000
	81101A	#ABF	3832	QUICK ST GU FRENCH	0.0000
	81101A	#ABJ	3832	QUICK ST GU JAP	0.0000
	81101A	#UFJ	4008	1MB SRAM MEMORY CARD	0.0000
	81101A	#UK6		COMMERCIAL COC	0.0000
	81101A	#UN2	4023	REAR PANEL OPTION	0.0000
A3	81110-66403		4008	TIMING BOARD	1.0000
A4	81110-66404		3837	DELAY-WIDTH BOARD	1.0000
A5	E4821-66451		3809	BIOS Baord	1.0000
A6	81110-66408		3919	10V OUTPUT Board	1.0000
A10	81100-68700		3903	FRONT PANEL AY 811XXA	1.0000
A11	81100-68710		4021	BASE CHASSIS AY 811XXA	1.0000
MP2	81110-64102			COVER BOTTOM	1.0000
MP3	81110-04101			COVER TOP	1.0000
MP4	81110-61210			BRACKET FRONTEND	1.0000
MP5	81110-24510			CONNECTOR CASE	1.0000
MP6	81110-24701			SPACER FRONTEND	1.0000
MP7	0515-0430			SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP8	0515-0430			SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP9	0515-0430			SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP10	0515-0430			SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP11	0515-0430			SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP12	0515-0430			SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP13	0515-0430			SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP14	0515-0430			SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP15	81110-44302			Label CE/CSA	1.0000
MP16	2190-0067			WASHER-LK INTL T 1/4 IN .256-IN-ID	1.0000
MP17	2950-0216			NUT-HEX-DBL-CHAM 1/4-36-THD .062-IN-	1.0000
MP20	81110-01101			HEATSINK SHEET	1.0000
MP23	E2755-44341			LBL 4AY THERMOPR	1.0000
MP24	E2755-44341			LBL 4AY THERMOPR	1.0000
MP27	0515-0372			SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-	1.0000
MP28	0515-0372			SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-	1.0000
MP29	0515-0372			SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-	1.0000
MP30	0515-0372			SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-	1.0000
MP31	0515-0372			SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-	1.0000
MP32	0515-0372			SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-	1.0000
MP108	1251-7999			DUST COVER-MICRO RBN 24 CONT CONN	1.0000
MP110	6960-0002			PLUG-HOLE TR-HD FOR .5-D-HOLE STL	1.0000
MP111	6960-0002			PLUG-HOLE TR-HD FOR .5-D-HOLE STL	1.0000
MP112	6960-0002			PLUG-HOLE TR-HD FOR .5-D-HOLE STL	1.0000
MP113	6960-0002			PLUG-HOLE TR-HD FOR .5-D-HOLE STL	1.0000
MP114	6960-0002			PLUG-HOLE TR-HD FOR .5-D-HOLE STL	1.0000
MP115	6960-0002			PLUG-HOLE TR-HD FOR .5-D-HOLE STL	1.0000
MP116	6960-0002			PLUG-HOLE TR-HD FOR .5-D-HOLE STL	1.0000
MP117	6960-0002			PLUG-HOLE TR-HD FOR .5-D-HOLE STL	1.0000
MP118	6960-0002			PLUG-HOLE TR-HD FOR .5-D-HOLE STL	1.0000
MP119	6960-0002			PLUG-HOLE TR-HD FOR .5-D-HOLE STL	1.0000
MP150	0515-2048			SCREW-MACH M5 X 0.8 12MM-LG	1.0000

MP151	0515-2048	SCREW-MACH M5 X 0.8 12MM-LG	1.0000
MP152	0515-2048	SCREW-MACH M5 X 0.8 12MM-LG	1.0000
MP153	0515-2048	SCREW-MACH M5 X 0.8 12MM-LG	1.0000
MP158	0515-1410	SCREW-MACHINE ASSEMBLY M3 X 0.5 20MM	1.0000
MP159	0515-1410	SCREW-MACHINE ASSEMBLY M3 X 0.5 20MM	1.0000
MP160	0515-1410	SCREW-MACHINE ASSEMBLY M3 X 0.5 20MM	1.0000
MP161	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP162	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP163	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP164	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP165	0515-1946	SCREW-MACH M3 X 0.5 6MM-LG 90-DEG-FL	1.0000
MP169	0380-4210	STANDOFF-HEX 10-MM-LG M3.0 X 0.5-THD	1.0000
MP170	0380-4210	STANDOFF-HEX 10-MM-LG M3.0 X 0.5-THD	1.0000
MP171	0380-4210	STANDOFF-HEX 10-MM-LG M3.0 X 0.5-THD	1.0000
MP200	1460-1345	TILT STAND SST	1.0000
MP201	1460-1345	TILT STAND SST	1.0000
MP202	5041-9167	Foot	1.0000
MP203	5041-9167	Foot	1.0000
MP204	5041-9168	Foot Bottom No S	1.0000
MP205	5041-9168	Foot Bottom No S	1.0000
MP206	5041-9186	Fr.Cap,Strap-Han	1.0000
MP207	5041-9186	Fr.Cap,Strap-Han	1.0000
MP208	5041-9187	R. Cap,Strap-Han	1.0000
MP209	5041-9187	R. Cap,Strap-Han	1.0000
MP210	5041-9170	Trim Strip Side	1.0000
MP211	5041-9170	Trim Strip Side	1.0000
MP213	5063-9210	Strap Handle	1.0000
MP214	5063-9210	Strap Handle	1.0000
MP220	5021-2840	KEY-LOCK-FOOT	1.0000
MP221	5021-2840	KEY-LOCK-FOOT	1.0000
MP222	5021-2840	KEY-LOCK-FOOT	1.0000
MP223	5021-2840	KEY-LOCK-FOOT	1.0000
MP231	81110-46001	BUMPER FRONT	1.0000
MP232	81110-46002	Bumper rear	1.0000
MP309	81110-47401	CURSOR KNOB RPG	1.0000
MP400	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP401	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP402	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP403	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP404	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP405	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP406	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP407	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP408	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP409	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP410	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP411	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP412	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP413	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP414	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP415	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP416	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP417	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP418	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP419	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP420	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP421	2950-0035	NUT-HEX-DBL-CHAM 15/32-32-THD	1.0000
MP422	2950-0035	NUT-HEX-DBL-CHAM 15/32-32-THD	1.0000
MP423	2950-0035	NUT-HEX-DBL-CHAM 15/32-32-THD	1.0000
MP424	2950-0035	NUT-HEX-DBL-CHAM 15/32-32-THD	1.0000
MP425	2950-0035	NUT-HEX-DBL-CHAM 15/32-32-THD	1.0000
MP430	2190-0102	WASHER-LK INTL T 15/32 IN .472-IN-ID	1.0000
MP431	2190-0102	WASHER-LK INTL T 15/32 IN .472-IN-ID	1.0000
MP432	2190-0102	WASHER-LK INTL T 15/32 IN .472-IN-ID	1.0000
MP433	2190-0102	WASHER-LK INTL T 15/32 IN .472-IN-ID	1.0000
MP434	2190-0102	WASHER-LK INTL T 15/32 IN .472-IN-ID	1.0000
MP437	2190-0054	WASHER-LK INTL T 1/2 IN .505-IN-ID	1.0000
MP440	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP441	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP442	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP443	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP444	0515-0430	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-	1.0000
MP450	1400-0824	STRAP-CABLE PLSTC	1.0000
MP451	1400-0824	STRAP-CABLE PLSTC	1.0000

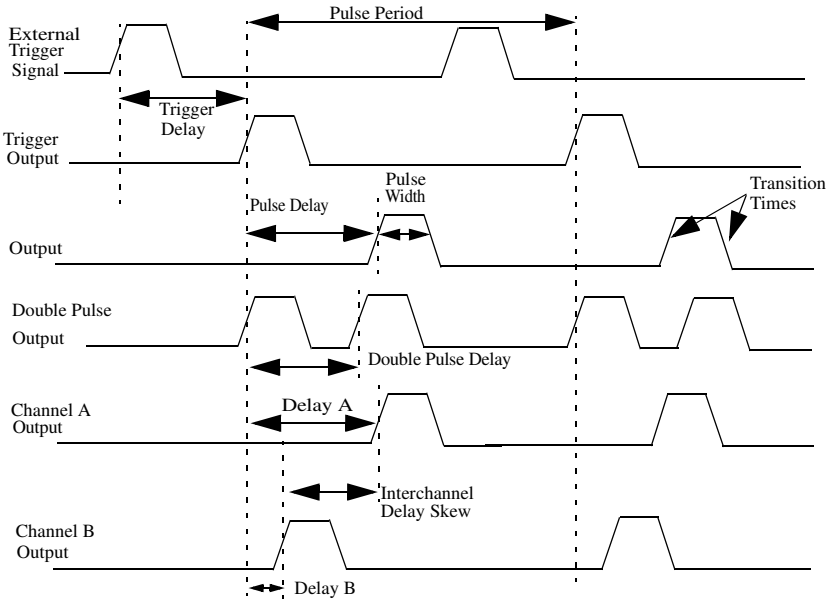
MP452	1400-0824	STRAP-CABLE PLSTC	1.0000
MP453	1400-0824	STRAP-CABLE PLSTC	1.0000
MP600	81110-68301	PACKAGING ASSY	1.0000
MP601	E8311-10020	Agilent USER SW	1.0000
W9	8120-1689	OPT-902 3-COND 2-M-LG	0.5000
W10	81110-61610	CablAy BNC-SMA	1.0000
W14	81110-61611	CblAy BNC-MCX1	1.0000
W15	81110-61611	CblAy BNC-MCX1	1.0000
W16	81110-61611	CblAy BNC-MCX1	1.0000
W17	81110-61611	CblAy BNC-MCX1	1.0000

========== End of Report ==========

Pulse Parameter Definitions

Here you find the pulse parameter definitions of terms used in the instrument specifications. In the following figure a graphical overview of the pulse parameters is provided:

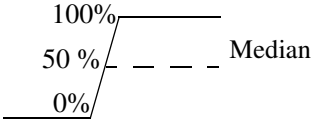
Figure 1 Overview of the Pulse Parameters



Time Reference Point:

The time reference point is at the median of the amplitude (50% amplitude point on pulse edge).

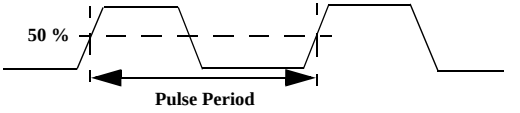
Figure 2 Time Reference at Median Amplitude



Pulse Period:

The time interval between the leading edge medians of consecutive output pulses

Figure 3 Pulse Period



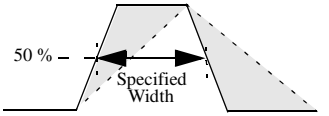
Trigger Delay

Interval between trigger point of the external trigger input signal and the trigger output pulse's leading-edge median.

Pulse Width:

Interval between leading- and trailing-edge medians. The specified and displayed value is that obtained with fastest edges, essentially equal to the interval from the start of the leading edge to the start of the trailing edge. By designing so that the pulse edges turn about their start points, the interval from leading-edge start stays unchanged (in practice, start points may shift with changes in transition time) when transition times are varied. This is more convenient for programming and the width display is easy to interpret.

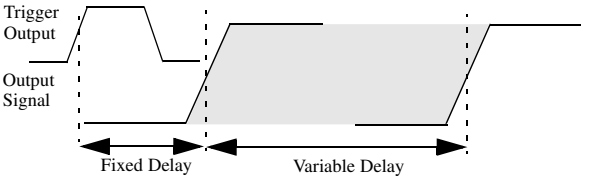
Figure 4 **Pulse Width**



Pulse Delay:

Interval between leading edge medians of trigger output pulse and output pulse. The specified and displayed value is that obtained with the fastest leading edge. Pulse delay has two components, a fixed delay from trigger output to output signal and a variable delay with respect to the trigger output.

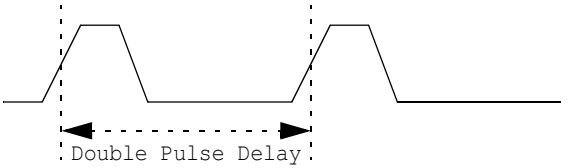
Figure 5 Pulse Delay



Double Pulse Delay:

Interval between leading edge medians of the double pulses.

Figure 6 Double Pulse Delay



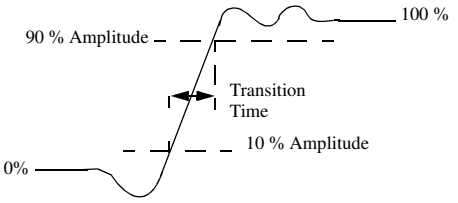
Interchannel Delay (Skew)

Interval between corresponding leading-edge medians of the output signals.

Transition Time:

Interval between the 10%- and 90%- amplitude points on the leading/trailing edge.

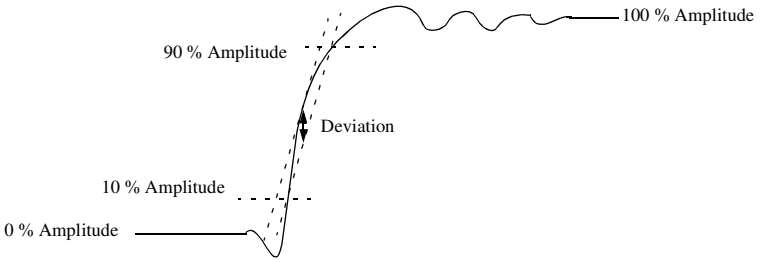
Figure 7 Transition Time



Linearity:

Peak deviation of an edge from a straight line through the 10%- and 90%- amplitude points, expressed as percentage of pulse amplitude.

Figure 8 Linearity



Jitter:

Short-term instability of one edge relative to a reference edge. Usually specified as rms value, which is one standard deviation or “sigma”. If distribution is assumed Gaussian, six sigma represents 99.74% of the peak-peak jitter.
The reference edge for period jitter is the previous leading edge. That for delay jitter is the leading edge of the trigger output. Width jitter is the stability of the trailing edge with regard to the leading edge.

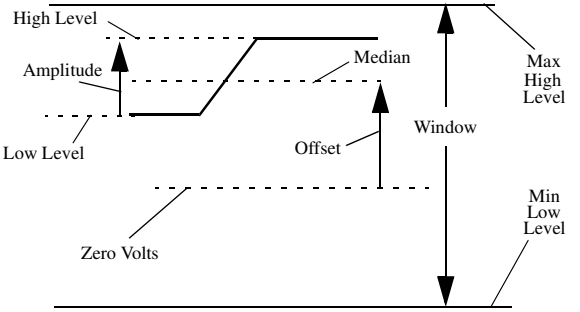
Stability:

Long-term average instability over a specific time, for example, hour, year. Jitter is excluded.

Pulse Levels:

Pulse output is specified as pulse top and pulse base (usually referred to as high level and low level), or as peak to peak amplitude and median offset. A “window” specification shows the limits within which the pulse can be positioned.

Figure 9 Pulse Amplitude

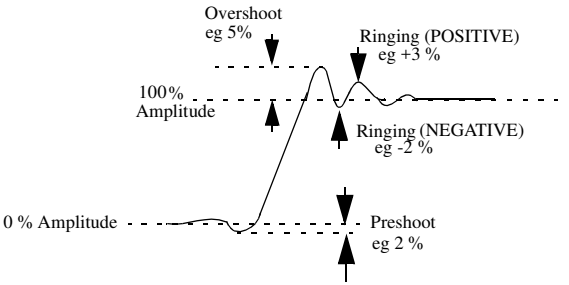


Preshoot, Overshoot, Ringing:

Preshoot and overshoot are peak distortions preceding/following an edge. Ringing is the positive-peak and negative-peak distortion, excluding overshoot, on pulse top or base. A combined preshoot, overshoot, and ringing specification of e.g. 5% implies:

- Overshoot/undershoot < 5%
- Largest pulse-top oscillation
  <± 5%, of pulse amplitude.

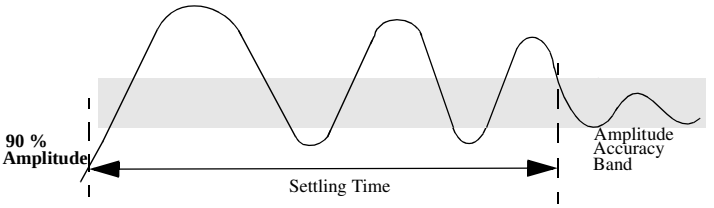
Figure 10 Preshoot, Overshoot, Ringing



Settling Time:

Time taken for pulse levels to settle within level specifications, measured from 90% point on leading edge.

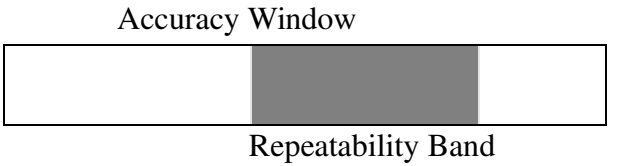
Figure 11 Settling Time



Repeatability:

When an instrument operates under the same environmental conditions and with the same settings, the value of a parameter will lie within a band inside the accuracy window. Repeatability defines the width of this band.

Figure 12 Repeatability



Agilent 81101A
Performance Test

Introduction

Use the tests in this chapter if you want to check that the Agilent 81101A 50 MHz Pulse Generator is working correctly. Before starting any testing allow all test equipment to warm up for at least 30 minutes.

Conventions Used

When referring to actions that you perform during the tests, the following conventions are used:

FUNCTION This indicates that a labelled button must be pressed

[**MODE/TRG**] This shows that a soft-key must be pressed. A soft-key is an unlabelled button whose label is shown on the display, and which can vary according to the job that the button is doing

CONTINUOUS PULSES This is an option shown on the display, and is selected by use of the vernier keys. It is shown in upper or lower case to match the case displayed.

Test Results Tables

Tables for entering the results of the tests are included at the end of this chapter. The tests are numbered and reference numbers for each Test Result (TR) are given in a small table at the end of each test. The reference number shows you where the actual results should be entered in the Test Results Tables.

The Test Results tables at the end of the chapter should be photo-copied, and the Test Results entered on the copies. Then, if the tests need to be repeated, the tables can be copied again.

Recommended Test Equipment and Accessories

The following tables list the recommended test equipment you need to perform all the tests in this chapter. You can use alternative instruments if they meet the critical specifications given. The test set-ups and procedures assume you are using the recommended equipment.

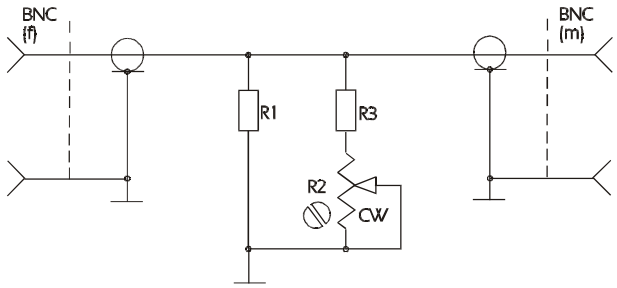
Test Equipment	Model	Critical Specifications
Oscilloscope or	Agilent 54121T	20 GHz, 10 bit vertical resolution, Histogram
Oscilloscope	Agilent 54750A + Agilent 54751A	20 GHz, 15 bit vertical resolution, Histogram
Counter or	Agilent 5334B #010, 030	Period and Time Interval measurements Oven Osci, 1.3 GHz C-Channel
Counter	Agilent 53132A #001/010, 030	Frequency measurements > 150 MHz High-Stability Timebase, 3 GHz Channel
Digital Voltmeter	Agilent 3458A	DCV up to 20 V
Pulse Generator	Agilent 8110A	up to 150 MHz
Delay line	Agilent 54008A	22 ns

Accessories	Model	Critical Specifications
Digitizing Oscilloscopes Accessories Attenuators Power Splitter SMA/SMA (m-m) adaptor SMA/BNC Adaptor SMA Cable	8493C#020 33340C#020 8493C#006 33340C#006 11667B 1250-1159 E9632A (1250-1700) 8120-4948	20 dB 6 dB
50 Ω Feedthrough Termination	10100C **See Figure**	2 W,1% 10 W,0.1%
Adapter	1251-2277	BNC to Banana
Cable Assemblies, BNC	E9637A (8120-1839)	
Torque Wrench	8710-1582	5/16 in, 5 lb-in (56 Ncm)

NOTE: When you connect the test equipment for the first time, and whenever you change the setup during the course of these tests, use the 8710-1582 torque wrench to tighten and loosen SMA connectors. This will ensure that the connectors are at the correct tightness and give the best signal transfer.

50 Ohm, 0.1%, 10 W Feedthrough Termination

The following figure provides a schematic and a parts list except for the case. The case must provide shielding and maintain grounding integrity.



50 Ohm, 0.1%, 10 W Feedthrough Termination

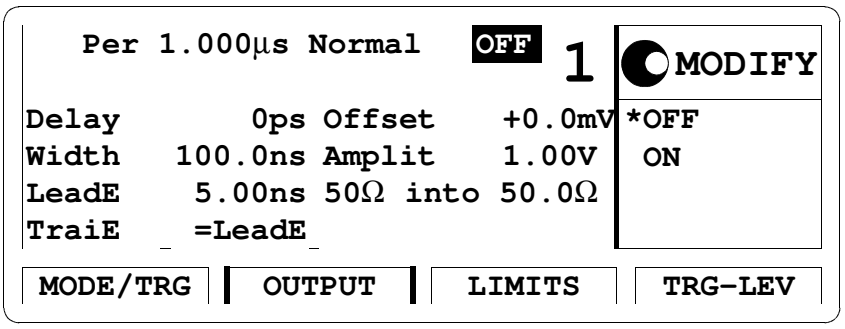
The following parts are required:

1. R1 = 53.6Ω, 1%, 10 W; Part Number: 0699-0146
2. R2 = 200 Ω, 10%, 0.5 W, Variable trimmer; Part Number: 2100-3350
3. R3 = 681 Ω;, 1%, 0.5 W; Part Number: 0757-0816
4. BNC (M): Part Number: 1250-0045
5. BNC (F): Part Number: 1250-0083

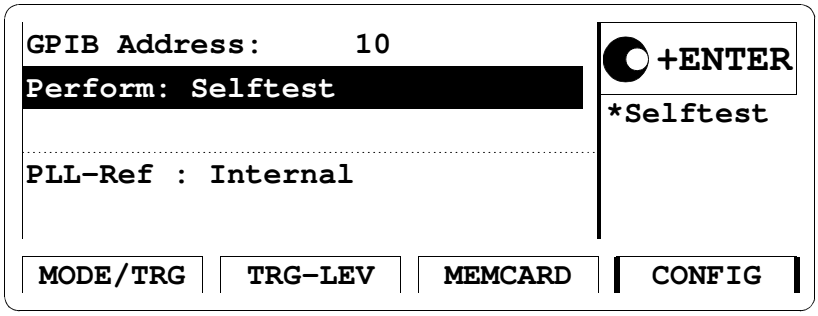
Getting Started

The Agilent 81101A is controlled by selecting options in a series of **pages** that are displayed on the instrument's screen. When the Agilent 81101A is being tested, different situations can arise. The following examples illustrate this

Typical Examples of Displayed Screens



The OUTPUT Screen in a Agilent 81101A



The CONFIG Screen in an Agilent 81101A

Instrument Serial Numbers

You will need to write the serial numbers of the instrument at the top of the Test Reports. These can be found as follows:

Press HELP, [**SERIAL #**]

The Agilent 81101A display lists the instrument's product and serial number, firmware revision and date.

The display on your instrument should look similar to this:

FRAME	**:**	**81101A 50 MHz**
Serial No	**:**	**DE38700132**
FIRMWARE	**:**	**01.00.01**
DATE	**:**	**xx/xx/98**

The serial number given for the **FRAME** applies to the Mainframe, the Power Supply, the Microprocessor Board, and the Timing Board as well as the Output Channel.

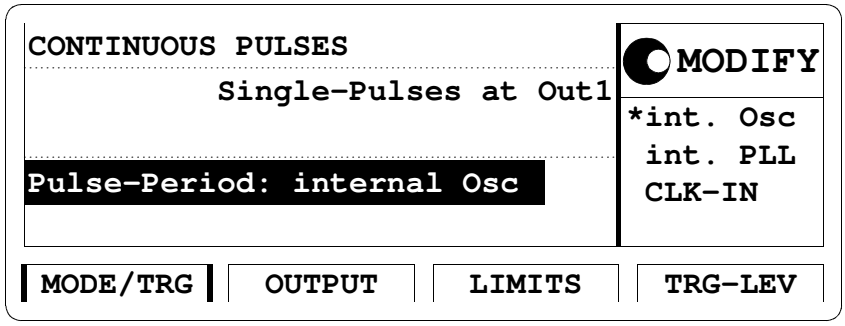
Initial Setup of the Agilent 81101A

In the majority of these tests the initial setting up of the instrument is identical. Therefore, it is described once here, and then referred-to where appropriate. In cases where the initial setup differs, an illustration of the settings is shown.

Set up the Agilent 81101A as follows:

1. Select [**MODE/TRG**]

- **CONTINUOUS PULSES**
- **Single-Pulses at Out 1**
- **Pulse-Period:internal Osc**



MODE/TRG Screen

Test 1: Period (PLL not active)

Test Specifications

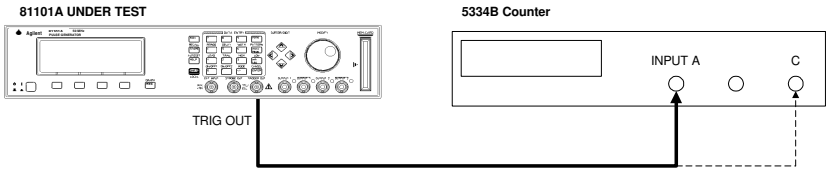
Range	20 ns to 999.5 s
Resolution	3.5 digits, best case 5 ps
Accuracy	±5%

Equipment Needed

Counter
Cable, 50 Ω, coaxial, BNC

Procedure

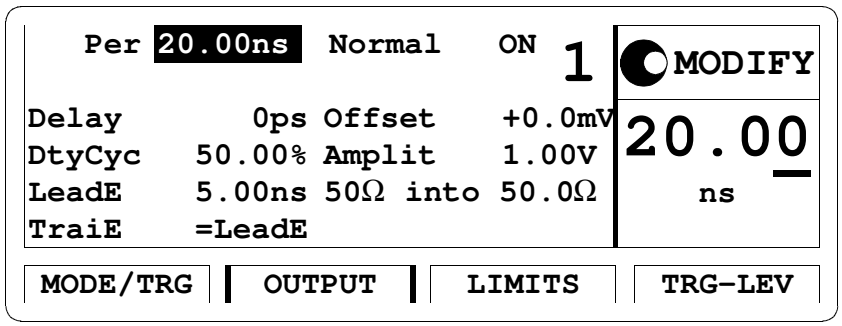
1. Connect the Agilent 81101A to the Counter as shown:



Connecting the Agilent 81101A to the Counter

2. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"

On the Agilent 81101A set up [OUTPUT] page as shown in the following illustration:



Configuring Output

3. Set the Counter to:

FUNCTION	Period A
INPUT A	50 Ω
SENSE	On

4. Check the Agilent 81101A period at the following settings:

Period	Acceptable Range	TR entry
20.00 ns	19.00 ns to 21.00 ns	1 - 1
50.00 ns	47.5 ns to 52.5 ns	1 - 2
99.90 ns	94.905 ns to 104.895 ns	1 - 3

Period	Acceptable Range	TR entry
100 ns	95 ns to 105 ns	1 - 4
500 ns	475 ns to 525 ns	1 - 5
1 µs	950 ns to 1050 ns	1 - 6
500 µs	475µs to 525 µs	1 - 7
500 ms	475 ms to 525 ms	1 - 8

Test 2: PLL Period

NOTE: This test is only performed if PLL is switched on.

Test Specifications

Range 20 ns to 999.5 s
Resolution 4 digits, best case 1 ps
Accuracy ± 0.01%

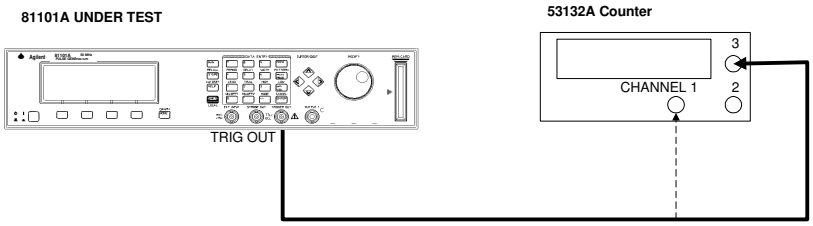
Equipment Needed

Counter Agilent 53132A
Cable, 50 Ω, coaxial, BNC

NOTE: The Agilent 53132A counter is used in frequency mode to meet the MIL CAL A uncertainty requirements for TAR (Test Accuracy Ratio) > 4:1.

Procedure

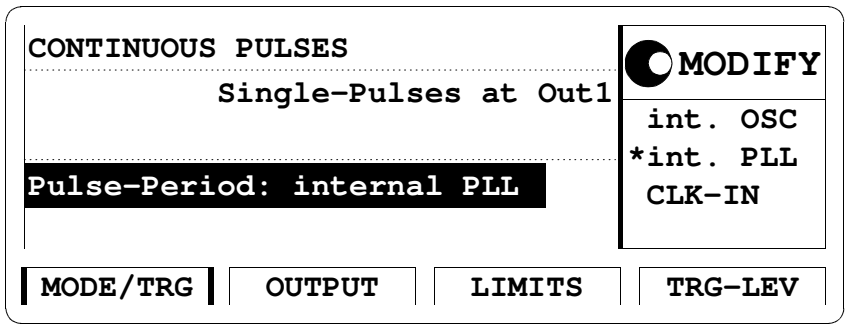
Connect the Agilent 81101A to the counter as follows:



Connecting Agilent 81101A to the Counter

5. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"

6. Select the [**MODE/TRG**] screen on the Agilent 81101A and set up as follows:



The MODE/TRG Screen Setup

7. On the Agilent 81101A set up [**OUTPUT**] page as shown in the test before!

8. Set the Counter to measure the frequency at the choosen input 1 / 3

9. Check the Agilent 81101A PLL pulse period at the following settings:

Period	Frequency	Acceptable Range	TR Entry
20.00 ns	50 MHz	49.995 MHz to 50.005 MHz	2 - 1
50.00 ns	20 MHz	19.998 MHz to 20.002 MHz	2 - 2
100 ns	10 MHz	9.999 MHz to 10.001 MHz	2 - 3
500 ns	2 MHz	1.9998 MHz to 2.0002 MHz	2 - 4
1 µs	1 MHz	999.9 kHz to 1.0001 MHz	2 - 5
50 µs	20 kHz	9.998 kHz to 20.002 kHz	2 - 6
5 ms	200 Hz	199.980 Hz to 200.020 Hz	2 - 7
500 ms	2 Hz	1.9998 Hz to 2.0002 Hz	2 - 8
5 s	0.2 Hz	0.19998 Hz to 0.20002 Hz	2 - 9

Test 3: Width

Test Specifications

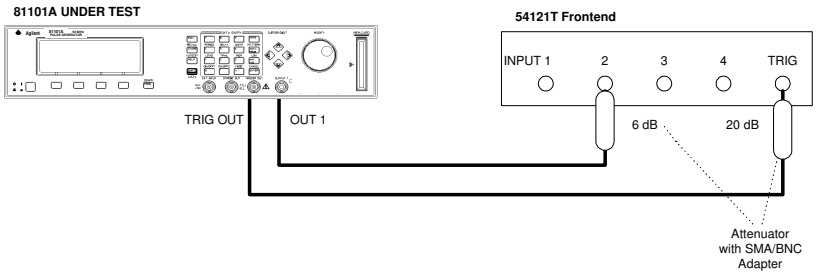
Range	10 ns to (period - 10 ns)
Resolution	3.5 digits, best case 5 ps
Accuracy	± 5% ± 250 ps

Equipment Needed

Digitizing Oscilloscope with Accessories
Counter
Cable, 50 Ω, coaxial, BNC

Procedure

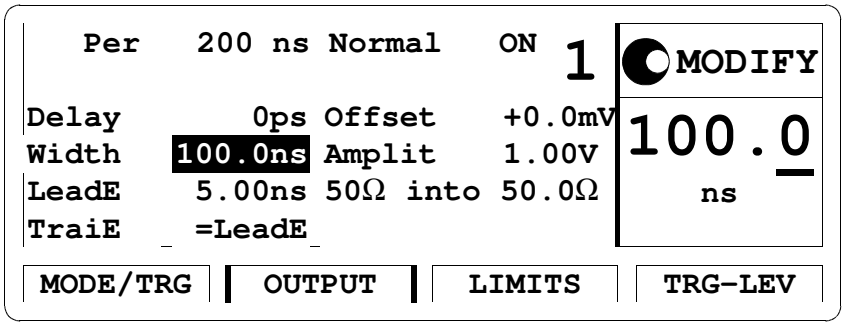
1. Connect Agilent 81101A to the Scope as shown:



Connecting Agilent 81101A to the Scope

2. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"

3. On the Agilent 81101A set up [OUTPUT] page as shown in the following illustration:



Configuring Output Screen

4. Set the Digitizing Oscilloscope Agilent 54121T:

- Press AUTOSCALE
- Select the Display menu and set the Number of Averages to 32
- Select the delta V menu and turn the voltage markers On
- Set the preset levels to 50% -50% and press AUTO LEVEL SET
- Select the delta t menu and turn the time markers ON
- Set START ON EDGE = POS 1 and STOP ON EDGE = NEG1

5. Change the oscilloscope timebase to 1 ns/div

6. Change the Agilent 81101A Width to 10 ns

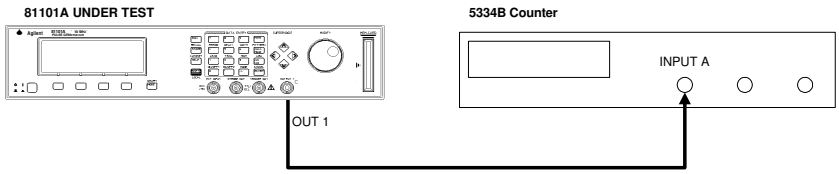
7. Center the pulse in the Scope display

8. Press the PRECISE EDGE FIND key for each new Width setting

9. Check the Agilent 81101A pulse width at the following settings:

Oscilloscope Timebase	Period	Width	Acceptable Range	TR Entry
2 ns/div	200 ns	10.00 ns	9.250 ns to 10.750 ns	3 - 1
10 ns/div	200 ns	50.00 ns	47.25 ns to 52.75 ns	3 - 2
20 ns/	1 µs	100.0 ns	94.75 ns to 105.25 ns	3 - 3
100 ns	1 µs	500.0 ns	474.75 ns to 525.25 ns	3 - 4

10. Connect the Agilent 81101A to the Counter as shown:



Connecting Agilent 81101A to the Counter

11. Set the Counter to:

FUNCTION	TI A→ B
SENSE	On
INPUT A	50 Ω
COM A	On
INPUT B	50 Ω, negative slope

12. Check the Agilent 81101A width at the following settings:

Period	Width	Acceptable Range	TR Entry
100 µs	50 µs	47.5 µs to 52.5 µs	3 - 6
10 ms	5 ms	4.75 ms to 5.25ms	3 - 7
999 ms	500ms	475 ms to 525 ms	3 - 8

Test 4: Delay

Test Specifications

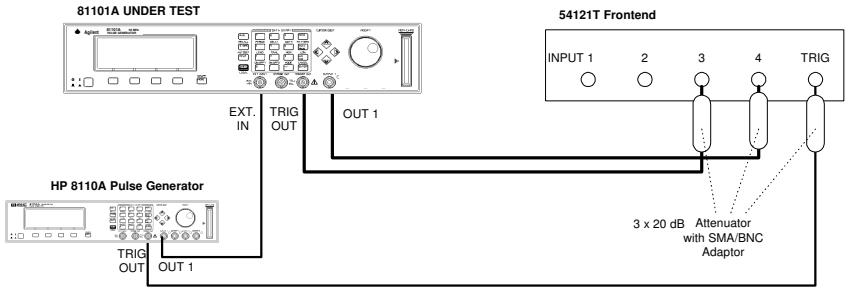
Range	Fixed typical Delay of EXT INPUT to TRIGGER OUT 12 ns TRIGGER OUT to OUTPUT 1/2 17 ns Variable Delay: 0 ns to (period - 20 ns)
Resolution	3.5 digits, best case 5 ps
Accuracy	±5% ±1 ns

Equipment Needed

Digitzing Oscilloscope with Accessories
Pulse Generator
Counter
Cable, 50 Ω, coaxial, BNC

Procedure

Connect Agilent 81101A to the Scope as shown:



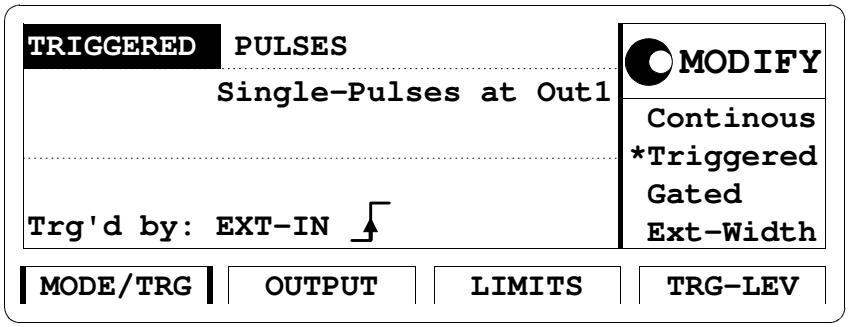
Connecting Agilent 81101A to the Scope

13. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"

14. Set the Pulse Generator to:

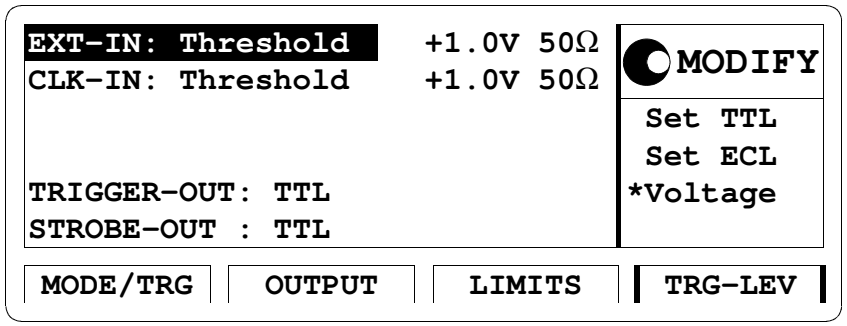
Period	1 µs
Width	100 ns
Amplitude	1 V
Offset	+1.0 V
Output	Enable

15. Select the [**MODE/TRG**] screen on the Agilent 81101A and set up as follows:



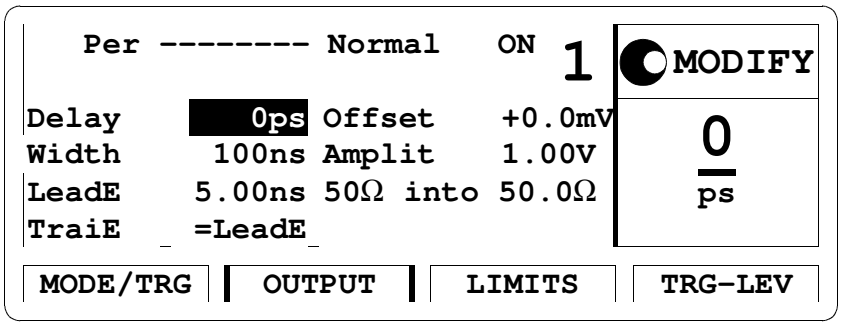
The MODE/TRG Screen Setup

16. On the Agilent 81101A select [**TRIG-LEV**] page and set up as follows:



The TRG-LEV Screen Setup

17. On the Agilent 81101A set up [OUTPUT] page as shown in the following illustration:



Configuring Output Screen

18. Set the Digitizing Oscilloscope Agilent 54121T:

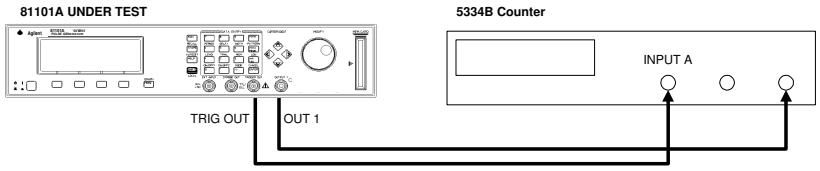
- Press AUTOSCALE
- Set timebase to TIME/DIV = 10 ns/div
- Center the positive-going edges of the two signals
- Select the Display menu and set the screen function to single; set the number of averages to 32
- Select the Delta V menu and turn the voltage markers ON and assign marker 1 to channel 3 and marker 2 to channel 4
- Set Preset levels to 50% - 50% and press AUTO LEVEL SET
- Select the Delta t menu and turn the time markers ON
- Set START ON EDGE= POS1 and STOP ON EDGE= POS 1
- Press the PRECISE EDGE FIND key

19. Check the Agilent 81101A delay at the following settings:

NOTE: Record the value of the fixed delay and subtract it from the other readings.

Oscilloscope Timebase	Delay	Acceptable Range	TR Entry
10 ns/div	0 ps	fixed Delay of TRIG OUT to OUT 1/2: 17 ns typ.	4 - 1
10 ns/div	5.000 ns	3.75 ns to 6.25 ns	4 - 2
20 ns/div	10.00 ns	8.500 ns to 11.50 ns	4 - 3
20 ns/div	50.00 ns	46.50 ns to 53.50 ns	4 - 4
50 ns/div	100.0 ns	94.00 ns to 106.00 ns	4 - 5
200 ns/div	500.0 ns	474.00 ns to 526.00 ns	4 - 6

20. Connect the Agilent 81101A to the Counter as follows:



Connecting Agilent 81101A to the Counter

21. Set Agilent 81101A to **`Continuous-Pulses`** on the MODE/TRG screen

22. Set the Counter to:

FUNCTION TI	A → B
SENSE	On
INPUT A	50 Ω
INPUT B	50 Ω

23. Check the Agilent 81101A delay at the following settings:

NOTE: Subtract the fixed delay from the other readings

Period	Delay	Acceptable Range	TR Entry
100 µs 10 ms 999 ms	50 µs 5 ms 500ms	47.5 µs to 52.5 µs 4.75 ms to 52.5ms 475 ms to 525 ms	4 - 7 4 - 8 4 - 9

Test 5: Double Pulse Delay

Test Specifications

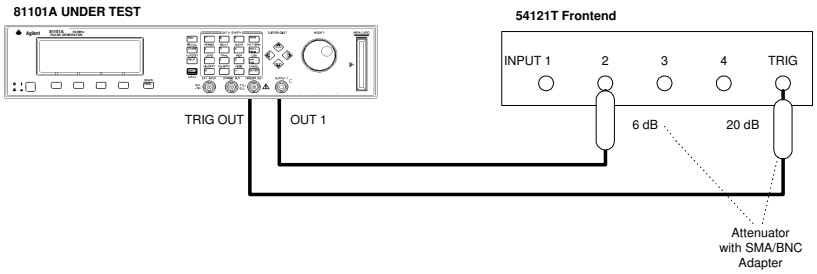
Range	20 ns to (period - width - 10 ns)
Resolution	3.5 digits, best case 5 ps
Accuracy	± 5% ± 500 ps

Equipment Needed

Digitizing Oscilloscope with Accessories
Counter
Cable, 50 Ω, coaxial, BNC

Procedure

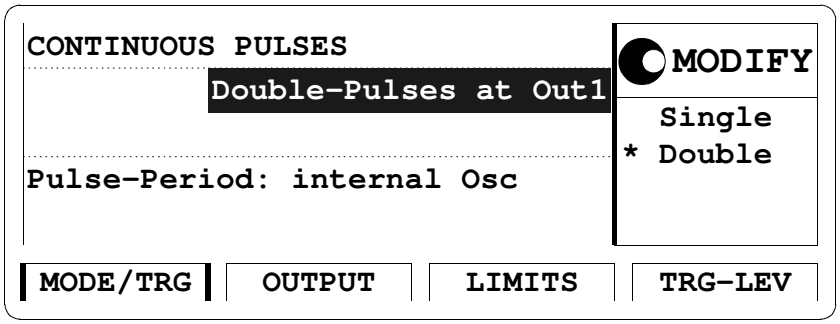
1. Connect Agilent 81101A to the Scope as shown:



Connecting Agilent 81101A to the Scope

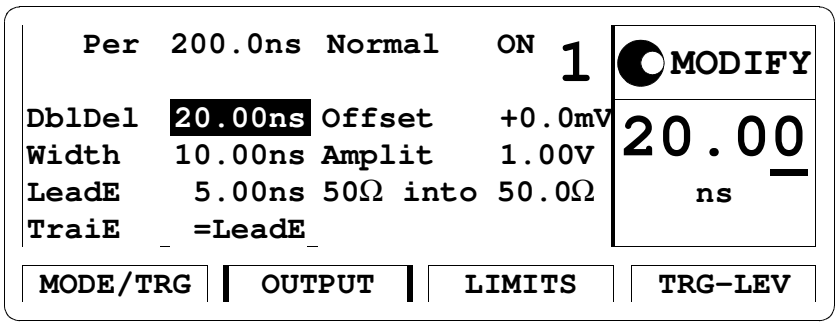
2. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"

3. Select the [**MODE/TRG**] screen on the Agilent 81101A and set up Output 1 and Output 2 as follows:



The MODE/TRG Screen Setup

4. On the Agilent 81101A set up [**OUTPUT**] page as shown in the following illustration:



Configuring Output Screen

5. Set the Digitizing Oscilloscope Agilent 54121T:

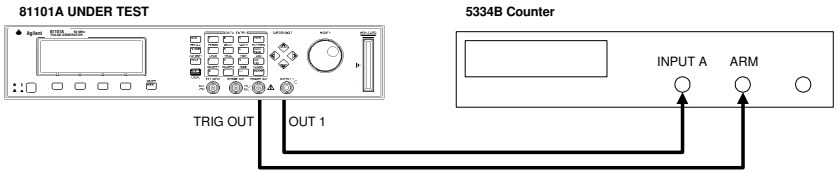
- Press AUTOSCALE
- Center the double pulse signal
- Select the Display menu and set the Number of Averages to 32
- Select the Delta V menu and turn the Voltage markers On
- Set Preset Levels = 50% -50% and press AUTO LEVEL SET
- Select the Delta t menu and turn the Time markers On
- Set START ON EDGE = POS1 and STOP ON EDGE = POS2

6. Press the PRECISE EDGE FIND key for each new Double Delay setting

7. Check the Agilent 81101A double delay at the following settings:

Oscilloscope Timebase	Double Delay	Acceptable Range	TR Entry
2 ns/div	20.00 ns	18.5 ns to 21.5 ns	5 - 1
10 ns/div	50.00 ns	47.00 ns to 53.00 ns	5 - 2
20 ns/div	100.0 ns	94.5 ns to 105.5 ns	5 - 3

8. Connect the Agilent 81101A to the Counter as shown:



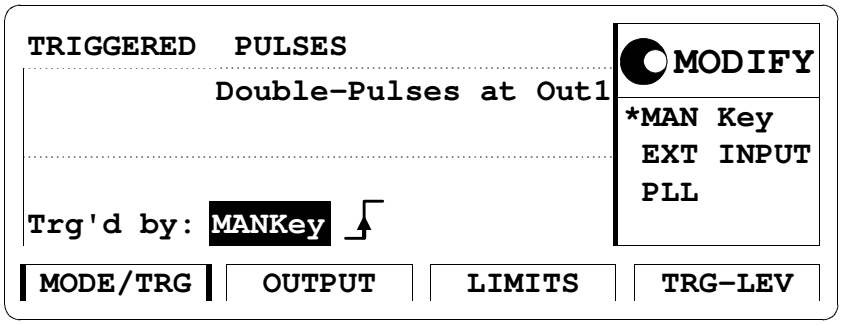
Connecting Agilent 81101A to the Counter

9. Set the Counter to:

FUNCTION	Period A
INPUT A	50 Ω
SENSE	On
(EXT ARM SELECT	a. Start (ST): leading edge b. Stop (SP): trailing edge)

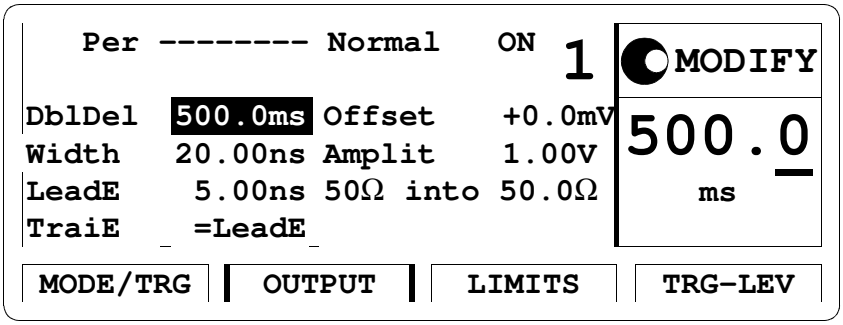
10. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"

11. Select the[**MODE/TRG**]screen on the Agilent 81101A and set up as follows;



The MODE/TRG Screen Setup

12. On the Agilent 81101A set up [**OUTPUT**] page as shown in the following illustration:



Configuring Output Screen

13. Check the Agilent 81101A double pulse delay at the following settings:

    Press MAN to check each new setting!

Double Delay	Acceptable Range	TR Entry
500 ms	475 ms to 525 ms	5 - 4
1 s	950.00 ms to 1050.00 ms	5 - 5

Test 6: Jitter

The following tests are required:

1. Period Jitter
   a. Internal Oscillator
   b. Internal PLL
2. Width Jitter
3. Delay Jitter

Test 6.1a: Period Jitter, Internal Oscillator

Test Specifications

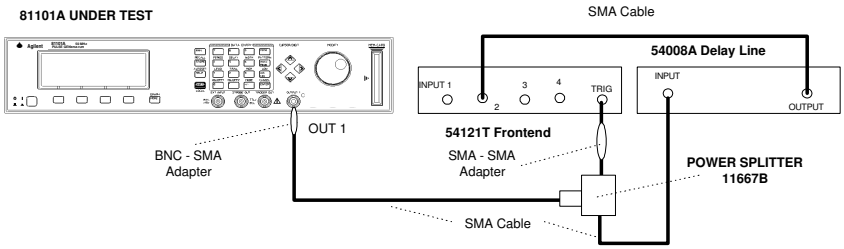
RMS-Jitter 0.01% + 15 ps

Equipment Needed

Digitizing Oscilloscope with Accessories
Delay Line (22 ns)
Power Splitter
Cable, 50 Ω, coaxial, BNC
Cable, SMA

Procedure

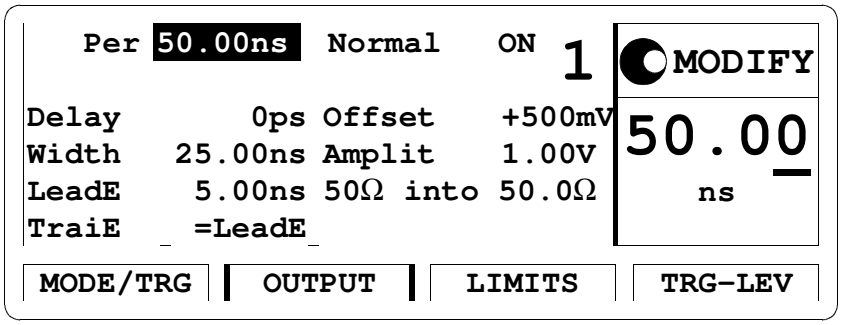
1. Connect Agilent 81101A to the Scope as shown:



Equipment Set-up for Jitter Test

2. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"

3. On the Agilent 81101A set up [**OUTPUT**] page as shown in the following illustration:



Configuring Output Screen

4. Set the Digitizing Oscilloscope Agilent 54121T:

- Press AUTOSCALE
- Select the Display menu and set the Number of Averages to 64
- Select the Channel menu and set the Attenuation factor of channel 2 to 2
- Set the VOLTS/DIV of channel 2 to 10 mV/div
- Set OFFSET to 500 mV
- Select the Timebase menu and set the TIME/DIV to 100 ps/div
- Center the first positive-going edge of the signal (approximate Delay = 28ns)
- Select the Delta V menu and turn the V markers On
- Set the Marker 1 Position to 490 mV and the Marker 2 Position to 500 mV
- Select the Delta t menu and turn the T Markers On
- Set START ON EDGE = POS1 and STOP ON EDGE = POS1
- Press the PRECISE EDGE FIND key

5. RECORD the delta t reading. This is the rise time of the reference signal within a 1% amplitude window of the signal connected to Input 2. This value is needed later to calculate the correct jitter.(delta.t.up)

6. Select the Timebase menu and center the second positive-going edge of the signal (approximate Delay = 78 ns)

7. Press MORE and HISTOGRAM

- Select the Window submenu and set:
- Source is channel 2
- Choose the Time Histogram
- Press WINDOW MARKER 1 and set it to 490 mV
- Press WINDOW MARKER 2 and set it to 500 mV

8. Select the Acquire submenu, set the Number of Samples to 1000 and press START ACQUIRING

9. After the data for the time histogram has been acquired (# Samples = 100%), select the Result submenu.

10. Press MEAN and SIGMA. RECORD the values of sigma

11. The RMS-jitter is calculated as follows:

$$RMS\text{ - }jitter = \frac{6sigma\text{ - }delta.t.up}{6}$$

12. The RMS-jitter for period of 50 ns is 20 ps. Enter the result in the Test Report as TR entry 6.1a - 1

13. Set the Agilent 81101A period to 500 ns

14. Repeat steps 6 to 11

NOTE: TIME/DIV = 200 ps/div; approximate Delay = 527 ns

15. The RMS-jitter for period of 500 ns is 65 ps. Enter the result in the Test Report as TR entry 6.1a - 2

Test 6.1b: Period Jitter, Internal PLL

Test Specifications

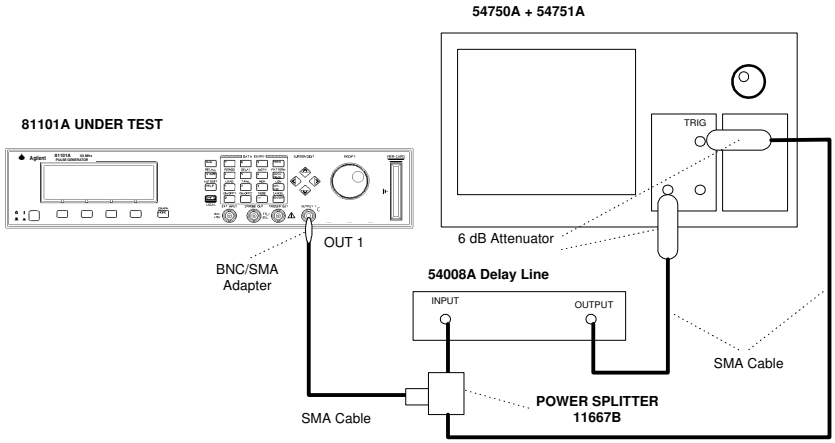
RMS-Jitter 0.001% + 15 ps

Equipment Needed

Digitizing Oscilloscope with Accessories
Delay Line (22 ns)
Power Splitter
Cable, 50 Ω, coaxial, BNC
Cable, SMA

Procedure

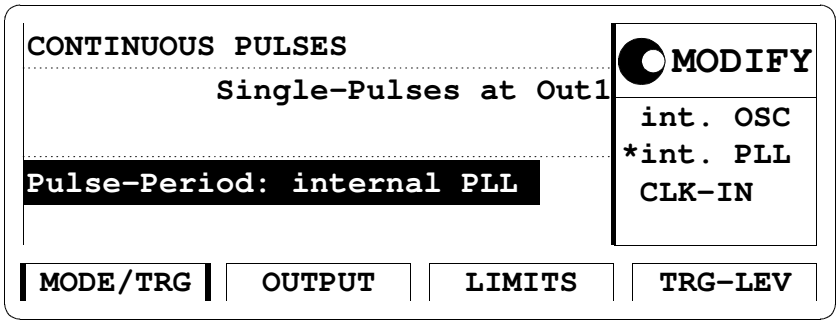
1. Connect Agilent 81101A to the Scope as shown.



Equipment Set-up for Jitter Test using the Agilent 54750A + 54751A
Using the Agilent 54121T the Set-up is the same as before.

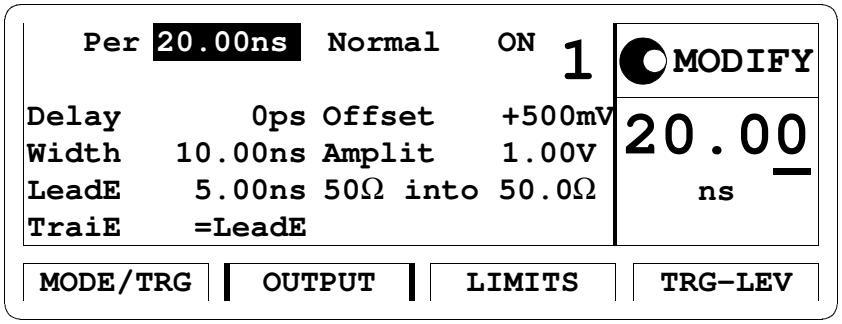
2. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"

3. Select the [**MODE/TRG**] screen on the Agilent 81101A and set up as follows:



The MODE/TRG Screen Setup

4. On the Agilent 81101A set up [**OUTPUT**] page as shown in the following illustration:



Configuring Output Screen

5. Set the Digitizing Oscilloscope Agilent 54121T:

- Press AUTOSCALE
- Select the Display menu and set the Number of Averages to 64
- Select the Channel menu and set the Attenuation factor of channel 2 to 2
- Set the VOLTS/DIV of channel 2 to 10 mV/div
- Set OFFSET to 500mV
- Select the Timebase menu and set the TIME/DIV to 100 ps/div
- Center the first positive-going edge of the signal (approximate Delay = 28 ns)
- Select the Delta V menu and turn the V markers On
- Set the Marker 1 Position to 490 mV and the Marker 2 Position to 500mV
- Select the Delta t menu and turn the T Markers On
- Set START ON EDGE = POS1 and STOP ON EDGE = POS1
- Press the PRECISE EDGE FIND key

6. RECORD the delta t reading. This is the rise time of the reference signal within a 1% amplitude window of the signal connected to Input 2. This value is needed later to calculate the correct jitter. (delta.t.up)
7. Select the Timebase menu and center the second positive-going edge of the signal (approximate Delay = 78 ns)

8. Press MORE and HISTOGRAM

- Select the Window submenu and set:

- Source is channel 2
- Choose the Time Histogram
- Press WINDOW MARKER 1 and set it to 490 mV
- Press WINDOW MARKER 2 and set it to 500 mV

9. Select the Acquire submenu, set the Number of Samples to 1000 and press START ACQUIRING
10. After the data for the time histogram has been acquired (# Samples = 100%), select the Result submenu.

11. Press MEAN and SIGMA. RECORD the values of sigma

12. The RMS-jitter is calculated as follows:

$$RMS\text{ - }jitter = \frac{6sigma\text{-}delta.t.up}{6}$$

13. The RMS-jitter for period of 20 ns is 15.2 ps. Enter the result in the Test Report as TR entry 6.1b - 1

NOTE: See the Agilent54750A User's Guide / Service Guide to get the info needed to do the Jitter Test using this scope.

Test 6.2: Width Jitter (PLL not active)

Test Specifications

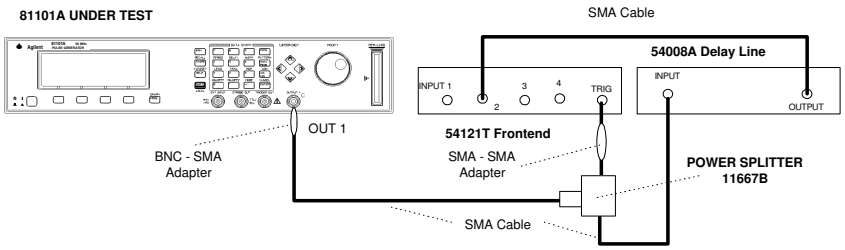
RMS-Jitter 0.01% + 15 ps

Equipment Needed

Digitizing Oscilloscope with Accessories
Delay Line (22 ns)
Power Splitter
Cable, 50 Ω, coaxial, BNC
Cable, SMA

Procedure

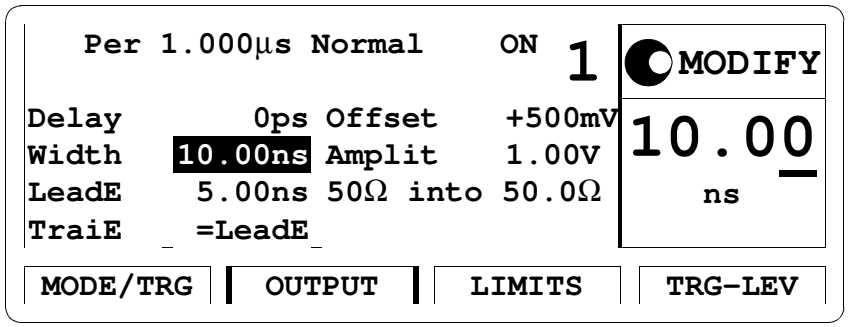
1. Connect Agilent 81101A to the Scope as shown:



Equipment Set-up for Jitter Test

2. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"

3. On the Agilent 81101A set up [**OUTPUT**] page as shown in the following illustration:



Configuring Output Screen

4. Set the Digitizing Oscilloscope Agilent 54121T:

- Press AUTOSCALE
- Select the Display menu and set the Number of Averages to 128
- Select the Channel menu and set the Attenuation factor of channel 2 to 2
- Set the VOLTS/DIV 500 mV
- Select the Timebase menu and set the TIME/DIV to 10 ps/div
- Center the first negative-going edge of the signal (approximate Delay = 36 ns)
- Select the Delta V menu and turn the V markers On

- Set the Marker 1 Position to 500 mV and the Marker 2 Position to 490 mV
- Select the Delta t menu and turn the T Markers On
- Set START ON EDGE = NEG1 and STOP ON EDGE = NEG1
- Press the PRECISE EDGE FIND key

5. RECORD the delta t reading. This is the fall time of the referencesignal within a 1% amplitude window of the signal connected to Input 2. This value isneeded later to calculate the correct jitter. (delta.t.dn)

6. Set the Agilent 81101A Pulse Width to 50 ns

7. Select the Timebase menu and center the first negative-going edge of the signal (approximate Delay = 77 ns)

8. Press MORE and HISTOGRAM

9. Select the Window submenu and set:

- Source is channel 2
- Choose the Time Histogram
- Press WINDOW MARKER 1 and set it to 500 mV
- Press WINDOW MARKER 2 and set it to 490 mV

10. Select the Acquire submenu, set the Number of Samples to 1000 and press START ACQUIRING

11. After the data for the time histogram has been acquired (# Samples = 100%), select the Result submenu.

12. Press MEAN and SIGMA. RECORD the value of sigma

13. The RMS-jitter is calculated as follows:

$$\text{RMS - jitter} = \frac{6 \text{ sigma - delta.t.dn}}{6}$$

14. The RMS-jitter for pulse width of 50 ns is 20 ps. Enter the result in the Test Report as TR entry 6.2 - 1

15. Set the Agilent 81101A for pulse width of 500ns

16. Repeat steps 7 to 13

NOTE: TIME/DIV = 100ps/div. Approximate delay = 527 ns

17. The RMS-jitter for pulse width of 500 ns is 65 ps. Enter the result in the Test Report as TR entry 6.2 - 2

Test 6.3: Delay Jitter (PLL not active)

Test Specifications

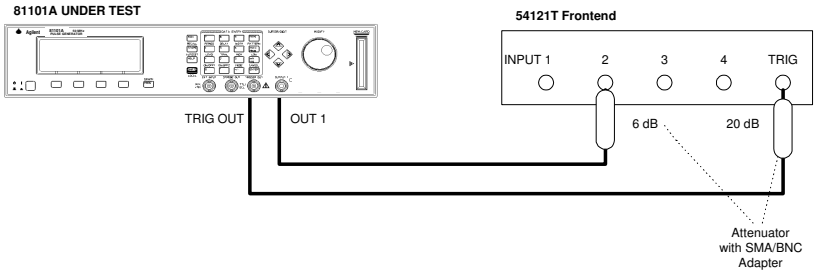
RMS-Jitter 0.01% + 15 ps

Equipment Needed

Digitizing Oscilloscope with Accessories

Procedure

1. Connect Agilent 81101A to the Scope as shown:



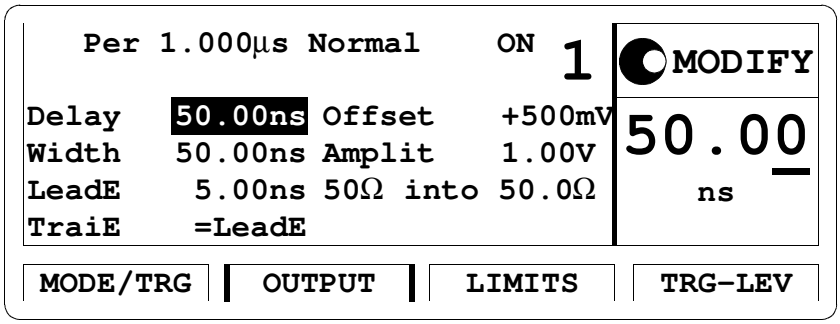
Equipment Set-up for Delay Jitter Test

2. For calculating the RMS-jitter, the rise time of the reference signal within a 1% amplitude window is required. If this value

is not already measured in the Period Jitter test, then perform the first 6 steps of the Period Jitter test.

3. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"

4. On the Agilent 81101A set up [**OUTPUT**] page as shown in the following illustration:



Configuring Output Screen

5. Set the Digitizing Oscilloscope Agilent 54121T:

- Press AUTOSCALE
- Select the Display menu and set the Number of Averages to 64
- Set the VOLTS/DIV = 10 mV/div
- Set OFFSET to 500 mV
- Select the Timebase menu and set the TIME/DIV to 100 ps/div
- Center the first positive-going edge of the signal (approximate Delay = 65 ns)

6. Press MORE and HISTOGRAM
7. Select the Window submenu and press WINDOW MARKER 1 and set it to 490 mV
8. Press WINDOW MARKER 2 and set it to 500 mV
9. Select the Acquire submenu, set the Number of Samples to 1000 and press START ACQUIRING
10. After the delta for the time histogram has been acquired (# Samples = 100%), select the Result submenu.
11. Press MEAN and SIGMA. RECORD the values of sigma!
12. The RMS-jitter is calculated as follows:

$$\text{RMS - jitter} = \frac{6\text{sigma - delta.t.up}}{6}$$

13. The RMS-jitter for delay of 50 ns is 20 ps. Enter the result in the Test Report as TR entry 6.3 - 1
14. Set Agilent 81101A for delay of 500 ns
15. Repeat steps 9 to 12

NOTE: TIME/DIV = 100 ps/div. Approximate delay = 515 ns

16. The RMS jitter for delay of 500 ns is 65 ps. Enter the result in the Test Report as TR entry 6.3 - 2

Test 7: High and Low Levels

The following tests are required:

1. High level from 50Ω into 50Ω
2. Low level from 50Ω into 50Ω
3. High level from 1KΩ into 50Ω
4. Low level from 1KΩ into 50Ω

Test Specifications

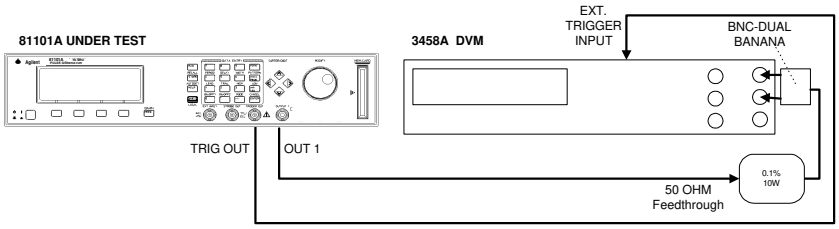
	Load Impedance 50 Ω	
Source Impedance	50 Ω	1 KΩ
High Level	-9.90 V to +10.0 V	-19.8 V to +20.0 V
Low Level	-10.0 V to +9.9 V	-20.0 V to +19.8 V
Amplitude	0.10 Vpp to 10.0 Vpp	0.20 Vpp to 20.0 Vpp
Level Resolution	10 mV	20 mV
Level Accuracy	± 3% of ampl ± 75 mV	± 5% of ampl ± 150 mV for amplitude ≤ 19V

Equipment Needed

1. Digitizing Voltmeter (DVM)
2. 50 Ω Feedthrough Termination, 0.1%, 10 W Adapter.
3. BNC to dual banana plug (1251-2277)
4. Cable, 50 Ω, coaxial, BNC

Procedure

Connect Agilent 81101A to the DVM as shown:

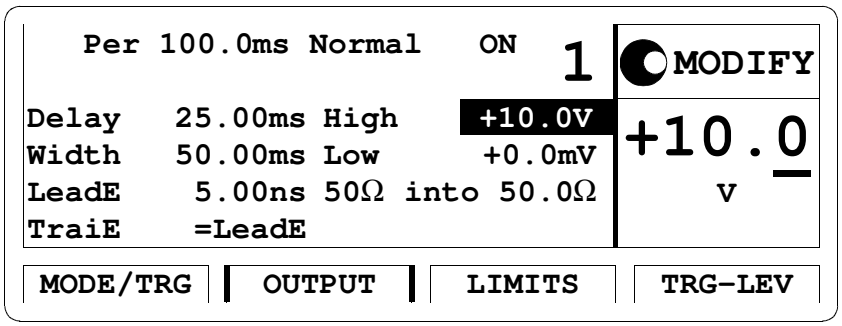


Connecting the DVM for High and Low Levels Tests

Test 7.1: High Level, 50 Ohms into 50 Ohms

1. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"

2. On the Agilent 81101A set up [**OUTPUT**] page as shown in the following illustration:



Configuring Output Screen

3. Set the DVM Agilent 3458A to:

Function: DCV
Trigger: TRIG EXT
AD-Converter integration time NPLC: 0.1
(Number of Power Line Cycles)

4. Check the Agilent 81101A high level at the following high level settings with the low level set to 0.0 V.

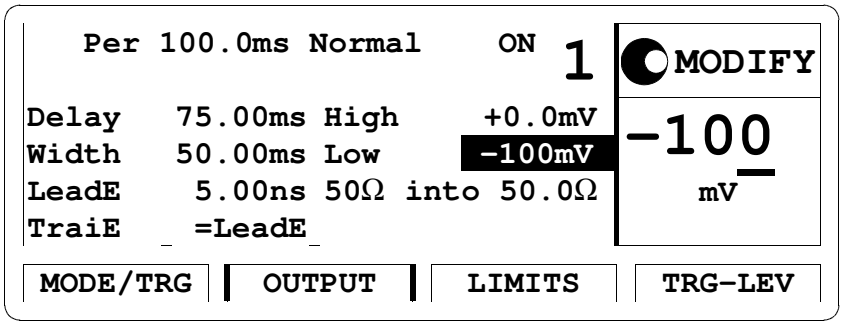
High Level	Acceptable Range	TR Entry
10.0 V	9.625 V to 10.375 V	7.1 - 1
5.0 V	4.775 V to 5.225 V	7.1 - 2
3.0 V	2.845 V to 3.165 V	7.1 - 3
1.0 V	0.895 V to 1.105 V	7.1 - 4
0.5 V	410 mV to 590 mV	7.1 - 5
0.1 V	22 mV to 178 mV	7.1 - 6

The low level may vary within ± 3% of amplitude ± 75 mV

Test 7.2: Low Level, 50 Ohms into 50 Ohms

1. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"

2. On the Agilent 81101A set up [**OUTPUT**] page as shown in the following illustration:



Configuring Output Screen

3. Check the Agilent 81101A low level at the following low level settings with the high level set to 0.0 V

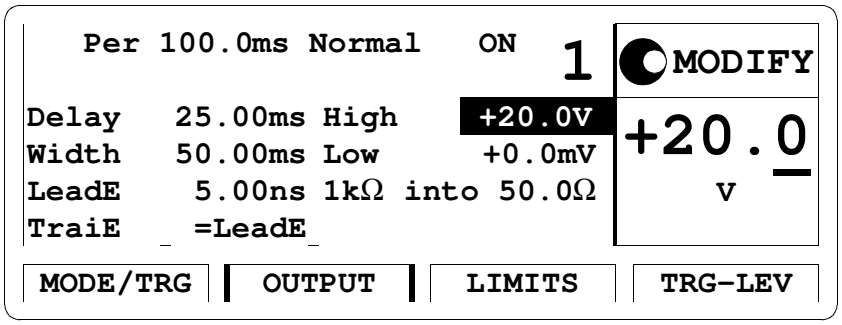
Low Level	Acceptable Range	TR Entry
-0.1 V	-22 mV to -178 mV	7.2 - 1
-0.5 V	-410 mV to -590 mV	7.2 - 2
-1.0 V	-0895 V to -1.105 V	7.2 - 3
-3.0 V	-2.845 V to -3.165 V	7.2 - 4
-5.0 V	-4.775 V to -5.225 V	7.2 - 5
-10.0 V	-9.625 V to -10.375 V	7.2 - 6

The high level 0.0 V may vary $\pm$ 3% of amplitude $\pm$75 mV.

Test 7.3: High Level, 1K Ohms into 50 Ohms

1. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A

2. On the Agilent 81101A set up [**OUTPUT**] page as shown in the following illustration:



Configuring Output Screen

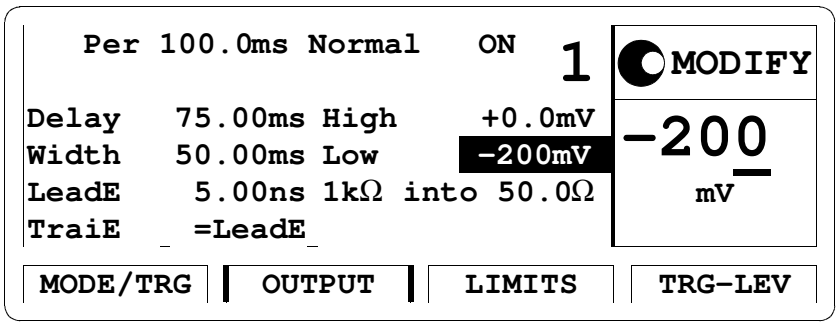
3. Check the Agilent 81101A high level at the following high level settings with the low level set to 0.0 V.

High Level	Acceptable Range	TR Entry
19.0 V	17.9 V to 20.1 V	7.3 - 1
10.0 V	9.35 V to 10.65 V	7.3 - 2
5.0 V	4.60 V to 5.40 V	7.3 - 3
1.0 V	0.80 V to 1.20 V	7.3 - 4
0.2 V	40 mV to 360 mV	7.3 - 5

The low level 0.0 V may vary ± 5% of amplitude ± 150 mV.

Test 7.4: Low Level, 1K Ohms into 50 Ohms

1. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"
2. On the Agilent 81101A set up [**OUTPUT**] page as shown in the following illustration:



Configuring Output Screen

3. Check the Agilent 81101A low level at the following low level settings with the high level set to 0.0 V.

Low Level	Acceptable Range	TR Entry
-0.2 V	-40 mV to -360 mV	7.4 - 1
-1.0 V	-0.80 V to -1.20 V	7.4 - 2
-5.0 V	-4.60 V to -5.40 V	7.4 - 3
-10.0 V	-9.350 V to -10.650 V	7.4 - 4
-19.0 V	-17.90 V to -20.10 V	7.4 - 5

The high level 0.0 V may vary $\pm$ 5% of amplitude $\pm$ 150 mV

Test 8: Transition Time

Test Specifications

Range	5.0 ns to 200 ms (measured between 10% and 90% of amplitude)
Accuracy	± 10% ± 200 ps
Linearity	typical ± 3% for transitions > 100 ns

Equipment Needed

Digitizing Oscilloscope with Accessories
Cable, SMA

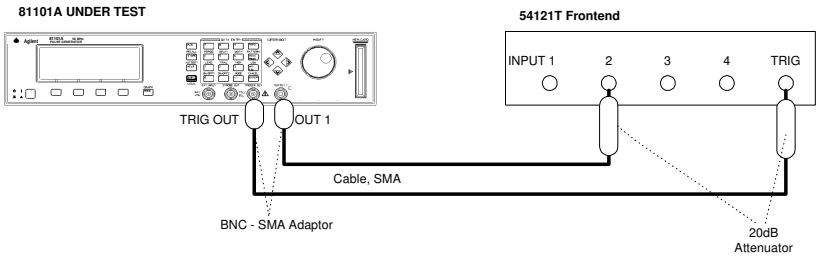
Procedure

Perform the tests as shown in the following sections:

Test 8.1a: Leading Edge Test

Minimum Leading Edge and Leading Edge ranges .

1. Connect Agilent 81101A to the Scope as shown:



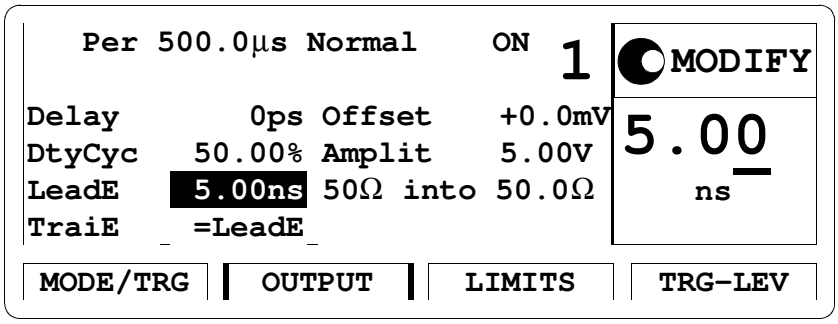
Connecting Agilent 81101A to the Scope

NOTE:

When you connect the test equipment the first time, and whenever you change the setup during the following tests, use the torque wrench (8170-1582) to tighten and loosen the SMA connectors. This will ensure that the connectors are at the correct tightness and give the best signal transfer!

2. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"

3. On the Agilent 81101A set up **[OUTPUT]** page as shown in the following illustration:



Configuring Output Screen

4. Set the Digitizing Oscilloscope Agilent 54121T:

- Press AUTOSCALE
- Center one pulse on screen, e.g.:
- TIME/DIV = 50 µs/div, DELAY = 380 µs,
- Select the Display menu and set the Number of Averages to 32
- Select the Channel menu and set the Attenuation factor to 10
- Select the Delta V menu and turn the voltage markers On
- Set the Preset Levels = 10-90% and press AUTO LEVEL SET
- Select the Timebase menu and set TIME/DIV = 1 ns/div, DELAY = 20 ns
- Select the Delta t menu and turn the markers On
- Set START ON EDGE = POS1 and STOP ON EDGE = POS1

5. Set period of Agilent 81101A to: Period = 1 µs and change the Agilent 81101A Delay to center the leading edge of the first pulse on the screen

6. After the averaging, while the oscilloscope is in the Delta t menu, Press the PRECISE EDGE FIND key

7. Check the Agilent 81101A rise times at the following leading edge settings:

Oscilloscope TIME/ DIV	Period	Leading Edge	Trailing Edge	Acceptable Range	TR Entry
2 ns/div	1 µs	5.0 ns	5.0 ns	≤5 ns to 5.7 ns	8.1a - 1
5 ns/div	1 µs	10 ns	10 ns	8.8 ns to 11.2 ns	8.1a - 2
10 ns/div	1 µs	50 ns	50 ns	44.8 ns to 55.2ns	8.1a - 3
100 ns/div	5 µs	500 ns	500 ns	449.8 ns to 550.2 ns	8.1a - 4
1µs/div	50 µs	5 µs	5 µs	4.4998 µs to 5.5002 µs	8.1a - 5
10 µs/div	500 µs	50 µs	50 µs	45 µs to 55 µs	8.1a - 6
100 µs	5 ms	500 µs	500 µs	450 µs to 550 µs	8.1a - 7
10 ms/div	500 ms	50 ms	50 ms	45 ms to 55 ms	8.1a - 8

Test 8.1b: Trailing Edge Test

Minimum Trailing Edge and Trailing Edge range.

1. Connect Agilent 81101A to the Scope as shown in Test 8.1a Leading Edge Test.

2. Set up the Agilent 81101A as described in Test 8.1a Leading Edge Test.

3. Set the digitizing oscilloscope Agilent 54121T:

- Select the oscilloscopes Timebase menu and set TIME/DIV to 1 ns/div
  and DELAY to approximately 520ns
- Select the oscilloscopes Delta t menu and set START ON EDGE = NEG1 and STOP ON EDGE = NEG1

4. While the oscilloscope is in the Delta t menu, press the PRECISE EDGE FIND key

5. Check the Agilent 81101A output signal falls at the following trailing edge settings:

Oscilloscope TIME/DIV	Delay	Period	Trailing Edge	Leading Edge	Acceptable Range	TR Entry
2 ns/div	529 ns	1 µs	5.0 ns	5.0 ns	≤5 ns to 5.7 ns	8.1b - 1
5 ns/div	529 ns	1 µs	10 ns	5 ns	8.8 ns to 11.2 ns	8.1b - 2
10 ns/div	529 ns	1 µs	50 ns	50 ns	44.8 ns to 55.2 ns	8.1b - 3
100 ns/div	25 µs	5 µs	500 ns	500 ns	449.8 ns to 550.2 ns	8.1b - 4
1 µs/div	25 µs	50 µs	5 µs	5 µs	4.4998 µs to5.5002 µs	8.1b - 5
10 µs/div	250 µs	500 µs	50 µs	50 µs	45 µs to 55 µs	8.1b - 6
100 µs/div	2.5 ms	5 ms	500 µs	500 µs	450 µs to550 µs	8.1b - 7
10 ms/div	250 ms	500 ms	50 ms	50 ms	45 ms to 55 ms	8.1b - 8

Test 9: Pulse Aberration Test

The following tests are required:

Overshoot and Ringing
Preshoot

Test Specifications

Overshoot/Preshoot/Ringing
± 5% of amplitude ± 20 mV

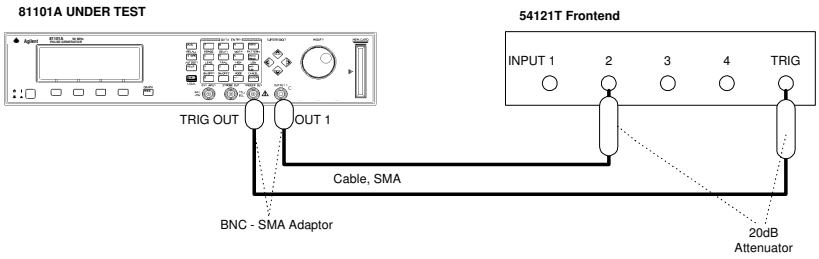
Equipment Needed

Digitizing Oscilloscope with Accessories

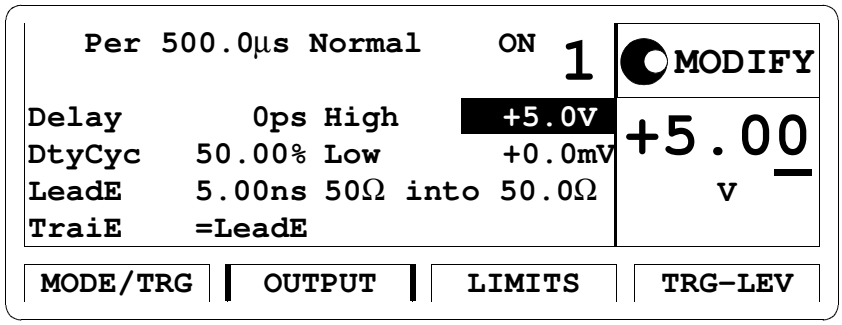
Procedure

6. Set up the Agilent 81101A as described in "Initial Setup of the Agilent 81101A"

1. Connect Agilent 81101A to the Scope as shown:



Connecting Agilent 81101A to the Scope



Configuring Output Screen

Overshoot and Ringing

2. Set the digitizing oscilloscope Agilent 54121T:

- Press AUTOSCALE
- Select the Display menu and set the Number of Averages to 32
- Select the Channel menu and set the Attenuation factor to 10
- Center one pulse horizontally and vertically on screen
- (e.g. TIME/DIV = 50µs/div, DELAY = 250 µs)
- Select the delta V menu and turn the voltage markers On
- Set the VARIABLE LEVELS = 95% - 105% and press AUTO LEVEL SET
- Select the channel menu and center vertically the top pulse (offset = 5 V)
- Set the VOLTS/DIV = 200 mV/div

- Select the Timebase menu and set TIME/DIV = 5 ns/div, DELAY = 16 ns (>> 500 ns)

3. Set the Agilent 81101A to period = 500 ns

4. Check that Overshoot and Ringing are within the ±5% of amplitude ±20 mV window

5. Enter the result in the Test Report as TR entry 9 - 1

NOTE: Take the oscilloscope's trace flatness error (GaAs input circuit) into account.

Preshoot

6. Set Agilent 81101A to:
- Period = 500 µs
- High Level = 5 V
- Low Level = 0 V
- Delay = 10 ns

7. Set the digitizing oscilloscope, Agilent 54121T:

- Press AUTOSCALE
- Select the Display menu and set the Number of Averages to 32
- Select the Channel menu and set the Attenuation factor to 10
- Center one pulse horizontally and vertically on screen
- (e.g. TIME/DIV = 50µs/div, DELAY = 265 µs)
- Select the delta V menu and turn the voltage markers On
- Set the VARIABLE LEVELS = -5% to +5% and press AUTO LEVEL SET

- Select the channel menu and center vertically the bottom of the pulse (offset = 0 V)
- Set the VOLTS/DIV = 200 mV/div
- Select the Timebase menu and set TIME/DIV = 5 ns/div, DELAY = 16 ns

8. Set Agilent 81101A to period = 500 ns
9. Check that Preshoot is within the ±5% of amplitude ± 20 mV window.
10. Enter the result in the Test Report as TR entry 9 - 3

Agilent 81101A Performance Test Records

Test Facility:

_____ Report No. _____
_____ Date _____
_____ Customer _____
_____ Tested By _____

×

Model Agilent 81101A 50 MHz Pulse Generator

Serial No. _____

Options _____ Ambient temperature _____°C
_____ Relative humidity _____%
_____
_____

Firmware Rev. _____ Line frequency _____Hz

Special Notes:

_____
_____
_____
_____
_____

Test Equipment Used				
	Description	Model No.	Trace No.	Cal. Due Date
1.	Oscilloscope	Agilent 54121T	_____	_____
2.	Counter	Agilent 5334B	_____	_____
3.	Digital Voltmeter	Agilent 3458A	_____	_____
4.	Pulse Generator	Agilent 8110A	_____	_____
5.	Delay Line	Agilent 54008A	_____	_____
6.	_____			
7.	_____			
8.	_____			
9.	_____			
10.	_____			
11.	_____			
12.	_____			
13.	_____			
14.	_____			

Test Results for Agilent 81101A Mainframe

Serial No. _____ Ambient temperature _____ °C

Customer _____ Relative humidity _____ %

CSO# _____ Line frequency _____ Hz

Tested by _____ Date _____

Comments

_____
_____
_____

Internal Oscillator Period

Scope Uncertainty factor _____

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
1-1	20.0ns	19.000 ns	_____	21.000 ns	____	____
1-2	50.0ns	47.5 ns	_____	52.5 ns	____	____
1-3	99.9ns	94.905 ns	_____	104.895 ns	____	____

Counter Uncertainty factor _____

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
1-6	100 ns	95.0ns	_____	105.0 ns	____	____
1-7	500 ns	475.0 ns	_____	525.0 ns	____	____
1-8	1 µs	950.0 ns	_____	1050.0 ns	____	____
1-9	5 00µs	475 µs	_____	5 25 µs	____	____
1-10	500 ms	475 ms	_____	525 ms	____	____

PLL Period
(Results measured as frequency by counter)

Counter Uncertainty factor _____

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
2-1	20.00 ns	49.995MHz	_____	50.005 MHz	__	__
2-2	50.00 ns	19.9980MHz	_____	20.0020MHz	__	__
2-3	100 ns	9.9990MHz	_____	10.0010MHz	__	__
2-4	500 ns	1.9998MHz	_____	2.0002MHz	__	__
2-5	1 µs	999.9 kHz	_____	1.0001 MHz	__	__
2-6	50 µs	19.998 kHz	_____	20.002 kHz	__	__
2-7	5 ms	199.98 Hz	_____	200.02 Hz	__	__
2-8	500 ms	1.9998 Hz	_____	2.0002 Hz	__	__
2-9	5 s	0.19998 Hz	_____	0.20002 Hz	__	__

Period Jitter

Scope Uncertainty factor _____

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
6.1a-1	50 ns		_____	20 ps	____	____
6.1a-2	500 ns		_____	65 ps	____	____
6.1b-1	20 ns		_____	15.2 ps	____	____

Test Results for Agilent 81101A Output Channel

Width

Scope Uncertainty factor _____

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
3-1	10.0 ns	9.250ns	_____	10.750 ns	____	____
3-2	50.0 ns	47.25 ns	_____	52.75 ns	____	____
3-3	100 ns	94.75 ns	_____	105.25 ns	____	____
3-4	500 ns	474.75 ns	_____	525.25 ns	____	____
3-5	50 µs	47.5 µs	_____	52.5 µs	____	____
3-6	5 ms	4.75 ms	_____	5.25 ms	____	____
3-7	500 ms	475 ms	_____	525 ms	____	____

Width Jitter

Scope Uncertainty factor _____

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
6.2-1	50 ns		_____	20 ps	____	____
6.2-2	500 ns		_____	65 ps	____	____

Delay

Scope Uncertainty factor _____

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
4-1	0.00 ns		_____	Fixed Delay	____	____
4-2	5.00 ns	3.75 ns	_____	6.25 ns	____	____
4-3	10 ns	8.50 ns	_____	11.50 ns	____	____
4-4	50.0 ns	46.5 ns	_____	53.5 ns	____	____
4-5	100 ns	94.0 ns	_____	106.0 ns	____	____
4-6	500 ns	474.0 ns	_____	526.0 ns	____	____
4-7	50 µs	47.5 µs	_____	52.5 µs	____	____
4-8	5 ms	4.75 ms	_____	5.25 ms	____	____
4-9	500 ms	475 ms	_____	525 ms	____	____

Delay Jitter

Scope Uncertainty factor _____

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
6.3-1	50 ns		_____	20 ps	____	____
6.3-2	500 ns		_____	65 ps	____	____

Double Pulse Delay

Scope Uncertainty factor _____

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
5-1	20.0 ns	18.50 ns	_____	21.50 ns	____	____
5-2	50.0ns	47.00 ns	_____	53.00 ns	____	____
5-3	100ns	94.50 ns	_____	105.50 ns	____	____

Counter Uncertainty factor _____

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
5-4	500 ms	475 ms	_____	525 ms	____	____
5-5	1 s	950.0 ms	_____	1050.0 ms	____	____

High Level 50Ω-50Ω

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
7.1-1	10.0 V	9.625 V	_____	10.375 V	____	____
7.1-2	5.0 V	4.775 V	_____	5.225 V	____	____
7.1-3	3.0V	2.845 V	_____	3.165 V	____	____
7.1-4	1.0 V	0.895 V	_____	1.105 V	____	____
7.1-5	0.5 V	410 mV	_____	590 mV	____	____
7.1-6	0.1 V	22 mV	_____	178 mV	____	____

High Level 1KΩ–50Ω

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
7.3-1	19.0 V	17.90V	_____	20.10 V	____	____
7.3-2	10.0 V	9.35 V	_____	10.65 V	____	____
7.3-3	5.0 V	4.60 V	_____	5.40 V	____	____
7.3-4	1.0 V	0.80 V	_____	1.20V	____	____
7.3-5	0.2 V	40 mV	_____	360mV	____	____

Low Level 50Ω-50Ω

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
7.2-1	-0.1 V	-22 mV	_____	-178 mV	____	____
7.2-2	-0.5 V	-410 mV	_____	-590 mV	____	____
7.2-3	-1.0 V	-0.895 V	_____	-1.105 V	____	____
7.2-4	-3.0V	-2.845 V	_____	-3.165 V	____	____
7.2-5	-5.0V	-4.775 V	_____	-5.225 V	____	____
7.2-6	-10.0V	-9.625 V	_____	-10.375 V	____	____

Low Level 1KΩ-50Ω

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
7.4-1	-0.2V	-40 mV	_____	-360 mV	____	____
7.4-2	-1.0V	-0.80 V	_____	-1.20 V	____	____
7.4-3	-5.0V	-4.60V	_____	-5.40 V	____	____
7.4-4	-10.0V	-9.350 V	_____	-10.650 V	____	____
7.4-5	-19.0V	-17.90 V	_____	-20.10 V	____	____

Leading Edge

Scope Uncertainty factor _____

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
8.1a-1	5.0 ns	≤5 ns	_____	5.7 ns	____	____
8.1a-2	10 ns	8.8 ns	_____	11.2 ns	____	____
8.1a-3	50 ns	44.8 ns	_____	55.2 ns	____	____
8.1a-4	500 ns	449.8 ns	_____	550.2 ns	____	____
8.1a-5	5 µs	4.4998 µs	_____	5.5002 µs	____	____
8.1a-6	50 µs	45 µs	_____	55 µs	____	____
8.1a-7	500 µs	450 µs	_____	550 µs	____	____
8.1a-8	50 ms	45 ms	_____	55 ms	____	____

Trailing Edge

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
8.1b-1	5.0 ns	≤5 ns	_____	5.7 ns	____	____
8.1b-2	10 ns	8.8 ns	_____	11.2 ns	____	____
8.1b-3	50 ns	44.8 ns	_____	55.2ns	____	____
8.1b-4	500 ns	449.8 n	_____	550.2 ns	____	____
8.1b-5	5 µs	4.4998 µs	_____	5.5002 µs	____	____
8.1b-6	50 µs	45 µs	_____	55 µs	____	____
8.1b-7	500 µs	450 µs	_____	550 µs	____	____
8.1b-8	50 ms	45 ms	_____	55 ms	____	____

Overshoot and Ringing

Scope Uncertainty factor _____

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
9-1	5V		_____	± 5% of ampl. ±20mV	____	____
9-2	500 mV		_____	±5% of ampl. ±20mV	____	____

Preshoot

TR Entry	Test	Limit Min	Actual Result	Limit Max	Pass	Fail
9-3	0 V		_____	±5% of ampl. ±20mV	____	____