Keysight 16800 Series
Portable Logic Analyzers

Quickly debug, validate, and optimize your digital system—
at a price that fits your budget

Data Sheet

KEYSIGHT TECHNOLOGIES

Features and Benefits

- 250 ps resolution (4 GHz) timing zoom to find elusive timing problems quickly, without double probing
- 15” display, with available touch screen, allows you to see more data and navigate quickly
- View Scope—time-correlated measurements and displays of your logic analyzer and oscilloscope data let you effectively track down problems across the analog and digital portions of your design
- Eight models with 34/68/102/136/204 channels, up to 32 M memory depth and models with a pattern generator provide the measurement flexibility for any budget
- Application support for every aspect of today’s complex designs—FPGA dynamic probe, digital VSA (vector signal analysis) and broad processor and bus support

Table of Contents

Selection Guide for 16800 Series Portable Logic Analyzers

Choose from eight models to get the measurement capability for your specific application.

Characteristic	16801A, 16821A [1]	16802A, 16822A [1]	16803A, 16823A [1]	16804A	16806A
Logic analyzer channels	34	68	102	136	204
Pattern generator channels [1]	48	48	48	N/A	N/A
High-speed timing zoom	4 GHz (250 ps) with 64 K depth	4 GHz (250 ps) with 64 K depth			
Maximum timing sample rate (Half/full ch)	1.0 GHz (1.0 ns)/500 MHz (2.0 ns)	1.0 GHz (1.0 ns)/500 MHz (2.0 ns)			
Maximum state clock rate	250 MHz with Option 250	450 MHz with Option 500			
		250 MHz with Option 250			
Maximum state data rate	250 Mb/s with Option 250	500 Mb/s with Option 500			
		250 Mb/s with Option 250			
Maximum memory depth (samples)	1 M with Option 001	1 M with Option 001			
	4 M with Option 004	4 M with Option 004			
	16 M with Option 016	16 M with Option 016			
	32 M with Option 032	32 M with Option 032			
Supported signal types	Single-ended	Single-ended			
Automated threshold/sample position	Yes	Yes			
Simultaneous eye diagrams, all channels					
Probe compatibility	40-pin cable connector	40-pin cable connector			

1. Pattern generator available with 16821A, 16822A and 16823A.

Probes are ordered separately. Please specify probes when ordering to ensure the correct connection between your logic analyzer, pattern generator, and the device under test.

Characteristic	16821A, 16822A, 16823A	
	Half channel	**Full channel**
Maximum clock	300 MHz	180 MHz
Data channels	24	48
Memory depth in vectors	16 M	8 M
Logic levels supported	5 V TTL, 3-state TTL, 3-state TTL/CMOS, 3-state 1.8 V, 3-state 2.5 V, 3-state 3.3 V, ECL, 5 V PECL, 3.3 V LVPECL, LVDS	

Models with a built-in pattern generator give you more measurement flexibility.

Logic Analysis for Tracking Real-time System Operation

Keysight 16800 Series portable logic analyzers offer the performance, applications, and usability your digital development team needs to quickly debug, validate, and optimize your digital system—at a price that fits your budget.

The logic analyzer's timing and state acquisition gives you the power to:

- Accurately measure precise timing relationships using 4 GHz (250 ps) timing zoom with 64 K depth.
- Find anomalies separated in time with memory depths upgradeable to 32 M.
- Buy what you need today and upgrade in the future. 16800 Series logic analyzers come with independent upgrades for memory depth and state speed.
- Sample synchronous buses accurately and confidently using eye finder. Eye finder automatically adjusts threshold and setup and hold to give you the highest confidence in measurements on high-speed buses.
- Track problems from symptom to root cause across several measurement modes by viewing time-correlated data in waveform/chart, listing, inverse assembly, source code, or compare display.
- Set up triggers quickly and confidently with intuitive, simple, quick, and advanced triggering. This capability combines new trigger functionality with an intuitive user interface.
- Access the signals that hold the key to your system's problems with the industry's widest range of probing accessories with capacitive loading down to 0.7 pF.
- Monitor and correlate multiple buses with split analyzer capability, which provides single and multibus support (timing, state, timing/state or state/state configurations).

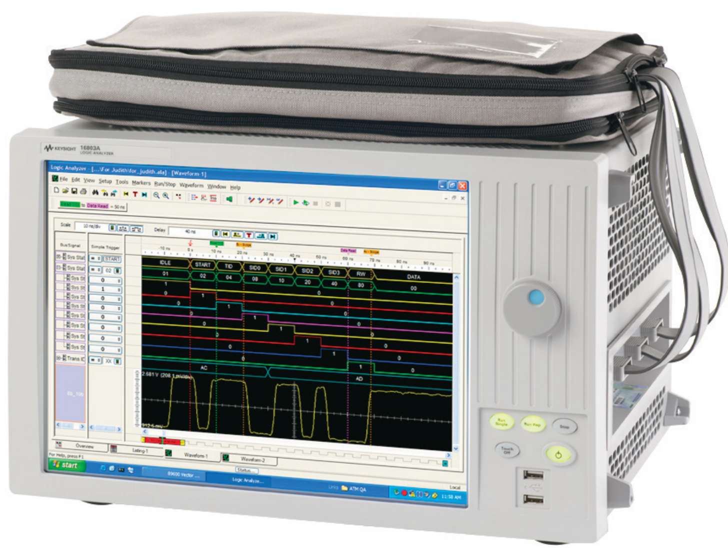


Figure 1. With eight models to choose from, you can get a logic analyzer with measurement capabilities that meet your needs.

Accurately measure precise timing relationships

16800 Series logic analyzers let you make accurate high-speed timing measurements with 4 GHz (250 ps) high-speed timing zoom. A parallel acquisition architecture provides high-speed timing measurements simultaneously through the same probe used for state or timing measurements. Timing zoom stays active all the time with no tradeoffs. View data at high resolution over longer periods of time with 64 K-deep timing zoom.

Logic Analysis for Tracking Real-time System Operation (Continued)

Automate measurement setup and quickly gain diagnostic clues

16800 Series logic analyzers make it easy for you to get up and running quickly by automating your measurement setup process. In addition, the logic analyzer's setup/hold window (or sampling position) and threshold voltage settings are automatically determined so you can capture data on high-speed buses with the highest accuracy. Auto Threshold and Sample Position mode allow you to...

- Obtain accurate and reliable measurements
- Save time during measurement setup
- Gain diagnostic clues and identify problem signals quickly
- Scan all signals and buses simultaneously or just a few
- View results as a composite display or as individual signals
- See skew between signals and buses
- Find and fix inappropriate clock thresholds
- Measure data valid windows
- Identify signal integrity problems related to rise times, fall times, data valid window widths

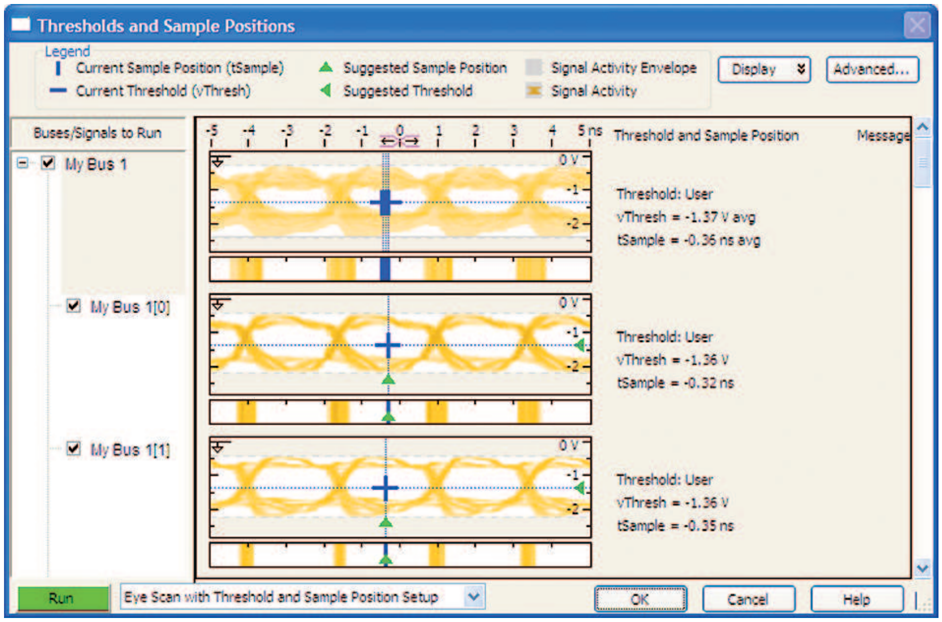


Figure 2. Identify problem signals quickly by viewing eye diagrams across all buses and signals simultaneously.

Identify problem signals over hundreds of channels simultaneously

As timing and voltage margins continue to shrink, confidence in signal integrity becomes an increasingly vital requirement in the design validation process. Eye scan lets you acquire signal integrity information on all the buses in your design, under a wide variety of operating conditions, in a matter of minutes. Identify problem signals quickly for further investigation with an oscilloscope. Results can be viewed for each individual signal or as a composite of multiple signals or buses.

Extend the life of your equipment

Easily upgrade your 16800 Series logic analyzer. "Turn on" additional memory depth and state speed when you need more. Purchase the capability you need now, then upgrade as your needs evolve.

Keysight 16800 Series Logic Analyzer Specifications and Characteristics

Channel count per measurement mode

	16801A/16821A	16802A/16822A	16803A/16823A	16804A	16806A
State analysis [1]	32 data + 2 clocks	64 data + 4 clocks	98 data + 4 clocks	132 data + 4 clocks	200 data + 4 clocks
Conventional timing	34	68	102	136	204
Transitional timing for sample rates < 500 MHz	34	68	102	136	204
Transitional timing for 500 MHz sample rate	–	34	68	102	170

1. Unused clock channels can be used as data channels.

Timing zoom (Simultaneous state and timing without double probing—All channels, all the time)

Timing analysis sample rate	4 GHz (250 ps)
Time interval accuracy	
– Within a pod pair	± (1.0 ns + 0.01% of time interval reading)
– Between pod pairs	± (1.75 ns +0.01% of time interval reading)
Memory depth	64 K samples
Trigger position	Start, center, end, or user-defined
Minimum data pulse width	1 ns

Other

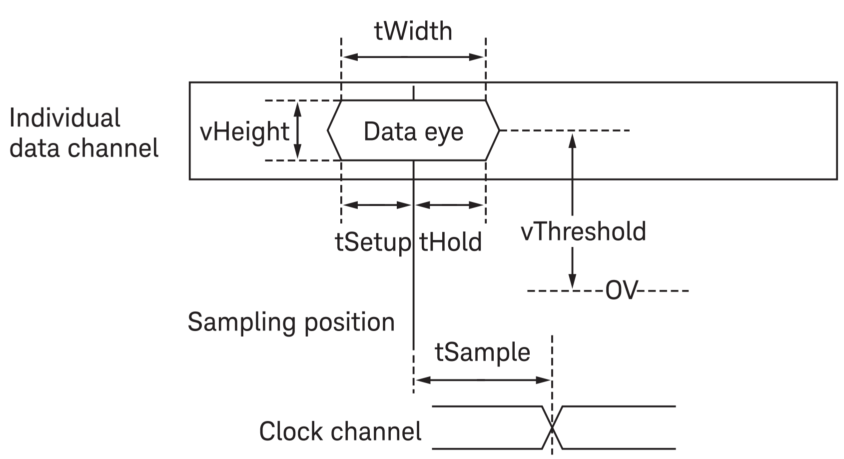
Voltage threshold	–5 V to 5 V (10 mV increments)
Threshold accuracy	± 50 mV + 1% of setting

Keysight 16800 Series Logic Analyzer Specifications and Characteristics (Continued)

State (synchronous) analysis mode	Option 250	Option 500 [3] (Available on 16802A, 16803A, 16804A, 16806A, 16822A and 16823A)
tWidth [*,1]	1.5 ns	1.5 ns
tSetup	0.5 tWidth	0.5 tWidth
tHold	0.5 tWidth	0.5 tWidth
tSample range [2]	–3.2 ns to +3.2 ns	–3.2 ns to +3.2 ns
tSample adjustment resolution	80 ps typical	80 ps typical
Maximum state data rate on each channel	250 Mb/s	500 Mb/s
Memory depth [4]	Option 001: 1 M samples	Option 001: 1 M samples
	Option 004: 4 M samples	Option 004: 4 M samples
	Option 016: 16 M samples	Option 016: 16 M samples
	Option 032: 32 M samples	Option 032: 32 M samples
Number of independent analyzers [5]	2 (1 for 16801A or 16821A)	1
Number of clocks [6]	4 (2 for 16801A or 16821A)	1
Number of clock qualifiers [6]	4 (2 for 16801A or 16821A)	N/A
Minimum time between active clock edges [*,7]	4.0 ns	2.0 ns
Minimum master-to-slave clock time	1 ns	N/A
Minimum slave-to-master clock time	1 ns	N/A
Minimum slave-to-slave clock time	4.0 ns	N/A
Minimum state clock pulse width		
– Single edge	1.0 ns	1.0 ns
– Multiple edge	1.0 ns	2.0 ns

* Items marked with an asterisk (*) are specifications. All others are characteristics. "Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

1. Minimum eye width in system under test.
2. Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.
3. Use of eye finder is recommended in 450 MHz and 500 Mb/s state mode.
4. In 250 Mb/s state mode, with all pods assigned, memory depth is half the maximum memory depth. With one pod pair (34 channels) unassigned, the memory depth is full. One pod pair (34 channels) must remain unassigned for time tags in 500 Mb/s state mode.
5. Independent analyzers may be either state or timing. When the 500 Mb/s state mode is selected, only one analyzer may be used.
6. In the 250 Mb/s state mode, the total number of clocks and qualifiers is 4 (2 for 16801A or 16821A).
7. Tested with input signal Vh = +1.3 V, Vl = +0.7 V, threshold = +1.0 V, tr/tf = 180 ps ± 30 ps (10%, 90%).



Keysight 16800 Series Logic Analyzer Specifications and Characteristics (Continued)

State (synchronous) analysis mode	Option 250	Option 500 (Available on 16802A, 16803A, 16804A, 16806A, 16822A and 16823A)
Clock qualifier setup time	500 ps	N/A
Clock qualifier hold time	0	N/A
Time tag resolution	2 ns	1.5 ns
Maximum time count between stored states	32 days	32 days
Maximum trigger sequence speed	250 MHz	500 MHz
Maximum trigger sequence levels	16	16
Trigger sequence level branching	Arbitrary 4-way if/then/else	2-way if/then/else
Trigger position	Start, center, end, or user-defined	Start, center, end, or user-defined
Trigger resources	– 16 patterns evaluated as =, =/, >, ≥, <, ≤ – 14 double-bounded ranges evaluated as in range, not in range – 1 timer for every 34 channels – 2 global counters – 1 occurrence counter per sequence level – 4 flags	– 14 patterns evaluated as =, =/, >, ≥, <, ≤ – 7 double-bounded ranges evaluated as in range, not in range – 1 occurrence counter per sequence level – 4 flags
Trigger resource conditions	Arbitrary Boolean combinations	Arbitrary Boolean combinations
Trigger actions	– Go To – Trigger, send e-mail, and fill memory – Trigger and Go To – Store/don't store sample – Turn on/off default storing – Timer start/stop/pause/resume – Global counter increment/decrement/reset – Occurrence counter reset – Flag set/clear	– Go To – Trigger and fill memory
Store qualification	Default (global) and per sequence level	Default (global)
Maximum global counter	2E+24	N/A
Maximum occurrence counter	2E+24	2E+24
Maximum pattern width	Smaller of 128 bits or maximum number of channels	Smaller of 128 bits or maximum number of channels
Maximum range width	Smaller of 64 bits or maximum number of channels	Smaller of 64 bits or maximum number of channels
Timers range	60 ns to 2199 seconds	N/A
Timer resolution	2 ns	N/A
Timer accuracy	± (5 ns +0.01%)	N/A
Timer reset latency	60 ns	N/A

Keysight 16800 Series Logic Analyzer Specifications and Characteristics (Continued)

Timing (asynchronous) analysis mode	Conventional timing	Transitional timing [2]
Sample rate on all channels	500 MHz	500 MHz
Sample rate in half channel mode	1 GHz	N/A
Number of independent analyzers [1]	2 (1 for 16801A or 16821A)	2 (1 for 16801A or 16821A)
Sample period (half channel)	1.0 ns	N/A
Minimum sample period (full channel)	2.0 ns	2.0 ns
Minimum data pulse width	1 sample period + 1.0 ns	1 sample period + 1.0 ns
Time interval accuracy	± (1 sample period + 1.25 ns + 0.01% of time interval reading)	± (1 sample period + 1.25 ns + 0.01% of time interval reading)
Memory depth in full channel mode	Option 001: 1 M samples	Option 001: 1 M samples
	Option 004: 4 M samples	Option 004: 4 M samples
	Option 016: 16 M samples	Option 016: 16 M samples
	Option 032: 32 M samples	Option 032: 32 M samples
Memory depth in half channel mode	Option 001: 2 M samples	N/A
	Option 004: 8 M samples	
	Option 016: 32 M samples	
	Option 032: 64 M samples	
Maximum trigger sequence speed	250 MHz	250 MHz
Maximum trigger sequence levels	16	16
Trigger sequence level branching	Arbitrary 4-way if/then/else	Arbitrary 4-way if/then/else
Trigger position	Start, center, end, or user-defined	Start, center, end, or use r-defined

1. Independent analyzers may be either state or timing. When the 500 Mb/s state mode is selected, only one analyzer may be used.
2. Transitional timing speed and memory depth are halved unless a spare pod pair (34 channels) is unassigned.

Keysight 16800 Series Logic Analyzer Specifications and Characteristics (Continued)

Timing (asynchronous) analysis mode	Conventional timing	Transitional timing
Trigger resources	– 16 patterns evaluated as =, =/, >, ≥, <, ≤ – 14 double-bounded ranges evaluated as in range, not in range – 3 edge/glitch – 1 timer for every 34 channels (no timer for 16801A or 16821A) – 2 global counters – 1 occurrence counter per sequence level – 4 flags	– 15 patterns evaluated as =, =/, >, ≥, <, ≤ – 14 double-bounded ranges evaluated as in range, not in range – 3 edge/glitch – 1 timer for every 34 channels (no timer for 16801A or 16821A) – 2 global counters – 1 occurrence counter per sequence level – 4 flags
Trigger resource conditions	Arbitrary Boolean combinations	Arbitrary Boolean combinations
Trigger actions	– Go To – Trigger, send e-mail, and fill memory – Trigger and Go To – Turn on/off default storing – Timer start/stop/pause/resume – Global counter increment/decrement/reset – Occurrence counter reset – Flag set/clear	– Go To – Trigger, send e-mail, and fill memory – Trigger and Go To – Turn on/off default storing – Timer start/stop/pause/resume – Global counter increment/decrement/reset – Occurrence counter reset – Flag set/clear
Maximum global counter	2E+24	2E+24
Maximum occurrence counter	2E+24	2E+24
Maximum range width	32 bits	32 bits
Maximum pattern width	Smaller of 128 bits or maximum number of channels	Smaller of 128 bits or maximum number of channels
Timer value range	60 ns to 2199 seconds	60 ns to 2199 seconds
Timer resolution	2 ns	2 ns
Timer accuracy	± (5 ns +0.01%)	± (5 ns +0.01%)
Greater than duration	4.0 ns to 67 ms in 4.0 ns increments	4.0 ns to 67 ms in 4.0 ns increments
Less than duration	8.0 ns to 67 ms in 4.0 ns increments	8.0 ns to 67 ms in 4.0 ns increments
Timer reset latency	60 ns	60 ns

A Built-in Pattern Generator Gives You Digital Stimulus and Response in a Single Instrument

Selected 16800 Series models (16821A, 16822A and 16823A) also include a 48-channel pattern generator to drive down risk early in product development. With a pattern generator you can:

- Substitute for missing boards, integrated circuits (ICs) or buses instead of waiting for missing pieces
- Write software to create infrequently encountered test conditions and verify that the code works – before complete hardware is available
- Generate patterns necessary to put a circuit in a desired state, operate the circuit at full speed or step the circuit through a series of states
- Create a circuit initialization sequence

Keysight 16800 Series portable logic analyzers with a pattern generator offer a variety of features that make it easier for you to create digital stimulus tests.

Vectors up to 48 bits wide

Vectors are defined as a “row” of labeled data values, with each data value from one to 48 bits wide. Each vector is output on the rising edge of the clock. Create stimulus patterns for the widest buses in your system.

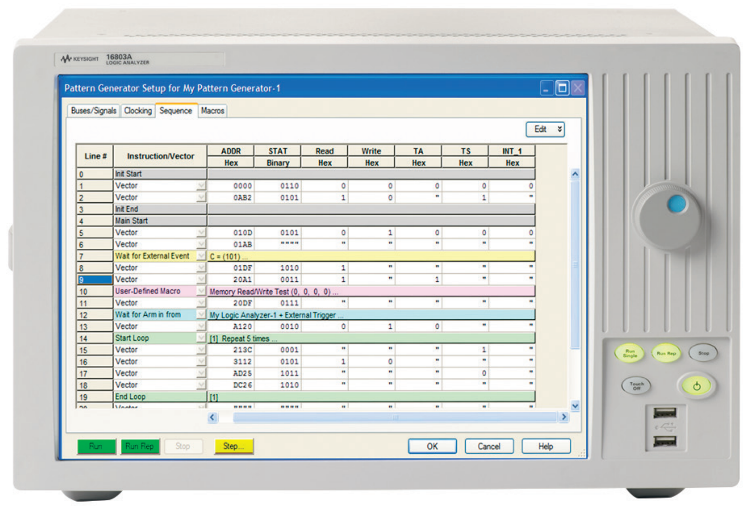


Figure 3. Models with a built-in pattern generator give you more measurement flexibility.

Depth up to 16 M vectors

With the pattern generator, you can load and run up to 16 M vectors of stimulus. Depth on this scale is most useful when coupled with powerful stimulus generated by electronic design automation tools, such as SynaptiCAD’s WaveFormer and VeriLogger. These tools create stimulus using a combination of graphically drawn signals, timing parameters that constrain edges, clock signals, and timing and Boolean equations for describing complex signal behavior. The stimulus also can be created from design simulation waveforms. The SynaptiCAD tools allow you to convert .VCD files into .PGB files directly, offering you an integrated solution that saves you time.

Synchronized clock output

You can output data synchronized to either an internal or external clock. The external clock is input via a clock pod, and has no minimum frequency (other than a 2 ns minimum high time).

The internal clock is selectable between 1 MHz and 300 MHz in 1-MHz steps. A Clock Out signal is available from the clock pod and can be used as an edge strobe with a variable delay of up to 8 ns.

Initialize (INIT) block for repetitive runs

When running repetitively, the vectors in the initialize (init) sequence are output only once, while the main sequence is output as a continually repeating sequence. This “init” sequence is very useful when the circuit or subsystem needs to be initialized. The repetitive run capability is especially helpful when operating the pattern generator independent of the logic analyzer.

“Send Arm out to...” coordinates activity with the logic analyzer

Verify how your system responds to a specific stimulus sequence by arming the logic analyzer from the pattern generator. A “Send Arm out to...” instruction acts as a trigger arming event for the logic analyzer or other test equipment to begin measurements. Arm setup and trigger setup of the logic analyzer determines the action initiated by “Send Arm out to... .”

A Built-in Pattern Generator Gives You Digital Stimulus and Response in a Single Instrument (Continued)

"Wait for External Event..." for input pattern

The clock pod also accepts a 3-bit input pattern. These inputs are level-sensed so that any number of "Wait for External Event" instructions can be inserted into a stimulus program. Up to four pattern conditions can be defined from the OR-ing of the eight possible 3-bit input patterns. A "Wait for External Event" also can be defined to wait for an Arm. This Arm signal can come from the logic analyzer. "Wait for External Event..." allows you to execute a specific stimulus sequence only when the defined external event occurs.

Simplify creation of stimulus programs with user-defined macros and loops

User macros permit you to define a pattern sequence once, then insert the macro by name wherever it is needed. Passing parameters to the macro will allow you to create a more generic macro. For each call to the macro you can specify unique values for the parameters.

Loops enable you to repeat a defined block of vectors for a specified number of times. Loops and macros can be nested, except that a macro cannot be nested within another macro. At compile time, loops and macros are expanded in memory to a linear sequence.

Convenient data entry and editing feature

You can conveniently enter patterns in hex, octal, binary, decimal, and signed decimal (two's complement) bases. To simplify data entry, you can view the data associated with an individual label with multiple radixes. Delete, Insert, and Copy commands are provided for easy editing. Fast and convenient Pattern Fills give the programmer useful test patterns with a few key strokes. Fixed, Count, Rotate, Toggle, and Random patterns are available to help you quickly create a test pattern, such as "walking ones." Pattern parameters, such as step size and repeat frequency, can be specified in the pattern setup.

ASCII input file format: your design tool connection

The pattern generator supports an ASCII file format to facilitate connectivity to other tools in your design environment. Because the ASCII format does not support the instructions listed earlier, they cannot be edited into the ASCII file. User macros and loops also are not supported, so the vectors need to be fully expanded in the ASCII file. Many design tools will generate ASCII files and output the vectors in this linear sequence. Data must be in hex format, and each label must represent a set of contiguous output channels.

Configuration

The pattern generator operates with the clock pods, data pods, and lead sets described later in this document. At least one clock pod and one data pod must be selected to configure a functional system. You can select from a variety of pods to provide the signal source needed for your logic devices. The data pods, clock pods and data cables use standard connectors. The electrical characteristics of the data cables are described for users with specialized applications who want to avoid the use of a data pod.

Direct connection to your target system

You can connect the pattern generator pods directly to a standard connector on your target system. Use a 3M brand #2520 Series or similar connector. The clock or data pods will plug right in. Short, flat cable jumpers can be used if the clearance around the connector is limited. Use a 3M #3365/20, or equivalent, ribbon cable; a 3M #4620 Series or equivalent connector on the pattern generator pod end of the cable, and a 3M #3421 Series or equivalent connector at your target system end of the cable.

Probing accessories

The probe tips of the Keysight 10474A, 10347A, 10498A, and E8142A lead sets plug directly into any 0.1-inch grid with 0.026-inch to 0.033-inch diameter round pins or 0.025-inch square pins. These probe tips work with the Keysight 5090-4356 surface mount grabbers and with the Keysight 5959-0288 through-hole grabbers, providing compatibility with industry standard pins.

Pattern Generator Specifications and Characteristics (16821A, 16822A, and 16823A)

Pattern generator characteristics	
Maximum memory depth	16 MVectors
Number of output channels at > 180 MHz and ≤ 300 MHz clock	24
Number of output channels at ≤ 180 MHz clock	48
Number of different macros	Limited only by the pattern generator's available memory depth
Maximum number of lines in a macro	Limited only by the pattern generator's available memory depth
Maximum number of parameters in a macro	Limited only by the pattern generator's available memory depth
Maximum number of macro invocations	Limited only by the pattern generator's available memory depth
Maximum loop count in a repeat loop	Limited only by the pattern generator's available memory depth
Maximum number of repeat loop invocations	1000
Maximum number of "Wait" event patterns	4
Number of input lines to define a pattern	3
Maximum width of a label	48 bits
Maximum number of labels	Limited only by system memory
Maximum number of vectors in all formats	16 MVectors
Minimum number of vectors in binary format when loading into hardware	4096

Lead set characteristics	
Keysight 10474A 8-channel probe lead set [1]	Provides most cost effective lead set for clock and data pods. Grabbers are not included. Lead wire length is 12 inches.
Keysight 10347A 8-channel probe lead set	Provides 50 Ω coaxial lead set for unterminated signals, required for 10465A ECL Data Pod (unterminated). Grabbers are not included.
Keysight 10498A 8-channel probe lead set [1]	Provides most cost effective lead set for clock and data pods. Grabbers are not included. Lead wire length is 6 inches.
Keysight E8142A 8-channel probe lead set	Provides lead set for LVDS clock and data pods. Grabbers are not included. Lead wire length is 6 inches.

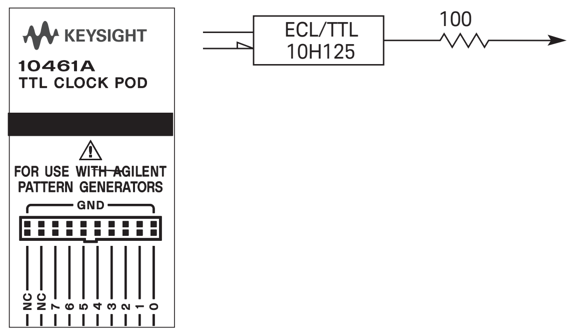
1. For all clock and data pods except 10465A unterminated ECL Data Pod and E8140A/E8141A clock and data pods.

Pattern Generator Specifications and Characteristics (16821A, 16822A, and 16823A) (Continued)

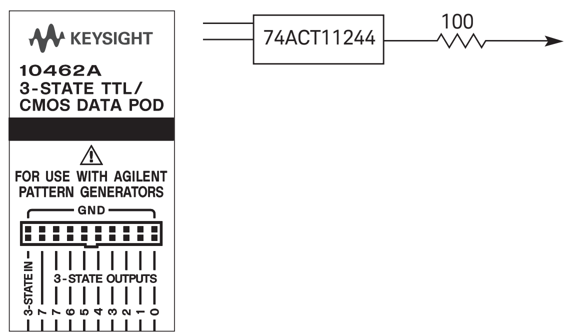
Data pod characteristics

Note: Data pod output parametrics depend on the output driver and the impedance load of the target system. Check the device data book for the specific drivers listed for each pod.

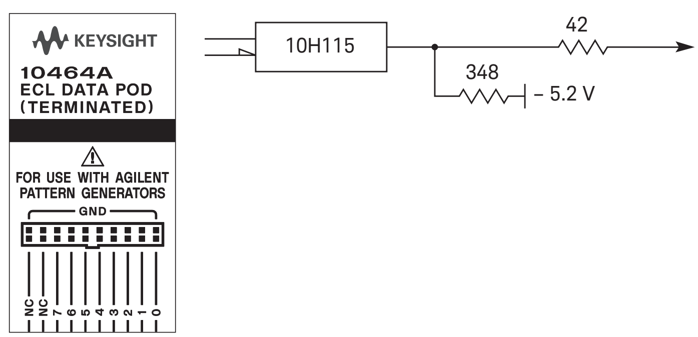
Keysight 10461A TTL data pod	
Output type	10H125 with 100 Ω series
Maximum clock	200 MHz
Skew [1]	Typical < 2 ns; worst case = 4 ns
Recommended lead set	Keysight 10474A



Keysight 10462A 3-state TTL/CMOS data pod	
Output type	74ACT11244 with 100 Ω series; 10H125 on non 3-state channel 7 [2]
3-state enable	Negative true, 100 KΩ to GND, enabled on no connect
Maximum clock	100 MHz
Skew [1]	Typical < 4 ns; worst case = 12 ns
Recommended lead set	Keysight 10474A



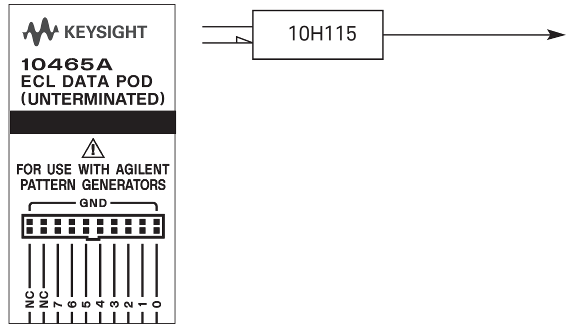
Keysight 10464A ECL data pod (terminated)	
Output type	10H115 with 330 Ω pulldown, 47 Ω series
Maximum clock	300 MHz
Skew [1]	Typical < 1 ns; worst case = 2 ns
Recommended lead set	Keysight 10474A



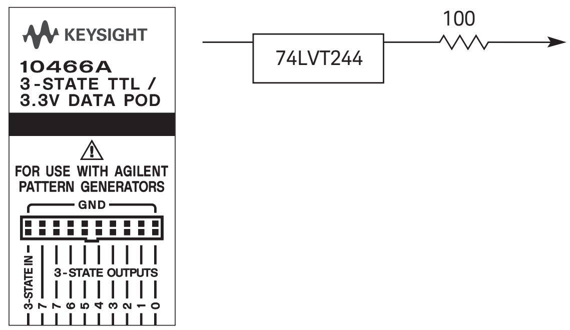
1. Typical skew measurements made at pod connector with approximately 10 pF/50 KΩ load to GND; worst case skew numbers are a calculation of worst case conditions through circuits. Both numbers apply to any channel within the pattern generator.
2. Channel 7 on the 3-state pods has been brought out in parallel as a non 3-state signal. By looping this output back into the 3-state enable line, the channel can be used as a 3-state enable.

Pattern Generator Specifications and Characteristics (16821A, 16822A, and 16823A) (Continued)

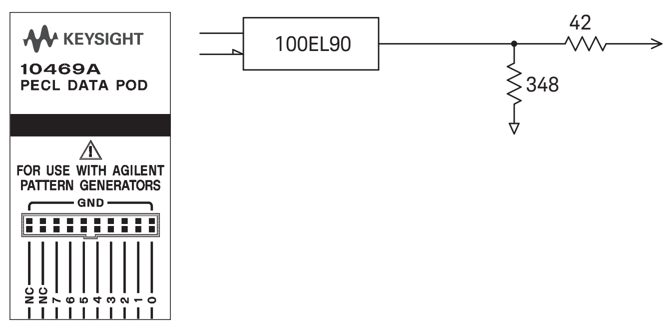
Keysight 10465A ECL data pod (unterminated)	
Output type	10H115 (no termination)
Maximum clock	300 MHz
Skew [1]	Typical < 1 ns; worst case = 2 ns
Recommended lead set	Keysight 10347A



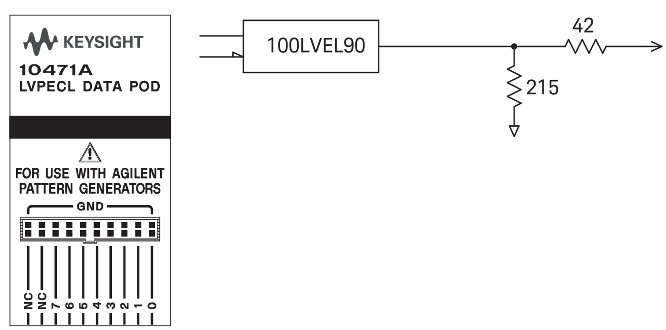
Keysight 10466A 3-state TTL/3.3 volt data pod	
Output type	74LVT244 with 100 Ω series; 10H125 on non 3-state channel 7 [2]
3-state enable	Negative true, 100 KΩ to GND, enabled on no connect
Maximum clock	200 MHz
Skew [1]	Typical < 3 ns; worst case = 7 ns
Recommended lead set	Keysight 10474A



Keysight 10469A 5 volt PECL data pod	
Output type	100EL90 (5 V) with 348 ohm pulldown to ground and 42 ohm in series
Maximum clock	300 MHz
Skew [1]	Typical < 500 ps; worst case = 1 ns
Recommended lead set	Keysight 10498A



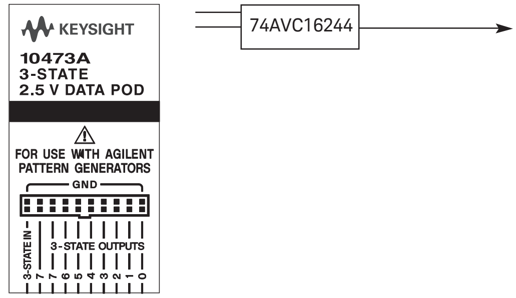
Keysight 10471A 3.3-volt LVPECL data pod	
Output type	100LVEL90 (3.3 V) with 215 Ω pulldown to ground and 42 Ω in series
Maximum clock	300 MHz
Skew [1]	Typical < 500 ps; worst case = 1 ns
Recommended lead set	Keysight 10498A



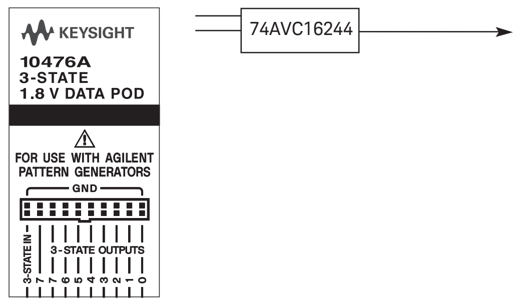
1. Typical skew measurements made at pod connector with approximately 10 pF/50 KΩ load to GND; worst case skew numbers are a calculation of worst case conditions through circuits. Both numbers apply to any channel within the pattern generator.
2. Channel 7 on the 3-state pods has been brought out in parallel as a non 3-state signal. By looping this output back into the 3-state enable line, the channel can be used as a 3-state enable.

Pattern Generator Specifications and Characteristics (16821A, 16822A, and 16823A) (Continued)

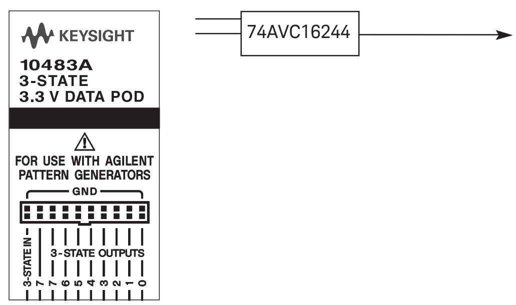
Keysight 10473A 3-state 2.5-volt data pod	
Output type	74AVC16244
3-state enable	Negative true, 38 KΩ to GND, enabled on no connect
Maximum clock	300 MHz
Skew [1]	Typical < 1.5 ns; worst case = 2 ns
Recommended lead set	Keysight 10498A



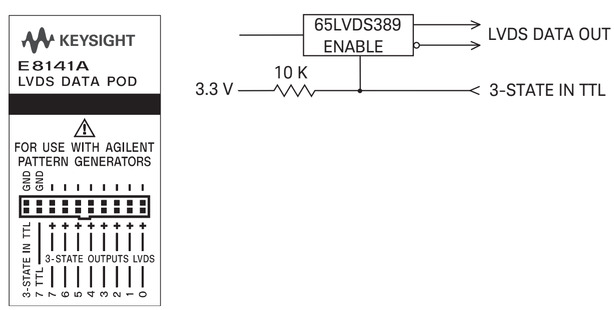
Keysight 10476A 3-state 1.8-volt data pod	
Output type	74AVC16244
3-state enable	Negative true, 38 KΩ to GND, enabled on no connect
Maximum clock	300 MHz
Skew [1]	Typical < 1.5 ns; worst case = 2 ns
Recommended lead set	Keysight 10498A



Keysight 10483A 3-state 3.3-volt data pod	
Output type	74AVC16244
3-state enable	Negative true, 38 KΩ to GND, enabled on no connect
Maximum clock	300 MHz
Skew [1]	Typical < 1.5 ns; worst case = 2 ns
Recommended lead set	Keysight 10498A



Keysight E8141A LVDS data pod	
Output type	65LVDS389 (LVDS data lines) 10H125 (TTL non-3-state channel 7)
3-state enable	Positive true TTL; no connect=enabled
Maximum clock	300 MHz
Skew	Typical < 1 ns; worst case = 2 ns
Recommended lead set	E8142A

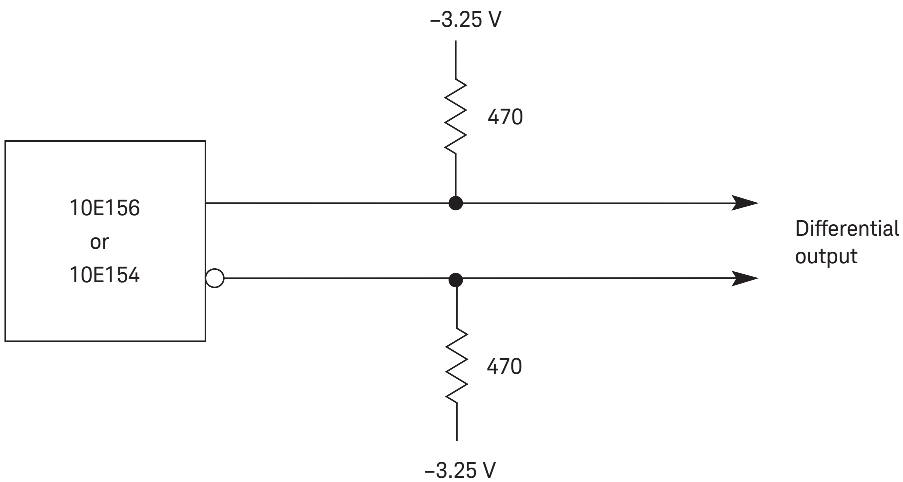


1. Typical skew measurements made at pod connector with approximately 10 pF/50 KΩ load to GND; worst case skew numbers are a calculation of worst case conditions through circuits. Both numbers apply to any channel within the pattern generator.

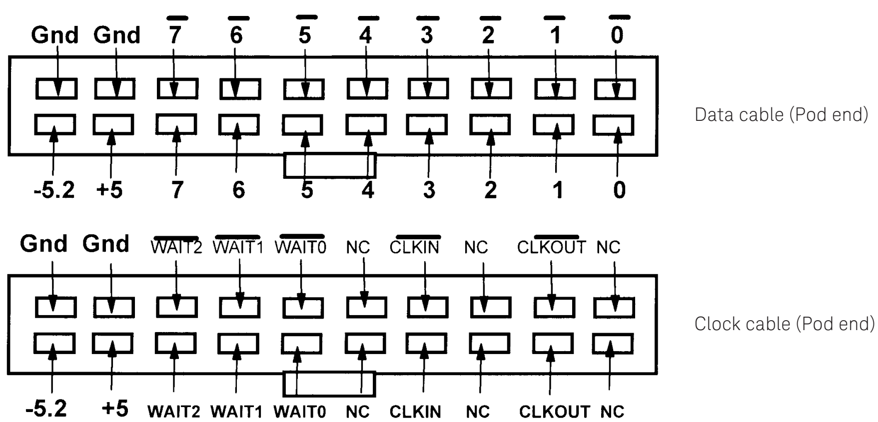
Pattern Generator Specifications and Characteristics (16821A, 16822A, and 16823A) (Continued)

Data cable characteristics without a data pod

The pattern generator data cables without a data pod provide an ECL terminated (1 KΩ to –5.2 V) differential signal (from a type 10E156 or 10E154 driver). These are usable when received by a differential receiver, preferably with a 100 Ω termination across the lines. These signals should not be used single ended due to the slow fall time and shifted voltage threshold (they are not ECL compatible).



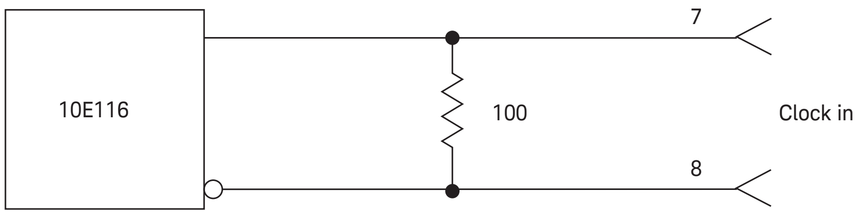
Pattern generator cable pin outs

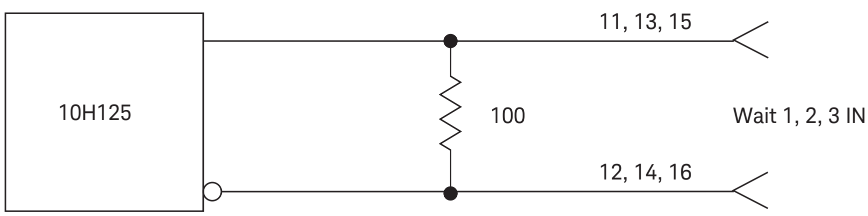


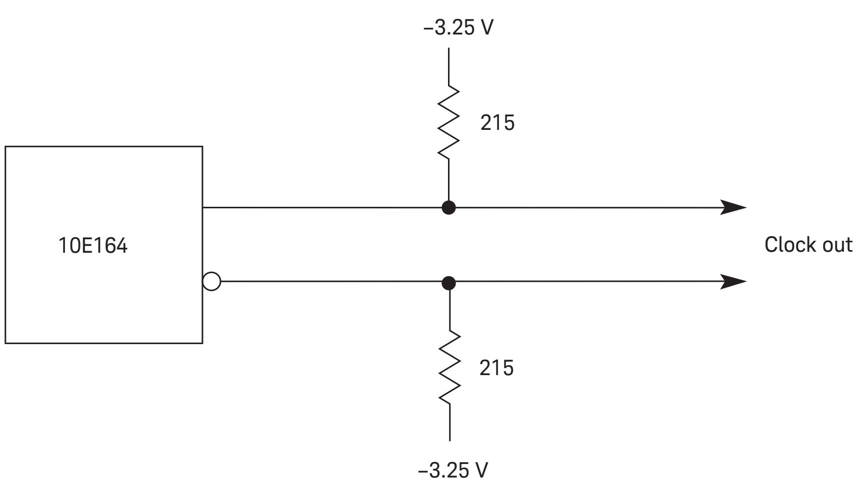
Pattern Generator Specifications and Characteristics (16821A, 16822A, and 16823A) (Continued)

Clock cable characteristics without a clock pod

The pattern generator clock cables without a clock pod provide an ECL terminated (1 KΩ to –5.2 V) differential signal (from a type 10E164 driver). These are usable when received by a differential receiver, preferably with a 100 Ω termination across the lines. These signals should not be used single ended due to the slow fall time and shifted voltage threshold (they are not ECL compatible).



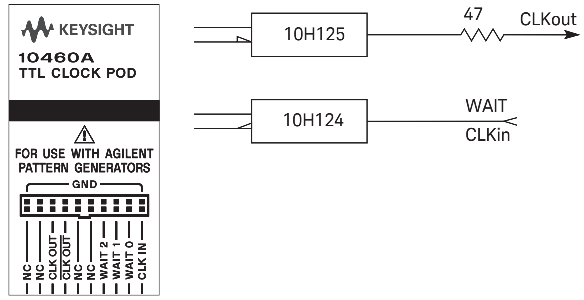




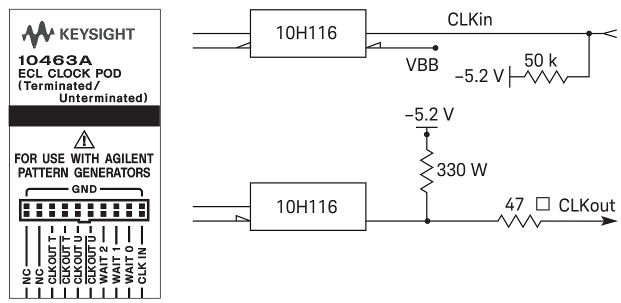
Pattern Generator Specifications and Characteristics (16821A, 16822A, and 16823A) (Continued)

Clock pod characteristics

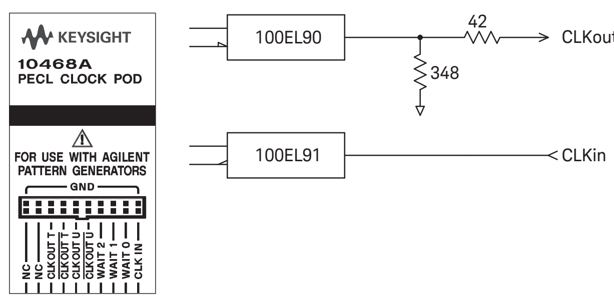
10460A TTL clock pod	
Clock output type	10H125 with 47 Ω series; true and inverted
Clock output rate	100 MHz maximum
Clock out delay	Approximately 8 ns total in 14 steps
Clock input type	TTL – 10H124
Clock input rate	DC to 100 MHz
Pattern input type	TTL – 10H124 (no connect is logic 1)
Clock-in to clock-out	Approximately 30 ns
Pattern-in to recognition	Approximately 15 ns + 1 clk period
Recommended lead set	Keysight 10474A



10463A ECL clock pod	
Clock output type	10H116 differential unterminated; and differential with 330 Ω to –5.2 V and 47 Ω series
Clock output rate	300 MHz maximum
Clock out delay	Approximately 8 ns total in 14 steps
Clock input type	ECL – 10H116 with 50 KΩ to –5.2 V
Clock input rate	DC to 300 MHz
Pattern input type	ECL – 10H116 with 50 KΩ (no connect is logic 0)
Clock-in to clock-out	Approximately 30 ns
Pattern-in to recognition	Approximately 15 ns + 1 clk period
Recommended lead set	Keysight 10474A

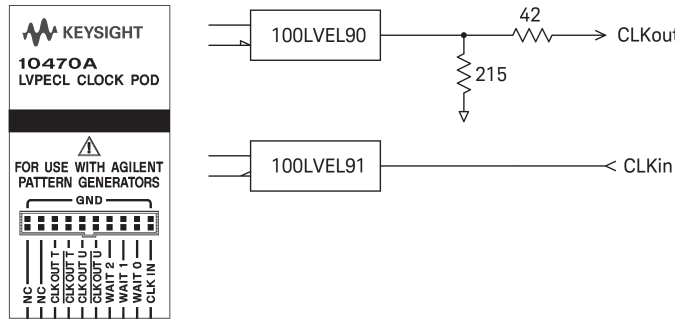


10468A 5-volt PECL clock pod	
Clock output type	100EL90 (5 V) with 348 Ω pulldown to ground and 42 Ω in series
Clock output rate	300 MHz maximum
Clock out delay	Approximately 8 ns total in 14 steps
Clock input type	100EL91 PECL (5 V), no termination
Clock input rate	DC to 300 MHz
Pattern input type	100EL91 PECL (5 V), no termination (no connect is logic 0)
Clock-in to clock-out	Approximately 30 ns
Pattern-in to recognition	Approximately 15 ns + 1 clk period
Recommended lead set	Keysight 10498A

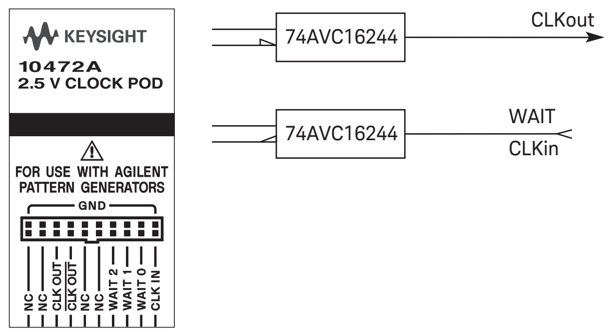


Pattern Generator Specifications and Characteristics (16821A, 16822A, and 16823A) (Continued)

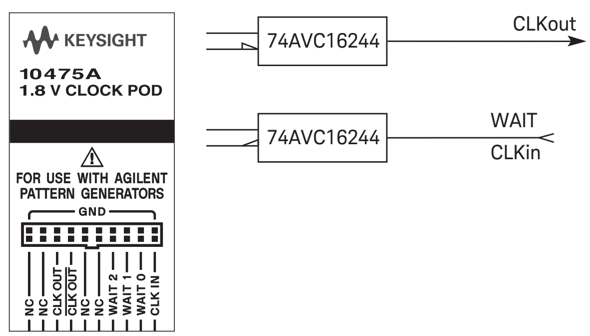
10470A 3.3-volt LVPECL clock pod	
Clock output type	100LVEL90 (3.3 V) with 215 Ω pulldown to ground and 42 Ω in series
Clock output rate	300 MHz maximum
Clock out delay	Approximately 8 ns total in 14 steps
Clock input type	100LVEL91 LVPECL (3.3 V), no termination
Clock input rate	DC to 300 MHz
Pattern input type	100LVEL91 LVPECL (3.3 V), no termination (no connect is logic 0)
Clock-in to clock-out	Approximately 30 ns
Pattern-in to recognition	Approximately 15 ns + 1 clk period
Recommended lead set	Keysight 10498A



10472A 2.5-volt clock pod	
Clock output type	74AVC16244
Clock output rate	200 MHz maximum
Clock out delay	Approximately 8 ns total in 14 steps
Clock input type	74AVC16244 (3.6 V max)
Clock input rate	DC to 200 MHz
Pattern input type	74AVC16244 (3.6 V max; no connect is logic 0)
Clock-in to clock-out	Approximately 30 ns
Pattern-in to recognition	Approximately 15 ns + 1 clk period
Recommended lead set	Keysight 10498A

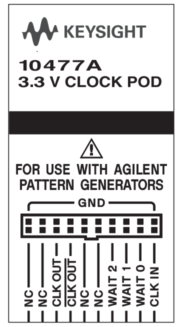


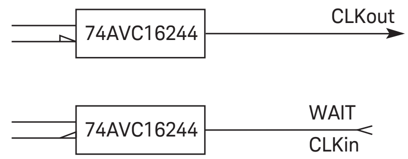
10475A 1.8-volt clock pod	
Clock output type	74AVC16244
Clock output rate	200 MHz maximum
Clock out delay	Approximately 8 ns total in 14 steps
Clock input type	74AVC16244 (3.6 V max)
Clock input rate	DC to 200 MHz
Pattern input type	74AVC16244 (3.6 V max; no connect is logic 0)
Clock-in to clock-out	Approximately 30 ns
Pattern-in to recognition	Approximately 15 ns + 1 clk period
Recommended lead set	Keysight 10498A



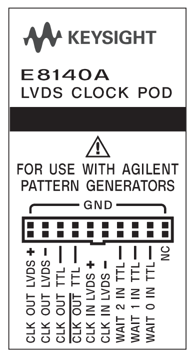
Pattern Generator Specifications and Characteristics (16821A, 16822A, and 16823A) (Continued)

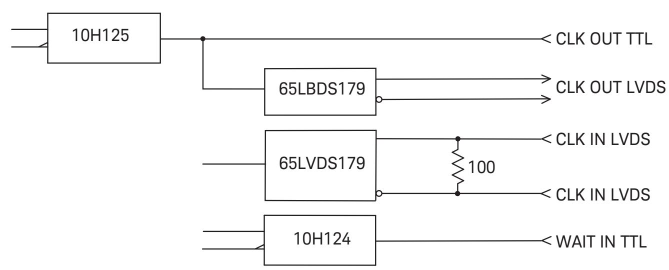
10477A 3.3-volt clock pod	
Clock output type	74AVC16244
Clock output rate	200 MHz maximum
Clock out delay	Approximately 8 ns total in 14 steps
Clock input type	74AVC16244 (3.6 V max)
Clock input rate	DC to 200 MHz
Pattern input type	74AVC16244 (3.6 V max; no connect is logic 0)
Clock-in to clock-out	Approximately 30 ns
Pattern-in to recognition	Approximately 15 ns + 1 clk period
Recommended lead set	Keysight 10498A





E8140A LVDS clock pod	
Clock output type	65LVDS179 (LVDS) and 10H125 (TTL)
Clock output rate	200 MHz maximum (LVDS and TTL)
Clock out delay	Approximately 8 ns total in 14 steps
Clock input type	65LVDS179 (LVDS with 100 Ω)
Clock input rate	DC to 150 MHz (LVDS)
Pattern input type	10H124 (TTL) (no connect = logic 1)
Clock-in to clock-out	Approximately 30 ns
Pattern-in to recognition	Approximately 15 ns + 1 clk period
Recommended lead set	Keysight 10498A





Unleash the Complementary Power of a Logic Analyzer and an Oscilloscope

Seamless scope integration with View Scope

Easily make time-correlated measurements between Keysight logic analyzers and oscilloscopes. The time-correlated logic analyzer and oscilloscope waveforms are integrated into a single logic analyzer waveform display for easy viewing and analysis. You can also trigger the oscilloscope from the logic analyzer (or vice versa), automatically de-skew the waveforms and maintain marker tracking between the two instruments. Perform the following more effectively:

- Validate signal integrity
- Track down problems caused by signal integrity
- Validate correct operation of A/D and D/A converters
- Validate correct logical and timing relationships between the analog and digital portions of a design

Connection

The Keysight logic analyzer and oscilloscope can be physically connected with standard BNC and LAN connections. Two BNC cables are connected for cross triggering, and the LAN connection is used to transfer data between the instruments. The View Scope correlation software is standard in the logic analyzer's application software version 3.50 or higher. The View Scope software includes:

- Ability to import some or all of the captured oscilloscope waveforms
- Auto scaling of the scope waveforms for the best fit in the logic analyzer display

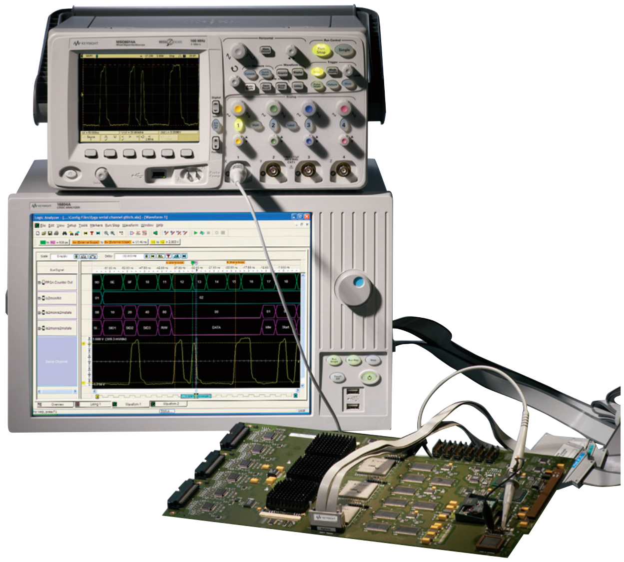


Figure 4. View Scope seamlessly integrates your scope and logic analyzer waveforms into a single display.

Feature	Benefit
Automated setup	Quickly get to your first measurement using the logic analyzer's Help wizard for easy setup, regardless of which supported Keysight oscilloscope you connect to.
Integrated waveform display	Instantly validate the logical and timing relationships between the analog and digital portions of your design. View oscilloscope and logic analyzer waveforms integrated into a single logic analyzer waveform display.
Automatic measurement de-skew	Save time and gain confidence in measurement results with measurements that are automatically de-skewed in time.
Cross trigger the logic analyzer and oscilloscope	Start your debug approach from either the analog or digital domain with the flexibility to trigger the oscilloscope from the logic analyzer (or vice versa).
Tracking markers	Precisely relate information on the oscilloscope's display to the corresponding point in time on the logic analyzer display with tracking markers. The oscilloscope's time markers automatically track adjustments of the logic analyzer's global markers.

Table 1. Key features and benefits of integrating Keysight oscilloscope and logic analyzer capabilities.

Compatibility	
Keysight logic analyzers	16800 Series portable logic analyzers
	16900 Series modular logic analysis systems
Keysight oscilloscopes	InfiniiVision 2000 X-Series, 3000 X-Series, 5000 Series, 6000 Series, 7000 Series
	Infiniium 9000 Series, 90000A Series, 90000 X-Series, 90000 Q-Series

Get Instant Insights into your Design with Multiple Views and Analysis Tools

Acquisition and analysis tools provide rapid insight into your toughest debug problems

You have unique measurement and analysis needs. When you want to understand what your target is doing and why, you need acquisition and analysis tools that rapidly consolidate data into displays that provide insight into your system's behavior.

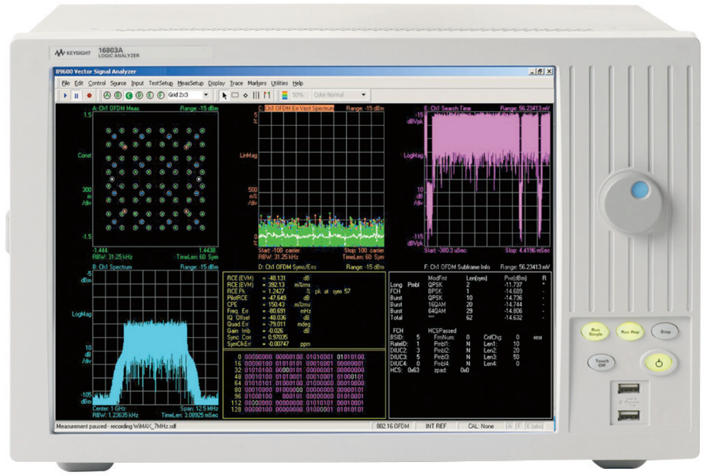


Figure 5. Perform in-depth time, frequency and modulation domain analysis on your digital baseband and IF signals with Keysight's 89600 Vector Signal Analysis software.

Optional analysis and automated measurement packages	
B4655A FPGA dynamic probe	Gain unprecedented visibility into your FPGA's internal activity. Make incremental real-time measurements in seconds without stopping the FPGA, changing the design or modifying design timing. Quickly set up the logic analyzer with automatic pin mapping and signal bus naming by leveraging work you did in your design environment. www.keysight.com/find/fpga
89601A-300 digital vector signal analysis, hardware connectivity for logic analyzers	Perform time-domain, spectrum, and modulation quality analysis on digital Baseband and IF signals. www.keysight.com/find/dvsa
B4601C serial-to-parallel analysis package	Eliminate the tedious, time-consuming, and error-prone task of sifting through thousands of analysis package serial bits by looking at long vertical columns of captured 1's and 0's. The B4601C serial-to-parallel analysis package is general-purpose software that allows easy viewing and analysis of serial data.
B4606A advanced customization environment–development and runtime package	Tailor your logic analyzer interface with a wide range of control, analysis and display capabilities specific to your measurement application. Create integrated dialogs, graphical displays and analysis functions to quickly manipulate measurement data into a format that provides additional insight and answers. www.keysight.com/find/logic-customview
B4607A advanced customization environment–runtime package	Run the macros and graphical views created with a B4606A development package or obtain and run a variety of commonly requested tools from Keysight and it's partners to help customize your measurement environment.
B4608A ASCII remote programming interface	Remotely control a 16900-, 16800-, 1680-, or 1690-Series logic analysis system by issuing ASCII commands. This interface is designed to be as similar as possible to the RPI on the 16700 Series logic analysis system, so that you can reuse existing programs. Requires either B4606A or B4607A to be enabled. You can also use the B4606A to customize and add RPI commands.
B4610A data import package	Use the logic analyzer GUI to view data obtained from tools other than a logic analyzer.
B4630A MATLAB connectivity and analysis package	Make an easy connection to MATLAB and transfer your logic analyzer measurement data for processing. Display the results on the logic analyzer in an XY scattergram chart.

Get Instant Insights into your Design with Multiple Views and Analysis Tools (Continued)

Save time analyzing your unique design with a turnkey setup

Keysight and our partners provide an extensive range of bus and processor analysis probes. They provide non-intrusive, full-speed, real-time analysis to accelerate your debugging process.

- Save time making bus- and processor-specific measurements with application specific analysis probes that quickly and reliably connect to your device under test.
- Display processor mnemonics or bus cycle decode.
- Get support for a comprehensive list of industry-standard processors and buses.

Available device support

Microprocessors/microcontrollers	FPGAs	I/O buses	Memory buses	Serial buses	Graphics buses
AMD, Analog Devices, ARM, AT&T, Dallas, DEC, Freescale, GTE, IBM, IDT, Infineon, Intel, LSI Logic, McDonnell Douglas, MIPS, Motorola, National, NEC, PACE, PMC Sierra/QED, Rockwell, Siemens, Texas Instruments, Toshiba, Zilog	Xilinx Kintex 7, Virtex 7, Virtex 6, Spartan 6, Virtex 5, Virtex 4, Altera Cyclone IV, Stratix IV GX, Arria II GX	PCI, PCI Express®, Serial ATA (SATA 1 and 2), SCSI, Serial Attached SCSI (SAS)	DDR1, DDR2, PC-100/133, GDDR3, Fully Buffered DIMM (FB-DIMM), Rambus	Fibre Channel, I^2C, IEEE-1394, Serial ATA (SATA 1 and 2), USB 2.0/1.1, PCI Express, RS-232, CAN, IEEE-488	AGP2x, AGP4x, AGP3.0, PCI Express

16800 Series Instrument Characteristics

Standard data views	
Waveform	Integrated display of data as digital waveforms, analog waveforms imported from an external oscilloscope, and/or as a chart of a bus' values over time
Listing	Displays data as a state listing
Compare	Compares data from different acquisitions and highlights differences
Source code	Displays time-correlated source code and inverse assembly simultaneously in a split display
	Define the trigger event by simply clicking on a line of source code
	Obtain source-code-level views of dynamically loaded software or code moved from ROM to RAM during a boot-up sequence using address offsets
	Requires access to source files via the LAN or instrument hard drive to provide source code correlation
	Source correlation does not require any modification or recompilation of your source code
Eye scan	Displays eye diagrams across all buses and signals simultaneously, allowing you to identify problem signals quickly
Data display	
Numeric bases for data display	Binary, hex, octal, decimal, signed decimal (two's complement), ASCII, symbols, and processor mnemonics
Symbolic support/object file format compatibility	
Number of symbols/ranges	Unlimited (limited only by amount of virtual memory available on 16800 Series logic analyzers)
Object file formats supported	IEEE-695, Aout, Omf86, Omf96, Omf386, Sysrof, ELF/DWARF1 [1], ELF/DWARF2 [1], ELF/Stabs1, ELF/Stabs2, ELF/Mdebug Stabs, TICOFF/COFF, TICOFF/Stabs
ASCII	GPA (general purpose ASCII)
User defined symbols	Specify a mnemonic for a given bit pattern for a label or bus
Available data/file formats	
ala	Contains information to reconstruct the display appearance, instrument settings, and trace data (optional) that were present when the file was created
xml	Extensible markup language for configuration portability and programmability
csv	CSV (comma-separated values) format for transferring data to other applications like Microsoft Excel
mfb	Export logic analyzer data for post-processing. Mfb data can be parsed using programming tools
Standard analysis tools	
Filter/colorize	Show, hide, or color certain samples in a trace for easier identification and analysis
Find (next/previous)	Locate specific data in a captured trace

1. Supports C++ name de-mangling.

16800 Series Instrument Characteristics (Continued)

16800 Series PC characteristics		
Operating system	Microsoft Windows 7 Embedded (64-bit)	
Processor	Core 2 Duo, M890, 3.0 GHz microprocessor	
Chipset	Intel Q45	
System memory	4 GB	
Hard disk drive	500 GB	
Installed on hard drive	Operating system, latest revision of the logic and protocol application software, optional application software ordered with the logic analyzer	
16800 Series instrument controls		
LCD display	Large 38.1-cm (15-in.) display makes is easy to view a large number of waveforms or states (Touch screen available via Option 103)	
Front-panel hot keys	Dedicated hot keys for selecting run mode and disabling touch screen (if ordered)	
Front-panel knob	General-purpose knob adjusts viewing and measurement parameters	
Keyboard and mouse	PS/2 keyboard and mouse (shipped standard)	
16800 Series video display modes		
Available touch-screen display	Size	38.1 cm (15 in.) diagonal
	Resolution	1024 x 768
External display	Simultaneous display capability	Front panel and external display can be used simultaneously at 1024 x 768 resolution
	Supports up to four external monitors at up to 1600 x 1200 (with PCI video card)	

Programmability

You can write programs to control the logic analyzer application from remote computers on the local area network using COM or ASCII.

The COM automation server is part of the logic analyzer application. This software allows you to write programs to control the logic analyzer. All measurement functionality is controllable via the COM interface.

The B4608A Remote Programming Interface (RPI) lets you remotely control a 16800 Series logic analyzer by issuing ASCII commands to the TCP socket on port 6500. This interface is designed to be as similar as possible to the RPI on 16700 Series logic analysis systems, so that you can reuse existing programs.

The remote programming interface works through the COM automation objects, methods, and properties provided for controlling the logic analyzer application. RPI commands are implemented as Visual Basic modules that execute COM automation commands, translate their results, and return proper values for the RPI. You can use the B4606A advanced customization environment to customize and add RPI commands.

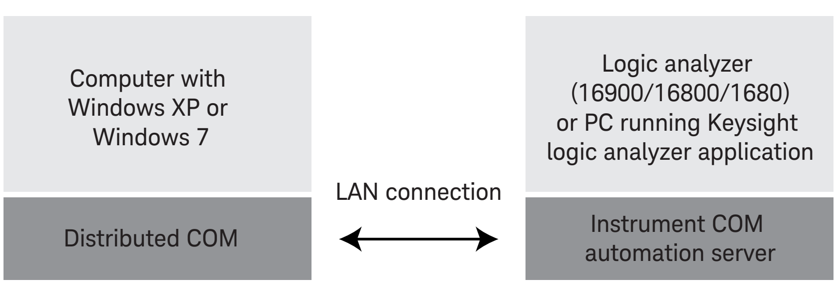


Figure 6. 16800 Series programming overview.

16800 Series Interfaces

Peripheral interfaces	
Display	15-pin XGA connector, DVI
Keyboard	PS/2
Mouse	PS/2
Serial	9-pin D-sub
PCI card expansion slot	1 full profile
USB	Six 2.0 ports, two in front, four in rear
Connectivity interfaces	
LAN	10Base-T, 100Base-T, 1000Base-T
Connector	RJ-45
Interface with external instrumentation	
Trigger or arm external devices or receive signals that can be used to arm measurement hardware within the logic analyzer with Trigger In/Out	
Trigger in	
Input	Rising edge or falling edge
Action taken	When received, the logic analyzer takes the actions described in the trigger sequence step
Input signal level	± 5 V max
Threshold level	Selectable: ECL, LVPECL, LVTTL, PECL, TTL
	User defined (± 5 V in 50 mV increments)
Minimum signal amplitude	200 mV
Connector	BNC
Input resistance	4 kΩ nominal
Trigger out	
Trigger	Rising edge or falling edge. OR of selected events that cause Trigger Out (logic analyzer trigger or flags)
Output signal	VOH (output high level) 2.0 V min
	VOL (output low level) 0.5 V max
	Pulse width approx. 80 to 160 ns
Threshold level	LVTTL (3.3 V logic)
Signal load	50 Ω (For good signal quality, the trigger out signal should be terminated in 50 Ω to ground)
Connector	BNC

16800 Series Physical Characteristics

Dimensions

Power	
16801A	115/230 V, 48 to 66 Hz, 605 W max
16802A	115/230 V, 48 to 66 Hz, 605 W max
16803A	115/230 V, 48 to 66 Hz, 605 W max
16804A	115/230 V, 48 to 66 Hz, 775 W max
16806A	115/230 V, 48 to 66 Hz, 775 W max
16821A	115/230 V, 48 to 66 Hz, 775 W max
16822A	115/230 V, 48 to 66 Hz, 775 W max
16823A	115/230 V, 48 to 66 Hz, 775 W max

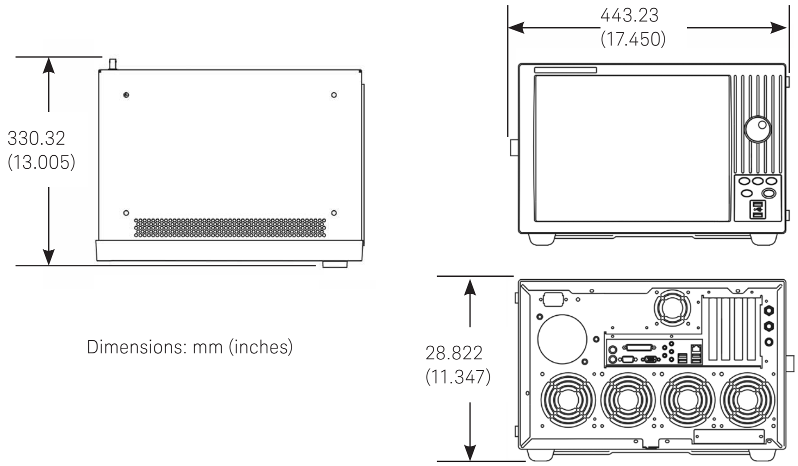


Figure 7. 16800 Series exterior dimensions.

Weight	Max net	Max shipping
16801A	12.9 kg (28.5 lbs)	19.7 kg (43.5 lbs)
16802A	13.2 kg (28.9 lbs)	19.9 kg (43.9 lbs)
16803A	13.7 kg (30.3 lbs)	20.5 kg (45.3 lbs)
16804A	14.2 kg (31.3 lbs)	21.0 kg (46.3 lbs)
16806A	14.6 kg (32.1 lbs)	21.4 kg (47.1 lbs)
16821A	14.2 kg (31.2 lbs)	20.9 kg (46.2 lbs)
16822A	14.2 kg (31.6 lbs)	21.1 kg (46.6 lbs)
16823A	14.5 kg (32.0 lbs)	21.3 kg (47.0 lbs)

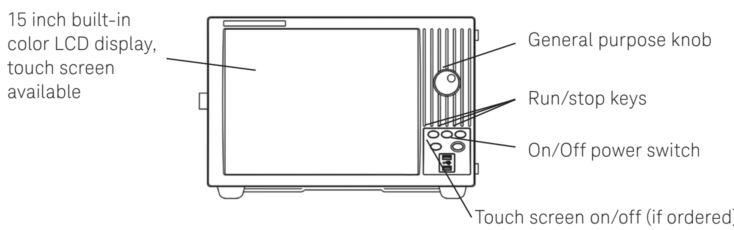


Figure 8. 16800 Series front panel.

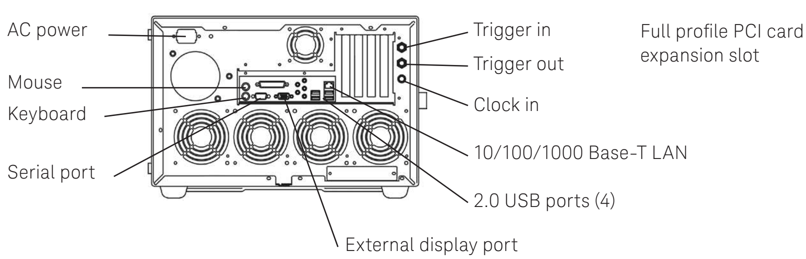


Figure 9. 16800 Series back panel.

Instrument operating environment	
Temperature	0° C to 50° C (32° F to 122° F)
Altitude	To 2000 m (6,561 ft)
Humidity	8 to 80% relative humidity at 40° C (104° F)

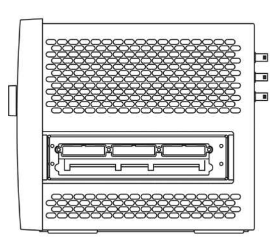


Figure 10. 16800 Series side view.

16800 Series Accessories

Keysight 1184BZ testmobile

The Keysight 1181BZ testmobile gives you a convenient means of organizing and transporting your logic analysis system mainframes and accessories.

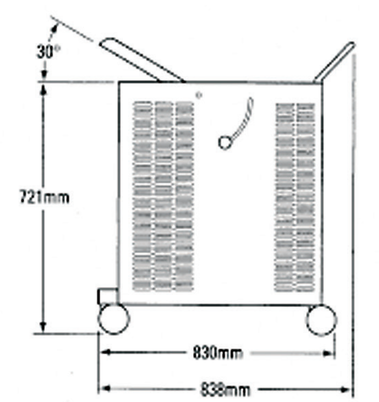
The testmobile includes the following:

- Heavy-duty casters make moving instruments easy
- Includes a steel buckle and nylon strap to secure instruments to the cart
- Total load capacity: 226.8 kg (200 lbs)

Weight	
1181BZ	Max net: 44.5 kg (98 lbs)

Optional accessories	
35181E	Antistatic mat for work surface
35181HZ	Testmobile printer/plotter stand
35181J	Storage drawer, 3.5 inch (89 mm)
35181KZ	Testmobile work surface
35181M	Testmobile drawer, 5.25 inch (133 mm)

Figure 11. Keysight 1181BZ testmobile cart.



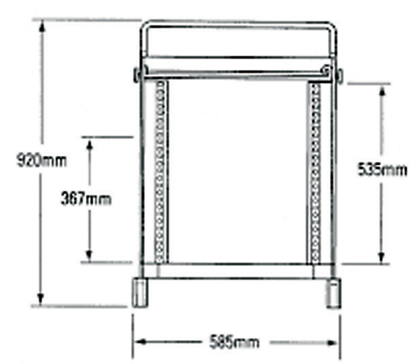


Figure 12. Keysight 1181BZ testmobile cart dimensions.

16800 Series Accessories (Continued)

Rack accessories

Stationary shelf

This light-duty fixed shelf is designed to support 16800 Series logic analyzers. The shelf can be used in all standard Keysight racks. The stationary shelf is mounted securely into place using the supplied hardware and is designed to sit at the bottom of the EIA increment. Features of the stationary shelf include:

- Snap-in design for easy installation
- Smooth edges

Sliding shelf

The sliding shelf provides a flat surface with full product accessibility. It can be used in all Keysight racks to support 16800 Series logic analyzers. The shelf and slides are preassembled for easy installation. Features of the sliding shelf include:

- Snap-in design for easy installation
- Smooth edges

Consider purchasing the steel ballast (C2790AC) to use with the sliding shelf. The ballast provides anti-tip capability when the shelf is extended.

Figure 13. Sliding shelf installed in rack.

Specifications

	J1520AC	J1526AC
Material	Cold-rolled steel	Cold-rolled steel
Weight	8 kg (17.6 lbs)	9.9 kg (22 lbs)
Color	Quartz gray	Quartz gray
Length	678 mm (26.7 in)	723.9 mm (28.5 in)
Height	44 mm (1.73 in)	44.5 mm (1.75 in)
Width	444 mm (17.5 in)	482.6 mm (19 in)
Load capacity	68 kg (150 lbs)	Capacity 68 kg (150 lbs)
EIA units	1	2
Contains	1 stationary shelf	1 sliding shelf
	2 rear brackets	2 rear brackets
	Mounting hardware	1 cable strap
		Mounting hardware

Figure 14. Stationary shelf (J1520AC).

Figure 15. Sliding shelf (J1526AC).

Ordering Information

Each 16800 Series portable logic analyzer comes with one PS/2 keyboard, one PS/2 mouse, accessory pouch and power cord standard.

Selecting a logic analyzer to meet your application and budget is as easy as 1, 2, 3.

1 Choose measurement capability
Logic analyzer
Logic analyzer with 48-channel pattern generator

2 Choose the channel count				
34 channels	68 channels	102 channels	136 channels	204 channels
16801A	16802A	16803A	16804A	16806A
16821A	16822A	16823A	–	–

3 Choose the memory depth and state speed	
Memory depth (samples)	1 M: <Model number>-001
	4 M: <Model number>-004
	16 M: <Model number>-016
	32 M: <Model number>-032
State speeds	250 MHz: <Model number>-250
	450 MHz: <Model number>-500 [1]

1. Applies to 68, 102, 136 and 204 channel models.

Additional 16800 Series options

Keysight product or option number	Description	Ordering information
16800A-103 [1]	Add touch screen	Must be ordered at time of purchase
16800A-109 [2]	External removable hard drive	Must be ordered at time of purchase
E5862A	Additional external hard drive	

1. Option 16800A-102, which provides a “Front panel with 15 inch display” is automatically included as part of the base product and is a no charge option. If you select Option 16800A-103, the “non-touch screen” 15 inch display that would normally ship in the logic analyzer is replaced by a “touch screen” 15 inch display.
2. Option 16800A-101, which provides a “Standard internal hard drive for 16800 series logic analyzers”, is automatically included as part of the base product and is a no charge option. If you select Option 16800A-109, the hard drive that would normally ship internal to the logic analyzer is shipped in an external enclosure.

All models of 16800 family portable logic analyzers come automatically with the no charge option 16800A-111 which provides a “Standard Configuration”.

16800 Series Probing Options

16800 Series logic analyzer probes	
Logic analyzer probes are ordered separately. Please specify probes when ordering to ensure the correct connection between your logic analyzer and the device under test.	General-purpose flying lead – 17-ch E5383A
	Connector probes – Mictor: 34-ch E5346A – Samtec: 34-ch E5385A
	Connectorless probes – 34-ch E5394A soft touch – 17-ch E5396A soft touch – 34-ch E5404A pro-series soft touch

Pattern generator clock and data pods	
For models with a pattern generator, order at least one clock pod and at least one data pod for every 8 output channels.	TTL/CMOS – 16720A-011 TTL clock pod and lead set – 16720A-012 3-state TTL/3.3-V data pod and lead set – 16720A-013 3-state TTL/CMOS data pod and lead set – 16720A-014 TTL data pod and lead set
	2.5 V – 16720A-015 2.5-V clock pod and lead set – 16720A-016 2.5-V data pod and lead set
	3.3 V – 16720A-017 3.3-V clock pod and lead set – 16720A-018 3.3-V 3-state data pod and lead set
	ECL – 16720A-021 ECL clock pod and lead set – 16720A-022 ECL data pod and lead set – 16720A-023 ECL unterminated data pod and lead set
	5 V PECL – 16720A-031 5-V PECL clock pod and lead set – 16720A-032 5-V PECL data pod and lead set
	LVPECL – 16720A-033 LVPECL clock pod and lead set – 16720A-034 LVPECL data pod and lead set
	1.8 V – 16720A-041 1.8-V clock pod and lead set – 16720A-042 1.8-V data pod and lead set
	LVDS – 16720A-051 LVDS clock pod and lead set – 16720A-052 LVDS data pod and lead set

16800 Series Probing Options (Continued)

Upgrade memory depth or state speed after purchase					
Logic analyzer channels	34	68	102	136	204
Logic analyzer models	16801A, 16821A	16802A, 16822A	16803A, 16823A	16804A	16806A
After purchase upgrade models	E5876A	E5877A	E5878A	E5879A	E5880A
Memory depth (samples)	4 M: <After-purchase model number>-004 16 M: <After-purchase model number>-016 32 M: <After-purchase model number>-032				
State speed	450 MHz: <After-purchase model number>-500 [1]				

1. Applies to 68, 102, 136 and 204 channel models.

Related literature

Publication title	Publication number
16800 Series Logic Analyzers - Color brochure	5989-5062EN
Considerations When Selecting a Logic Analyzer - Application note	5989-5138EN
16900 Series Logic Analysis Systems - Color brochure	5989-0420EN
Measurement Modules for the 16900 Series - Data sheet	5989-0422EN
B4655A FPGA Dynamic Probe - Data sheet	5989-0423EN
Probing Solutions for Keysight Technologies Logic Analyzers - Catalog	5968-4632E

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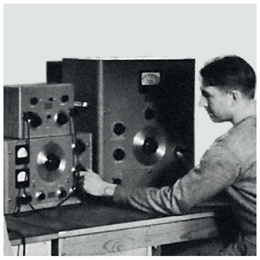
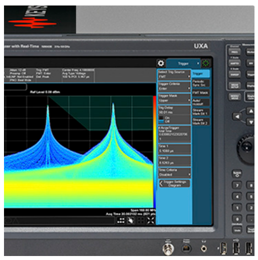


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